

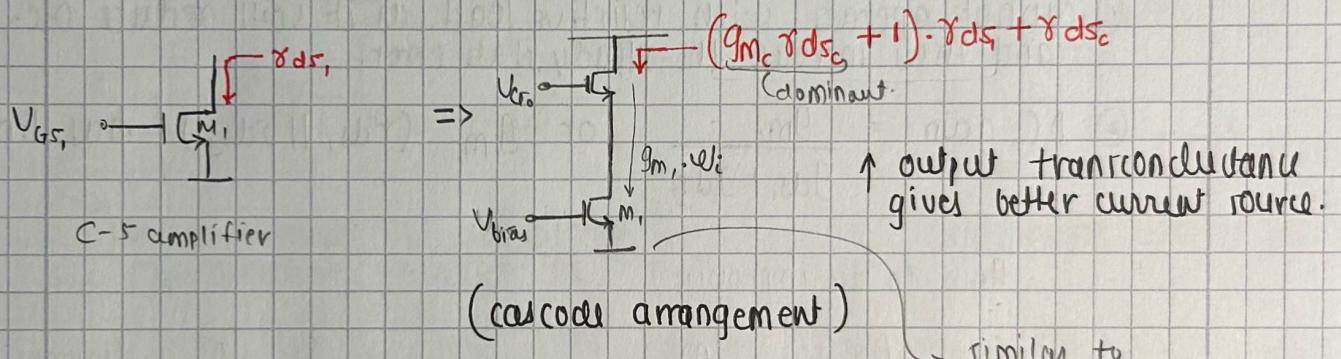
We had transconductance of g_m , and o/p conductance = $g_{ds_1} + g_{ds_2}$
 in order to increase the dc gain; we said we need to reduce the output conductance.

* we know, if we have a current source, we can optimize that by using a current buffer (common gate).

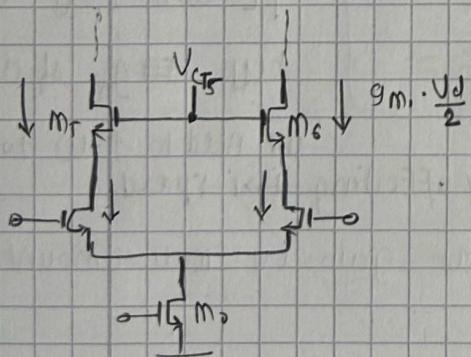
We can use this logic to increase the gain of our circuit.

↪ active load / current mirror (M_3, M_4) looks like a current source

so does the differential pair (M_1, M_2) and both need current buffers.

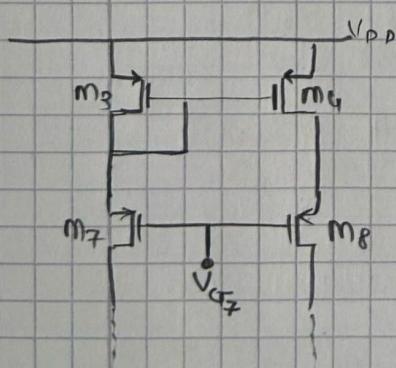


* implementing the sum in our op-amp:



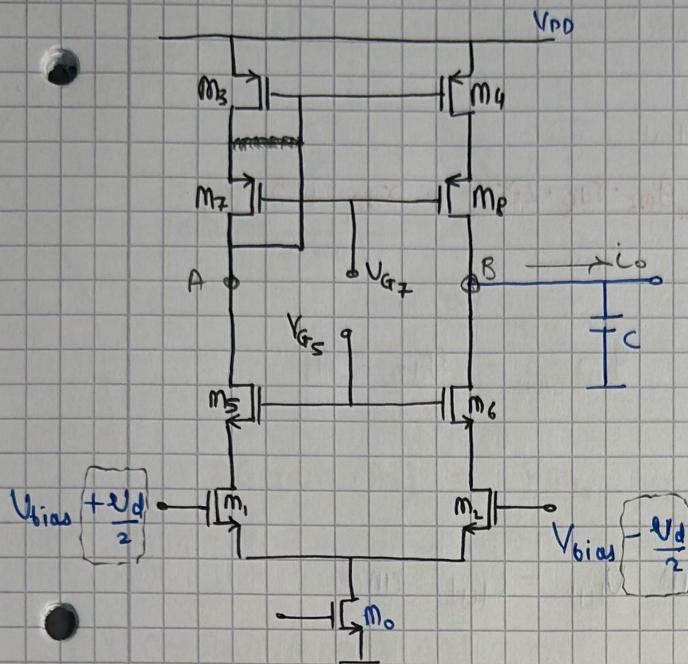
This gives us sum current $g_m \cdot V_d / 2$ but with much higher output resistance.

V_{GS_1} and V_{GS_2} are such that all the mosfets are in saturation.



→ P.T.O.

* Telescopic (cascode) Amplifier:



As before, even though the circuit is asymmetrical, if we terminate V_{out} node by V_{term} which is $= V_{DD} - V_{SD_8}$ tail node voltage (U_f) ≈ 0

now, in quiescent condition, when both inputs are at V_{bias} ,

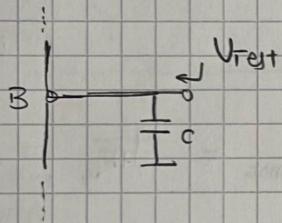
because of symmetry $U_A = U_B = V_{DD} - V_{SG_3}$

and $i_O = 0$

and when we apply $\pm U_{in}$ there will be some current at output node.

\therefore when we apply $\pm U_d/2$; $i_{tot} = g_{m_1} \cdot U_d$

* Output impedance or conductance;



we apply V_{test} and measure i_{test} by taking

$\frac{V_{test}}{i_{test}}$ we can find output resistance.

\hookrightarrow assume n-mos contribute ideal g_{mr} and $g_{dr} = 0$ and calculate for p-mos and then assume p-mos contributions ideal and calculate for n-mos and finally add them up.

for $Z_{out,pmos}$; assume $g_{ds,nmos} = 0$.

\therefore looking up from output node;

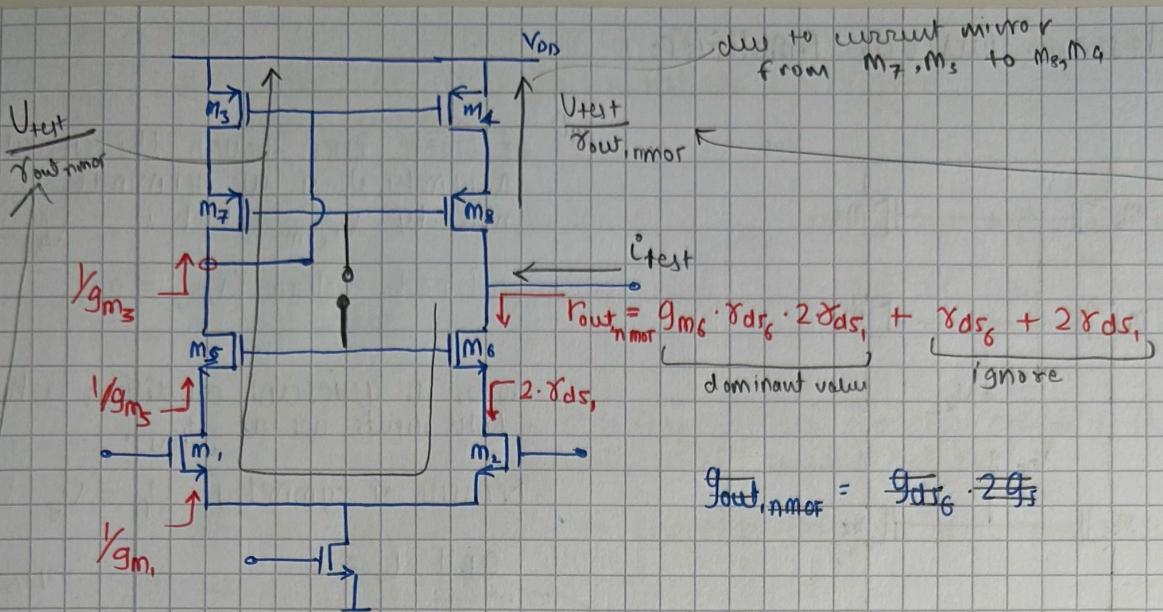
$$R_{out} = \underbrace{g_{m_p} r_{ds_2} r_{ds_4}}_{pmos} + \underbrace{r_{ds_2} + r_{ds_4}}_{\text{dominant.}} \quad (\text{ignore.})$$

$$g_{out} = \frac{1}{R_{out,pmos}} = \frac{g_{dr_4} g_{ds_2}}{g_{m_p}}$$

looking down from output node; assume $g_{ds,pmos} = 0$

$$r_{out} = ?$$

\rightarrow P.T.O.



total current drawn from $V_{\text{test}} = i_{\text{test}}$ and

$$i_{\text{test}} = \frac{V_{\text{test}}}{r_{\text{out}, \text{nmos}}} + \frac{V_{\text{test}}}{g_{\text{out}, \text{nmos}}} \\ = 2 \times \frac{V_{\text{test}}}{g_{m_6} \cdot r_{d_{s_6}} \cdot 2 \gamma_{d_{s_6}}}$$

$$i_{\text{test}} = \frac{V_{\text{test}}}{r_{\text{out}, \text{nmos}}} \quad \therefore \frac{1}{r_{\text{out}, \text{nmos}}} = \frac{1}{g_{m_6}}$$

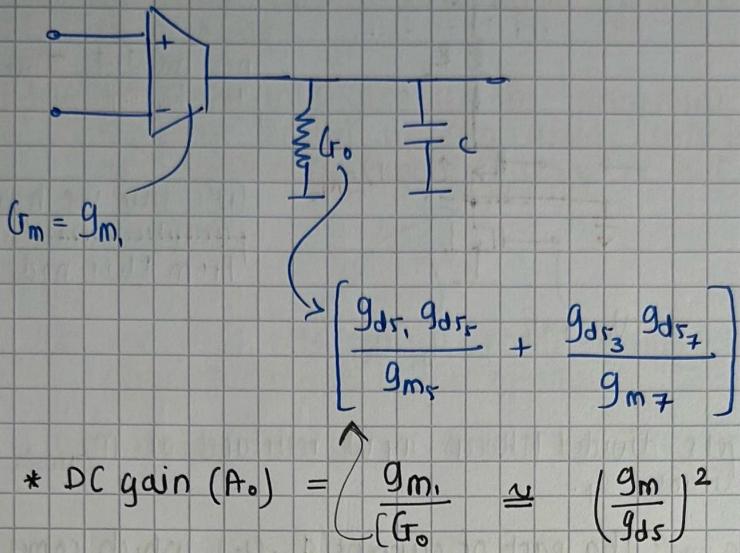
$$\therefore g_{\text{out}, \text{nmos}} = \frac{g_{m_6} \cdot g_{d_{s_6}} \cdot g_{d_{s_6}}}{g_{m_6}}$$

$$\therefore G_{\text{out, total}} = g_{\text{out, pmos}} + g_{\text{out, nmos}}$$

$$G_{\text{out}} = \frac{g_{d_{s_4}} \cdot g_{d_{s_8}}}{g_{m_8}} + \frac{g_{d_{s_6}} \cdot g_{d_{s_6}}}{g_{m_6}} \quad \left(\text{also } g_{m_6} \text{ and } g_{d_{s_6}} = g_{m_6} \text{ and } g_{d_{s_5}} \right)$$

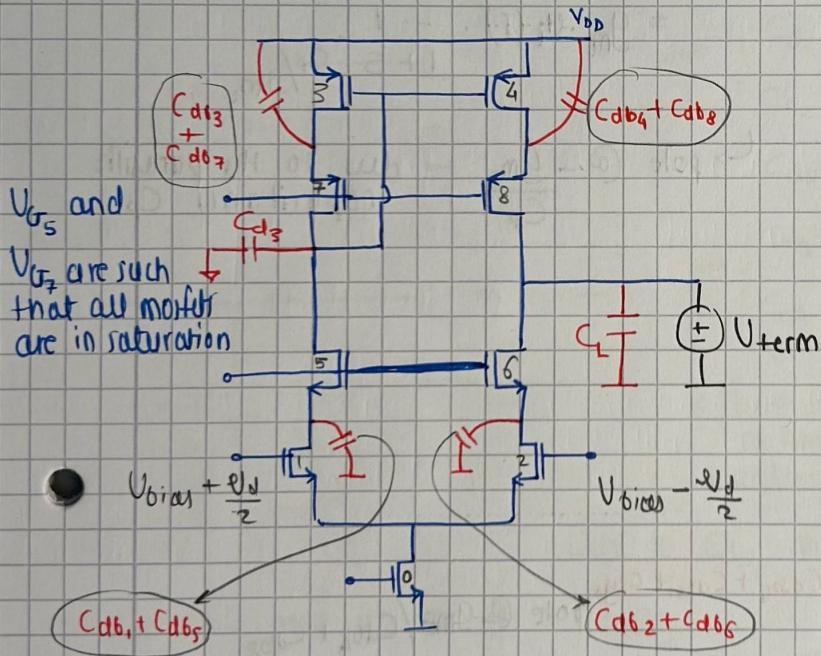
* Earlier, we had $(g_{d_{s_3}} + g_{d_{s_5}})$ as G_{out} of signed single stage opamp
now, we have reduced G_{out} significantly.
consequently giving us much higher DC gain.

* Also called as single stage cascode op-amp:



* If we connect the resistive load at output, it will not be any better than previous op-amp.

* Obtaining poles and zeros:



as usual, we will calculate trans-admittance by terminating Vout node with V_{term}

with every node we'll have parasitic capacitance.

but primary parasitic was C_{d_3} which consists of;

$$C_{d_3} = C_{g_{s_3}} + C_{g_{s_4}} + C_{d_{10_7}} + C_{d_{10_5}}$$

any parasitic such as $C_{d_{10_8}} + C_{d_{10_9}}$ would be absorbed into load. cap.

first let's ignore parasitics which are green-circled. Now, the effect of C_{d_3} will be same as before.

if we apply $\pm V_{dd}/2$ at nodes 3 and 7, we get a current of $\pm g_m \frac{V_{dd}}{2}$

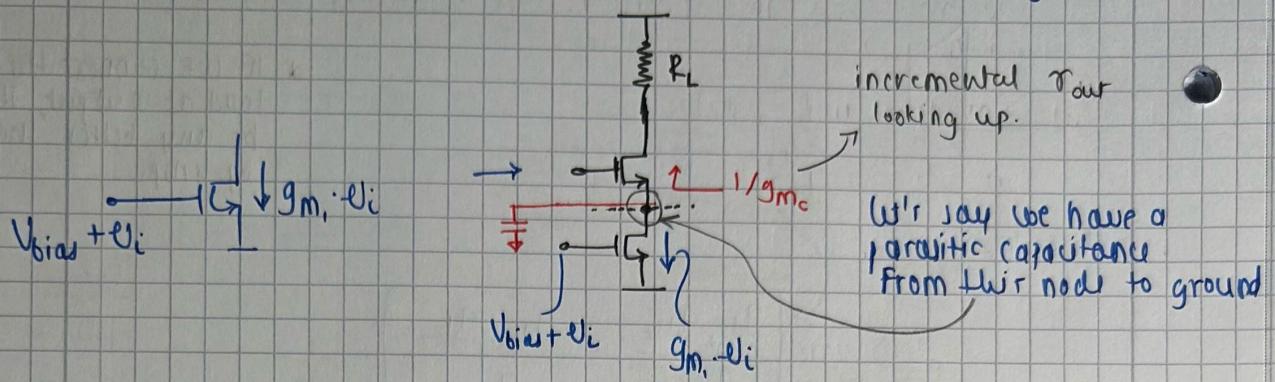
but at high frequencies, current from node 3 directly goes into C_{d_3} and does not get mirrored.

\therefore we will have pole and zero doublet just like before.

we have $P_2 @ \frac{g_{m_3}}{C_{d_3}}$ and $Z_1 @ \frac{2 g_{m_3}}{C_{d_3}}$

non-dominant pole.

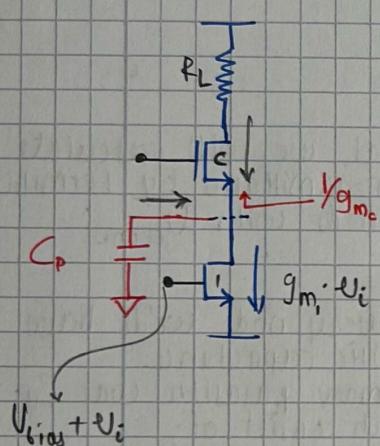
* Let's analyze in layman terms about the contribution of green-circled parasitics by taking a look at a simple cascode stage.



incremental T or
looking up.

We say we have a
parasitic capacitance
from this node to ground

so, the current gets divided between input resistance of $m_{cascode}$ and the parasitic capacitance C_p .



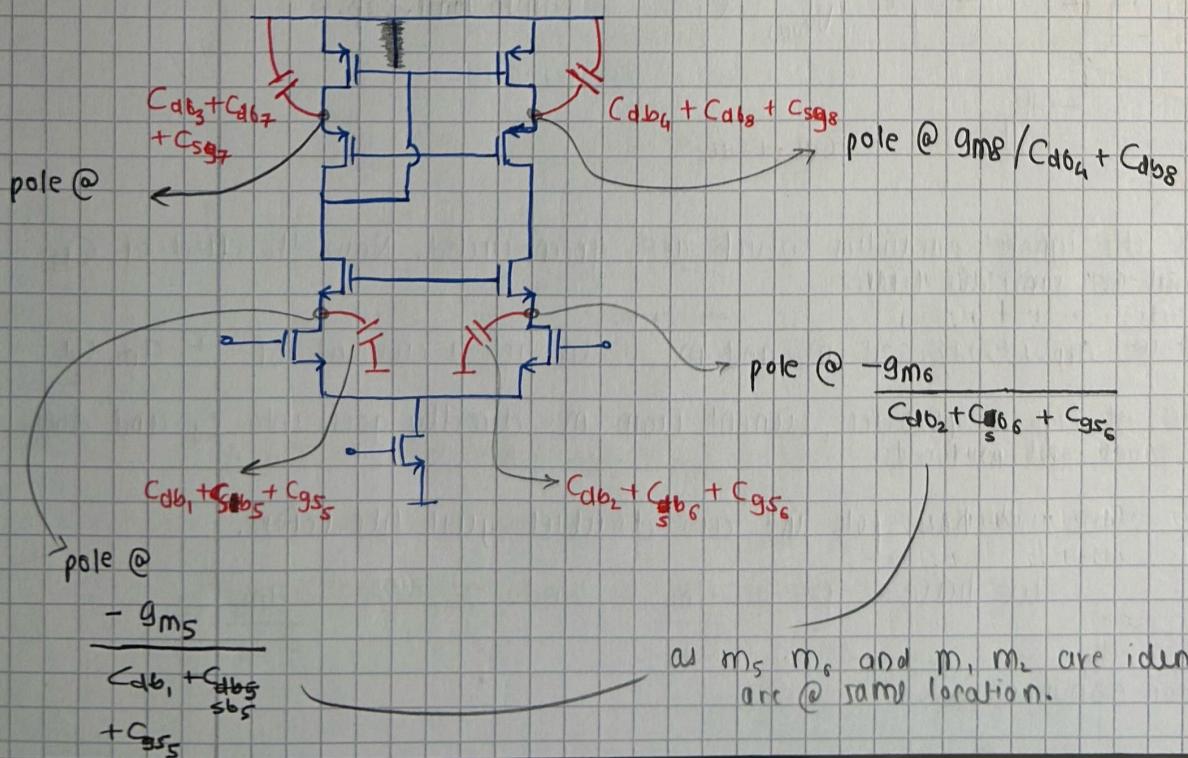
: The part of current ($g_m \cdot U_i$) which comes out from m_c is;

$$g_m \cdot U_i(s) \cdot \frac{g_m}{g_m + sC_p}$$

$$= g_m \cdot U_i(s) \cdot \frac{1}{1 + s \cdot C_p/g_m}$$

\hookrightarrow pole @ $-\frac{g_m}{C_p}$ due to the parasitic capacitance C_p .

In our structure;



Hence, there will be lots of poles and zeros associated with each node.

∴ we make use of a simulator, in order to take all poles and zeros in account.

(ii) Simulator will give us the magnitude and phase and by looking at the phase margin we can decide whether these poles and zeros are at sufficiently high frequency or not.

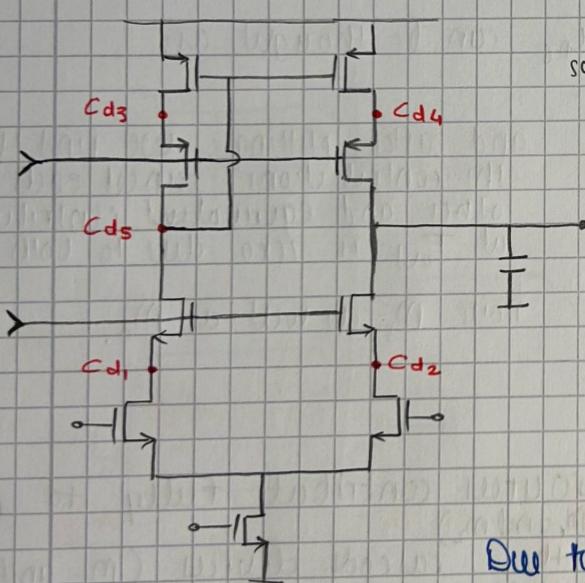
| Vdo 34 |

So, we saw telescopic cascode opamp. Let's determine some more characteristics of this op-amp.

We already evaluated the DC gain $A_0 = \frac{g_{m1}}{G_{out}} \approx \left(\frac{g_{m1}}{g_{ds}} \right)^2$

↪ dominant pole @ G_{out}/C

* Now the concern for stability is the non-dominant poles and zeros:



$$\begin{aligned} & \text{some } \left\{ \begin{array}{l} C_{d1} = C_{db1} + C_{sb5} + C_{gs5} \\ C_{d2} = C_{db2} + C_{sb6} + C_{gs6} \end{array} \right\} \begin{array}{l} - g_{m5}/C_{d1} \\ - g_{m5}/C_{d2} \end{array} \\ & C_{d5} = C_{db5} + C_{sb7} + 2C_{gs5} \\ & \text{some } \left\{ \begin{array}{l} C_{d3} = C_{db3} + C_{sb7} + C_{gs7} \\ C_{d4} = C_{db4} + C_{sb8} + C_{gs8} \end{array} \right\} \begin{array}{l} - g_{m7}/C_{d3} \\ - g_{m7}/C_{d4} \end{array} \end{aligned}$$

* There is a feedback loop around M_3 and M_7 so that gives us some modification in pole values related to that node.

Due to C_{ds} there will be a pole @ $\frac{-g_{m3}}{C_{ds}}$

and a zero @ $2 \times \frac{-g_{m3}}{C_{ds}}$

poles

* These parasitics act only on half of the current. Only the current from M_1 gets mirrored on M_4 and goes through pole due to C_{d4} but current from M_2 doesn't end up giving zeros as well.

TIMP

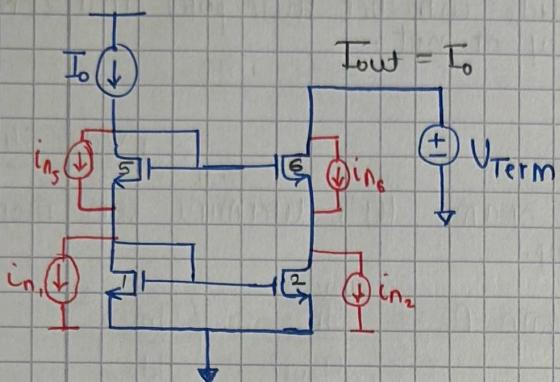
∴ we say there will be lots of parasitic poles and zeros and they will be analyzed in freq. response using simulator.

Effect of all of these poles and zeros should be such that we get adequate phase margin.

* Noise and offset:

Let's take an example current mirror and derive some results which we can use further for our cascaded op-amp.

V_{term} is such that $I_{out} = I_o$

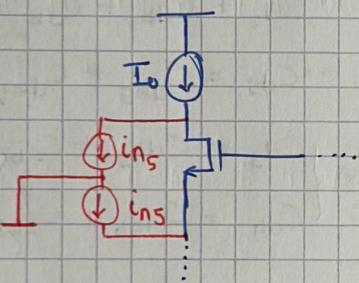


- * first let's take noise due to M_2 : we can simply see that all of i_{n2} comes through I_{out} . \therefore all of i_{n2} appears at output.

	In, out
M_2	i_{n2}
M_1	i_{n1}
M_5	0
M_6	0

- * talking about i_{n1} , due to M_1 ; all of i_{n1} gets mirrored onto M_2 and also contributes fully to the I_{out} .

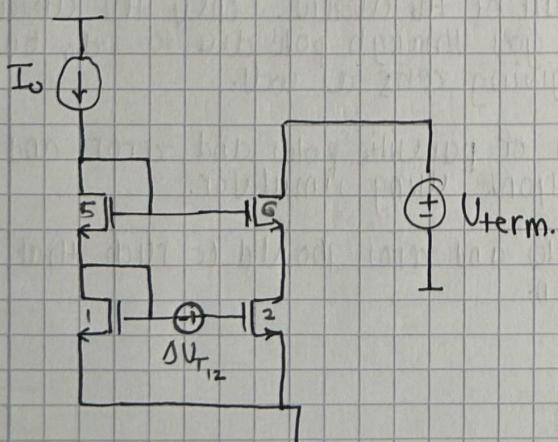
- * noise i_{n1} and i_{n2} can be thought as:



and after splitting; we find that the contributions cancel each other and equivalent contribution at I_{out} is zero due to both noise M_1 as well as M_2 .

Conclusion: Main current source contributes fully to the output, and the cascode devices (M_5 and M_6) do not contribute anything to the output noise.

* Offset or mismatch:



So, when we have mismatch between M_1 and M_2 , M_1 will have some ΔU_{T12} which will correspond to I_o now the ΔU_{T12} of M_2

is different from M_1 by $1/\Delta U_{T12}$

\therefore current in M_2 will be some what different from M_1 ,

by $\Delta U_{T12} \cdot g_{m2}$

* We know, we can model a current factor error as a current source in parallel with the mosfet.

This analysis becomes same as the noise analysis.

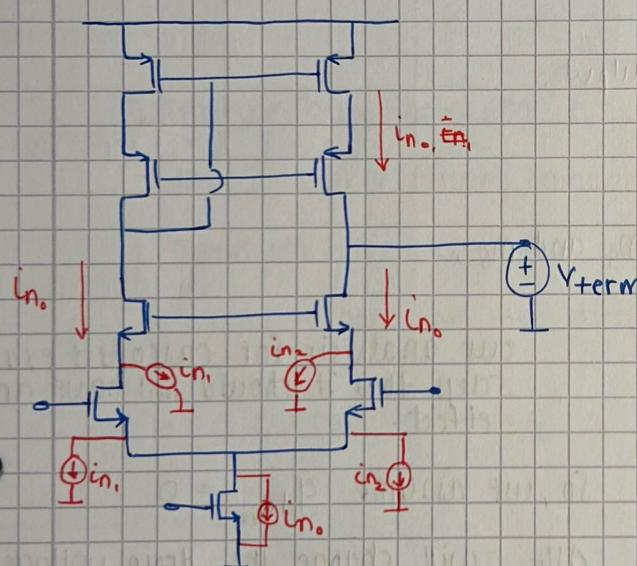
Mismatch

$$\begin{array}{l} m_1 \\ m_2 \end{array} \quad \rightarrow \quad \Delta V_{T_{12}} \cdot g_m \\ \begin{array}{l} m_5 \\ m_6 \end{array} \quad \rightarrow \quad 0 \quad \text{IMP}$$

Conclusion: both the noise and

mismatch errors are contributed by the main current mirror devices and there is zero contribution from cascode devices.

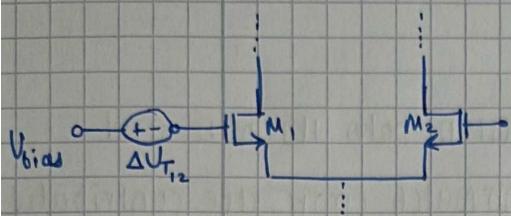
* We can apply these result to our telescopic cascode op-amp.



	$i_{n,out}$
m_0	0
m_1	i_{n1}
m_2	$-i_{n2}$
m_3	i_{n3}
m_4	$-i_{n4}$
m_5	0
m_6	0
m_7	0
m_8	0

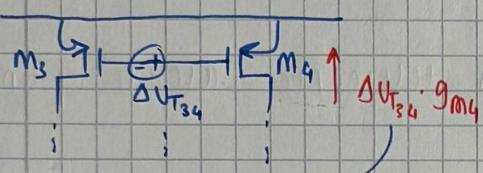
∴ resulting noise is exactly same as of single stage op-amp.

* Mismatch or offset: for simplicity, we will consider threshold voltage mismatch only.



If we consider mismatch in M_1 and M_2 , it will result in current $g_{m_1} \cdot \Delta V_{T_{T2}}$ and this current as discussed while deriving results for example circuit, will fully show up at $i_{out, mismatch}$.

now, if we consider mismatch betw M_3 and M_4 ,



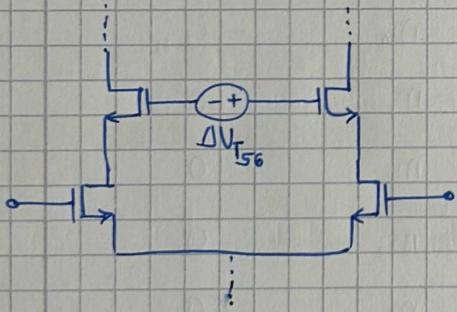
$$\Delta V_{T_{T2}} = -g_{m_1} \cdot \Delta V_{T_{T2}}$$

$$\Delta V_{T_{T34}} = -g_{m_4} \cdot \Delta V_{T_{T34}}$$

→ all of this is drawn from output.

VUEMP

* talking about mismatch in M_5 and M_6 ;



our analysis for cascoded example says that it should not have any effect.

$$\text{So, we assume } g_{ds_{T_{T12}}} = 0$$

$\Delta V_{T_{T56}}$ will change the drain voltage of M_1 and M_2 . This changes i_{ds} of

M_1 and M_2 but if $g_{ds_{T_{T12}}} = 0$ it means that the current in M_1 and M_2 will not respond to v_{ds} and the currents in M_1 and M_2 will exactly be the same as before. Same goes with M_7 and M_8 .

$$\Delta V_{T_{T56}}$$

$$g_m$$

$$\Delta V_{T_{T78}}$$

$$g_m$$

$$i_{out} = i_{A_1} - i_{A_2} + i_{n_3} - i_{n_4}$$

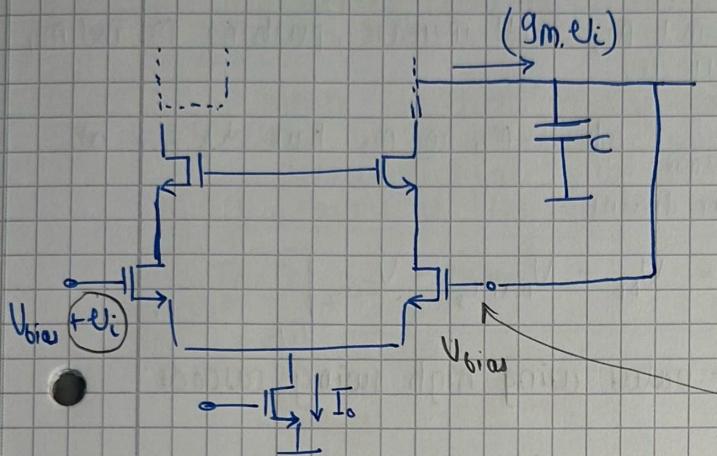
$$S_{out} = S_{in_1} + S_{in_2} + S_{in_3} + S_{in_4}$$

$$= \frac{16}{3} kT (g_{m_1} + g_{m_3})$$

$$S_{in} = \frac{S_{out}}{g_{m_1}^2} = \frac{16}{3} \frac{kT}{g_{m_1}} \left(1 + \frac{g_{m_3}}{g_{m_1}}\right)$$

$$\therefore \sigma_{V_{os}}^2 = \sigma_{V_{T_{12}}}^2 + \sigma_{V_{T_{24}}}^2 \cdot \left(\frac{g_{m_3}}{g_{m_1}} \right)^2$$

* Slew Rate:



if the input is at steady state
and is V_{bias} their voltage will also
be at V_{bias}

and after applying e_i their voltage
doesn't change suddenly due to ' C '.

When we keep increasing e_i , there will be a value of e_i for which, all
of the I_o will be flowing through M_1 and nothing will flow through M_2 .

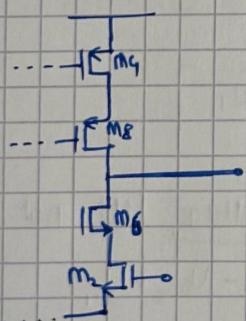
\therefore maximum rate of change of current in the direction: $\pm I_o/c$

similar goes for -ve direction: $-I_o/c$

$$\therefore \text{slew rate} = \pm \frac{I_o}{c}$$

— x — x —

* Swing limits:



if $V_{out} \uparrow$, M_8 squeezes. $\therefore V_{d_{\text{8}}} \uparrow$ can go up until but
not more than $1 \cdot V_{T_p}$ than $V_{G_{\text{8}}}$

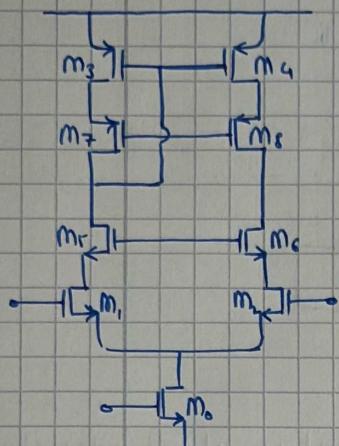
$$\therefore V_{out} < V_{G_8} + V_{T_p}$$

if $V_{out} \downarrow$, M_5 squeezes. $\therefore V_{d_5} \downarrow$ can go down but
not more than $1 \cdot V_{T_n}$ than V_{G_5}

$$\therefore V_{out} > V_{G_5} - V_{T_n}$$

\therefore We have to adjust V_{G_6} or V_{G_5} and V_{G_8} or V_{G_6} in order to get max. swing.

$$\therefore U_{G_5} - U_{T_5} < U_{out} < U_{G_7} + U_{T_7}$$



U_{G_7} should be maximized so that the upper limit is as large as possible.

as $U_{G_7} \uparrow$ beyond a certain value source terminal

of M_4 and M_5 will increase, pushing M_3 and M_6 into triode.

$\therefore U_{G_7 \max}$ where M_4 and M_5 have $V_{D,SAT}$ at their drains

$$\therefore U_{G_7 \max} = V_{DD} - V_{D,SAT_3} - V_{SG_7} \Big|_{I_{D/2}}$$

→ we can set U_{G_7} to this value using high swing cascade biasing technique

Now,

we would like to minimize U_{G_5} so that the lower limit is as small as possible.

as $U_{G_5} \downarrow$; source-terminal of M_3 and M_6 will \downarrow putting M_1 and M_2 into triode.

$\therefore U_{G_5 \min}$ is where M_1, M_2 have $V_{D,SAT}$ at their drains:

$$\therefore U_{G_5 \min} = V_{bias} - U_T + U_{GS_5} \Big|_{I_{D/2}}$$

* we also need to compute limits on V_{bias} :

$$V_{bias} > V_{DSAT_0} + U_{GS_1}$$

$\left(V_{DSAT_1} + U_{T_1} \right) \Big|_{I_{D/2}}$

(gate voltage of M_1 can go \uparrow by drain voltage but not more than U_{T_1})

$$V_{bias} < U_{G_5} + U_{GS_5} + U_{T_1}$$

$$\left(V_{DSAT_5} + U_{T_5} \right)$$