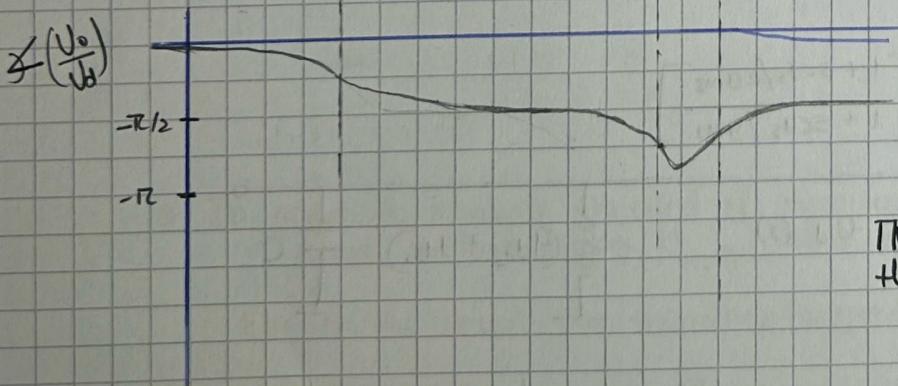
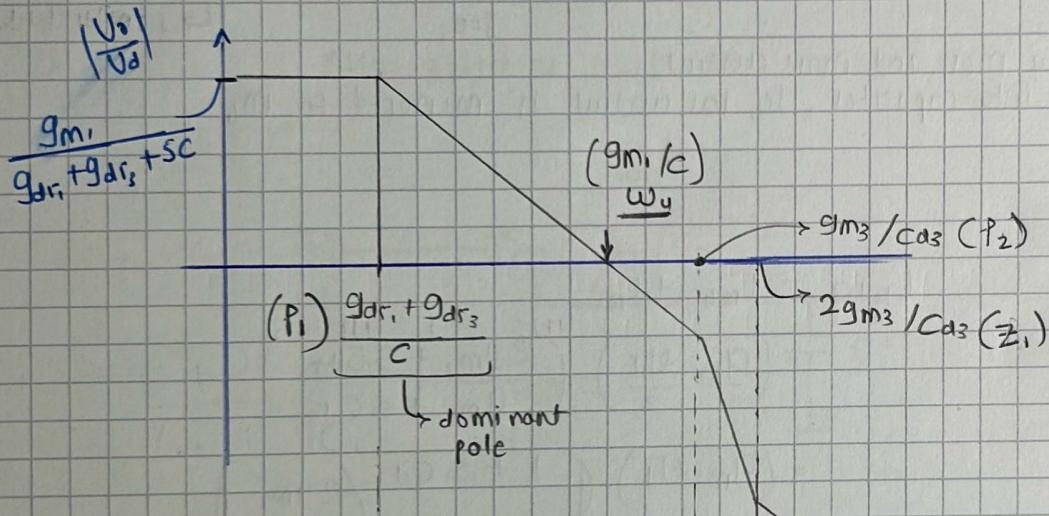


Let's look at bode plot for such frequency response.

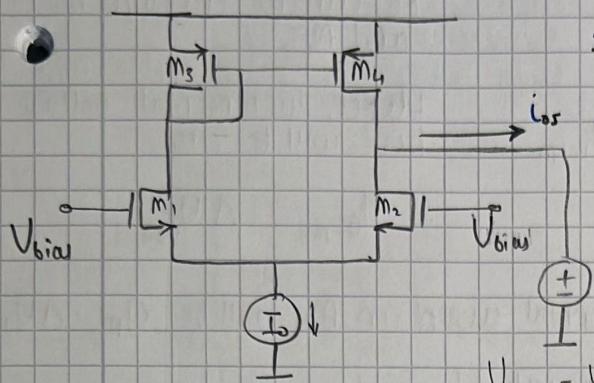


The phase lag never reaches  $-180^\circ$ . So, this is unconditionally stable.

\* We still need to calculate characteristics like large signal limits of the op-amp as well as non-ideal features like noise and offset.

\* Offset of the op-amp:

now  $m_1$  and  $m_2$  must be identical and  $m_3$  and  $m_4$  must be identical. But in reality, there will be some mismatch.



∴ we need to add appropriate sources to the circuit that represent the mismatch, find the output, and calculate the offset.

To avoid complexity due to unsymmetric injection of offsets into the circuit, we will assume  $g_{ds}$  to be very small. They won't affect the answer very much.

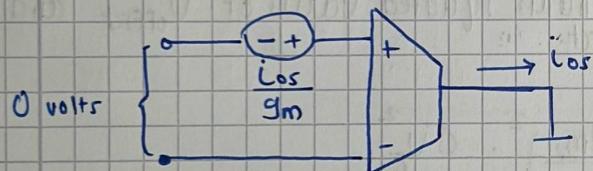
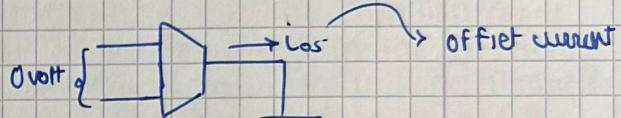
$$V_{term} = V_{DD} - V_{SG3}$$

We will also assume that, there is only a threshold voltage mismatch between mosfets.

The current  $i_{os}$  will be zero, but due to mismatch, it will be non-zero. Which means;

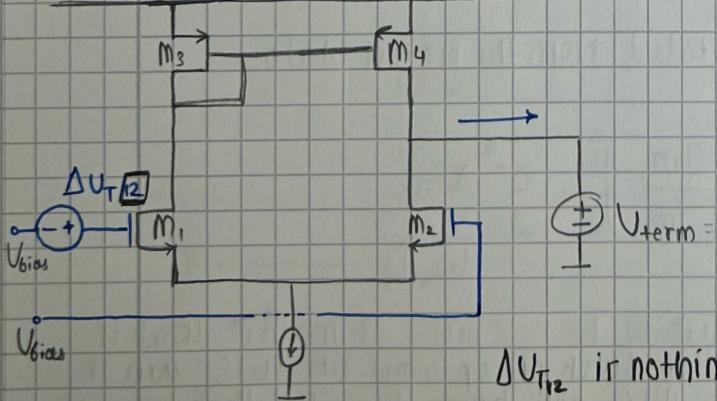


if we represent  $i_{os}$  as input voltage,



∴ we will first calculate  $i_{os}$  and then divide it by transcond. of the single stage op-amp circuit in order to get the input referred offset.

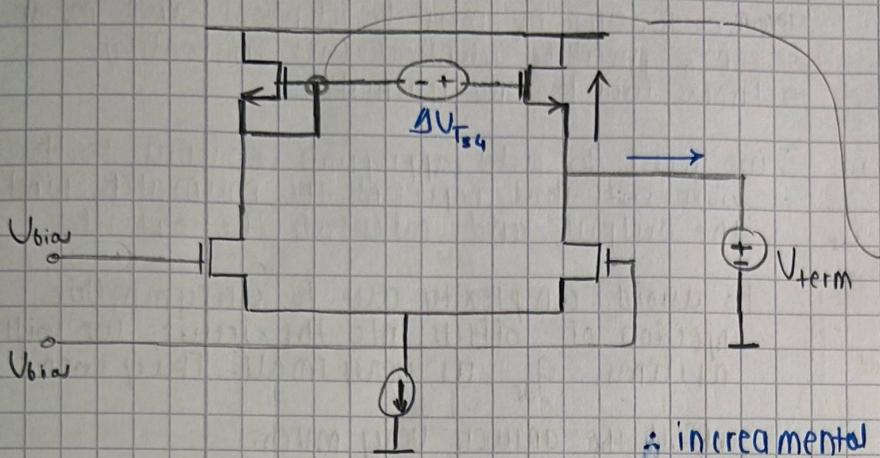
Now; we can see in the following circuit that any change in the  $V_T$  can be represented as equivalently a change in the gate-source voltage.



∴ So, mismatched  $V_T$  b/w  $m_1$ ,  $m_2$  will be represented equivalently as mismatch in gate-source voltage b/w  $m_3$  and  $m_4$ . means a series voltage source at gate of  $m_1$ .

$\Delta V_{T12}$  is nothing but the differential input to the op-amp

$$\therefore i_{os} = g_m \cdot \Delta V_{T12}$$



as, diff. input at  $M_1$  and  $M_2$  is zero, there will be no current through  $M_1$  and  $M_2$ .

Hence, incremental voltage here will be zero.

$$\therefore \Delta V_{G_S M_4} = \Delta V_{T_{34}}$$

$\therefore$  incremental current in  $M_4$  will be  $g_m \cdot \Delta V_{T_{34}}$

and that will go through  $V_{term}$ .

\* Hence, total  $i_{os} = g_m \cdot \Delta V_{T_{12}} - g_m \cdot \Delta V_{T_{34}}$

$$\therefore \text{Input referred offset voltage} = \frac{i_{os}}{g_m} = \Delta V_{T_{12}} - \frac{g_m}{g_m} \Delta V_{T_{34}}$$

offset due to mismatch in  $M_1$  and  $M_2$  appears directly in input referred  $V_{off}$ .

\* What we really want is the mean squared value of  $V_{off}$  and standard deviation of offset.

$$\overline{V_{off}^2} = \overline{V_{os}^2} = \overline{V_{T_{12}}^2} + \left( \frac{g_m}{g_m} \right)^2 \cdot \overline{V_{T_{34}}^2}$$

$$\overline{V_{os}^2} = \sqrt{\overline{V_{T_{12}}^2} + \left( \frac{g_m}{g_m} \right)^2 \cdot \overline{V_{T_{34}}^2}}$$

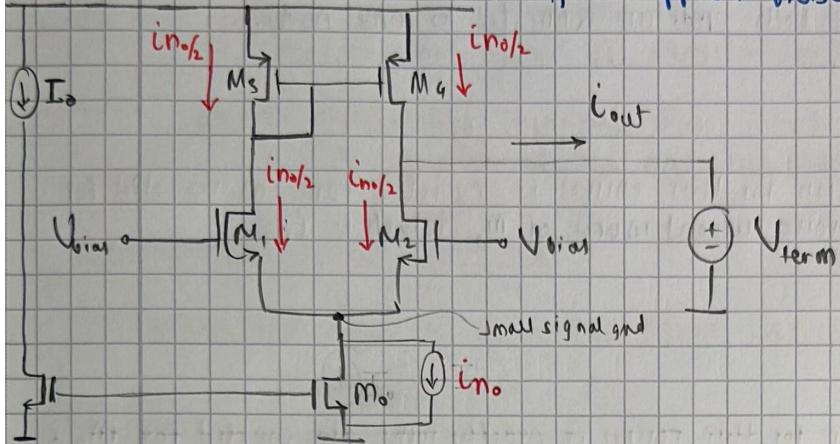
This can be further calculated from the process data

$$\overline{V_{os}^2} = \frac{A_{V_{Tn}}^2}{W_L} + \left( \frac{g_m}{g_m} \right)^2 \cdot \frac{A_{V_T}^2}{W_L L_3}$$

Basically, if  $\overline{V_{os}^2}$  comes out to be 2 mV. It means that if we make a million batch of op-amp like this, then if we measure  $V_{os}$  of all, 99% will have  $V_{off}$  less than 3 mV

## \* Single stage op-amp : 'Noire'

We'll calculate input referred noise of the circuit. As before, we will calculate  
 (i) output current going into  $V_{term}$  and from that calculate  
 the input referred noise.



Eq. Input referred noise

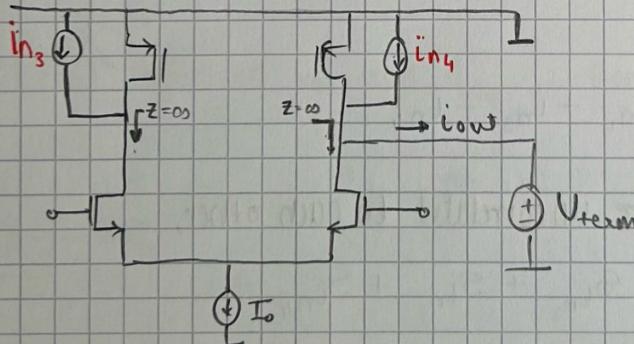
$$= \frac{i_{out}}{g_m}$$

assume  $g_{dr} = 0$

$i_{out}$

$M_0$  0 → In general if we inject something into the common mode node or the tail-node of the op-amp, in the differential output, its effect will be zero. because it will get symmetrically divided into  $M_1$  and  $M_2$ , and mirrored in  $M_3$  and  $M_4$ , giving net effect at  $i_{out}$  to be zero.

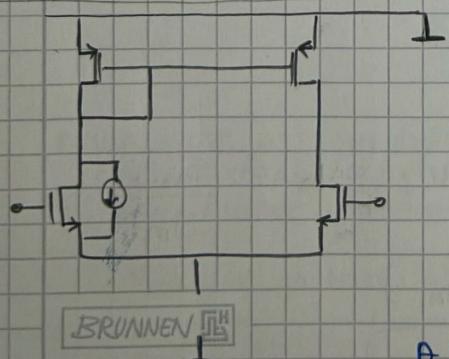
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all  $i_{in}$  show up at  $i_{out}$ .

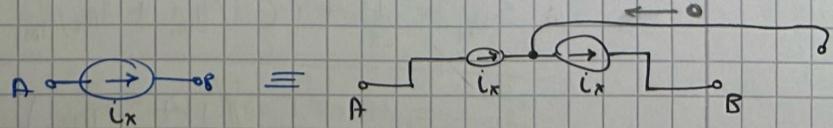
and  $i_{in3}$  seen as impedance looking into drain of  $M_1$  ∴ get reflected completely on  $M_4$  and appears at  $i_{out}$ .

$$\therefore i_{out} = -i_{in4} + i_{in3}$$



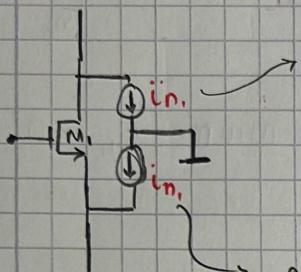
now, this  $i_x$  is connected b/w two nodes earlier  $i_{in}, i_{in3}, i_{in4}$  had one node to ground.

\* Trick: in any circuit, if we have a current source b/w A and B, we can replace that with a series combination of two sources of exactly same value.



If we take the floating node and connect it to any node in the circuit, it will not affect the circuit. Because current into that is zero due to identical  $i_{x_3}$

usually we connect the middle node to ground to analyse floating current sources. Where both ends are connected to same node.



analysing for this source is exactly same as we did for noise current source of  $M_3$ , which is  $i_{n_3}$

analysing for this source is exactly same as we did for  $M_3$ 's noise current source ( $i_{n_3}$ )

| $\therefore i_{\text{out}}$ |              |
|-----------------------------|--------------|
| $i_{n_1}$ (upper)           | $i_{n_2}$    |
| $i_{n_3}$ (lower)           | X no effect. |

It turns out that all of noise current source appears at the output node.

| $i_{n_2}$ (upper) - $i_{n_2}$ | } |
|-------------------------------|---|
| $i_{n_3}$ (lower) X           |   |

Exactly same thing happen in case of  $M_2$ . All noise current source due to  $M_2$  appear at output node.

$$\therefore i_{\text{out}} = i_{n_1} - i_{n_2} + i_{n_3} - i_{n_4}$$

as all these terms are uncorrelated to each other,

$$\begin{aligned} S_{i_{\text{out}}} &= S_{i_{n_1}} + S_{i_{n_2}} + S_{i_{n_3}} + S_{i_{n_4}} \\ &= \frac{8}{3} kT (g_{m_1} + g_{m_2} + g_{m_3} + g_{m_4}) \\ &= \frac{16}{3} kT (g_{m_1} + g_{m_3}) \end{aligned}$$

and input referred noise voltage source  $S_{v_{in}} = \frac{S_{i_{\text{out}}}}{g_{m_1}^2}$

$$\therefore S_{v_{in}} = \frac{16}{3} kT \left( \frac{1}{g_{m_1}} + \frac{g_{m_3}}{g_{m_1}^2} \right)$$

$$\boxed{S_{v_{in}} = \frac{16}{3} \frac{kT}{g_{m_1}} \left( 1 + \frac{g_{m_3}}{g_{m_1}} \right)}$$

\* If we look at the expression;  $SV_{in} = \frac{16}{3} \frac{kT}{g_m} \left( 1 + \frac{g_{m_3}}{g_m} \right)$   
 dominant part.

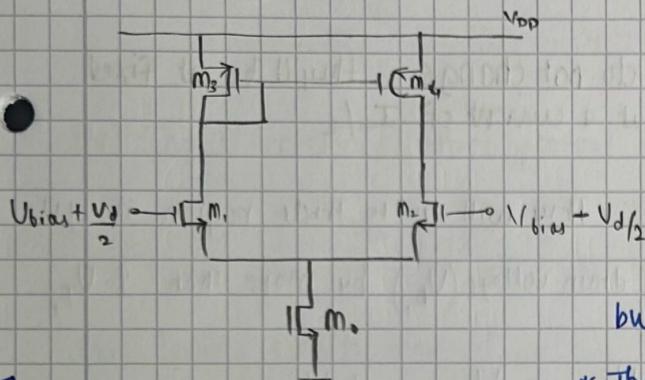
we know, if we refer the noise of mosfet to its input, it will be  $\frac{3}{3} \frac{kT}{g_m}$ .

→ representing noise as additive to  $V_{GS}$  instead to  $I_d$ .

and we have two transistors here, which have uncorrelated noise. Thus their spectral densities add up and we end up having  $\frac{16}{3} \frac{kT}{g_m}$ .

— x — x —

Now, we need to calculate large signal limits.



now, when the op-amp is working in negative feedback circuit,  $V_d$  is expected to be very small.

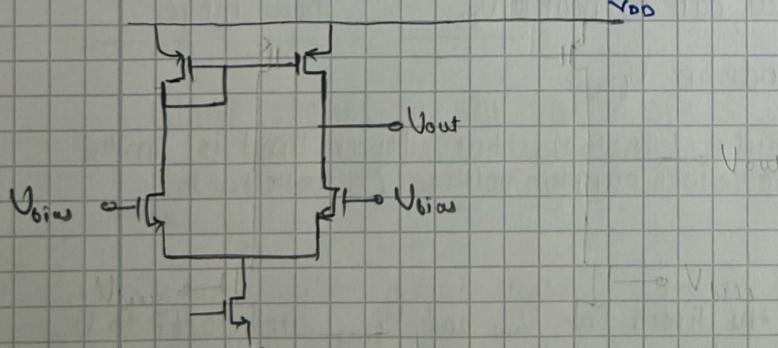
we assume that  $V_d$  is so small that it will not drag transistor into triode region.

but it will affect the output and  $V_{out}$  will be limited.

\* The  $V_{out}$  swing might push some transistor into triode region.

\* In an op-amp itself we can have different values of  $V_{bias}$ . ∵ we need to find out the limits of  $V_{bias}$  for which all transistors are in saturation region.

(i) find limits on  $V_{out}$  and  $V_{bias}$  : Assume  $V_d \approx 0$



$$V_{DSAT} = \sqrt{\frac{2 \cdot I_d}{M \cdot C_{ox} \cdot W/L}}$$

→ gate overdrive required for saturation.

\* When  $V_{out}$  increases,  $M_2$  will squeeze and its  $V_{ds}$  will reduce, pushing it to triode region.

\* when  $V_{out} \downarrow$  goes down, gate of  $M_2$  is @  $V_{bias}$  so as  $V_{out} \downarrow$ ,  $M_2$  will go further and further into triode region.

$$V_{out} < V_{dd} - V_{DSATM_2}$$

$$\sqrt{\frac{2 \cdot I_d/2}{M \cdot C_{ox} \cdot W^3/L^3}}$$

∴  $V_{out}$  can go below  $V_{bias}$  but not more than  $1 V_T$ ,

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$$V_{bias} - V_T < V_{out} < V_{dd} - V_{DSATM_2}$$

\* Limits on  $V_{bias}$ :

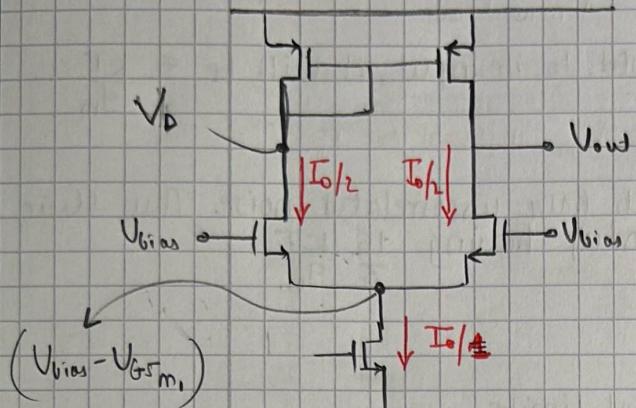
when there is no current flowing through  $V_{out}$  node,

$$\text{by symmetry } V_{out} = V_D$$

$\therefore$  as  $V_{bias}$  comes to low value,  $M_0$  squeezes and can go in triode region

$$V_{bias} > V_{GSM_0} + V_{DSAT_{M_0}}$$

$$V_{bias} > V_{T_{M_0}} + V_{DSAT_{M_0}} + V_{DSAT_{M_0}}$$



Now, the drain of  $M_0$  and  $M_1$  do not change, they'll be at fixed value of  $(V_D - V_{GSM_3})$  at a current of  $I_0/2$

$V_{bias}$  is at gate of  $M_0$  and  $M_1$   $\therefore$  they will go to triode region if gate voltage increased beyond the drain voltage ( $V_D$ ) by more than  $1 \cdot V_T$ ,

∴

$$V_{bias} < \underbrace{V_D - V_{T_3}}_{\text{drain voltage}} - V_{SAT_{M_3}} + V_{T_1}$$

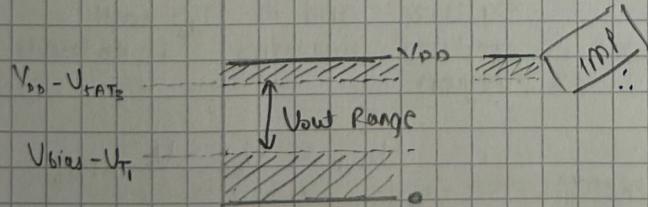
$$\left( \frac{V_{T_{M_1}} + V_{DSAT_{M_1}}}{I_0/2} \right) + V_{DSAT_{M_0}} < V_{bias} < V_D - V_{T_3} - V_{SAT_{M_3}} + V_{T_{M_0}}$$

Input common mode range.

\* Output Range:  $\rightarrow$  Upper side can go near to  $V_D$

but lower side depends on  $V_{bias}$ .

\*  $V_{bias}$ :  $\rightarrow$  Upper limit is fairly close to  $V_D$  but lower limit is limited to a little above lower supply voltage (0 volt).



$\therefore$  the limits for  $V_{out}$  and  $V_{bias}$  are closer to  $V_D$  when we take nmos and pmos as load.

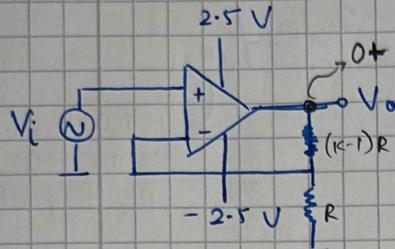
@ input

and if we take pmos and nmos as load,  
at input.

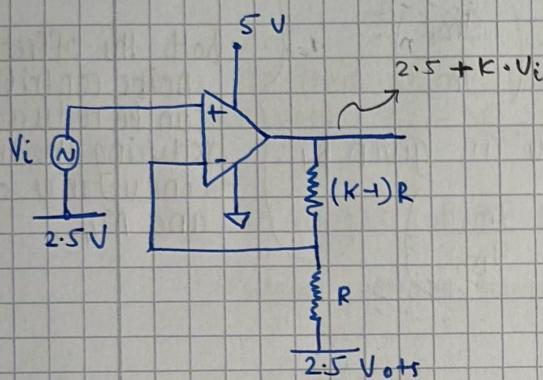
limits will be closer to lower rail.

\* The range of the op-amp is based on upper supply rail and lower supply rail and it's upto us what to call upper and lower supply rail (either +ve and +ve and some intermediate point to be gnd. and we can make gnd at the operating point [or])

upper rail to be  $V_{DD}$  and lower rail gnd. when we need to bias the input as well as the output at some intermediate value.



$0 + K \cdot V_i \rightarrow$  output will have quiescent value of 0 vols.



If we compare any two nodes from these two circuits, their Volt. diff. will be same.

\* all op-amps can be operated with single and dual rail.

— x — x —

\* Usually to maximize the voltage swing, we need to keep the operating point in the middle of the range of opamp.

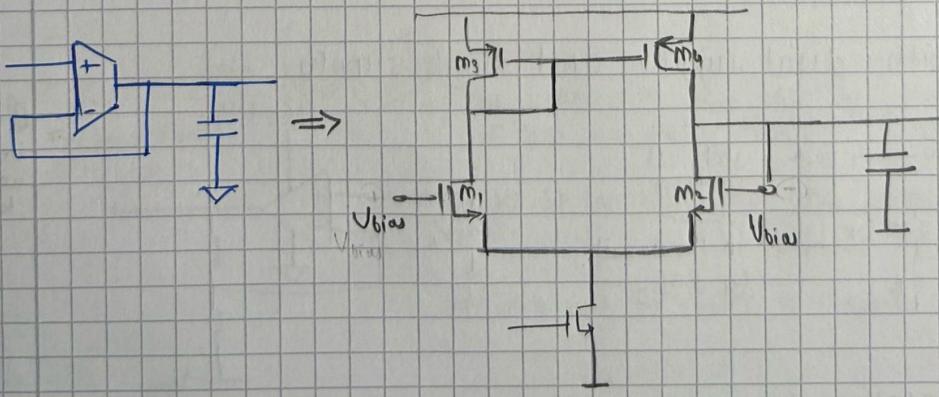
general rule.  
might not be  
applicable in special cases.

upper limit for  $V_{out}$

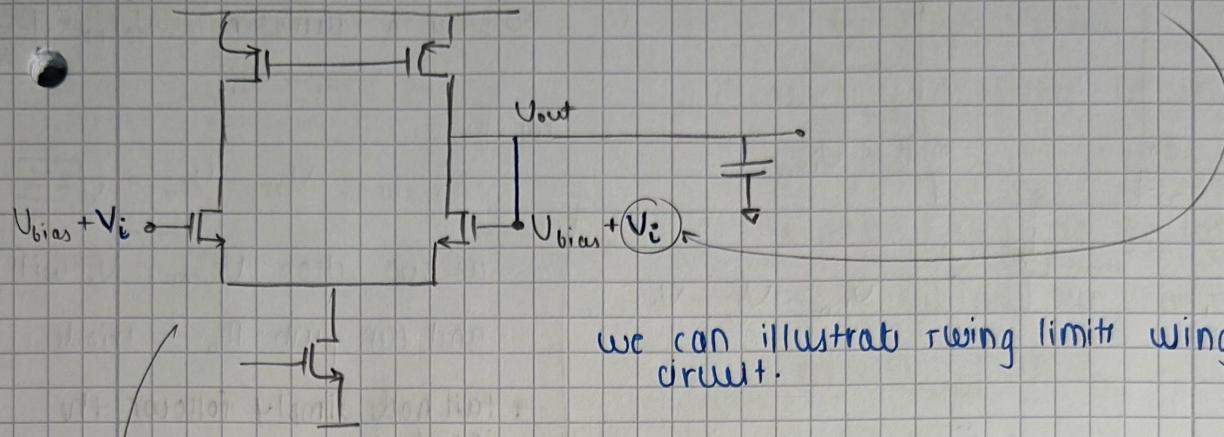
→ if we keep quiescent value of  $V_o$  @ middle, we get max. swing

lower limit for  $V_{out}$

Eg: Let's consider Voltage follower circuit with the op-amp.



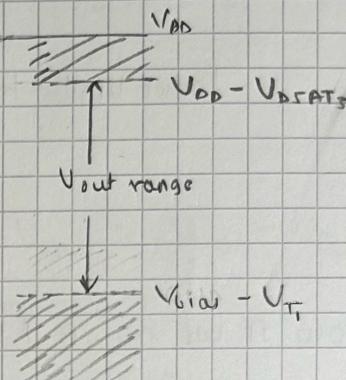
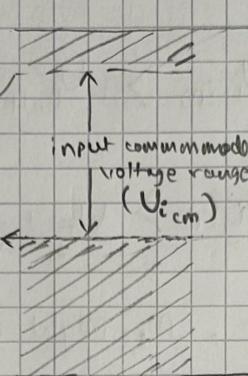
Now, let's say we have an incremental voltage  $V_i$ , the the output will also have same increment  $V_i$ . (voltage follower)



We know that;

$$V_{DD} - V_{T_3} + V_T < V_{DSAT_3}$$

$$V_{DSAT_0} + V_{DSAT_1} + V_T <$$



In this particular circuit, output offset is connected to  $V_{inm}$

$\therefore V_{out} = V_{bias} \text{ or } V_{inm} + V_{icm}$ .  $\therefore$  Output and input both voltage swing will be restricted by both, the input common mode range and the output range.

$$V_{icm,min} < V_{bias} + V_i < V_{icm,max}$$

$$V_{out,min} < V_{bias} + V_i < V_{out,max}$$

from these condition  
we can choose the  
value of  $V_{bias}$  for  
maxized signal swing.

for simplicity, take  $V_{DD} = 5$  Volt,  $V_{T_{min}} = 0.7$  v,  $V_{T_{max}} = 0.7$ . volt

$$V_{DSAT_{0,1,2,3,4,5}} = 0.2 \text{ Volt}$$

So,  $V_{bias}$  for maximum signal ( $V_{in}$ ) swing limit will be.  $\Rightarrow 2.5$  volt.

(clearing the confusion).

min. volt. @ drain required for  $M_1$  to stay in saturation is  $V_{DSAT} = \sqrt{\frac{I_o}{K_1}}$   
 $= V_{GS} - V_T$ ,

for  $M_0$ ;

$$V_{DSAT} = V_{GS} - V_T = \sqrt{\frac{2I_o}{K_0}}$$

as we drop  $V_{i,cm}$ ,  $V_x$  will  $\downarrow$   
and can push  $M_0$  to triode.

\* tail node simply follows the input.

$$\therefore \text{lower limit to } V_{i,cm} > V_{DSAT_0} \left| \frac{1}{I_o} + V_{GS} \right| \left| \frac{1}{I_{o/2}} \right|$$

$$V_{i,cm} > V_T + \sqrt{\frac{I_o}{K_1}} + \sqrt{\frac{2I_o}{K_0}}$$

\* Now if we go on  $\uparrow V_{i,cm}$ ,  $M_{1,2}$  might get pushed to triode region.

$V_{DD} - V_{DSAT_3}$   $M_3$  is always in saturation as its drain is connected to gate.

$V_{DSAT_1,2}$  is fixed at  $V_{DD} - V_{DSAT_{1,2}}$  and  $V_{i,cm}$  at  
gates of  $M_1$  if  $\uparrow$  ~~not~~ squeezes  $M_1$ .

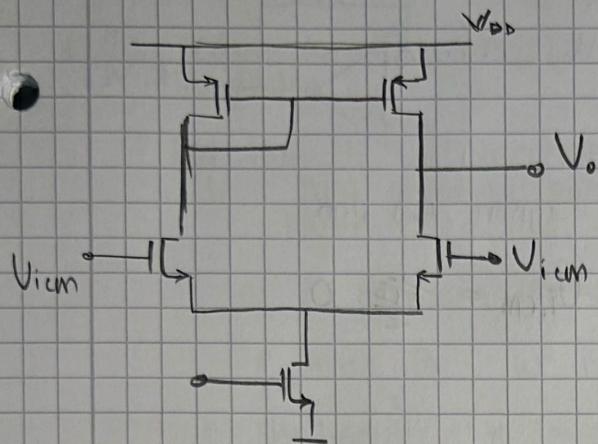
↪ and the gate voltage can rise above  $V_D$  but not  
more than  $1 \cdot V_T$  ( $V_{Gr} = V_{DSAT} + V_T$ )

$$\therefore V_{i,cm} < V_{DD} - \left( V_{GS_3} \right) \left| \frac{1}{I_{o/2}} \right| + V_T,$$

$$V_{i,cm} < V_{DD} - V_{T_3} - \sqrt{\frac{I_o}{K_3}} + V_T,$$

\* input structure of all the op-amp is similar to the above input structure  
then same results are applicable.

## \* Swing limit for $V_o$ .



we ignore  $\pm \frac{V_d}{2}$  as they are very small and we say that gate voltage is fixed at  $V_{i,cm}$ .

- ① as  $V_o \downarrow$  it pushes  $M_2$  in triode region.

\* drain ( $V_D$ ) can go lower than  $V_G$  but not more than  $1 \cdot V_T$ .

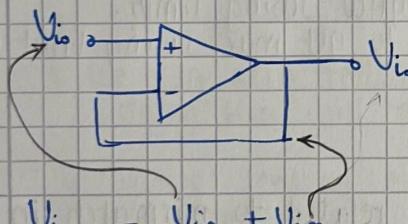
$$\text{as } V_{DSS} > V_{GS} - V_T \\ \therefore V_D > V_G - V_T$$

$$\therefore V_o \text{ must be } > V_{i,cm} - V_{T_2}$$

- ② as  $V_o \uparrow$ ,  $M_4$  squeezed,  $V_o < V_{DD} - (V_{SG} - V_{T_4})$

$$\therefore V_o < V_{DD} - \sqrt{\frac{I_o}{K_3}}$$

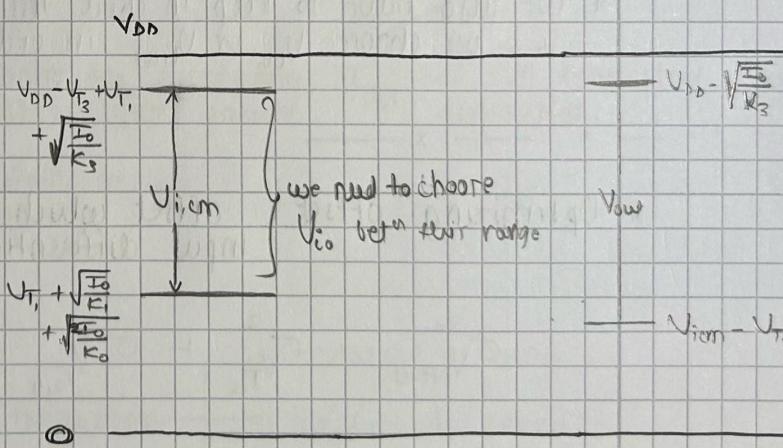
Now, let's illustrate using an example; let's take voltage follower.



$$V_{i,cm} = \frac{V_{i,0} + V_{i,1}}{2}$$

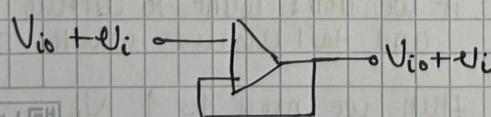
$$= \frac{V_{i,0} + V_{i,0}}{2}$$

$$\boxed{V_{i,cm} = V_{i,0}}$$



$V_{i,cm}$  has swing limit

now, when  $V_i$  is applied;

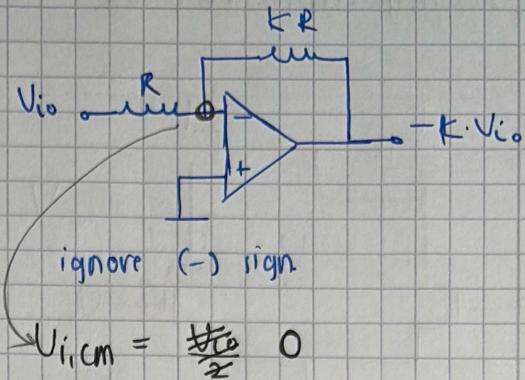
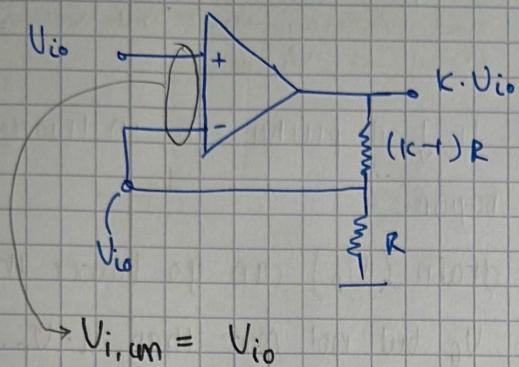


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$$\boxed{V_{i,cm} = V_{i,0} + V_i}$$

$$\text{and } V_{out} = V_{i,0} + V_i$$

both  $V_{i,cm}$  and  $V_{out}$  must follow these limits and then choose  $V_{i,0}$  accordingly. so that we can maximize  $V_i$



- \* When we make an inverting amplifier, common mode is not exercised at all giving us no common mode swing, and there is no effect of common mode swing. Once we choose operating point correctly after that the common mode doesn't change at all.

↳ advantage of non-inverting config.

### \* Summary of Single Stage op-amp

- \* We have a non-dominant pole and a zero both in -ve s-plane. and we try to keep them beyond unity gain b.w.
- \* We have noise and offset which we can adjust by appropriately sizing the current and the devices.
- \* We also have to keep in check the signal swing limits.  
→ we choose  $V_{i,o}$  or  $V_{bias}$  in order to get max swing limit for  $V_i$ .

- \* Optimizing offset : offset which is related to mismatch in the input differential pair.

$$\sigma_{V_{offset}}^2 = \sigma_{V_{T_{1,2}}}^2 + \sigma_{V_{T_{3,4}}}^2 \left( \frac{g_{m_3}}{g_{m_1}} \right)^2$$

can be reduced by increasing size of  $M_3$  and  $M_4$

- \* Contribution from  $M_{3,4}$  is reduced by reducing  $g_{m_3}$

as  $g_{m_3} = \frac{2I_0/2}{V_{DSAT_3}}$ ; if we don't want to disturb differential pair and tail current while reducing  $g_{m_3}$

then, we need to ↑  $V_{DSAT_3}$

trade off

but if  $V_{DSAT_3} \uparrow$  then upper swing limit ↓.

∴ we increase areas of all mosfets in the circuit.  
varianu

\* To reduce offset voltage  $\uparrow$  by factor of  $\geq 4$ , area of mosfet has to  $\uparrow$  by factor of 4

but then it will increase parasitic capacitance  $C_{gr}$ ,  $C_{ds}$ , etc. resulting in non-dominant pole and zero moving to lower frequencies ←

and to maintain the margins by maintaining the distance b/w gap  
 $P_1$  and  $P_2$  we need to shift the dominant pole resulting in shifting  $\omega_o$  to lower freq. eventually giving us reduction in speed of the op-amp at its  $(\frac{\omega_o}{k})$

 Trade off: optimizing offset leads to trading off speed of op-amp.

$$*\text{ Optimizing Noise: } S_{V_{in}} = \frac{16}{3} \frac{kT}{g_m} \left( 1 + \frac{g_{m3}}{g_m} \right)$$

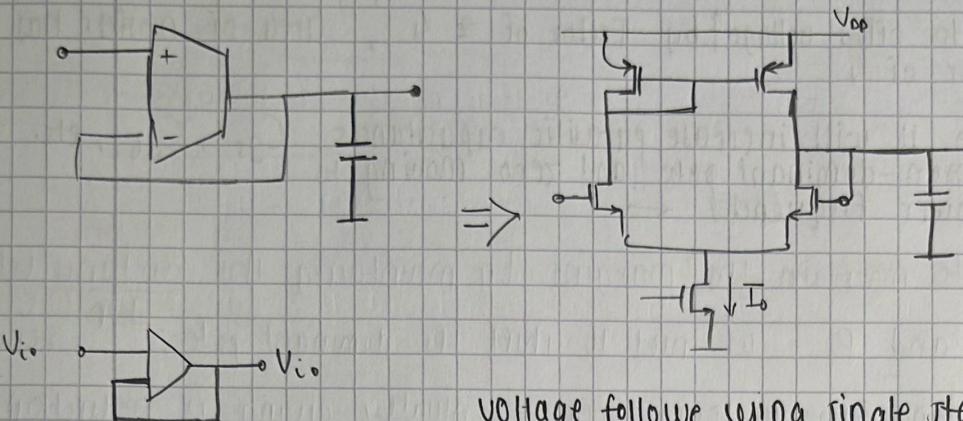
↳ similar to the case of  $V_{offset}$ , noise  $\downarrow$  by reducing  $g_{m3}$  which will be reducing  $V_{osat}$  increasing leading to affected swing limits.

\* we can also reduce noise by increasing  $g_{m,r}$  of all transistors, but doing this will result in larger power dissipation.

→ Noise Scaling principle or.  
Impedance scaling method.

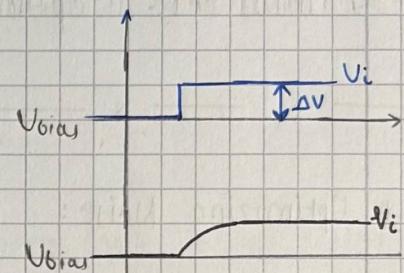
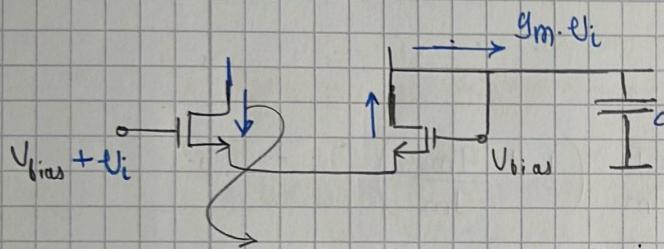
Offset, noise optimizing trade off →  reduced swing  
reduced speed  
higher power dissipation

\* Slew Rate: Maximum rate of change of output.



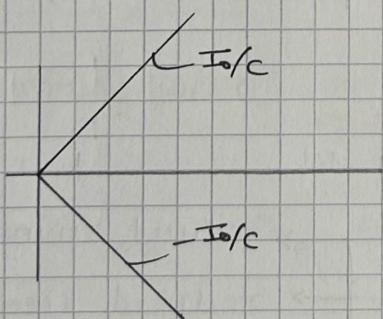
Voltage follower using single stage op-amp.

Now, let's say we applied a small step  $\Delta V_i$ . capacitor still holds  $V_{bias}$



current through  $M_1$  will increase by  $g_m \cdot \frac{\Delta V_i}{2}$  and current will be in opp. direction through  $M_2$ .

: total  $g_m \cdot \Delta V_i$  flows into capacitor. The output ( $V_o$ ) =  $V_{bias}$  will start rising at a rate  $\frac{g_m \cdot \Delta V_i}{C}$  which is =  $\frac{I_o}{C} \cdot \Delta V_i$



Now, if we go on increasing the magnitude of  $\Delta V_i$ , current in  $M_1$  ↑ and  $M_2$  ↓ by larger and larger amounts.

soon, we will reach a point where the  $\Delta V_i$  value is greater than saturation  $V_{o,sat}$  of differential pair. and

further that point all of  $I_o$  will flow through  $M_1$  and nothing will flow through  $M_2$ .

current through capacitor will be  $I_o$  : maximum rate of change of output =  $\pm \frac{I_o}{C}$  ... +ve step of  $\Delta V_i$

-  $\frac{I_o}{C}$  ... -ve step of  $\Delta V_i$

\* Slew rates in +ve and -ve sides might be different. But in our case they are same and =  $| \frac{I_o}{C} |$

### \* Trade off for optimized slew-rate:

To increase slew-rate, but not affect any other parameter of the op-amp, we need to  $\uparrow I_o$  but then  $g_m$  value changes

so, we need to reduce  $\frac{W}{L}$  of  $M_1$  and  $M_2$  in order to retain  $g_m$ .

$$\text{Or basically : } g_m = \frac{2I_o/2}{V_{D,SAT}} \quad | \quad \begin{array}{l} \text{if we want to } \uparrow I_o \text{ but keep } g_m \\ \text{const. we also need to } \downarrow V_{D,SAT} \end{array}$$

$\therefore$  for maximum slewrate we need to operate with large  $V_{D,SAT}$

$\curvearrowleft$  affects swing limits.

and for low power operation we need to trade off speed. ~~at~~

### \* Limitations of Single-stage op-amp:

① cannot operate with resistive load as it will reduce D.C. gain and thus increase the steady state error.

② DC gain =  $\frac{g_m}{g_{ds} + g_{dr}}$  or  $g_m (r_{ds,1} || r_{ds,3})$  has limited value

How do we improve?

$$A_o = \frac{g_m}{\lambda_1 I_o/2 + \lambda_3 I_o/2}$$

} As a designer, we only have freedom over  $L_1$  and  $L_3$

$$= \frac{g_m}{\frac{k_{\lambda_n}}{L_1} \cdot \frac{I_o}{2} + \frac{k_{\lambda_p}}{L_3} \cdot \frac{I_o}{2}}$$

}  $\uparrow L$  will  $\uparrow r_{ds}$  but to keep ~~g\_m~~  $g_m$  of all jamps, we need to  $\uparrow W$  too

resulting in  $\uparrow$  area ~~at~~ and eventually affecting the speed.

$\therefore$  Using this technique we can only increase gain by small amount. Thus we need some other technique.