Snehasish Kumar

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Research Interests

- Scalable compiler directed workload analysis
- Hardware software co-design for specialized architectures
- Core micro-architecture with a focus on the cache memory hierarchy

Academic

05/13 – 11/16 **PhD in Computing Science**, *Simon Fraser University*, British Columbia, Canada, *4.0/4.0*.
Senior Supervisor : Dr. Arrvindh Shriraman
My research is directed at facilitating energy efficient computation via specialization. I have adopted a two-pronged approach. First, a top down approach uses program analysis to determine program regions amenable for specialization using LLVM. Second, a bottom up approach evaluated architectural specialization to enable the efficient offload of accelerated program regions.
The former *workload-first* approach, uses program analysis to analyse and reconstruct program regions to aid the design and evaluation of specialized accelerators. An analysis of twenty-nine workloads revealed significant merit in analysis at the path granularity for specialization (IISWC'16). Further analysis of instruction dependency chains in frequently executed paths revealed opportunities for specialized macro-instructions (MICRO'16). An insight into the nature of frequently occurring paths led to the development of a new program abstraction for accelerators (HPCA'17). Robust alias analysis at the path granularity also enabled low overhead memory access interfaces for accelerators. I am also leading an ongoing effort to transparently generate application binaries with specialized regions offloaded to a tightly coupled FPGA substrate.
For the latter *architecture-first* approach, I designed and evaluated a hardware accelerator for software data structures. The access of and compute on data structures is offloaded to an array of processing elements which are tightly coupled to the last level cache (ICS'15). I also evaluated a specialized coherence protocol for fixed function accelerators (ISCA'15) which improves performance and reduces energy consumption by mitigating redundant data movement.
Publications : **HPCA'17, IISWC'16, MICRO'16, ICS'16, ISCA'15, ICS'15**

01/11 – 04/13 **MSc in Computing Science**, *Simon Fraser University*, British Columbia, Canada, *3.8/4.0*.
Senior Supervisor : Dr. Arrvindh Shriraman
Designed and evaluated a variable granularity cache memory hierarchy. The system adaptively varies the cache line size to eliminate data fetches not used by the application. Workloads benefited from increased effective cache space. Overall cache miss rates improved and dynamic energy consumption was reduced. The proposed architecture was modeled using the RUBY memory system simulator and evaluated on twenty-two workloads drawn from popular benchmark suites. A subsequent research work evaluated a variable granularity cache coherence protocol.
Publications : **ISCA'13, MICRO'12**

08/06 – 04/10 **B. Tech in Computer Engineering**, *Biju Patnaik University of Technology*, Orissa, India, *8.3/10.0*.
Supervisor : Dr. Satyananda Champati Rai
Designed and implemented a genetic algorithm to address the problem of channel allocation in cellular networks. The algorithm computes a pseudo optimal borrowing scheme amongst neighbouring cells. The implementation used variable separation to reduce the search space. The approach improved over the state of the art and consistently computed near optimal solutions.

Publications

2017 – **Needle : Leveraging program analysis to extract accelerators from whole programs,**
Snehasish Kumar, Nick Sumner, Vijayalakshmi Srinivasan, Steve Margerm, and Arrvindh Shriraman, *23rd ACM International Conference on High Performance Computer Architecture*, HPCA '17.
Acceptance Rate $\approx$ 22%.

2016 – **ChainSaw : Creating Von-Neumann Accelerators with Fused Instruction Chains,**
Amirali Sharifian, Snehasish Kumar, Apala Guha, and Arrvindh Shriraman,
49th Annual IEEE/ACM International Symposium on Microarchitecture, MICRO '16.
Acceptance Rate ≈ 22%.

– **SPEC-AX : Extracting Accelerator Benchmarks from Microprocessor Benchmarks,**
Snehasish Kumar, Nick Sumner, and Arrvindh Shriraman,
2016 IEEE International Symposium on Workload Characterization, IISWC '16.
Acceptance Rate ≈ 30%.

– **Peruse and Profit: Estimating the Accelerability of Loops,**
Snehasish Kumar, Vijayalakshmi Srinivasan, Amirali Sharifian, Nick Sumner, and Arrvindh Shriraman,
30th ACM International Conference on Supercomputing, ICS '16.
Acceptance Rate ≈ 24%.

2015 – **Fusion: Design Tradeoffs in Coherent Cache Hierarchies for Accelerators,**
Snehasish Kumar, Arrvindh Shriraman, and Naveen Vedula,
42nd Annual International Symposium on Computer Architecture, ISCA '15.
Acceptance Rate ≈ 19%.

– **DASX: Hardware Accelerator for Software Data Structures,**
Snehasish Kumar, Naveen Vedula, Arrvindh Shriraman, and Vijayalakshmi Srinivasan,
29th ACM International Conference on Supercomputing, ICS '15.
Acceptance Rate ≈ 25%.

2013 – **Protozoa : Adaptive Granularity Cache Coherence,**
Hongzhou Zhao, Arrvindh Shriraman, Snehasish Kumar, and Sandhya Dwarkadas,
40th Annual International Symposium on Computer Architecture, ISCA '13.
Acceptance Rate ≈ 19%.

2012 – **Amoeba-Cache : Adaptive Blocks for Eliminating Waste in the Memory Hierarchy,**
Snehasish Kumar, Hongzhou Zhao, Arrvindh Shriraman, Eric Matthews, Sandhya Dwarkadas, and Lesley Shannon,
45th Annual IEEE/ACM International Symposium on Microarchitecture, MICRO '12.
Acceptance Rate ≈ 18%.

Workshops

03/16 GCASR'16 – Statistical program analysis assisted cost-effective sampling in large scale scientific simulations

06/15 SFU-ZU workshop on Big Data – Data Structure Accelerators

12/13, 08/14 WoNDP'13, PACT'14 – SQRL : Hardware Accelerator for Collecting Software Data Structures

Invited Talks

06/16 IBM Research – Needle [HPCA '17]

01/16 SRC India Design Review – Caches [MICRO '12, ISCA '15]

01/16 Intel Bangalore – Fusion [ISCA '15]

Awards

08/16 President's PhD Scholarship, Simon Fraser University

'16, '14, '12 Graduate Fellowship, Simon Fraser University

01/14 Special Graduate Entrance Scholarship, Simon Fraser University

Projects

01/15 Networks : Parallel implementation of Kou, Markowsky and Berman (1981) algorithm

04/14 Natural Language Processing : Optimizing the Bitpar CKY parser

12/11 Computational Geometry : Interactive demo for the Linear Cell Complex (CGAL)

04/11 Machine Learning : Non-Negative Matrix Factorisation for large datasets

Professional and Academic Experience

06/13 – 12/13 Research Intern : Systems Technology and Architecture
IBM, T.J. Watson Research Centre

'11 – '16 Research Assistant : SYNAR Group, Simon Fraser University

'11, '13 Teaching Assistant : CMPT 880, 120, 165, 300