Snehasish Kumar

7360 Halifax Street, 502A
Burnaby V5A1M4
✆ +1 (604) 721 4323
✉ snehasish_kumar@sfu.ca
🖥 www.snehasish.net

Education

05/2013 – Present **PhD in Computing Science**, *Simon Fraser University*, British Columbia, Canada, *4.0/4.0*.
Senior Supervisor : Dr. Arrvindh Shriraman
The objective of my research is to facilitate energy efficient computation using hardware accelerators via a two pronged approach. The first, hardware-centric approach explores novel micro-architecture closely coupled with the cache memory hierarchy to offload computation. The second, software-centric approach uses program analyses techniques to deduce which parts of a given program are amenable to hardware acceleration. Furthermore, we aim to automatically extract micro-workloads from large programs using dynamic analyses. Together these approaches discover the potential sources and benefits of using hardware accelerated computation.
Accepted : ISCA '15, ICS '15
Submitted : ISCA '16, ICS '16

01/2011 – 04/2013 **MSc in Computing Science**, *Simon Fraser University*, British Columbia, Canada, *3.8/4.0*.
Senior Supervisor : Dr. Arrvindh Shriraman
A novel microarchitecture was proposed which incorporated adaptive granularity cache lines for memory hierarchies to eliminate bandwidth and energy waste. The system varies the cache line size dynamically based on the nature of the application to only bring in useful data. This increases cache utilisation and improves miss rate by increasing the effective cache size. A continuation of this research led to the design of a coherence protocol which adaptively changes the storage and coherence granularity in order to increase efficiency and reduce energy consumption.
Accepted : MICRO '12, ISCA '13

08/2006 – 04/2010 **B. Tech in Computer Engineering** , *Biju Patnaik University of Technology*, Orissa, India, *8.3/10.0*.
Supervisor : Dr. Satyananda Champati Rai
I was responsible for the design and implementation of a constrained vector genetic algorithm to solve the problem of selecting an optimal borrowing scheme for the channel allocation problem in wireless mobile networks.

Publications

2015 **Fusion : Design Tradeoffs in Coherence Hierarchies for Accelerators,**
Snehasish Kumar, Arrvindh Shriraman, and Naveen Vedula, In *Proceedings of the 42nd Annual International Symposium on Computer Architecture*, ISCA 2015.

DASX : Hardware Accelerator for Software Data Structures,
Snehasish Kumar, Naveen Vedula, Arrvindh Shriraman, and Vijayalakshmi Srinivasan, In *Proceedings of the 29th ACM International Conference on Supercomputing*, ICS 2015.

2013 **Protozoa: Adaptive Granularity Cache Coherence,**
Hongzhou Zhao, Arrvindh Shriraman, Snehasish Kumar, and Sandhya Dwarkadas, In *Proceedings of the 40th Annual International Symposium on Computer Architecture*, ISCA 2013, pages 547–558.

Architectural Support for a Variable Granularity Cache Memory System,
Snehasish Kumar, *MSc Thesis*.

2012 **Amoeba-Cache: Adaptive Blocks for Eliminating Waste in the Memory Hierarchy,**
Snehasish Kumar, Hongzhou Zhao, Arrvindh Shriraman, Eric Matthews, Sandhya Dwarkadas, and Lesley Shannon, In *Proceedings of the 2012 45th Annual IEEE/ACM International Symposium on Microarchitecture*, IEEE MICRO 2012, pages 376–388.

2011 **MiCi: A Novel Micro-Level Temporal Channel Imploration for Mobile Hosts,**
Snehasish Kumar, Satyananda Champati Rai, Rajib Mall, and Sateesh Kumar Pradhan, *CoRR*, abs/1104.4204.

Presentations and Posters

01/2016 CoolCaches : Energy Efficient Caches,
Semiconductor Research Corporation, India Design Review, Bengaluru, India
Microarchitecture Research Lab, Intel, Bengaluru, India

05/2015   DASX : Hardware Accelerator for Software Data Structures,
International Conference on Supercomputing, Newport Beach, CA, USA
1st Joint SFU-ZU Workshop on Big Data, Zhejiang University, Hangzhou, China

05/2015   Fusion : Design Tradeoffs in Coherent Cache Hierarchies for Accelerators,
International Symposium on Computer Architecture, Portland, OR, USA

08/2014   DAX : Hardware Accelerator for Collecting Software Data Structures
Parallel Architectures and Compiler Techniques, Edmonton, AB, Canada

12/2012   Amoeba-Cache : Adaptive Blocks for Eliminating Waste in the Memory Hierarchy
International Symposium on Microarchitecutre, Vancouver, BC, Canada

Awards

01/2014   Special Graduate Entrance Scholarship, Simon Fraser University

01/2016   Graduate Fellowship, Simon Fraser University

08/2014   Graduate Fellowship, Simon Fraser University

01/2012   Graduate Fellowship, Simon Fraser University

Projects

04/2015   Parallel implementation and analysis of the KMB algorithm
Mentor: Dr. Jiangchuan Liu, Network Modelling Lab, SFU

12/2014   Implementation of Apriori on Hadoop
Mentor: Dr. Ke Wang, Database and Data Mining Lab, SFU

04/2014   Optimizing the Bitpar CKY parser
Mentor: Dr. Anoop Sarkar, Natural Language Lab, SFU

12/2011   Interactive demo for the Linear Cell Complex (Computational Geometry Algorithms Library)
Mentor: Dr. Guillaume Damiand , CNRS at LIRIS, Universitè Claude Bernard

04/2011   Non-Negative Matrix Factorisation for very large datasets
Mentor: Dr. Oliver Schulte, Computational Logic Group, SFU

Work Experience

06/2013 – 12/2013   Research Intern : Systems Technology and Architecture
IBM, T.J. Watson Research Centre
Mentor: Dr. Vijayalakshmi Srinivasan

2011 – 2015   Research Assistant : SYNAR Group, Simon Fraser University

2011, 2013   Teaching Assistant : CMPT 880, 120, 165, 300

Technical Skills

Languages   C++11, C, Python, Java, Matlab, R

Simulators   Multifacet GEMS(Ruby), MacSim

Leadership

05/2012 – 03/2013   Councillor, Graduate Student Society, Simon Fraser University

11/2008 – 07/2010   Microsoft Student Partner

09/2009 – 07/2010   Treasurer, IEEE Student Chapter