# Sneha Sudhakaran

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## Summary

GPU design engineer at Imagination Tech with prior roles at Qualcomm & ARM. Driven by a strong enthusiasm for innovation, contributed to a startup called 'Signalchip' which went on to release India's first 5G basestation SoC. With 7+ years of experience in digital design engineering, I now seek to apply my skill-set in research and innovation.

## Education

- **R.V College of Engineering, VTU** — *Aug 2013 - May 2017*, Bangalore, India
  - Bachelors in Engineering - Electronics and Communication - GPA: **9.15 /10**

  (Relevant Courses : uProcessors, Engg Math & Physics, Optical Fibers, VLSI, Signal Processing)
- **Royale Concorde International School** — Bangalore, India
  - All India secondary school exam, 2013 : **95.2%**
  - All India secondary school certificate exam, 2011 : **GPA - 10/10**

## Awards and Achievements

- National Science Olympiad Foundation (NSO) '13, International Rank 196
- National Subject Topper in Physics '13, CBSE India
- COMEDK (Engineering Entrance Exam) '13 – All India National Rank 194
- International Mathematics Olympiad (IMO)'13, International Rank 379
- Gold Medallist; Academic Excellence Award; Most Conscientious Student Award - RCIS '13
- ThanQ Award by Qualcomm for improvements in the GPU microarch that reduced power consumption in chips.
- INSPIRE Scholarship awarded to the top 1 percentile in the country based on the National CBSE examinations.

## Experience

- **Imagination Technologies** — *Jan 2023 - Present*
  *Senior Design Engineer* — Bangalore,India
  - Led the design of a burst instruction cache for the burst processor in the graphics geometry pipeline. Managed the L1 cache and its micro-architecture, specification analysis, documentation, and system verilog RTL.
  - Automotive chips: Design and analysis of auto-test logic with integrated BIST in GPU modules, using various test methods to ensure data validity.
  - PPA (power performance area) analysis and assessments for new GPU features in incremental chip tapeouts, using Joules by Cadence.
- **Qualcomm** — *April 2018 - Jan 2023*
  *Senior Design Engineer* — Bangalore,India
  - Designed clock controllers for the camera, video and graphics modules inside the Snapdragon chips, by choosing appropriate PLLs, clock tree and power components.
  - Designed the GPU vertex fetch block for Snapdragon projects. Implemented vertex fetch L1 cache changes that reduced the modules' power by 3%.
  - Analyzed the graphics geometry pipeline RTL with Veloce, optimizing the GPU Binning and Rendering passes, using performance benchmarks like Manhattan, Attan, Aztec etc.
  - Using Python, automated the RTL generation of the SoC Register Bank IP RTL, cutting the spec-to-delivery time by 70%.
  - Improved SoC hardware-accelerator fuse wire routing by serialisation logic, reducing feedthroughs in hard macros.
  - Carried out multiple ECOs in the SoC netlist followed by LEC and formal verification.
- **Signalchip** — *Jun 2017 - April 2018*
  *Design Engineer* — Bangalore,India
  - Microarchitecture, RTL design, and verification of a new dual-functional UART/USIM module.
  - Designed an Ethernet SGMII PHY RTL as per IEEE 802.3 and Cisco standards, covering the serdes, 8b10b codec, and error detection module.
  - Performed SoC bring-up and verification for DDR firewall, MCDMA, SGDMA, Interrupt Handler, and Configuration firewall with SystemC and Verilog.

- Conducted SV verification, testbench setup, and test generation for UART, USIM, and SGMII PCS.
- Enhanced RTL environments with Perl and Python for flow and test automation.

- **Hewlett Packard Enterprises** *Jan 2017 - April 2017*
  *Research Intern* Bangalore,India
  - Used Machine Learning tools like IBM Watson for benchmarking and backend validation of the HPE data archiving product(which performs OCR and language-recognition in text).
  - Java-based test automation for the existing verification testbenches and regressions created for the HPE data archiving product.

- **ARM** *May 2016 - Jul 2016*
  *Intern* Bangalore,India
  - Researched large repository management systems for ARM code using Git and SVN, and trained the ATEG team on migrating to a new architecture repository system.
  - Successfully completed extensive courses on the ARM ISA and the RISC architecture.

## PROJECTS

- **Traffic Violation Detection using Image Processing:**

  Utilized frame-by-frame image processing on traffic videos to detect violations, transmitting images and SMS notifications to mobile devices via IEEE 802.11 on a Raspberry Pi. Presented at the ITS Conference 2017, RVCE:

  Sneha S , Kariyappa B S et all, Video-Based Traffic Violation Detection System, *National Conference on Leveraging Intelligent Transportation System for Smart Cities*, ITS-2017 2nd–4th March 2017, RVCE, Bangalore.

- **Train Approaching Alarm System:**

  Created a prototype of an adhoc network based on the IEEE 802.15.4 protocol and the Atmega328 Processor, in order to identify in advance, the arrival of trains at unmanned railway crossings. Upon detection, the wireless node signals another base node at the unmanned crossing to trigger an alarm.

- **Team Helios Racing - Baja SAE**

  Designed an overheating-warning circuit and an odometer for an all-terrain-vehicle at University, the team received notable recognitions at the 2016 SAE competition.

- **Obstacle avoiding Robot**

  Developed an obstacle avoiding robot by using the hr-s04 sensors. It intelligently senses the surroundings and makes decisions to maneuver around objects. Developed using the Atmega328 microcontroller.

## SKILLS

- **Programming Languages:** Python, C, C++, SystemC, System Verilog, VHDL, Perl, Matlab
- **Tools:** Cadence Virtuoso, Questasim, Spyglass, Synopsys Design Compiler, Veloce Emulator, Verdi, Ansys HFSS
- **Data Science & Machine Learning:** IBM Watson, Kaggle, OpenCV libraries, Pytorch, Tensorflow
- **DevOps & Version Control:** Git, github, SVN, Jenkins, Perforce, Clearcase
- **Other Tools & Technologies:** Raspberry Pi, Arduino, Zigbee, FPGA, PCB, Qiskit