Report - Lab 6

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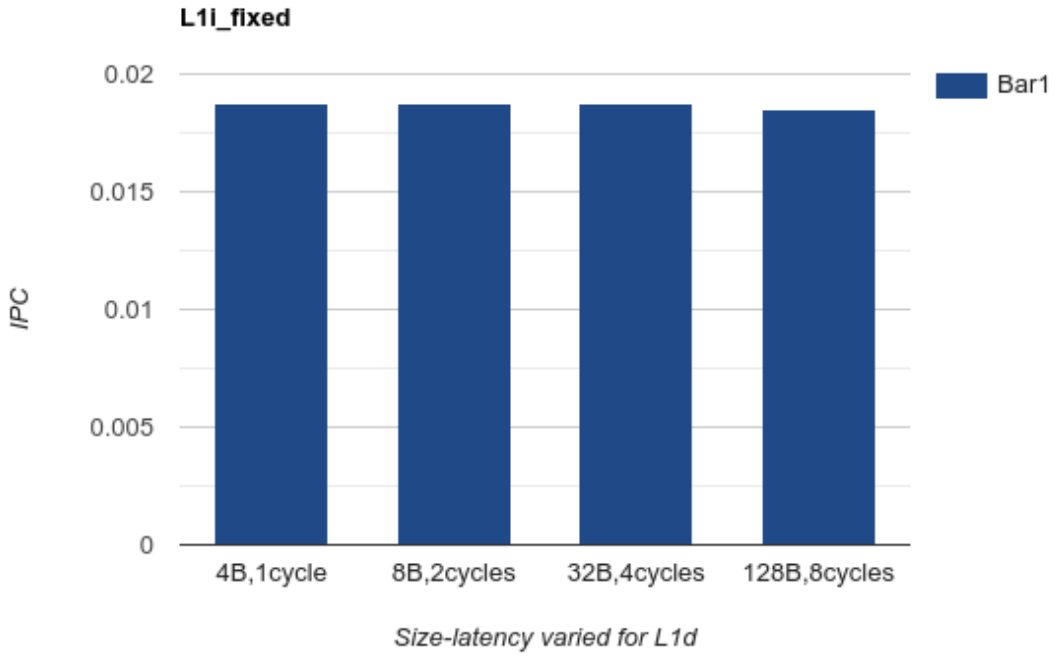
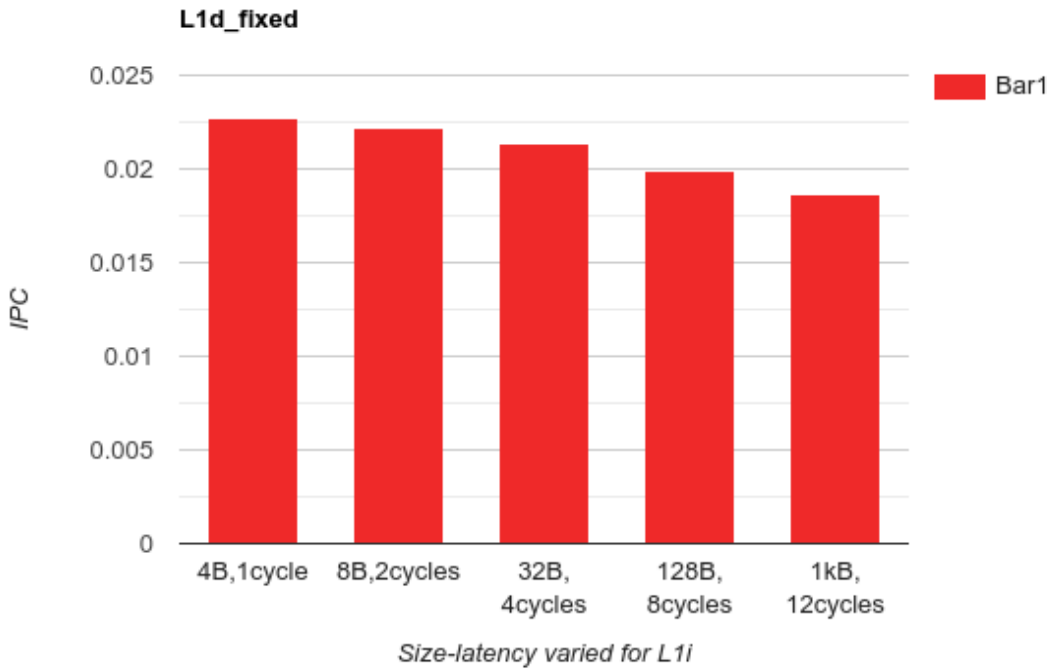
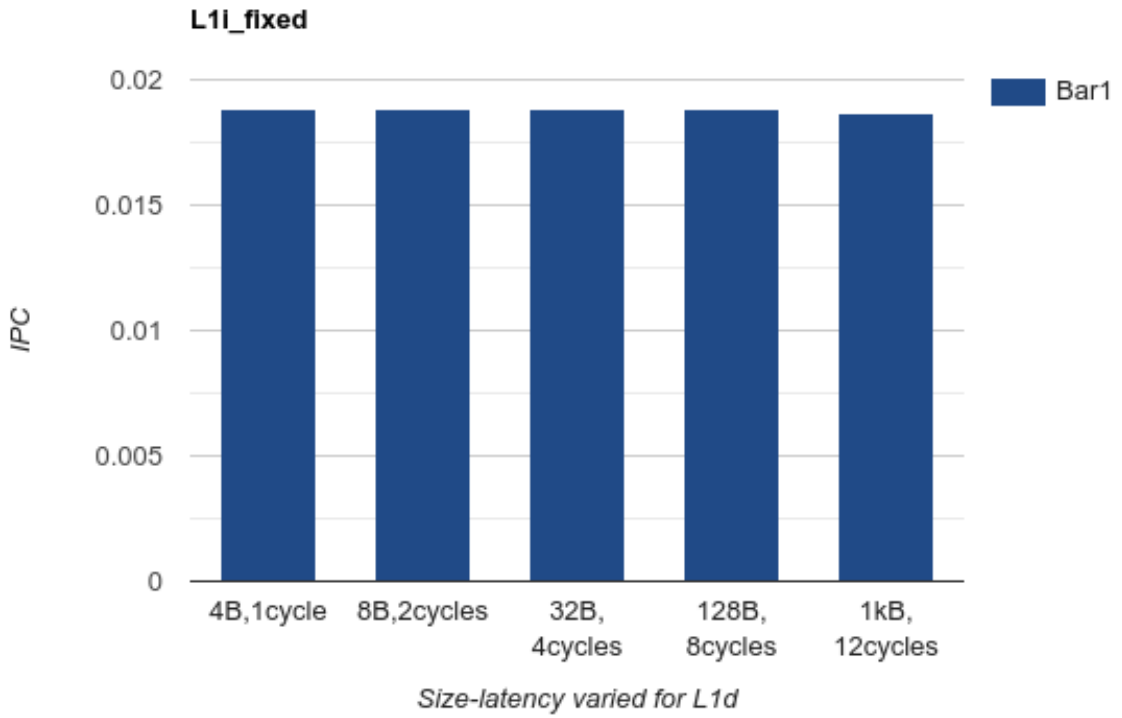
L1i Cache: Size = 1kB, Latency = 12 Cycles (varying L1d)
L1d Cache: Size = 1kB, Latency = 12 Cycles (varying L1i)

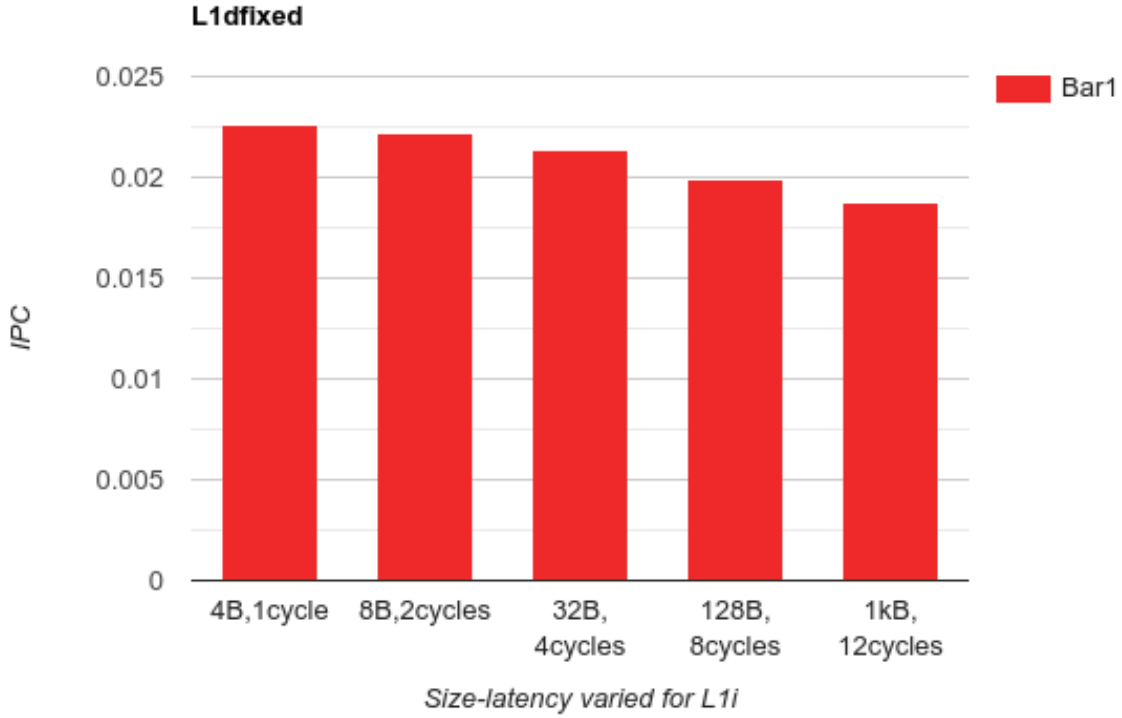
1. evenorodd.out



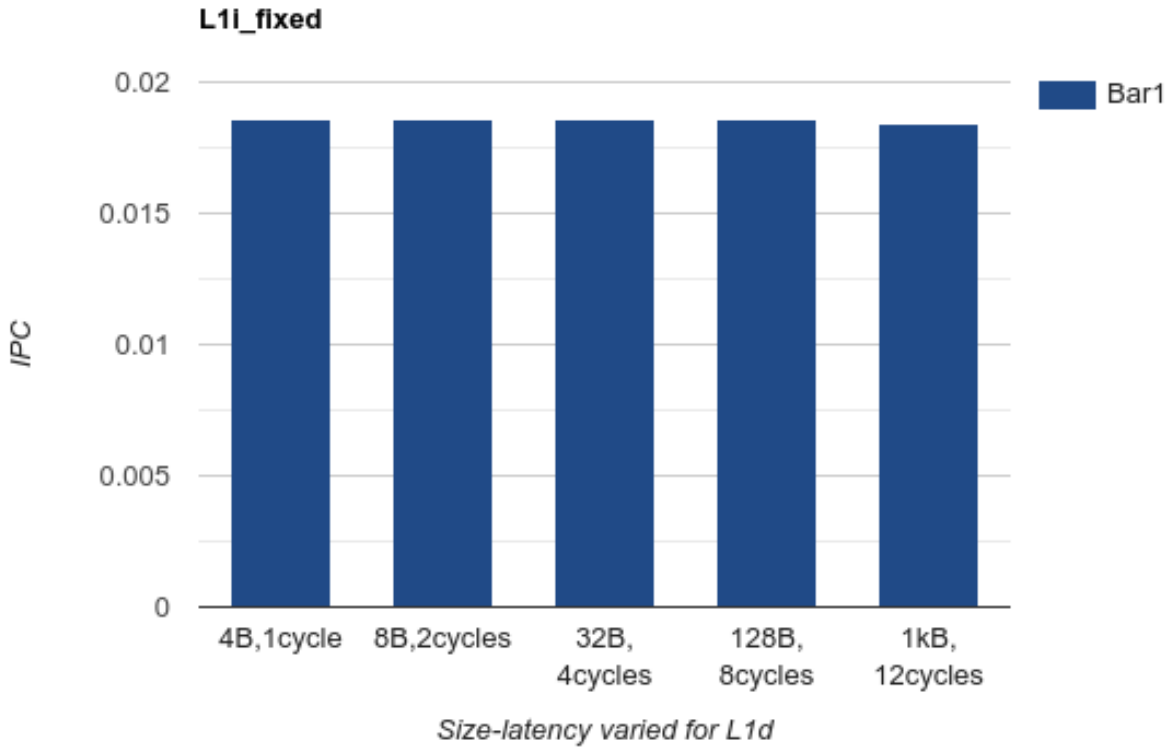


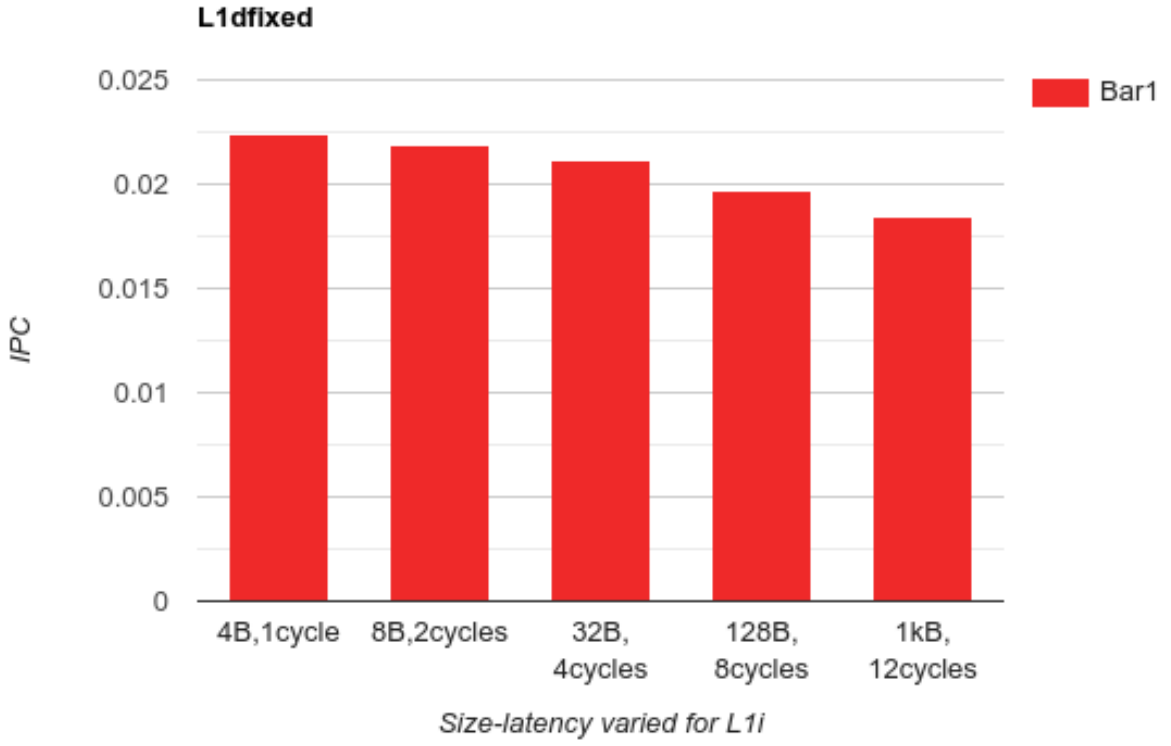
2. 1-even.out


L1i_fixed
0.02
0.015
0.01
0.005
0
IPC
Bar1
4B,1cycle
8B,2cycles
32B, 4cycles
128B, 8cycles
1kB, 12cycles
Size-latency varied for L1d

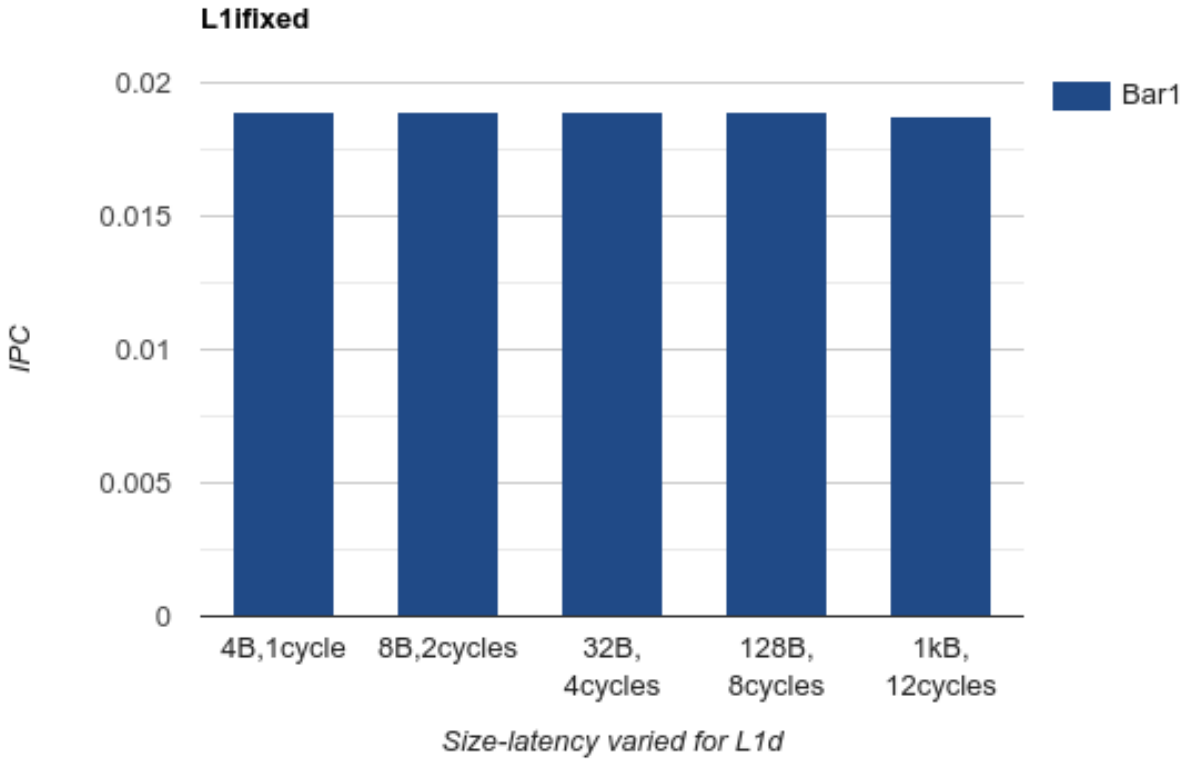

L1dfixed
0.025
0.02
0.015
0.01
0.005
0
IPC
Bar1
4B,1cycle
8B,2cycles
32B, 4cycles
128B, 8cycles
1kB, 12cycles
Size-latency varied for L1i

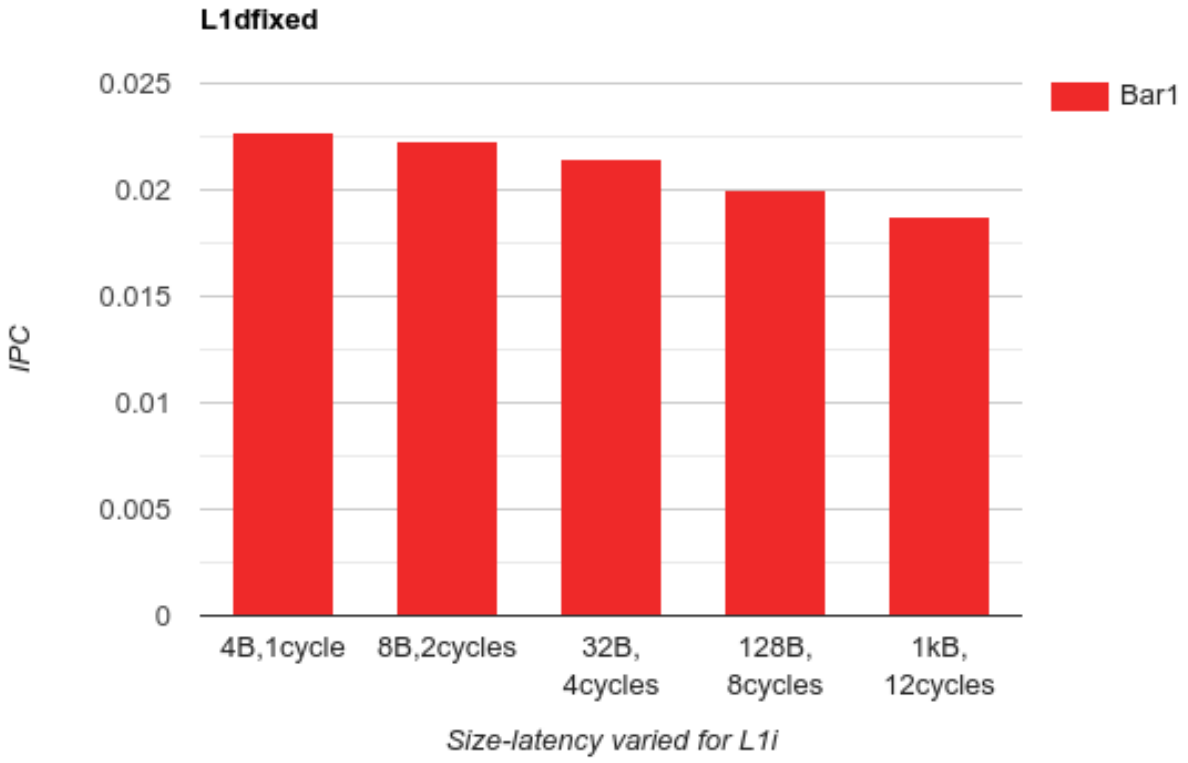
3. 2-prime.out


L1i_fixed
0.02
0.015
0.01
0.005
0
IPC
Bar1
4B,1cycle
8B,2cycles
32B, 4cycles
128B, 8cycles
1kB, 12cycles
Size-latency varied for L1d

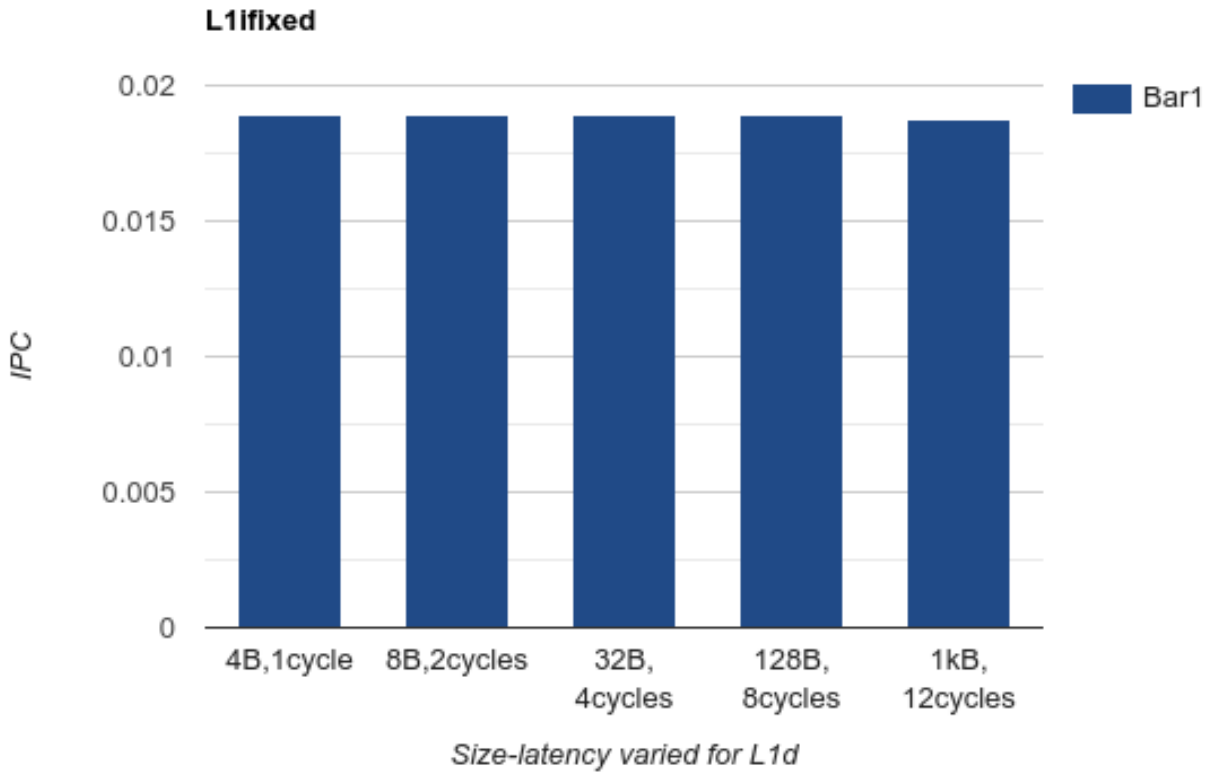

L1dfixed
0.025
0.02
0.015
0.01
0.005
0
IPC
Bar1
4B,1cycle
8B,2cycles
32B, 4cycles
128B, 8cycles
1kB, 12cycles
Size-latency varied for L1i

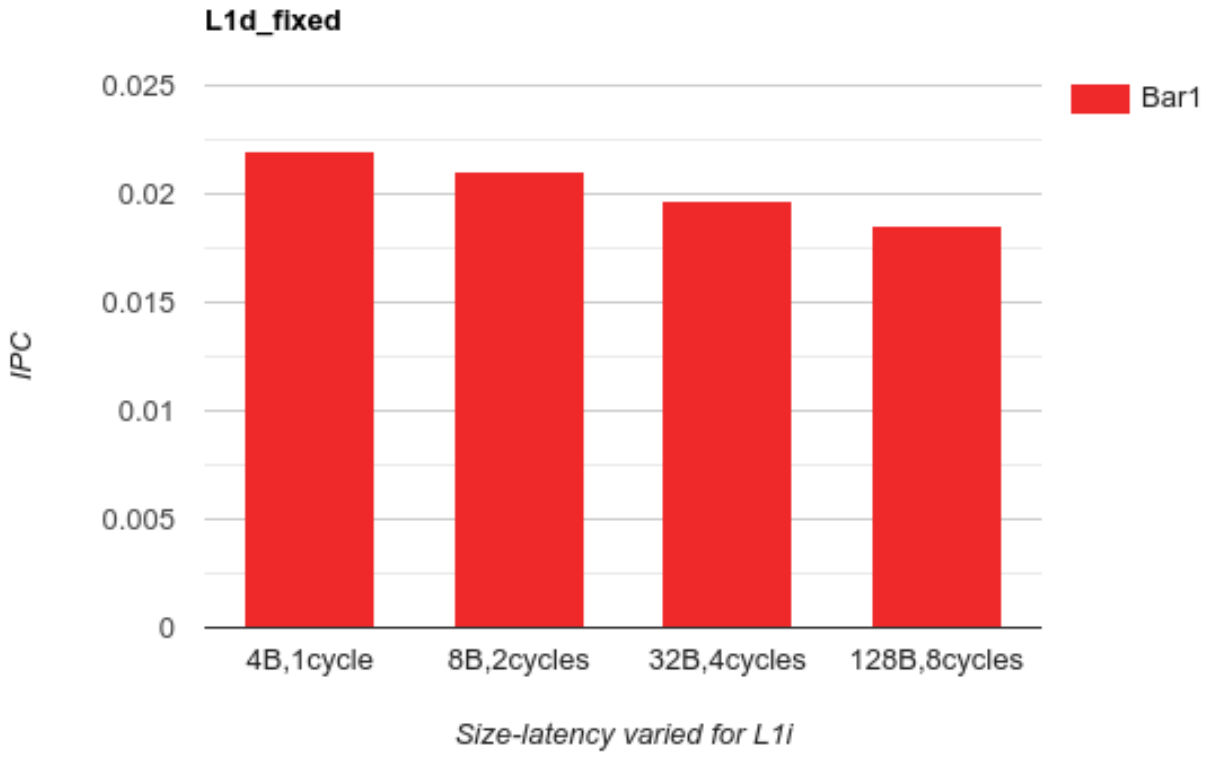
4. 5-fibonacci.out





5. 6-arithmetic.out





Inferences:

- Since the number of data cache accesses is very low compared to the instruction cache, varying the data cache size barely makes any difference at all.
- Hence, the plots obtained are constant for most programs.

- For the instruction cache, as the cache size is increased, latency increases and hence the IPC decreases.
- Moreover, increasing the cache size should increase the number of hits, so it should increase the IPC. But here, in all cases, increasing latency dominates over the decreasing IPC.
