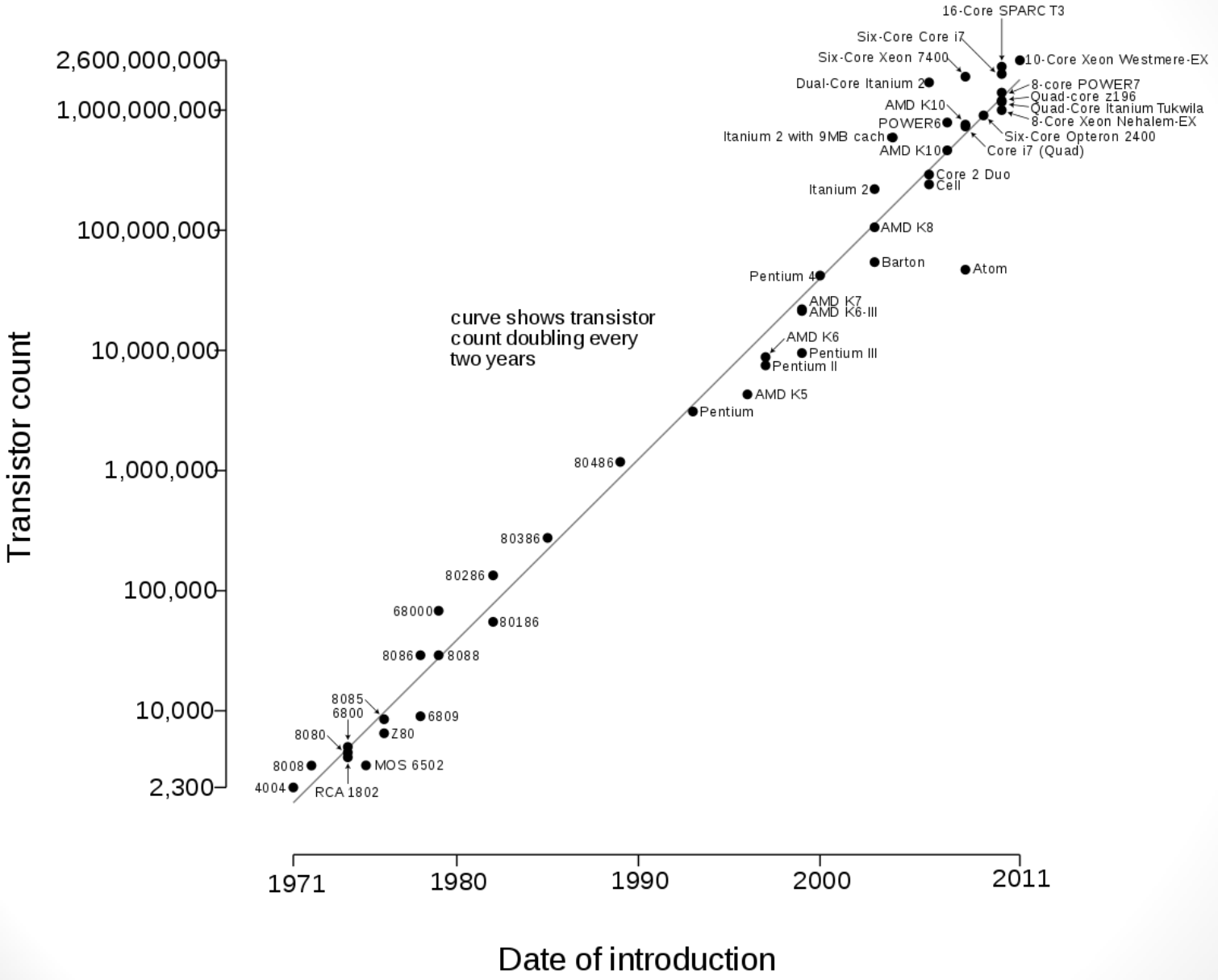
Phase Change Memory – An alternative for DRAM

Snehil Verma

What is the problem with DRAM?

Microprocessor Transistor Counts 1971-2011 & Moore's Law



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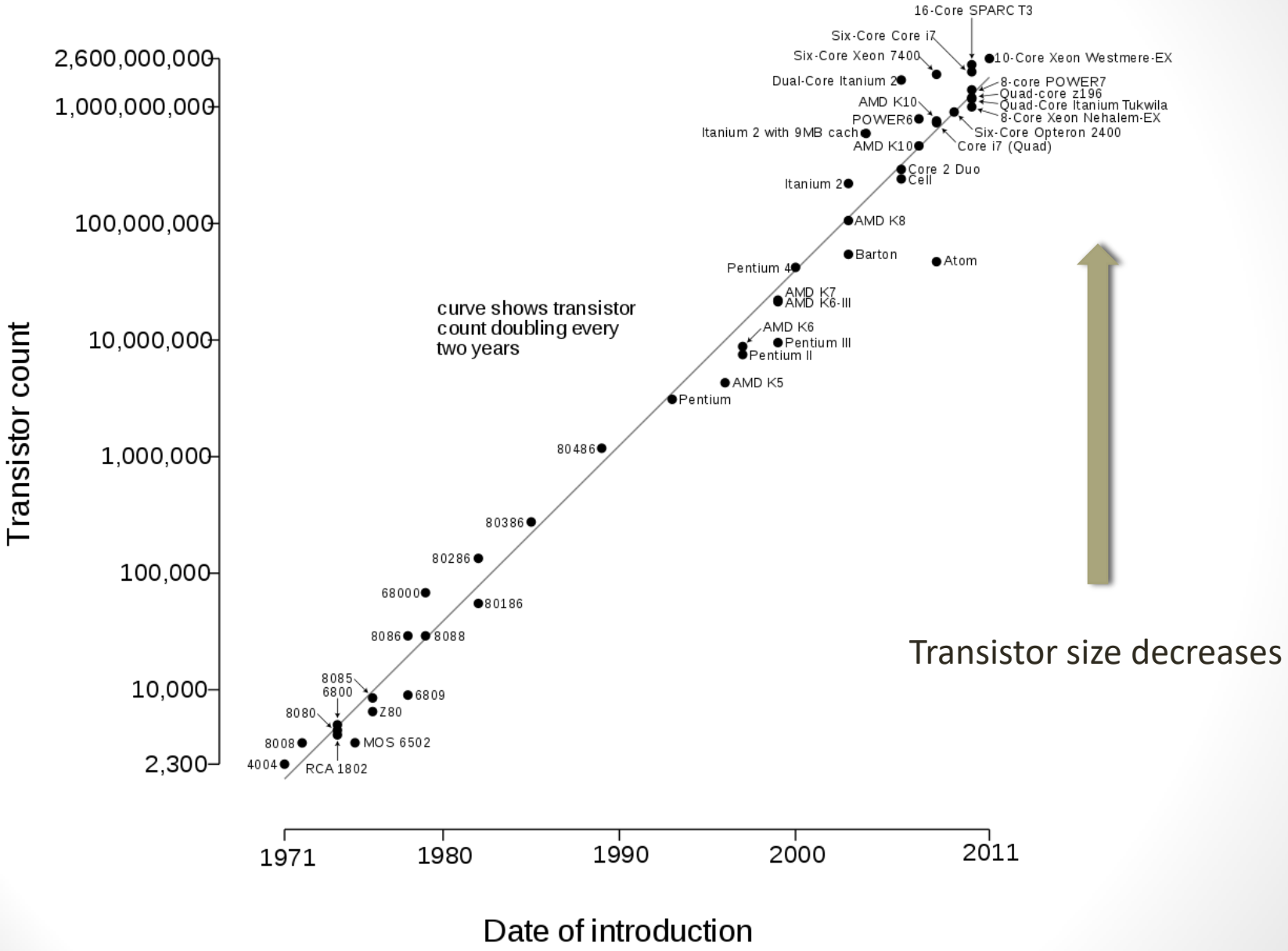

Problems with DRAM

Decreasing sizes of transistors → Affects the scalability

Problems with DRAM

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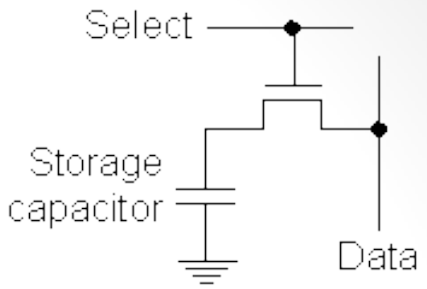
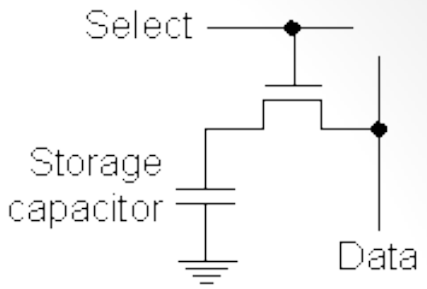
- ✓Storage
- ✓Sensing Mechanisms

} Became less Reliable !!

DRAM Scalability

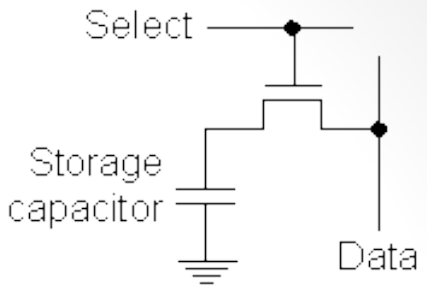


DRAM Scalability



- Capacitor
- ✓ Manufacturing small CAPs →Store sufficient charges for reliable sensing

DRAM Scalability



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- ✓ Increases sub-threshold leakage → difficult to ensure DRAM retention time

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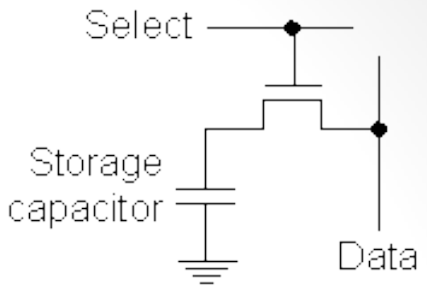

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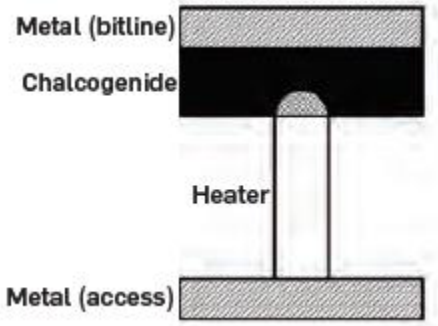
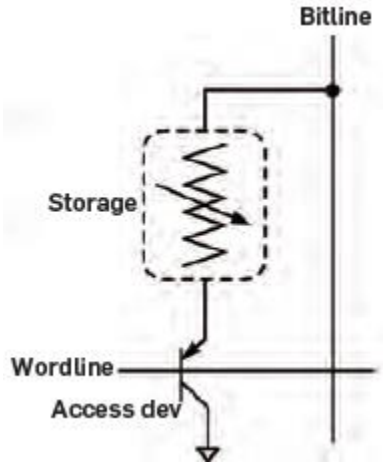
According to ITRS, "manufacturable solutions are not known" for DRAM beyond 40nm

So, what’s next ?

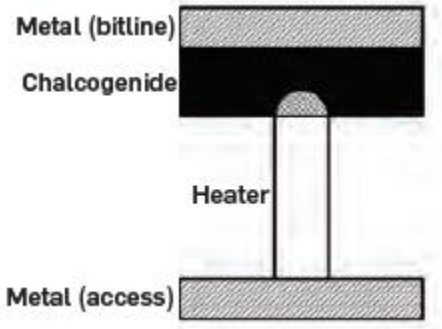
Phase Change Memory

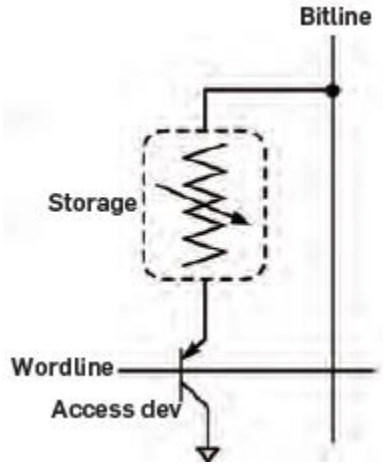




- ✓Storage element

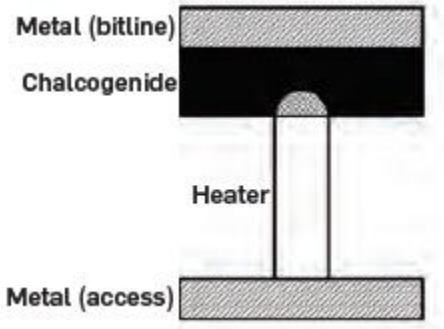
Phase Change Memory

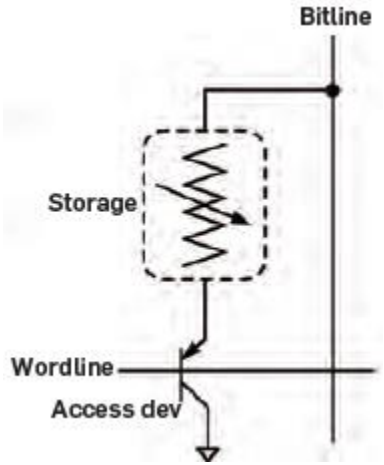




- ✓Storage element
- ✓2 metal electrodes

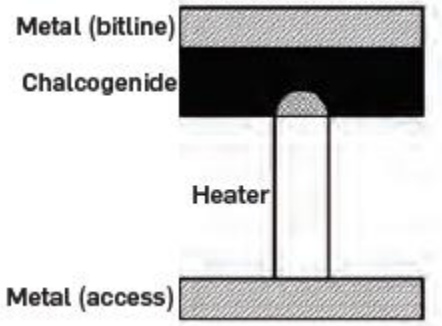
Phase Change Memory

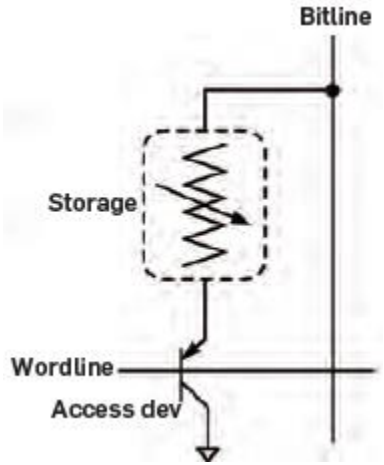




- ✓Storage element
- ✓2 metal electrodes
- ✓Resistive heater

Phase Change Memory



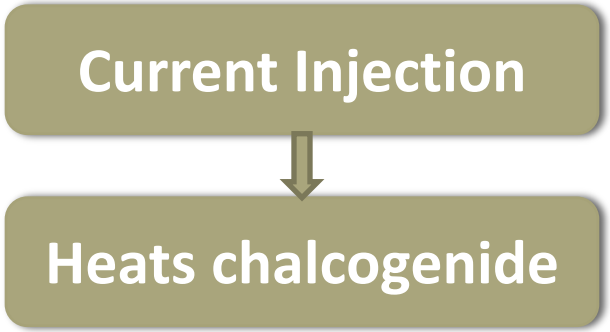


- ✓Storage element
- ✓2 metal electrodes
- ✓Resistive heater
- ✓Chalcogenide – Phase changing material

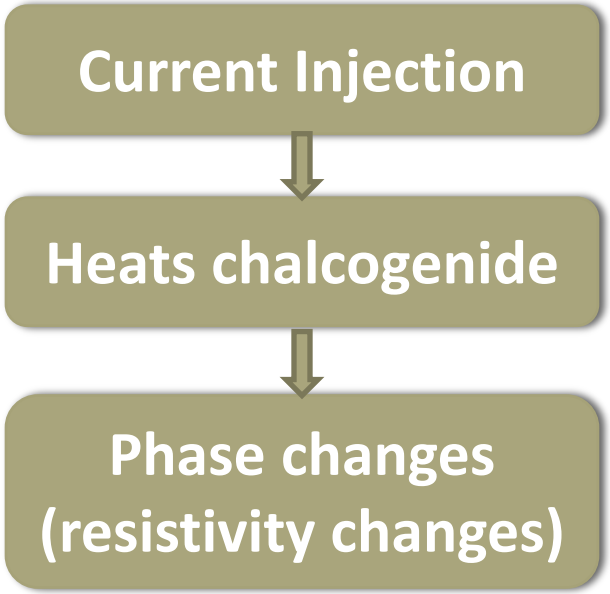
Operation

Current Injection

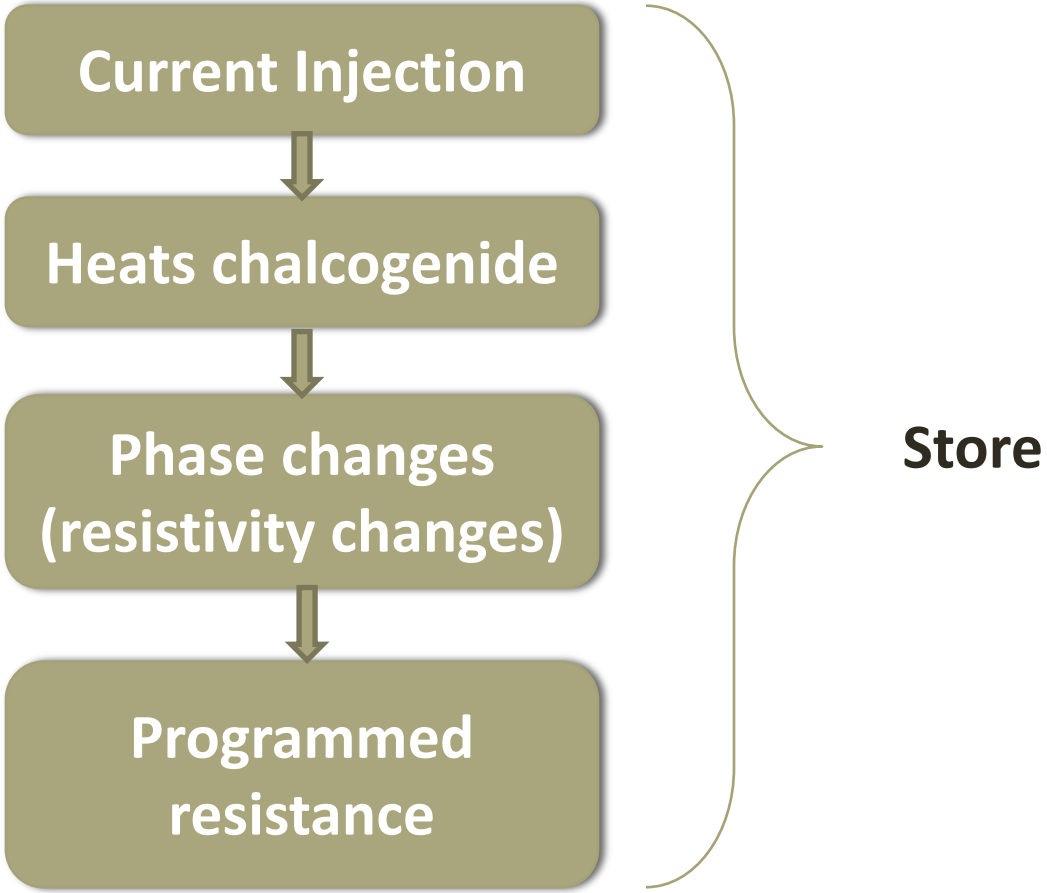
Operation



Operation


Current Injection
Heats chalcogenide
Phase changes
(resistivity changes)

Operation

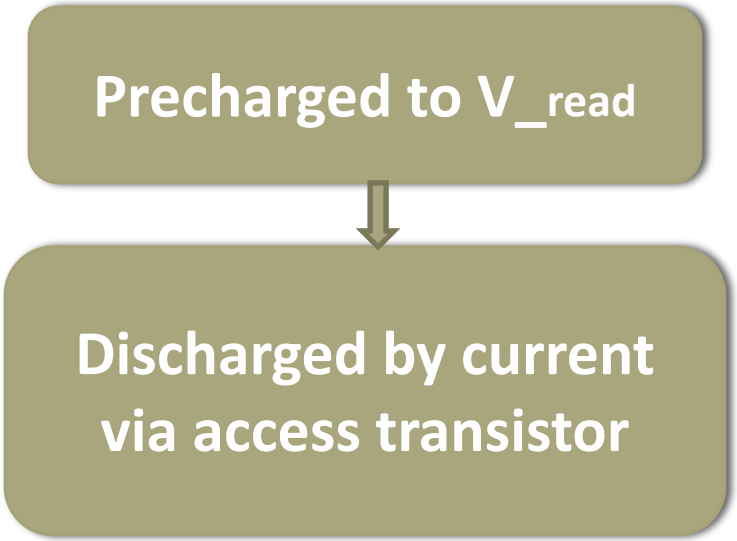


Non – Destructive !

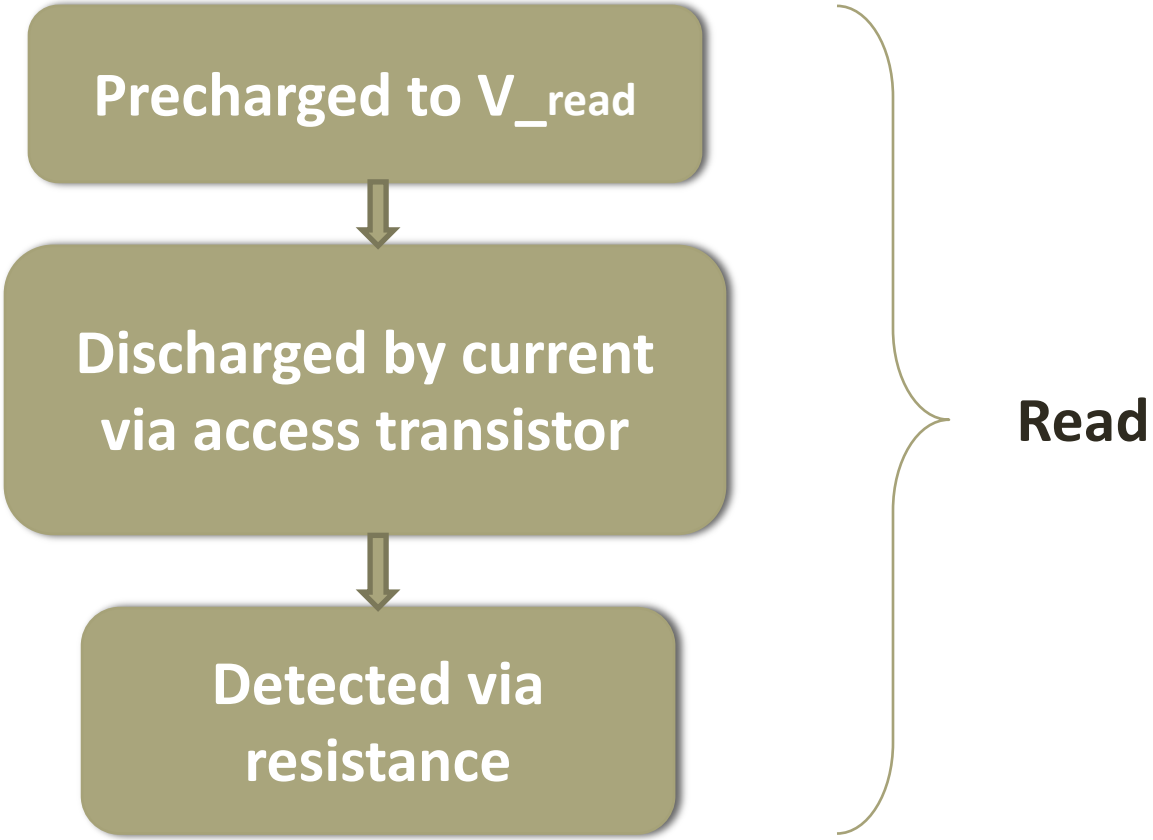
Operation

Precharged to V_read

Operation


Precharged to V_read
Discharged by current via access transistor

Operation


Precharged to V_read
Discharged by current via access transistor
Detected via resistance
Read

Challenges faced by PCM to compete with DRAM

Energy Cost

Energy intensive current injection for writes

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Endurance

Writes induces thermal expansion and contraction → degrades injection contacts

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Latency

High as compared to DRAM

Energy cost mitigating technique

Buffer organization

- ✓Narrow buffers – reduce PCM write energy

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- ✓Additional buffer rows

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Empirically → Reorganizing a single, wide buffer into multiple, narrow buffers reduce energy costs.

Improving memory lifetime

Partial writes

- ✓Write the same data that is already stored ← Unnecessary !!

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- ✓Tracking using dirty bits

Latency

What can be done ?

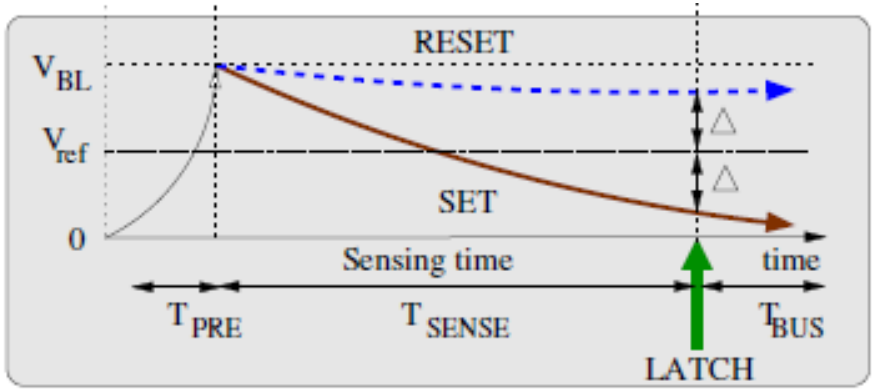


Fig: Timing components for the read operation

What can be done ?

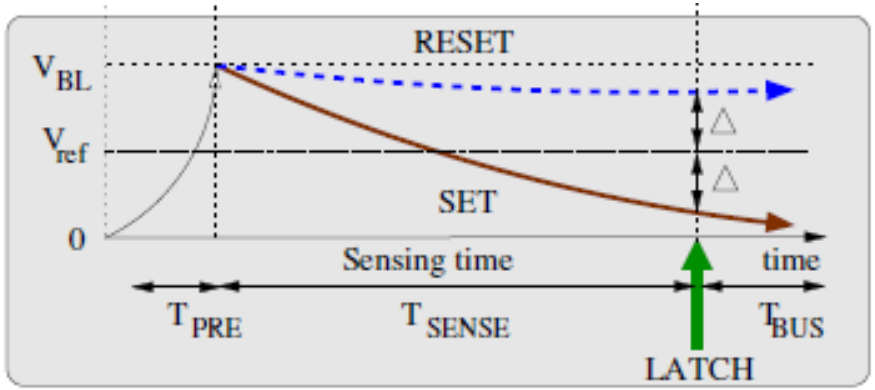
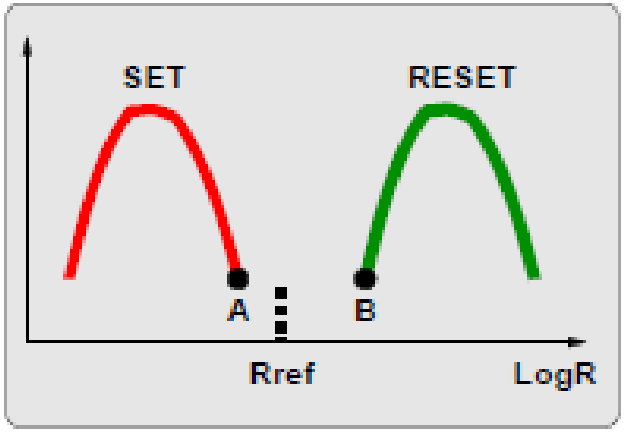


Fig: Timing components for the read operation

- ✓Sensing time dominates the read latency

Probability of cell state



Try to decrease sensing time.

Early Read

Reduce target resistance

Early Read

Reduce target resistance

RC time constant↓

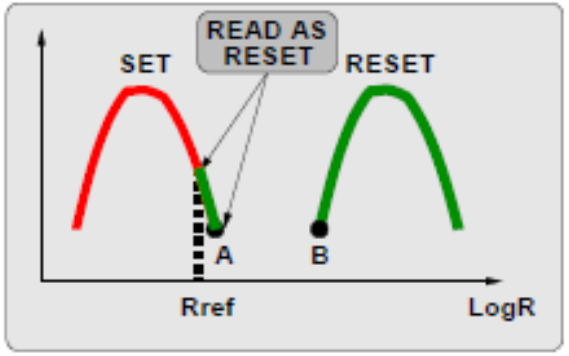
Early Read

Reduce target resistance

RC time constant↓

T_{SENSE} ↓

Probability of cell state



Trade – off ?

- ✓ BER (Bit Error Rate)

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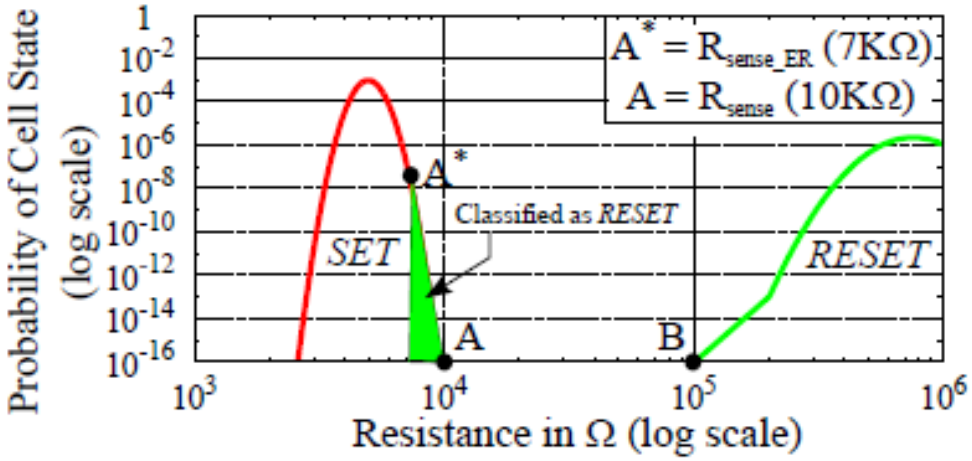
- A – 7kΩ → BER – 10^{-16}

  A* - 10kΩ → BER – 10^{-5}



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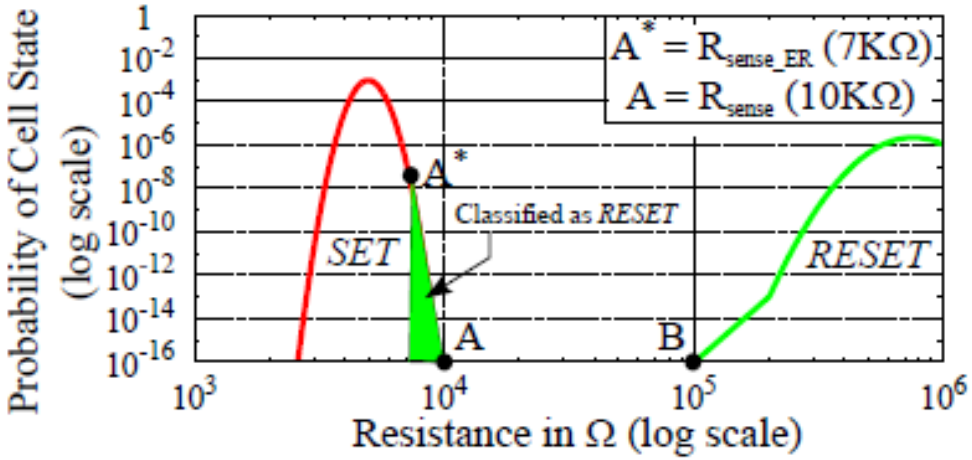
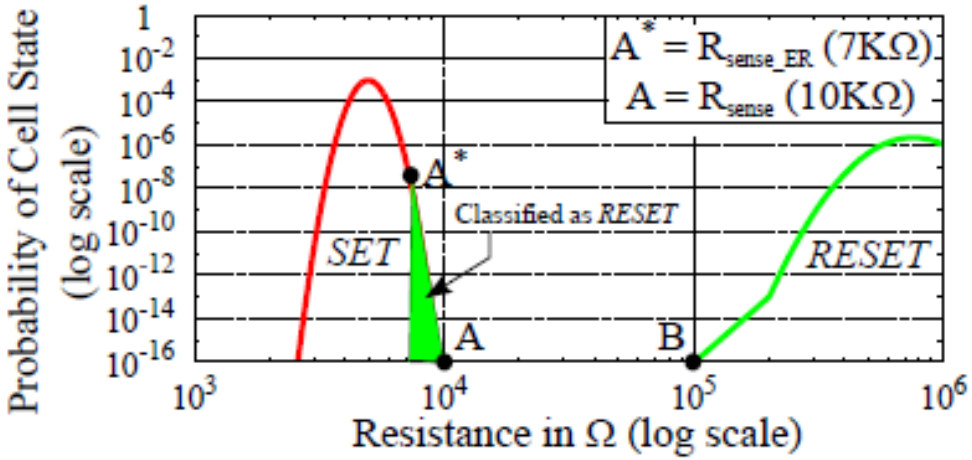
- BER increases exponentially



Trade – off ?

- ✓BER (Bit Error Rate)
- A – 7kΩ → BER – 10^{-16}

  A* - 10kΩ → BER – 10^{-5}
- BER increases exponentially
- Unidirectional errors → Berger Code



Turbo read

Sensing Voltage ↑

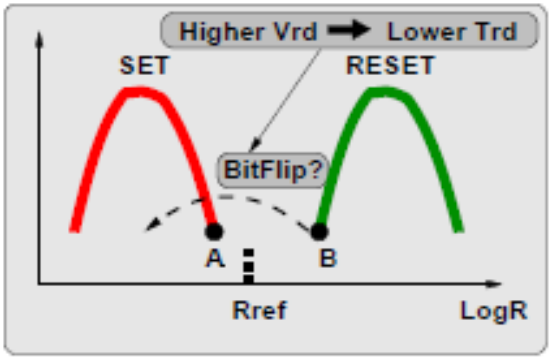
Turbo read

Sensing Voltage ↑

T_{SENSE} ↓

At the cost of some data errors

Probability of cell state



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Energy Costs	Baseline 2.2x → 1x

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Lifetime	More than 10 years

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	PCM
Energy Costs	Baseline 2.2x → 1x
Lifetime	More than 10 years
Latency	Reduction of 30% on baseline

Thank You!

Questions?