

Snehil Verma

MASTER'S STUDENT · DEPARTMENT OF ELECTRICAL AND COMPUTER ENGINEERING

2501 Speedway, EER 5.860, Austin, TX 78712, United States

☎ (+1) 737-217-5056 | ✉ snehilv@utexas.edu | ✉ snehilverma41@gmail.com | 🏠 snehilverma41.github.io



Education

The University of Texas at Austin

4.0*/4.0

M.S. IN ELECTRICAL AND COMPUTER ENGINEERING

Fall 2018 - Present

TRACK: ARCHITECTURE, COMPUTER SYSTEMS, AND EMBEDDED SYSTEMS (ACSES)

Indian Institute of Technology, Kanpur

8.9/10

B.TECH IN ELECTRICAL ENGINEERING (WITH DISTINCTION)

Fall 2014 - Spring 2018

MINOR IN COMPUTER SYSTEMS, COMPUTER SCIENCE AND ENGINEERING

* Calculated at the end of Spring'19

Publications

- **S. Verma**, Q. Wu, B. Hanindhito, G. Jha, E. John, R. Radhakrishnan, and L. John, "Metrics for Machine Learning Workload Benchmarking," International Workshop on Performance Analysis of Machine Learning Systems (FastPath), In conjunction with *ISPASS*, March 2019. [Publication] [Presentation]
- R. Radhakrishnan, **S. Verma**, Q. Wu, B. Hanindhito, G. Jha, E. John, and L. John, "Demystifying Hardware Infrastructure Choices for Deep Learning Using MLPerf," *NVIDIA GPU Technology Conference (GTC)*, March 2019. [Presentation]
- **S. Verma**, N. Deshmukh, P. Agrawal, B. Panda, and M. Chaudhuri, "DFCM++: Augmenting DFCM with Early Update and Data Dependence-driven Value Estimation," 1st Championship Value Prediction (CVP-1), In conjunction with *45th International Symposium on Computer Architecture (ISCA 2018)*, June 2018. [Publication] [Presentation] [Code]

Experience and Projects

Power and Performance Debugging via Emulation

Samsung SARC | ACL

GPU PERFORMANCE INTERN MENTORED BY RAGHAVAN R. SRINIVASA

Summer'19 - Present

Qualitative and Quantitative analysis of the MLPerf benchmark suite

UT Austin

GRADUATE RESEARCH ASSISTANT AT LAB FOR COMPUTER ARCHITECTURE UNDER PROF. LIZY K. JOHN

Fall'18 - Present

- **FastPath, ISPASS'19**: Proposed a **new metric for benchmarking ML workloads** that consider time and accuracy from the perspective of comparing the hardware used for training. Showed that merely taking into account the time for training to multiple thresholds makes the metric less sensitive to the specific threshold chosen and the seed values
- **NVIDIA GTC'19**: An extensive study on the **impact of hardware infrastructure choices on deep learning performance**. Presented quantitative analysis on various configurations of Dell systems with NVIDIA GPUs using MLPerf [v0.5]
- **Under review**: Analyzed and characterized the MLPerf [v0.5] benchmark suite exposing various **system-level trends**

Improving Data Locality by Kernel Fusion in DNNs [PRESENTATION]

UT Austin

COURSE PROJECT FOR COMPARCH: PARALLELISM AND LOCALITY UNDER PROF. MATTAN EREZ

Spring'19

- Studied *Convolutional Sequence to Sequence Learning* model for translation, a part of **Facebook AI Research Sequence-to-Sequence Toolkit (FairSeq)** implemented using **PyTorch** (lacks support for explicit memory management)
- Explored various methods of performing kernel fusion involving libraries like **CUTLASS**, **cuBLAS**, and **cuDNN**
- Integrated our C++/CUDA extensions with PyTorch and showed **~2x reduction** w.r.t the global memory/L2\$/DRAM writes

Graph Placement Optimization on a HMS [REPORT] [PRESENTATION]

UT Austin

COURSE PROJECT FOR COMPARCH: USER SYSTEM INTERPLAY UNDER PROF. MATTAN EREZ

Fall'18

- Proposed a novel optimization technique that **statically** makes **fine-grain placement** decisions based on the natural properties of a graph: the number of incoming/outgoing edges, topology, frontier composition
- Modified a light-weight shared memory graph processing framework (**Ligra**) to incorporate the proposed method
- Evaluated the same, demonstrating its good adaptability and up to **2x performance improvement**

Value Prediction: DFCM++ [PUBLICATION] [PRESENTATION] [POSTER] [CODE]

IIT Kanpur

UNDERGRADUATE RESEARCHER UNDER PROF. B. PANDA AND PROF. M. CHAUDHURI

Spring'18

- Proposed a series of enhancements on top of existing DFCM predictor: **Early Update**, **Value Estimator**, **PC Blacklist**, and **Dynamic Context Length**. The design achieved an IPC improvement of **28.1%** with respect to the baseline, i.e, without any value predictor, and **40.2%** in comparison to the base DFCM
- Presented at 1st **Championship Value Prediction (CVP-1)**, **ISCA'18** and secured **second** position in the unlimited track

Perceptron Learning driven Cache Replacement policy [REPORT]

Texas A&M University

VISITING RESEARCH SCHOLAR AT HIGH PERFORMANCE COMPUTING LAB UNDER PROF. EUN J. KIM

Summer'17

- Familiarized myself with various cache performance improvement techniques such as **Reuse Prediction**, **Inclusive Cache Management** and **Sharing Awareness Cache Management**
- Proposed and modeled **Coherence-Aware Reuse Prediction** on **ZSim** that achieved a geometric mean speedup of **20%** over LRU and resulted in a **40%** drop in average MPKI with respect to LRU, when evaluated on PARSEC for 4 MB LLC

Emerging Non-Volatile Memory [PRESENTATION] [TERM PAPER]

IIT Kanpur

COURSE PROJECT UNDER PROF. YOGESH S. CHAUHAN AND PROF. BAQUER MAZHARI

Spring'18

- Studied various emerging **flexible** non-volatile memory technologies like **ReRAM**, **FeRAM**, **PCRAM**, and **Flash**
- Delved into the approaches for making flexible NVMs, their operating principles, and some common architectures
- Performed a literature survey on **binary metal-oxide resistive switching RAM**. The study encompasses the switching mechanism, design, and electrical characteristics of various binary metal-oxide ReRAMs

Other Projects

IIT Kanpur

- Designed a stable **PLL** with low power linear Current Starved VCO consuming a maximum power of $182\mu\text{W}$ [REPORT]
- Studied the **noise cancellation techniques** and effectively applied them to design a 2.4 GHz **Inductorless LNA**
- Employed **adaptive biasing** to design a two-stage folded cascode **OTA** suitable for large capacitive loads [REPORT]
- Implemented a BSIM4-like model on **Verilog-A** and extracted parameters using **IC-CAP** simulation software [REPORT]
- Designed a **H_∞ controller** and tuned it for desired performances in order to make the system robust [REPORT]
- Built an **all-terrain vehicle** capable of autonomous navigation using Embedded Systems and Google Maps API [PPT]
- Selected among the **top 5 best ideas** for a game developed using Unity3D Game Engine for **Microsoft Code.Fun.Do**

Technical Skills

Programming languages

C, C++, C#, CUDA, Regent, Java, Python, Bash, Perl, Verilog(-A), HSPICE

Tools / Platforms

perf, NVProf, NVVP, CACTI, PAPI, SimPoints, PINTool, Docker, Git, ~~TeX~~, Cadence Virtuoso, Synopsys, Silvaco (Athena and Atlas), PSPICE, Microcap, Mentor Graphics, Ardupilot, Arduino, Processing, MATLAB, GNU Octave

Selected Coursework

UT AUSTIN

Computer Architecture*

Comp Arch: User-System Interplay*

Comp Arch: Parallelism and Locality*

Superscalar Microprocessor Architecture*

IIT KANPUR

Computer Architecture

Microelectronics-I (Circuits), II (Devices)

Introduction To Flexible Electronics*

Modern Memory Systems*

Digital Electronics

S/C Optical Communication Devices*

Principles of Data Base Systems

Analog/Digital VLSI Circuits*

Power Electronics

Data Structures and Algorithms

Compact Modeling*

Robust Control Systems*

* indicates Graduate Level Courses

Scholastic Achievements

- Professional Development Award**, UT Austin - research presentation at **FastPath**, **ISPASS'19** 2019
- Second position** in unlimited track, **1st Championship Value Prediction**, **ISCA'18** 2018
- Microsoft Research India Travel Grant** - research presentation at **CVP-1**, **ISCA'18** 2018
- ISCA 2018 Student Travel Grant Award** and **Departmental (E.E.) Travel Grant Award**, IIT Kanpur 2018
- TAMU-IITK summer undergraduate research scholarship** - awarded to two students per department 2017
- Academic Excellence Award** - awarded to top 7% students in the institute 2015, 2017
- JEE Advanced 2014**, **All India Rank 387** amongst 120,000 candidates 2014
- KVPY National Fellowship**, Department of Science and Technology, Government of India 2014
- Certificate of Merit** at National Level, HBCSE - **International Chemistry Olympiad 2013-14** 2014

Teaching Experience

Academic Mentor

IIT Kanpur

INSTITUTE COUNSELLING SERVICE

Fall'15 - Spring'16

- Tutored students having difficulties in **Engineering Design and Graphics** by conducting institute level remedial classes and doubt-clearing sessions. Personally mentored academically weaker students to cope with their academic load