Snehil **Verma**

Master's Student · Department of Electrical and Computer Engineering
4305 Duval St, Apt. 311, Austin, TX 78751, United States
(+1) 737-217-5056 | snehilv@utexas.edu | snehilverma41@gmail.com | snehilverma41.github.io

Education

The University of Texas at Austin *-/ 4.0*
M.S. in Electrical and Computer Engineering *Fall 2018 - Present*
Track: Architecture, Computer Systems, and Embedded Systems (ACSES)

Indian Institute of Technology, Kanpur *8.9/ 10*
B.Tech in Electrical Engineering (with DISTINCTION) *Fall 2014 - Spring 2018*
Minor in Computer Systems, Computer Science and Engineering

Research Interests

Computer Architecture, Memory Systems, Performance Evaluation

Publications

- **Snehil Verma**, Nayan Deshmukh, Prakhar Agrawal, Biswabandan Panda, and Mainak Chaudhuri, "DFCM++: Augmenting DFCM with Early Update and Data Dependence-driven Value Estimation," 1st Championship Value Prediction (CVP-1), In *Proceedings of the 45th International Symposium on Computer Architecture (ISCA 2018)*, Los Angeles, USA, 2018. [Report] [Code] [Presentation]

Experience

Qualitative and Quantitative analysis of MLPerf benchmark suite *UT Austin*
Graduate Research Assistant under Prof. L. K. John *Fall 2018 - Present*

- Objective is to study the computational behavior of the benchmarks included in MLPerf suite on various platforms. With the data obtained from the measurement, we aim to identify the performance bottlenecks in order to motivate better designing of the hardware machines. The proposed abstract is accepted to appear in the **GPU Technology Conference (GTC) 2019** (AI and Deep Learning Conference held by NVIDIA)
- Motivated by the fact that measuring quality and performance at the same time is challenging, we are working on **new metrics** for Machine Learning Workloads. Our work is under submission to a conference

Value Prediction: DFCM++ [REPORT] [CODE] [PRESENTATION] *IIT Kanpur*
Undergraduate Researcher under Prof. B. Panda and Prof. M. Chaudhuri *January 2018 - June 2018*

- Proposed a series of enhancements on top of existing DFCM predictor: **Early Update**, **Value Estimator**, **PC Blacklister**, and **Dynamic Context Length**. The design achieved an IPC improvement of **28.1%** with respect to the baseline, i.e, without any value predictor, and **40.2%** in comparison to the base DFCM

Perceptron Learning driven Cache Replacement policy [REPORT] *Texas A&M University*
Visiting Research Scholar under Prof. E. J. Kim *June 2017 - July 2017*

- Familiarized myself with various cache performance improvement techniques such as **Reuse Prediction**, **Inclusive Cache Management** and **Sharing Awareness Cache Management**
- Proposed **Coherence-Aware Reuse Prediction** that achieved a geometric mean speedup of **20%** over LRU and resulted in a **40%** drop in average MPKI with respect to LRU, for 4 MB LLC

Selected Projects

Emerging Non-Volatile Memory [PRESENTATION] [TERM PAPER] *IIT Kanpur*
Department of Electrical Engineering *January 2018 - April 2018*

- Studied various emerging **flexible** non-volatile memory technologies like **ReRAM**, **FeRAM**, **PCRAM**, and **Flash**
- Prof. B. Mazhari guided the research as a part of the course Introduction to Flexible Electronics. The work comprised of the approaches for making flexible NVMs, their operating principles, and some common architectures
- Performed a literature survey on **binary metal-oxide resistive switching RAM**. The study, supervised by Prof. Chauhan, encompasses the switching mechanism, design and electrical characteristics of various binary metal-oxide ReRAMs

Circuit Design and Implementation

IIT Kanpur

Department of Electrical Engineering

- Designed a stable **PLL** with low power linear Current Starved VCO consuming a maximum power of 182μW [REPORT]
- Studied the **noise cancellation techniques** and effectively applied them to design a 2.4 GHz **Inductorless LNA**
- Employed **adaptive biasing** to design a two-stage folded cascode **OTA** suitable for large capacitive loads [REPORT]

Verilog-A implementation and parameter extraction for BSIM4 like model [REPORT]

IIT Kanpur

Course project for Compact Modelling under Prof. Y. S. Chauhan *January 2018 - April 2018*

- Implemented a threshold voltage based model taking second-order effects, such as **mobility degradation** with vertical field, **velocity saturation**, channel length modulation (**CLM**), and drain induced barrier lowering (**DIBL**), into account
- Extracted the parameters using IC-CAP simulation software which were then tuned to match the measured TCAD data
- Examined the model for **Gummel Symmetry Test**, **Derivative Test**, and **Inverter Characteristics**

Other Projects

IIT Kanpur

- Designed a **H_∞ controller** and tuned it for desired performances in order to make the system robust [REPORT]
- Performed a literature survey on Multiple-Input Multiple-Output (**MIMO**) systems and its potential in 4G and 5G [REPORT]
- Built an **all-terrain vehicle** capable of autonomous navigation using Embedded Systems and Google Maps API [PPT]
- Designed a website implementing a miniature version of the **railway inquiry system** to handle standard queries
- Selected among the **top 5 best ideas** for a game developed using Unity3D Game Engine for **Microsoft Code.Fun.Do**

Technical Skills

Programming languages C, C++, C#, Java, Python, Bash, Perl, Verilog, Verilog-A, HSPICE, MySQL

Tools / Platforms PINTool, Cadence, Synopsys, Silvaco (Athena and Atlas), PSPICE, Microcap, Mentor Graphics, Ardupilot, Arduino, Processing, MATLAB, GNU Octave, CodeVisionAVR, MS Visual Studio, Git, LaTeX, Unity, AutoCAD, SolidWorks

Selected Coursework

UT Austin

Computer Architecture*†
Comp Arch: User System Interplay*†
Comp Arch: Parallelism and Locality*‡
Superscalar Microprocessor Architecture*‡

IIT Kanpur

Computer Architecture	Microelectronics-I (Circuits), II (Devices)	Introduction To Flexible Electronics*
Modern Memory Systems*	Digital Electronics	S/C Optical Communication Devices*
Principles of Data Base Systems	Analog/Digital VLSI Circuits*	Power Electronics
Data Structures and Algorithms	Compact Modeling*	Robust Control Systems*

* indicates *Graduate Level Courses* † indicates *ongoing* ‡ indicates *to be taken in Spring'19*

Scholastic Achievements

- Secured **second position** in the unlimited track of **1st Championship Value Prediction, ISCA'18**
- Awarded with a **travel grant** of $1500 by **Microsoft Research Labs, India** for attending and presenting at CVP-1, ISCA'18
- Recipient of the **ISCA 2018 Student Travel Grant Award** and the **Departmental (E.E.) Travel Grant Award**, IIT Kanpur
- Recipient of **TAMU-IITK summer undergraduate research scholarship 2017** (awarded to two students per branch)
- Received **Academic Excellence Award** for outstanding academic performance (awarded to top 7% students in the institute) for the academic years 2014-15 and 2016-17
- Received **A* grade** in 3 courses, including Electrical Engineering Lab I (awarded to **top 1-2%** students in a course)
- Secured **All India Rank 387** in **JEE Advanced 2014**, amongst 120 thousand successful candidates selected from over 1.4 million aspirants who appeared for JEE Mains 2014
- Selected for the **Kishore Vaigyanik Protsahan Yojana (KVPY)** Scholarship in the year 2014, funded by the Department of Science and Technology, Government of India, and secured **All India Rank 236** in the national test
- Awarded **Certificate of Merit** by HBCSE in **International Chemistry Olympiad 2013-14** at the **National Level**

Teaching Experience

Academic Mentor

IIT Kanpur

Institute Counselling Service *July 2015 - April 2016*

- Tutored students having difficulties in **Engineering Design and Graphics** by conducting institute level as well as Hall level remedial classes and doubt-clearing sessions
- Personally mentored academically weaker students to cope with their academic load