

Snehil Verma

MASTER'S STUDENT · DEPARTMENT OF ELECTRICAL AND COMPUTER ENGINEERING

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Education

Cockrell School of Engineering, The University of Texas at Austin

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M.S. IN ELECTRICAL AND COMPUTER ENGINEERING

Expected 2020

TRACK: ARCHITECTURE, COMPUTER SYSTEMS, AND EMBEDDED SYSTEMS (ACSES)

Indian Institute of Technology, Kanpur

8.9/10

B.TECH IN ELECTRICAL ENGINEERING (WITH DISTINCTION)

2018

MINOR IN COMPUTER SYSTEMS, COMPUTER SCIENCE AND ENGINEERING

Modi Public School, Kota

90.8 %

ALL INDIA SENIOR SCHOOL CERTIFICATE EXAMINATION, CBSE

2014

Delhi Public School, Jamshedpur

10/10

ALL INDIA SECONDARY SCHOOL EXAMINATION, CBSE

2012

Research Interests

Computer Architecture, Memory Systems

Publications

- **Snehil Verma**, Nayan Deshmukh, Prakhar Agrawal, Biswabandan Panda, and Mainak Chaudhuri, "DFCM++: Augmenting DFCM with Early Update and Data Dependence-driven Value Estimation," 1st Championship Value Prediction (CVP-1), In *Proceedings of the 45th International Symposium on Computer Architecture (ISCA 2018)*, Los Angeles, USA, 2018. [Report] [Code] [Presentation]

Research Experience

DFCM++ Value Predictor [REPORT] [CODE] [PRESENTATION]

IIT Kanpur

COURSE PROJECT FOR COMPUTER ARCHITECTURE UNDER PROF. PANDA AND PROF. CHAUDHURI

January 2018 - June 2018

- Reviewed the literature on **computational** and **context-based** value predictors
- Implemented multiple value predictors like last-value, stride, (D)FCM, and (D)VTAGE (state-of-the-art) predictors
- Proposed a series of enhancements on top of existing DFCM predictor: **Early Update**, **Value Estimator**, **PC Blacklist**, and **Dynamic Context Length**. The design achieved an IPC improvement of **28.1%** with respect to the baseline, i.e, without any value predictor, and **40.2%** in comparison to the base DFCM
- Showed the effectiveness of our enhancements on some of the state-of-the-art value predictors such as (D)VTAGE
- Presented at 1st **Championship Value Prediction (CVP-1)**, ISCA'18 and secured **second** position in the unlimited track

Emerging Non-Volatile Memory [PRESENTATION] [TERM PAPER]

IIT Kanpur

DEPARTMENT OF ELECTRICAL ENGINEERING

January 2018 - April 2018

- Studied various emerging **flexible** non-volatile memory technologies like **ReRAM**, **FeRAM**, **PCRAM**, and **Flash**
- Prof. B. Mazhari guided the research as a part of the course Introduction to Flexible Electronics. The work comprised of the approaches for making flexible NVMs, their operating principles, and some common architectures
- Performed a literature survey on **binary metal-oxide resistive switching RAM**. The study, supervised by Prof. Chauhan, encompasses the switching mechanism, design and electrical characteristics of various binary metal-oxide ReRAMs

Perceptron Learning Driven Coherence-Aware Reuse Prediction for LLC [REPORT]

Texas A&M University

RESEARCH PROJECT UNDER PROF. E. J. KIM, DEPARTMENT OF COMPUTER SCIENCE AND ENGINEERING

June 2017 - July 2017

- Performed extensive literature survey on replacement policies, and inclusive, non-inclusive and exclusive caches
- Familiarized myself with various cache performance improvement techniques such as **Reuse Prediction**, **Inclusive Cache Management** and **Sharing Awareness Cache Management**
- Used an execution-driven simulator **ZSim** to model detailed micro-architectural behaviors
- Employed 8 multi-threaded applications and kernels from the **PARSEC benchmark** suite for evaluation
- Proposed **Coherence-Aware Reuse Prediction** that achieved a **geometric mean speedup of 20%** over LRU and resulted in a **40% drop in average MPKI** with respect to LRU, for 4 MB LLC
- Extended the work under the supervision of Prof. B. Panda, Department of Computer Science and Engineering, IIT Kanpur. Studied the correlation between the shared status of a cache block and its chances of being reused [PPT]

Phase Locked Loop (Design and Implementation) [REPORT]

IIT Kanpur

UNDERGRADUATE PROJECT UNDER PROF. S. QURESHI, DEPARTMENT OF ELECTRICAL ENGINEERING

January 2017 - May 2017

- Studied PLL and its various blocks i.e **Phase-Frequency Detector**, **Charge Pump** and **Voltage Controlled Oscillator**
- Realized the whole circuit on **Cadence Virtuoso** using SCL's 180nm CMOS technology library
- Designed a **low power linear Current Starved VCO** which consumed a maximum power of 182μW
- Performed **stability analysis** on the whole circuit and the Low Pass Filter was modified to attain enhanced stability
- Pre-layout simulation results: Settling time of the PLL (±5%) came out to be around 33μs and Lock time around 125μs

Design of 2.4 GHz Inductorless Low-Noise Amplifier (LNA)

IIT Kanpur

RESEARCH PROJECT UNDER PROF. Y. S. CHAUHAN, DEPARTMENT OF ELECTRICAL ENGINEERING

May 2016 - July 2016

- Studied the **noise cancellation techniques** of inductorless LNAs, and effectively applied them to design a better circuit
- Designed the schematic of the circuit on **Cadence Virtuoso Analog Design Environment** (IC 616)
- Extracted the netlist and modified the same in **SPICE3** in accordance with the commercial **Tower Semiconductor/SCL** 180 nm CMOS technology library for the simulation
- Coded for **S-parameter and Linearity Analyses** and simulated the same on **Synopsys HSPICE (RF)**
- Validated that LNA designed without on-chip inductors achieves **performance comparable** to inductor-based designs

Selected Projects

Verilog-A implementation and parameter extraction for BSIM4 like model [REPORT]

IIT Kanpur

COURSE PROJECT FOR COMPACT MODELLING UNDER PROF. Y. S. CHAUHAN

January 2018 - April 2018

- Implemented a threshold voltage based model taking second-order effects, such as **mobility degradation** with vertical field, **velocity saturation**, channel length modulation (**CLM**), and drain induced barrier lowering (**DIBL**), into account
- Extracted the parameters using IC-CAP simulation software which were then tuned to match the measured TCAD data
- Examined the model for **Gummel Symmetry Test**, **Derivative Test**, and **Inverter Characteristics**

Mini Railway Inquiry System

IIT Kanpur

COURSE PROJECT FOR PRINCIPLES OF DATA BASE SYSTEMS UNDER PROF. M. ATRE

January 2018 - April 2018

- Designed a website implementing a miniature version of the railway inquiry system to handle standard queries such as trains between stations, fetch train route, and all reachable stations
- Optimized SQL queries by creating indexes on the most frequently used queries and creating a plan tree

Two-Stage Folded Cascode OTA Suitable for Large Capacitive Loads [REPORT]

IIT Kanpur

COURSE PROJECT FOR ANALOG/DIGITAL VLSI CIRCUITS UNDER PROF. S. QURESHI

August 2017 - November 2017

- Modified the circuit design mentioned in the paper titled *Enhanced Single-Stage Folded Cascode OTA Suitable for Large Capacitive Loads* [PAPER] and optimized the same for low power, better output voltage swing and slew rate
- Employed **Adaptive biasing** and **current folding stage**, that provide class AB stage with **dynamic current boosting**
- Simulated the schematic and **layout** design, in **Mentor Graphics**, using TSMC's 180 nm CMOS technology library

Advances in MIMO : System Model and Potentials [REPORT]

IIT Kanpur

TERM PAPER FOR PRINCIPLES OF COMMUNICATION UNDER PROF. ADITYA K. JAGANNATHAM

August 2016 - November 2016

- Performed a literature survey on Multiple-Input Multiple-Output (MIMO) systems and its potential in **4G** and **5G**
- Explained the **mathematical modeling** of MIMO systems along with their advantages and drawbacks
- Provided a detailed review on latest development in MIMO domain such as **Multi-user MIMO**, **Massive MIMO** and **MIMO-OFDM** techniques, and further emphasizing their importance in cellular communication systems

Evaluating "Reducing Risk In Type 1 Diabetes Using H_∞ Control" [REPORT]

IIT Kanpur

COURSE PROJECT FOR ROBUST CONTROL SYSTEMS UNDER PROF. RAMPRASAD POTLURI

August 2016 - November 2016

- Evaluated and reproduced the results of the paper titled *Reducing Risk In Type 1 Diabetes Using H_∞ Control* [PAPER]
- Designed the **H_∞ controller** and tuned it for desired performances in order to make the system as **robust** as possible
- Designed the **Iodine Feedback Loop** and conceptualised the role of **safety mechanism** used in the research paper

Semi-Autonomous Surveillance and Transportation Robot (SASTR) [PPT]

IIT Kanpur

SUMMER PROJECT UNDER ROBOTICS CLUB, STUDENTS GYMKHANA

May 2015 - June 2015

- Designed an all-terrain vehicle that could travel autonomously from one place to another
- Programmed **Arduino** microcontroller to receive the data from different sensors like **GPS** and **IMU**, and transmit the required data to the base (a computer) via wireless module **Telemetry**
- Implemented **PID controller** in order to minimize the deviation of the robot from the actual path
- Implemented the **Direction Cosine Matrix (DCM) Algorithm** to extract roll, pitch and yaw from the **IMU** of the robot
- Developed a **GUI** application, using **C#** language, to input destination from the user and find the shortest path to the destination. Application ensured smooth transmission of data between user and the robot via **serial communication**

Scholastic Achievements

- Secured **second position** in the unlimited track of **1st Championship Value Prediction, ISCA'18**
- Awarded with a **travel grant** of \$1500 by **Microsoft Research Labs, India** for attending and presenting at CVP-1, ISCA'18
- Recipient of the **ISCA 2018 Student Travel Grant Award** and the **Departmental (E.E.) Travel Grant Award**, IIT Kanpur
- Recipient of **TAMU-IITK summer undergraduate research scholarship 2017** (awarded to two students per branch)
- Received **Academic Excellence Award** for outstanding academic performance (awarded to top 7% students in the institute) for the academic years 2014-15 and 2016-17
- Received **A* grade** in 3 courses, including Electrical Engineering Lab I (awarded to **top 1-2%** students in a course)
- Secured **All India Rank 387** in **JEE Advanced 2014**, amongst 120 thousand successful candidates selected from over 1.4 million aspirants who appeared for JEE Mains 2014
- Selected for the **Kishore Vaigyanik Protsahan Yojana (KVPY)** Scholarship in the year 2014, funded by the Department of Science and Technology, Government of India, and secured **All India Rank 236** in the national test
- Awarded **Certificate of Merit** by HBCSE in **International Chemistry Olympiad 2013-14** at the **National Level**

Technical Skills

Programming languages

C, C++, C#, Java, Python, Bash, Perl, Verilog, Verilog-A, HSPICE, MySQL

Tools / Platforms

PINTool, Cadence, Synopsys, Silvaco (Athena and Atlas), PSPICE, Microcap, Mentor Graphics, Ardupilot, Arduino, Processing, MATLAB, GNU Octave, CodeVisionAVR, MS Visual Studio, Git, \LaTeX , Unity, AutoCAD, SolidWorks

Operating Systems

Linux, Windows

Selected Coursework

UT Austin (ongoing)

Computer Architecture*

Comp Arch: User System Interplay*

IIT Kanpur

Microelectronics-I (Circuits), II (Devices)

Introduction To Flexible Electronics*

Data Structures and Algorithms

Digital Electronics

S/C Optical Communication Devices*

Computer Architecture

Analog/Digital VLSI Circuits*

Power Electronics

Modern Memory Systems*

Compact Modeling*

Robust Control Systems*

Principles of Data Base Systems

* indicates *Graduate Level Courses*

Teaching Experience

Academic Mentor

IIT Kanpur

INSTITUTE COUNSELLING SERVICE

July 2015 - April 2016

- Tutored students having difficulties in **Engineering Design and Graphics** by conducting institute level as well as Hall level remedial classes and doubt-clearing sessions
- Personally mentored academically weaker students to cope with their academic load

Extra-Curricular Activities

- Selected among the **top 5 best ideas** for a game developed using Unity3D Game Engine for **Microsoft Code.Fun.Do**
- Designed an LED Matrix and coded **ATmega32** in order to simulate a game "Space Invaders" for the event Electromania in Techkriti'15, inter-college technical festival of IIT Kanpur
- Designed a **hand gesture controlled robot** using **flex sensors** in Takneek'15, inter-hostel technical competition of IITK
- Worked as a member of **brakes designing team**, a part of **Society of Automotive Engineers (SAE)** IIT Kanpur team
- Fabricated a **remote controlled aeroplane model** for the event Aviator in Takneek'14 and won **3rd prize** for the same

Miscellaneous

- Talks given:
 - Spring'18 | Plasticine: A Reconfigurable Architecture For Parallel Patterns [PPT]
 - Spring'18 | Flexible Non-volatile Memory [PPT]
 - Spring'18 | BeBoP: A Cost Effective Predictor Infrastructure for Superscalar Value Prediction
 - Fall'17 | Phase Change Memory [PPT]
 - Fall'17 | Memory Power Management via Dynamic Voltage/Frequency Scaling
 - Summer'17 & Fall'17 | Perceptron Learning Driven Coherence-Aware Reuse Prediction for LLC [PPT-TAMU] [PPT-IITK]
- Member of **SIGARCH ACM** and **TCCA**
- Blogs:
 - Talk attended on Qualcomm Datacenter Technologies & Centriq 2400 Processor by Dr. Niket Choudhary
 - My ISCA-2018 experience