Snehil **Verma**

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EDUCATION

The University of Texas at Austin **4.0/ 4.0**
M.S. in ECE, Track: Architecture, Computer Systems, and Embedded Systems (ACSES) Fall 2018 – Spring 2020

Indian Institute of Technology Kanpur **8.9/ 10**
B.Tech in Electrical Engineering (with DISTINCTION), Minor in Computer Systems Fall 2014 – Spring 2018

EXPERIENCE AND PROJECTS

GPU Hardware Internship **Samsung SARC | ACL**
Affiliated with Teams: PPA, Architecture, ML Strategic Planning, and Workload Characterization Summer'19 – Present

- Executed power/performance flows on SoC emulation platform to identify performance bottlenecks and blocks using high power
- Developed microbenchmarks targeted at specific architectural features, and initiated the research on ML-based power prediction
- Delved into the design exploration of Texture Cache, analyzed its performance, and studied SOTA Texture Compression techniques

Qualitative and Quantitative analysis of the MLPerf benchmark suite **UT Austin**
Graduate Research Assistant at Lab for Computer Architecture under Prof. Lizy K. John Fall'18 – Present

- **FastPath, ISPASS'19** : Proposed a new metric for benchmarking ML workloads from the perspective of comparing training hardware
- **NVIDIA GTC'19** : An extensive study on the impact of hardware infrastructure choices on deep learning performance for training
- **arXiv e-print** : Analyzed and characterized the MLPerf [v0.5] training benchmark suite exposing various system-level trends

Improving Data Locality by Kernel Fusion in DNNs [PPT] **UT Austin**
Course Project for Computer Architecture: Parallelism and Locality under Prof. Mattan Erez Spring'19

- Integrated our C++/CUDA extensions, performing kernel fusion, with PyTorch to optimize *Convolutional Seq-to-Seq Learning* model

Graph Placement Optimization on a Heterogeneous Memory System [REPORT] [PPT] **UT Austin**
Course Project for Computer Architecture: User System Interplay under Prof. Mattan Erez Fall'18

- Incorporated a novel fine-grain static graph placement technique on *Ligra* that takes decisions based on natural properties of the graph

Value Prediction: DFCM++ [PUBLICATION] [CODE] [PPT] **IIT Kanpur**
Course Project for Computer Architecture under Prof. B. Panda and Prof. M. Chaudhuri Spring'18

- Enhanced the existing DFCM predictor achieving an IPC improvement of 28.1% over the baseline and 40.2% over the base DFCM

Emerging Non-Volatile Memory [PPT] [TERM PAPER] **IIT Kanpur**
Course Project under Prof. Yogesh S. Chauhan and Prof. Baquer Mazhari Spring'18

- Performed a literature survey on emerging flexible NVMs encompassing their operating principles and some common architectures
- Studied various binary metal-oxide resistive switching RAMs, their switching mechanisms, designs, and electrical characteristics

Perceptron Learning Driven Coherence-Aware Reuse Prediction for LLC [REPORT] **Texas A&M University**
Visiting Research Scholar at High Performance Computing Lab under Prof. Eun J. Kim Summer'17

- Modeled Coherence-Aware Reuse Prediction on ZSim that achieved a speedup of 20% over LRU when evaluated on PARSEC

Other Projects **UT Austin, IIT Kanpur**

- Developed an assembler and a cycle-accurate simulator for LC-3b RISC ISA capable of handling virtual to physical memory translation
- Coded best-offset hardware prefetcher highlighting its IPC and MPKI characteristics against next-line and IP-stride prefetchers
- Implemented a threshold voltage based BSIM4-like model on Verilog-A and extracted parameters using IC-CAP simulation [REPORT]
- Designed a low-power PLL [REPORT] , a 2.4GHz inductorless LNA, and a 2-stage folded cascode OTA employing adaptive biasing [REPORT]
- Built an all-terrain vehicle capable of autonomous navigation using Embedded Systems and Google Maps API [PPT]
- Selected among the top 5 best ideas for a game developed using Unity3D Game Engine for Microsoft Code.Fun.Do

TECHNICAL SKILLS

PROGRAMMING	C, C++, CUDA, OpenCL, OpenGL, Regent, Python, Bash, Perl, Verilog, Verilog-A, HSPICE, MySQL
TOOLS / PLATFORMS	perf, NVProf, CACTI, PAPI, SimPoints, PIN, Cadence Virtuoso, Synopsys, Silvaco, Mentor Graphics

RELEVANT COURSEWORK

COMPUTER SYSTEMS & ELECTRONICS	Computer Architecture, CompArch: User-System Interplay, CompArch: Parallelism and Locality, Superscalar Microprocessor Arch, Modern Memory Systems, Operating Systems, High-Speed Computer Arithmetic, Principles of Data Base Systems, Microelectronics, Digital Electronics, Analog/Digital VLSI Circuits
OTHER COURSES	Data Structures and Algorithms, Probability and Statistics, Compact Modeling

SCHOLASTIC ACHIEVEMENTS

- **Professional Development Award, UT Austin** - research presentation at **FastPath, ISPASS'19** 2019
- **Second position** in unlimited track, **1st Championship Value Prediction, ISCA'18** 2018
- **Microsoft Research India Travel Grant** - research presentation at **CVP-1, ISCA'18** 2018
- **TAMU-IITK summer undergraduate research scholarship** - awarded to two students per department 2017
- **Academic Excellence Award** - awarded to top 7% students in the institute 2015, 2017
- **JEE Advanced 2014** , All India Rank 387 amongst 120,000 candidates 2014