Snehil **Verma**

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EDUCATION

Cockrell School of Engineering, The University of Texas at Austin **-/ 4.0**
M.S. in Electrical and Computer Engineering, Track: Architecture, Computer Systems, and Embedded Systems (ACSES) Expected 2020

Indian Institute of Technology, Kanpur **8.9/ 10**
B.Tech in Electrical Engineering (with DISTINCTION), Minor in Computer Systems, Computer Science and Engineering 2018

EXPERIENCE

DFCM++ Value Predictor (Second position in unlimited track at CVP-1, ISCA'18) [REPORT] [CODE] [PPT] **IIT Kanpur**
Course Project for Computer Architecture under Prof. Panda and Prof. Chaudhuri January 2018 - June 2018

- Proposed a series of enhancements on top of existing DFCM predictor: **Early Update** , **Value Estimator** , **PC Blacklister** , and **Dynamic Context Length** . The design achieved an IPC improvement of **28.1%** with respect to the baseline, i.e, without any value predictor, and **40.2%** in comparison to the base DFCM

Emerging Non-Volatile Memory [PPT] [TERM PAPER] **IIT Kanpur**
Department of Electrical Engineering January 2018 - April 2018

- Performed a literature survey on emerging **flexible** non-volatile memory technologies like **ReRAM** , **FeRAM** , **PCRAM** , and **Flash**
- The work comprised of the approaches for making flexible NVMs, their operating principles, and some common architectures
- Studied various **binary metal-oxide resistive switching RAMs** , their switching mechanisms, designs and electrical characteristics

Perceptron Learning Driven Coherence-Aware Reuse Prediction for LLC [REPORT] **Texas A&M University**
Research project under Prof. E. J. Kim, Department of Computer Science and Engineering June 2017 - July 2017

- Familiarized myself with various cache performance improvement techniques such as **Reuse Prediction** , **Inclusive Cache Management** and **Sharing Awareness Cache Management** . Proposed **Coherence-Aware Reuse Prediction** that achieved a geometric mean speedup of **20%** over LRU and resulted in a **40%** drop in average MPKI with respect to LRU, for 4 MB LLC

PROJECTS

Circuit Design and Implementation | Department of Electrical Engineering **IIT Kanpur**

- Designed a stable **PLL** with low power linear Current Starved VCO which consumed a maximum power of 182μW [REPORT]
- Studied the noise cancellation techniques of inductorless LNAs, and effectively applied them to design a 2.4 GHz **Inductorless LNA**
- Employed adaptive biasing to design a two-stage folded cascode **OTA** suitable for large capacitive loads [REPORT]

Verilog-A implementation and parameter extraction for BSIM4 like model [REPORT] **IIT Kanpur**
Course project for Compact Modelling under Prof. Y. S. Chauhan January 2018 - April 2018

- Implemented a threshold voltage based model taking second-order effects, such as mobility degradation with vertical field, velocity saturation, channel length modulation (CLM), and drain induced barrier lowering (DIBL), into account
- Extracted the parameters using IC-CAP simulation software which were then tuned to match the measured TCAD data
- Examined the model for Gummel Symmetry Test, Derivative Test, and Inverter Characteristics

Other Projects **IIT Kanpur**

- Designed the H_∞ **controller** and tuned it for desired performances in order to make the system as robust as possible [REPORT]
- Performed a literature survey on **Multiple-Input Multiple-Output (MIMO)** systems and its potential in 4G and 5G [REPORT]
- Built an **all-terrain vehicle** capable of autonomous navigation using Embedded Systems and Google Maps API [PPT]
- Designed a website implementing a miniature version of the **railway inquiry system** to handle standard queries
- Selected among the **top 5 best ideas** for a game developed using Unity3D Game Engine for **Microsoft Code.Fun.Do**

TECHNICAL SKILLS

PROGRAMMING	C, C++, C#, Java, Python, Bash, Perl, Verilog, Verilog-A, HSPICE, MySQL
TOOLS/ PLATFORMS	PINTool, Cadence, Synopsys, Silvaco (Athena and Atlas), PSPICE, Mentor Graphics, Microcap, Ardupilot Arduino, Processing, MATLAB, CodeVisionAVR, Git, LaTeX, Unity, AutoCAD, SolidWorks

RELEVANT COURSEWORK

COMPUTER SYSTEMS & ELECTRONICS OTHER COURSES	Computer Architecture*, Computer Architecture: User System Interplay*, Modern Memory Systems Principles of Data Base Systems, Microelectronics, Digital Electronics, Analog/Digital VLSI Circuits Data Structures and Algorithms, Probability and Statistics, Compact Modeling

* Ongoing

SCHOLASTIC ACHIEVEMENTS

- Awarded with a travel grant of $1500 by **Microsoft Research Labs, India** for attending and presenting at CVP-1, ISCA'18
- Recipient of the **ISCA 2018 Student Travel Grant Award** and the **Departmental (E.E.) Travel Grant Award** , IIT Kanpur
- Recipient of **TAMU-IITK summer undergraduate research scholarship 2017** (awarded to two students per branch)
- Received **Academic Excellence Award** for outstanding academic performance for the academic years 2014-15 and 2016-17
- Secured **All India Rank 387** in **JEE Advanced 2014** , amongst 120 thousand successful candidates selected from over 1.4 million aspirants who appeared for JEE Mains 2014
- Selected for the **Kishore Vaigyanik Protsahan Yojana (KVPY)** Scholarship in the year 2014, funded by the Department of Science and Technology, Government of India, and secured **All India Rank 236** in the national test