Design of a 4-bit Counter Type/Ramp Type Analog to Digital converter (ADC)

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Abstract—**This paper presents the mixed signal design of a Counter Type/ Ramp Type ADC. The Digital part of the circuit i.e 4- bit counter is simulated on Makerchip tool. All the Simulations are done using eSim and Makerchip tool only. Since the counter used is taken to be 4-Bit, the input voltage that can be converted to analog is limited to 0-15V. A 4-Bit Digital to Analog Converter (DAC) is used as an internal part, having the step size of 1V.**

Keywords— ***ADC, DAC, Counter, Op-Amp/Comparator, Ramp.***

REFRENCE CIRCUIT DETAILS

Analog to Digital Converter is an electronic device that converts the analog data into digital form. Due to various advantages of the digital signals over analog signals such as easy processing and storage. The analog signal are converted into digital signals and the processing is done, after processing the signal it is converted back to analog form to get the original output. In this conversion from Analog to Digital, ADCs plays a vital role.

In this paper we will study about Counter type/ Ramp type DAC. It consists of following components such as: Counter, DAC, AND gate, Op-Amp. The block diagram of the Counter type/ Ramp type DAC is shown in the figure 1.

In Counter/Ramp type ADC, the analog voltage to be converted is applied to non-inverting terminal of the Op-Amp based comparator Circuit and the inverting terminal of comparator is connected to the output of the DAC. For the conversion, the binary counter is initially RESET and hence the output of the output of the DAC is 0V. The analog input applied to comparator is continuously compared with the DAC output during the conversion. If the analog input is greater than the DAC output, the comparator output is High and the counter is incremented and so the output from the DAC. Now again the DAC output is compared with the applied input if again input voltage (V_A) is greater than the applied voltage, the counter is increment and so the DAC output. This process is repeated until the DAC output becomes greater than the applied input voltage by some threshold V_T volts and the output of the comparator becomes Low.

For every sampling interval the DAC output follows a ramp fashion so that it is called as Digital ramp type ADC. And this ramp looks like stair cases for every sampling time so that it is also called as staircase approximation type ADC.

The conversion time of this ADC is given by,

$$T_c = \text{(No. of steps)}. T_{CLK.} \qquad (1)$$

Where,

$$T_{CLK}=1/f_{CLK}$$

Now if we consider the worst-case scenario, then the conversion time will be given by,

$$T_c(max) = (2^n-1). T_{CLK} \qquad (2)$$

Here, n= 4 (No. of Bits)

$$T_c(max)=15.T_{CLK} \qquad (3)$$

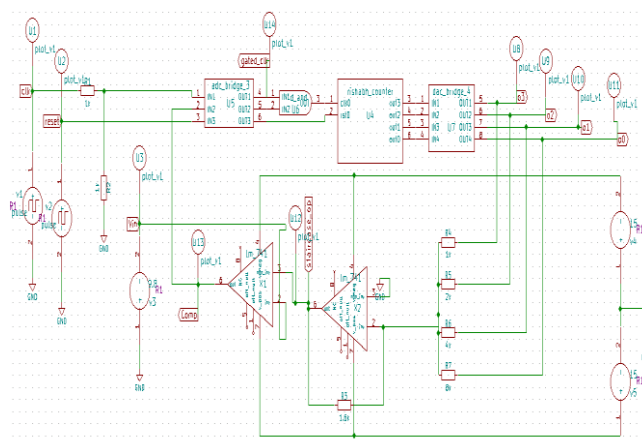## IMPLEMENTED CIRCUIT

Fig.1   Implemented Circuit of Counter Type/ Ramp Type
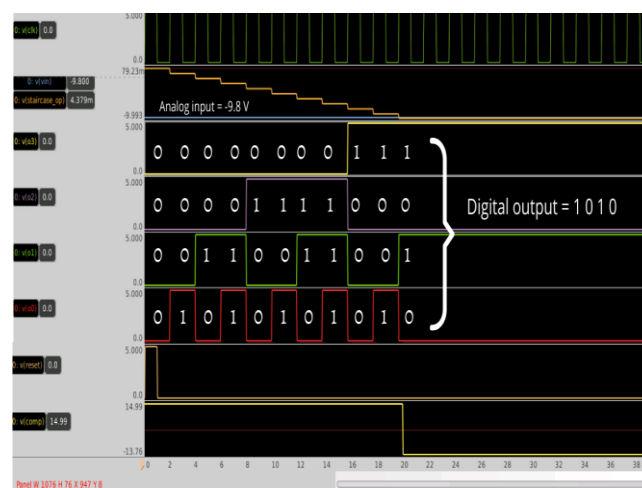
IMPLEMENTED CIRCUIT WAVEFORM

Fig.2   Implemented waveform of 4-Bit Counter Type ADC

REFRENCES

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