SPI MASTER DESIGN PARAMETERS

Technology Used: osu018(18nm Technology)

Total Area: 8930.20 (units sq) Microns

PLACEMENT ANALYSIS:

Total stdcells	193
Total cell width	7.50e+04
Total cell height	1.93e+05
Total cell area	7.50e+07
Total core area	7.50e+07
Average cell height	1.00e+03
FINAL NUMBER OF ROUTING TRACKS	53

6 routing layers

Metal1: 87 vertical tracks from -3um with 1um pitch

Metal2: 127 vertical tracks from -3.2um with 0.8um pitch

Metal3: 87 vertical tracks from -3um with 1um pitch

Metal4: 127 vertical tracks from -3.2um with 0.8um pitch

Metal5: 87 vertical tracks from -3um with 1um pitch

Metal6: 64 vertical tracks from -3.2um with 1.6um pitch

Summary: Total components = 193

Longest row has width 94.8 um.

PRE ROUTE-STA:

Computed maximum clock frequency (zero margin) = **689.47 MHz**

setup at destination = **191.309** hold at destination = **40.0909**

ROUTING ANALYSIS:

Total number of routes completed by the end of stage 3 are 1309 with 0 failed routed.

POST ROUTE-STA:

Computed maximum clock frequency (zero margin) = **667.034 MHz**

setup at destination = **191.196** hold at destination = **40.0432**