SPI SLAVE DESIGN PARAMETERS

Technology Used: osu018(18nm Technology)

Total Area: 6589.08 (units sq) Microns

PLACEMENT ANALYSIS:

Total stdcells	131
Total cell width	5.66e+04
Total cell height	1.31e+05
Total cell area	5.66e+07
Total core area	5.66e+07
Average cell height	1.00e+03
FINAL NUMBER OF ROUTING TRACKS	37

6 routing layers

Metal1: 64 vertical tracks from 0um with 1um pitch

Metal2: 128 vertical tracks from -3.2um with 0.8um pitch

Metal3: 64 vertical tracks from 0um with 1um pitch

Metal4: 128 vertical tracks from -3.2um with 0.8um pitch

Metal5: 64 vertical tracks from 0um with 1um pitch

Metal6: 64 vertical tracks from -3.2um with 1.6um pitch

Summary: Total components = 131

Longest row has width 95.6 um.

PRE ROUTE-STA:

Computed maximum clock frequency (zero margin) = **726.423 MHz**

setup at destination = **137.573**

hold at destination = **-3.75179**

ROUTING ANALYSIS:

Total number of routes completed by the end of stage 3 are 839 with 0 failed routed.

POST ROUTE-STA:

Computed maximum clock frequency (zero margin) = **702.022 MHz**

setup at destination = **138.456**

hold at destination = **-3.6104**