22bec121

Experiment – 7 Date:-7/3/2024

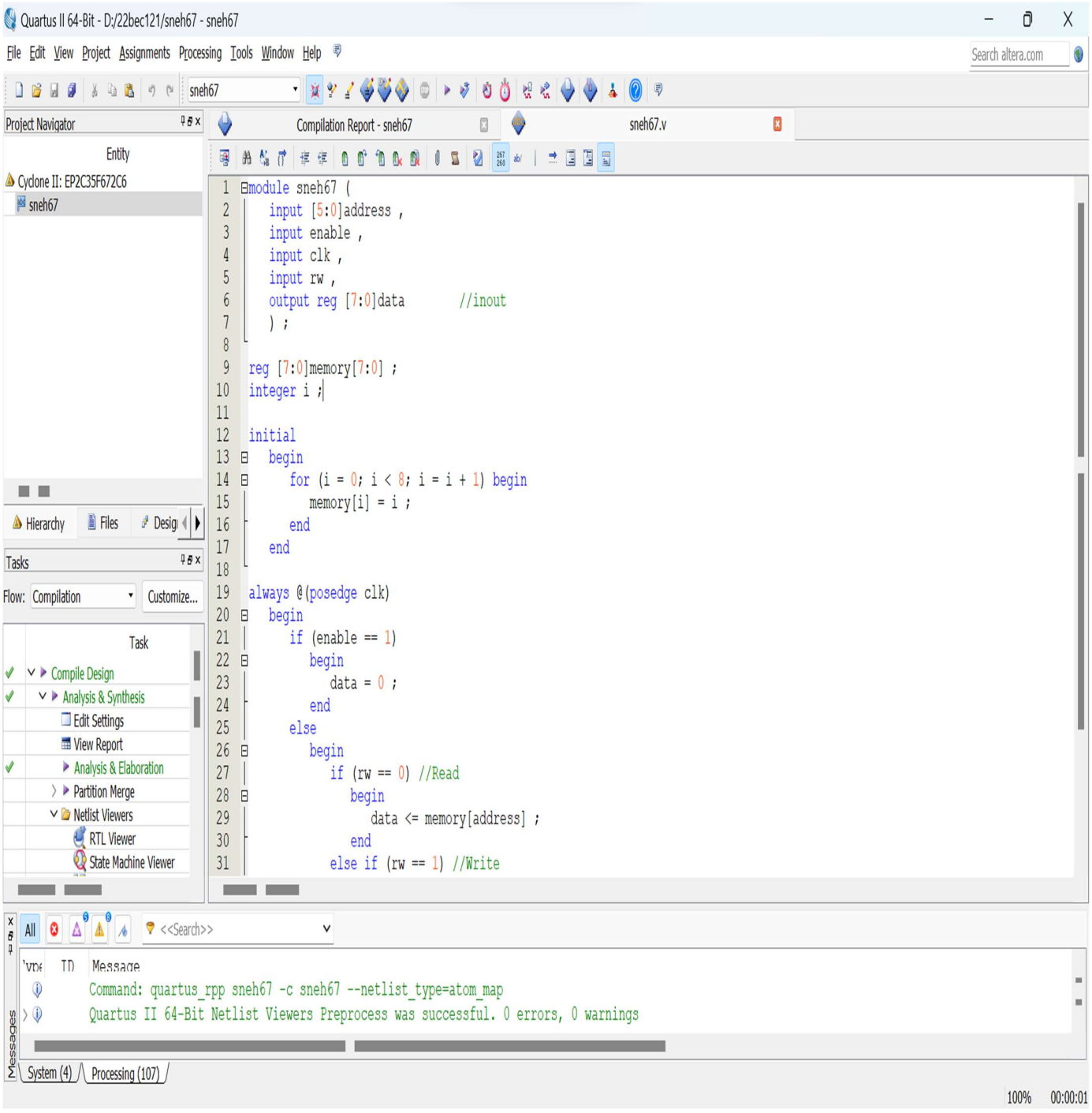
Lab Work

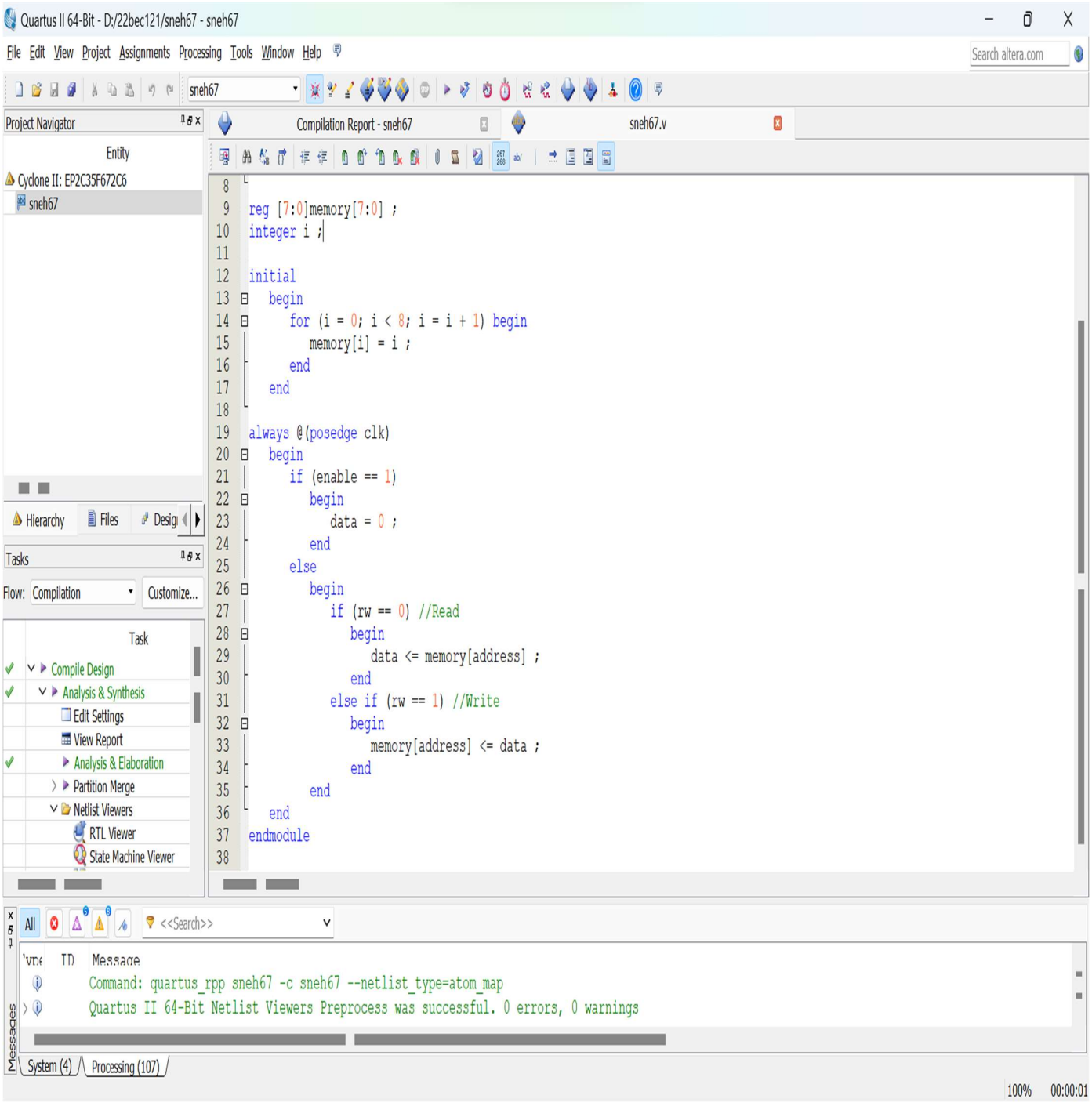
Q1 .To design a and implement a 8 x 8 RAM on FPGA .

Code (RAM)

```
module sneh67 (
        input [5:0]address ,
        input enable ,
        input clk ,
        input rw ,
        output reg [7:0]data       //inout
        ) ;

reg [7:0]memory[7:0] ;
integer i ;

initial
        begin
                for (i = 0; i < 8; i = i + 1) begin
                        memory[i] = i ;
                end
        end

always @(posedge clk)
        begin
                if (enable == 1)
                        begin
                                data = 0 ;
                        end
```

```
        else
            begin
                if (rw == 0) //Read
                    begin
                        data <= memory[address] ;
                    end
                else if (rw == 1) //Write
                    begin
                        memory[address] <= data ;
                    end
            end
    end
endmodule
```


Quartus II 64-Bit - D:/22bec121/sneh67 - sneh67
File Edit View Project Assignments Processing Tools Window Help
Search altera.com
sneh67
Project Navigator
Entity
Cyclone II: EP2C35F672C6
sneh67
Hierarchy
Files
Tasks
Flow: Compilation
Customize...
Task
Compile Design
Analysis & Synthesis
Edit Settings
View Report
Analysis & Elaboration
Partition Merge
Netlist Viewers
RTL Viewer
State Machine Viewer
Compilation Report - sneh67
sneh67.v
1 module sneh67 (
2 input [5:0]address ,
3 input enable ,
4 input clk ,
5 input rw ,
6 output reg [7:0]data //inout
7) ;
8
9 reg [7:0]memory[7:0] ;
10 integer i ;
11
12 initial
13 begin
14 for (i = 0; i < 8; i = i + 1) begin
15 memory[i] = i ;
16 end
17 end
18
19 always @(posedge clk)
20 begin
21 if (enable == 1)
22 begin
23 data = 0 ;
24 end
25 else
26 begin
27 if (rw == 0) //Read
28 begin
29 data <= memory[address] ;
30 end
31 else if (rw == 1) //Write
All
<<Search>>
Type ID Message
Command: quartus_rpp sneh67 -c sneh67 --netlist_type=atom_map
Quartus II 64-Bit Netlist Viewers Preprocess was successful. 0 errors, 0 warnings
Messages
System (4)
Processing (107)
100%
00:00:01


Quartus II 64-Bit - D:/22bec121/sneh67 - sneh67
File Edit View Project Assignments Processing Tools Window Help
Search altera.com
sneh67
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sneh67.v
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end
end
always @(posedge clk)
begin
if (enable == 1)
begin
data = 0 ;
end
else
begin
if (rw == 0) //Read
begin
data <= memory[address] ;
end
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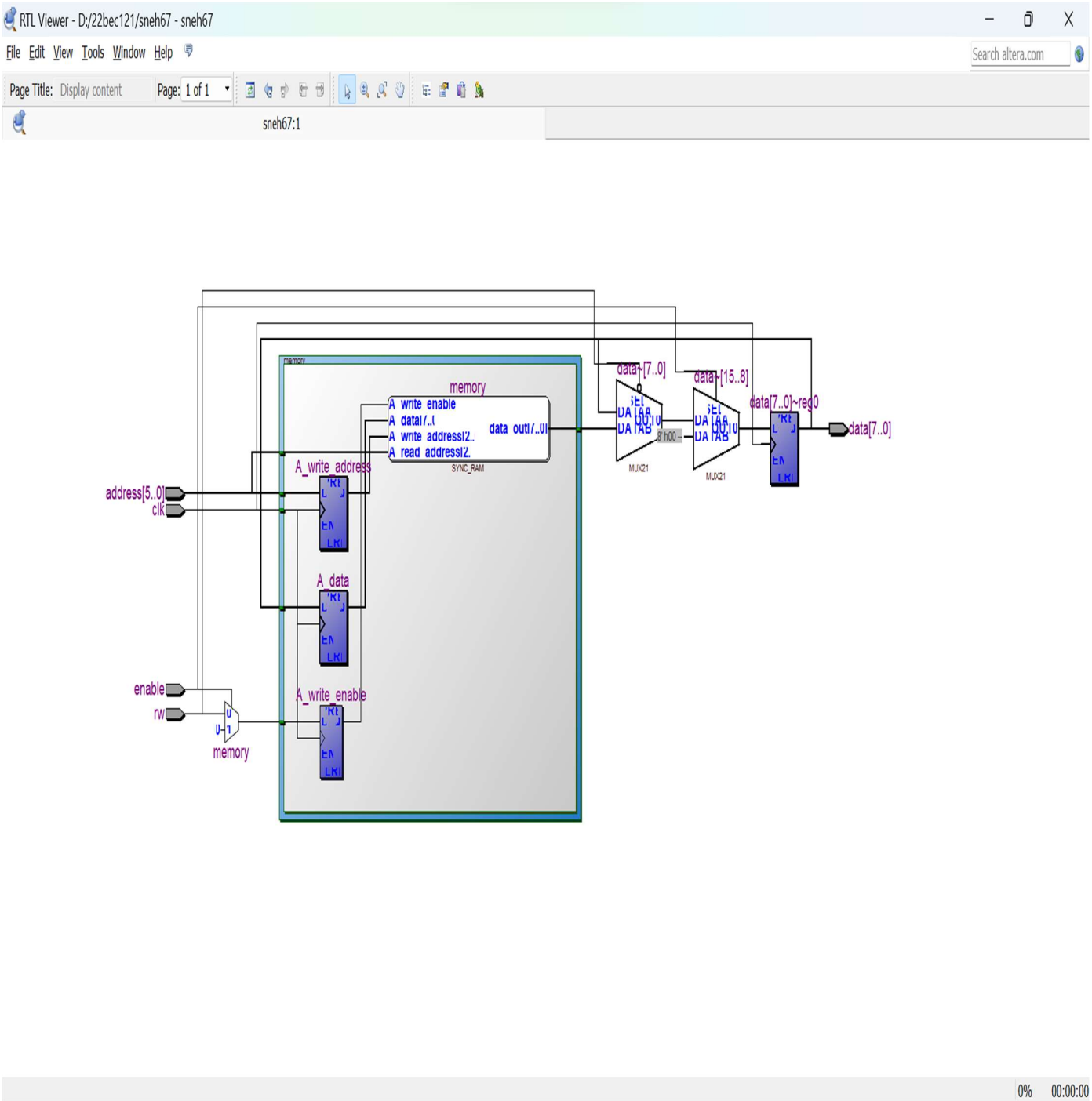
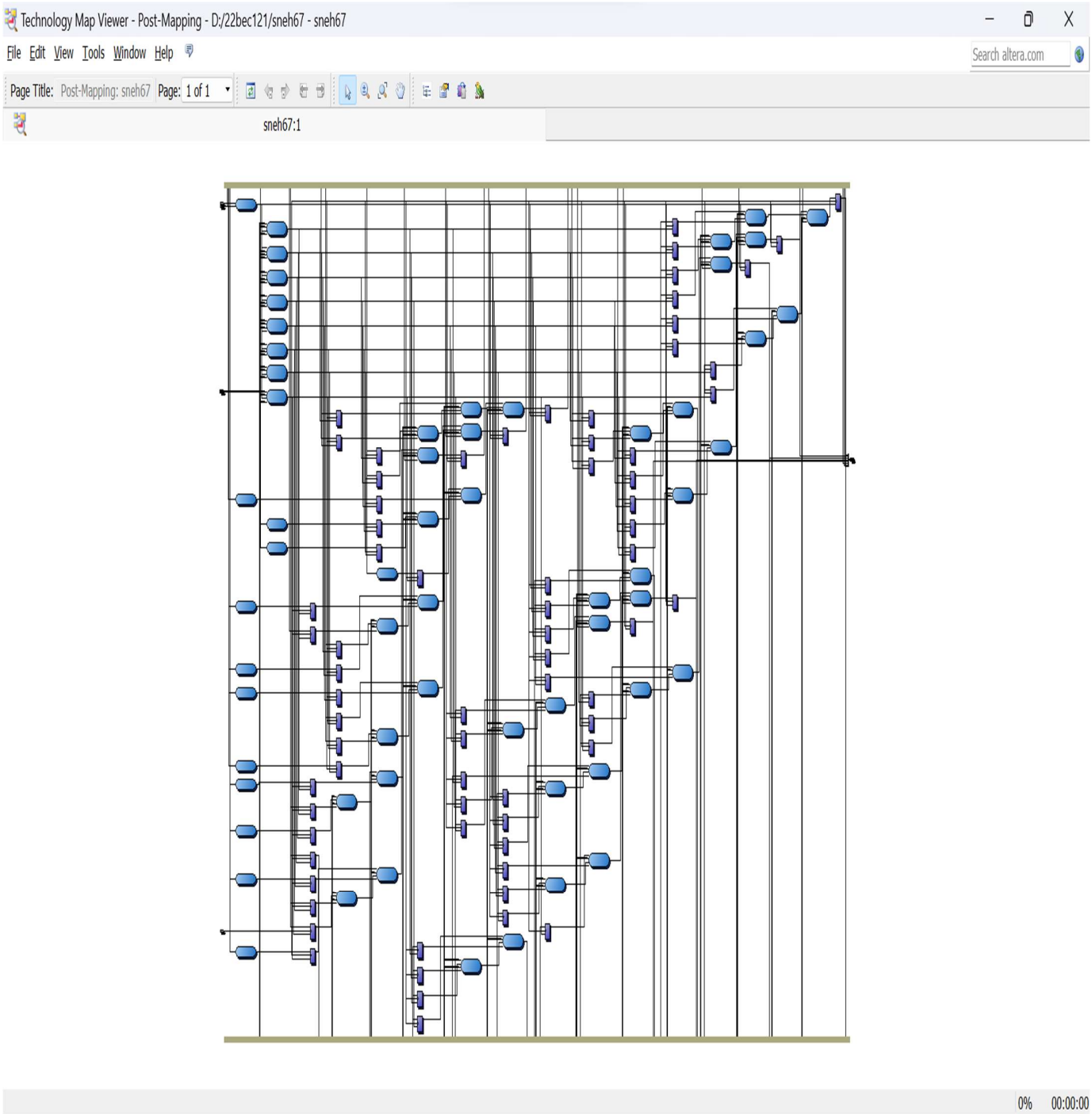
00:00:01

Output 1)Cyclone II (RTL View)

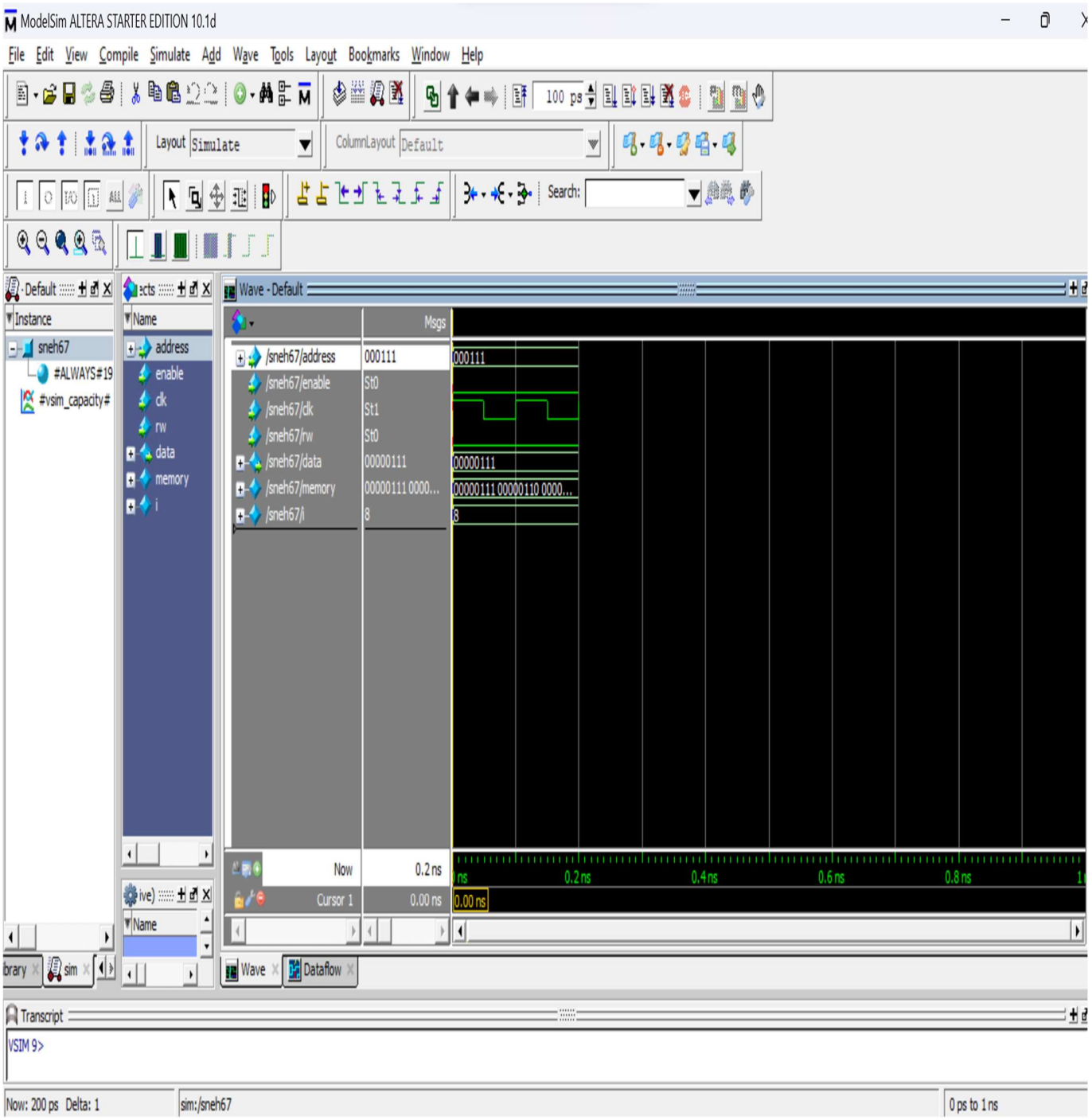


2)Cyclone II (TTL View)

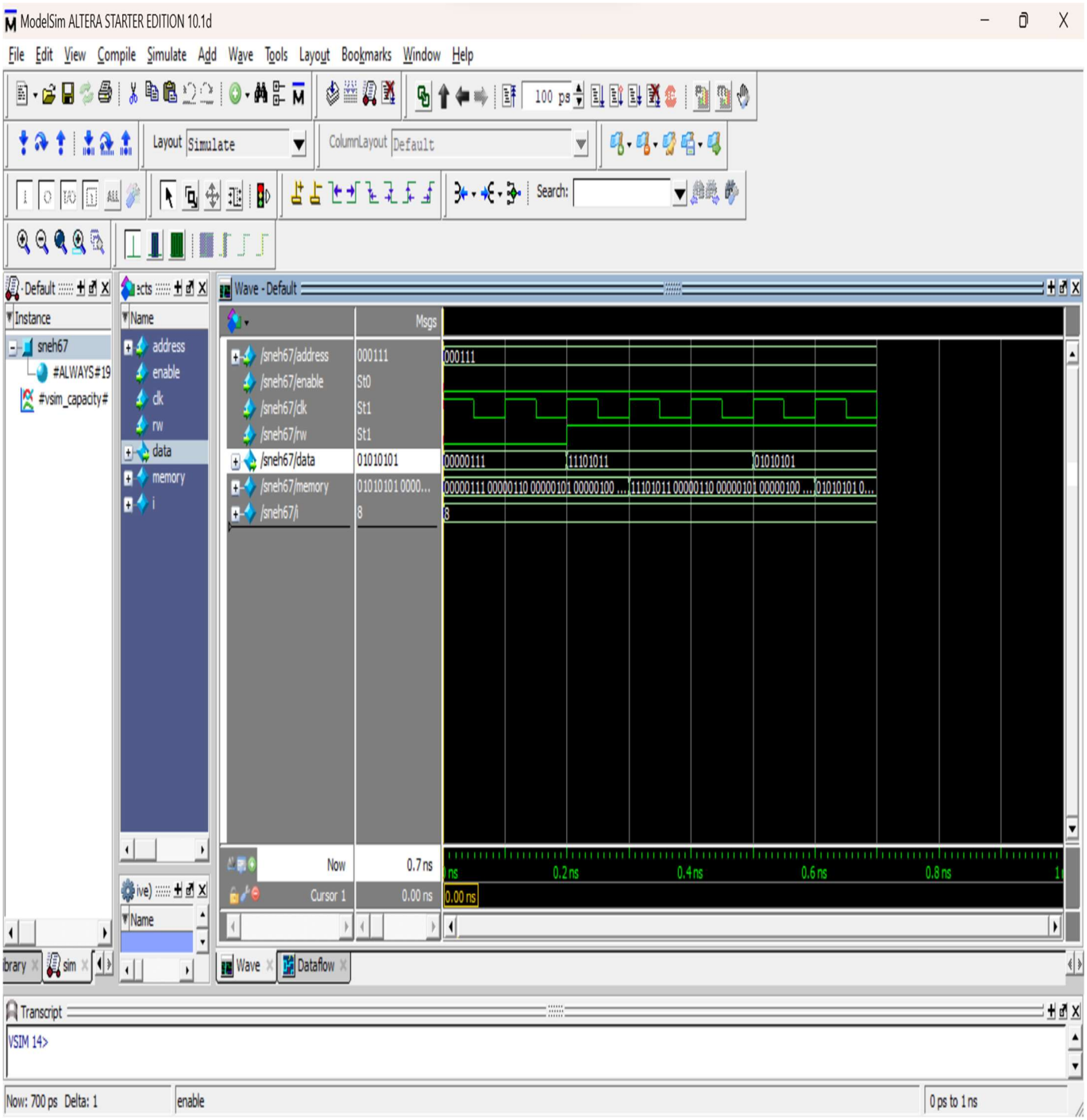


Simulation Results :-

Read



Write


ModelSim ALTERA STARTER EDITION 10.1d
File Edit View Compile Simulate Add Wave Tools Layout Bookmarks Window Help
Wave - Default
/sneh67/address
/sneh67/enable
/sneh67/clk
/sneh67/rw
/sneh67/data
/sneh67/memory
/sneh67/i
Now
Cursor 1
Transcript
VSIM 14>
Now: 700 ps Delta: 1
enable
0 ps to 1 ns

Conclusion :- In this experiment we learnt to design a 8 x 8 RAM and the concepts of RAM in depth .

We also learnt that what is the RTL and TTL of a RAM and also verified it using the Simulation .

We also found what problem occurs if we use inout declaration for data (it shows work file empty during simulation) ,

So we use output declaration and it still works same as a RAM performing both Read and Write Operation.

We also implemented RAM on a FPGA Kit . Also , we learned the different types of RAM used in Day – to – Day Scenarios .