22bec121

Experiment – 4 Date:-8/2/2024

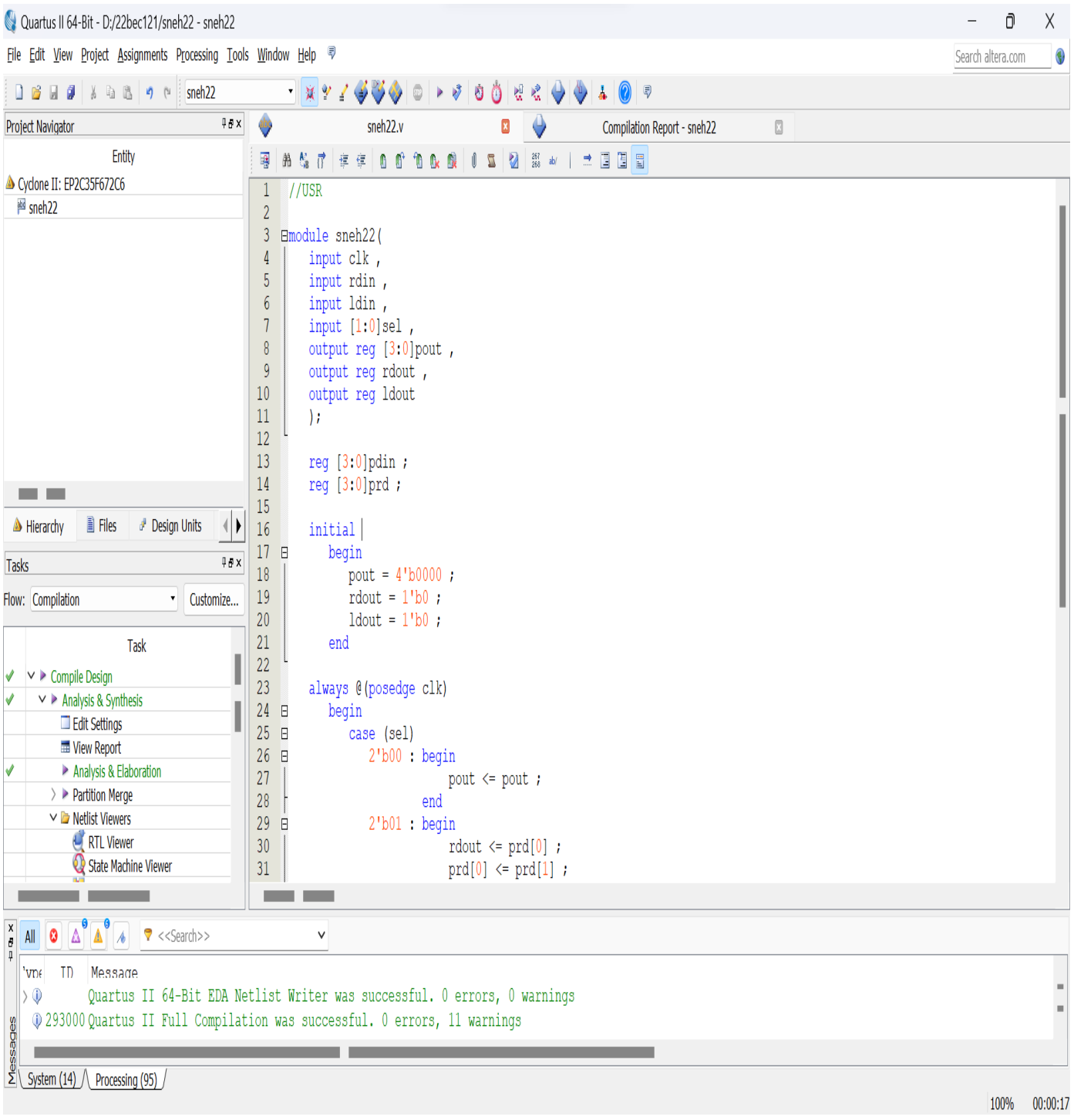
Lab Work

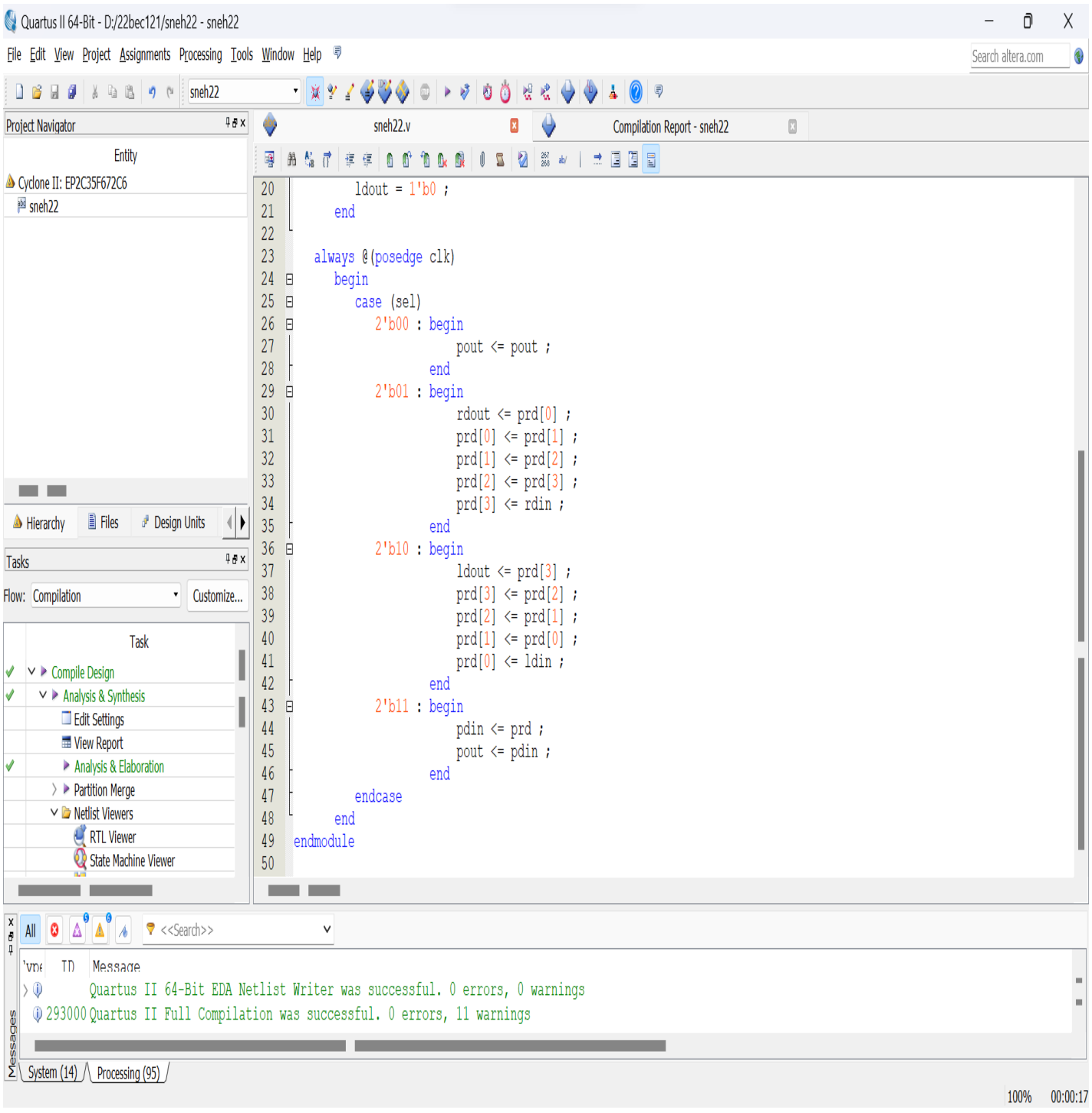
Q1 . Prepare the Verilog code for universal shift register(USR).

Code (USR)

```
//USR

module sneh22(
        input clk ,
        input rdin ,
        input ldin ,
        input [1:0]sel ,
        output reg [3:0]pout ,
        output reg rdout ,
        output reg ldout
        );

        reg [3:0]pdin ;
        reg [3:0]prd ;

        initial
                begin
                        pout = 4'b0000 ;
                        rdout = 1'b0 ;
                        ldout = 1'b0 ;
                end

        always @(posedge clk)
                begin
                        case (sel)
```

```
                2'b00 : begin
                                pout <= pout ;
                        end
                2'b01 : begin
                                rdout <= prd[0] ;
                                prd[0] <= prd[1] ;
                                prd[1] <= prd[2] ;
                                prd[2] <= prd[3] ;
                                prd[3] <= rdin ;
                        end
                2'b10 : begin
                                ldout <= prd[3] ;
                                prd[3] <= prd[2] ;
                                prd[2] <= prd[1] ;
                                prd[1] <= prd[0] ;
                                prd[0] <= ldin ;
                        end
                2'b11 : begin
                                pdin <= prd ;
                                pout <= pdin ;
                        end
        endcase
    end
endmodule
```


Quartus II 64-Bit - D:/22bec121/sneh22 - sneh22
File Edit View Project Assignments Processing Tools Window Help
Search altera.com
sneh22
Project Navigator
Entity
Cyclone II: EP2C35F672C6
sneh22
Hierarchy
Files
Design Units
Tasks
Flow: Compilation
Customize...
Task
Compile Design
Analysis & Synthesis
Edit Settings
View Report
Analysis & Elaboration
Partition Merge
Netlist Viewers
RTL Viewer
State Machine Viewer
sneh22.v
Compilation Report - sneh22
1 //USR
2
3 module sneh22(
4 input clk ,
5 input rdin ,
6 input ldin ,
7 input [1:0]sel ,
8 output reg [3:0]pout ,
9 output reg rdout ,
10 output reg ldout
11);
12
13 reg [3:0]pdin ;
14 reg [3:0]prd ;
15
16 initial
17 begin
18 pout = 4'b0000 ;
19 rdout = 1'b0 ;
20 ldout = 1'b0 ;
21 end
22
23 always @(posedge clk)
24 begin
25 case (sel)
26 2'b00 : begin
27 pout <= pout ;
28 end
29 2'b01 : begin
30 rdout <= prd[0] ;
31 prd[0] <= prd[1] ;
All
<<Search>>
ID Message
Quartus II 64-Bit EDA Netlist Writer was successful. 0 errors, 0 warnings
293000 Quartus II Full Compilation was successful. 0 errors, 11 warnings
Messages
System (14)
Processing (95)
100%
00:00:17



Output 1)Cyclone II (RTL View)

RTL Viewer - D:/22bec121/sneh22 - sneh22

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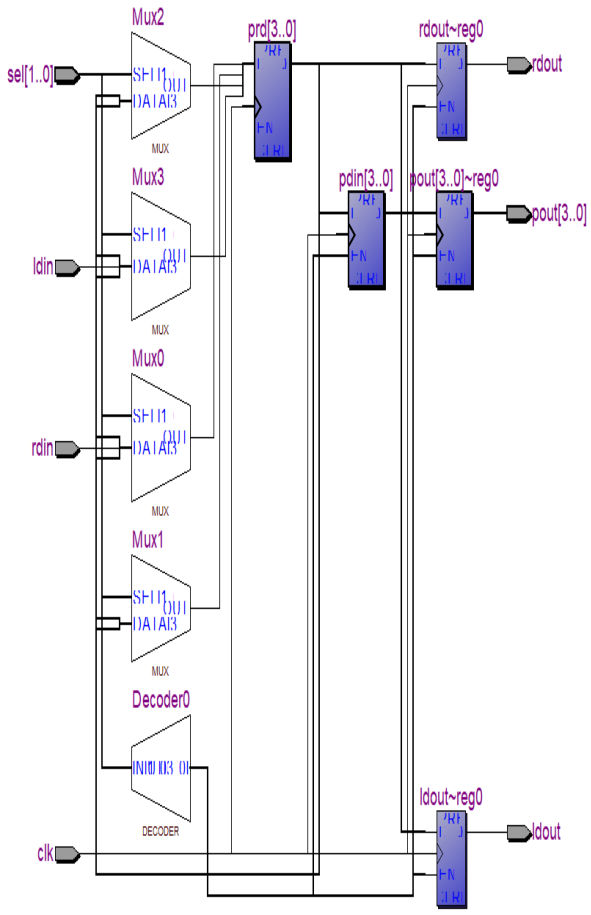
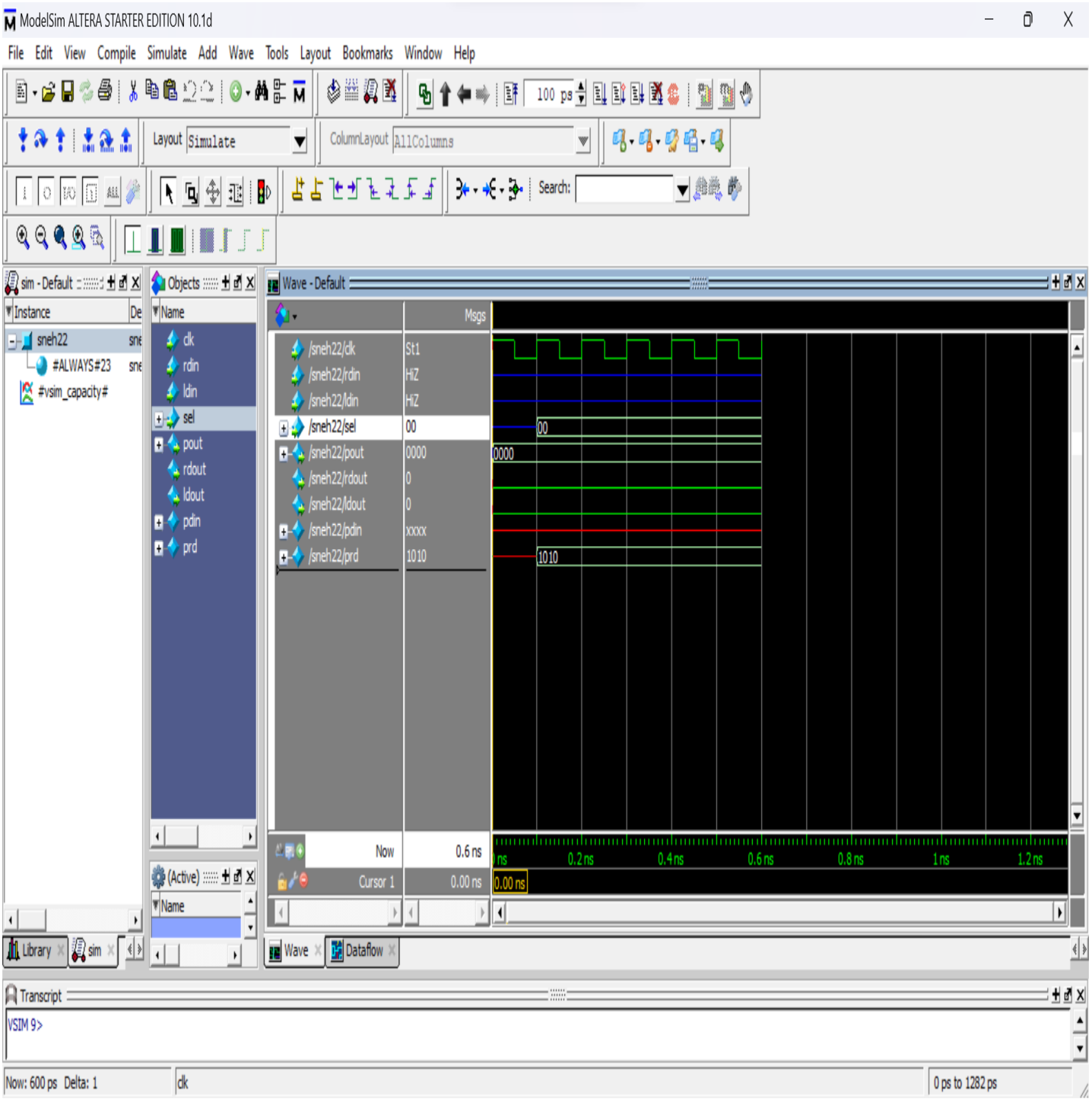
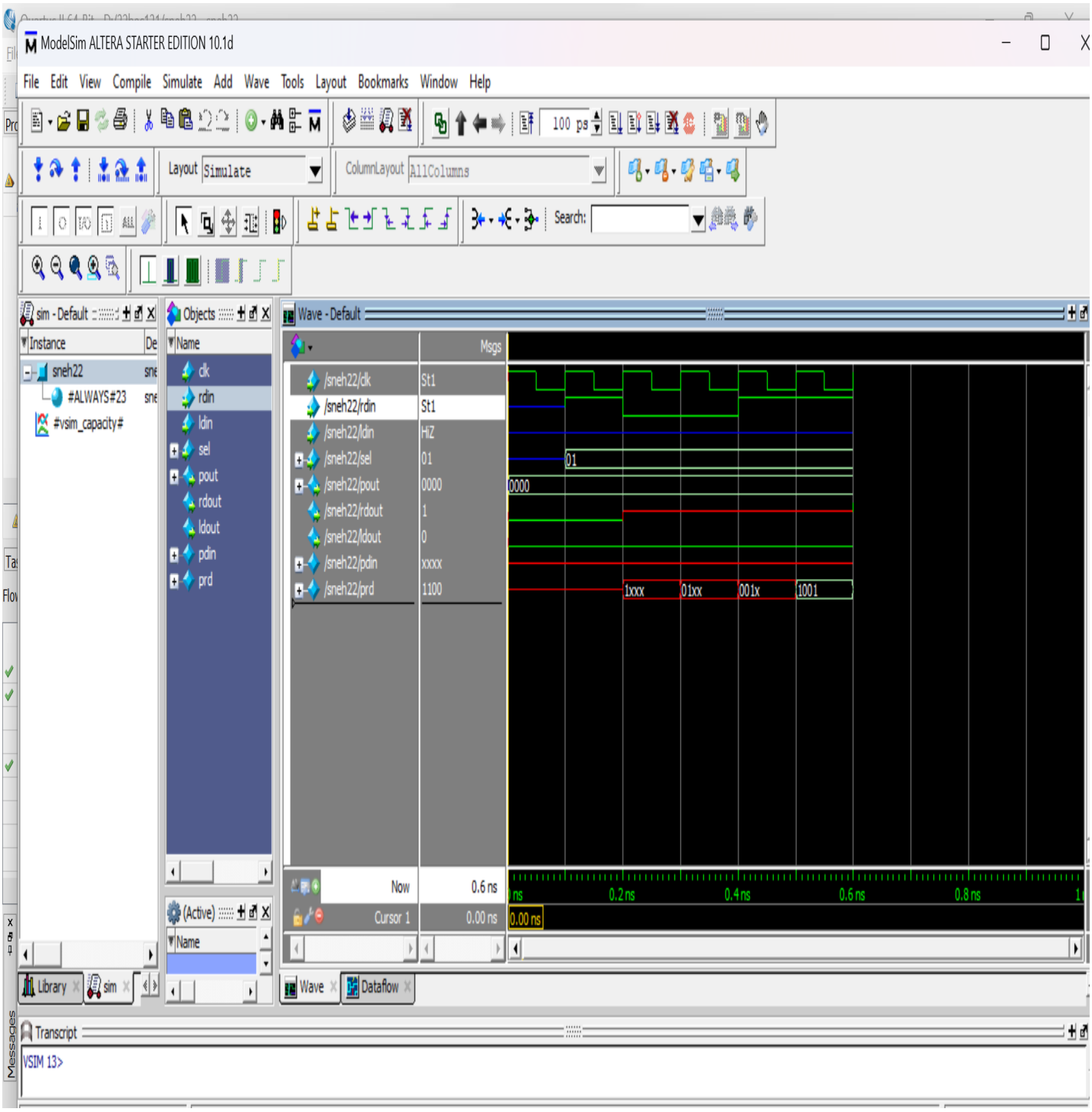


100% 00:00:02

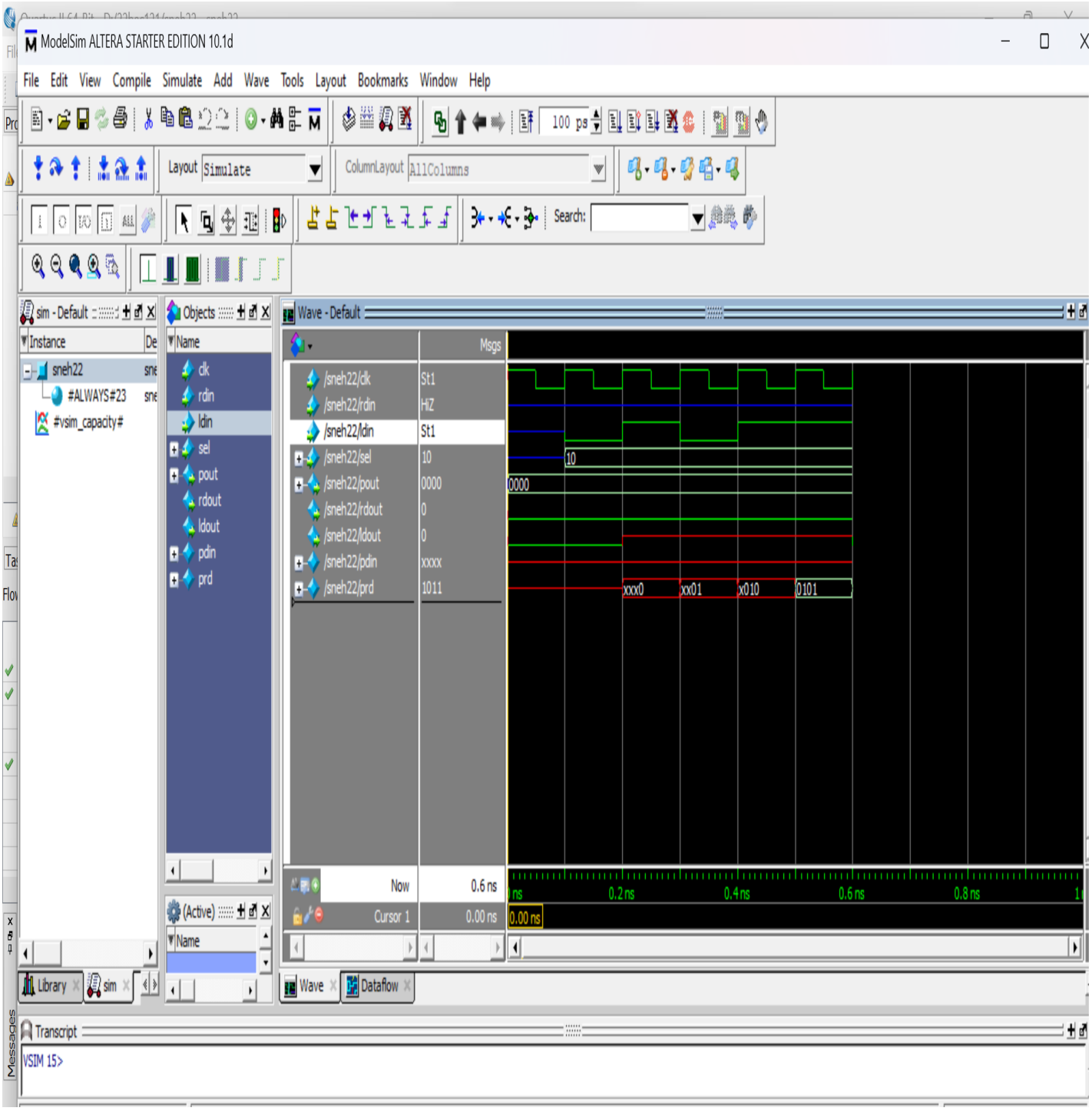
Simulation 1) No operation



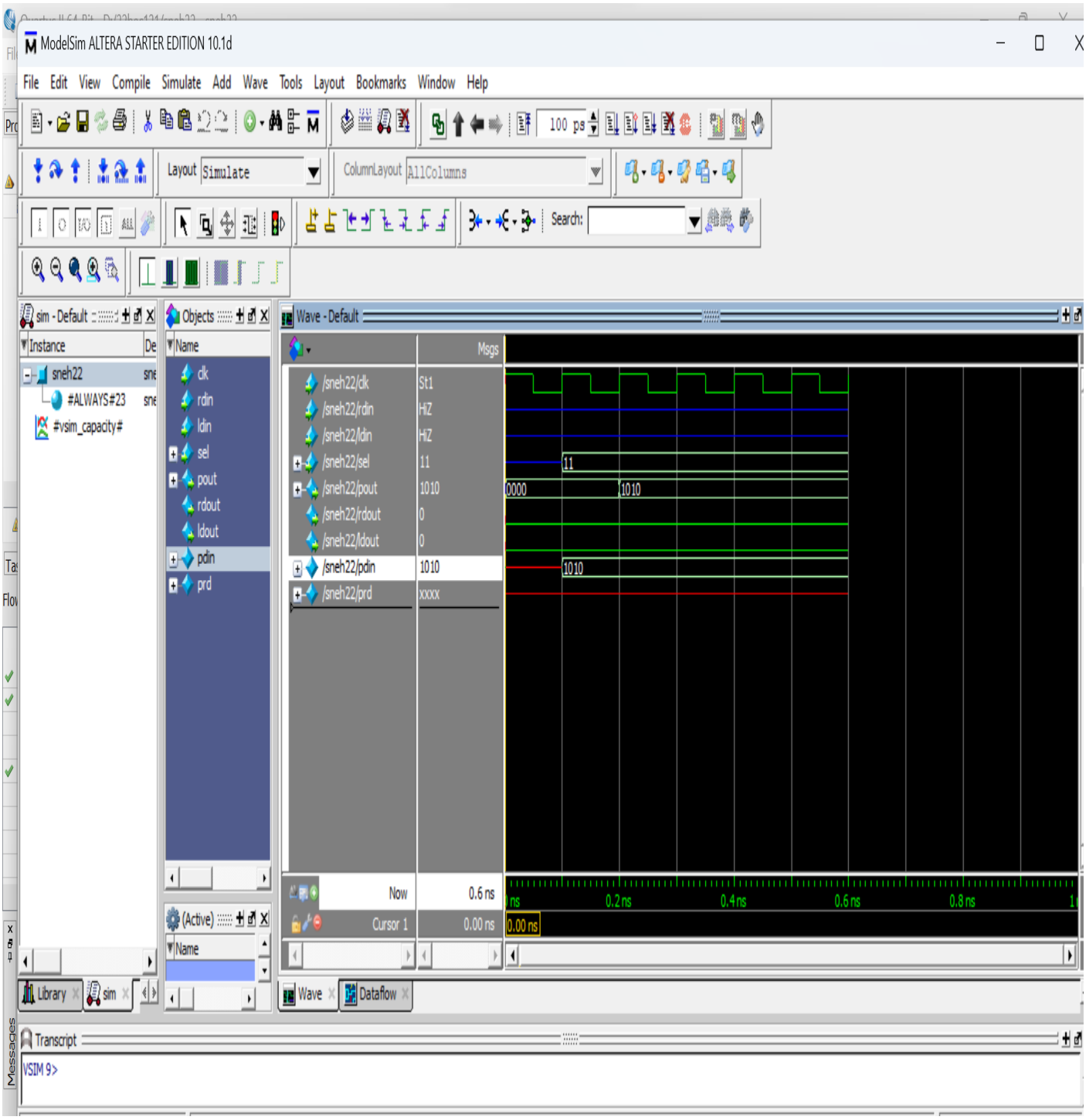
Simulation 2) Right Shift



Simulation 3) Left Shift



Simulation 4) Parallel Load



Conclusion :-In this experiment we learnt that how Shift Registers are synthesized and what are their modes of operation (SISO , SIPO , PISO and PIPO) . We also learnt to implement the Universal Shift Register in Verilog and its Simulation

Then we implemented the USR on the FPGA Kit and successfully completed all the modes of Universal Shift Register .