22bec121

Experiment – 3 Date:-1/2/2024

Lab Work

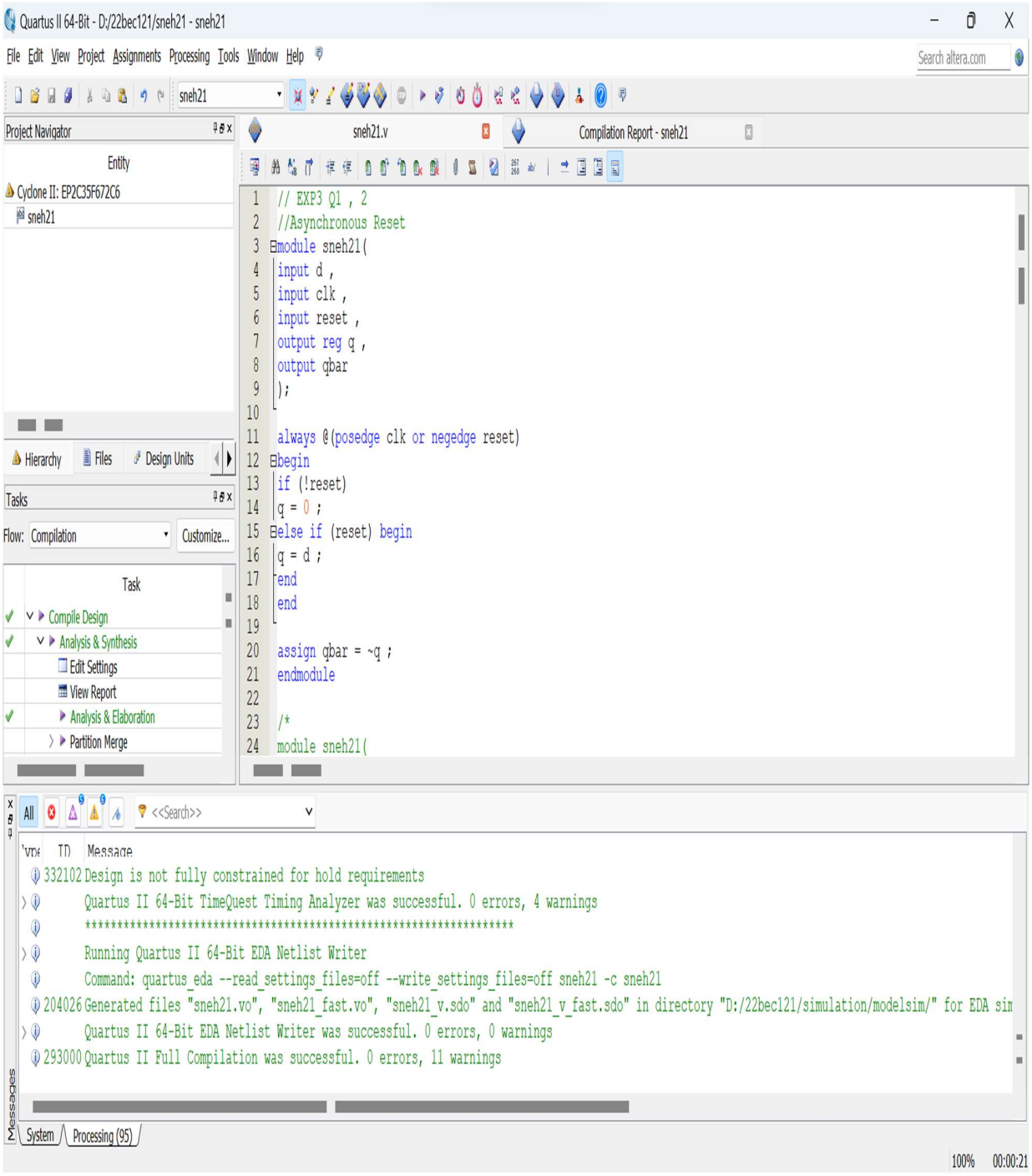
Q1 . Prepare the Verilog code for all the flip flops.

Code (D Flip Flop)

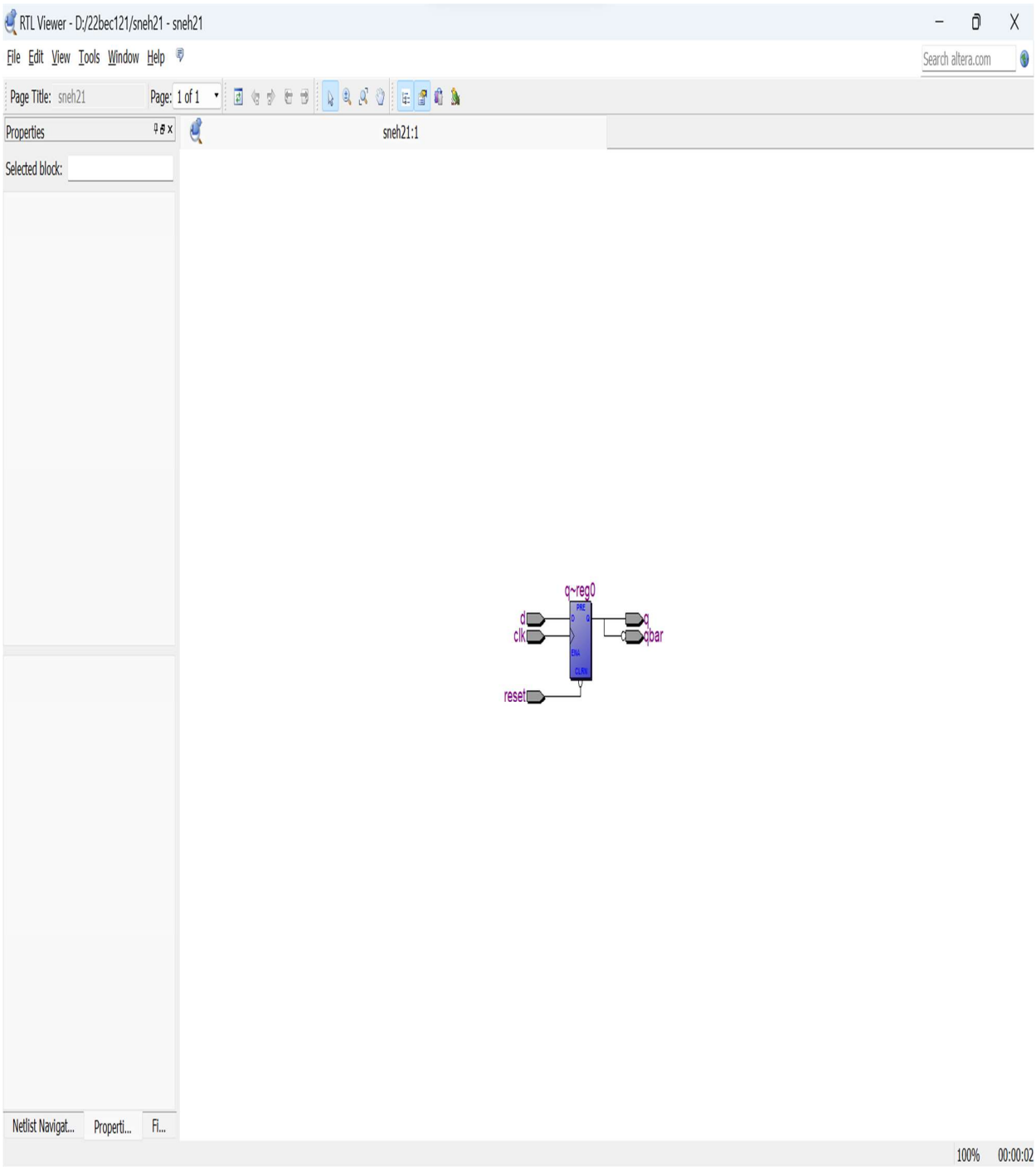
```
//Asynchronous Reset
module sneh21(
input d ,
input clk ,
input reset ,
output reg q ,
output qbar
);

always @(posedge clk or negedge reset)
begin
if (!reset)
q = 0 ;
else if (reset) begin
q = d ;
end
end

assign qbar = ~q ;
endmodule
```



Output 1)Cyclone II (RTL View), 2) Cyclone II (TTL View)


RTL Viewer - D:/22bec121/sneh21 - sneh21
File Edit View Tools Window Help
Search altera.com
Page Title: sneh21
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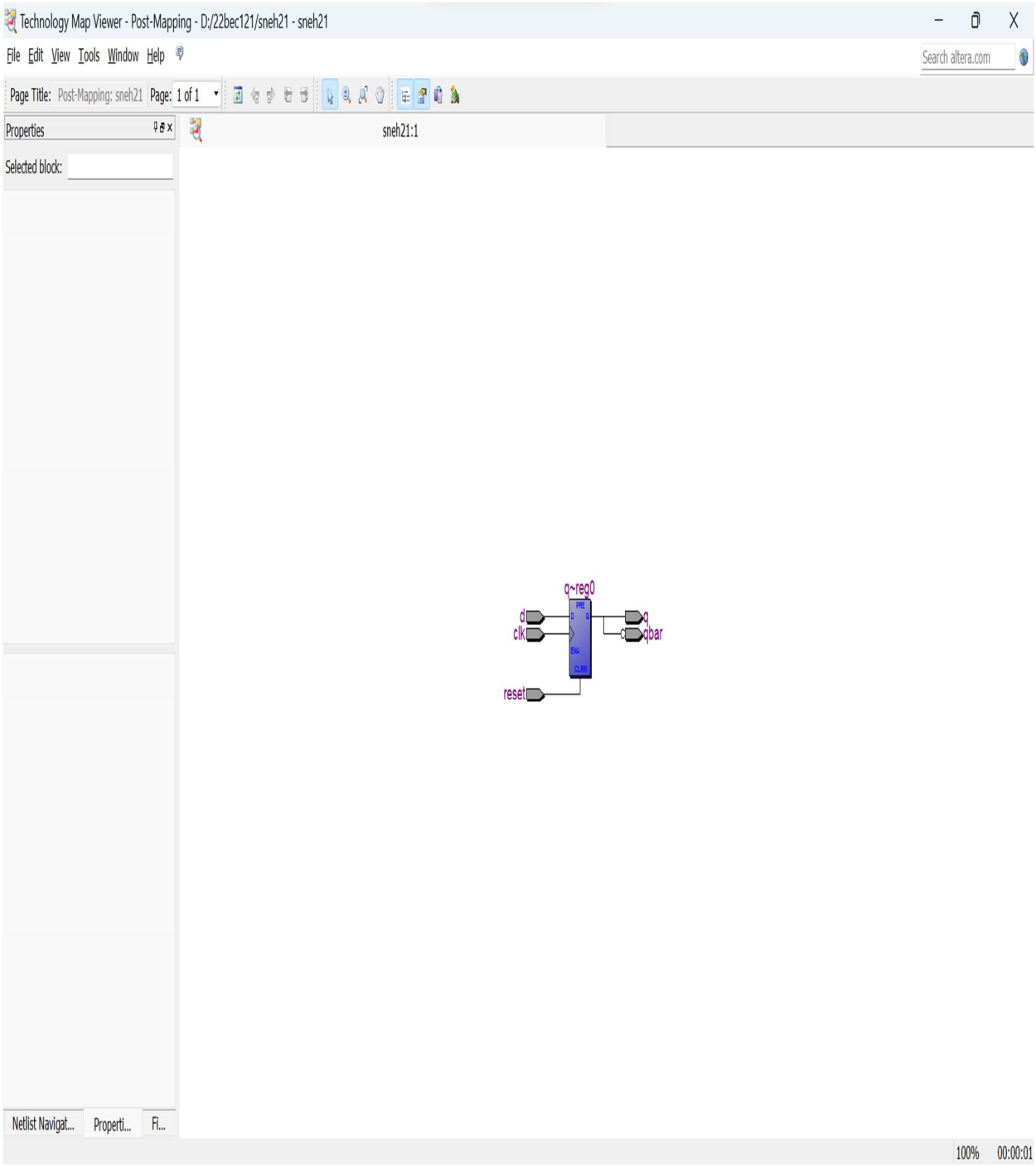
Properties
Selected block:
sneh21:1
q~reg0
PRE
D
Q
ENA
CLRN
d
clk
reset
q
qbar
Netlist Navigat...
Properti...
Fi...
100%
00:00:02



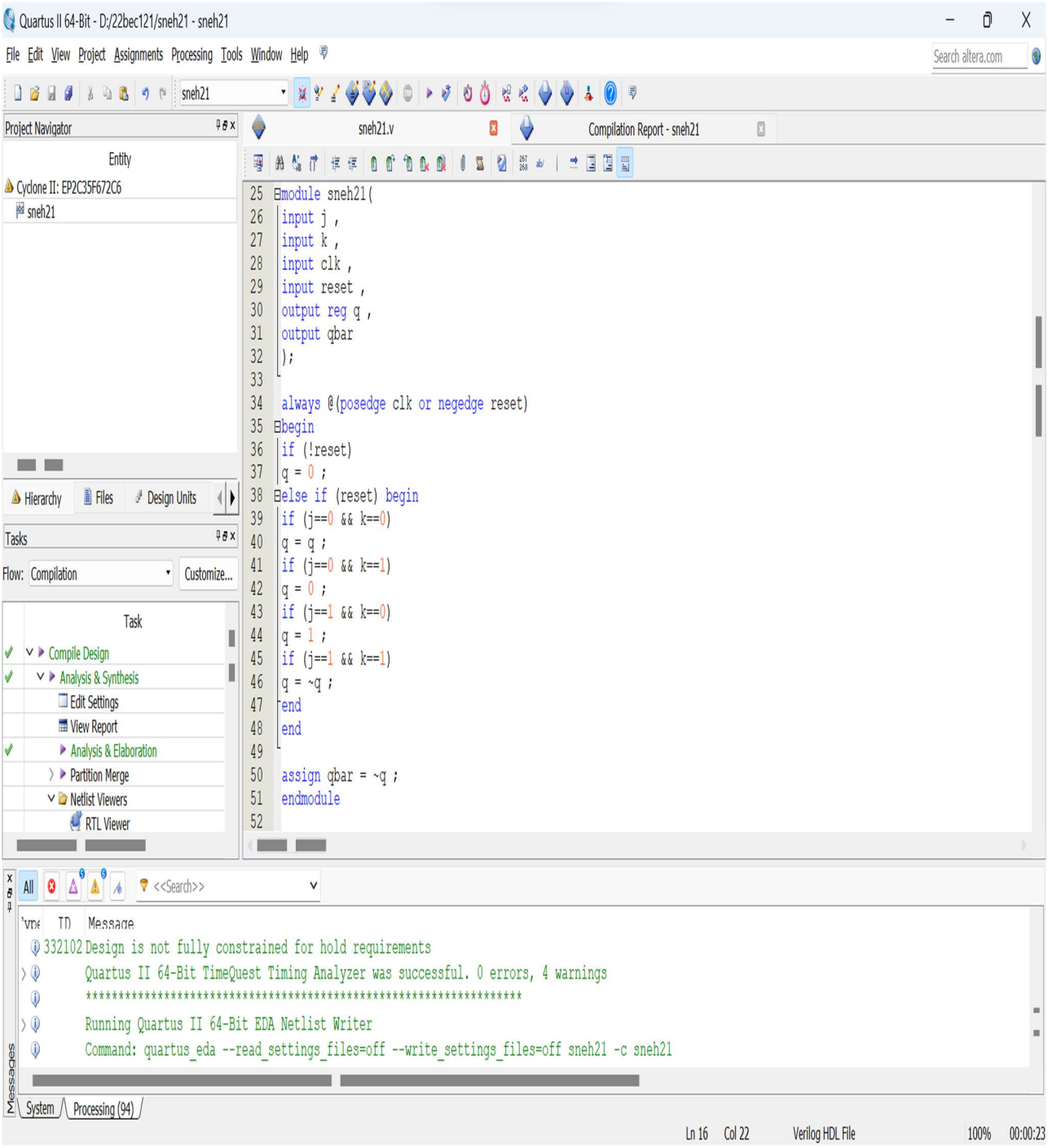
Code (JK Flip Flop)

module sneh21(

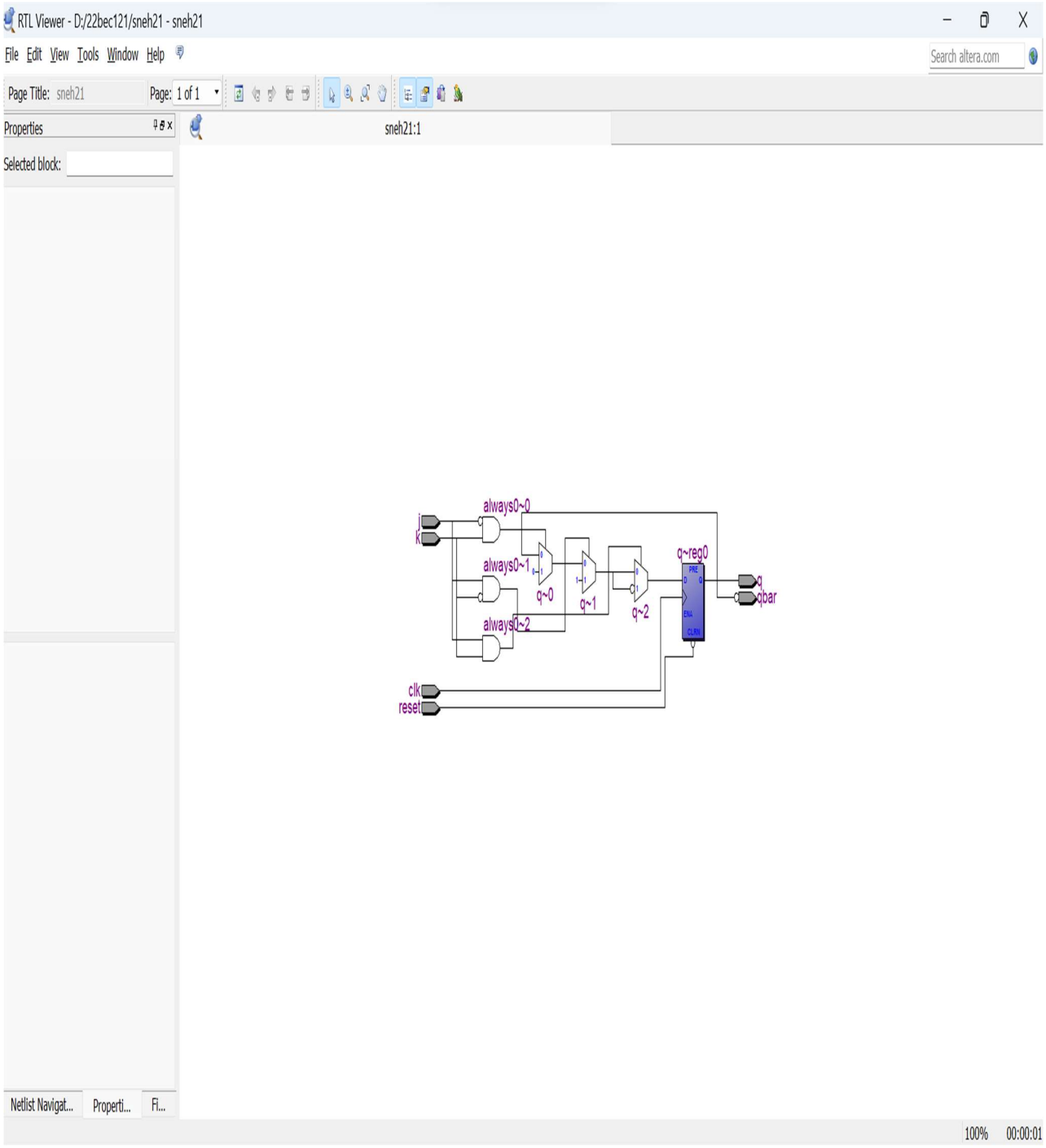
```
input j ,
input k ,
input clk ,
input reset ,
output reg q ,
output qbar
);

always @(posedge clk or negedge reset)
begin
if (!reset)
q = 0 ;
else if (reset) begin
if (j==0 && k==0)
q = q ;
if (j==0 && k==1)
q = 0 ;
if (j==1 && k==0)
q = 1 ;
if (j==1 && k==1)
q = ~q ;
end
end

assign qbar = ~q ;
endmodule
```



Output 1)Cyclone II (RTL View), 2) Cyclone II (TTL View)


RTL Viewer - D:/22bec121/sneh21 - sneh21
File Edit View Tools Window Help
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Page Title: sneh21
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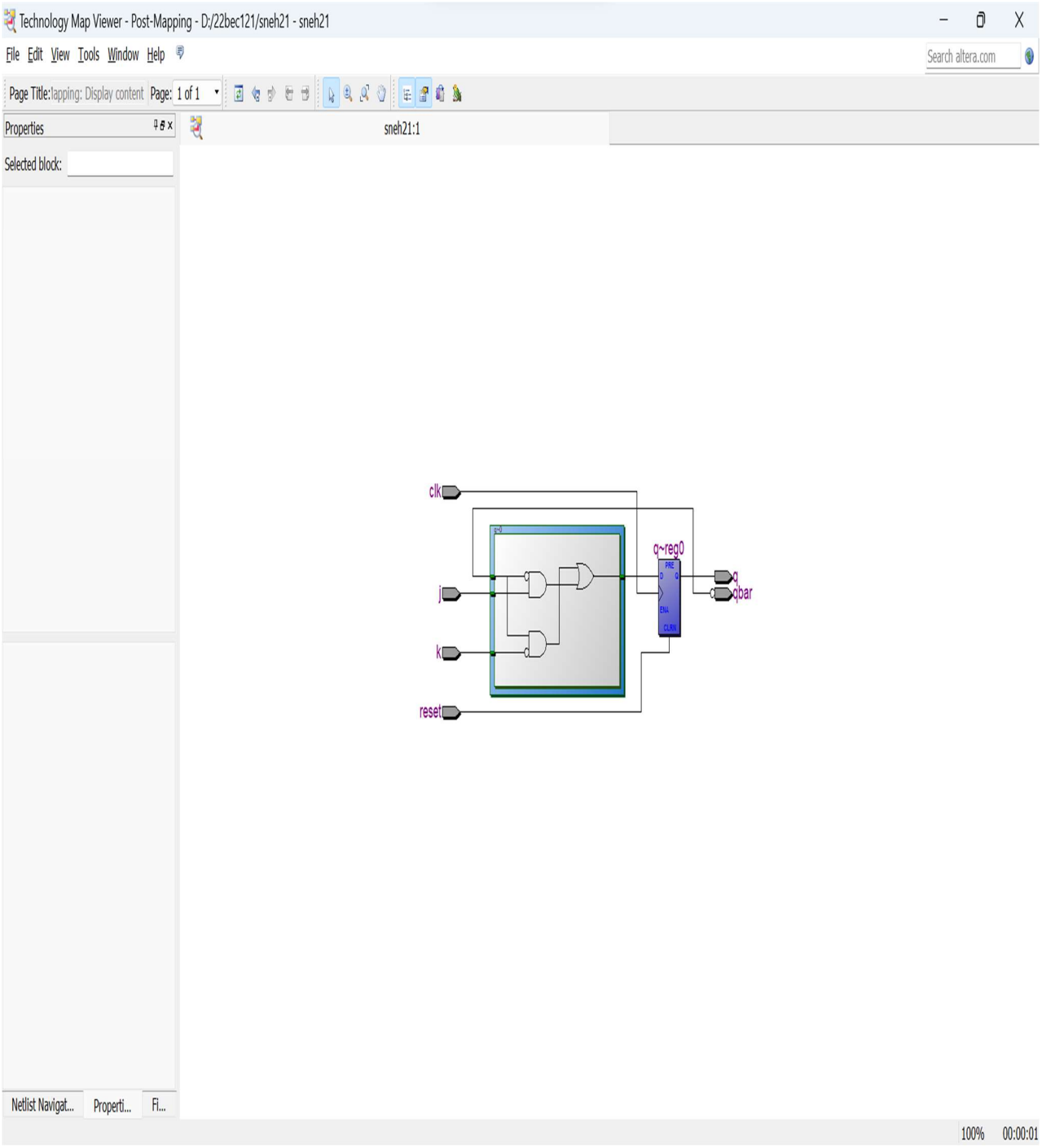
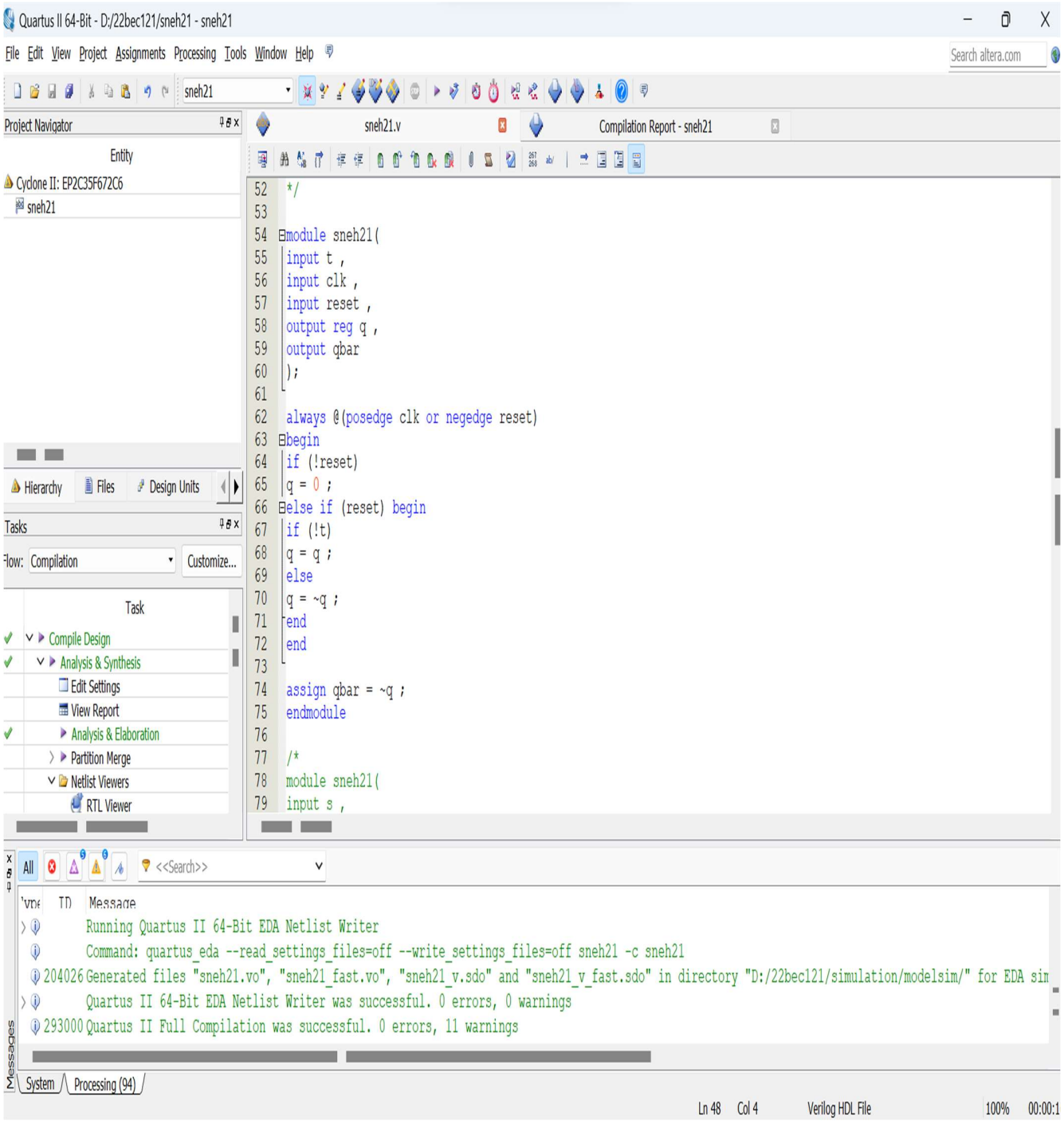
Properties
Selected block:
sneh21:1
always0~0
always0~1
always0~2
q~0
q~1
q~2
q~reg0
PRE
ENA
CLRN
q
qbar
clk
reset
Netlist Navigat...
Properti...
Fi...
100%
00:00:01

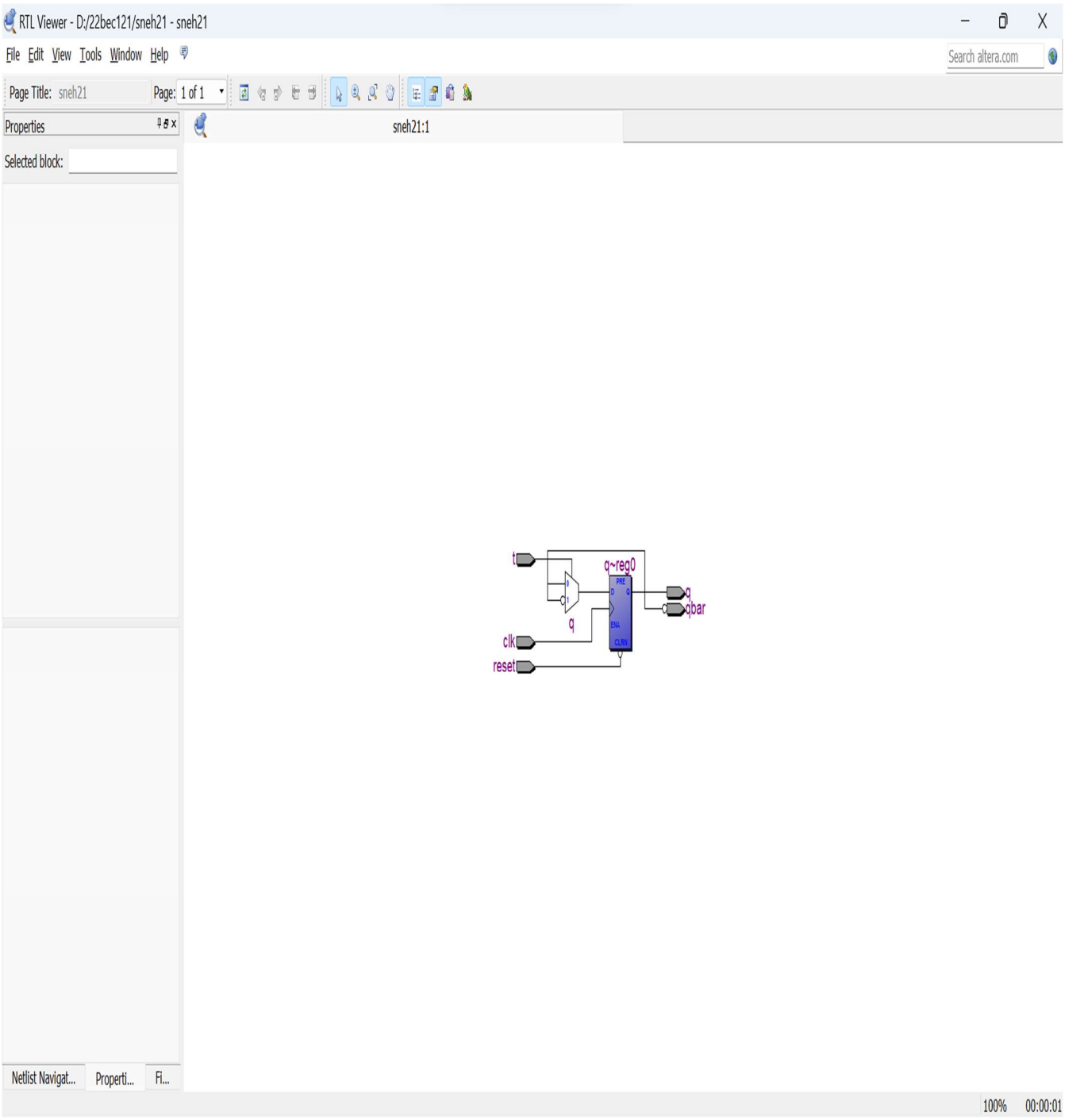


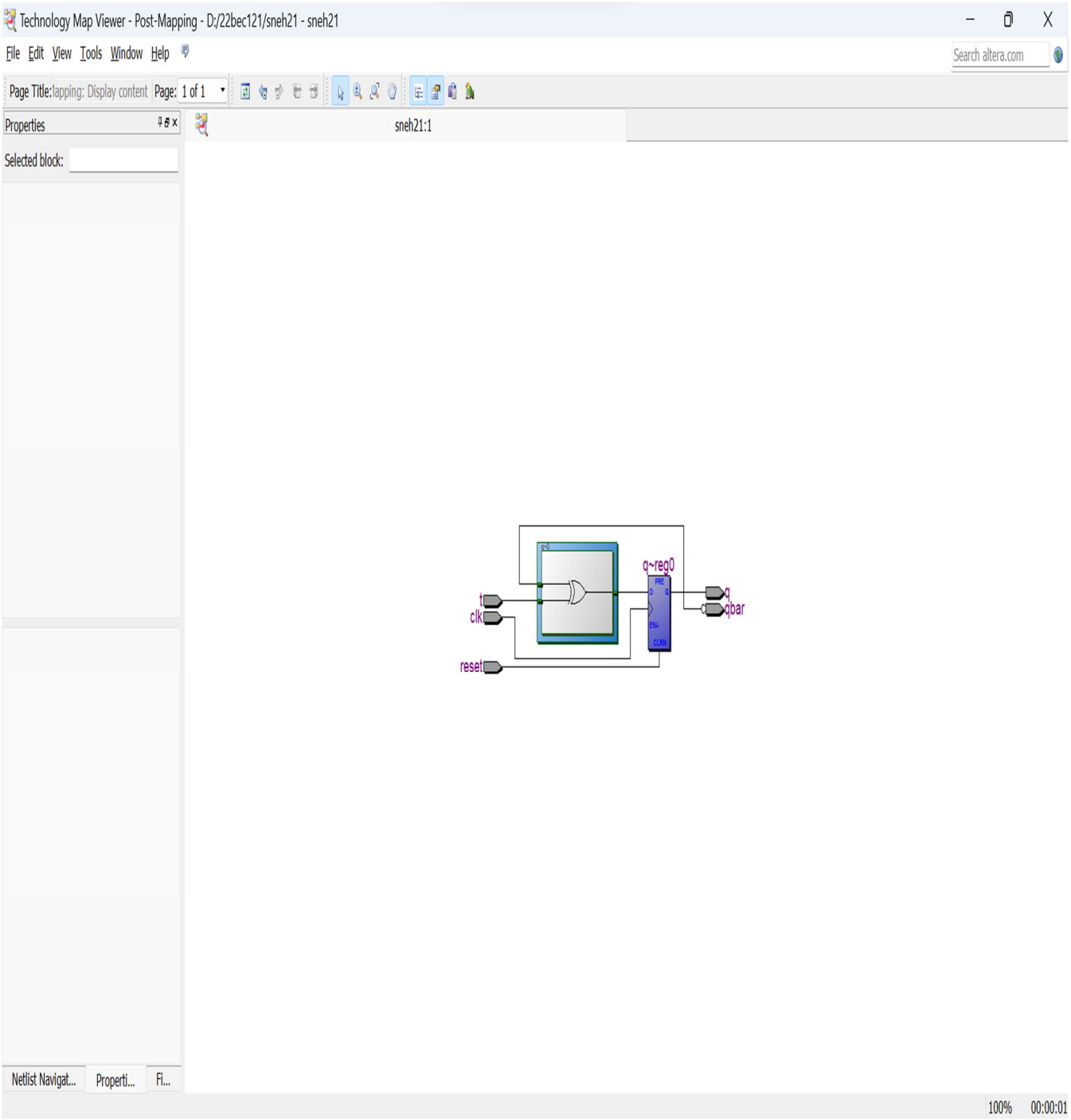
Code (T Flip Flop)

```
module sneh21(
input t ,
input clk ,
input reset ,
output reg q ,
output qbar
);

always @(posedge clk or negedge reset)
begin
if (!reset)
q = 0 ;
else if (reset) begin
if (!t)
q = q ;
else
q = ~q ;
end
end

assign qbar = ~q ;
endmodule
```



Output 1)Cyclone II (RTL View), 2) Cyclone II (TTL View)

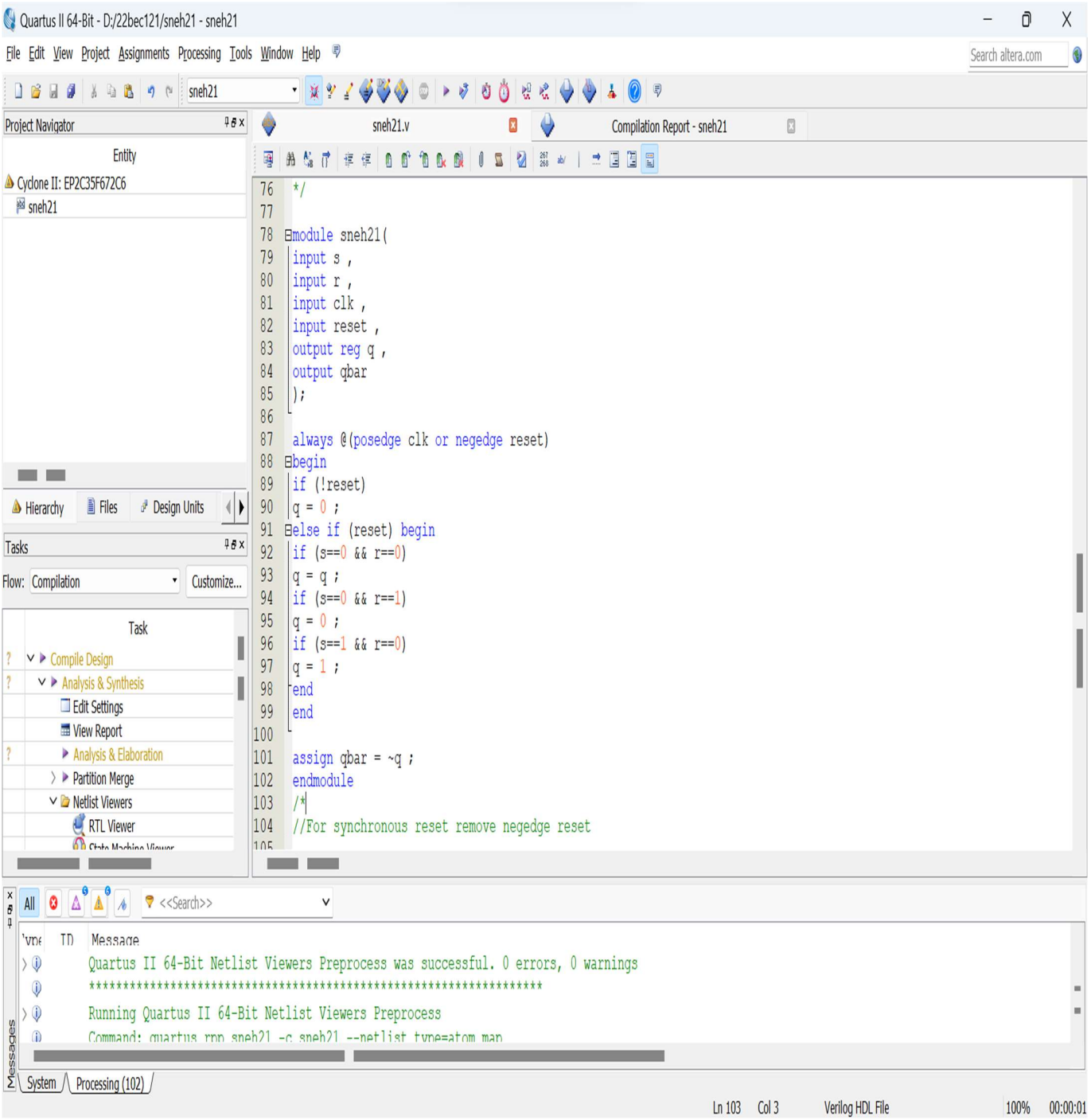

RTL Viewer - D:/22bec121/sneh21 - sneh21
File Edit View Tools Window Help
Search altera.com
Page Title: sneh21
Page: 1 of 1
Properties
Selected block:
sneh21:1
t
clk
reset
q
q~reg0
PRE
D
Q
ENA
CLRN
q
qbar
Netlist Navigat...
Properti...
Fi...
100%
00:00:01



Code (SR Flip Flop)

```
module sneh21(
input s ,
input r ,
```

```
input clk ,
input reset ,
output reg q ,
output qbar
);

always @(posedge clk or negedge reset)
begin
if (!reset)
q = 0 ;
else if (reset) begin
if (s==0 && r==0)
q = q ;
if (s==0 && r==1)
q = 0 ;
if (s==1 && r==0)
q = 1 ;
end
end

assign qbar = ~q ;
endmodule
```



Output 1)Cyclone II (RTL View), 2) Cyclone II (TTL View)

RTL Viewer - D:/22bec121/sneh21 - sneh21

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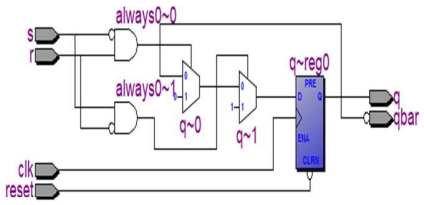
Properties

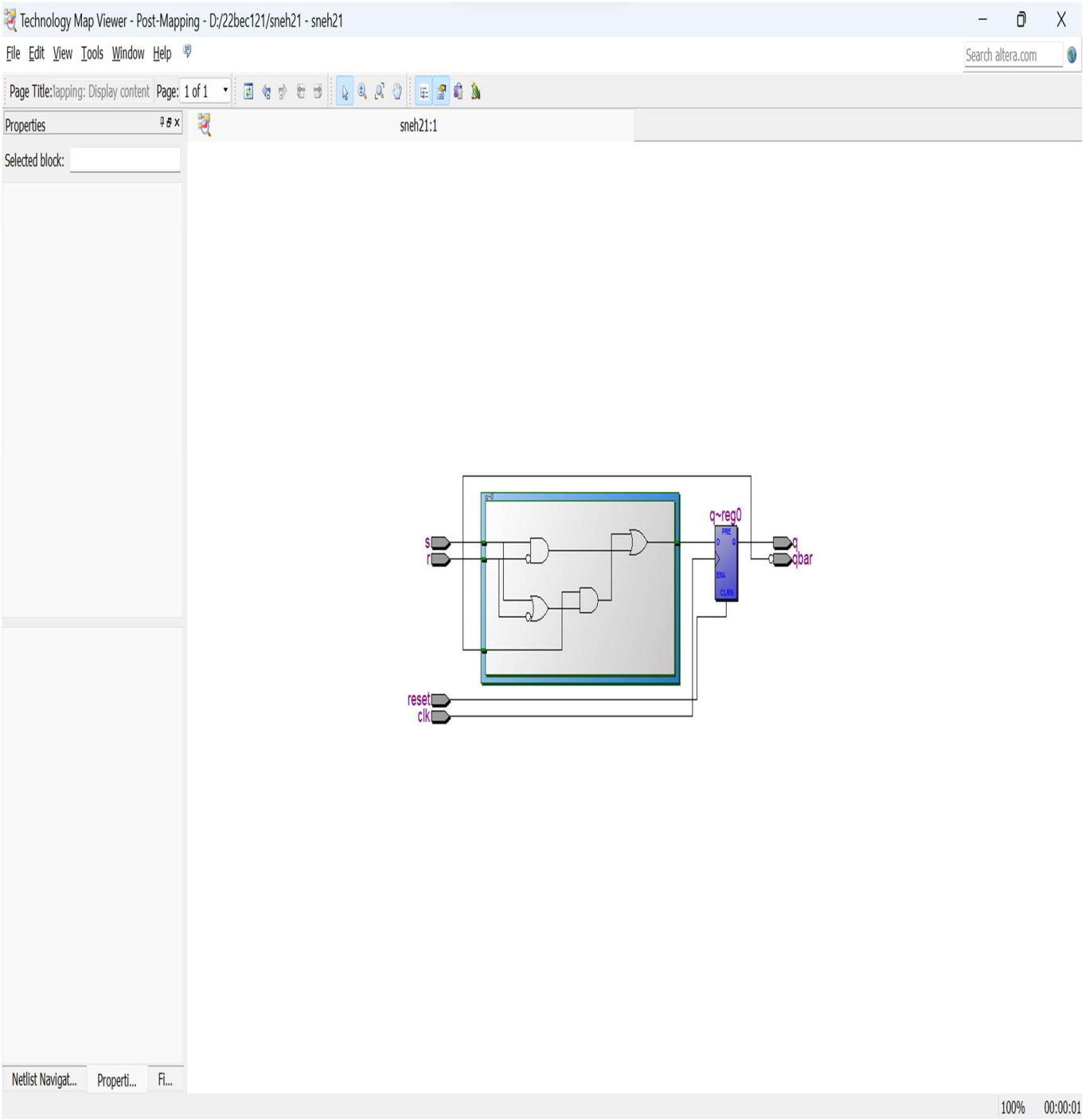
sneh21:1

Selected block:



Netlist Navigat... Properti... Fi...

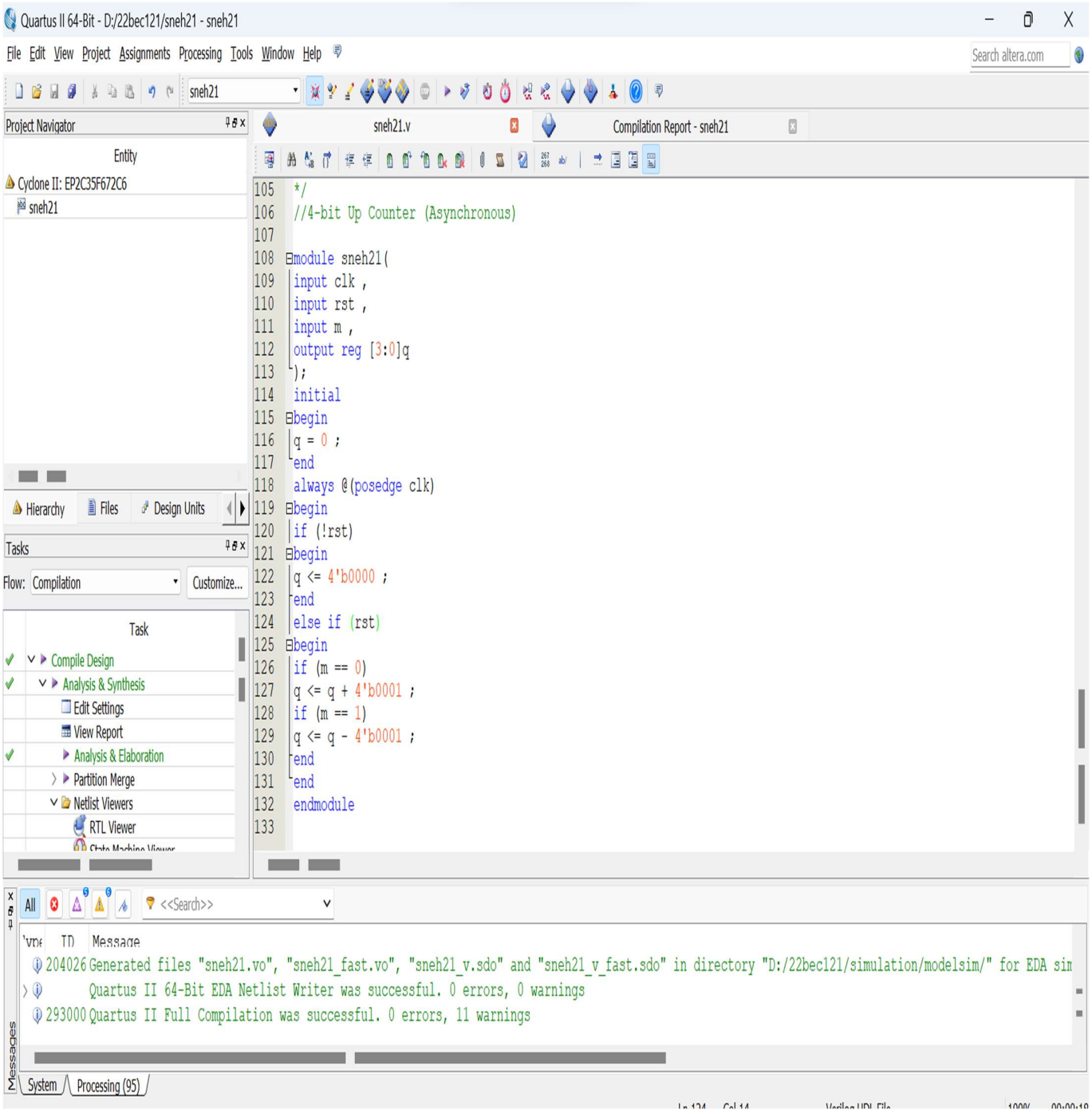
100% 00:00:01



Q2 . Prepare the code for 4 – bit counter (Up/Down). Observer the RTL and TTL of the same.

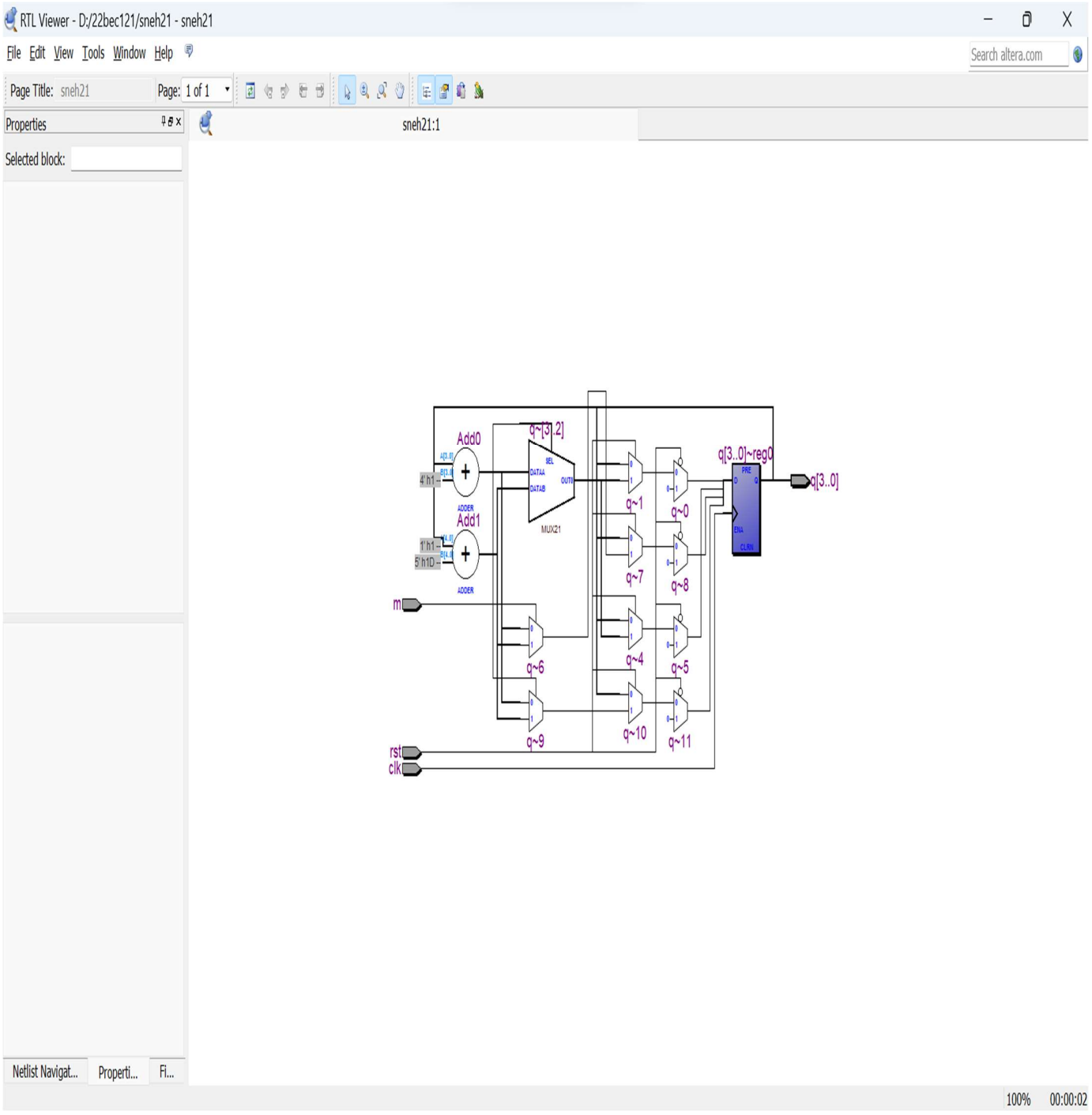
Code

```
module sneh21(
input clk ,
input rst ,
input m ,
output reg [3:0]q
);
initial
begin
q = 0 ;
end
always @(posedge clk)
begin
if (!rst)
begin
q <= 4'b0000 ;
end
else if (rst)
begin
if (m == 0)
q <= q + 4'b0001 ;
if (m == 1)
q <= q - 4'b0001 ;
end
end
endmodule
```



Output

1)Cyclone II (RTL View), 2) Cyclone II (TTL View)


RTL Viewer - D:/22bec121/sneh21 - sneh21
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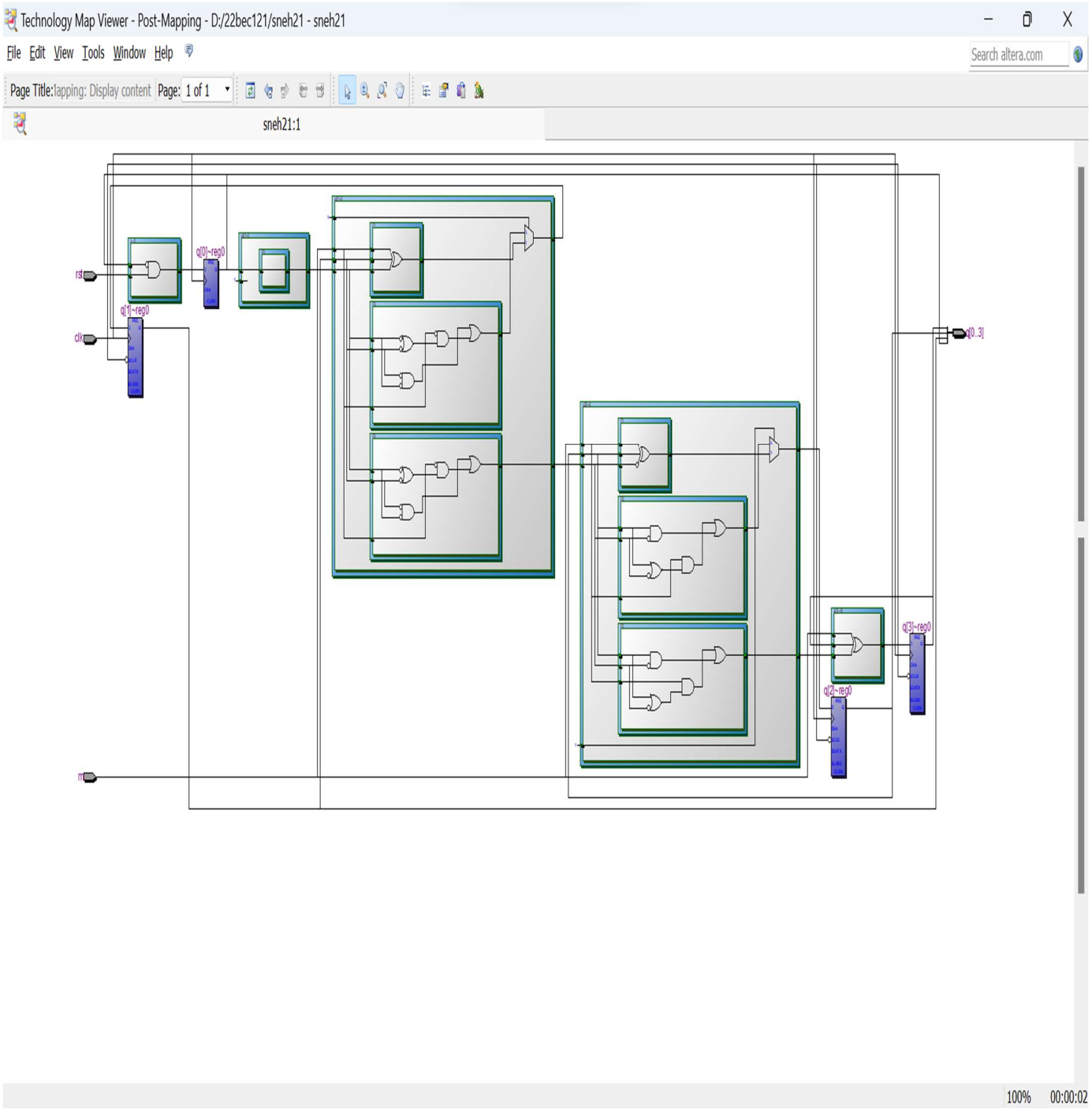
Search altera.com
Page Title: sneh21
Page: 1 of 1
Properties
Selected block:
sneh21:1
Add0
Add1
ADDER
4'h1
1'h1
5'h1D
q~[3..2]
SEL
DATAA
DATAB
OUTR
MUX21
q[3..0]~reg0
PRE
ENA
CLRN
q[3..0]
m
rst
clk
q~0
q~1
q~4
q~5
q~6
q~7
q~8
q~9
q~10
q~11
Netlist Navigat...
Properti...
Fi...
100%
00:00:02



Conclusion :-In this experiment we learnt that how Flip Flops are synthesized and what is their hardware formed while synthesis. A common observation is that every flip flop is synthesized using the D flip flop in RTL as well as TTL View.

Then we implemented the mode controlled synchronous as well as asynchronous counter in Verilog and further implemented it on FPGA .