

**22bec121**

**Experiment – 3**

**Date:-1/2/2024**

**Lab Work**

**Q1 . Prepare the Verilog code for all the flip flops.**

**Code (D Flip Flop)**

**//Asynchronous Reset**

**module sneh21(**

**input d ,**

**input clk ,**

**input reset ,**

**output reg q ,**

**output qbar**

**);**

**always @(posedge clk or negedge reset)**

**begin**

**if (!reset)**

**q = 0 ;**

**else if (reset) begin**

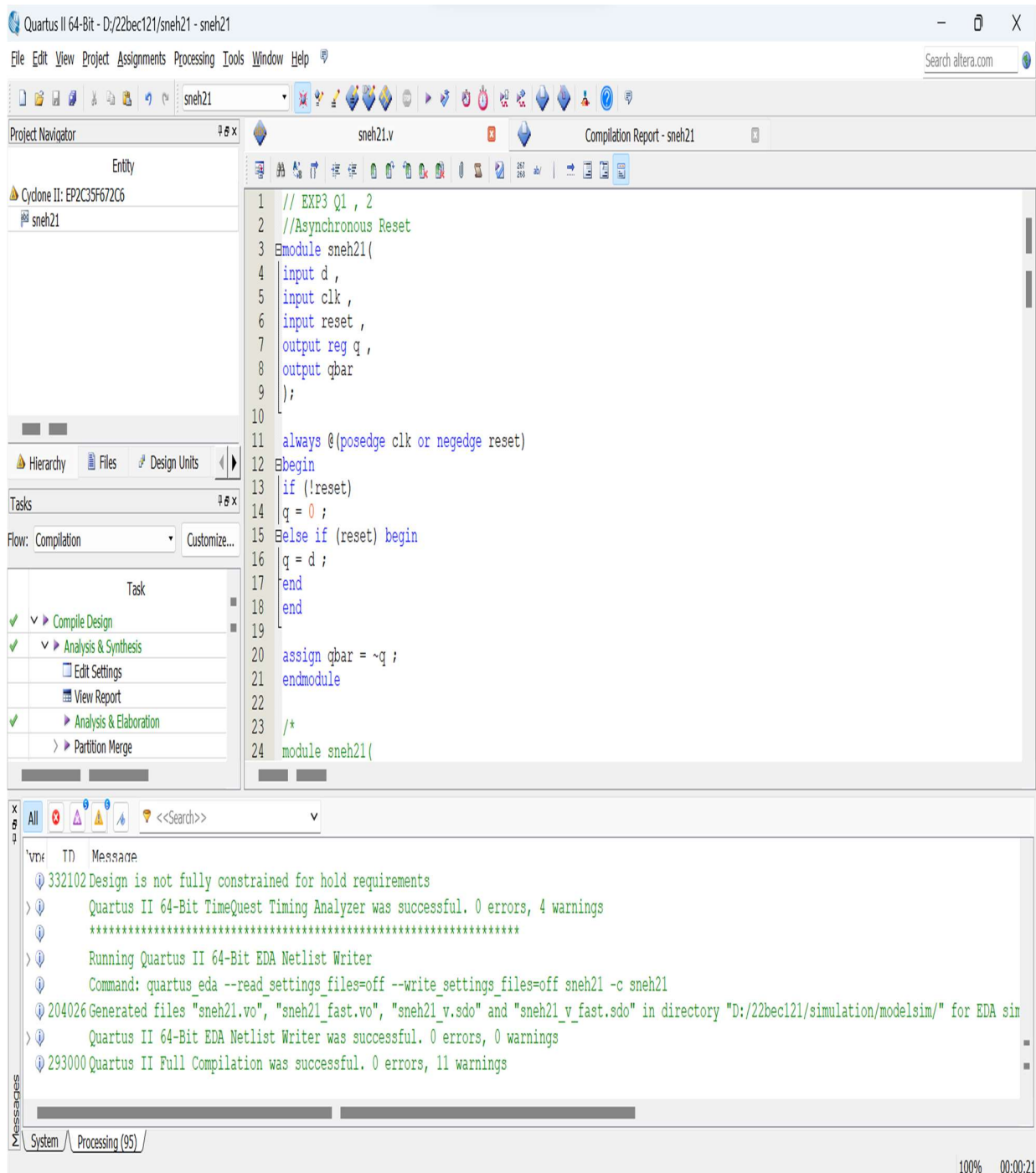
**q = d ;**

**end**

**end**

**assign qbar = ~q ;**

**endmodule**



**Output 1)Cyclone II (RTL View), 2) Cyclone II (TTL View)**

RTL Viewer - D:/22bec121/sneh21 - sneh21

File Edit View Tools Window Help

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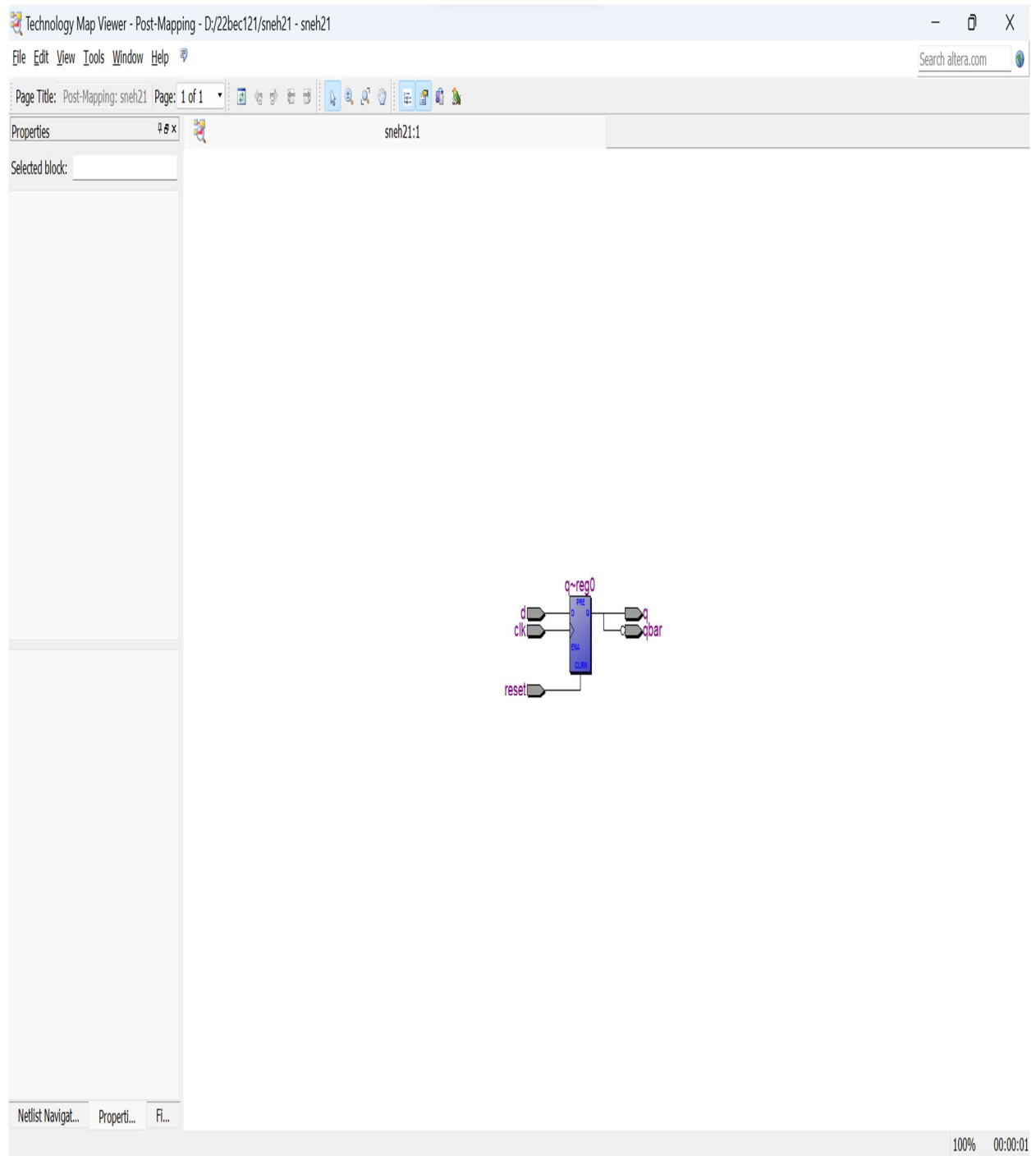
Properties 48x sneh21:1

Selected block:

The diagram shows a D flip-flop component. It has three inputs: 'a' (data), 'clk' (clock), and 'reset'. It has two outputs: 'q' and 'qbar'. The flip-flop is labeled 'a~reg0' at the top. The 'reset' input is connected to the 'CLR' pin of the flip-flop. The 'a' input is connected to the 'D' pin. The 'clk' input is connected to the 'CLK' pin. The output 'q' is connected to the 'Q' pin, and 'qbar' is connected to the 'Qbar' pin.

Netlist Navigat... Properti... Fi...

100% 00:00:02



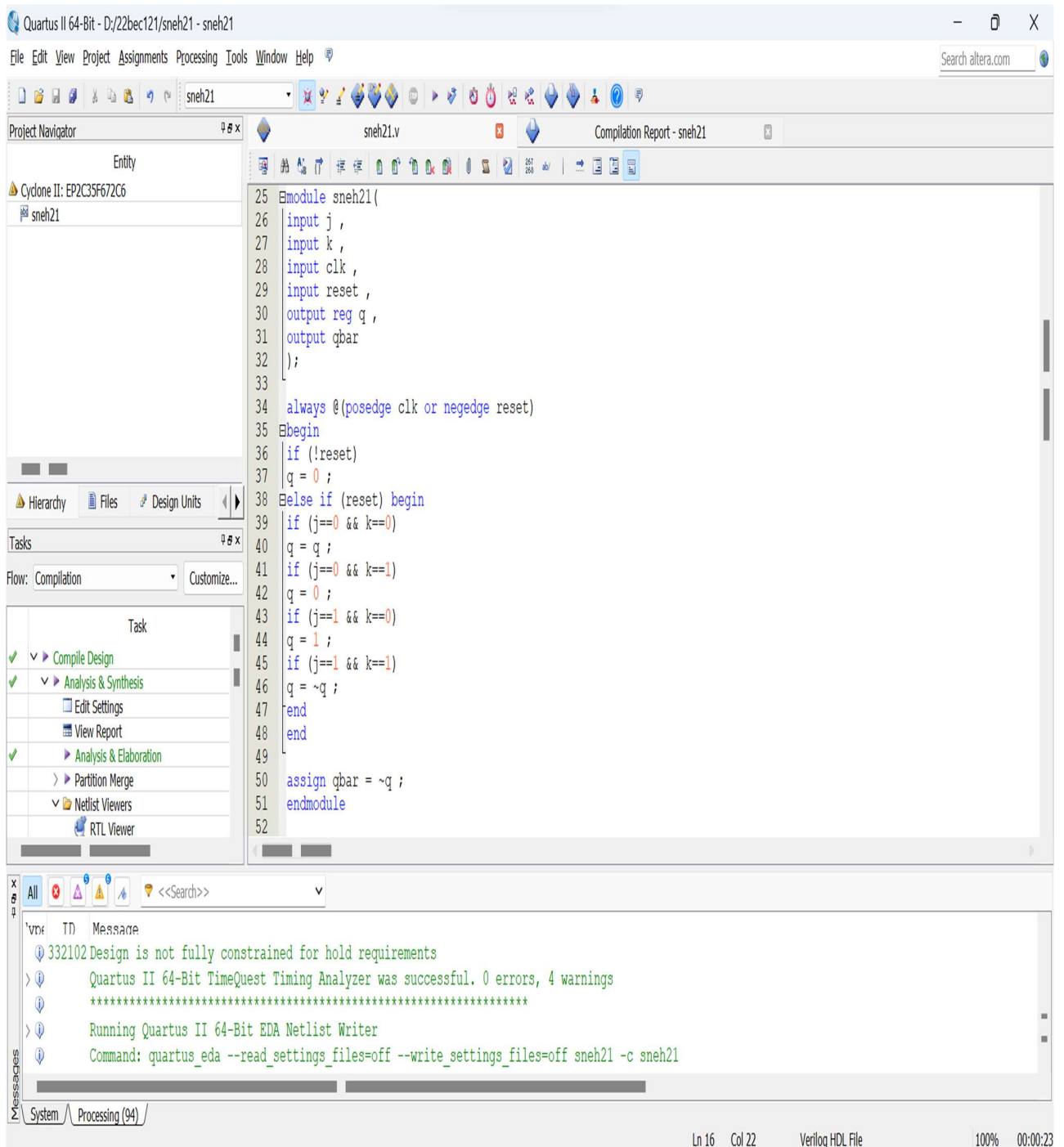
## Code (JK Flip Flop)

```
module sneh21(
```

```
input j ,  
input k ,  
input clk ,  
input reset ,  
output reg q ,  
output qbar  
);
```

```
always @(posedge clk or negedge reset)  
begin  
if (!reset)  
q = 0 ;  
else if (reset) begin  
if (j==0 && k==0)  
q = q ;  
if (j==0 && k==1)  
q = 0 ;  
if (j==1 && k==0)  
q = 1 ;  
if (j==1 && k==1)  
q = ~q ;  
end  
end
```

```
assign qbar = ~q ;  
endmodule
```



**Output 1)Cyclone II (RTL View), 2) Cyclone II (TTL View)**

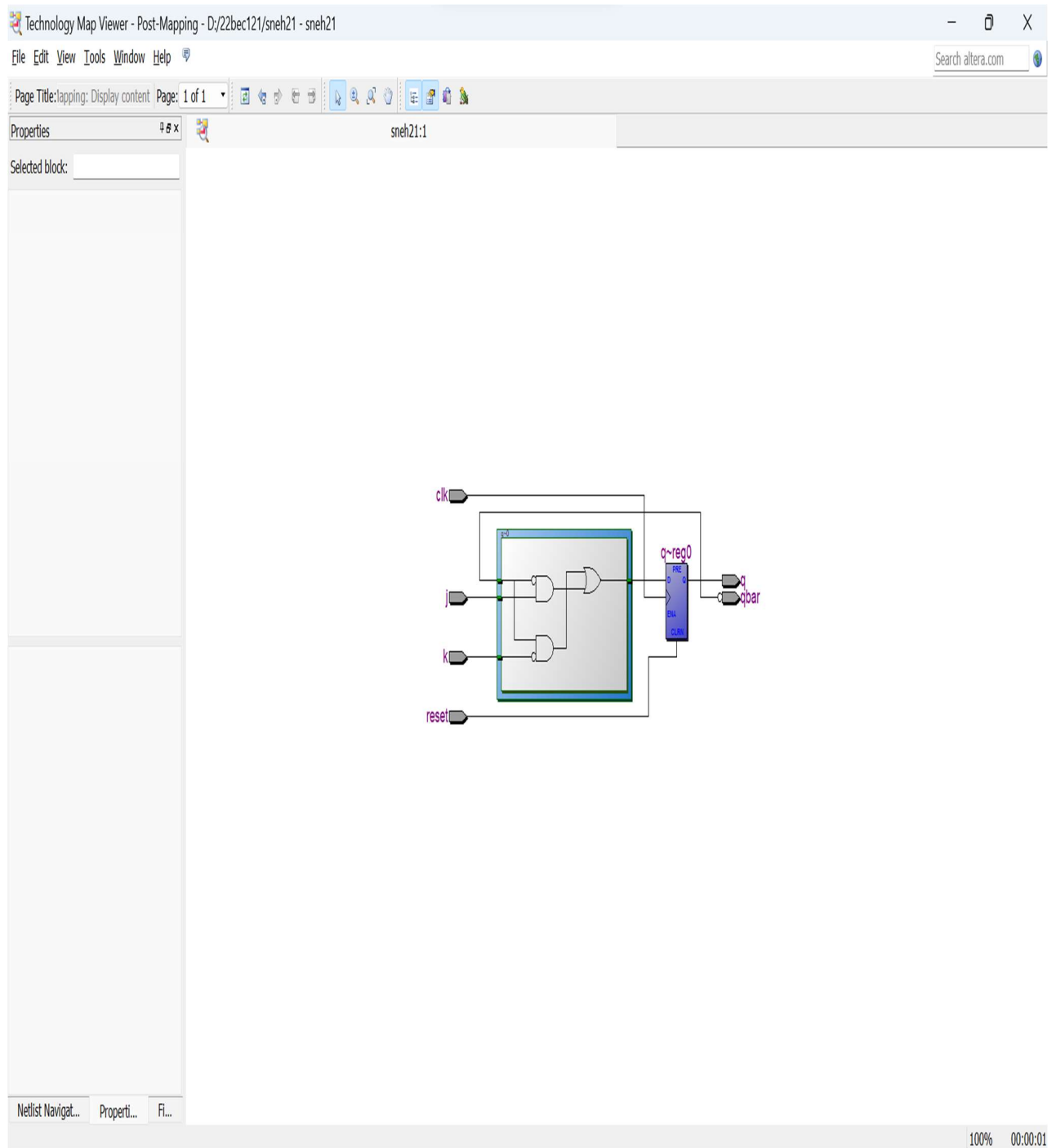
RTL Viewer - D:/22bec121/sneh21 - sneh21

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Properties Selected block: sneh21:1

100% 00:00:01



## Code (T Flip Flop)



```
module sneh21(  
input t ,  
input clk ,  
input reset ,  
output reg q ,  
output qbar  
);
```

```
always @(posedge clk or negedge reset)  
begin  
if (!reset)  
q = 0 ;  
else if (reset) begin  
if (!t)  
q = q ;  
else  
q = ~q ;  
end  
end
```

```
assign qbar = ~q ;  
endmodule
```

Quartus II 64-Bit - D:/22bec121/sneh21 - sneh21

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Project Navigator

Entity

Cyclone II: EP2C35F672C6

sneh21

sneh21.v

Compilation Report - sneh21

```

52 */
53
54 module sneh21(
55     input t ,
56     input clk ,
57     input reset ,
58     output reg q ,
59     output qbar
60 );
61
62     always @(posedge clk or negedge reset)
63     begin
64         if (!reset)
65             q = 0 ;
66         else if (reset) begin
67             if (!t)
68                 q = q ;
69             else
70                 q = ~q ;
71         end
72     end
73
74     assign qbar = ~q ;
75 endmodule
76
77 /*
78 module sneh21(
79     input s ,

```

Tasks

Flow: Compilation Customize...

Task

- ✓ Compile Design
- ✓ Analysis & Synthesis
  - Edit Settings
  - View Report
- ✓ Analysis & Elaboration
- > Partition Merge
- > Netlist Viewers
- RTL Viewer

Messages

All <<Search>>

Message

Running Quartus II 64-Bit EDA Netlist Writer

Command: quartus\_eda --read\_settings\_files=off --write\_settings\_files=off sneh21 -c sneh21

204026 Generated files "sneh21.vo", "sneh21\_fast.vo", "sneh21\_v.sdo" and "sneh21\_v\_fast.sdo" in directory "D:/22bec121/simulation/modelsim/" for EDA sim

Quartus II 64-Bit EDA Netlist Writer was successful. 0 errors, 0 warnings

293000 Quartus II Full Compilation was successful. 0 errors, 11 warnings

System Processing (94)

Ln 48 Col 4 Verilog HDL File 100% 00:00:1

**Output 1)Cyclone II (RTL View), 2) Cyclone II (TTL View)**

RTL Viewer - D:/22bec121/sneh21 - sneh21

File Edit View Tools Window Help

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Properties # x

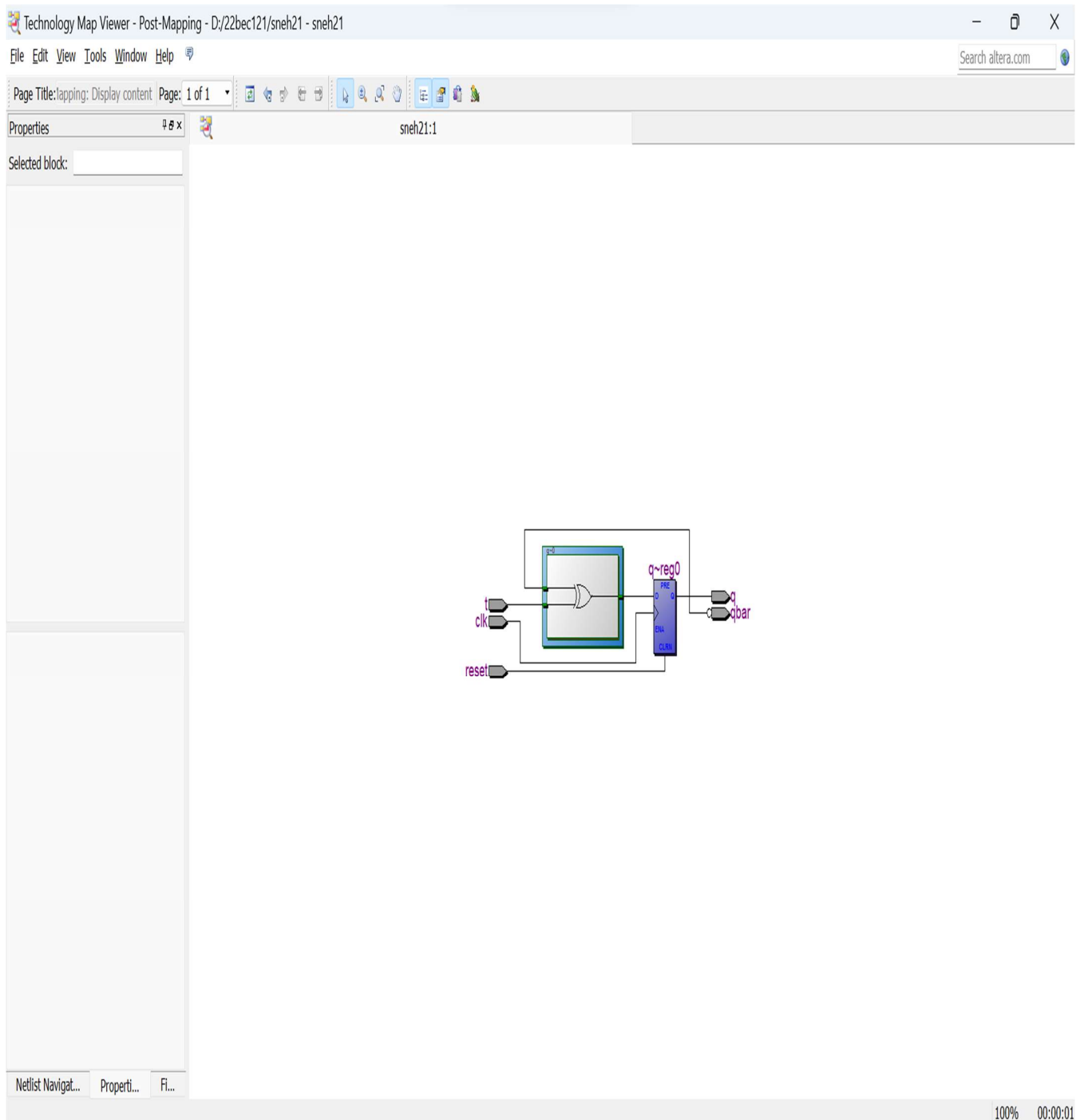
Selected block:

sneh21:1

The diagram shows a D flip-flop block with the following connections:

- PRE** (Preset): Connected to input **t**.
- EN** (Enable): Connected to input **q**.
- CLK** (Clock): Connected to input **clk**.
- CLR** (Clear): Connected to input **reset**.
- D** (Data): Connected to input **q**.
- Q** (Output): Labeled **q~reqQ**, connected to output **q**.
- Q'** (Complement Output): Labeled **qbar**.

Netlist Navigat... Properti... Fi...



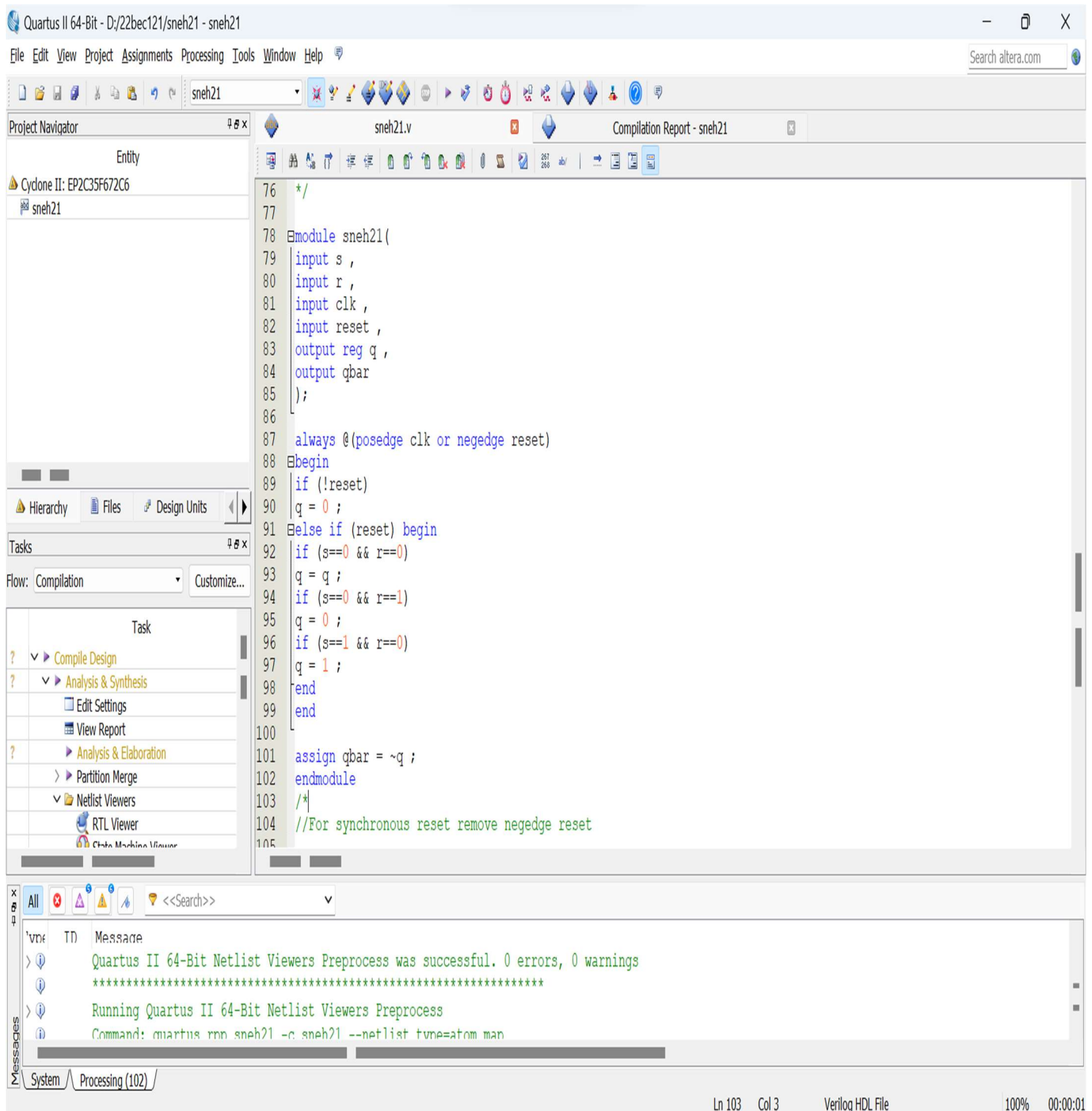
## Code (SR Flip Flop)

```
module sneh21(  
input s ,  
input r ,
```

```
input clk ,  
input reset ,  
output reg q ,  
output qbar  
);
```

```
always @(posedge clk or negedge reset)  
begin  
if (!reset)  
q = 0 ;  
else if (reset) begin  
if (s==0 && r==0)  
q = q ;  
if (s==0 && r==1)  
q = 0 ;  
if (s==1 && r==0)  
q = 1 ;  
end  
end
```

```
assign qbar = ~q ;  
endmodule
```



**Output 1)Cyclone II (RTL View), 2) Cyclone II (TTL View)**

RTL Viewer - D:/22bec121/sneh21 - sneh21

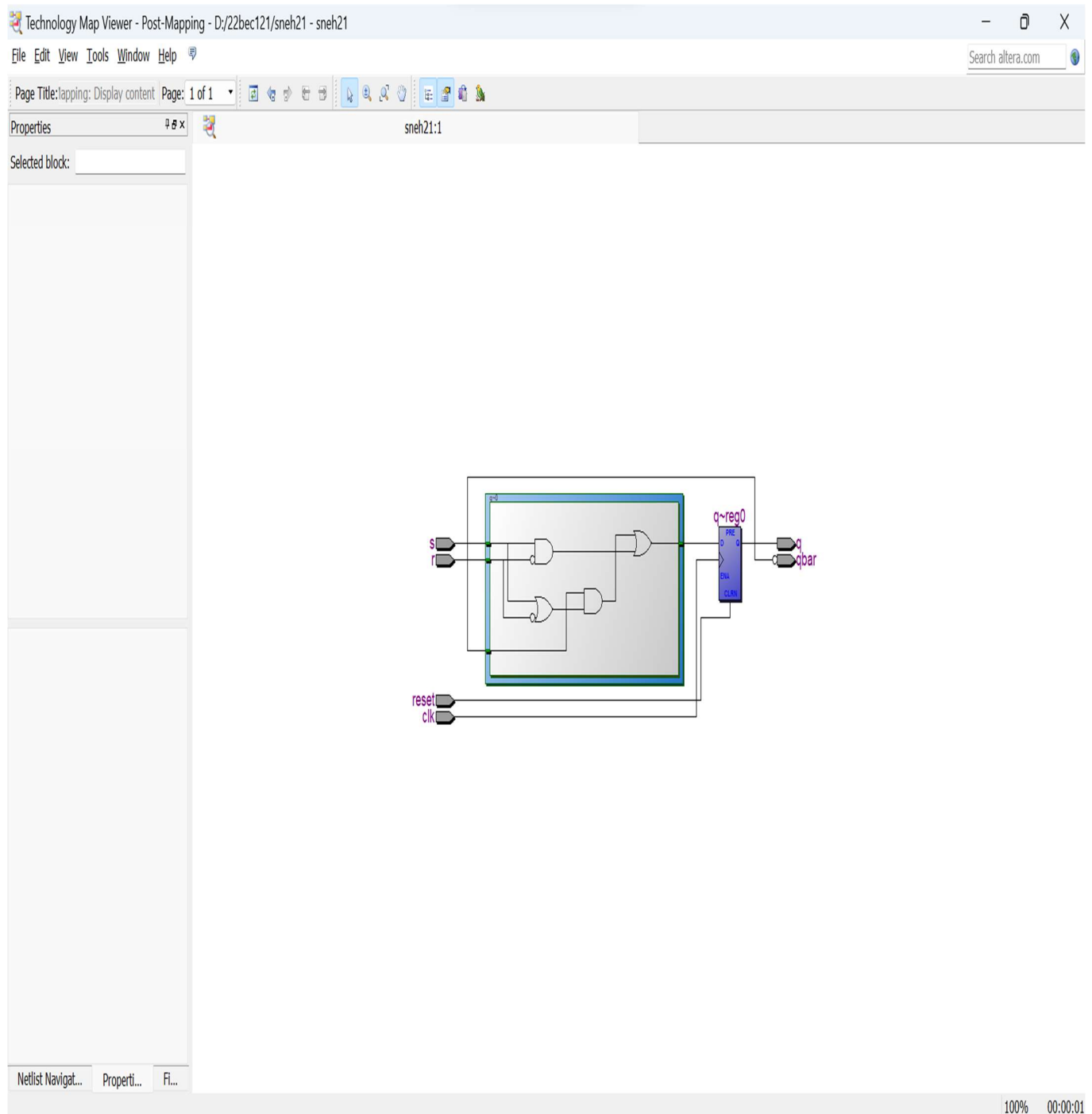
File Edit View Tools Window Help

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Properties Selected block: sneh21:1

Netlist Navigat... Properti... Fi...

100% 00:00:01



**Q2 . Prepare the code for 4 – bit counter (Up/Down). Observer the RTL and TTL of the same.**



## Code

```
module sneh21(  
    input clk ,  
    input rst ,  
    input m ,  
    output reg [3:0]q  
);  
initial  
begin  
    q = 0 ;  
end  
always @(posedge clk)  
begin  
    if (!rst)  
    begin  
        q <= 4'b0000 ;  
    end  
    else if (rst)  
    begin  
        if (m == 0)  
            q <= q + 4'b0001 ;  
        if (m == 1)  
            q <= q - 4'b0001 ;  
        end  
    end  
endmodule
```

Quartus II 64-Bit - D:/22bec121/sneh21 - sneh21

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Project Navigator

Entity

Cyclone II: EP2C35F672C6

sneh21

sneh21.v

Compilation Report - sneh21

```

105 */
106 //4-bit Up Counter (Asynchronous)
107
108 module sneh21(
109     input clk ,
110     input rst ,
111     input m ,
112     output reg [3:0]q
113 );
114     initial
115     begin
116         q = 0 ;
117     end
118     always @(posedge clk)
119     begin
120         if (!rst)
121         begin
122             q <= 4'b0000 ;
123         end
124         else if (rst)
125         begin
126             if (m == 0)
127                 q <= q + 4'b0001 ;
128             if (m == 1)
129                 q <= q - 4'b0001 ;
130         end
131     end
132 endmodule
133

```

Tasks

Flow: Compilation Customize...

Task

- ✓ Compile Design
- ✓ Analysis & Synthesis
  - Edit Settings
  - View Report
- ✓ Analysis & Elaboration
- Partition Merge
- Netlist Viewers
  - RTL Viewer
  - Clock Machine Viewer

Messages

204026 Generated files "sneh21.vo", "sneh21\_fast.vo", "sneh21\_v.sdo" and "sneh21\_v\_fast.sdo" in directory "D:/22bec121/simulation/modelsim/" for EDA sim

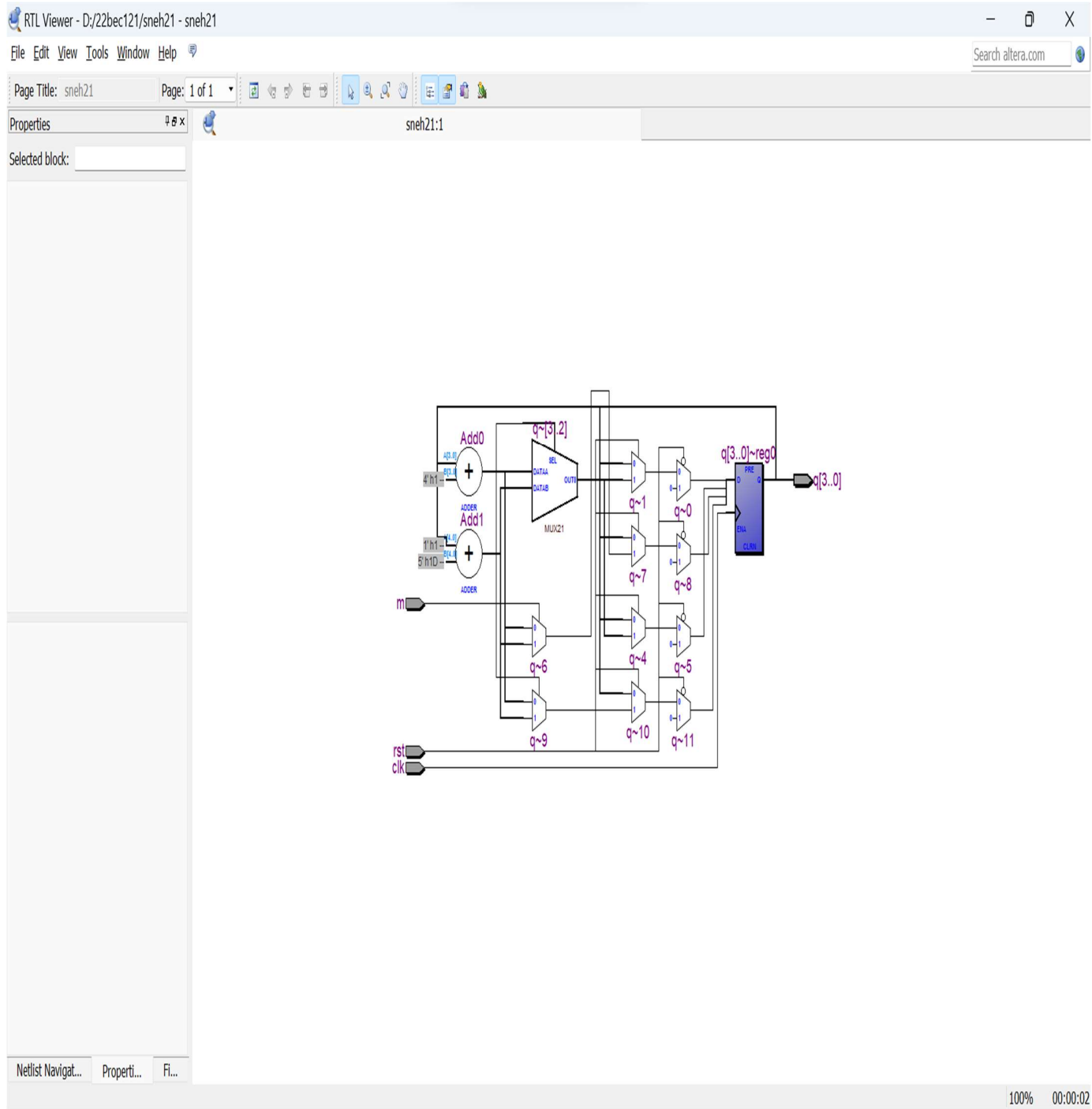
> Quartus II 64-Bit EDA Netlist Writer was successful. 0 errors, 0 warnings

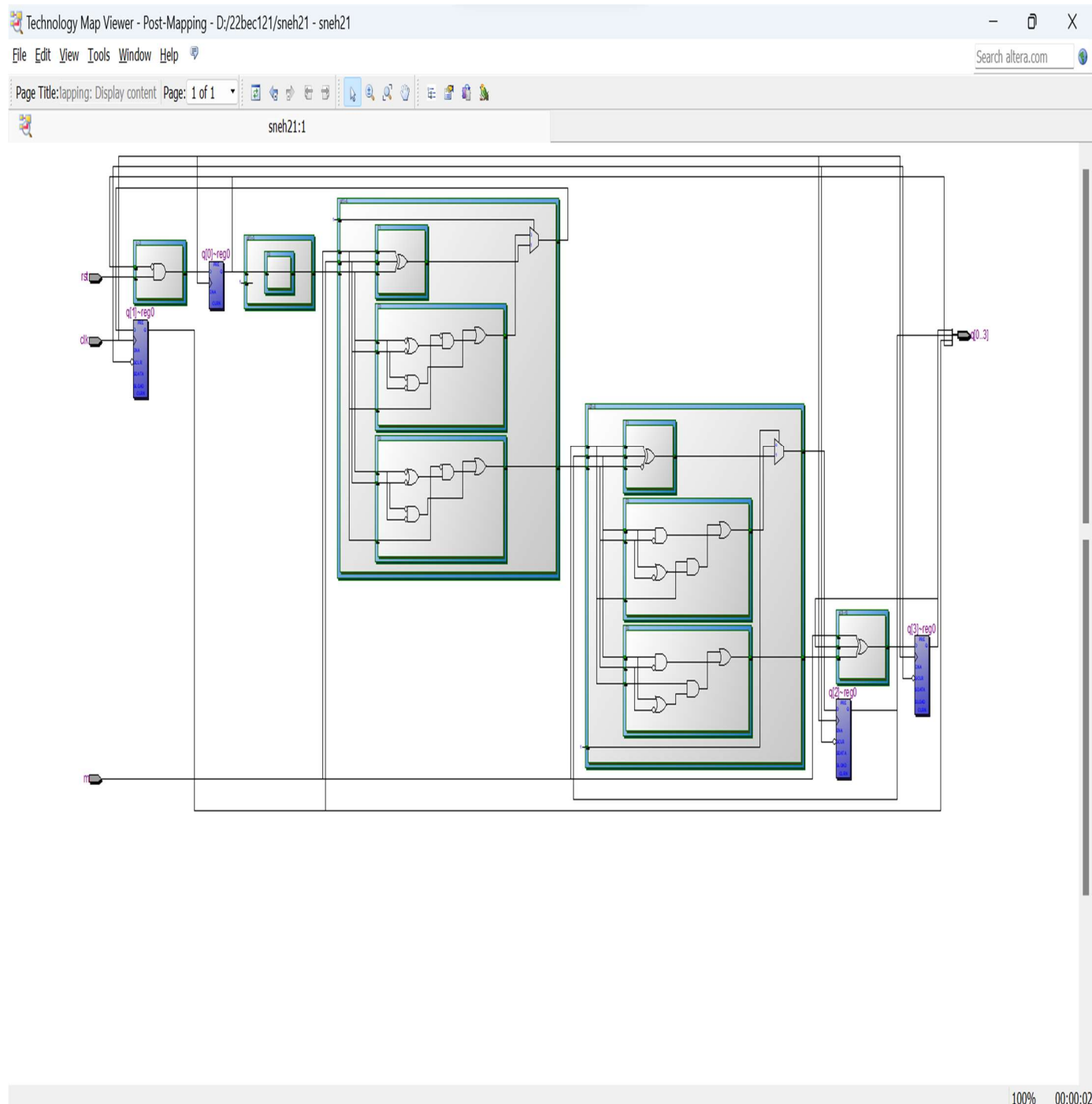
293000 Quartus II Full Compilation was successful. 0 errors, 11 warnings

System Processing (95%)

## Output

### 1)Cyclone II (RTL View), 2) Cyclone II (TTL View)





**Conclusion :-**In this experiment we learnt that how Flip Flops are synthesized and what is their hardware formed while synthesis. A common observation is that every flip flop is synthesized using the D flip flop in RTL as well as TTL View.

**Then we implemented the mode controlled synchronous as well as asynchronous counter in Verilog and further implemented it on FPGA .**