Registers

A register is a group of memory elements (here we use flip-flops) that work together as a unit.

two basic functions of registers:

- Data storage
- Data Movement.

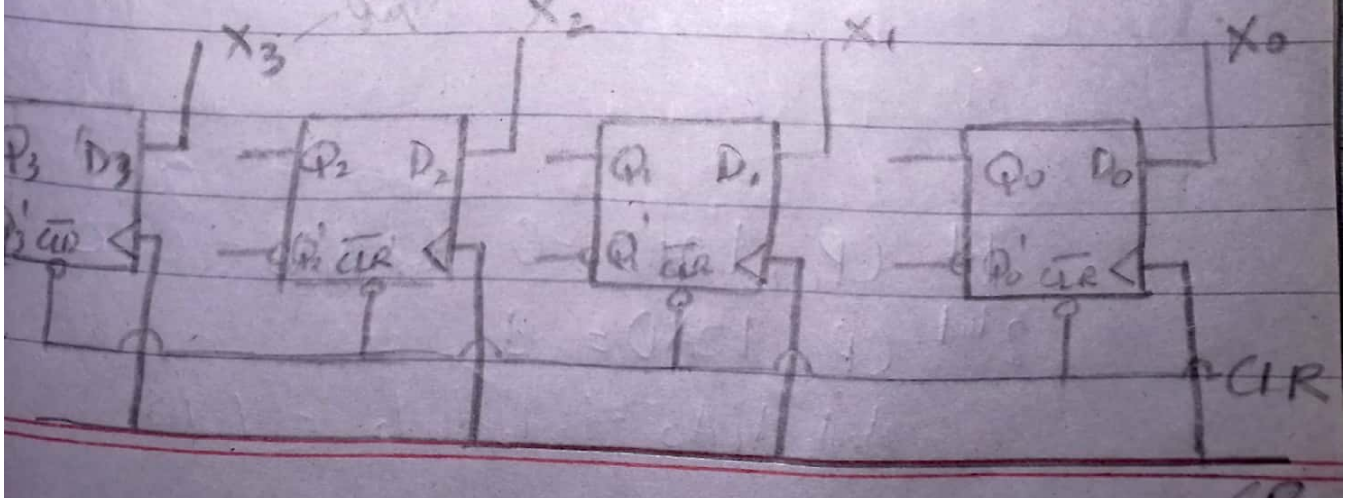
Two types ① Buffer Register
② Shift "

store digital data or load I/O control bus data

moves data left or right, or load I/O control bus data.

Buffer Register: (store digital word)

Q: Design a 4-bit buffer register and discuss its working.



Working:

~~CLR = 0,~~

B.R always use parallel loading.

CLR = 0:

$Q_3 Q_2 Q_1 Q_0 = 0000$

CLR = 1:

1st CP, $Q_3 Q_2 Q_1 Q_0 = X_3 X_2 X_1 X_0 = 1010$

1st CP me ho load ka data ho ye.

Just an example input

Controlled Buffer Register:

Q: Design a 4-bit controlled buffer register & discuss its working.

Working:

CLR = 0:

$A_3 A_2 A_1 A_0 = 0000$

0 (No load)

1 (load)

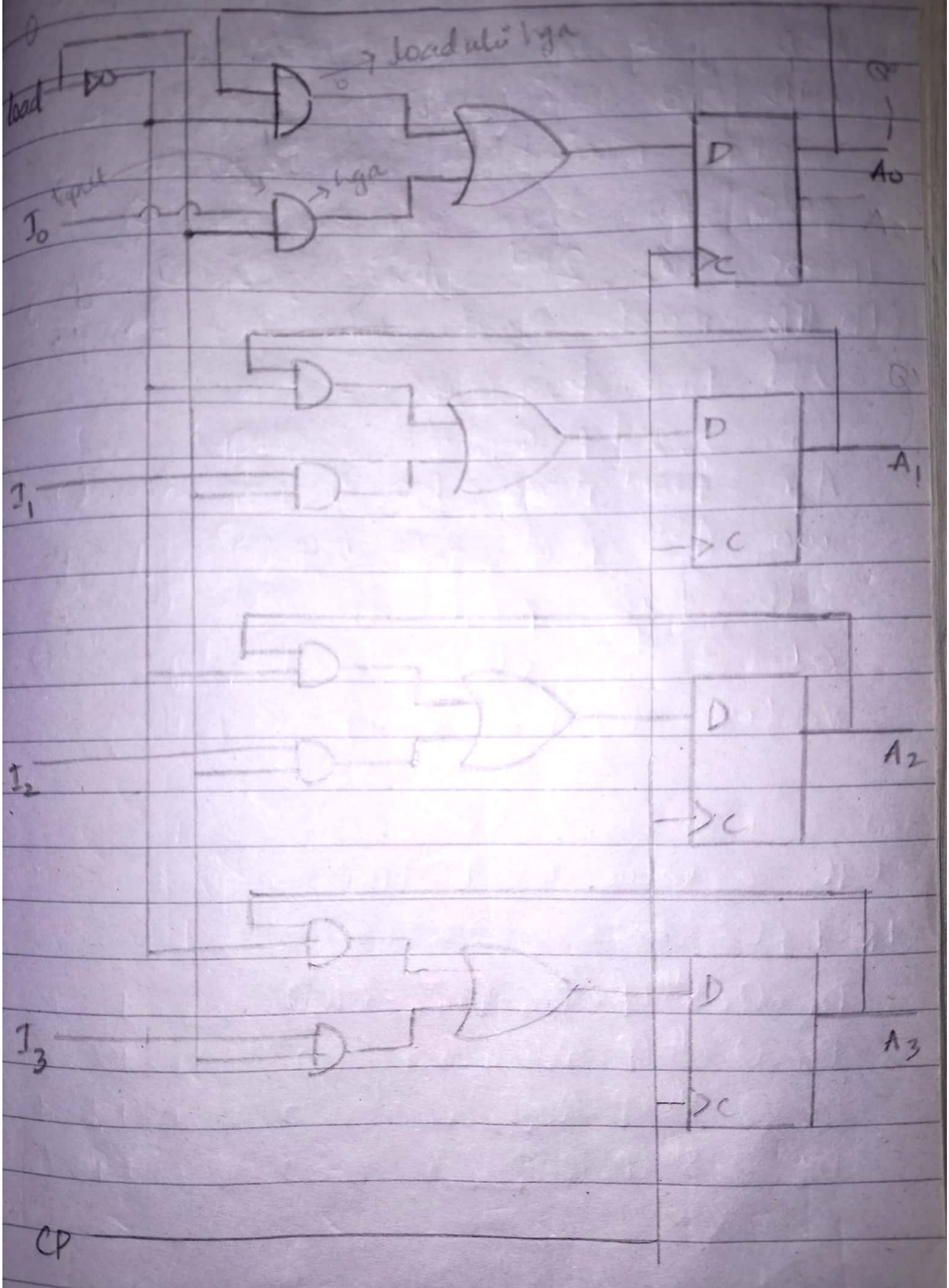
CLR = 1:

1st CP, LOAD = 0, $A_3 A_2 A_1 A_0 = 0000$

previous state maintain

2nd CP, LOAD = 1

$A_3 A_2 A_1 A_0 = I_3 I_2 I_1 I_0 = 1010$


load
I_0
I_1
I_2
I_3
CP
D
C
A_0
A_1
A_2
A_3

can also store data.

① Store kunge

② Read kunge.

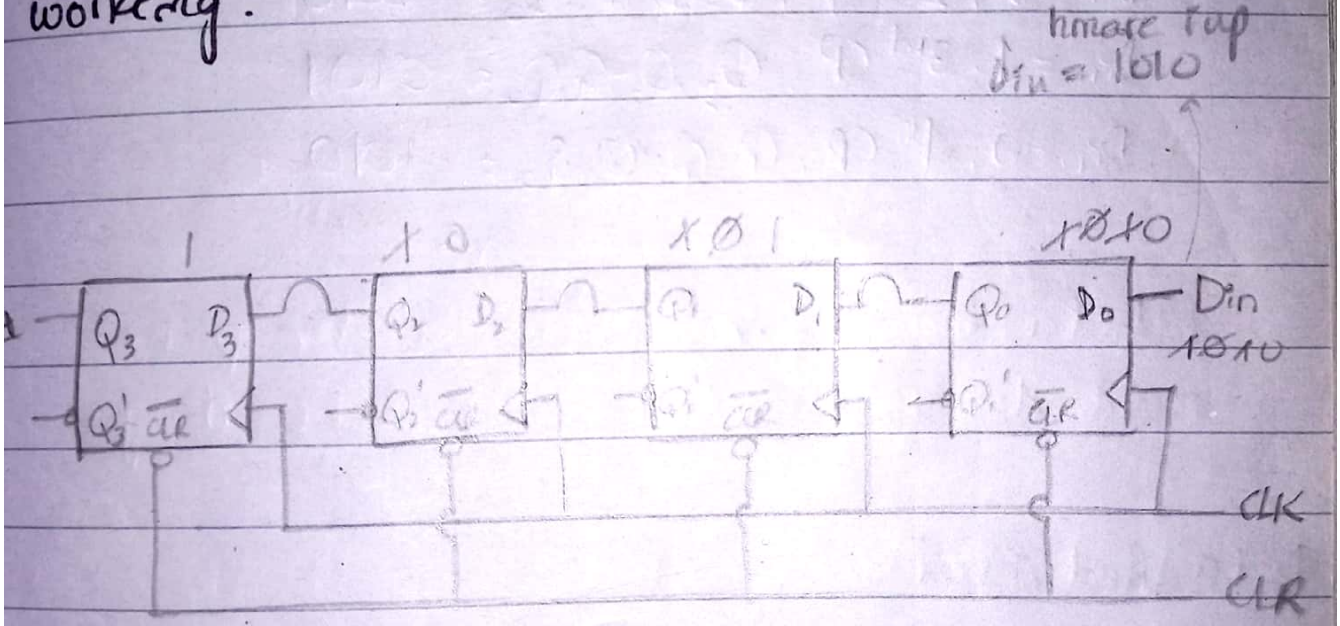
Shift Register:

A shift register moves data bits left or right. (series register)

jo aage se value nikalegi wo wapis gharm ke piche ayegi, use rotate kehte hain.

Shift left Register:

Q: Design a 4-bit shift left register. Also discuss its working.



⇒ Every FF sets up the next flip flop.

aye 1 CP me kam shi krega.

| Din always on LSB FF
| Dout " " MSB FF

Working: 2 parts me kam

① Data store

② " Read.

Data: 1010

Data storage:

CLR = 0, $Q_3Q_2Q_1Q_0$ = 0000

CLR = 1 :

Din = 1, 1st CP, $Q_3Q_2Q_1Q_0$ = 0001

Din = 0, 2nd CP, $Q_3Q_2Q_1Q_0$ = 0010

Din = 1, 3rd CP, $Q_3Q_2Q_1Q_0$ = 0101

Din = 0, 4th CP, $Q_3Q_2Q_1Q_0$ = 1010

Data ko bahir nikalne k liye piche se dummy value (0) 4 bit. bhrge.

Data Retrieval:

CLR = 1 :

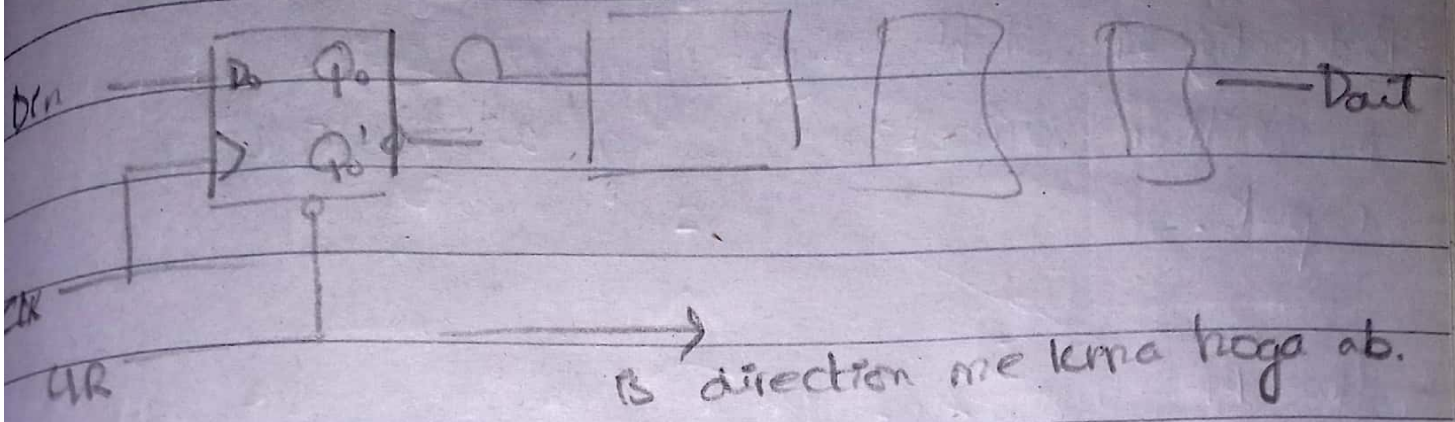
Din = 0, 5th CP, $Q_3Q_2Q_1Q_0$ = 0100, Dout = 1

Din = 0, 6th CP, $Q_3Q_2Q_1Q_0$ = 1000, Dout = 0

Din = 0, 7th CP, $Q_3Q_2Q_1Q_0$ = 0000, Dout = 1

Din = 0, 8th CP, $Q_3Q_2Q_1Q_0$ = 0000, Dout = 0

Shift Right ese hoga



RS direction me krna hoga ab.

1010 → 0 se start hoga right me, left me 1 se krna hoga.

One by one bits assign to (serial Input)

EK sath assign to (Parallel Input / loading)

Input → Output

SISO (Serial In Serial Out)
SIPO (Serial In Parallel Out)
PISO (Parallel In Serial Out)
PIPO (Parallel In Parallel Out).

↳ Buffer Register (All at same time)

Shift registers (Bit by Bit)

Bidirectional Shift Register:

Bidirectional shift registers can shift the data in either direction using a RIGHT/$\overline{\text{LEFT}}$ input.

⇒ 4to FF me 2.2 and gate hen, ek left k lie or ek right k lie. Or use OR gate se connect krdia.

⇒ It will work on SISO.

⇒ RIGHT/$\overline{\text{LEFT}}$ wali input 1 rkhi to mtlb right shift hga or 0 rkhi to left.

⇒ Jaha bhi hme control krna hta he kuch to hm use AND gate se connect kr dete hen.

⇒ Serial data in mera input he jo do jaga connect he bs ek G_7 or ek G_8 mtlb right and left.

⇒ Or isr AND gate ki dosri input RIGHT/$\overline{\text{LEFT}}$ se connect krdi mtlb ke hm agr 1 pass krnge to RIGHT me jaega or left 0 hjaega.

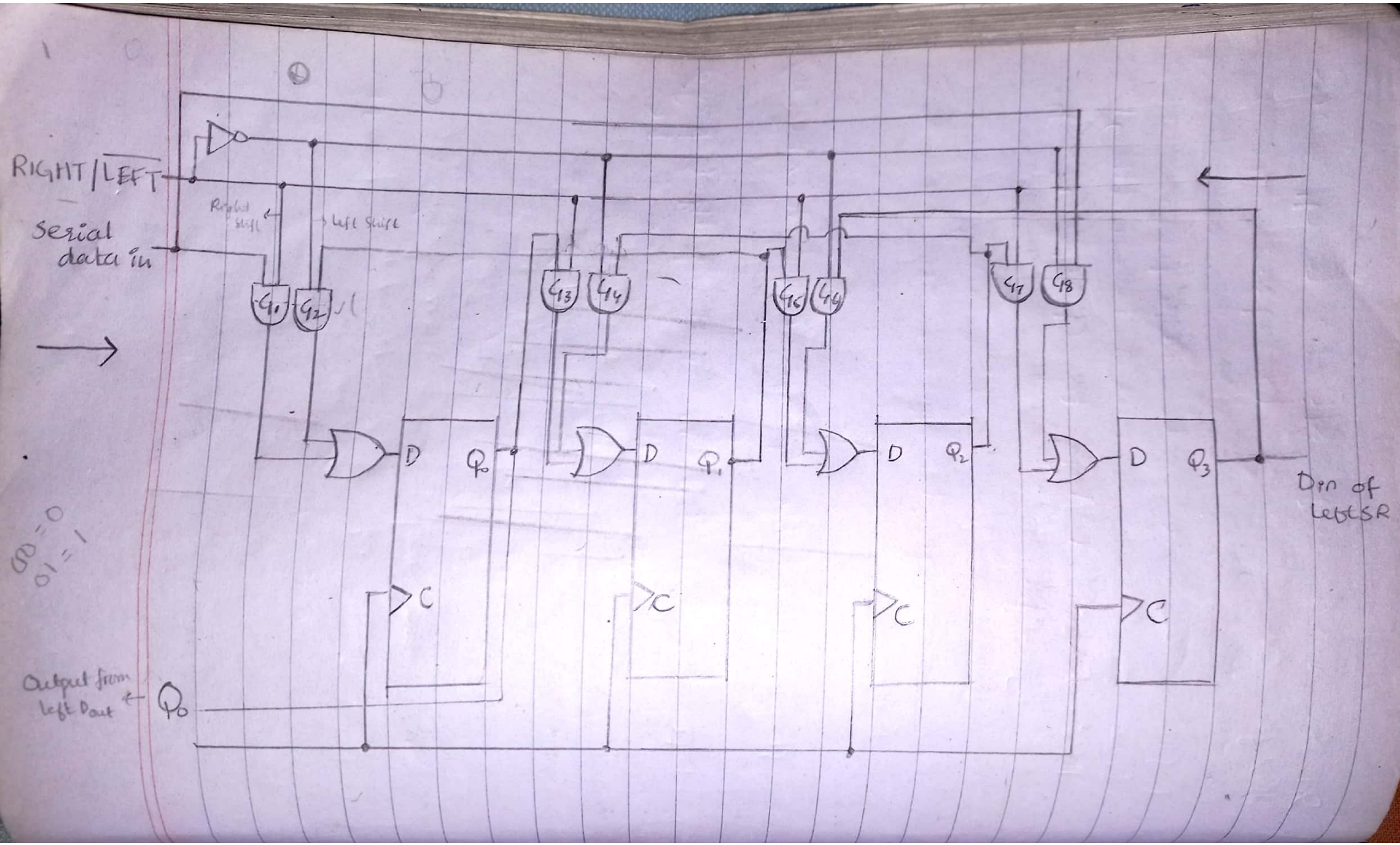
In short 1 duge R/$\bar{L}$ ko to G_1 work krega or 0 duge to G_8.

⇒ left wale sare gate RIGHT/$\overline{\text{LEFT}}$ ki true form se connected hen matlb jb bhi RIGHT 1 hga to G_1, G_3, G_5, G_7 on hjaega.

⇒ Or 0 duge to G_2, G_4, G_6, G_8 on hjaega.

⇒ left k case me Q_0 se output le rhe hen.

⇒ left k case me hr FF ka output picho wale ke AND gate se connected he.


RIGHT/LEFT
Right shift
Left Shift
Serial data in
G1
G2
G3
G4
G5
G6
G7
G8
D
Q0
Q1
Q2
Q3
C
Din of LeftSR
S0=0
S1=1
Output from left Dout
Q0

Controlled Shift Register.

3 possible cases honge.
1. Value load krhi hogi.
2. Value shift krhi hogi
3. Dono me se kuch nhi mtlb
Value retain krhi hogi

Q: Design a 4-bit controlled shift left register. Also discuss its working.

Control krne k lie AND gates l gate hen
to yhn 3 cheezon ko control krna he to
3 AND gate) lga denge or OR perform krdenge

⇒ jb load krenge to us wqt abr shift nhi krenge or na retain krenge

⇒ jb retain hogi to load or shift dono nhi hogi.

⇒ NOR (0 → 0 = 1)

no shift (↑ from second 0); no load (↓ from first 0); → retain (from 1)

jb SHL and load ko 0,0 denge
to NOR Gate me 1 ajaega mtlb
retain hogi value.

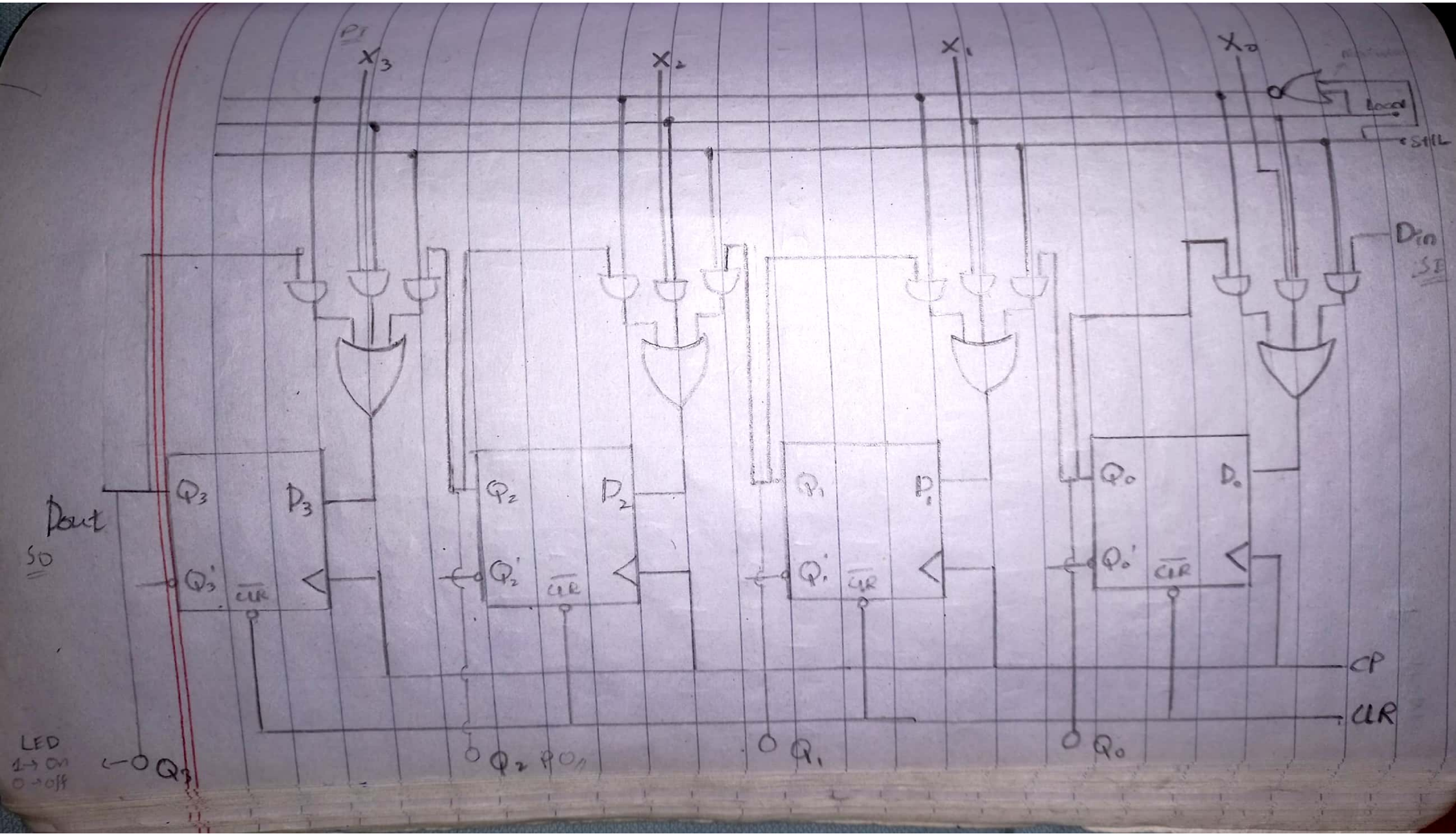
Jb shift krna he to ek Din bhi dnga to Din or shift ko ek gate se connect krdia.

=> Din sirf 1st me dnge or wo aage shift hota rhega. mtlb hr FF ka output dosre ka input bnega shifting me

=> Shift a load sath sath nhi hskta kyu ke ek loading me value aati hai or ek shifting ki value hoti to data clash hjega.

=> load ki true form me sabhi parallel input connect krta he to X_0 X_1 connect kr dnge.

=> Ds diag me serial input bhi hsktI or parallel bhi. Same for output.


X3
X2
X1
X0
Load
Shift
Din
SI
Q3
P3
Q2
P2
Q1
P1
Q0
D0
Dout
SO
Q3'
Q2'
Q1'
Q0'
CLR
CP
LED
1 → On
0 → Off
Q3
Q2
Q1
Q0