CSE 2441 – Introduction to Digital Logic
Fall 2014
Term Design Project

Objective: The term project consists of a design and implementation task that is based on knowledge you gained throughout the semester in the lecture and lab sessions. It is meant to challenge your ability to apply your understanding and knowledge of logic design on a practical problem. This is an **individual** project, so group design and reporting is neither appropriate nor acceptable.

Grading: The project will be graded as follows and will count 15% toward your final CSE 2441 course grade. Failure to complete the project will result in a course grade of Incomplete or F depending upon your standing in the course.

85% -- design completed, simulated, implemented, tested and meets all specifications
15% -- project report completed and submitted and meets all requirements
Bonus points (10 maximum) -- additional features or enhancements above the required specifications

ABET outcome assessment: ABET, Inc. is the organization that accredits engineering programs in the United States and in many other countries around the world. One of the accreditation criteria requires documentation that students have demonstrated an ability to design a system, component, or process to meet desired needs within realistic constraints. The CSE 2441 term design project has been selected as one source of this documentation for the Computer Engineering Program at UT Arlington.

Project timeline

11/11/2014 – Project assigned.

11/11/2014 – 12/3/2014 – The laboratory (127 ERB) will be open during regular lab hours and during TA office hours for demonstration of your completed design and/or for consultation. The one-hour rule will apply.

12/3/2014 – Last day to demonstrate project on the DE1.

12/3/2014 – All deliverables due by 5:00 PM.

Project description: There are three parts to this semester's project. All are centered on completing the design and implementation, on the DE1, of the TRISC processor. A RAM (TRISCRAM16x8A and TRISCRAM16x8C) module will be provided for use in your final implementation of parts A and C.

Part A (50 points) – Integrate the TRISC components that have been completed in the laboratory exercises, including the controller from lab 9, to implement a functioning processor that can execute a program consisting of INC and CLR instructions.

- Inputs – Clear/start (KEY0), clock (KEY1)
- Outputs – MAR(HEX0), MDOut(HEX1), MDIn(HEX2), controller output signals (LEDs)
- Must properly execute a program stored in TRISCRAM16x8A

Part B (25 points) – Design a controller module for TRISC that implements the LDA, STA, ADD, JMP, INC, and CLR instructions.

- Inputs – Clear/start (KEY0), clock (KEY1), IR (SW3, SW2, SW1, SW0)
- Outputs – State or phase variables (HEX0-HEX3 as necessary), controller output signals (LEDs)
- Must properly generate the control signal sequence for any or all of the LDA, STA, ADD, JMP, INC, and CLR instructions.

Part C (25 points) – Integrate the controller from Part B with TRISC components completed in the laboratory to implement a functioning processor that can execute a program consisting of LDA, STA, ADD, JMP, INC, and CLR instructions.

- Inputs – Clear/start (KEY0), clock (KEY1)

- Outputs – MAR(HEX0), MDOut(HEX1), MDIn(HEX2), controller output signals (LEDs)
- Must properly execute a program stored in TRISCRAM16x8C

Design and Implementation Tasks

1. Develop designs that meet the specifications. Identify design alternatives that you considered and why they were not chosen.
2. Capture and verify your design using Quartus II. You may use schematic capture or Verilog.
3. Implement and test your designs on an Altera DE-1 board.
4. Document your work in the laboratory notebook throughout the process.

Deliverables

1. Hard copy and electronic copy of the Term Design Project Report and an electronic copy of your design files. **Due by 5:00 PM on December 3 to carroll@uta.edu.** The report should be formatted as follows.
   - Cover sheet
   - Table of contents
   - List of figures and tables
   - Introduction
     - Project overview (include requirements and any added or special features)
     - Project status including any unresolved problems and future plans
     - Report overview
   - System design
     - System-level description and diagrams
     - Subsystem descriptions and diagrams
     - Hierarchical design structure
     - Operating procedure
   - Controller design details
     - Functional description and diagram showing I/O
     - State diagrams
     - Schematic diagrams and/or Verilog code
     - DE1 pin assignments
   - Alternative design considerations
     - Alternatives considered
     - Reasons for selection of final design
   - Integration and Test Plan
     - Integration strategy
     - Test strategy
     - Simulation results from Quartus II
     - Test results from DE1 implementation
   - Conclusion
     - Resolution of design and/or implementation issues
     - Lessons learned

2. Altera DE1 implementation of your design. **Must be demonstrated in the laboratory on or before 5:00 PM on December 3.**

3. Your lab notebook.

Note – you may pick up your report and notebook after course grades have been submitted (December 16). Unclaimed materials may be discarded after February 2, 2015.