Name: _____ ID# _____

Date Submitted: _____ Lab Section # _____

CSE 2441 – Introduction to Digital Logic Fall Semester 2014

Lab Number 6 – An Introduction to Synchronous Circuits

100 Points

(To be performed October 16-17, 2014)

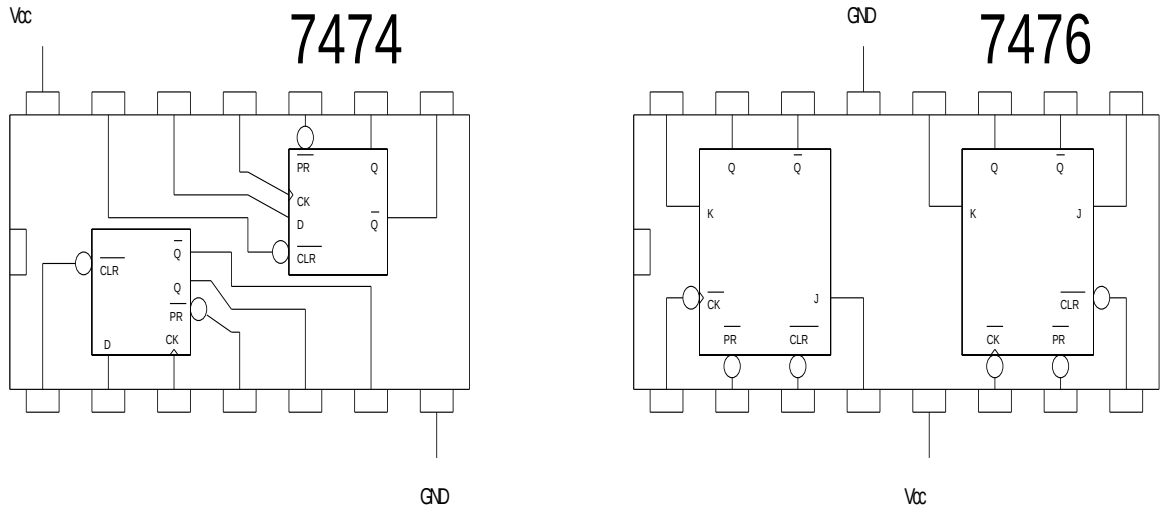
CSE 2441 **LABORATORYSESSION 6** **FALL 2014**

AN INTRODUCTION TO SYNCHRONOUS CIRCUITS

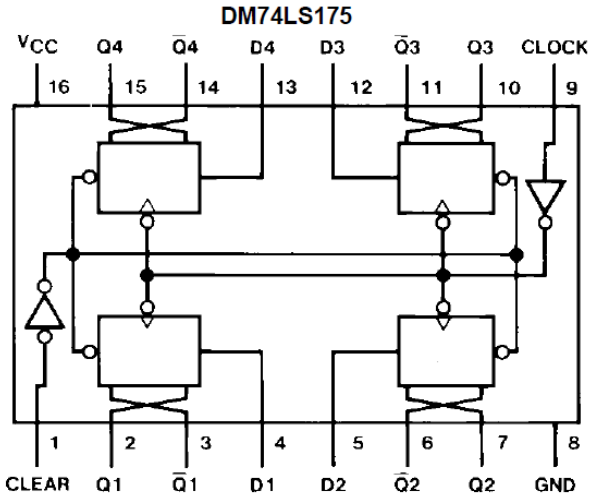
(100 POINTS)

PURPOSE/OUTCOMES -- To study the functional characteristics of D and JK flip-flops and their use in realizing basic registers and counters. After completing this laboratory, you'll have an understanding of how flip-flops work and be able to analyze and design basic registers and counters. Devices and circuits studied in this laboratory wil be implemented on the IDL-800.

BACKGROUND -- Flip-flops and latches are used as memory devices in sequential logic circuits. The D and JK flip-flop are the most commonly used flip-flops in synchronous sequential circuits. The figures below show pin-out diagrams for SN7474 and SN7476 implementations of D and JK filp-flops, respectively. Note that each package contains two flip-flops and that each flip-flop has data inputs, D or JK, clock inputs, clear and preset inputs, and complementary outputs. **Also note that the SN7476 uses non-standard Vcc and GND pins.**

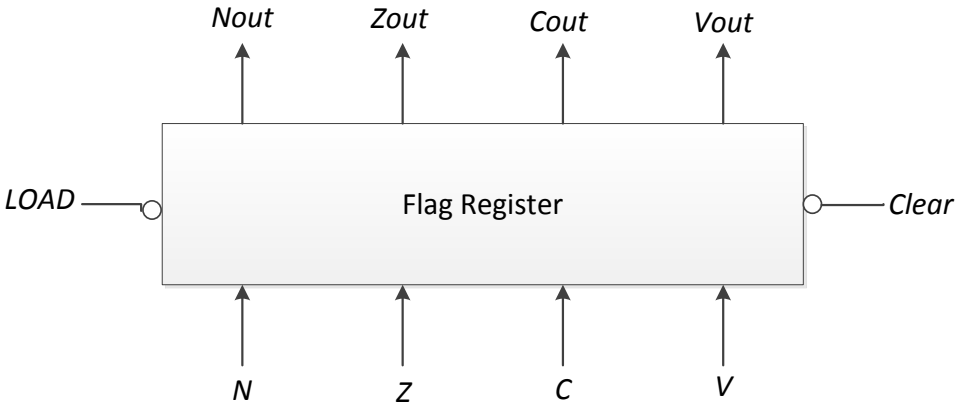


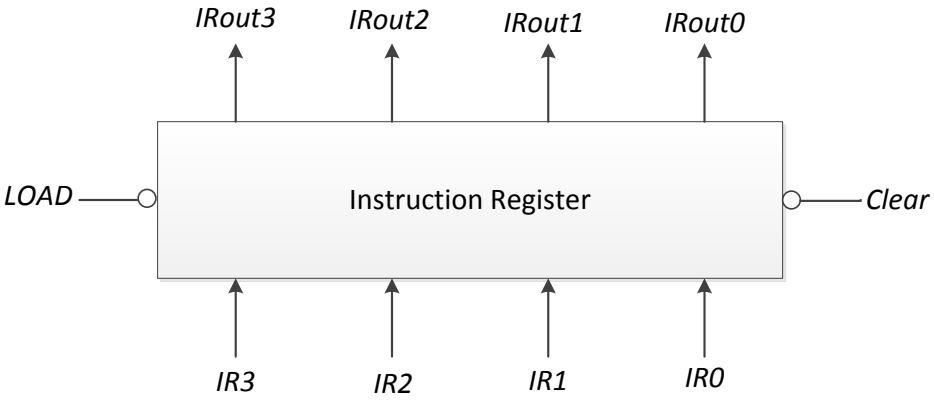
An SN74175/DM74LS175 is a four-bit data register with pin-outs as shown below. It contains four D flip-flops with common clock and clear signals.



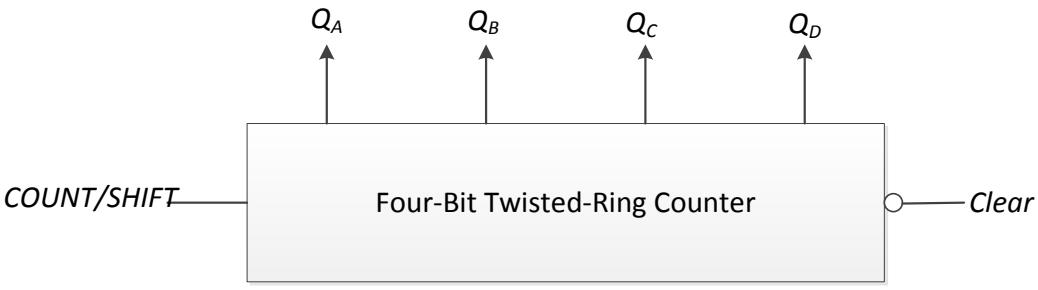
PRELAB ASSIGNMENT

1. Design the Instruction Register (IR) and Flag Register (FR) for your TRISC realization. Use a 74175 and other logic gates, as needed, in the realization. Capture and save your designs as block symbol files.





2. Design a four-bit twisted-ring (Johnson) counter using a 74175 as the basic component. Capture your design with Quartus II and save as a block symbol file for later use.



LAB ASSIGNMENT -- Complete each of the exercises detailed below on your solder-less breadboard and IDL-800, and record your results and answers in your laboratory notebook. Have the lab instructor check your work after each part.

Part 1 – Learn the functionality of D (SN7474) and JK (SN7476) flip-flops

Experimentally derive the state table of an SN7474 D flip-flop. Use the table format below. Use the following pin assignments when connecting the 7474 to the IDL-800.

D (pin 2) – SW7 *CK* (*pin 3*) – PULSE SWITCH A
Pre (*pin 4*) – SW1 *Clr (pin 1)* – SW0
Q (pin 5) – LED7 *Q' (pin 6)* – LED6
Power (pin 14) – +5 V *Ground* (*pin 7*) – GND

Present State (Q)	*Next State (Q*)*							
	PreClr = 00		PreClr = 01		PreClr = 10		PreClr = 11	
	D = 0	D = 1	D = 0	D = 1	D = 0	D = 1	D = 0	D = 1
0	NA	NA						
1	NA	NA						

NA – Not Allowed

Experimentally derive the state table of an SN7476 JK flip-flop. Use the table format below. Use the following pin assignments when connecting the 7476 to the IDL-800.

J (pin 4) – SW7 *K(pin 16)* *CK* (*pin 1*) – PULSE SWITCH A
Pre (*pin 2*) – SW1 *Clr (pin 3)* – SW0
Q (pin 15) – LED7 *Q' (pin 14)* – LED 6
Power (pin 5) – +5 V *Ground* (*pin 13*) – GND

Present State	*Next State*															
	PreClr = 00				PreClr = 01				PreClr = 10				PreClr = 11			
	JK= 00	JK = 01	JK = 10	JK = 11	JK = 00	JK = 01	JK = 10	JK = 11	JK = 00	JK = 01	JK = 10	JK = 11	JK = 00	JK = 01	JK = 10	JK = 11
0	NA	NA	NA	NA												
1	NA	NA	NA	NA												

NA – Not Allowed

Part 2 – Implement and test your FR/IR design. Your test procedure should demonstrate that *Clear* works correctly and that *Load* works for input patterns *0000*, *0101*, *1010*, and *1111*.

Part 3 – Implement and Test Your Four-Bit Twisted Ring Counter as follows.

a. Connect the *COUNT* input to the IDL-800 FUNCTION GENERATOR with amplitude at the Max setting. Place the FUNCTION GENERATOR in square-wave mode and 1-HZ to 10-HZ frequency range. Place the freguency fine-tune knob in its minimum (CCW) position. These settings should produce a clock pulse with a frequency of about 1-HZ.
b. Place the counter in the all-0 state.
c. Observe and record the state sequence of the counter in the form of a state diagram.
d. Slowly increase the frequency of the clock by turning the fine-tune knob clockwise. How does the state sequence change?
e. How many states would be in a 6-bit twisted-ring counter? *N*-bit?