Name: _____ ID# _____

Date Submitted: _____ Lab Section # _____

CSE 2441 – Introduction to Digital Logic Fall Semester 2014

Laboratory 1 – Policies, Procedures, Resources, Gates

100 Points

To be performed August 28-29, 2014

CSE 2441 LABORATORY SESSION 1 Fall 2014

Policies, Procedures, Resources, Gates

(100 Points)

PURPOSE: To introduce you to the digital logic lab policies and procedures and the equipment, tools, parts, and software that you'll be using during the semester.

POLICIES and PROCEDURES:

1. Laboratory assignments and other documents will be placed on the course Blackboard in advance. You have the responsibility for downloading and reading the relevant documents each week prior to your laboratory session. Some sessions require pre-work that must be completed before your come to lab. You will not be allowed to start the in-lab work unless you have completed the pre-work.
2. You are expected to record laboratory results in a notebook that will be provided by the department.
3. Most assignments will be due at the end of the scheduled laboratory period. Late submissions will be subject to a five-point reduction per day.
4. Most assignments will be performed individually.
5. You will be required to complete a significant design project at the end of the semester.
6. Please report any faulty equipment or parts to the TA as soon as possible.

RESOURCES:

1. **IDL-800 Digital Lab** – The IDL accommodates the assembly, implementation, and test of small digital logic circuits. It consists of a solder-less breadboard, power supplies, input switches, output LEDs, a function generator, and a digital volt meter (DVM).
2. **Parts kit** – You will be provided a parts kit containing a solder-less breadboard, commonly used integrated circuits (ICs), and jumper wire. ***You will be required to return the parts kit at the end of the semester.*** Additional parts will be available in the lab as needed. Please see the attached document for more details regarding IC nomenclature and package layout of some of the ICs available in the lab.
3. **Tools** – wire strippers, IC pullers, logic probes, etc. are available in the lab.
4. **Altera DE1 Design and Education Board** – The DE1 accommodates the implementation and test of small to complex digital logic circuits utilizing the Altera Cyclone II field programmable gate array (FPGA) and supporting devices. A DE1 will be checked out to you later in the semester. ***You will be required to return the DE1 at the end of the semester.***
5. **Software** – Altera Quartus II (v13.0sp1) Web-Edition is Installed on lab PCs in 127 ERB and on OIT PCs in the ELB. You may want to download the software to your own laptop from Altera. The web-edition is free. **DO NOT** download versions later than v13.0sp1!! Later versions are not compatible with the DE1 technology. Quartus II is Altera's industry standard computer-aided-design (CAD) software for design capture, simulation, and implementation of digital logic circuits.
6. **Flash drive** – please store your design and simulation files on a flash drive so that you can reuse them in future assignments if applicable.

TODAY'S ASSIGNMENT

1. Become familiar with the features of the IDL-800. Read the manual and practice using the switches and displays.
2. Perform the experiments (1-6) in Chapter 1 of the IDL-800 manual. Note that the ICs have been pre-inserted in the breadboard. You will need to wire power, ground, and input/output (I/O) connections for the experiments. You may connect the gate inputs to switches in parallel to save time. Use switches *SW1* and *SW0* for variables *A* and *B*, respectively. Connect gate outputs to LEDs for observing the results. Note that each IC chip contains multiple gates. However for this exercise, it's only necessary to use one gate per chip. Figure 1 shows a typical wiring layout for this experiment.
3. Record the results of your experiments in your laboratory notebook according to the format given below. Use the IDL-800 DVM to measure the actual gate input and output voltages (V_I) for each experiment. ***Have your lab instructor check your work after each part.***

1) NOT gate experiment (SN74LS04)

A	V_A	***Y***	V_Y
0			
1			

Y = *logic expression****?***

2) AND gate experiment (SN74LS08)

A	V_A	***B***	V_B	***Y***	V_Y
0		0			
0		1			
1		0			
1		1			

Y = ?

3) OR gate experiment (SN74LS32)

A	V_A	***B***	V_B	***Y***	V_Y
0		0			
0		1			
1		0			
1		1			

Y = ?

4) NAND gate experiment (SN74LS00)

A	V_A	***B***	V_B	***Y***	V_Y
0		0			
0		1			
1		0			
1		1			

Y = ?

5) NOR gate experiment (SN74LS02)

A	V_A	***B***	V_B	***Y***	V_Y
0		0			
0		1			
1		0			
1		1			

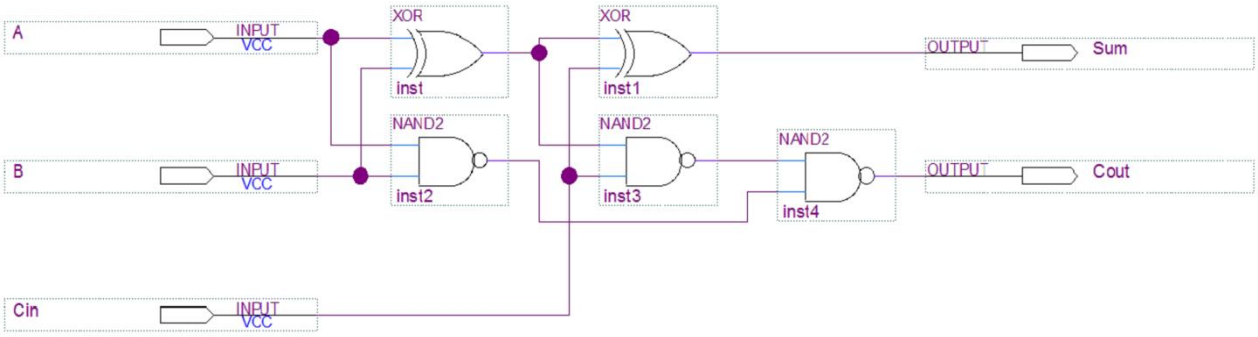
Y = ?

6) XOR gate experiment (SN74LS86)

A	V_A	***B***	V_B	***Y***	V_Y
0		0			
0		1			
1		0			
1		1			

Y = ?

4. Implement and test the following full-adder realization.



a. Construct the circuit using available gates in the SN74LS00 and SN74LS86 chips. Figure 2 shows a typical wiring layout for this circuit.

b. Experimentally complete the following truth table for the circuit. Use *SW2*, *SW1*, and *SW0* for variables *A*, *B*, and *Cin*, respectively. Display *Cout* and *Sum* on *LED1* and *LED0*. ***Have your lab instructor check your work.***

A	***B***	***Cin***	***Cout***	***Sum***
0	0	0		
0	0	1		
0	1	0		
0	1	1		
1	0	0		
1	0	1		
1	1	0		
1	1	1		

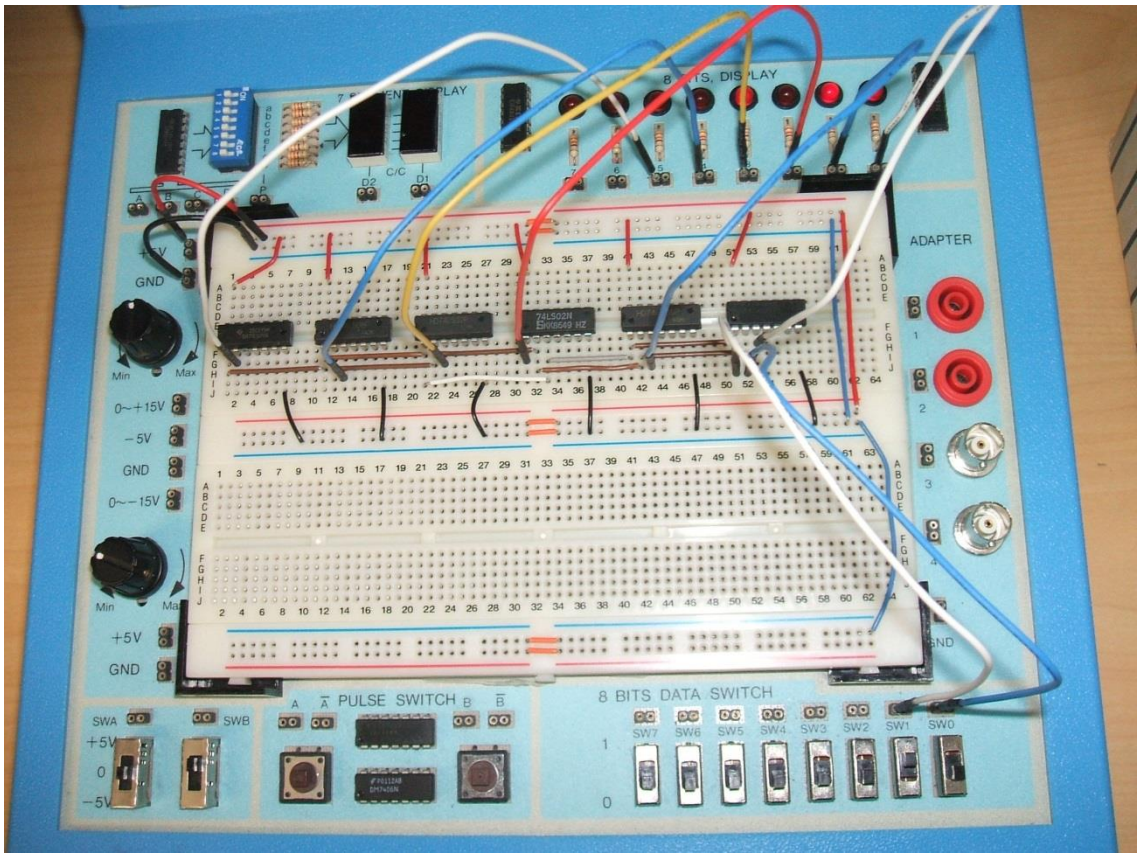


Figure 1 – Gates wired in parallel on wireless breadboard and IDL-800.

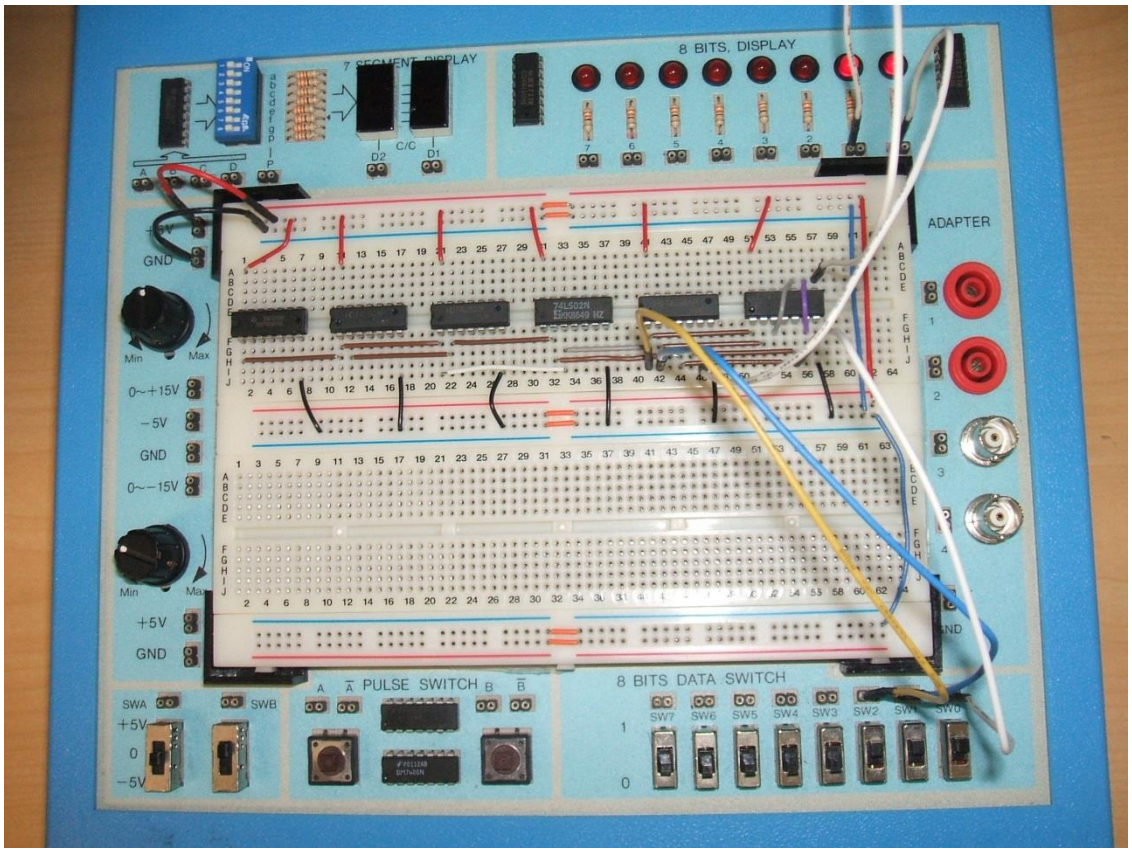


Figure 2 – Full-Adder layout and connectivity on IDL-800.