Name:		ID#
Date Submitted:	Lab Section #	
CSE 2441 – Introduction to Digital Logic		Fall Semester 2014
Lab Number 9 – Processor Control Unit		
To be performed November 6-7, 13-14, 2014		

PROCESSOR CONTROL UNIT

(100 POINTS)

PURPOSE/OUTCOMES

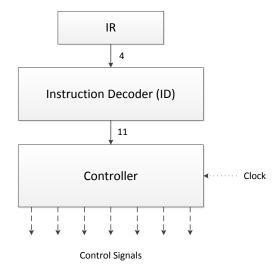
To design, implement on the DE1, and test an Instruction Decoder (ID) and controller for a subset of the Tiny Reduced Instruction Set Computer (TRISC) instruction set. By successfully completing this assignment, you will have demonstrated an ability to design a simple FSM-based controller.

BACKGROUND

You have been designing and implementing various components, e.g., ALU, PC, AC, IR, and FR, for the Tiny Reduced Instruction Set Computer (TRISC) over the past several laboratory exercises. In this lab, you will design and implement an Instruction Decoder (ID) and a controller to fetch and execute the INC and CLR instructions. Please refer to the class notes for more details on TRISC.

DESIGN REQUIREMENTS

- 1. Design an ID for decoding all of the opcodes in the TRISC instruction set. Find a realization that minimizes the number of integrated circuits needed to implement. You may also use Verilog.
- Design a controller for generating the sequence of control signals necessary to fetch and execute the INC and CLR instructions. Minimize the number of integrated circuits in your design by using a minimum number of states and by considering various types of combinational logic components and flipflops. You may also use Verilog.



LAB ASSIGNMENT

- 1. Design, implement, document, and test your ID. Use DE1 slide switches to simulate the IR. Display your decoder outputs on DE1 LEDs. Your documentation must clearly show I/O assignments.
- 2. Design, implement, document, and test your Controller. Again use DE1 slide switches to simulate the IR. Use a DE1 pushbutton switch for the clock input. Display your controller outputs on DE1 LEDs. Your documentation must clearly show I/O assignments.
- Integrate and test your ID and controller.