DDCO LAB MCQ

1. Turn off delay means, gate output transition to
    a. 1
    b. 0
    c. Z
    d. X

ans: c (Z)

2. What does timescale 1 Ns/1 Ps mean?
    a. It means all delays are interpreted in nanoseconds, and fractions are rounded off to the nearest picosecond.
    b. It means all delays are interpreted in picoseconds, and fractions are rounded off to the nearest nanosecond.
    c. It means all delays are interpreted in nanoseconds and in picosecond.
    d. None of choices

ans: a

3. Between variable and signal, which will be updated first?
    a. The signal will be updated first
    b. The variable will be updated first
    c. Both will be updated
    d. None of the choices

ans: a

4. initial
    begin
    a = 0; c = 0;
    b = #5 a + c;
    end
    a. The above Verilog code is intra assignment delay
    b. The above Verilog code is inter assignment delay
    c. The above Verilog code is both intra and inter assignment delay
    d. None of the choices

ans: a

5. What's the keyword in Verilog testbenches to indicate that interrupts the simulation with the possibility of resuming it?
    a. $finish
    b. $monitor
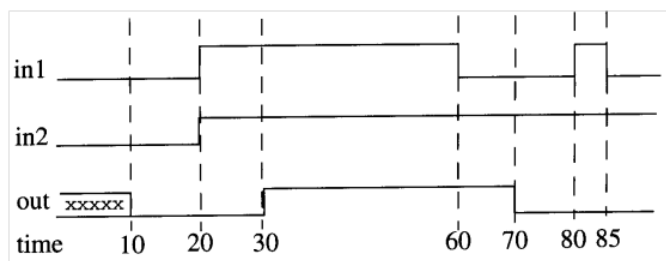   c. $stop
    d. $fish
    e. None of the above
    ans: c

6.   In Verilog `h1234 is a
   a.   16 bit hexadecimal number
   b.   32 bit hexadecimal number
   c.   4 bit hexadecimal number
   d.   Invalid notation

ans: b
7.   <= is used in
   a.   Blocking
   b.   Non Blocking
   c.   Both
   d.   None of the choices

ans: b
8.   What could be the expression for below figure where in1 and in2 are input reg variables and out is output variable of wire type

   a.   assign out = in1&in2
   b.   assign #10 out = in1&in2
   c.   assign #30 out = in1&in2
   d.   assign #40 out = in1&in2

ans: d
9.   What would be simulation time in below code when rval=10

```
`timescale 1 ns / 1 ps
module timescale_check2;
reg[31:0] rval;
initial begin
      rval = 20;
#10.566601 rval = 10;
end
initial begin
$monitor("TimeScale 1ns/1ps : Time=%0t,  rval = %d",$realtime,rval);
#100 ;
end
endmodule
```

   a.   0
   b.   10566
   c.   1056
   d.   None of the choices

ans: b

10.　　The phenomenon of clock skew is found in _____.

   a. Asynchronous circuit

   b. Synchronous circuit

   c. Both

ans: b