
Altera's MAX 10 FPGA's

It's time to rethink what an FPGA is

Designing with
the DECA Evaluation Board



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Texas
INSTRUMENTS

V | Five Years Out

Agenda

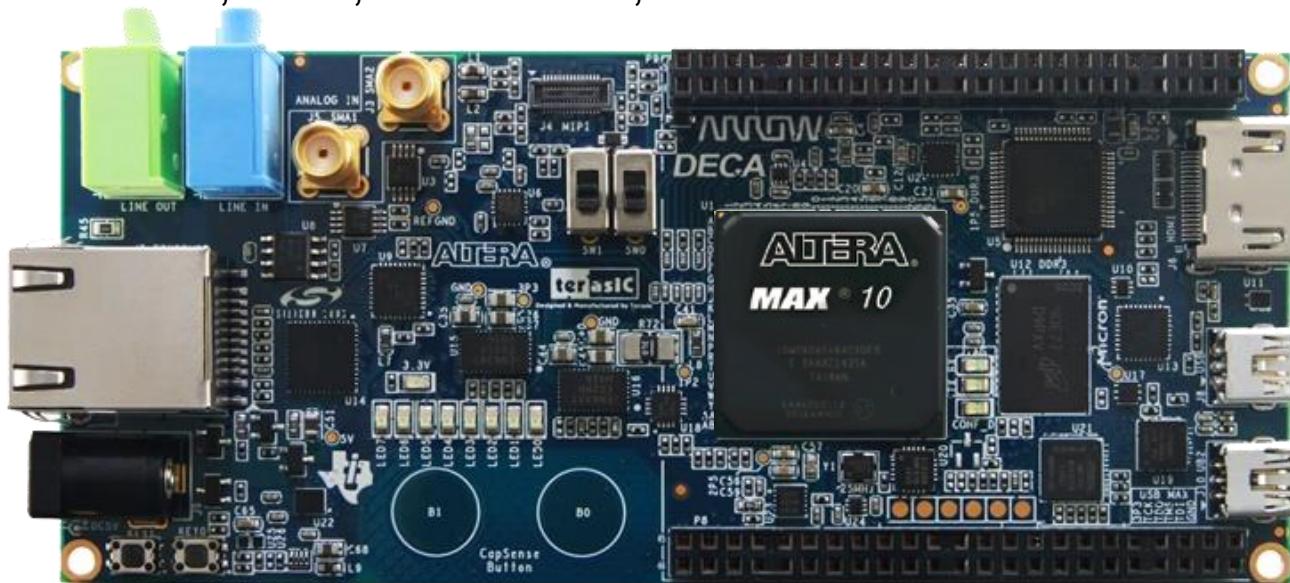
- What is DECA?
- MAX 10 Overview
- MAX 10 Architectural Details
- Getting to know your DECA development kit
- Silicon and IP Partner Solutions
- Lab Overview



What is DECA

- MAX 10 evaluation board designed to highlight the advantages of using MAX 10
 - ADC's: Two 12-bit, 8-channel, 1Msps
 - On-chip flash: dual configuration + user flash
 - Design Security (128-bit AES encryption)
 - Internal oscillator
 - Traditional FPGA resources
 - PLLs, RAM, DSP Blocks, LVDS I/O

Powered by



Interact with DECA

■ Sensors:

- Gesture, Proximity, and Ambient Light
- Humidity and Temperature
- Power Monitor
- Accelerometer

■ Interfaces:

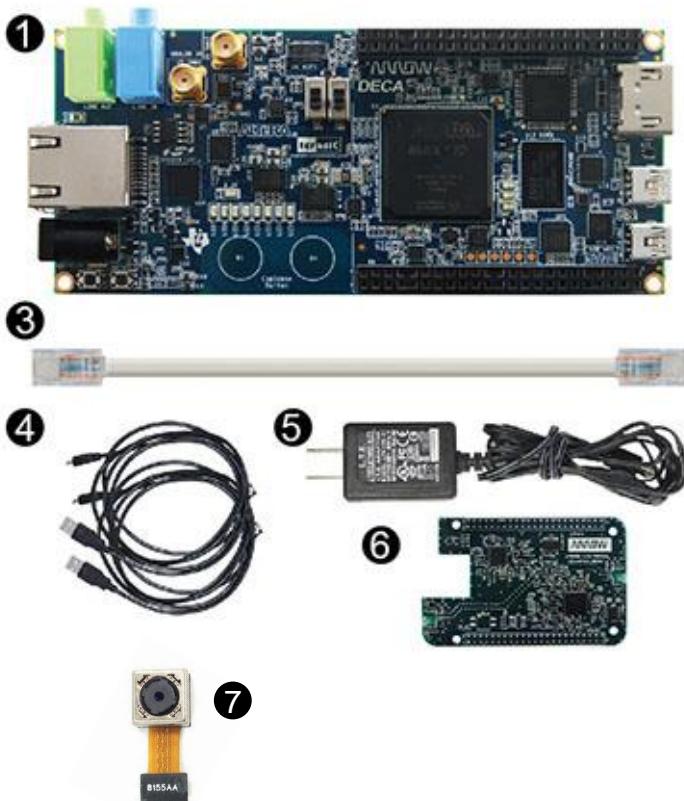
- Ethernet
- USB2.0 OTG
- SD/MMC
- HDMI
- MIPI CSI-2 interface
- CapSense Mechanical Button Replacement (MBR)



- Audio CODEC (Line In / Line Out)
- BeagleBone Compatible I/O expansion header
- Supporting the BLE / Wi-Fi combo Card

DECA – Workshop in a box!

■ Kit Contents include:



- ① DECA Board
- ② DECA Quick Start Guide
- ③ Ethernet Cat 5e Cable
- ④ Type A to Mini-B USB Cable x2
- ⑤ Power DC Adapter
- ⑥ BLE-WIFI Module
- ⑦ Camera Module

Altera MAX 10 FPGA Overview

Revolutionizing Non-Volatile
Integration!



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Innovation Leader Across the Board



FPGAs and CPLDs
Low Cost,
Non-volatile

FPGAs
Cost/Power Balance
SoC & Transceivers

FPGAs
Mid-range FPGAs
SoC & Transceivers

FPGAs
Optimized for
High Bandwidth

PowerSoCs
High-efficiency
Power Management

RESOURCES

Embedded Soft and Hard Processors

Nios II

ARM

Design Software



QUARTUS^{II}

DSP Builder

Development Kits



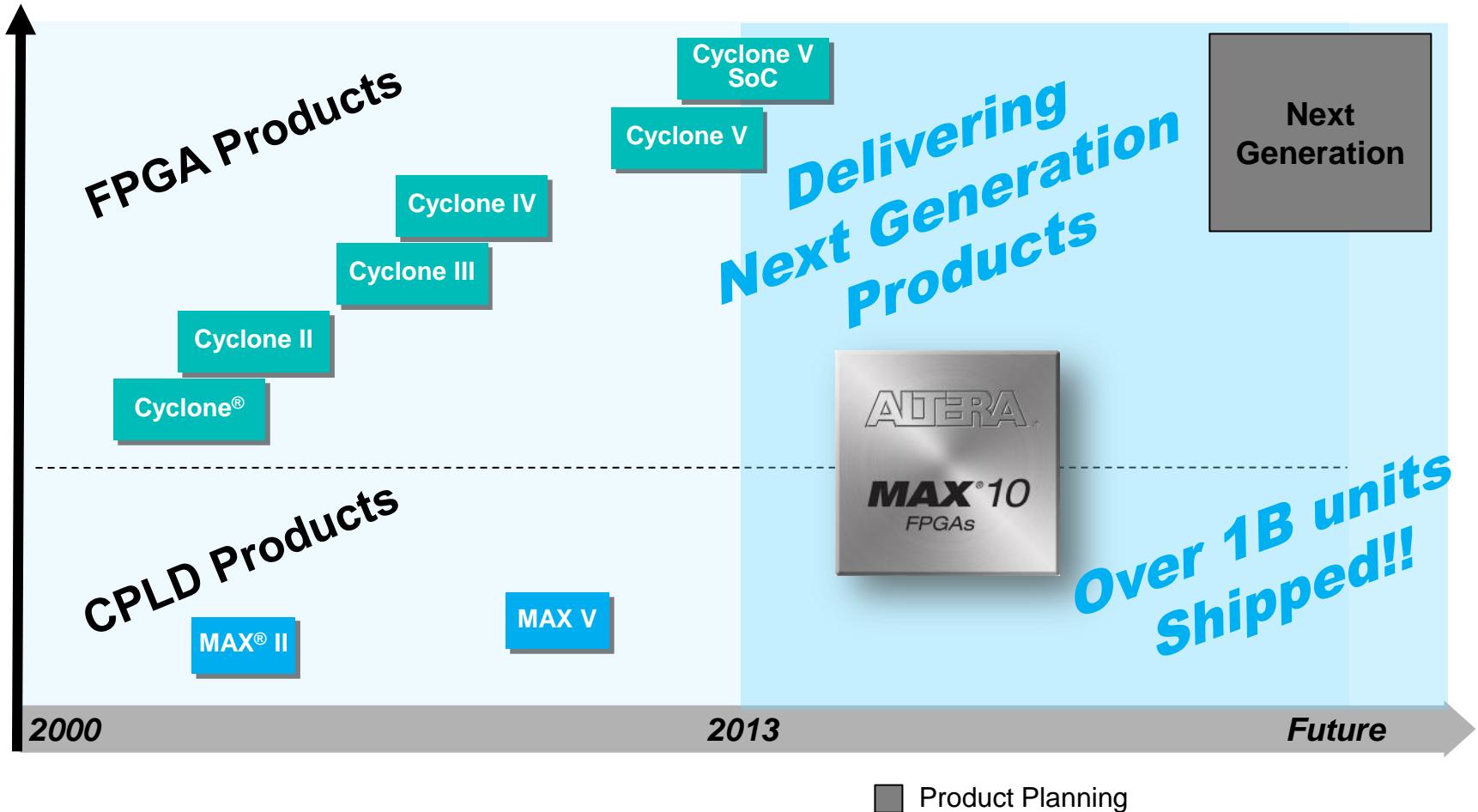
Intellectual Property (IP)

- Industrial
- Computing
- Enterprise



Low Cost Families – Altera Continues Focus & Investment

More performance,
features, or density

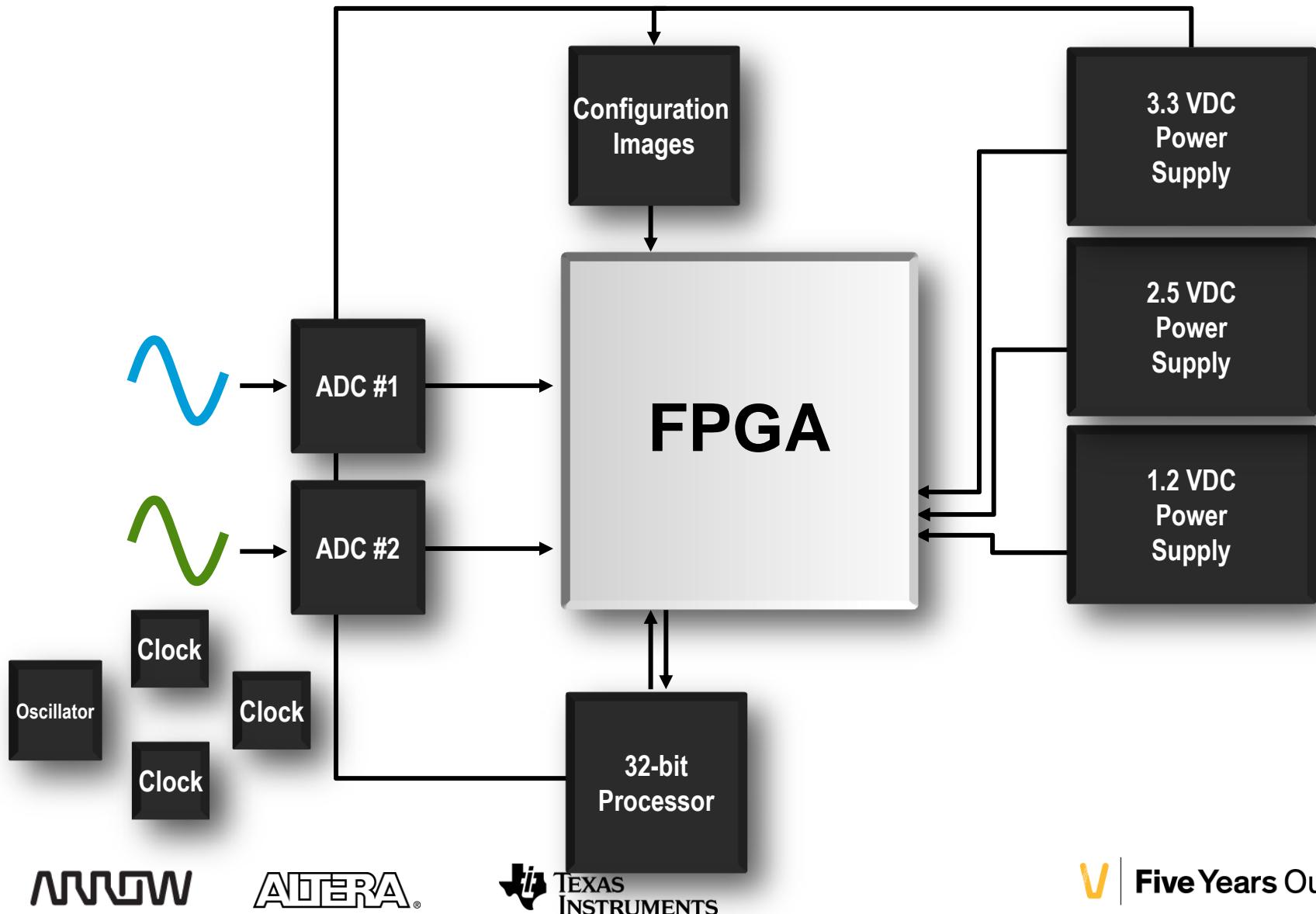


First Single-Chip FPGA to Combine...

- Non-volatile, instant-on capabilities
- Dual-configuration support
- Embedded processor support
- Integrated analog blocks
- Embedded RAM and DSP blocks
- DDR3 external memory interface

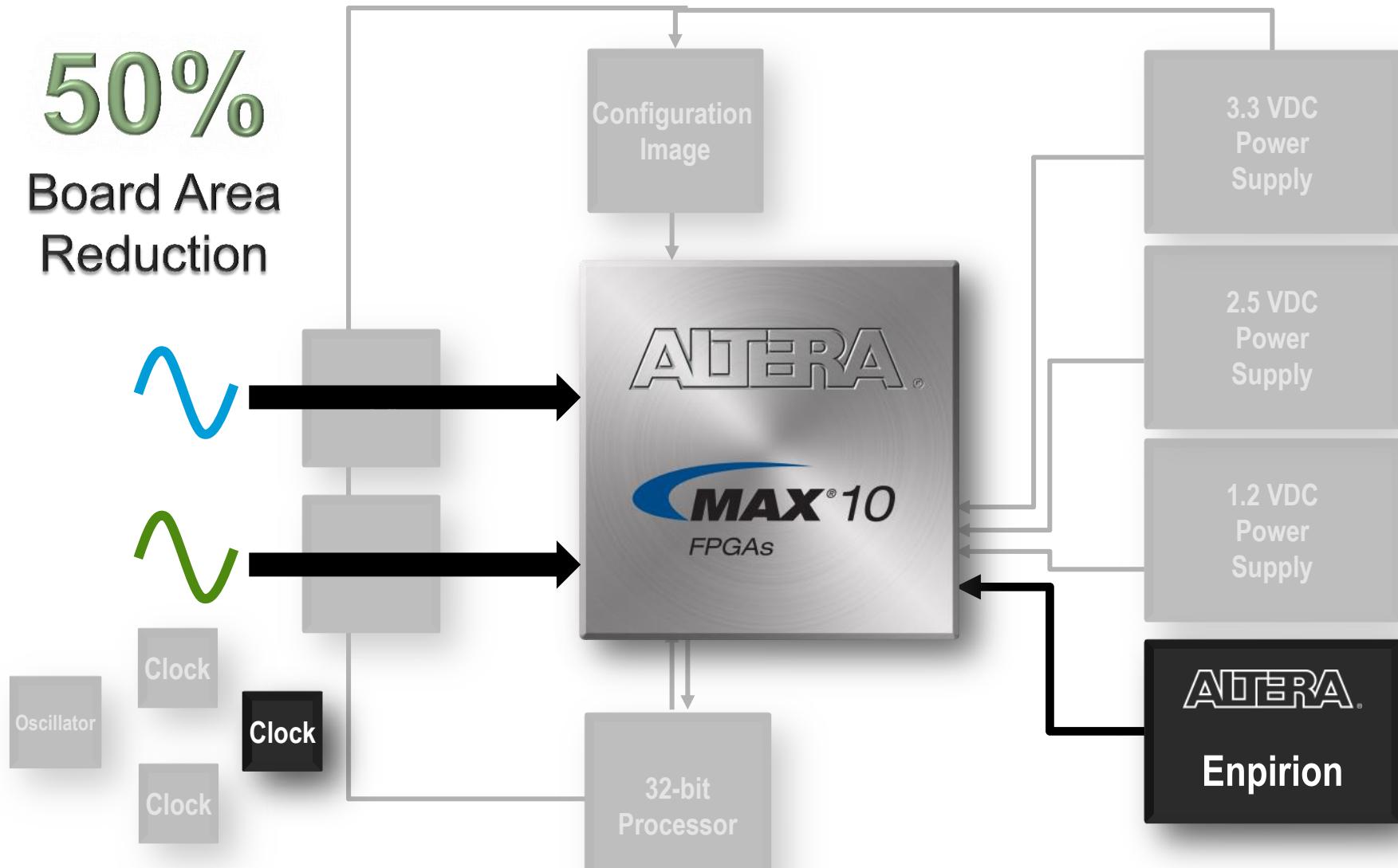


Traditional FPGA System Components

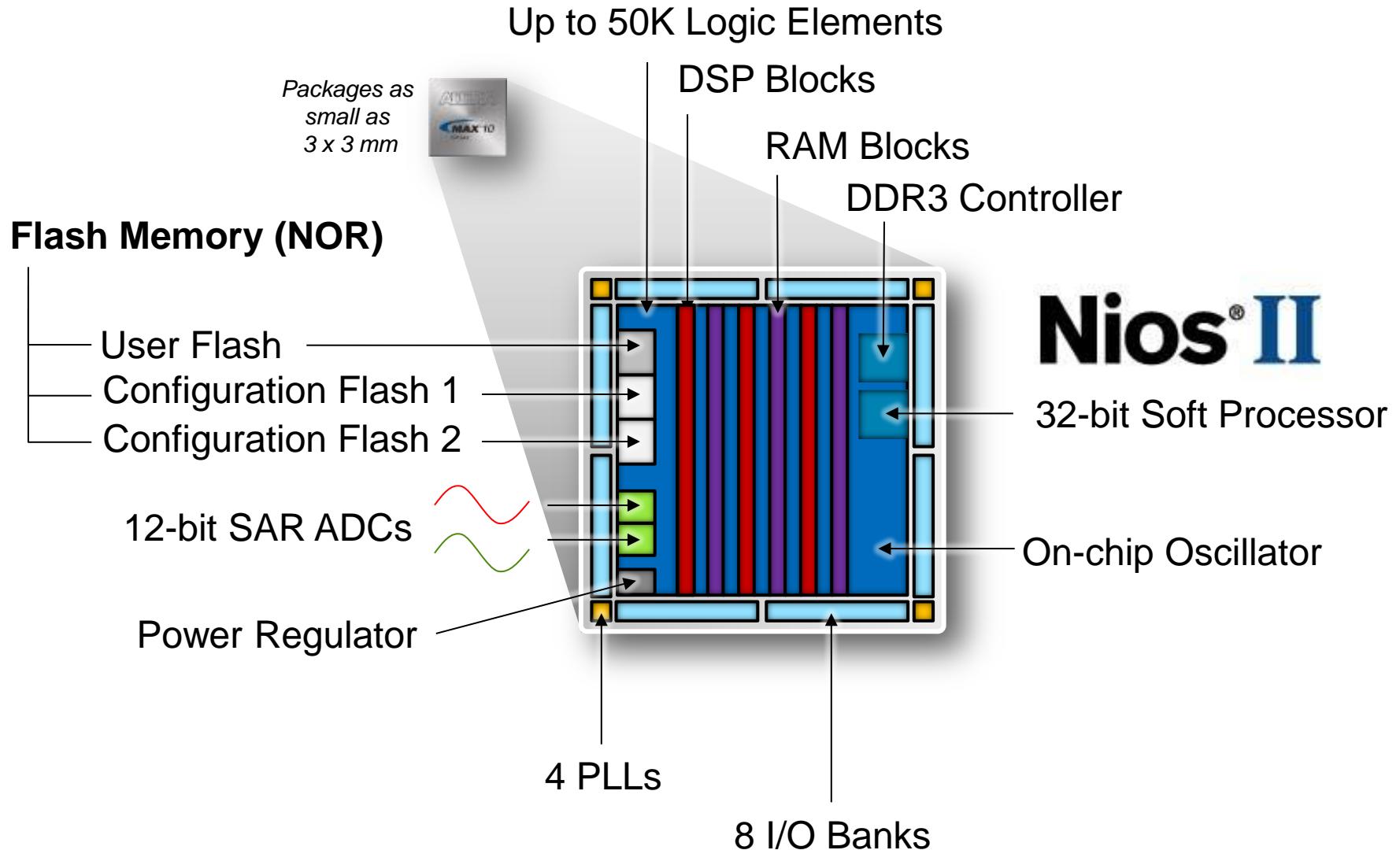


MAX 10 Simplifies Traditional FPGA Systems

50%
Board Area
Reduction



Lower BOM, Smaller PCB Area, Instant-on Configuration

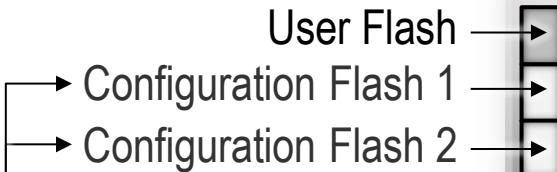


Integrated Embedded Flash

- Lower total cost of ownership
 - Reduced BOM
 - Smaller board area
- Reduced system risk
 - Fewer vendors to manage
 - Simpler PCB design
 - Supports long life cycles
- Fail-safe remote updates
 - Store two configuration images
- Improved system management
 - Instant-on configuration
 - Power-up sequencing



Flash Memory (NOR):



SPI and I2C soft interfaces supported in Quartus® II

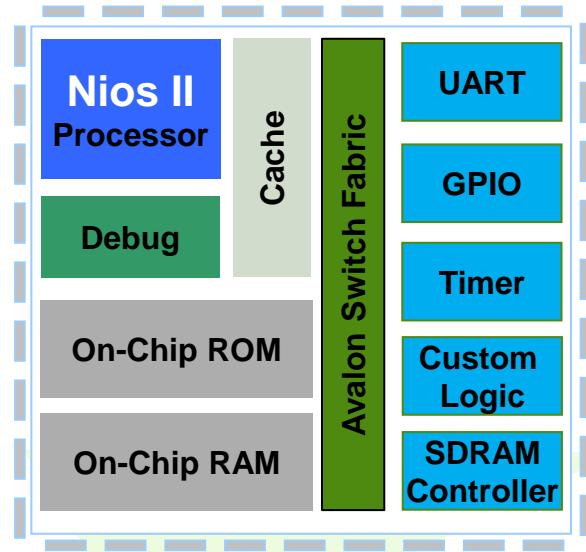
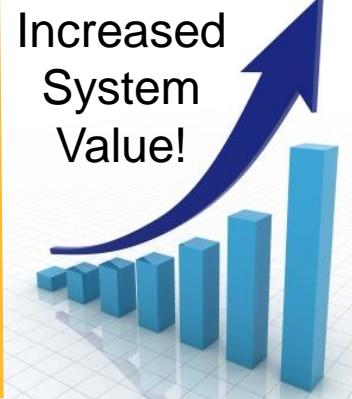


QUARTUS® II



Embedded Processing

- Single-chip embedded processor system
 - Soft core Nios II processor support
 - Very small footprint
 - No external RAM or storage needed
- User-customizable processor
 - Flexibility MCUs don't offer
- Supports real-time applications
 - Configuration in under 10 ms
 - Meets automotive and industrial regulatory requirements
- Supports longer life cycles



Customizable logic

Nios® II

Integrated Analog Blocks

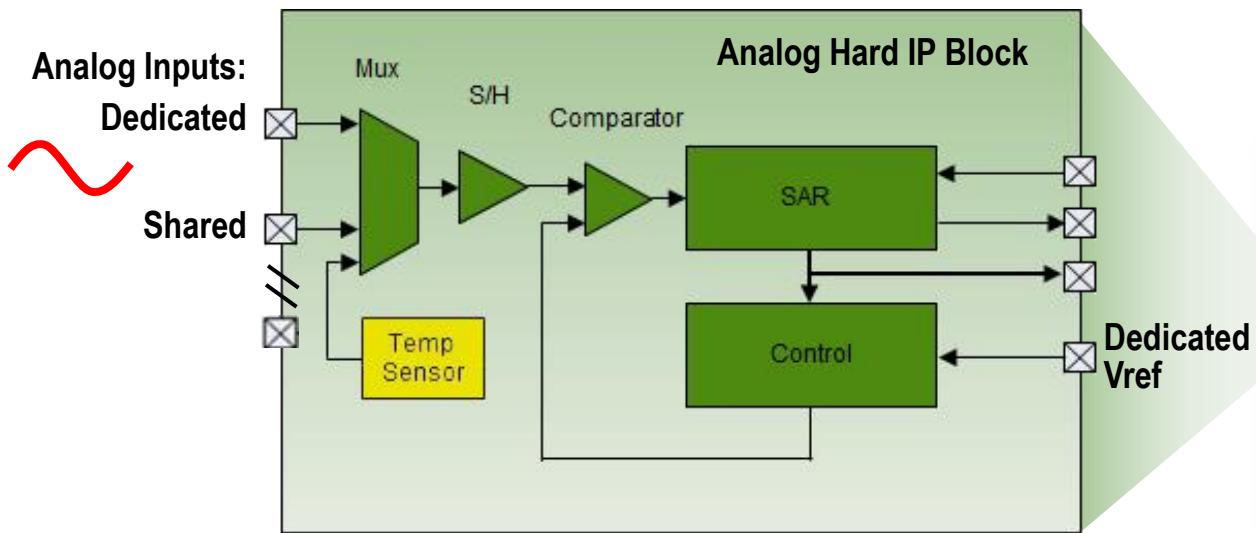


■ In-chip system monitoring

- Integrated ADCs
- Reduce board space
- Flexible sample sequencing
- Lower latency

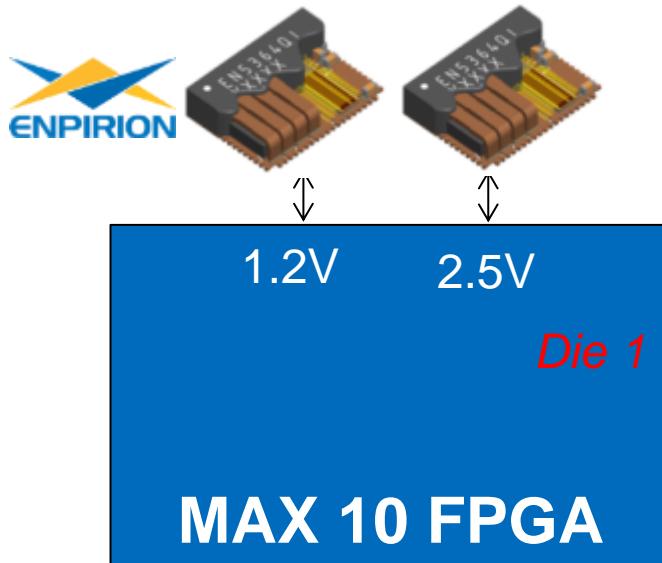
■ Measure environmental conditions

- Integrated temperature sensor

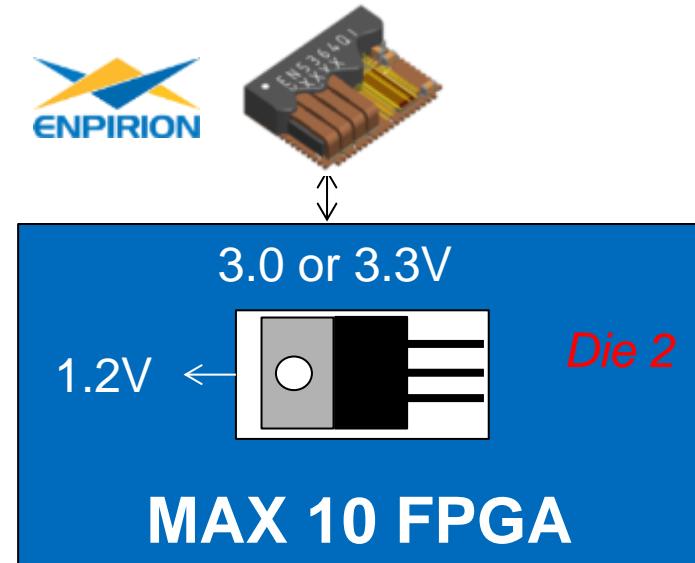


Optional Integrated Linear Regulator

Dual Supply Option



Single Supply Option

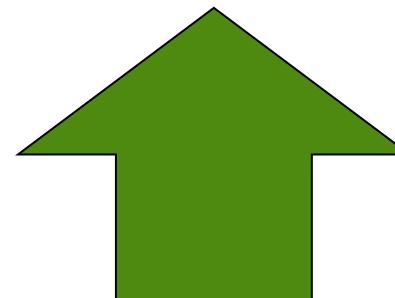
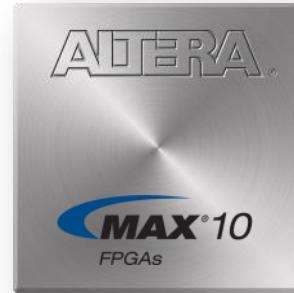
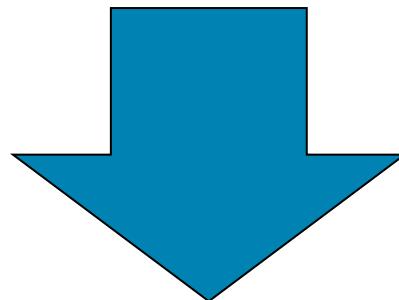


- Higher Performance
- More Features
- Higher Power Efficiency

- Simple, compact PCB
- Lower BOM cost

MAX 10 FPGA Customer Benefits

Single-chip advantage	Customer Benefits
Multiple-components → 1 component	Higher system reliability (less failure points) Reduced BOM/System Cost
Reduced PCB Footprint	Simpler PCB Design Fewer PCB layers → Lower PCB cost
Fewer Suppliers	Less vendors to manage
PLD have Longer Life-cycles	Avoids EOL vs other technologies



MAX 10 FPGA – Family Plan

Device	LEs	Block Memory (Kb)	User Flash ¹ (KB)	18x18 Mults	PLLs	Internal Config.	ADC, TSD	External RAM I/F
10M02	2,000	108	12	16	1, 2	Single	-	Yes ²
10M04	4,000	189	16 – 156	19	1, 2	Dual	1, 1	Yes ²
10M08	8,000	378	32 – 172	24	1, 2	Dual	1, 1	Yes ²
10M16	16,000	549	32 – 296	45	1, 4	Dual	1, 1	Yes ³
10M25	25,000	756	32 – 400	61	1, 4	Dual	2, 1	Yes ³
10M40	40,000	1,260	64 – 736	125	1, 4	Dual	2, 1	Yes ³
10M50	50,000	1,638	64 - 736	144	1, 4	Dual	2, 1	Yes ³

Notes:

1. User Flash size depends on configuration options used.
2. SRAM only.
3. SRAM, DDR3, DDR2, or LPDDR2.
4. ADC blocks available on die but may not be available in low pin count packages.



MAX 10 FPGA – Package Plan and Available I/O

Product Line	36-WLCSP 3x3mm ² 0.4mm Pitch	81-WLCSP 4x4mm ² 0.4mm Pitch	256-BGA 17x17mm ² 1.0mm Pitch	324-BGA 15x15mm ² 0.8mm Pitch	484-BGA 23x23mm ² 1.0mm Pitch	672-BGA 27x27mm ² 1.0mm Pitch
10M02 "D"	C (27)	-	-	C (160)	-	-
10M04 "D"	-	-	C/F/A (178)	C/F/A (246)	-	-
10M08 "D"	-	C/F (56)	C/F/A (178)	C/F/A (246)	C/F/A (250)	-
10M16 "D"	-	-	C/F/A (178)	C/F/A (246)	C/F/A (320)	-
10M25 "D"	-	-	C/F/A (178)	-	C/F/A (360)	-
10M40 "D"	-	-	C/F/A (178)	-	C/F/A (360)	C/F/A (500)
10M50 "D"	-	-	C/F/A (178)	-	C/F/A (360)	C/F/A (500)

Notes:

1 - "Easy PCB" utilizes 0.8mm PCB design rules

2 - A subset of p/n's available in Automotive grade.



= Denotes pin-out migration capable

C: Compact, F: Flash, A: Analog

Product Line	144-EQFP 22x22 mm ² 0.5 mm Pitch	153-BGA 8x8mm ² 0.5mm Pitch ⁽¹⁾	169-BGA 11x11mm ² 0.8mm Pitch
10M02 "S"	C (101)	C (112)	C (130)
10M04 "S"	C/F/A (101)	C/F/A (112)	C/F/A (130)
10M08 "S"	C/F/A (101)	C/F/A (112)	C/F/A (130)
10M16 "S"	C/F/A (101)	-	C/F/A (130)
10M25 "S"	C/F/A (101)	-	-
10M40 "S"	C/F/A (101)	-	-
10M50 "S"	C/F/A (101)	-	-



MAX 10 FPGA

Architectural Details



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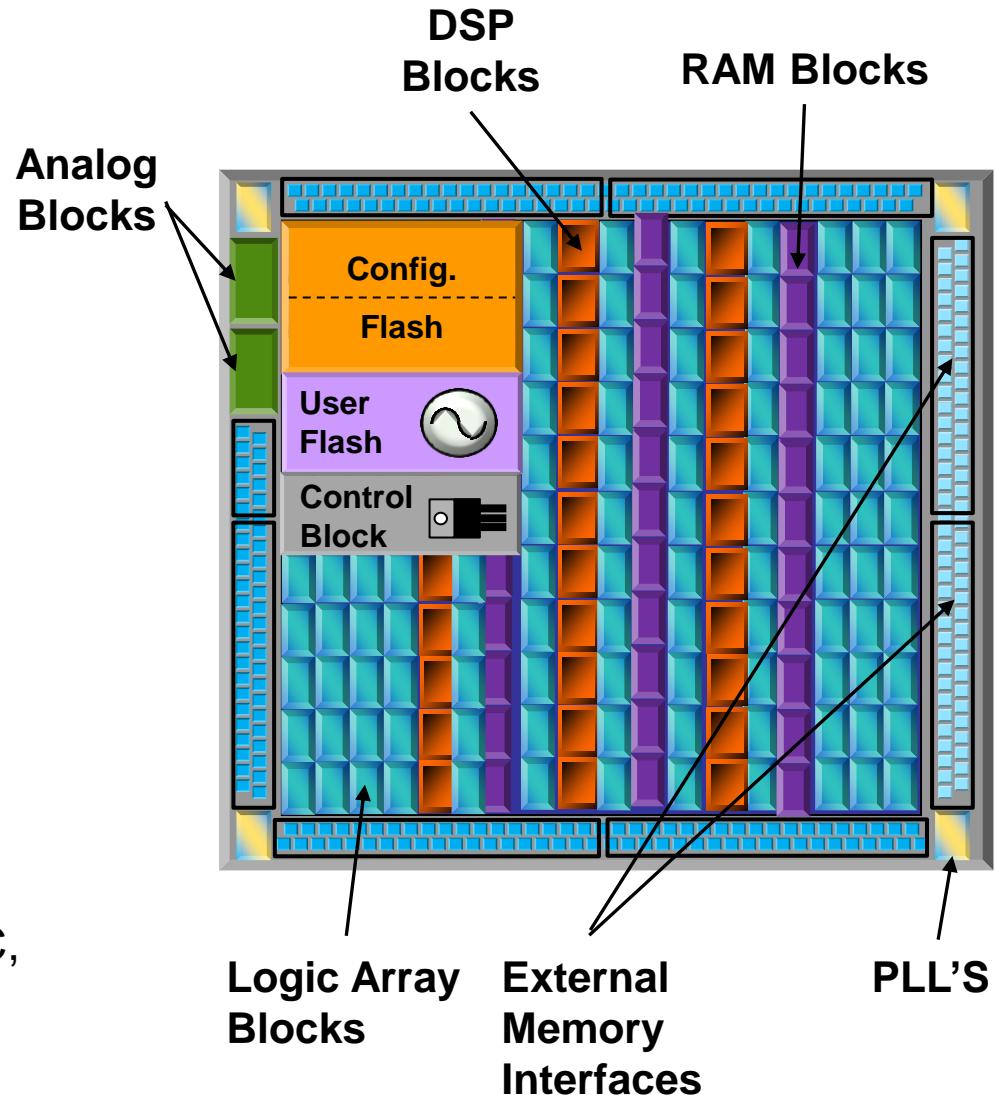
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Main Architecture

■ Consisting of:

- Logic array
- On-chip RAM & FLASH
- DSP blocks
- Up to two analog blocks
- Up to eight I/O banks
- Up to four PLL's
- Oscillator & Clocks
- Soft IP functionality
 - Nios® II 32-bit processor, Ethernet MAC, PCIe MAC, Video IP Suite, etc.



MAX 10 Building Blocks

Logic Array, Memories, and
Multipliers



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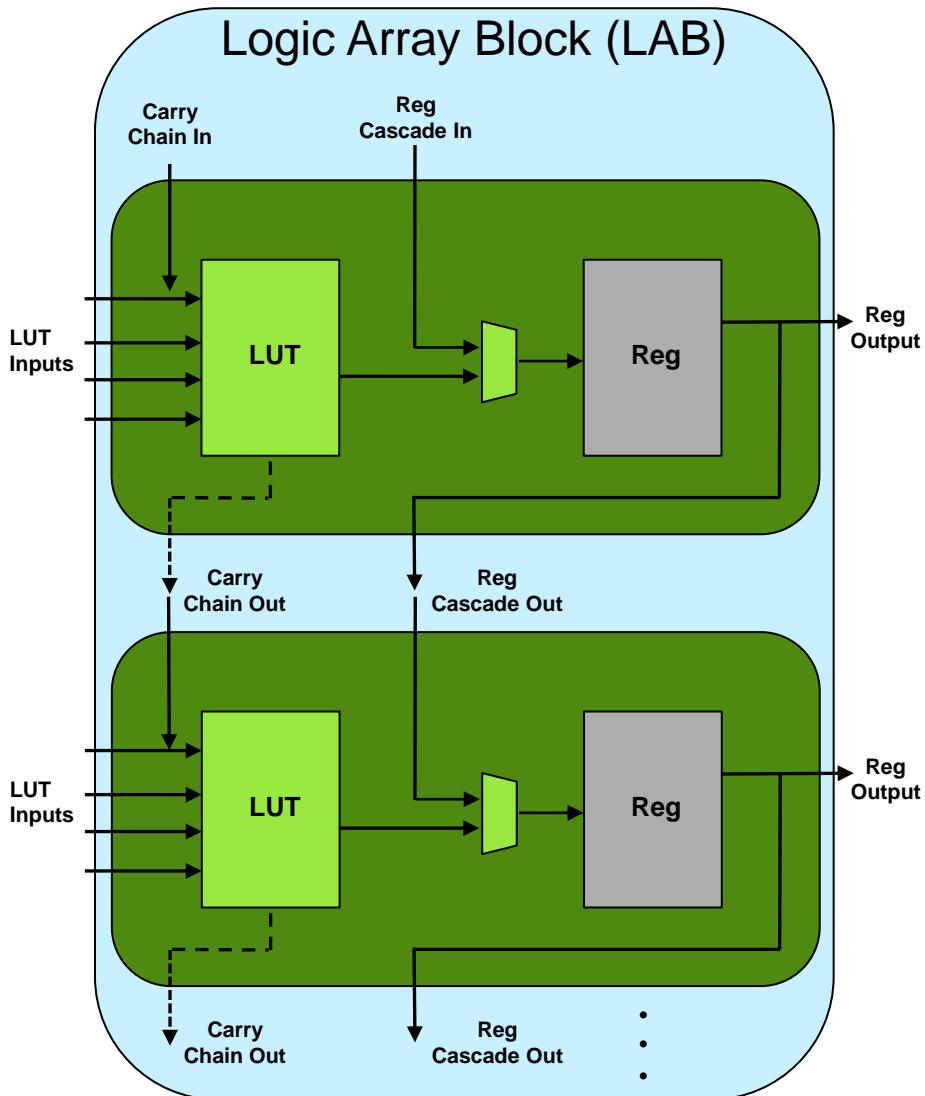
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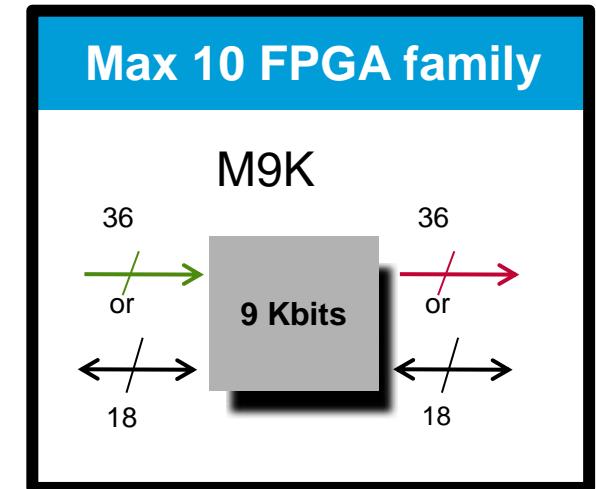
Logic Array, Basic Building Block

- Logic Element (LE)
 - 4-input Look Up Table (LUT) + Register
- Two dedicated paths between LEs:
 - Carry chain
 - Register Cascade
- Logic Array Block (LAB)
 - Consists of 16 LE's



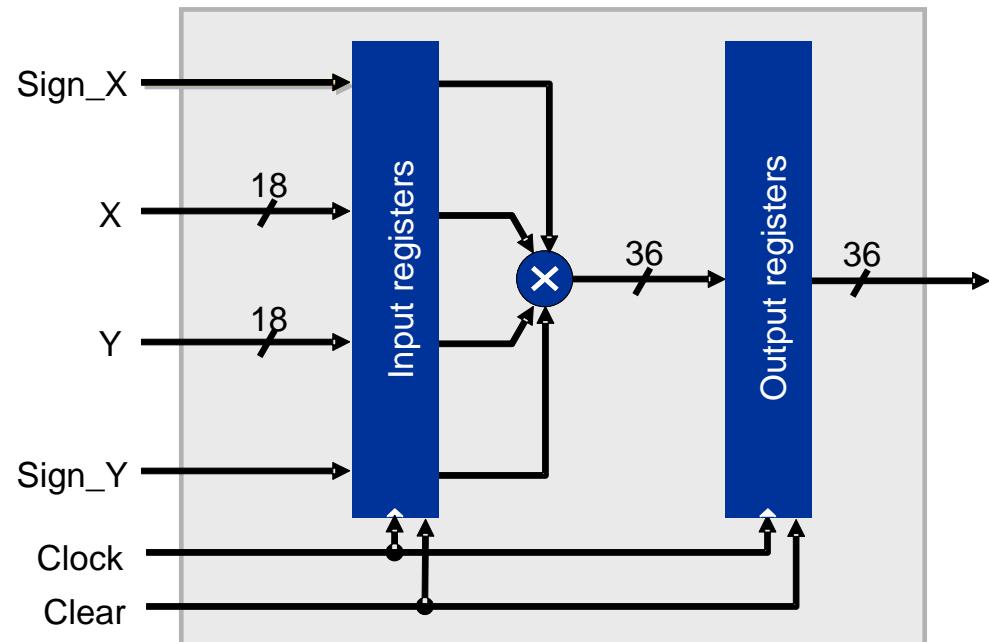
Block Memory (M9K)

Feature	M9K	Benefit
Block Size	9 Kbits	Optimizes Memory
Performance	Up to 315 MHz	Hi speed Performance
Dual-Port Read During Write Behavior	New Data or Old Data	Flexibility and Ease of Use
Parity Bit	Yes	Usability for High Reliability Apps
Clock Enables	4	Increased Flexibility and Reduced Power
Read and Write Enables	4	Increased Flexibility and Reduced Power



DSP Block Architecture

- 41 inputs (max.)
 - 36 data inputs
 - 5 control signal inputs
- 36 outputs (max.)
- Two modes of operation:
 - One 18x18 Multiplier
 - Two 9x9 Multipliers



MAX 10 FPGA Supply Variant	Speed Grade		
	-6	-7	-8
MAX 10D - Dual Supply	234 MHz	212 MHz	180 MHz
MAX 10S - Single Supply	198 MHz	183 MHz	160 MHz

Note: performance numbers per speed grade all assume registered inputs and outputs

MAX 10 Building Blocks

PLL's and Clocking



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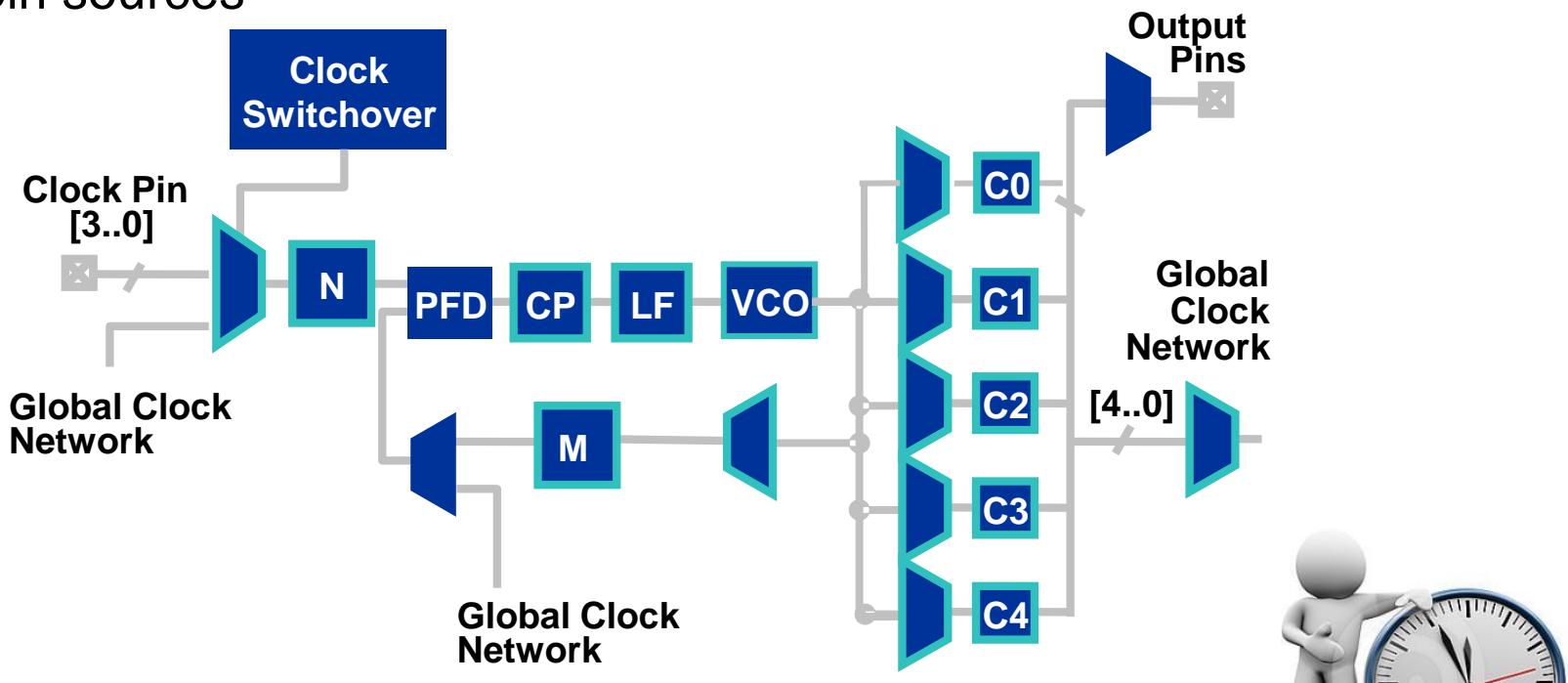
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Full Featured PLLs (Phase Locked Loop)

- MAX 10 FPGAs include up to 4 PLLs
 - Full featured capabilities
 - Enhanced to include Single PLL power supply option & 4 clock pin sources



Dynamically reconfigurable in user mode

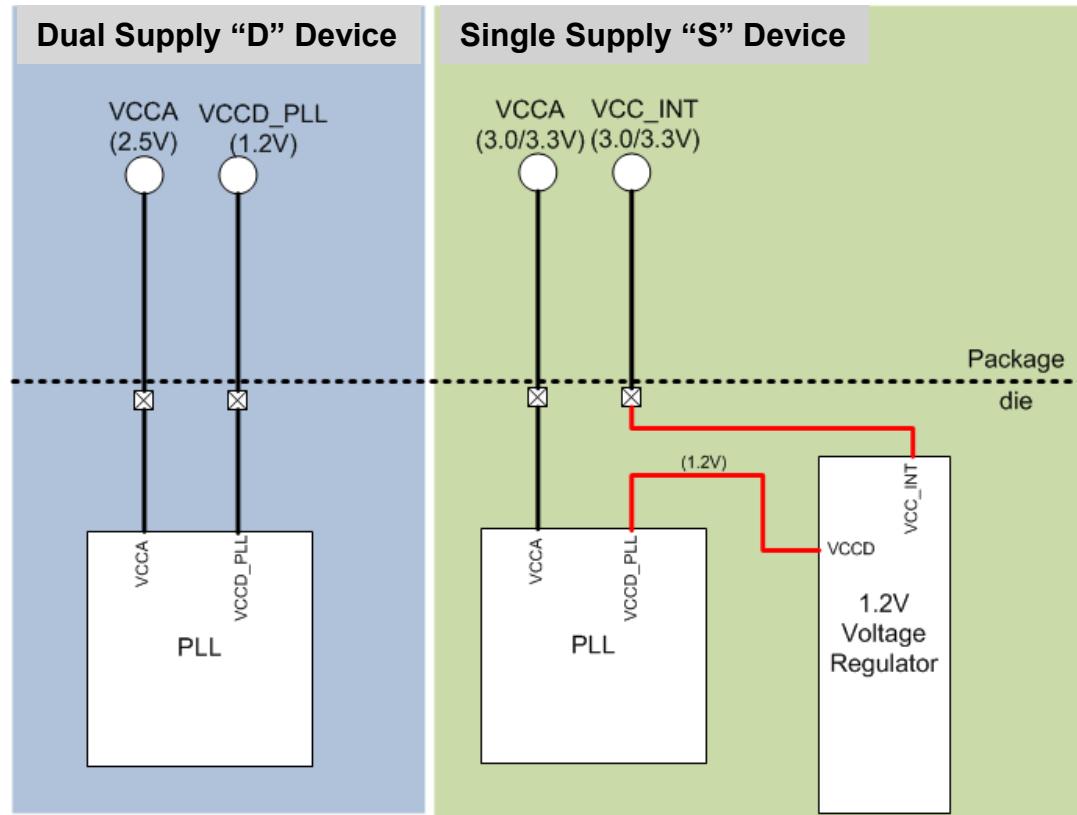
Density and Package PLL Support

- 4 PLLs supported in >=256 pin packages in 10M16 & larger
- 2 PLLs supported in >=256 pin packages in 10M08 & smaller
- 1 PLL supported in <=169 pin packages

Type	36-WLCSP	81-WLCSP	144-EQFP	153-MBGA	169-UBGA	256-FBGA	324-UBGA	484-FBGA	672-FBGA
Size	3 x 3 mm ²	4 x 4 mm ²	16 x 16 mm ²	8 x 8 mm ²	11 x 11 mm ²	17 x 17 mm ²	15 x 15 mm ²	23 x 23 mm ²	27 x 27 mm ²
Ball Pitch	0.4 mm	0.4 mm	0.4 mm	0.5 mm “Easy PCB”	0.8 mm	1.0 mm	0.8 mm	1.0 mm	1.0 mm
10M02	1	-	1	1	1	-	2	-	-
10M04	-	-	1	1	1	2	2	-	-
10M08	-	1	1	1	1	2	2	2	-
10M16	-	-	1	-	1	4	4	4	-
10M25	-	-	1	-	-	4	-	4	-
10M40	-	-	1	-	-	4	-	4	4
10M50	-	-	1	-	-	4	-	4	4

MAX 10 FPGA Single PLL Supply Support

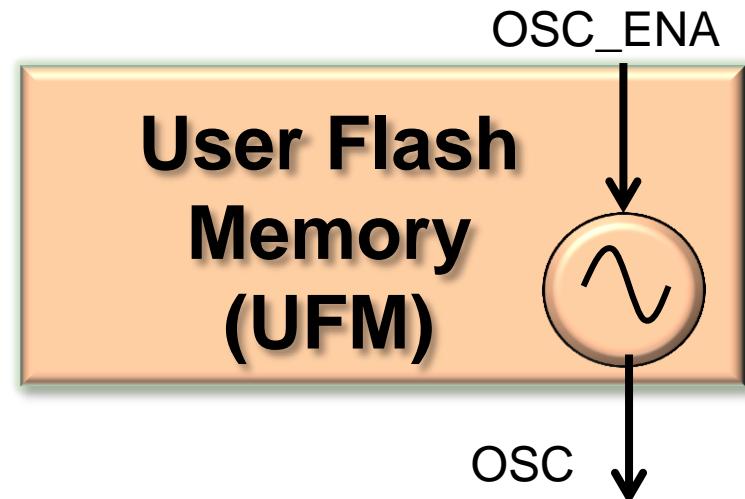
- Single supply devices support one 3.0/3.3V source for core and all PLL supplies



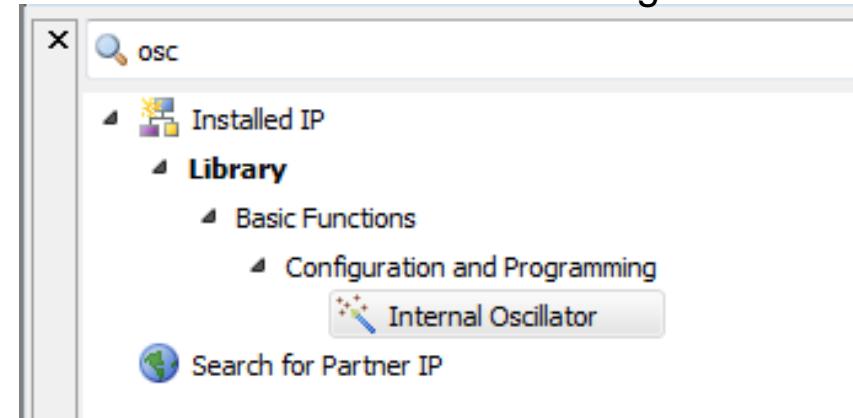
Internal Oscillator - Clock Source

- Uninterruptable clock source
- Ring Oscillator
- Great for self-running circuits:
 - Watchdog Timer
 - Sleep mode controller
- Located inside the UFM; accessible by the core fabric

Device	Operating Freq
10M02 – 10M25	55 – 116 MHz
10M40 – 10M50	35 – 77 MHz



Available from the IP Catalog



Low Power Clock Network

- Low power...when needed

- Dynamic enable/disable for power control/sleep
 - Unused networks automatically powered down

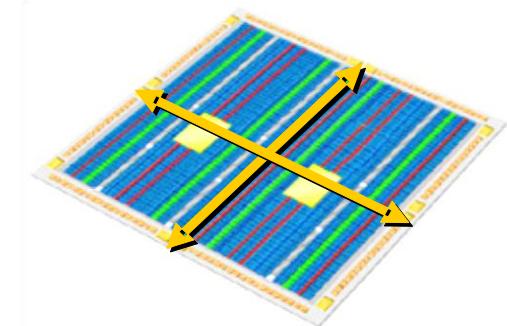


- High performance

- Up to 450MHz

- Abundant, flexible clocking resources

- Up to 20 global clock networks with dynamic user clock selection
 - Oscillator for Self-running applications - sleep controller, watch-dogs, etc.

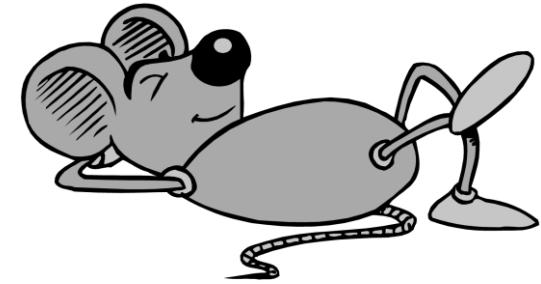


***Robust clocking resources
to support system integration***

Sleep Mode Capabilities

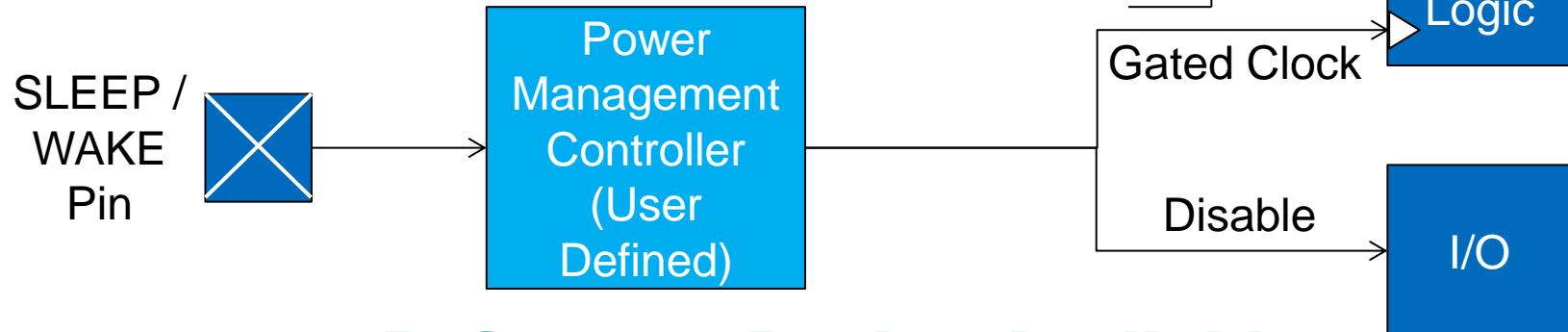
■ New Power saving feature

- Low power mode without losing state
- External control via single pin
- Wake-up from sleep in < 1 ms
- Gates clocks to internal logic
- Disables I/O



■ Significant Dynamic Power Reduction

- up to 95%



Reference Design Available

MAX 10 Building Blocks

Analog to Digital Converter



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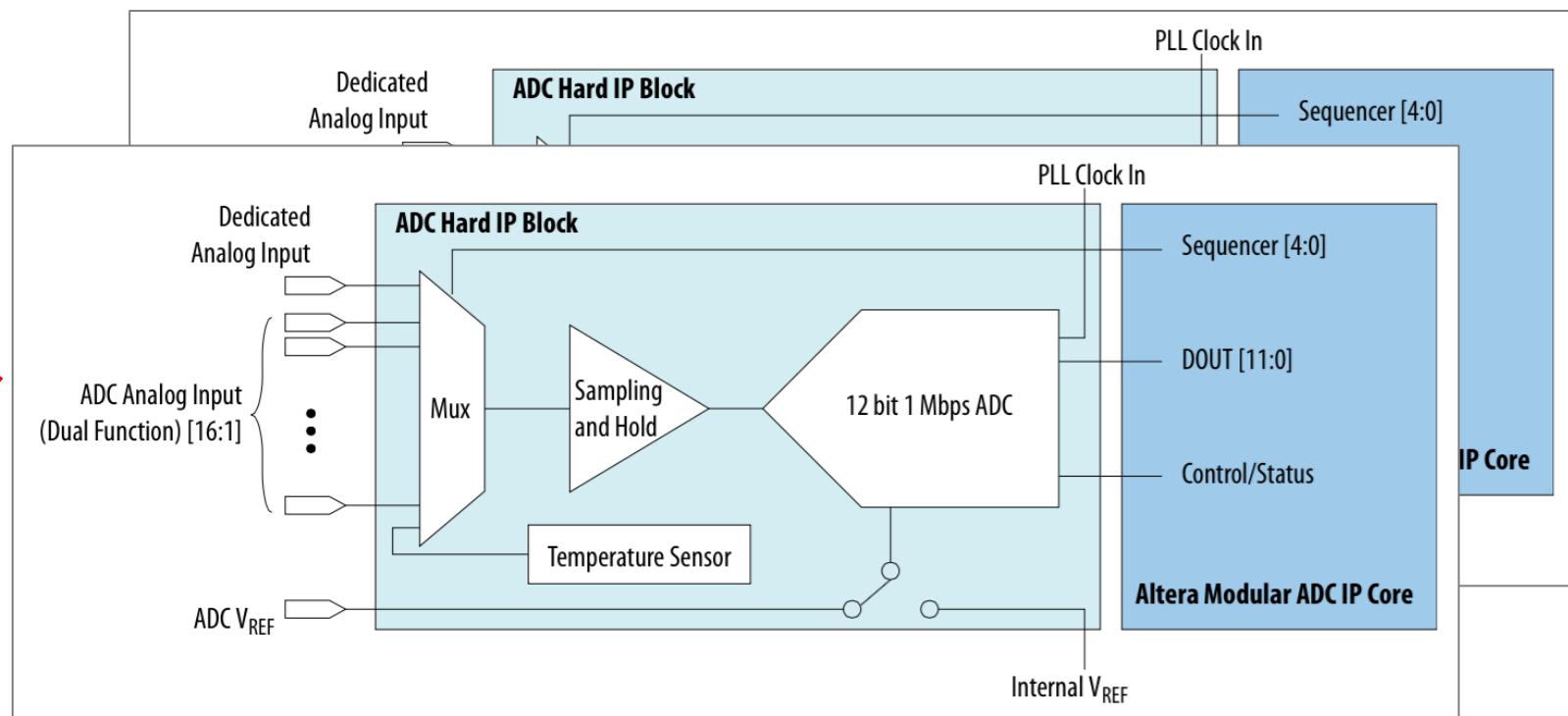
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ADC's - Analog Hard IP Block

■ Up to two, 12-bit SAR ADCs

- 1 Msps (each ADC)
- 18 Analog inputs (Max.)
- 1 Temperature Sensing Diode
 - Samples @ 50Ksps
- Two dedicated inputs
- Selectable Voltage Prescalers
- Selectable for temperature and Voltage measurements



ADC Channel Count vs. Package

■ ADC Channel GPIO count per device / package option

- Additional Dedicated Analog input per ADC block (not shown)
- Additional Temperature Sensing Diode only available on ADC1
- Only 8 channels can be migrated from 10M04 to 10M50 for ADC1
 - Denoted by: 

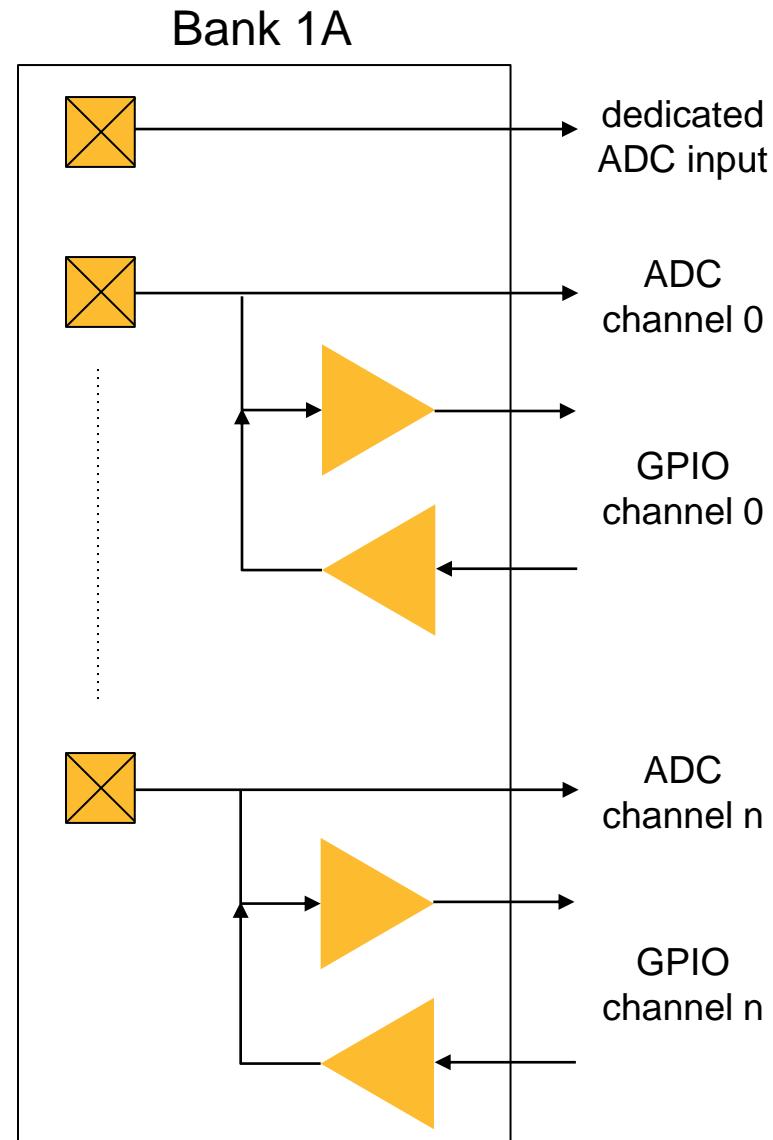
Package Details	Type	36-WLCSP	81-WLCSP	144-EQFP	153-MBGA	169-UBGA	256-FBGA	324-UBGA	484-FBGA	672-FBGA
	Voltage	Dual	Dual	Single	Single	Single	Dual	Dual	Dual	Dual
MAX 10 FPGA	10M04	-	-	8+0 	8+0 	8+0 	16+0 	16+0 	16+0 	-
	10M08	-	-	8+0 	8+0 	8+0 	16+0 	16+0 	16+0 	-
	10M16	-	-	8+0 	-	8+0 	16+0 	16+0 	16+0 	-
	10M25	-	-	8+0 	-	-	8+8 	-	8+8 	-
	10M40	-	-	8+0 	-	-	8+8 	-	8+8 	8+8 
	10M50	-	-	8+0 	-	-	8+8 	-	8+8 	8+8 

Note: ADC Channel Count = ADC1 + ADC2

DECA FPGA package

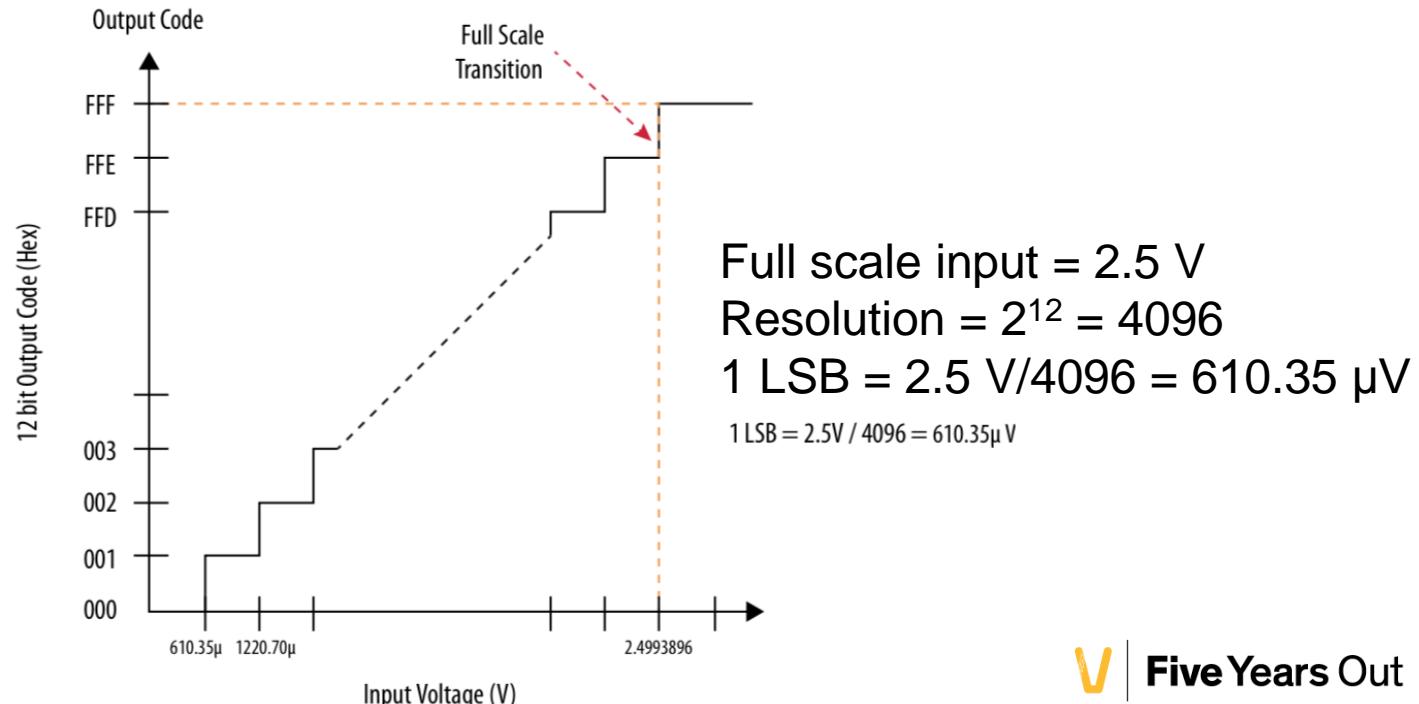
Analog Inputs

- Single ADC devices:
 - 1 dedicated analog input
 - 8 or 16 shared analog inputs
- Dual ADC devices:
 - 2 dedicated (1 per ADC)
 - 16 shared (8 per ADC)
- All inputs located in I/O bank 1A in upper left corner of device
- If ADC enabled, all GPIO buffers get tristated



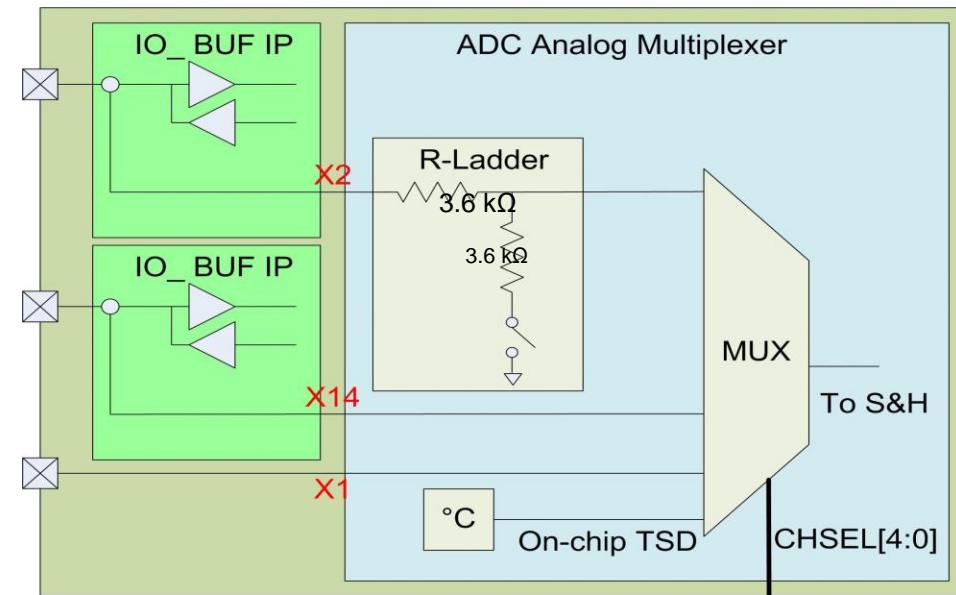
Voltage Conversion

- Dual supply devices: measure up to 2.5 V
- Single supply devices: measure up to 3.0 V or 3.3 V depending on supply voltage used
- Full scale voltage is actually full scale - 1 LSB
- 2.5 V full scale example:



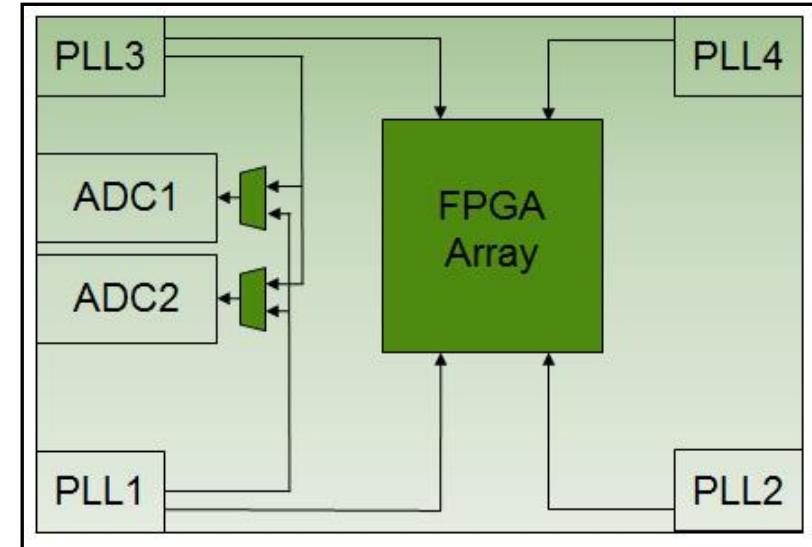
ADC Input Prescaler

- Divides analog input voltage by 2 (with an “R-ladder”)
- Increases maximum measurement range from 2.5 V to:
 - 3.0 V on dual power supply devices
 - 3.6 V on single power supply devices
- Output digital value requires adjustment if prescaler is used
- Available on channels 8 and 16 on single ADC devices
- Available on ADC1 channel 8 and ADC2 channel 16 in dual ADC devices



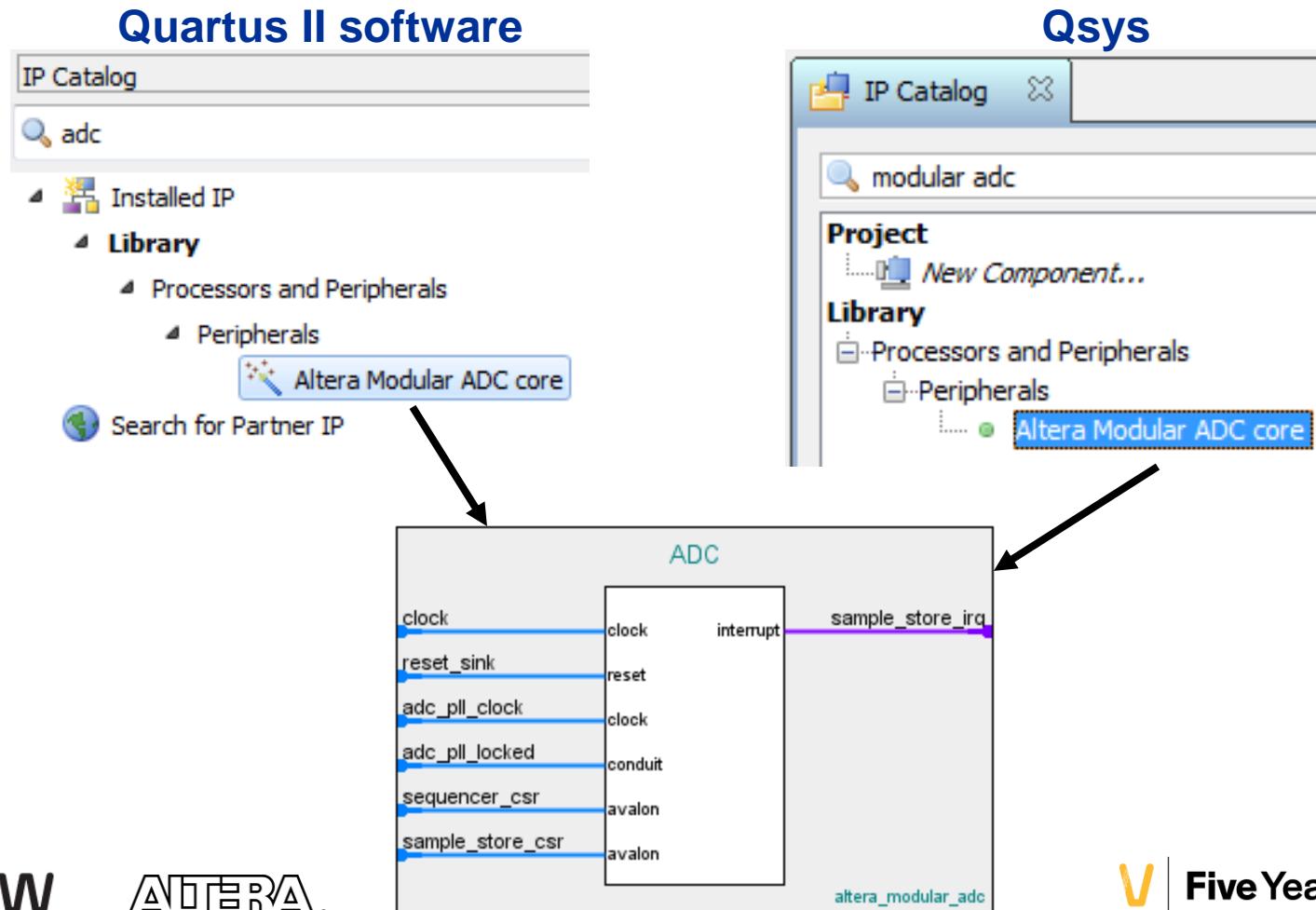
ADC Clocking

- ADC's support clocks from two PLLs
 - Top-left and bottom-left
- PLL will not be generated as part of the Megawizard
 - Designer will need to connect it
 - Restricted to PLL1 or PLL3
- Sample Frequency
 - Voltage: 1MHz
 - Temperature: 50 KHz
- Internal Clock Divide Block
 - Voltage – Divide 1, 2, 10, 20, 40, 80
 - Temperature – Divide 10, 20



Adding an ADC to a Design

- Available in **Peripherals** folder in IP Catalog in the Quartus® II software or in Qsys



ADC IP Parameter Editor

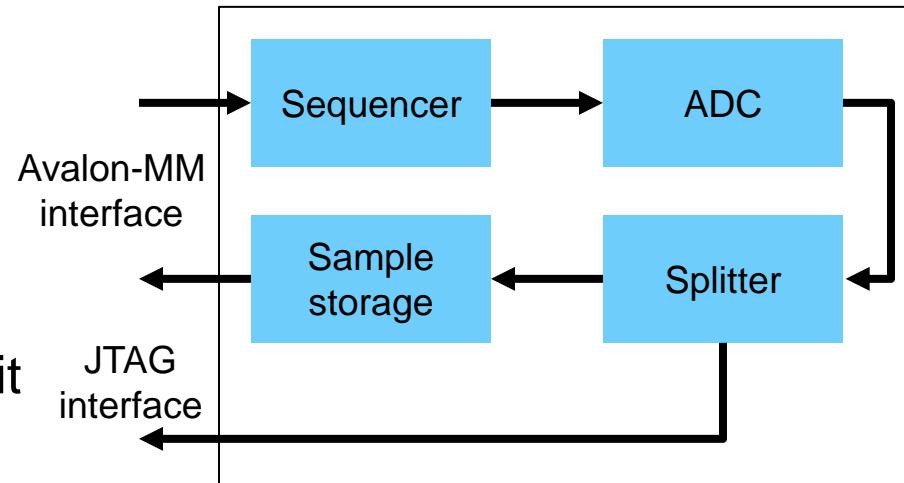
- Used to configure all options for single or dual ADC implementations

The screenshot shows the 'General' tab of the ADC IP Parameter Editor. It includes sections for 'Core Configuration', 'Clocks', and 'Reference Voltage'. In the 'Core Configuration' section, 'Core Variant' is set to 'Standard sequencer with Avalon-MM sample storage' and 'Debug Path' is set to 'Enabled'. Under 'Clocks', the 'ADC Input Clock' is set to '80 Mhz'. In the 'Reference Voltage' section, the 'Reference Voltage Source' is set to 'Internal' and the 'Internal Reference Voltage' is set to '2.5 V'. Below this, there are tabs for 'Channels' and 'Sequencer'. The 'Channels' tab is active, showing a row of buttons for channels CH0 through CH16 and TSD. Under 'Channel 8', the 'Use Channel 8' checkbox is checked. Under 'Channel 8 Prescaler', the 'Enable Prescaler for Channel 8' checkbox is unchecked.

Implementation and Operating Modes

■ Four main blocks

- Hard ADC
- Sequencer
- Sample storage
- Debug splitter for ADC Toolkit



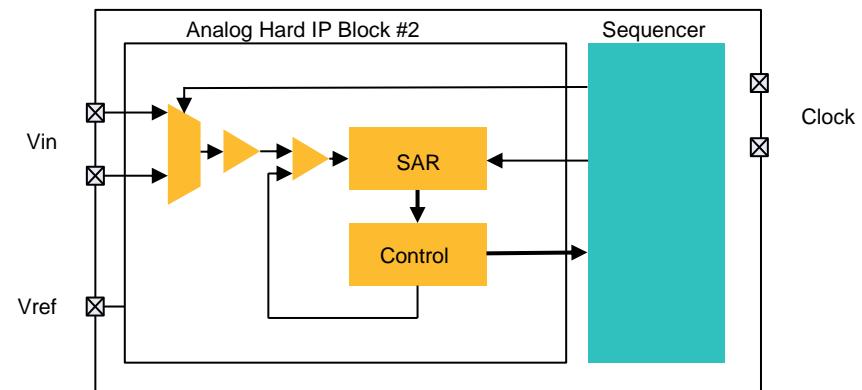
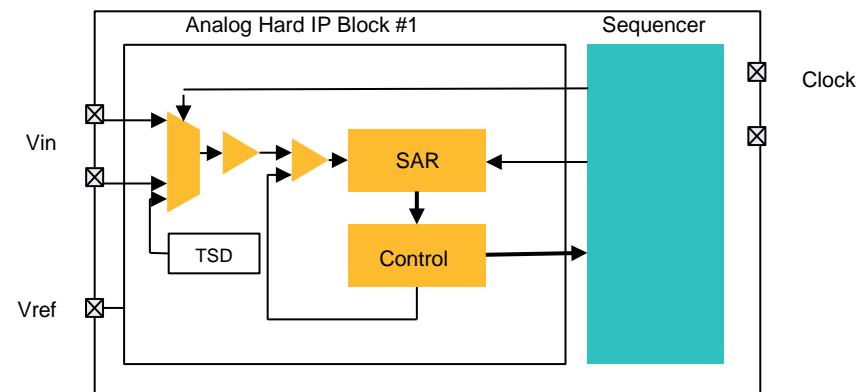
■ Modes of operation

- As a Nios® II slave component
 - Samples a predefined sequence of channels
 - Issues interrupt (IRQ) when complete
 - Or perform continuous conversions
- Standalone
 - Controlled by user-defined logic

0x3F	Slot 64	Ch n	Example sequence
0x04	Slot 5	Ch 0	
0x03	Slot 4	Ch 2	
0x02	Slot 3	Ch 0	
0x01	Slot 2	Ch 7	
0x00	Slot 1	Ch 0	

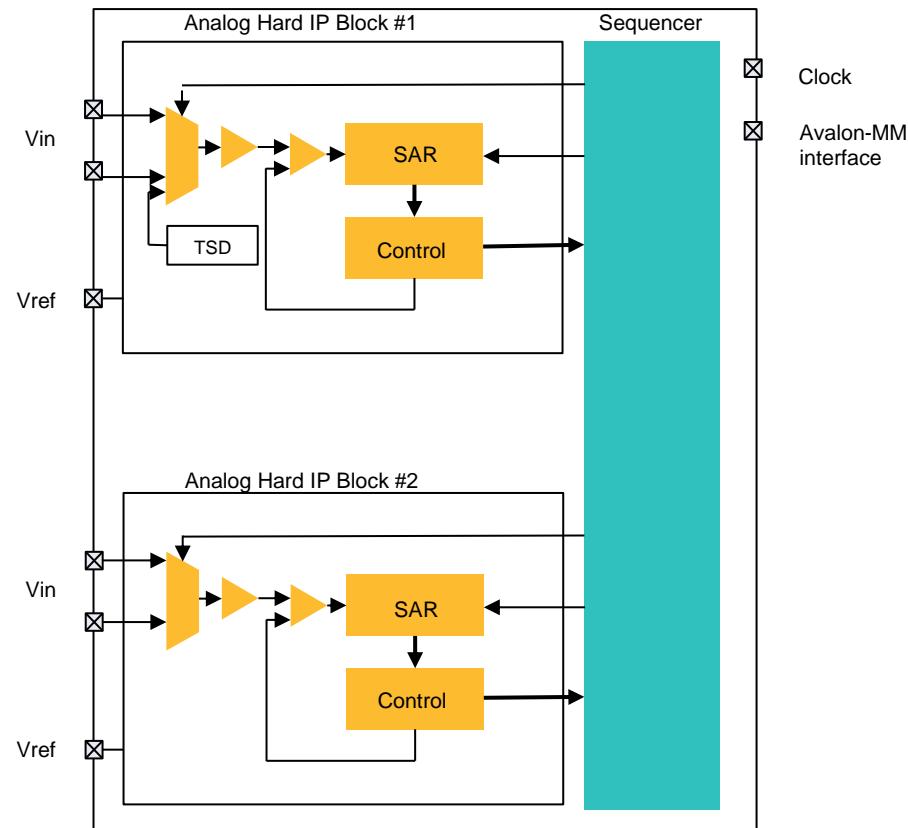
Separate ADC Sequencer Operation

- ADCs parameterized and instantiated separately
- Separate soft sequencer for each hard block
- Separate clock sources
- V_{ref} set individually for each ADC
 - But only 1 V_{ref} pin is available
 - 1 ADC can use external V_{ref} , while other uses internal



Dual ADC Operation

- Dual mode operation option use a single sequencer for both ADCs
- Simultaneous sample multiple inputs
 - Recommend using the dedicated inputs for this since they are matched for input delay
- Common sampling clock for both ADCs



MAX 10 Building Blocks

On-chip Flash and
Configuration



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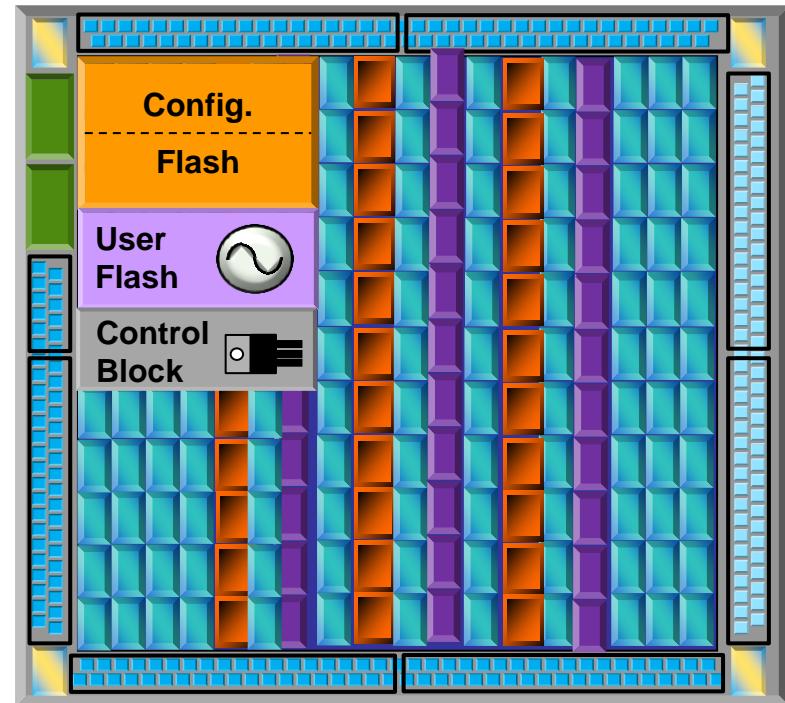
 **TEXAS
INSTRUMENTS**

V | Five Years Out

MAX 10 Flash Memory (CFM & UFM)

■ Two sections of flash

- Configuration Flash Memory (CFM)
 - Supports up to two images
 - Factory mode for in-system update
 - Application mode, or
 - Two personalities
- User Flash Memory (UFM)
 - Use Cases:
 - Store production date
 - Store Ethernet MAC Address
 - Local processor code storage
 - Nios II XIP (Execute in place)



Configuration Flash Memory (CFM)

- Instant On Configuration
- Single or Dual Configurations
- Less Board Space
- Smaller Bill of Materials
 - Reduces assembly costs
 - Simplified inventory management
- Increased Security
 - No exposed external interface

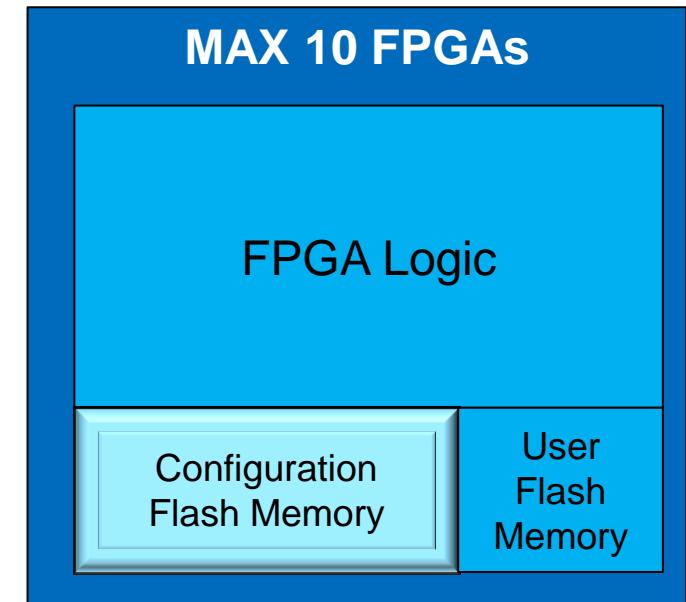


Figure Not to Scale

***Many Benefits to
Integrated Configuration Flash***

Dual Configuration Benefits

Capability	Use
Remote System Upgrade w/Fail-Safe Upgrade	Ship System Sooner
	Free Upgrades for Older Systems
	Paid Upgrades
Dual Personas	Reduce logic density by time multiplexing algorithms
	Reduce supply chain by combining multiple SKU's into one pre-programmed device



Infinite Possibilities with Dual Configuration

Dual Persona Configuration

- CONFIG_SEL pin selects one of two images from Configuration Flash Memory (CFM)
- At design time, CONFIG_SEL pin can be disabled to provide configuration *anti-tamper* protection

Use Case	Example
Two configurations on the Same Board	Instantly switch between two image processing algorithms.
One Image Per Board, on Two Boards	Consolidate two different sockets into a single BOM line item.



CONFIG_SEL

Dual Personas. Endless Possibilities.

Minimum Configuration Time (ms)

Product Line	Uncompressed, Unencrypted	Compressed, Unencrypted	Uncompressed, Encrypted	Compressed, Encrypted
10M02	1	4	3	4
10M04	1	5	7	5
10M08	1	5	7	5
10M16	2	9	12	9
10M25	2	12	17	12
10M40	3	31	43	31
10M50	3	31	43	31

Configures in Milliseconds

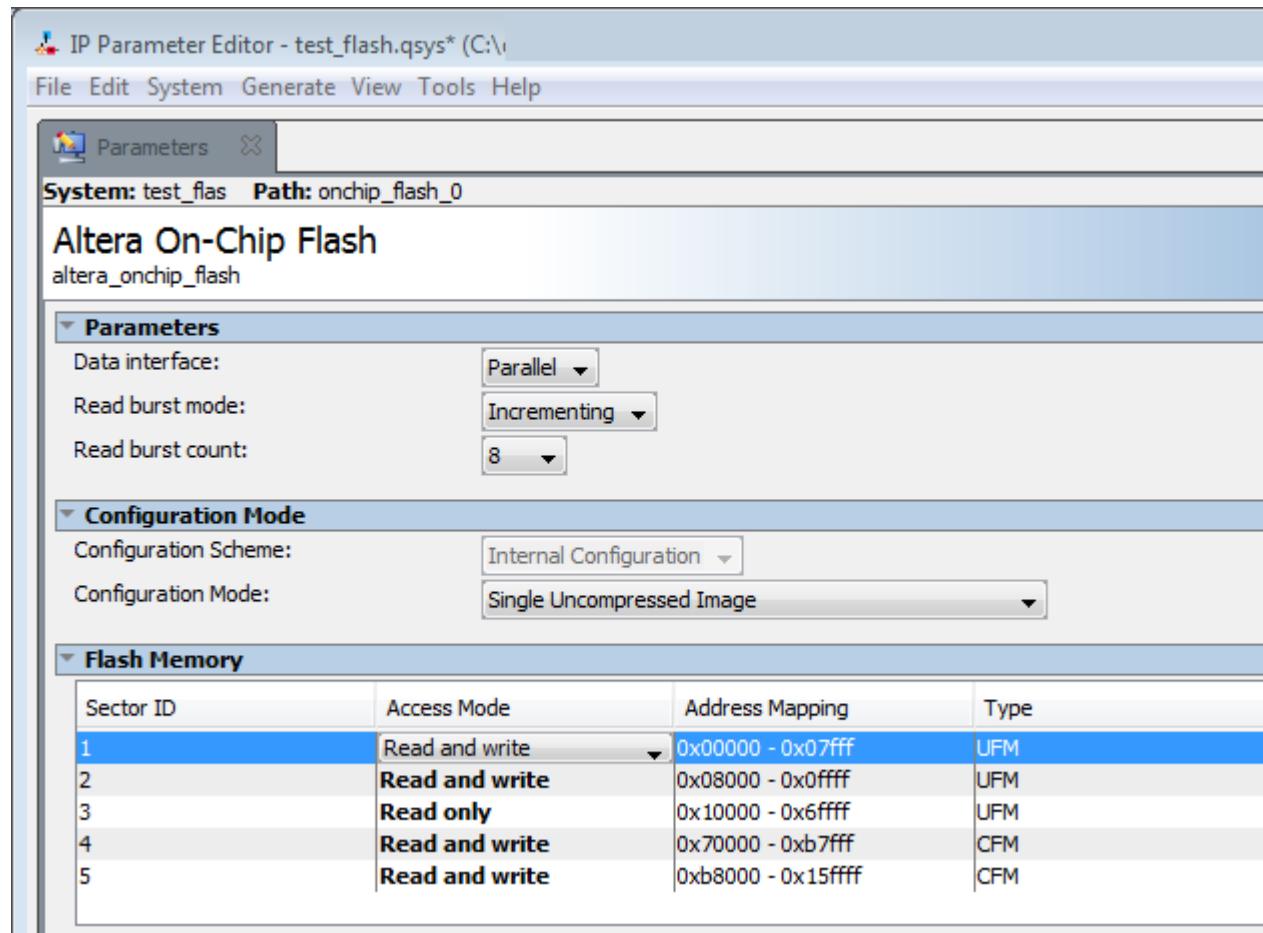
Configuration Flash Programming Methods

	Programming Method	Use Model
From JTAG	In System Programming (ISP)	Program configuration flash memory, right from the system board. User Flash Memory can also be programmed via ISP.
	Real Time ISP	Updates take effect at user defined time, or at next power cycle.
From FPGA User Mode	Remote System Upgrade (RSU)	Erase, Write, and Verify configuration flash memory from inside a user mode FPGA design.

Multiple Ways to Program Configuration Flash Memory

Update Flash via IP Parameter Editor

- Instantiate Flash interface
 - Parallel, or Serial
- Setup Configuration Mode
- Adjust the Access Mode to meet your design needs



Design Security – *Deny the Counterfeitors!*

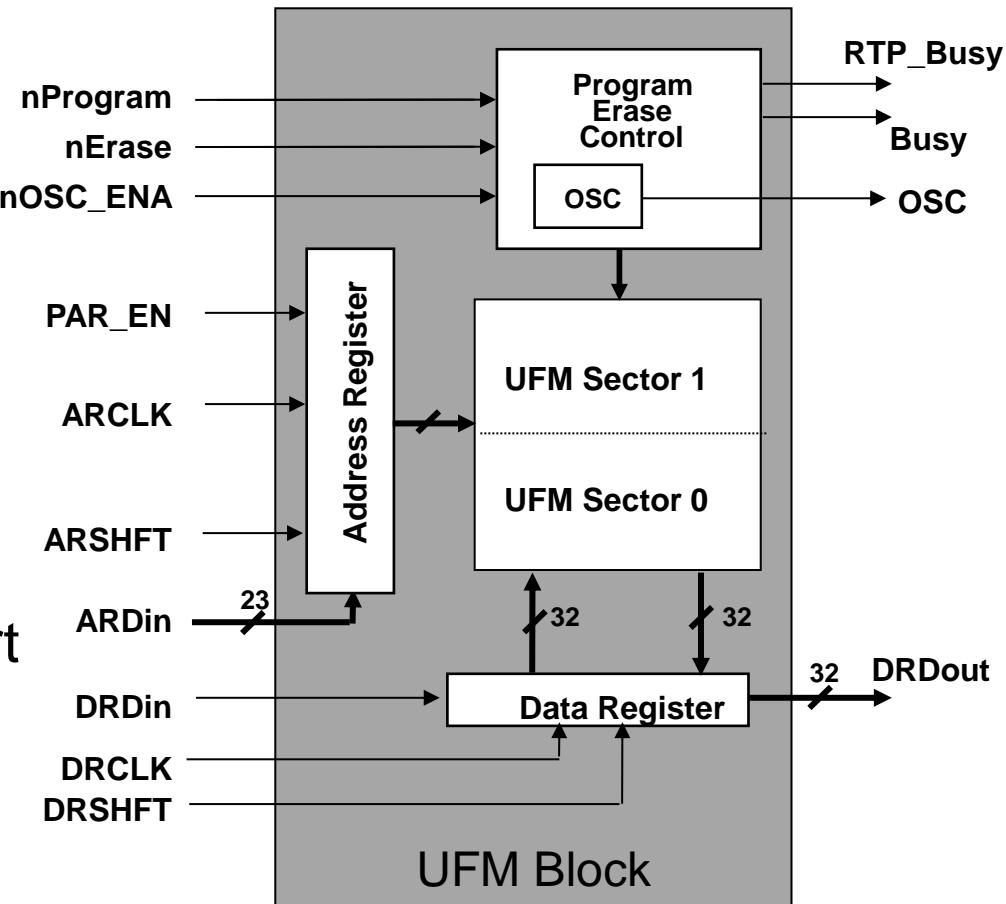
- Single chip solution with up to two secure configurations
- Advanced Encryption Standard (128-bit AES) protection
 - Non-volatile key for internal configuration
- JTAG port security protection
 - Read disable or Read/Write disable (OTP)
 - Prevents reverse engineering
- Embedded unique identification (ID)
 - 64 bit unique ID for traceability



Comprehensive Monolithic Design Protection

UFM Block Overview

- User Flash Memory Block
 - Up to 512 Kbits on largest device
- Supports native 32-bit parallel interface
 - Enhancement over MAX II/V UFM
 - Up to 320 Mbps read bandwidth
- SPI and I²C soft interfaces supported in Quartus® II
- Page and Sector erase support
- Integrated UFM oscillator available to core



Configuration scenarios & CFM utilization

Compression	RAM Preload	CFM0	CFM1	CFM2	UFM*
	<input checked="" type="checkbox"/>	CFM			UFM
	<input checked="" type="checkbox"/>	CFM			UFM
		CFM		UFM	
	<input checked="" type="checkbox"/>	CFM		UFM	
Dual Configuration		CFM	CFM		UFM

- 10,000 Erase and reprogram cycles
- Data retention
 - 20 years @ 80°C
 - 10 years @ 100°C

* Includes UFM0 & UFM1

Device	UFM Size
10M02	12 KB
10M04	16 - 156 KB
10M08	32 - 172 KB
10M16	32 - 296 KB
10M25	32 - 400 KB
10M40	64 - 736 KB
10M50	64 - 736 KB

MAX 10 Building Blocks

I/O, LVDS, and EMIF



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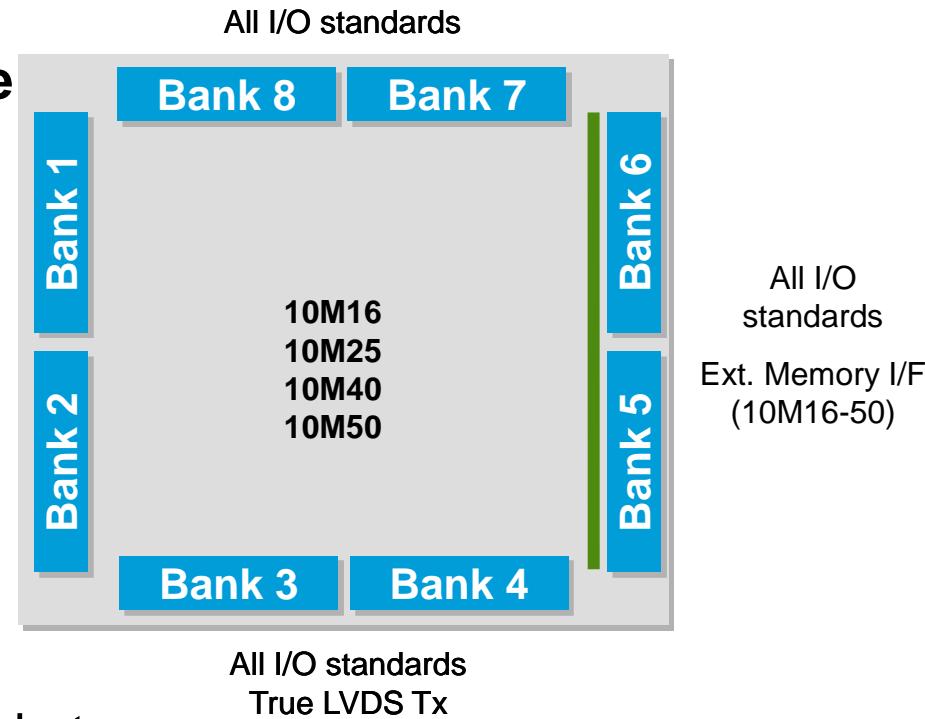
V | Five Years Out

I/O Features & Benefits

I/O features	Benefit
Multiple interfaces, standards, and features supported	<ul style="list-style-type: none">■ Easily bridge between different devices having different voltage levels or protocols■ Flexible I/O placements for easier PCB design and to reduce board area
Large number of I/O banks	Better granularity to mix and match different I/O requirements
Abundant I/O element registers	<ul style="list-style-type: none">■ Increase external memory interface performance■ Improve T_{co} performance
Dedicated differential output buffers	<ul style="list-style-type: none">■ Eliminate external resistors for LVDS, RSDDS, and mini-LVDS transmission■ LVDS interfaces up to 830 Mbps RX and 720 Mbps TX
Selectable series OCT (some with calibration)	On-chip termination reduces external passive cost & calibration eliminates variations due to PVT
Adjustable slew rates	Improve signal integrity by slowing down edge rates on non-performance-critical I/O pins

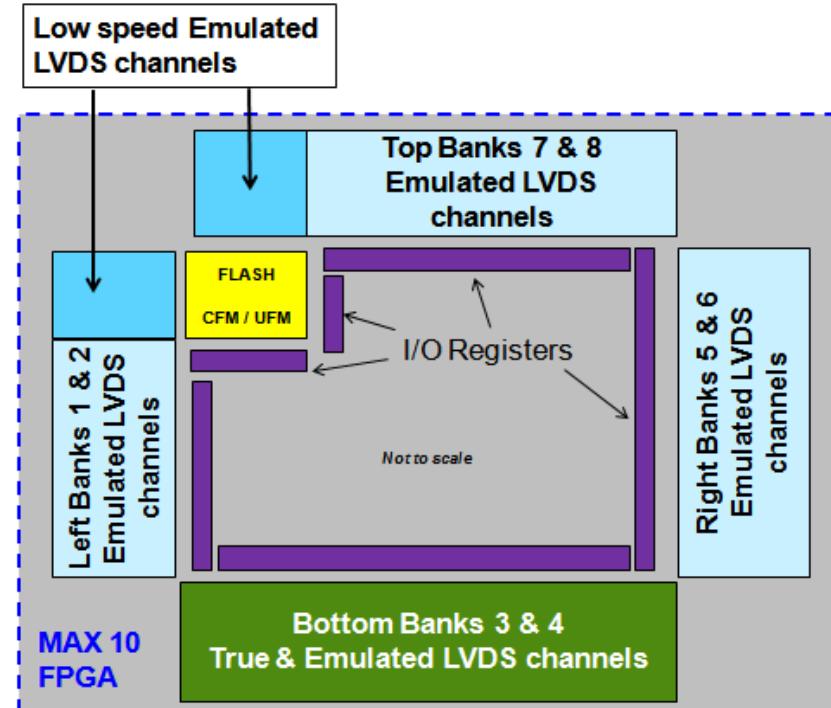
I/O Bank Details

- Interface to 3.3, 2.5, 1.8, 1.5, and 1.2V logic levels
- 3.3V PCI 32-bit, 33 MHz compatible
 - PCI clamp diode on all pins
- Output enable per pin
- Noise control features
 - Schmitt Triggers
 - Three step slew rate
 - Programmable output drive strength
- Emulated-LVDS I/O on all banks
 - True LVDS I/O, bottom banks only
- On-chip series termination & Hot-Socket Compliant



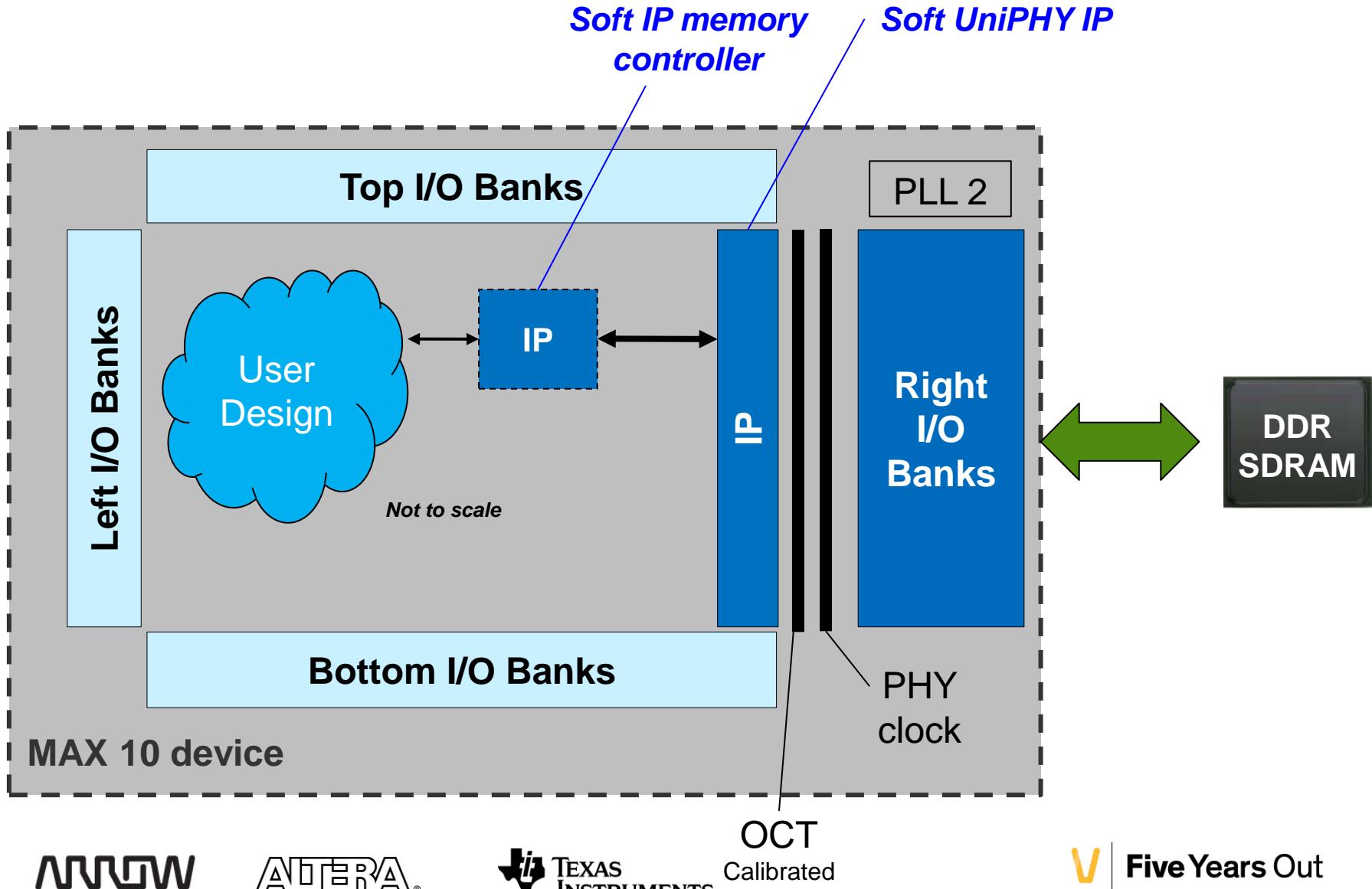
LVDS on Every I/O

LVDS Type	Description	Performance	
		Single-Supply Voltage	Dual-Supply Voltage
True	Full differential matched channel Rx / Tx (Banks 3, 4)	Up to 290 Mbps	Up to 720 Mbps
Emulated	Requires external 3-resistors at Tx (Banks 2, 5, 6, 7)	Up to 285 Mbps	Up to 600 Mbps
Low speed Emulated	Requires external 3-resistors at Tx (Banks 1a, 1b, 8)	Up to 200 Mbps	Up to 300 Mbps



Performance & Termination is Location/Bank Dependent

EMIF Solution Floorplan



MAX 10 device

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Texas
Instruments

OCT
Calibrated

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Powering DECA

With Enpirion Power SoC
Devices



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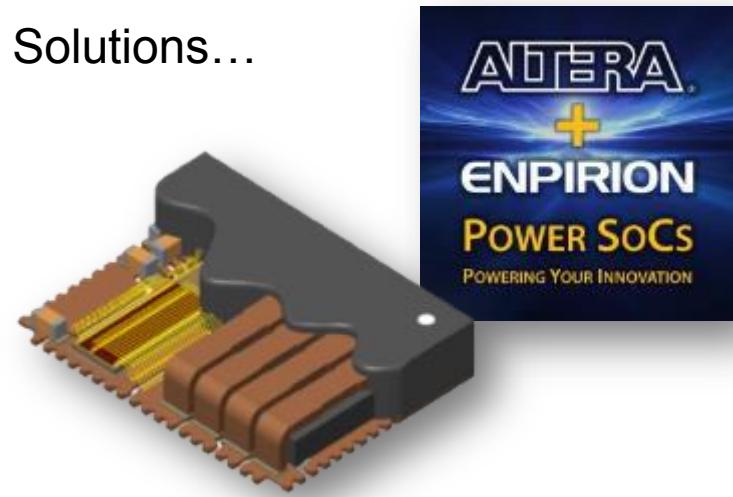
Texas
INSTRUMENTS

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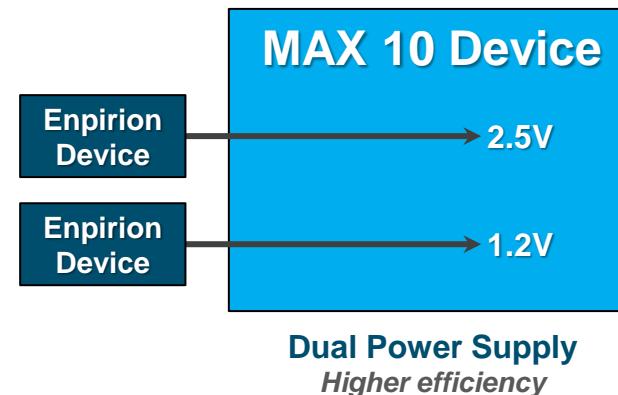
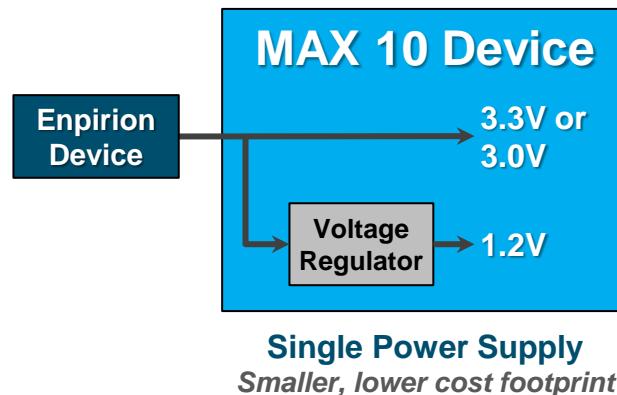
Enpirion® Power Solutions for MAX 10 FPGAs

Together, MAX 10 Devices with Enpirion Power Solutions...

- Shrink solution size
- Meet the toughest reliability requirements
- Simplify board design
- Reduce bill-of-materials complexity and cost
- Enable system size and efficiency trade-offs



A Complete Altera Solution: Enpirion PowerSoCs Ideal for MAX 10 Devices



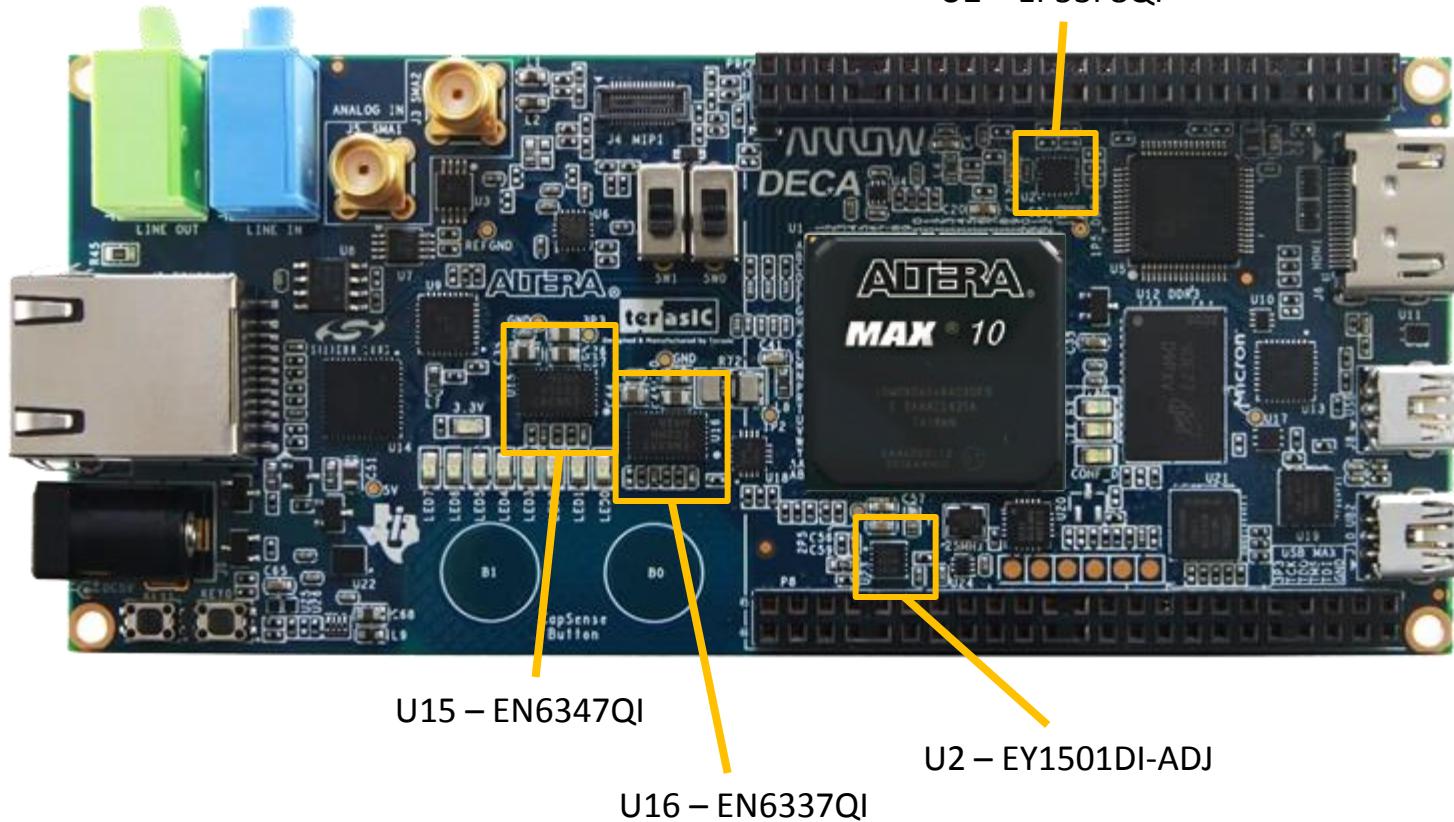
Power supply variant differences

Feature	Single Supply Variant	Dual Supply Variant
Core Speed	Fmax = 100 MHz	Fmax = 150+ MHz
DSP	Up to 198 MHz	Up to 234 MHz
LVDS	200 – 400 Mbps	380 – 830 Mbps
EMIF	Not Supported	DDR2 / LPDDR2 @ 200 MHz DDR3 @ 300 MHz
RAM Blocks	Up to 232 MHz	Up to 284 MHz
DSP Blocks	Up to 198 MHz	Up to 234 MHz
PLLs	Single PLL support	Up to 4
Analog Block	SNR: 54 dB SINAD: 53 dB	SNR: 64 dB SINAD: 63 dB

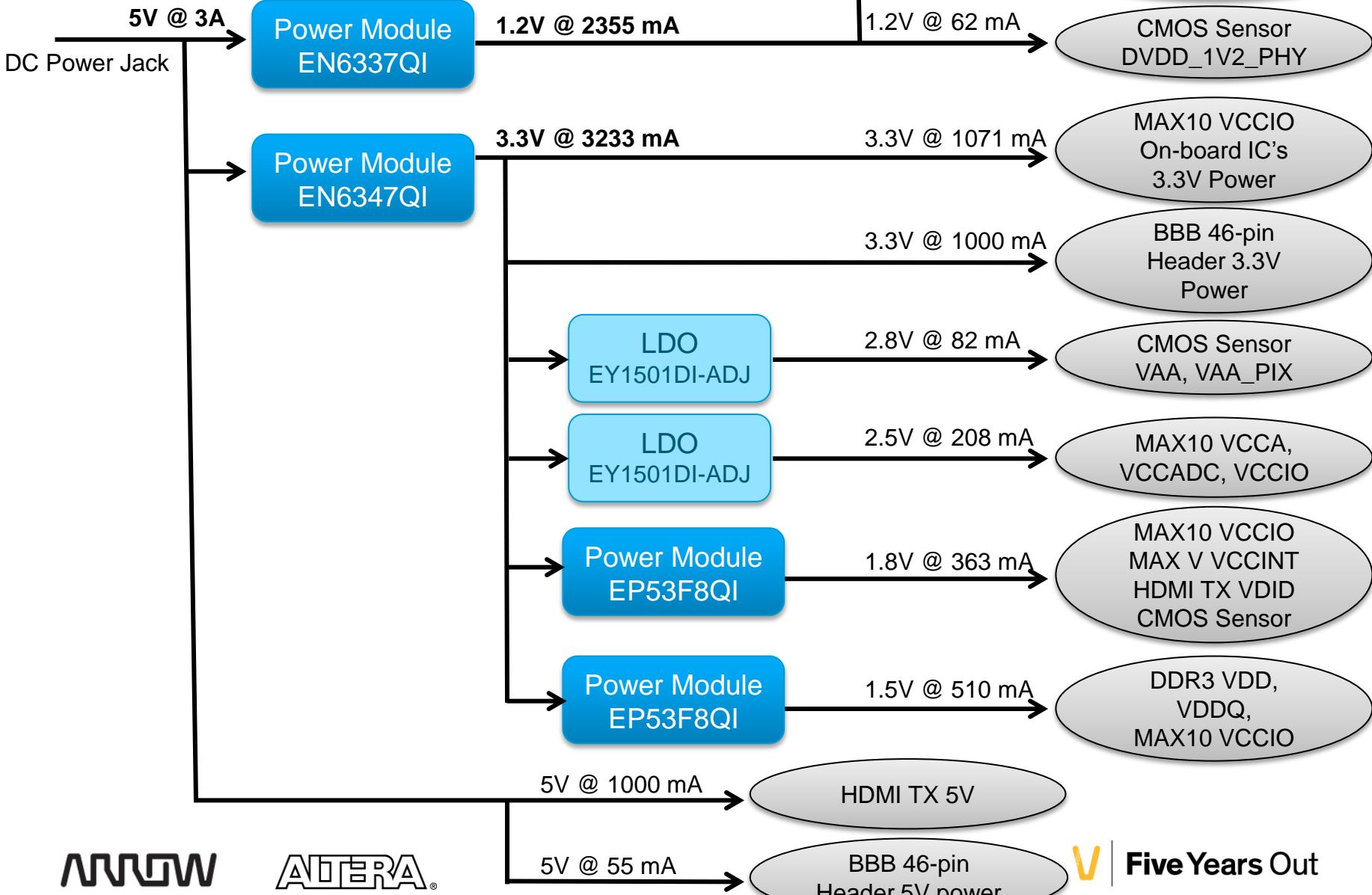
Single supply devices optimized for Simplicity

Dual supply devices offer increased Performance

DECA Power – Top side of board



DECA Power Tree



DECA Evaluation Board Details

Getting to know your kit



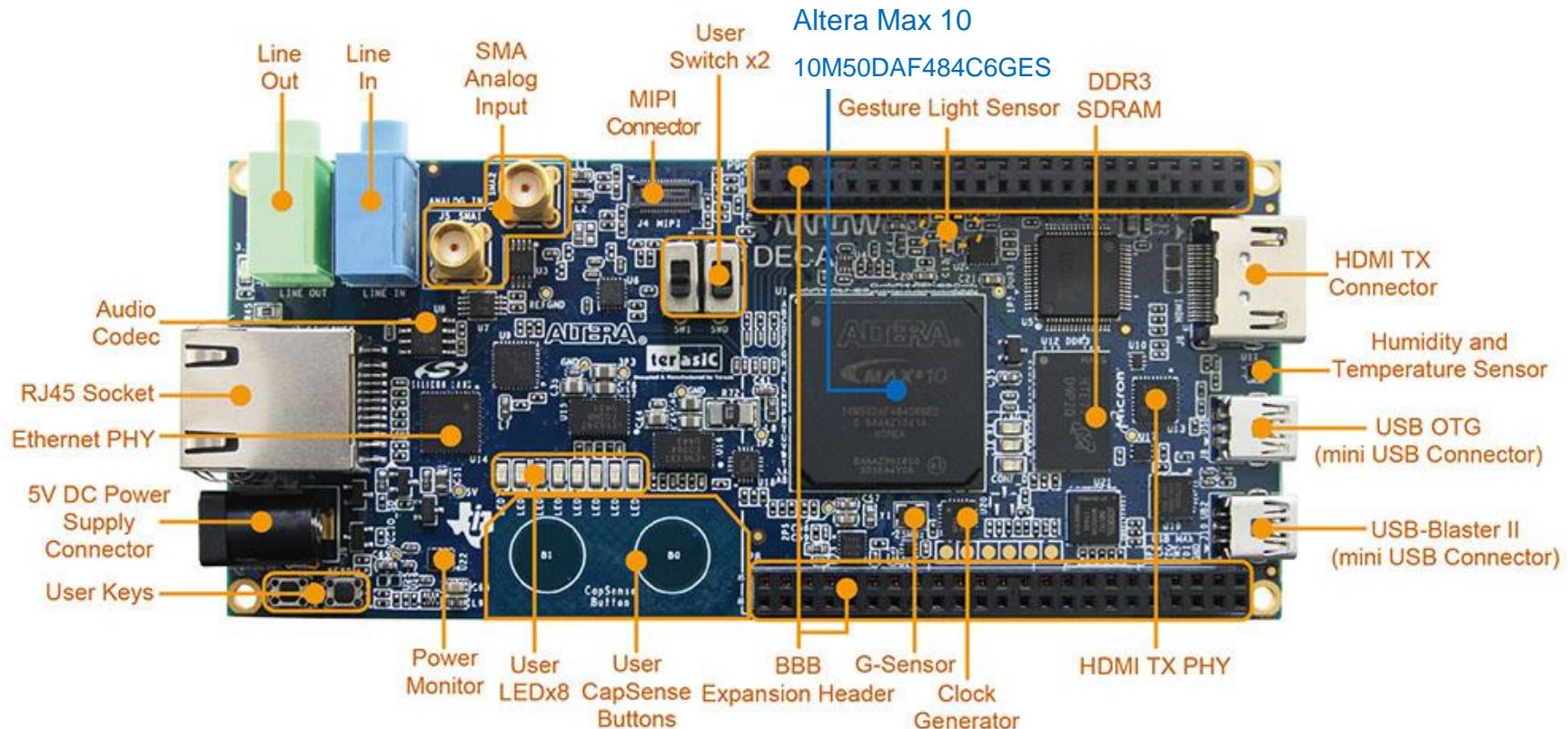
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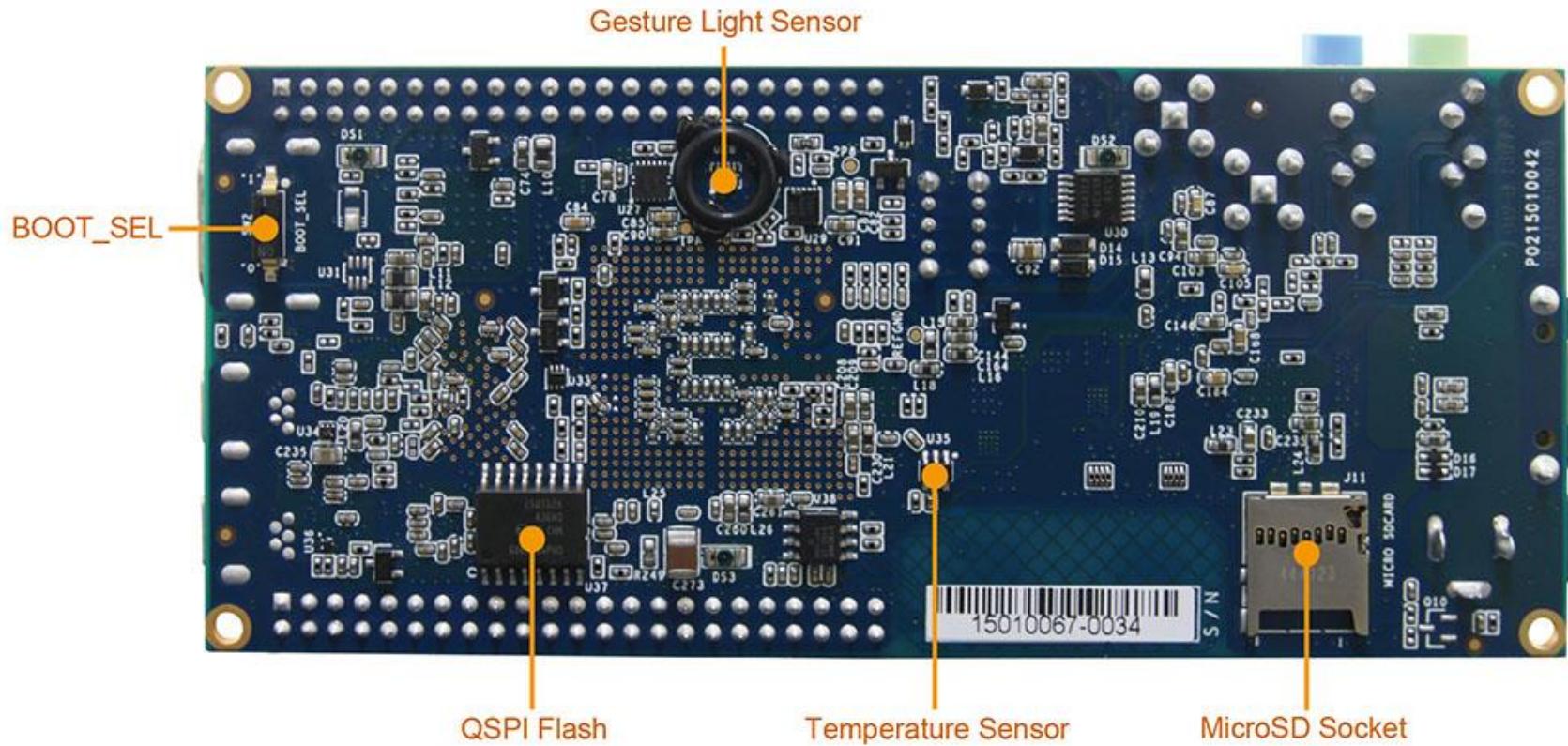
 **TEXAS
INSTRUMENTS**

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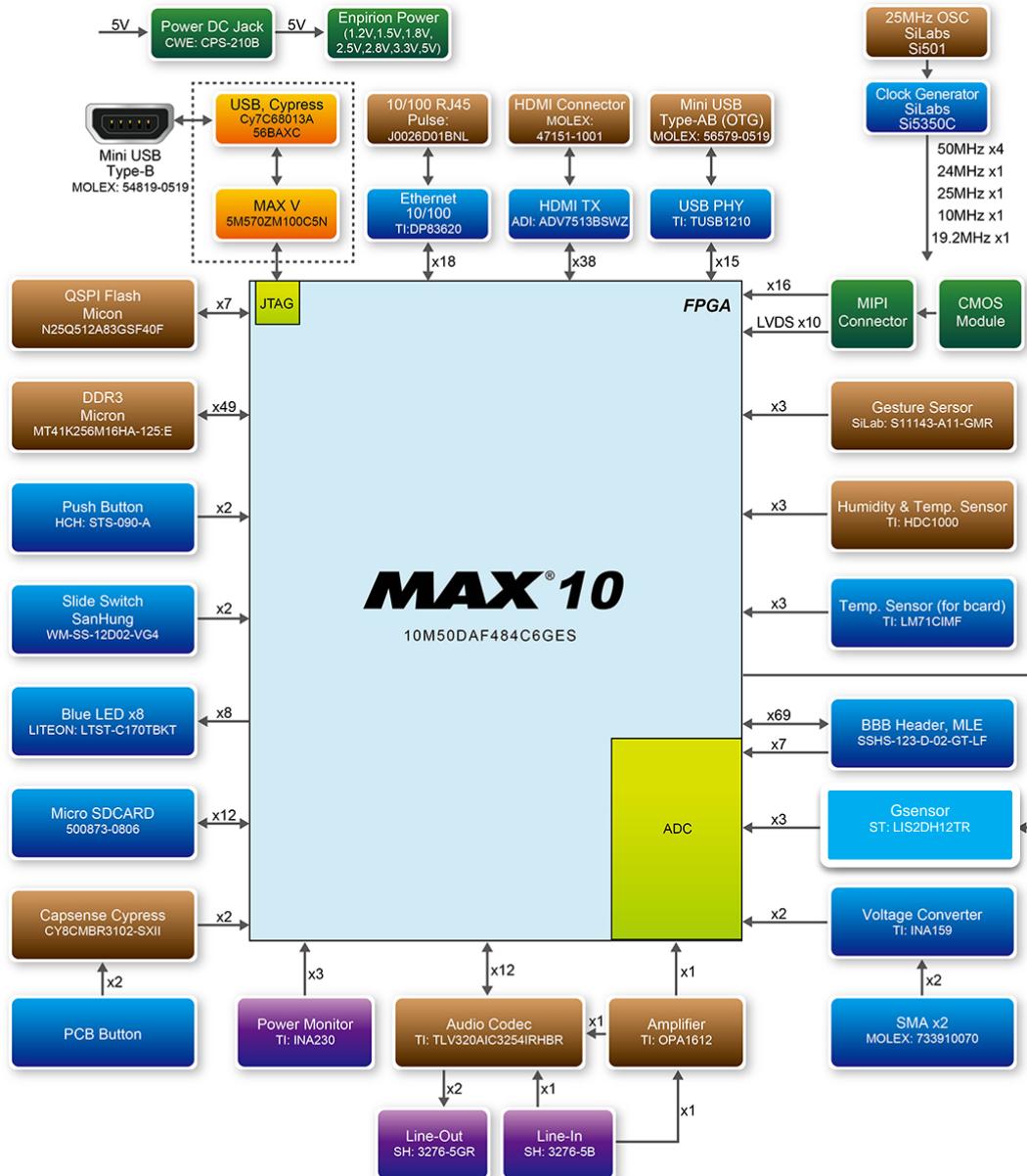
DECA Evaluation Board – Front



DECA Evaluation Board – Back



DECA Evaluation Board – Block Diagram



Things to know about your DECA board

■ Powering the DECA

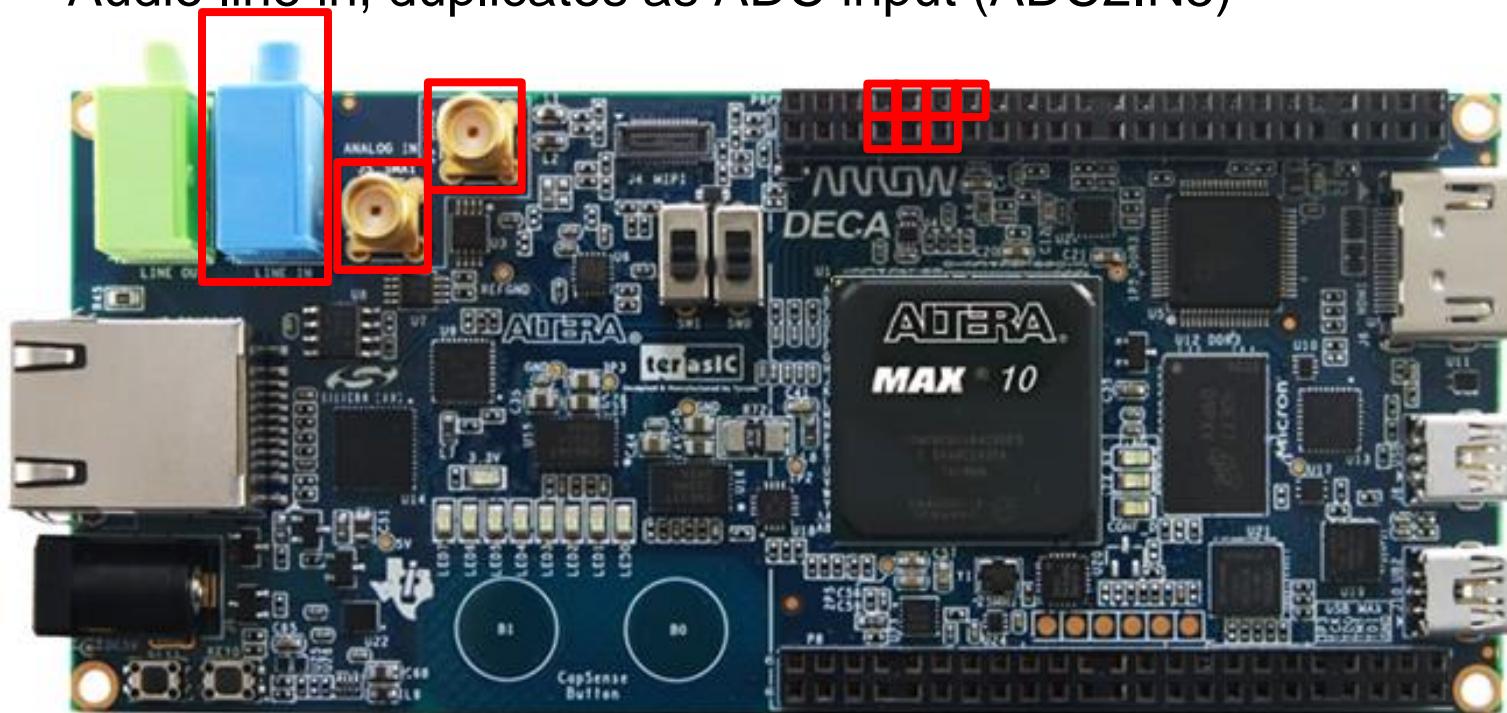
1. 5V adapter, 2A (or 3A) provided in kit
2. USB powered, UB2 J10 (USB-Blaster connection)



Things to know about your DECA board

■ ADC Inputs

- SMA inputs
- BBB header, P9
- Audio line in, duplicates as ADC input (ADC2IN5)



DECA Evaluation Board

Partner Solutions



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Texas Instruments

- TI played an integral part of the DECA design
- Providing 20 unique parts including:
 - Humidity and Temperature Sensors
 - Ethernet PHY
 - Audio CODEC
 - USB PHY
 - ESD Protection Devices
 - Power Monitor
 - OP-AMP's
 - Voltage Reference
 - Load Switch with Reverse Current Protection

HDC1000

Features

- | | |
|---|---------------------------|
| ▪ Relative Humidity Range | 0% to 100% |
| ▪ Humidity Accuracy | $\pm 3\%$ |
| ▪ Typical Drift | < 0.5%/yr |
| ▪ Supply Current (Measuring) | 180uA |
| ▪ Avg Supply Current (@1sps) | 1.1uA |
| ▪ Temperature Accuracy | $\pm 0.5^{\circ}\text{C}$ |
| ▪ Temperature Range (Operating) | -20°C to +85°C |
| ▪ Temperature Range (Functional) | -40°C to +125°C |
| ▪ Operating Voltage | 3V to 5V |
| ▪ Package | |
| ▪ 8 pin W CSP HDC1000 (1.59mm x 2.04mm) | |
| ▪ 6 pin DFN HDC1050 (3mm x 3mm) | |

Applications

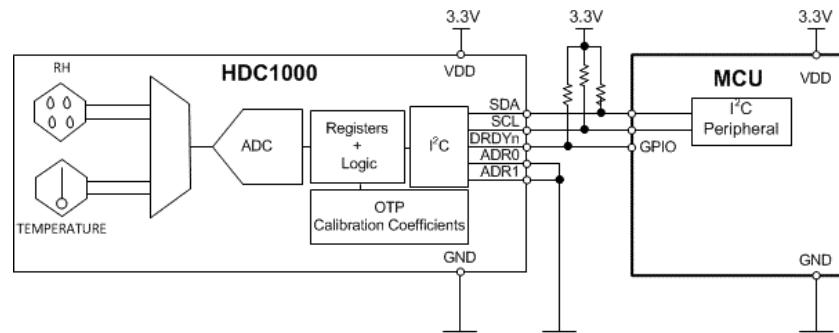
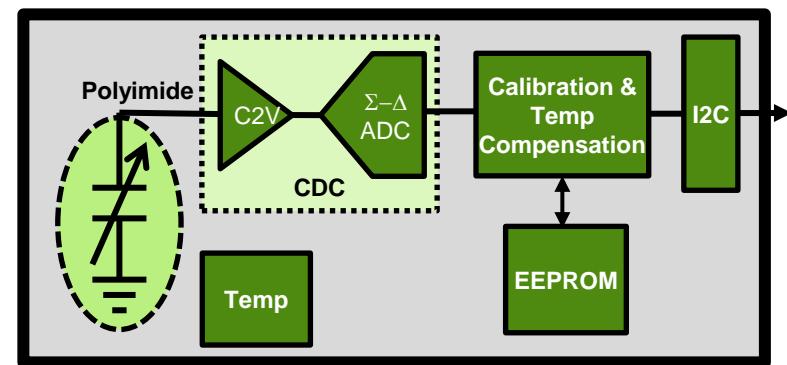
\$2.20 @ 1Ku

- HVAC
- White goods (dryer, fridge, microwave, dishwasher)
- Printers
- Handheld Meters
- Camera Defog
- Smart Thermostats and Room Monitors
- Medical Devices

Humidity & Temperature Sensor

Benefits

- Completely integrated humidity and temperature IC provides guaranteed performance
- Fully calibrated sensor enables quick time-to-market
- Very low power consumption
- Small package size supports compact designs



LM71

Features

- AEC-Q100 Grade 0 Qualified
- Accuracy specified over operating range of -40'C to +150'C
- Operating supply current 550uA max

Applications

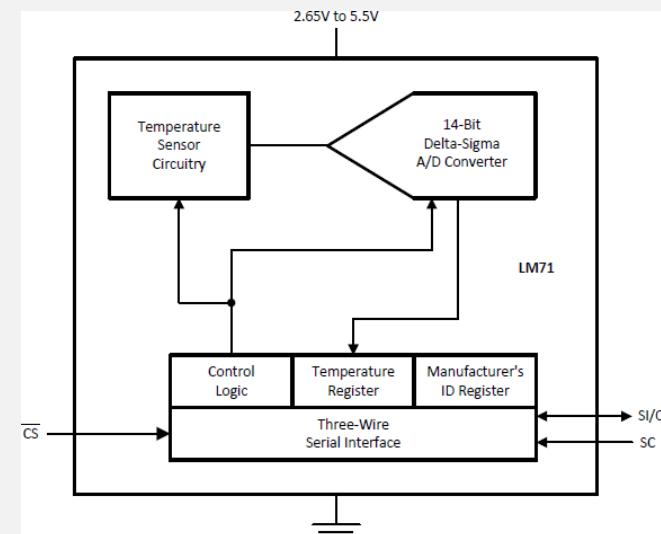
\$0.71 @ 1Ku

- Automotive Other
- Test & Measurement Solutions
- Computer
- Vending Machine

SPI/MICROWIRE 13-Bit Plus Sign Temperature Sensor

Benefits

- Automotive grade qualified
- Wide operating voltage range
- Low power consumption extends battery life



DP83620

Features

- Deterministic, low transmit and receive latency
- Dynamic Link Quality monitoring
- Auto-MDIX for 10/100 Mbps
- Error-free operation up to 150m, far exceeding IEEE specifications
- IEEE 802.3u 100BASE-FX Fiber Interface Optional 100BASE-TX fast link loss detection
- Industrial temperature range, -40 to 85C
- Small 7 x 7 mm² 48 pin LLP package
- Footprint compatible upgrade to DP83630 (with IEEE 1588)

Applications

\$1.52 @ 1Ku

- Factory Automation
- General Embedded Applications

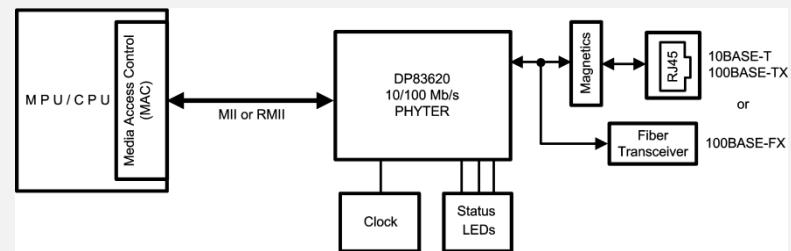


EVM PART # DP83620-EVK/NOPB

10/100 Ethernet PHY

Benefits

- Real-time communication
- Validate integrity of data link
- Auto-Negotiation determines proper configuration for Tx and Rx of data



TLV320AIC3254

1.8V Very Low-Power Stereo Codec with Embedded miniDSP

Features

- Embedded miniDSP (110MIPS)
- Power consumption: less than 5mW in stereo playback at 48kHz
- Single supply operation (1.8-3.6V)
- Support for stereo analog and digital microphones
- Integrated stereo headphones driver

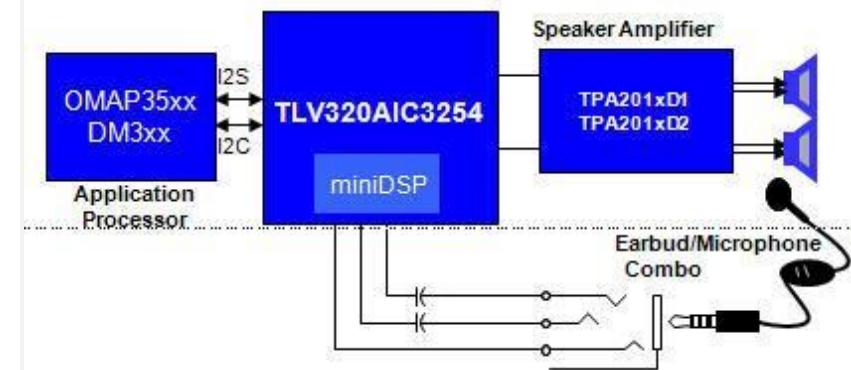
Benefits

- Allows to run advanced audio processing algorithms and offloads host processor
- Longer battery life (or smaller/cheaper batteries)
- Simplifies board design and reduces its cost (it eliminates 1 LDO for savings of ~\$0.1x)
- Digital mic improves system level noise immunity
- Integration reduces device count, simplifies board design

Applications

\$3.95 @ 1Ku

- Handset: Smartphone
- Portable Media Player
- Active Noise Cancellation (ANC)
- Wireless Headset
- Portable navigation Devices (PND)



TUSB1210

Features

- Fully compliant to USB 2.0 and USB OTG 1.3 Specifications
- Fully compliant to UMTI+ Low Pin Interface (ULPI) Specification Rev. 1.1 with a 12-pin SDR Interface supporting master & slave clock modes
- 20V VBUS overvoltage protection, DP,DM, ID 5V short-circuit protection for cable shorting to VBUS pin

Applications

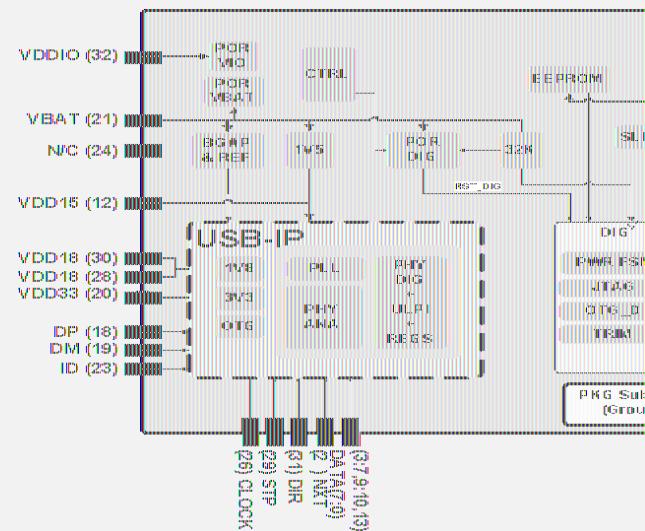
- Handset: Multimedia
- Handset: Smartphone
- Portable Media Player
- GPS: Personal Navigation Device
- Digital Still Camera
- Audio Dock: Performance

\$0.80 @ 1Ku

USB 2.0 ULPI Transceiver

Benefits

- Insure Interoperability across a wide range of PC and Consumer Platforms
- Insure Interoperability across a multiple processor platforms via a glueless, industry-standard interface
- Prevent damage to sensitive electronics introduced by new USB Charger Requirements.

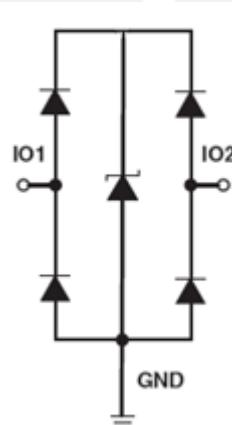


TPD2EUSB30A

Features

- System-level ESD protection for high speed applications
 - IEC 61000-4-2 (Level 4) ESD protection
 - 5-A Peak Pulse Current (8/20us Pulse)
- **Low I/O pin capacitance**
 - 0.9pF on DBZ package, 0.7pF on DRT package
- **3dB Bandwidth in excess of 4GHz**
- Voltage Breakdown of 4.5V
- 0.05pF Matching Capacitance between Differential Signal Pairs

Logic Block Diagram



Applications

\$0.15 @ 1Ku

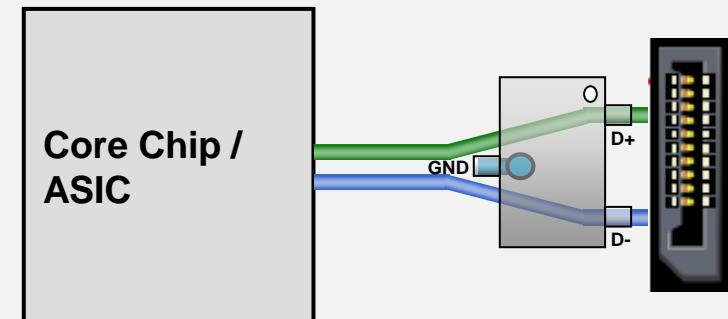
- DisplayPort
- USB 3.0 High-Speed
- HDMI
- e-SATA
- FireWire 1394

2-Channel ESD Protection for USB 3.0 Applications

Benefits

- Flow-through Single-in-Line Pin Mapping for the HS Lines ensures no additional board layout burden while placing ESD Protection Chip near the connector
- Flexible layout option to populate ESD chip only if the system needs require additional system-level protection
- Ideal for low-voltage USB data lines
- No layout skew for the differential pair
- Minimum distortion in the high-speed lines

Layout Example at
DisplayPort Interface



TPD4E001

Low Capacitance 4-Channel ESD Protection array for High-Speed Data Interfaces

Features

- ESD Protection exceeds
- +/-15 KV Human Body Model (HBM)
- +/-8 KV IEC 61000-4-2 (Contact Discharge)
- +/-15 KV IEC 61000-4-2 (Air-Gap Discharge)
- 0.9-V to 5.5-V Supply Voltage Range
- Low 1-nA Supply current
- **Low 1.5-pF Input Capacitance**
- **Low 1-nA (Max) Leakage Current**
- Alternate 2-, 3-, 6-channel options available:
TPD2E001, TPD3E001 and TPD6E001

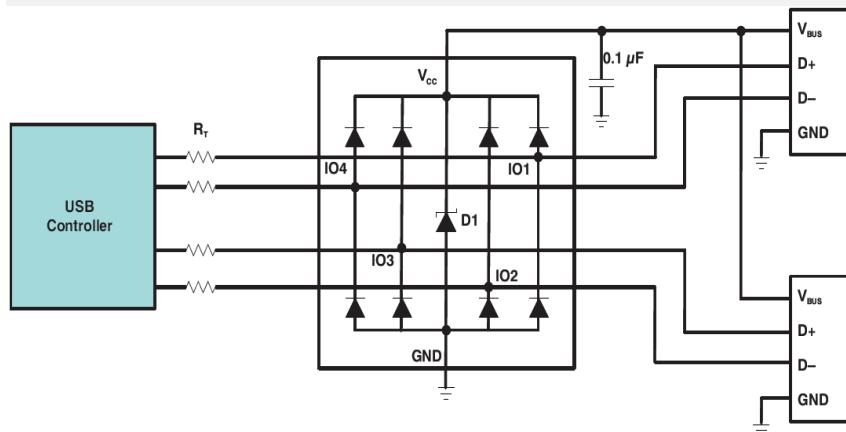
Applications

\$0.17 @ 1Ku

- USB 2.0
- Ethernet
- FireWire
- Video
- Cell Phones
- SVGA Video Connections
- Glucose Meter

Benefits

- Low capacitance makes it ideal for use in high-speed data IO interfaces.
- Offers little or no signal distortion due to low IO capacitance and ultra low leakage current specifications.
- Low leakage current enables usage in high precision analog measurement devices
- Vcc pin allows the device to work as transient suppressor
- Space saving DRL and QFN package options



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TPD4E05U06

Features

- Supports differential data rate up to 6Gbps
- Optimized package and pin-mapping for high-speed differential lines
- IEC 61000-4-2 Level 4: 12kV Contact, 15kV Air
- 2.5-A Peak Pulse Current (8/20 μ s Pulse)
- $C_{IO \text{ to GND}} = 0.5\text{pF}$
- $R_{dyn} = 0.8\Omega$
- Commercial and Automotive grade available

Applications

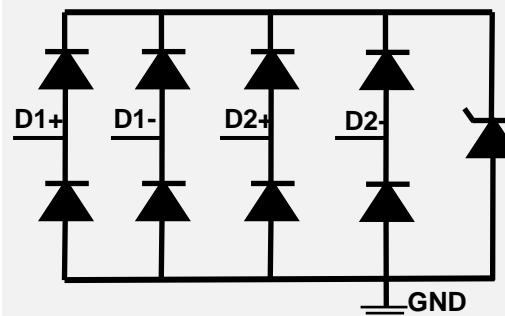
\$0.19 @ 1Ku

- HDMI
- USB3.0
- MHL
- DisplayPort

4-Channel ESD Protection for Ultra High Speed Data Lines

Benefits

- Flow-through pin mapping for easy top layer routing
- Low parasitic capacitance to protect high speed data lines
- Space saving footprint



DQA PACKAGE
(TOP VIEW)

D1+	1	10	N.C.
D1-	2	9	N.C.
GND	3	8	GND
D2+	4	7	N.C.
D2-	5	6	N.C.

2.5 mm x 1 mm x 0.5mm
(0.5-mm pitch)



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TPD4S012

Features

- IEC 61000-4-2 (Level 4) System level ESD Compliance:
 - +/-10 KV (Contact Discharge)
 - +/-10 KV (Air-Gap Discharge)
- USB Signal Pins (D+, D-, ID)
 - **0.8 pF Line Capacitance**
 - 6-V (min) Breakdown Voltage
- VBUS Line (V_{BUS})
 - **11 pF Line Capacitance**
 - 20-V (min) Breakdown voltage
- 3A Peak Pulse Current (8/20 μ sec Pulse) for V_{BUS} , D+, D-, and ID lines
- I_{off} feature

Applications

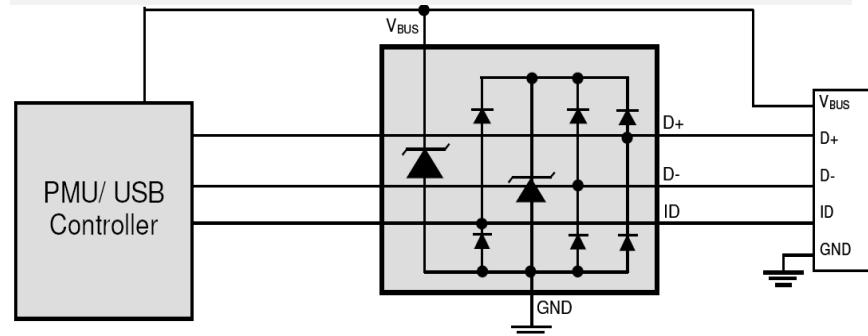
\$0.21 @ 1Ku

- USB High-Speed or USB OTG Interface
- USB charger interface
- Cell Phones

4-Channel ESD solution for USB-HS/ USB OTG/ USB Charger Interfaces

Benefits

- Flow through a Pin Mapping for the HS Lines ensures zero additional skew due to board layout while placing ESD Protection Chip near the connector.
- Supports Data Rates in excess of 480 Mbps
- Industrial Temperature Range
- Space saving DRY packages



INA230

Features

▪ APPLICATION CONFIGURABLE

- Reports Current, Voltage and Power
- Programmable Sample Averaging
- Independent Programmable Conversion Times

▪ HIGH ACCURACY

- 50uV Offset Voltage (Max)
- 40V/C offset drift (max)
- 0.5% Gain Error (Max)
- 120dB CMRR (Typ).

▪ WIDE DYNAMIC RANGE

- Common-Mode Range: 0V to 26V
- Supply Range: 2.7V to 5.5V

Applications

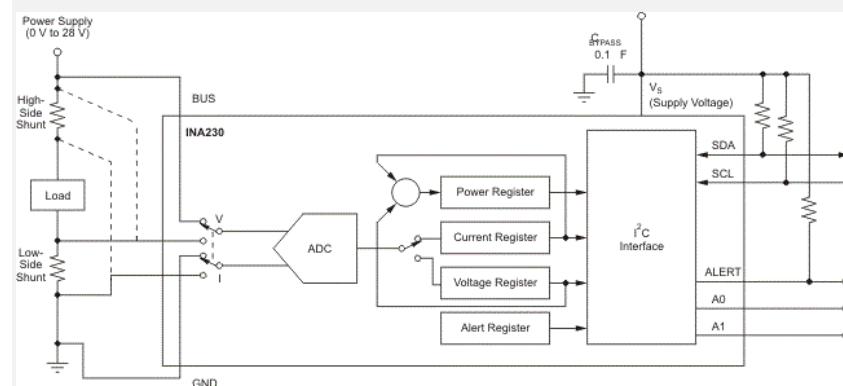
\$1.15 @ 1Ku

- Tablet: Multimedia
- Handset: Smartphone
- Commercial Notebook
- Server Motherboard
- Industrial Power

Precision Digital/Current/Voltage/Power Monitor

Benefits

- Adaptable configuration to optimize performance under multiple operating conditions
- Accurate power monitoring at low currents with wide dynamic range for high peak currents. Reduces IR loss thru smaller shunt resistors.
- Monitor across a wide common mode input range without requiring a high voltage supply or the need to scale the supply.



INA159

Features

- Laser trimmed on-chip resistors
- TCR tracking of resistors
- High Precision:
- Offset voltage: 100uV with 1.5uV/C drift
- Bandwidth: 1.5MHz
- Slew Rate: 15V/us
- 4-Corner Overview Slide

Applications

\$1.70 @ 1Ku

- Audio differentiable line driver
- Audio mix consoles
- Digital effects processors
- Telecom systems
- HI-FI Equipment
- Graphic/parametric equalizers

High-Speed, Precision Gain of 0.2 Level Translation Difference Amplifier

Benefits

- Yields accurate gain and high CMR of 96 dB.
- Maintains accuracy and CMR over temperatures.
- Combination of precision AC and DC performance make the device useful in a variety of sensor signal conditioning systems.

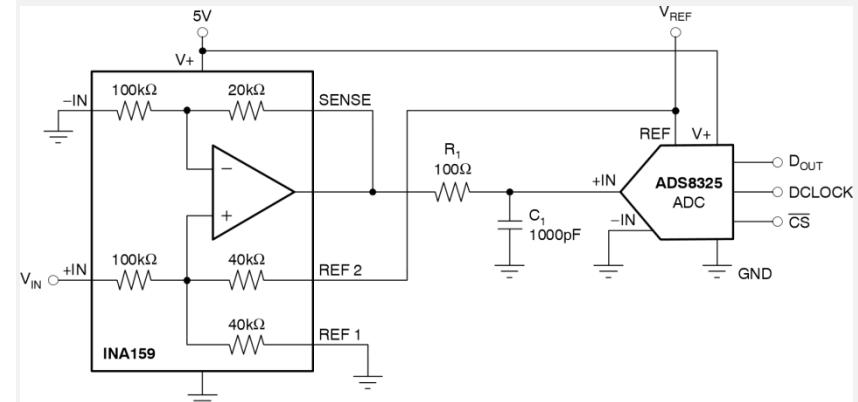


Figure 1. Typical Application

OPA4314

Features

- Low supply voltage operation with rail-to-rail in and out
- Low power of 210uA and wide 3MHz bandwidth
- Robust output drive can drive heavy loads without external compensation
- Low input bias current and low current noise density of 0.2pA and 5fA/rtHz respectively
- Powerpoint Overview Slides

Applications

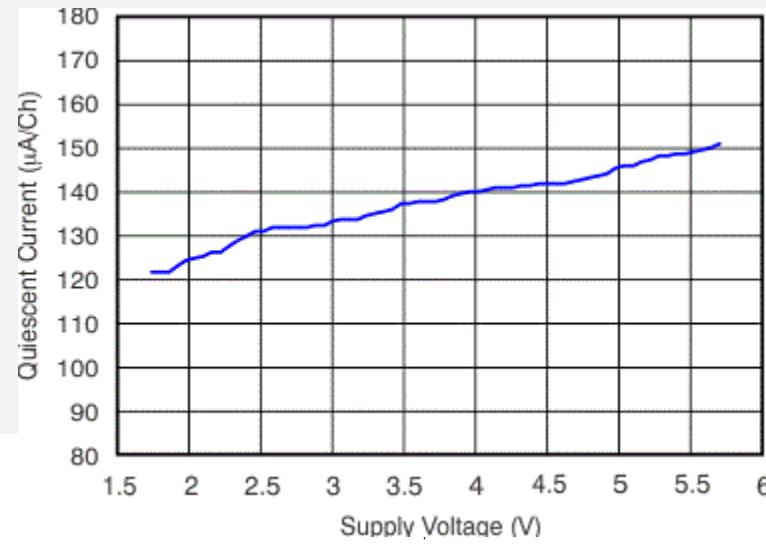
\$0.65 @ 1Ku

- Active filters
- Home glucose meters
- Fire and Smoke Detection
- Photodiode pre-amplifier
- Consumer Electronics Other

General purpose 1.8V, 3MHz, 210uA, RRIO, Quad CMOS Operational Amplifier

Benefits

- Maximizes dynamic range without concern to the power budget
- The OPAX314 offers power savings of up to 40% against similar competitive devices and has a wide BW for high gain configurations and multi-stage gains
- The OPAX314 can drive capacitive loads of up to 1000pF in positive unity gain configurations
- Ideal for high impedance sources such as photodiode amplifiers and multi-feedback active filters where noise is critical and impacts the digitization of the signal



REF3125

Features

- Precision Output Voltage:
- Low Temperature Drift: 20ppm/C
- High Accuracy: 0.2% Max
- Low Output Noise: 39uVpp
- Multiple Available Voltages: 1.25V, 2.048V, 2.5V, 3.0V, 3.3V, 4.096V
- Robust Design at Low Power
- Low Supply Current: 115uA
- High Output Current: +/-10mA
- Low Dropout Voltage: 50mV
- Micro-Package: SOT23-3

Applications

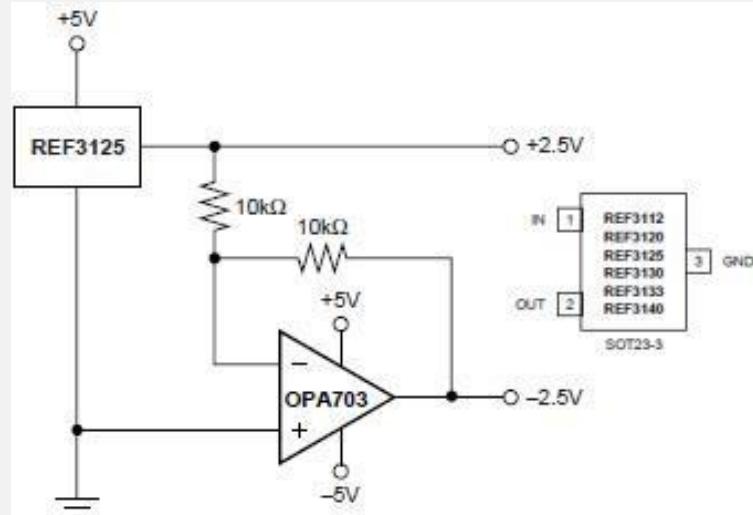
\$0.99 @ 1Ku

- Data Acquisition Systems
- Portable Equipment
- Medical Equipment
- Test Equipment
- Spot Regulator

20ppm/Degrees C Max, 100uA, SOT23-3
Series Voltage Reference

Benefits

- Simplifies design with reduced need for over temperature calibration and multiple output voltage options
- Minimizes need for additional load driving capability saving design time and expense



TPS22910A/12C

5.5V, 2A, 61mΩ Load Switch with Reverse Current Protection

Features

- Input Voltage Range: 1.4V to 5.5V
- 2A Maximum Continuous Current
- Low ON-Resistance
 - R_{ON} (typ) = 60mΩ at $V_{IN} = 5.0V$
 - R_{ON} (typ) = 61mΩ at $V_{IN} = 3.3V$
- $I_Q < 2\mu A$ (typ) & Shutdown: $< 1.2\mu A$ (typ)
- **Active Low Logic (TPS22910A)**
- Active High Logic (TPS22912C)
- **Under Voltage Lock Out**
- 4-WCSP Package:
 - 0.9mm x 0.9mm x 0.5mm and 0.5mm pitch

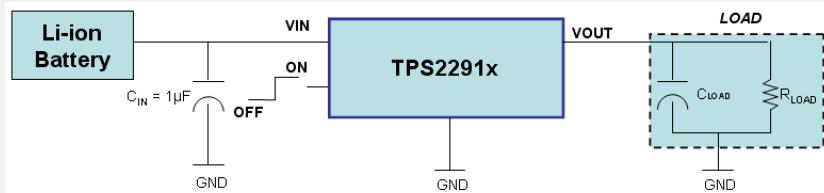
Applications

\$0.24 @ 1Ku

- Wearables
- Mobile Phone
- Storage
- Building Automation
- PC, Notebooks
- Electronic Point of Sale (EPOS)

Benefits

- Ideal for portable applications
- Minimum dropout through the pass FET
- **No reverse current to the battery while switch is enabled, disabled, or at $V_{IN} = 0V$**
- Minimum power consumption
- Controlled slew rate, limits inrush current at turn-on
- **Protects downstream circuitry from being supplied voltage lower than intended**
- Ultra-small package ideal for space constrained applications



V | Five Years Out

CC3100 SimpleLink™ WIFI

Features

- On-chip Internet & Wi-Fi security
- Wireless MCU separate from TCP/IP Stack, free for customer applications
- Flexible provisioning: AP mode, WPS, SmartConfig and more
- Cloud supported
- FCC/CE/ETSI/TELEC certified modules
- SDK for development with Code Composer Studio and IAR support

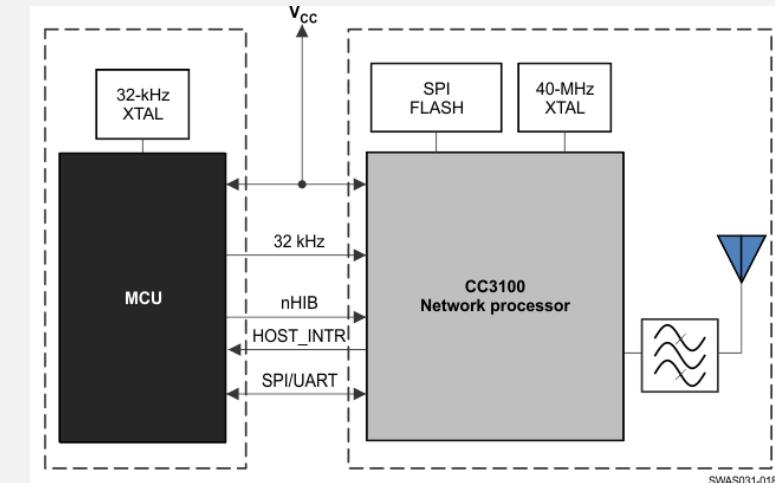
Applications

\$6.70 @ 1Ku

- Internet of Things (IoT)
- Home automation & appliance
- Safety and security
- Smart energy
- Industrial M2M communication
- Wireless audio streaming

Benefits

- **The lowest power:** Run for over a year on two AA batteries
- **First single chip programmable Wi-Fi solution:** Add Wi-Fi to any system
- **Easiest to design with:** No Wi-Fi experience needed; HW designs, 30+ software examples, extensive documentation and TI E2E support forum all readily available



SWAS031-018



CC2650 SimpleLink™ BLE

Features

- Lowest Power down to 1/10th of BT Classic
- Run BT stack and application on one single chip down to 6x6mm QFN package
- Bluetooth 4.1 compatible
- Industrial and extended temp range: -40 to 85°C and 125°C
- Automotive qualification option

Applications

\$6.30 @ 1Ku

- IoT – Connect cloud devices, mobile phones or tablets
- Home/Building Automation – security systems, lighting
- Health, Medical, Fitness, Wearables
- Retail - Locationing, Beacon
- Smart Grid – Battery operated devices

Benefits

- **Easiest to design with** – Get faster to market: Complete SW stack, wiki guides, dynamic design kits, low-cost tools, & software starting points
- **Lowest power** – Use a coin cell for multi-year, always-on operation or go battery-less with energy harvesting
- **Most integrated wireless MCU** – Less board space, more possibilities, single-chip Flash-based, 4x4 QFN



DECA Evaluation Board

Partner Solutions

Clocks and Timing Devices



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Si114x Optical Sensors

- Highest sensitivity and longest range proximity sensing
 - Up to 2 meters indoors
 - Up to 500mA LED drive
- High accuracy heart rate for wearables
- Lowest power consumption
 - Fast single pulse 25.6 μ s LED duty cycle
 - Once per second ALS at 0.6 μ A, UV at 1.2 μ A
- Advanced 2D and 3D gesture detection
 - Up to three independent LED drivers
- Integrated ambient light sensor (ALS)
 - High dynamic range from <0.1 to 125k lux (direct sunlight)
- Tiny 2 x 2 mm QFN



**Wearable
Heart Rate and
UV
Applications**



**Control panel
wake up on user
detection and
display
brightness**



**Gesture
Applications**



Clocks, Buffers and Oscillators

■ Si5350 - Perfect for clock consolidation

- Replaces 3-8 xtals, XOs, VCXOs with one small part
- Lower power, smaller footprint than competition
- Best in class jitter performance

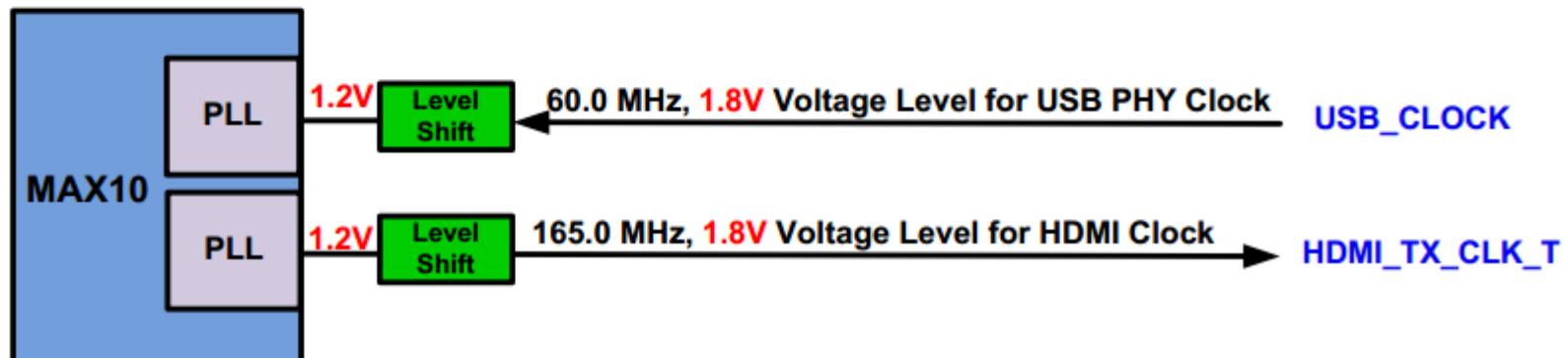
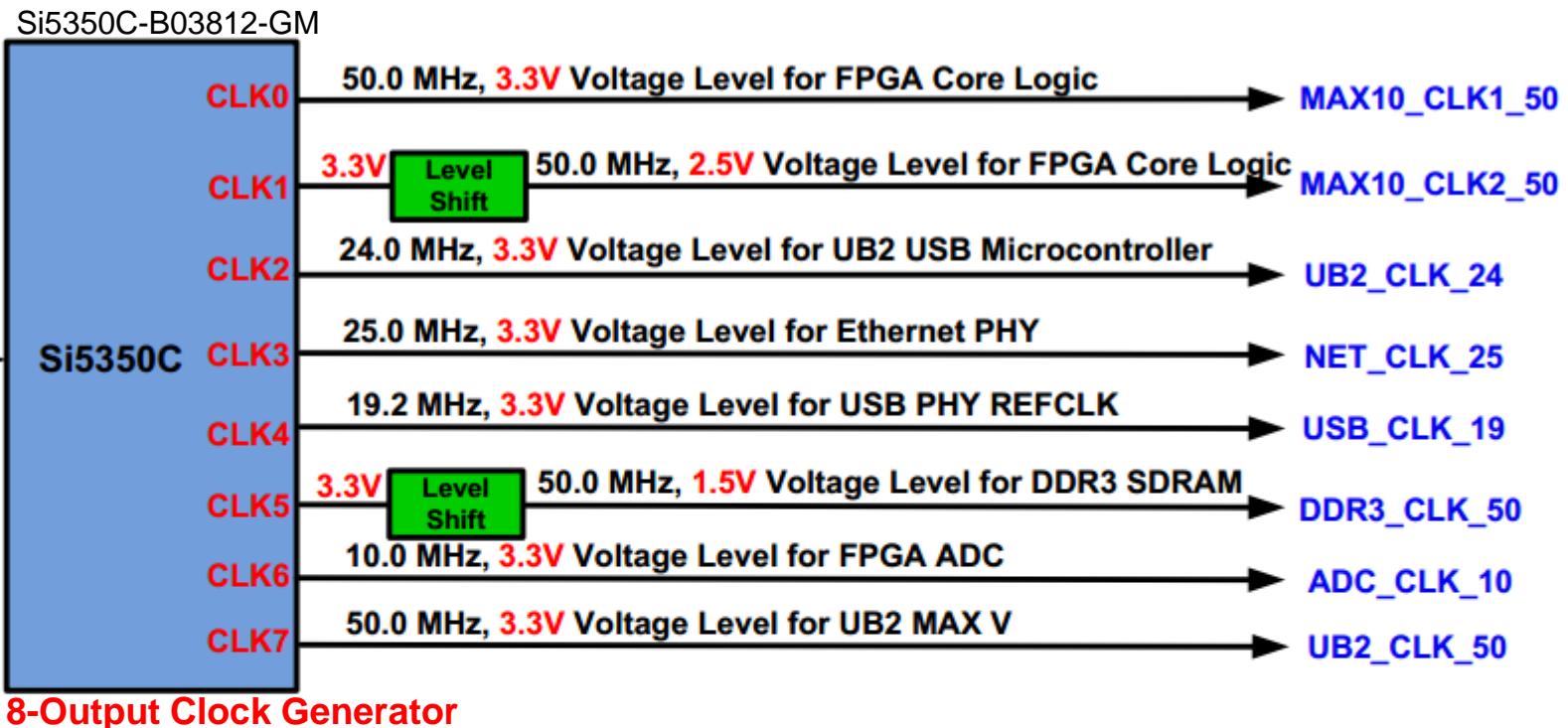
www.silabs.com/custom-timing



■ Si55301-06 – Level-Translating Buffers

- Single IC delivers multi-level clock outputs

DECA Clock Tree



DECA Evaluation Board

Partner Solutions

Connectors and
Expansion Headers



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100% of the connectors on DECA are from Molex!

Description	Part Number
RJ45 Modjack w/LED's and Integrated Magnetics	48074-9001
USB Mini-B Receptacle	54819-0519
USB Mini-AB Receptacle	56579-0519
HDMI Receptacle	47151-0001
microSD Card Socket Push-Pull Type	504077-1891
SMA 50 Ohm PCB Mount Jack Receptacle	73391-0070
Dual Row 46 Position Receptacle	90151-2246

DECA Evaluation Board

Partner Solutions

Memory
DDR3 & QSPI Flash



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Micron Memories

DRAM

- Broadest DRAM Portfolio in the Industry!

Product Family	Product Availability
SDRAM	64Mb/128Mb/256Mb; IT & AT available
DDR SDRAM	256Mb/512Mb; IT & AT available
DDR2 SDRAM	512Mb/1Gb/2Gb; IT & AT available
DDR3 SDRAM	1Gb/2Gb/4Gb/8Gb; IT & AT available
DDR4 SDRAM	4Gb now; 8Gb + IT/AT options in 2015
DRAM Modules	SDR to DDR3; 12 module form factors
RLDRAM2	288Mb/576Mb; IT available
RLDRAM3	576Mb/1.15Gb; IT available
LPDDR	50nm & 30nm available
LPDDR2	50nm & 30nm available
LPDDR3	25nm & 30nm available
LPDDR4	8Gb only – 25nm

- Supporting DRAM for Industrial, Automotive, Networking applications

Serial NOR

- Serial Peripheral Interface (SPI) or Serial
 - Multi I/O interface: x1 – x2 – x4
- N25Q/MT25Q (32Mb-2Gb available now)
 - High performance SPI with leading edge technology
 - Advanced security features
- Compatible with other SPI suppliers

Application Requirements	1Mb to 16Mb	32Mb to 256Mb	512Mb to 2Gb
Standard SPI	M25P	N25Q	MT25Q
Parametric Storage	M25PE		
Data Storage	M45PE		
Dual IO	M25PX	N25Q	MT25Q
Hi-Performance, XiP, 3V		N25Q	MT25Q
Low Power (1.8V)	N25Q	N25Q	MT25Q

Micron's Value Add!

- Product Longevity Program for customers with 7-10+ years product life cycles
- Micron feature strength in key markets
 - Automotive quality and temp products
 - Networking innovation in RLDRAM and HMC
 - Longevity on Legacy Products (SDR/DDR)



DECA Evaluation Board

Partner Solutions



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CapSense MBR3 Family

Applications

Industrial control panels
 White goods, small home appliances
 Keypads
 Elevator controls
 TVs, monitors
 Music players
 Mobile phones, tablets

Features

Up to 16 buttons, or 8 buttons and 8 LEDs
 Up to two 5-segment sliders
 SmartSense™ Auto-tuning eliminates manual tuning
 Proximity sensing of up to 30 cm
 LED control
 Buzzer output
 Liquid Tolerance
 Register-Configurable with EZ-Click™ software tool
 Wide operating voltage: 1.71-5.5 V
 Packages: 8-pin SOIC, 16-pin QFN, 16-pin SOIC, 24-pin QFN

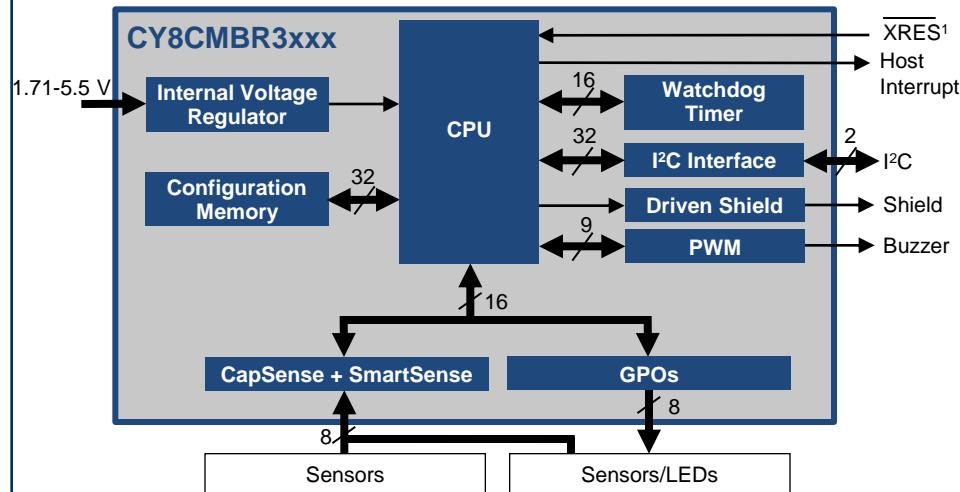
Collateral

Datasheet and Design Guide are available at
www.cypress.com/CapSenseMBR3

Family Table

MPN	CapSense Buttons	GPOs	Proximity Sensors	Communication Interface	Buzzer
CY8CMBR3002-SX1I	2	2	-	GPO I ² C	N N
CY8CMBR3102-SX1I	2	1	2	I ² C	Y
CY8CMBR3108-LQXI	8	4	2	I ² C	Y
CY8CMBR3110-SX2I	10	5	2	I ² C	Y
CY8CMBR3106S-LQXI	11	0	2	I ² C	Y
CY8CMBR3116-LQXI	16	8	2	I ² C	Y

Block Diagram



Availability

Sampling: Now
 Production: Now

¹ External reset

Arrow's BLE/WIFI module



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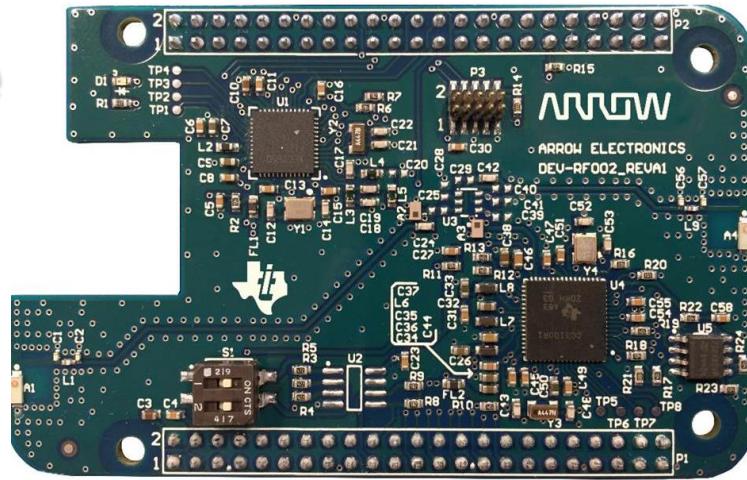
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Arrow's BLE/WIFI module

- IoT add-on card compatible with both Arrow's DECA and TI's Beaglebone Black
- WIFI
 - TI's CC3100
 - Dedicated Chip Antenna
- Bluetooth Low Energy
 - TI's CC2650
 - Dedicated Chip Antenna and CJTAG Programming header
- Configurable for BLE and WIFI to share single chip antenna



Designed by



Dallas Logic

Dallas Logic Overview



- Turn-key services – concept to production
 - Board level, FPGA and software design services
 - Rapid prototyping
 - Enclosure design
 - Manufacturing
- RF design capabilities
 - Wi-Fi, Bluetooth Low Energy, Zigbee etc...
 - We can manage your FCC compliance testing
- Analog frontend design and high speed data interfacing
- Embedded software and application development
- Domestic operations –McKinney, Texas (Founded in 2001)
- www.dallaslogic.com



3rd Party IP and Design Partners



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System Level Solutions (SLS)

■ Integration Specialist with these services:

- IP Cores
- FPGA Design
- Embedded Software and Firmware
- Hardware Design
- PCB Design
- Windows Driver & Application Software
- Linux Driver



■ Wide IP portfolio includes

- SDHC (on DECA)
- USB 2.0 (on DECA)



IP Cores

- Communication
 - USB2.0 (Device / Host / OTG)
 - USB3.0 (Device)
 - eUSB3.0 (Device with Altera Transceiver)
 - Ethernet MAC (10/100)
- Interface
 - I2C Master / Slave / Controller
 - I2S Controller
- Memory
 - SD/eMMC
 - ONFI / NAND
- Display
 - VGA / LCD Controller
- Processor
 - 8051
 - Intel 196 (80c196)
- Many more.....

3rd Party IP and Design Partners



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Northwest Logic Overview

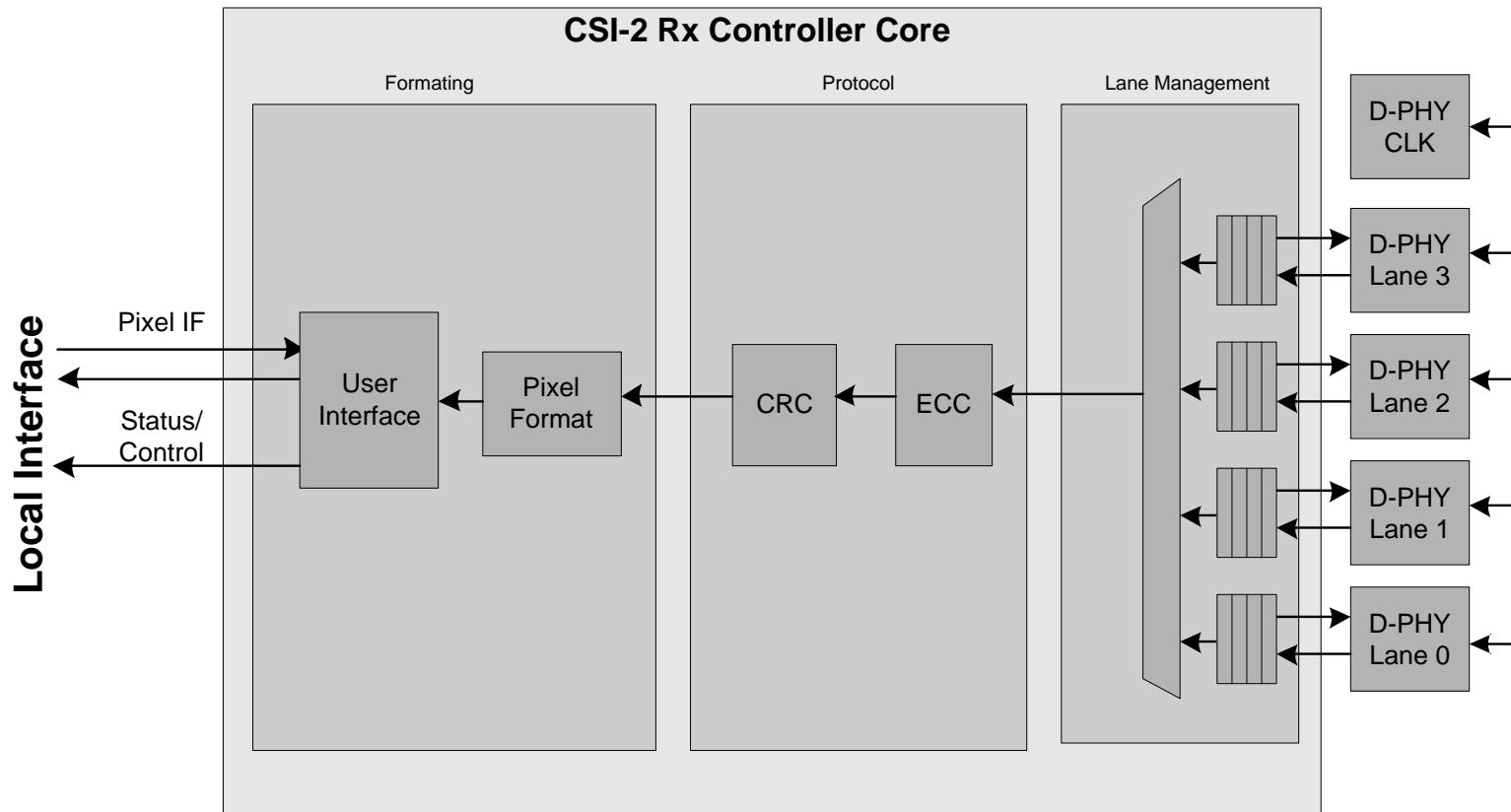
- Founded in 1995
 - Located in Beaverton, Oregon
- Provide IP Cores
 - Memory Interface Solution
 - PCI Express Solution
 - MIPI Solution
 - Peripheral Cores
- Complete Cross-Platform Support
 - Standard Cell ASIC
 - Structured ASIC
 - FPGA
- Supplement with Design Services
 - IP Core Customization
 - Logic, Board, Software Services



MIPI – Why Use Our IP Cores?

- Silicon-proven, high-quality cores
- High performance – high throughput, high clock rate, low latency
- Easy to use - simple user interface, easy to configure, etc.
- Optimized for use in ASICs and FPGAs
- Fully hardware validated
- Provided with a full featured Testbench
- Development boards and driver support available
- Available as source code
- Core license includes expert technical support
- Customization and integration services available
- Widely used - references available

MIPI – CSI-2 Rx Controller Core Architecture



MIPI – CSI-2 Controller Core Key Features

- High-performance, easy-to-use core
- Fully CSI-2 Specification compliant
- Implements all 3 CSI-2 MIPI Layers (Pixel to Byte packing, Low Level Protocol, Lane Management)
- Transmitter and Receiver Versions
- Support 1-8 data lanes
- Support all data types
- Operates using Byte Lane Clock
 - Minimizes power and timing closure challenges
- Single, double or quad pixel user interface
 - Optional Hsync/Vsync video interface
- Error injection/collection support
- Delivered fully integrated with target MIPI PHY
- Minimal ASIC gate count
- Easy configuration and control via core ports
- Provided as source code
- Provided with expert technical support
- Provided with a CSI-2 Testbench
- Customization and integration services available
- FPGA-Based Demo System available

For More Information

- Visit our website at: www.nwlogic.com
 - More information on Products and Capabilities
- Use website to generate Info Request
 - Will provide access to secure section of the website
 - Has all of the product datasheets, app notes, user guides, etc.
- Contact Brian Daellenbach at:
 - briand@nwlogic.com
 - 503-533-5800 x309

3rd Party IP and Design Partners



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About Terasic

- Founded in 2003 at Hsinchu, Taiwan.
- Provides advanced FPGA-based solutions for many world-leading companies - **GE-Health, Boeing, US Dept of Energy, DOD, Gaming, Finance Industry.**
- Altera Contract Manufacturer for **Altera Dev. Kits**
- Altera University Program Partner - Terasic **designed and made ALL Altera University Program Kits and reference designs.**
- Intel Cedarview Platform Design Partner
- Provided MIPI IP for DECA
- Designed Schematic and PCB for DECA

Lab Overview



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DECA Workshop Objectives

- What you should take away from today's labs:
 - A working knowledge of Quartus II and Qsys
 - A working knowledge of the Nios II software flow using Eclipse
- Explore many of the different sensors and interfaces available on DECA
- Walk away with a development kit you use for future projects

Choose your own lab adventure

	Lab Name	Target Audience	Time
1	FPGA Intro Lab	Beginner	1:00
2	Qsys Intro Lab	Beginner	0:30
3	Embedded Systems Lab	Nios II Beginner	2:30
4	Gesture Sensor Lab	Beginner to Intermediate	0:45
5	Data Capture using the MAX 10 ADC's	All users	1:00
6	USB 2.0 to SDHC (Mass Storage)	All users	0:30
7	Interact with DECA using BLE and WIFI on your Smartphone	All users	0:45
8	CMOS image capture using the MIPI camera interface and output to HDMI	Advanced	1:00
9	Boot Linux on DECA	Advanced	0:30

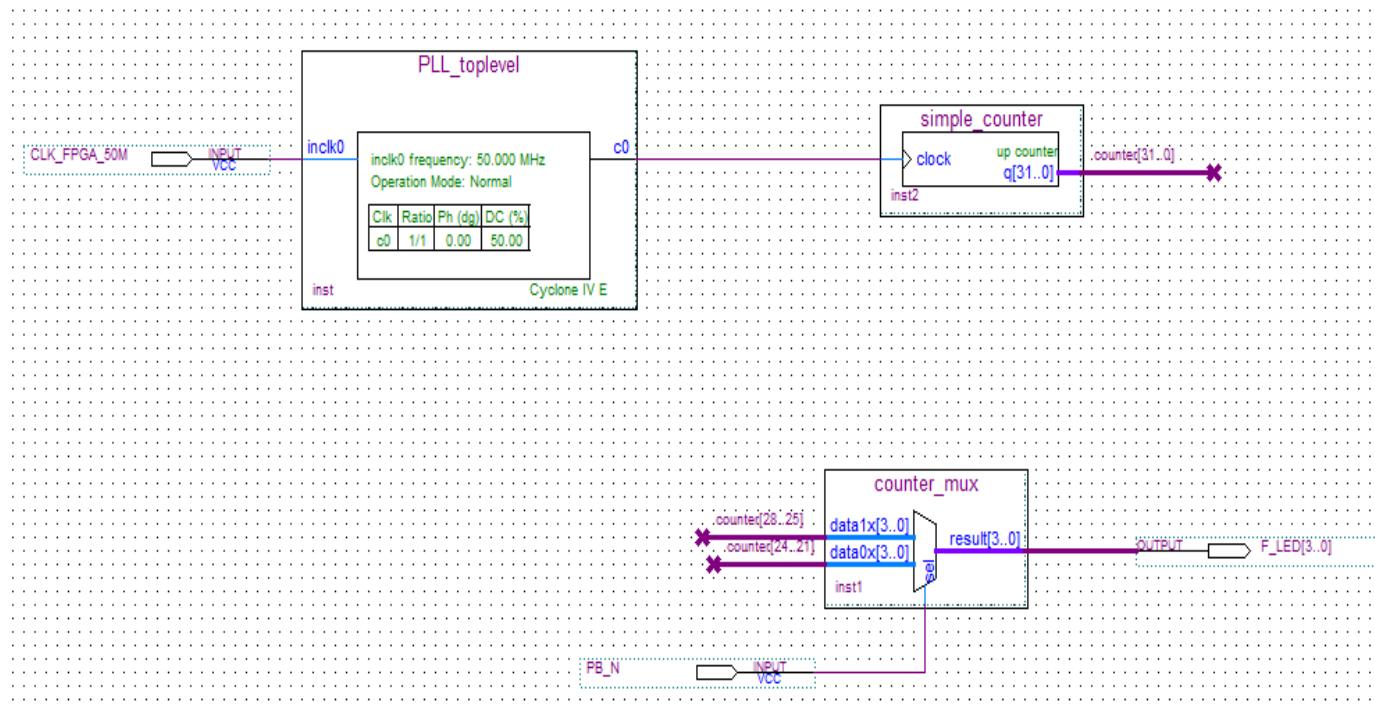
FPGA Intro Lab: Going over the basics

1

- A step-by-step guide to FPGA design using Quartus II
- No previous knowledge of Quartus II or FPGA design flow is required or assumed

FPGA Intro Lab: Going over the basics

- Build up the following design, add pin and timing constraints, compile, download and test the design



Qsys Introduction Lab, using System Console to display the board temperature

2

- Introduction to the Qsys design flow and how to use System Console
- No previous knowledge of Quartus II or FPGA design flow is required or assumed
- Build a system with LED's, push-buttons, and temperature sensor interface allowing you to view and update registers using System Console

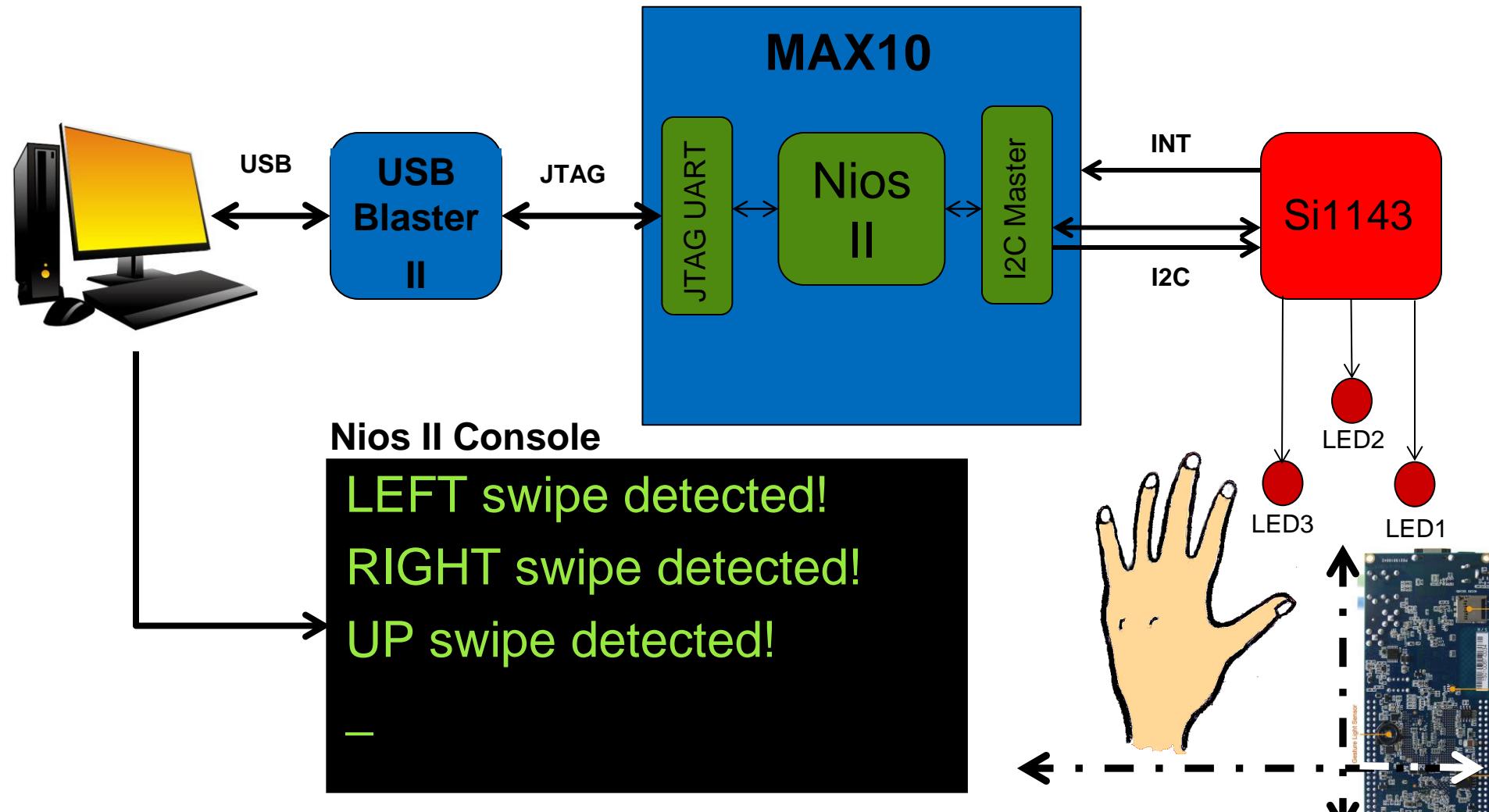
Embedded Systems Lab

- Build a Nios II Gen 2 processor system from scratch using Qsys
- Nios will interact with several sensors on the board in this lab
- Step-by-step guide for a complete system design

Gesture Sensor Lab

- Interact with the Si1143 Gesture Sensor
- Hardware Tasks
 - Create a Quartus II project
 - Create a simple Qsys system including a Nios II processor
 - Connect important signals in the top level design
 - Compile the project
 - Download the configuration file to the DECA
- Software Tasks
 - Create a project in Eclipse
 - Generate a BSP
 - Compile the console application
 - Run the application on the target Nios II processor
 - Wave your hands around to see them recognized!

Gesture Lab Block Diagram



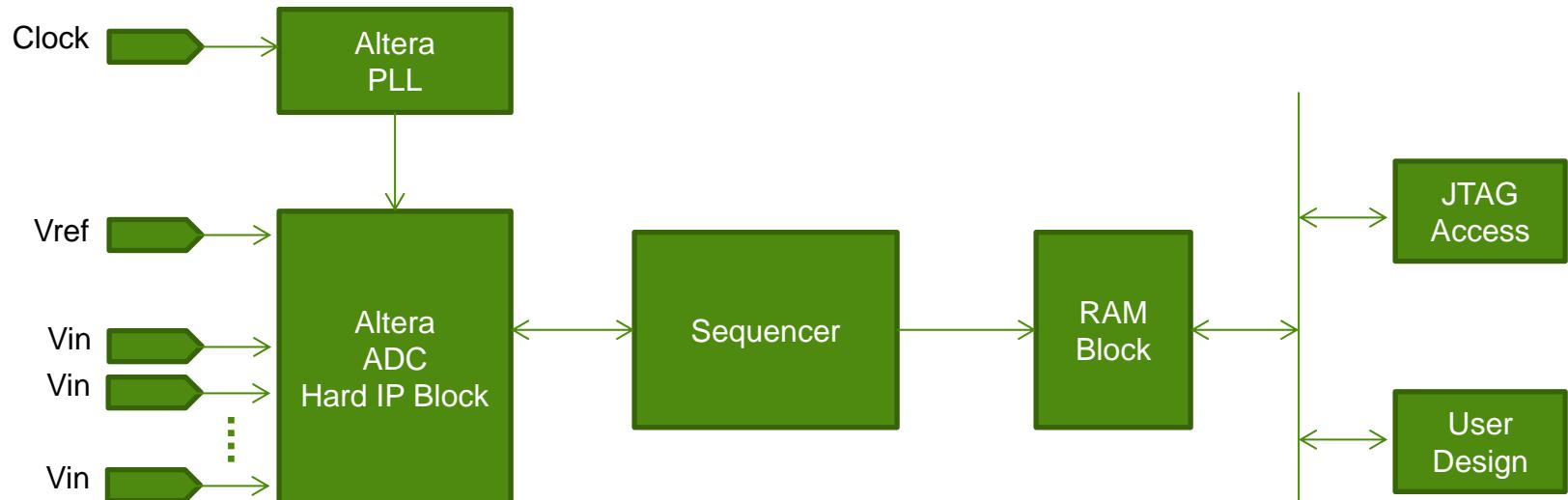
Analog Data Converter

■ Objective

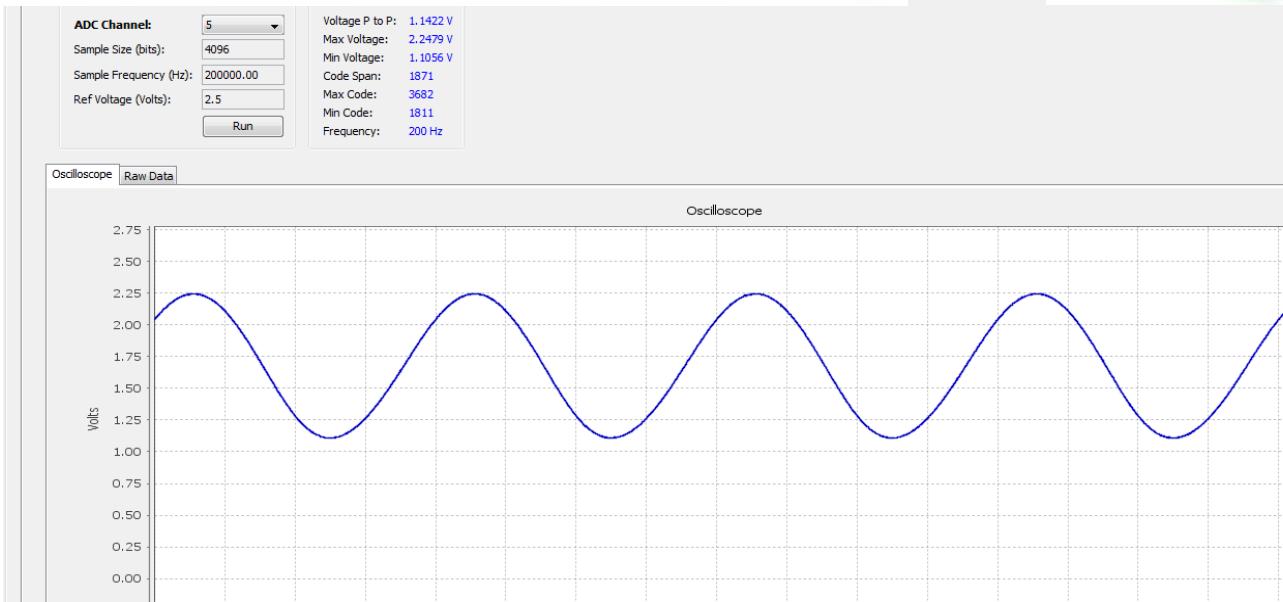
- Learn about the basic architecture and configuration options for the MAX 10 ADC.

■ Tasks

- Implement the MAX 10 ADC hard IP in an FPGA design
- Use Altera's ADC Toolkit to monitor and analyze the analog inputs
- Read the ADC data using a simple Nios software application



ADC Lab Setup

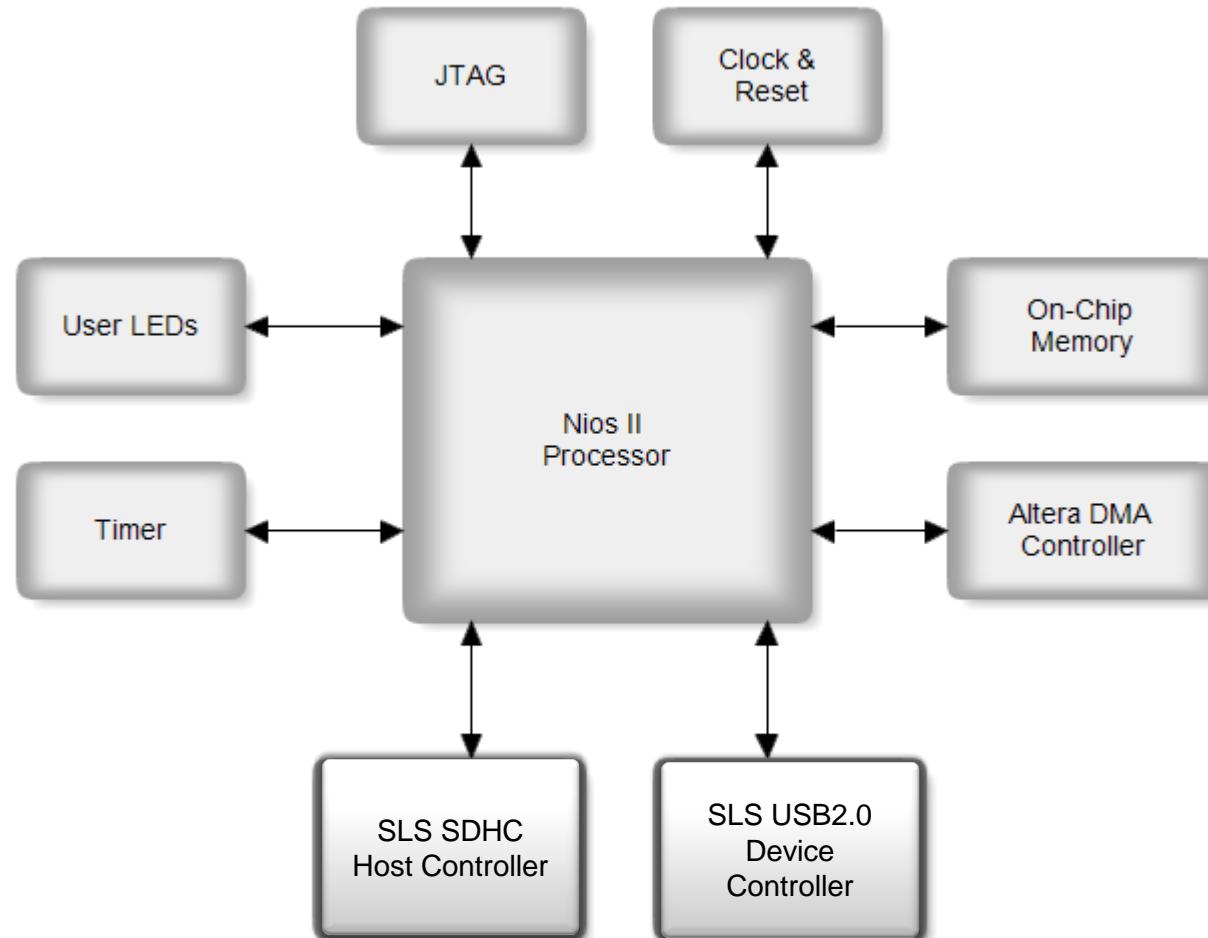
**NIOW****ALTERA**® **TEXAS INSTRUMENTS****Five Years Out**

USB 2.0 to SDHC LAB

- USB Mass Storage example design
- The DECA board with an SDHC card inserted will show up in Windows as a mass storage device
- Objective
 - Understand the dataflow of the SLS IP
- Tasks
 - Review the SLS IP and Qsys connections
 - Compile Nios II code
 - Target the design using the generated executable file (.elf)

USB 2.0 to SDHC LAB

■ Block Diagram



Interact with DECA using BLE and WIFI on your Smartphone

7

- Review high-level architecture of the DECA board and BLE/WIFI add-on module
- Walk through the design flow needed to implement a BLE/WIFI design
- Demo both the BLE and WIFI communication
 - WIFI demo based on CC3100 (TI)
 - Simple Web-server
 - BLE demo based on CC2650 (TI)
 - Interactive demo with your Smartphone

BLE / WIFI – Walkthrough lab

WIFI

- Setup the SSID of the Access Point (AP)
- Connect your phone to the AP
- Visit specific web-page (192.168.1.1 , or mysimplelink.net)
- Interact with web-page to display temperature, humidity, and g-sensor raw data, or
- Use web-page buttons to drive LED's

BLE

- Download Android or IOS app for your Smartphone
- Pair Bluetooth to CC2650 BLE device
- Launch BLE tool (Android) to read raw data

BLE WIFI – Web-page and App

Connect to both BLE and WIFI
using your Smartphone or laptop



- [Status](#)
- [Accerometer, Temperature & Humidity](#)
- [LED & Push Button](#)

WIFI BLE Info

Temperature:	<input type="text"/>
Humidity:	<input type="text"/>
X-axis:	<input type="text"/>
Y-Axis:	<input type="text"/>
Z-Axis:	<input type="text"/>



BLE Tool

Action+ Tools

i This app is compatible with some of your devices.

g+1 9

Services : 2

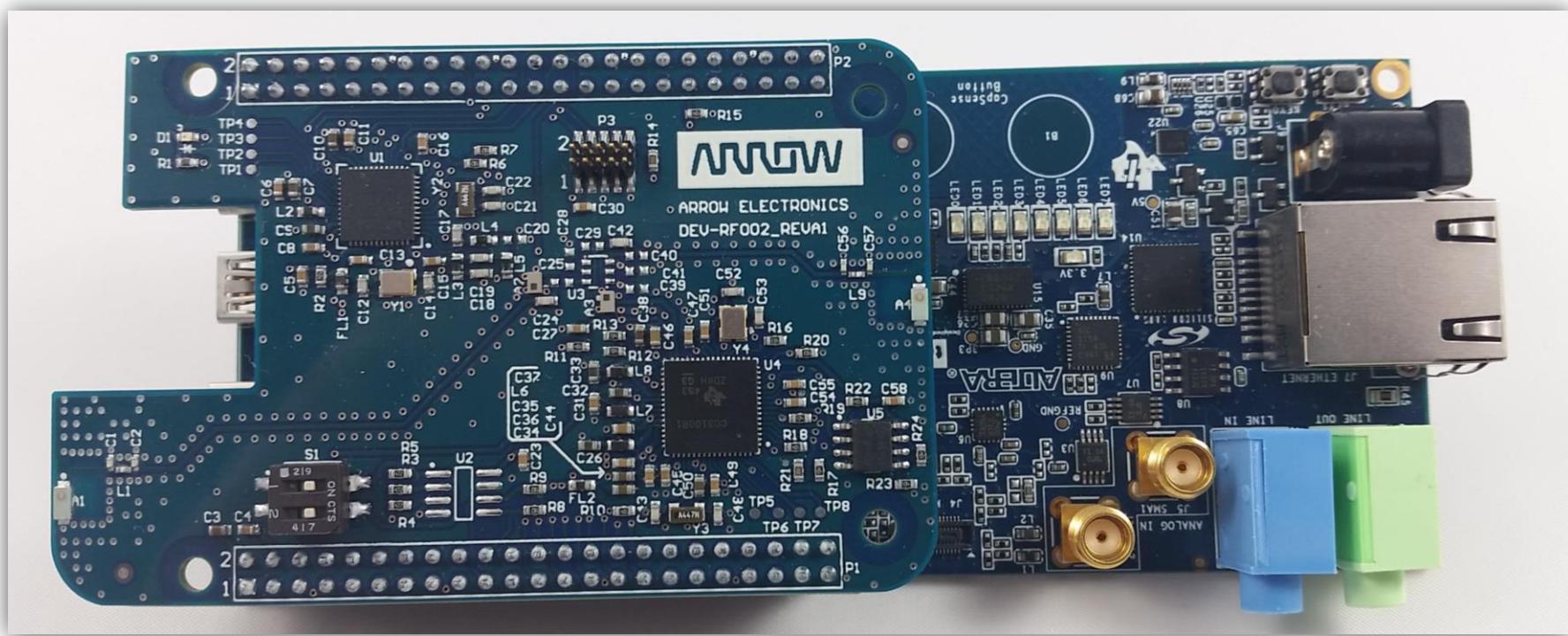
1800	Generic Access
2a00	Device Name
2a01	Appearance
2a02	Peripheral Privacy Flag
2a03	Reconnection Address
2a04	Peripheral Preferred Connection Parameters
1801	Generic Attribute
2a05	Service Changed
180d	Heart Rate
2a37	Heart Rate Measurement
2a38	Body Sensor Location
2a39	Heart Rate Control Point
180a	Device Information
2a23	System ID

Services : 2

1800	Generic Access
2a00	Device Name
2a01	Appearance
2a02	Peripheral Privacy Flag
2a03	Reconnection Address
2a04	Peripheral Preferred Connection Parameters
1801	Generic Attribute
2a05	Service Changed
180d	Heart Rate
2a37	Heart Rate Measurement
2a38	Body Sensor Location
2a39	Heart Rate Control Point
180a	Device Information
2a23	System ID

DECA with BLE/WIFI Cape

7



Five Years Out

CMOS Image Capture using the MIPI Camera Interface and Output to HDMI

- Configure a Qsys system to add a video pipeline to the design
- Run some Nios II software using Eclipse to configure and run the Video IP
- This lab will be step-by-step and there is no previous knowledge of Quartus II or Eclipse required

Boot Linux on DECA

- This will be more of a demonstration than an actual lab.
- Customers can connect to the development kit over Ethernet and launch a `hello_world` design that toggles the LEDs or perhaps reads one of the sensors on the board.

Getting Started



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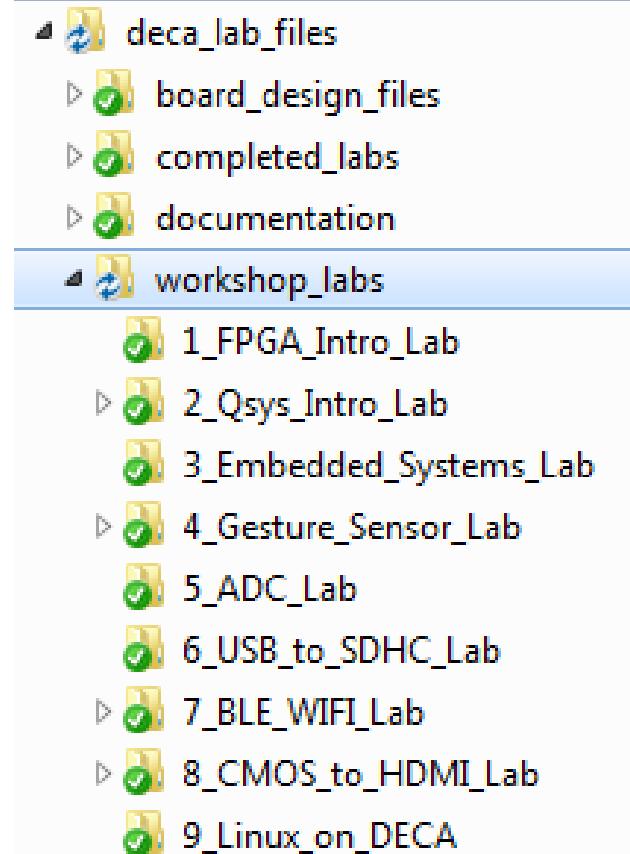
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Getting Started!

- Copying files from USB stick, or download from our [website](#)
- Pick three labs to complete
- Review the lab material before you begin
- Ask questions!
 - Don't hesitate
- The starting point for today's labs are in the subfolder titled workshop_labs



Lab List and Time Estimate

	Lab Name	Target Audience	Time
1	FPGA Intro Lab	Beginner	1:00
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8	CMOS image capture using the MIPI camera interface and output to HDMI	Advanced	1:00
9	Boot Linux on DECA	Advanced	0:30

Thank You



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