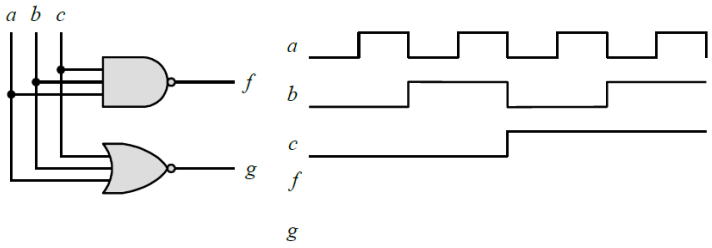
CPE 487 Midterm Exam (100 Points)

Due: October 18, 12:30pm

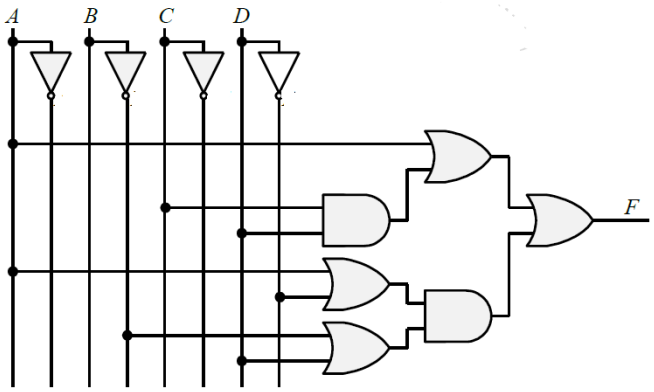
Signed _____ Date _____

Part1: By hands only

1. Complete the timing diagram of the following circuit by adding the timing trace for **f** and **g**:



2. Write Boolean expression for the following circuits:

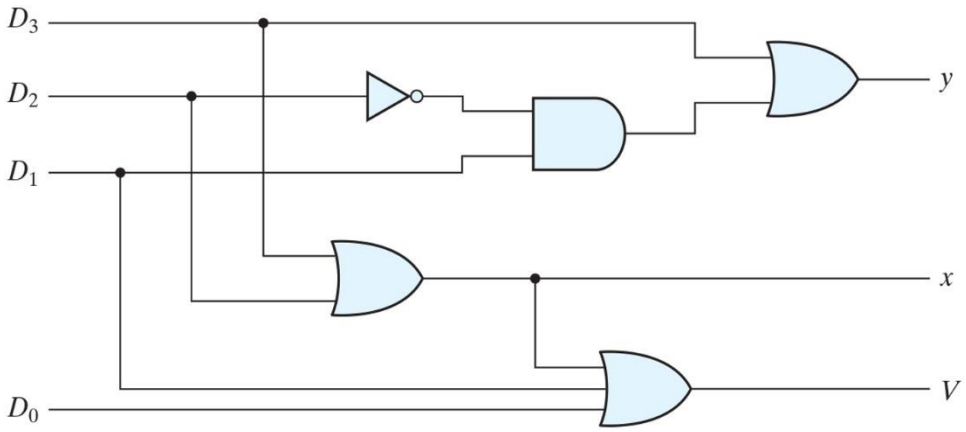


3. Draw the logic diagram corresponding to the following Boolean expression:

(AB + A'B')(CD' + C'D)

Part 2: Using Vivado

4. Use Vivado to write VHDL gate-level description encoder circuit shown below



5. Write behavioral (testbench) description of a four-input encoder circuit shown in #4, above.