Midterm Part 2

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October 25, 2022

I pledge my honor that I have abided by the Stevens Honor System.

Shiddharath Patel

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Purpose:

This lab's goal was to demonstrate how to use questions 4 and 5 in Vivado. After developing the necessary code to answer the problems, the code is uploaded to an FPGA board to validate the code for the midterm assignment and to gain experience interacting with hardware.

Data Collected:

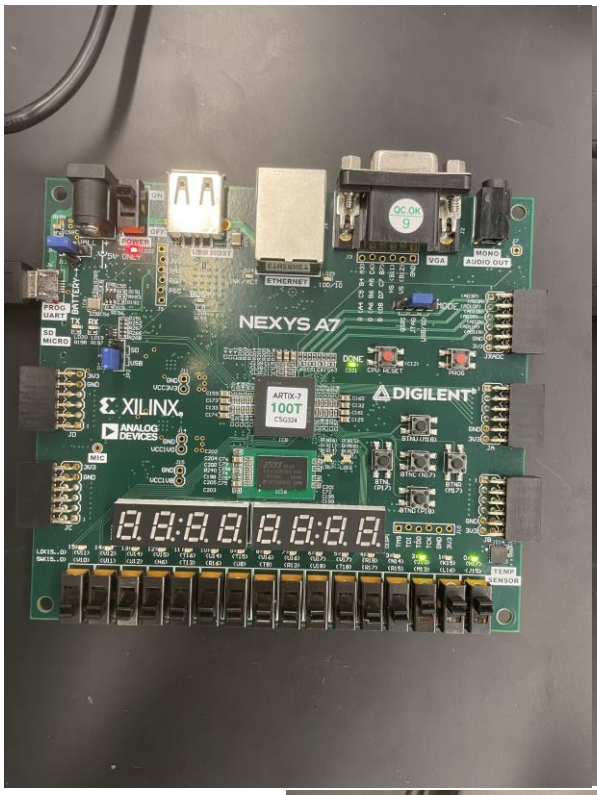
The VDHL code's output from Vivado demonstrated a connection between the four inputs and three outputs.

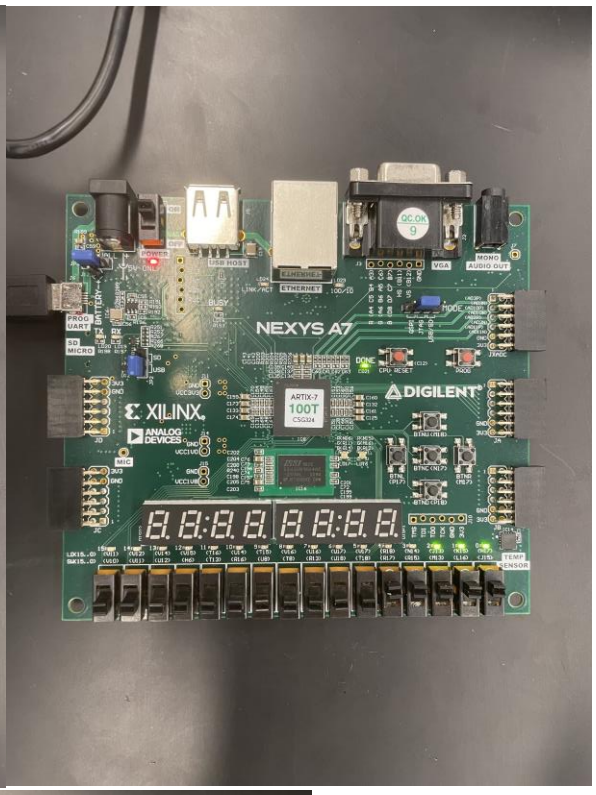
Calculation Truth Table:

D_0	D_1	D_2	D_3	x	y	V
0	0	0	0	0	0	0
1	0	0	0	0	0	1
0	1	0	0	0	1	1
1	1	0	0	0	1	1
0	0	1	0	1	0	1
1	0	1	0	1	0	1
0	1	1	0	1	0	1
1	1	1	0	1	0	1
0	0	0	1	1	1	1
1	0	0	1	1	1	1
0	1	0	1	1	1	1

Result Schematics and Waveforms:

The values in the table match the green blocks that are shown in the waveform output. In addition to the time output, which is the answer to question 5, the code from question 4 also produces the Circuit schematic. The group was able to successfully upload the code to the FPGA board using the three initial LEDs x, y, and V as well as the four initial LEDs. The three first LEDs were used as x, y, and V together with the four initial switches to achieve a successful outcome after uploading the code to the FPGA board. Below are some combinations shown in the FPGA board operating on the midterm program.


NEXYS A7
XILINX
DIGILENT
ANALOG DEVICES
ARTIX-7
100T
ETHERNET
VGA
MONO AUDIO OUT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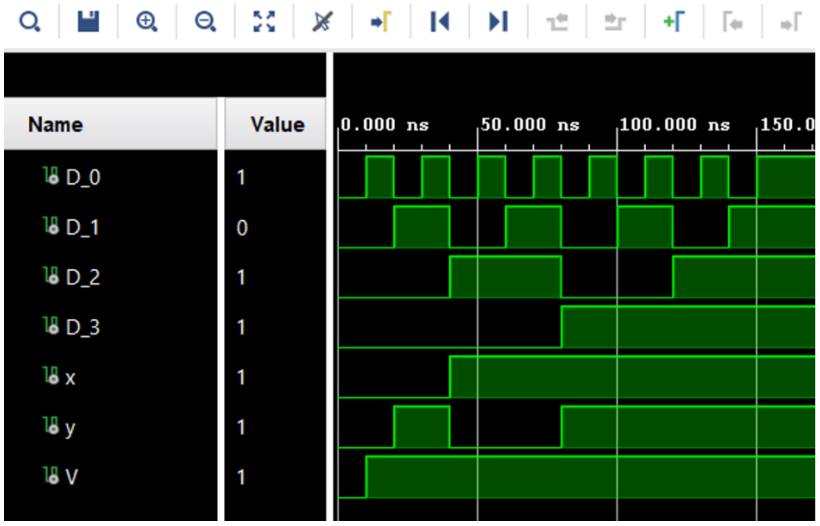
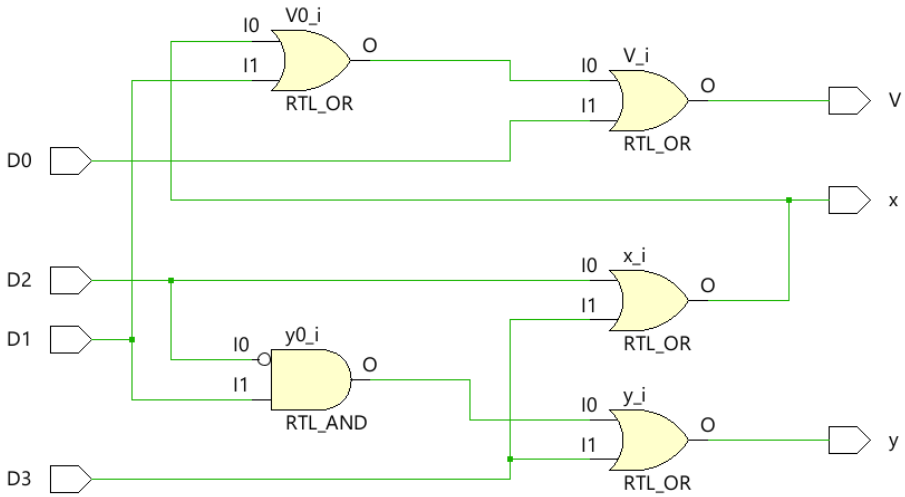


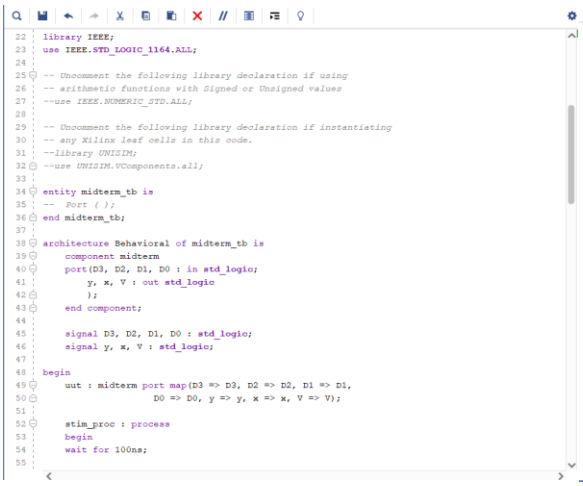


Conclusion:

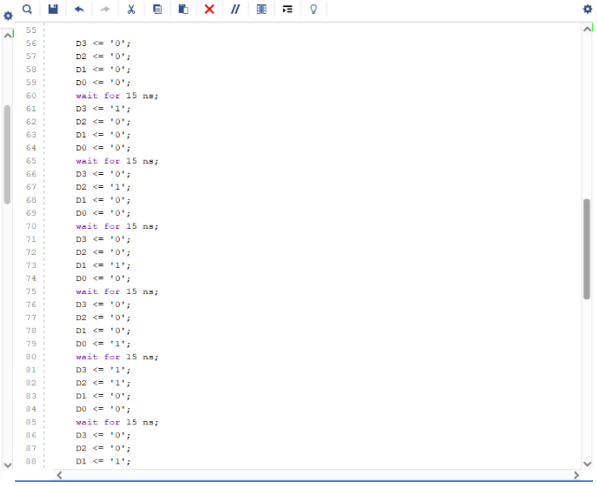
The outcomes of this lab confirmed the validity and compatibility of the code created for questions 4 and 5 on the midterm with an actual FPGA board. As can be seen from the manual calculations, Vivado was able to provide the desired outcome in the allotted time. Additionally, tweaking the physical switches after putting the code onto the FPGA board had positive results, displaying the outputs using LED lights that were comparable to the time output in the simulation. The team was able to evaluate its code and gain experience with hardware and software.

Source Code:

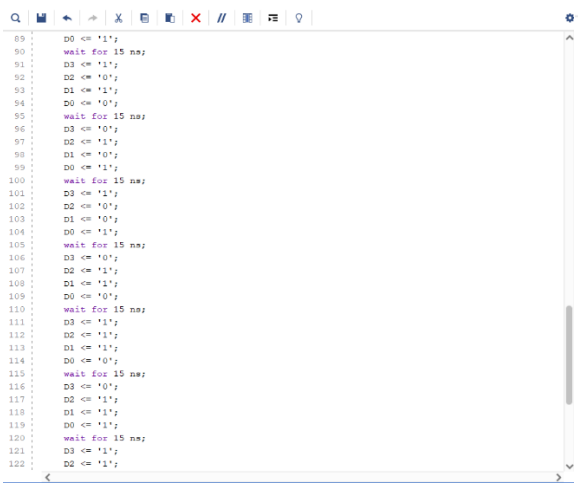
```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;

-- Uncomment the following library declaration if using
-- arithmetic functions with Signed or Unsigned values
--use IEEE.NUMERIC_STD.ALL;

-- Uncomment the following library declaration if instantiating
-- any Xilinx leaf cells in this code.
--library UNISIM;
--use UNISIM.VComponents.all;

entity midterm is
    Port ( D0 : in STD_LOGIC;
           D1 : in STD_LOGIC;
           D2 : in STD_LOGIC;
           D3 : in STD_LOGIC;
           y : out STD_LOGIC;
           x : out STD_LOGIC;
           V : out STD_LOGIC);
end midterm;

architecture MidtermFunction of midterm is

begin

    y <= ((not(D2) and D1) or D3);
    x <= (D2 or D3);
    V <= ((D2 or D3) or D1 or D0);

end MidtermFunction;
```



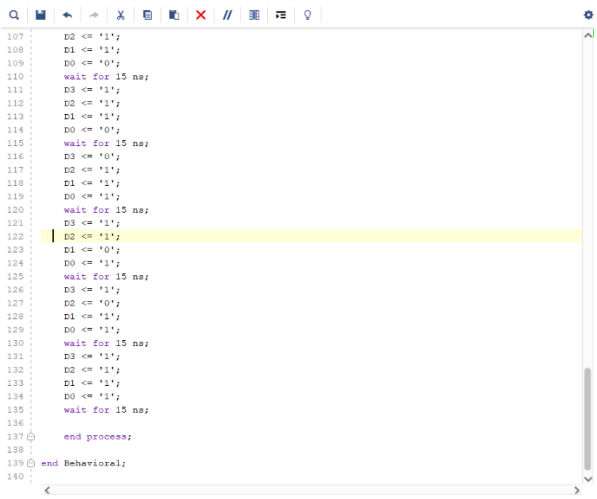
```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;

-- Uncomment the following library declaration if using
-- arithmetic functions with Signed or Unsigned values
--use IEEE.NUMERIC_STD.ALL;

-- Uncomment the following library declaration if instantiating
-- any Xilinx leaf cells in this code.
--library UNISIM;
--use UNISIM.VComponents.all;

entity midterm_tb is
--  Port ( );
end midterm_tb;

architecture Behavioral of midterm_tb is
    component midterm
    port(D3, D2, D1, D0 : in std_logic;
        y, x, V : out std_logic
        );
    end component;

    signal D3, D2, D1, D0 : std_logic;
    signal y, x, V : std_logic;

begin
    uut : midterm port map(D3 => D3, D2 => D2, D1 => D1,
                D0 => D0, y => y, x => x, V => V);

    stim_proc : process
    begin
    wait for 100ns;
```



```
    D3 <= '0';
    D2 <= '0';
    D1 <= '0';
    D0 <= '0';
    wait for 15 ns;
    D3 <= '1';
    D2 <= '0';
    D1 <= '0';
    D0 <= '0';
    wait for 15 ns;
    D3 <= '0';
    D2 <= '1';
    D1 <= '0';
    D0 <= '0';
    wait for 15 ns;
    D3 <= '0';
    D2 <= '0';
    D1 <= '1';
    D0 <= '0';
    wait for 15 ns;
    D3 <= '0';
    D2 <= '0';
    D1 <= '0';
    D0 <= '1';
    wait for 15 ns;
    D3 <= '1';
    D2 <= '1';
    D1 <= '0';
    D0 <= '0';
    wait for 15 ns;
    D3 <= '0';
    D2 <= '0';
    D1 <= '1';
```



```
    D0 <= '1';
    wait for 15 ns;
    D3 <= '1';
    D2 <= '0';
    D1 <= '1';
    D0 <= '0';
    wait for 15 ns;
    D3 <= '0';
    D2 <= '1';
    D1 <= '0';
    D0 <= '1';
    wait for 15 ns;
    D3 <= '1';
    D2 <= '0';
    D1 <= '0';
    D0 <= '1';
    wait for 15 ns;
    D3 <= '0';
    D2 <= '1';
    D1 <= '1';
    D0 <= '0';
    wait for 15 ns;
    D3 <= '1';
    D2 <= '1';
    D1 <= '1';
    D0 <= '0';
    wait for 15 ns;
    D3 <= '0';
    D2 <= '1';
    D1 <= '1';
    D0 <= '1';
    wait for 15 ns;
    D3 <= '1';
    D2 <= '1';
```



```
    D2 <= '1';
    D1 <= '1';
    D0 <= '0';
    wait for 15 ns;
    D3 <= '1';
    D2 <= '1';
    D1 <= '1';
    D0 <= '0';
    wait for 15 ns;
    D3 <= '0';
    D2 <= '1';
    D1 <= '1';
    D0 <= '1';
    wait for 15 ns;
    D3 <= '1';
    D2 <= '1';
    D1 <= '0';
    D0 <= '1';
    wait for 15 ns;
    D3 <= '1';
    D2 <= '0';
    D1 <= '1';
    D0 <= '1';
    wait for 15 ns;
    D3 <= '1';
    D2 <= '1';
    D1 <= '1';
    D0 <= '1';
    wait for 15 ns;

    end process;

end Behavioral;
```