Electronics/DAQ status

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Overview

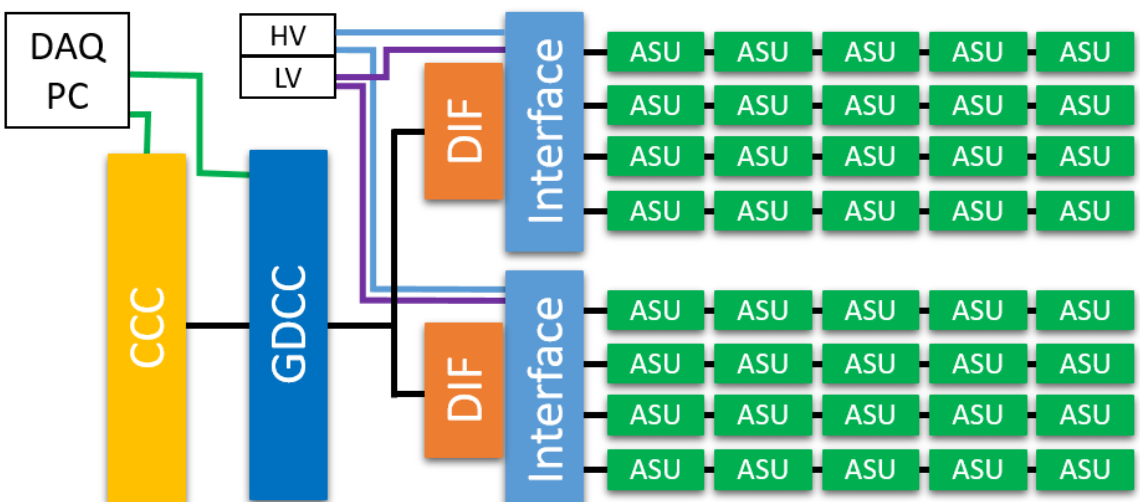
- Spill information implementation & Online monitor development
  - Basic system has been completed.

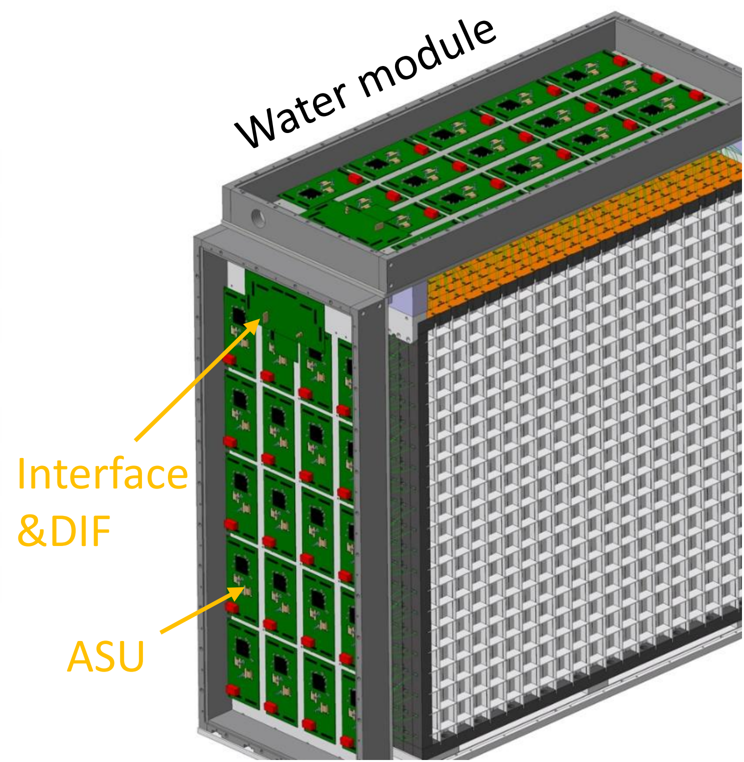
- Issue on the Interface board?
  - Failed to configure 20 ASUs on an Interface board.
  - Nets for slow control signals are suspected.

- What's remaining on electronics/DAQ development.
  - Solve electronics issues (probably on Interface board).
    - ✓ Then, measure all ASU boards for test operation and calibration.
  - Slow monitor
    - ✓ Power supplies (HV, LV), Water level sensor, Humidity sensor…
  - Prepare for data storage and offline analysis.
    - ✓ Including purchase of PCs.

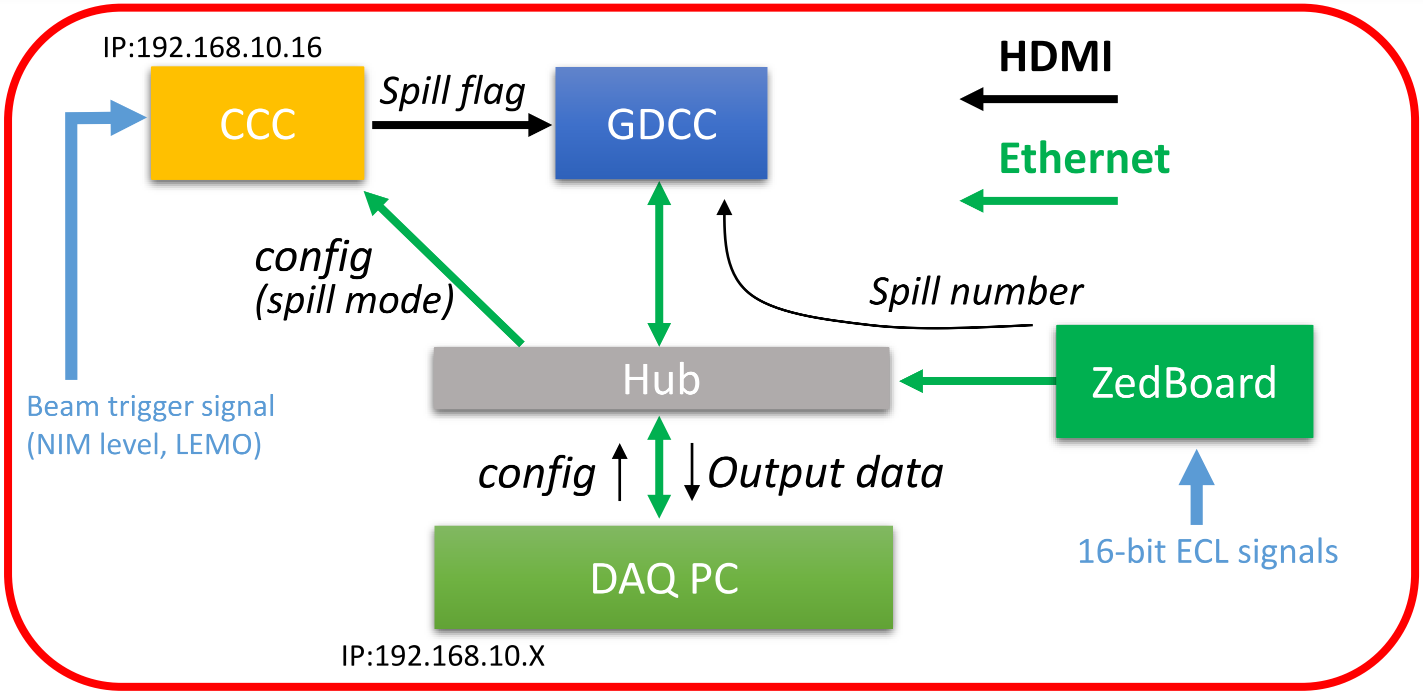
WAGASCI electronics

Electronics boards		Num /Mod
ASU (Active Sensor Unit)	Readouts a 32ch MPPC array with a SPIROC chip.	40
Interface	Transfers DAQ signals and MPPC bias voltage.	2
DIF (Detector InterFace)	Send DAQ signals and SPIROC configuration.	2
GDCC (Giga Data Concentrator Card)	Transfer signals between DAQ PC and DIFs.	1
CCC (Clock & Control Card)	Provides clock signals and fast control.	1

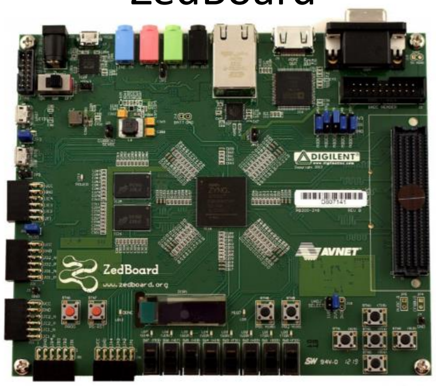




Spill Information Implementation



ZedBoard



- ***Spill flag*** : via HDMI

  Generated in the ***CCC*** firmware to its state.

  0x82 -> NU beam acquisition.

  0x92 -> Internal acquisition.

- ***Spill number*** : via Ethernet

  External 16-bit signal from beamline.

  ZedBoard receives it and send it on Ethernet.

➔ Filled into GDCC headers.

➔ Decoded with other DIF/SPIROC data.

Ethernet frame

- ***CCC*** : SiTCP

  using a fixed IP address.

- ***GDCC***, ***ZedBoard*** : Raw Ethernet frame

  only using MAC addresses.

  0x0809 -> Fast Command Packet

  0x0810 -> Normal GDCC Packet

  0x0811 -> DIF Data Packet

Raw data format

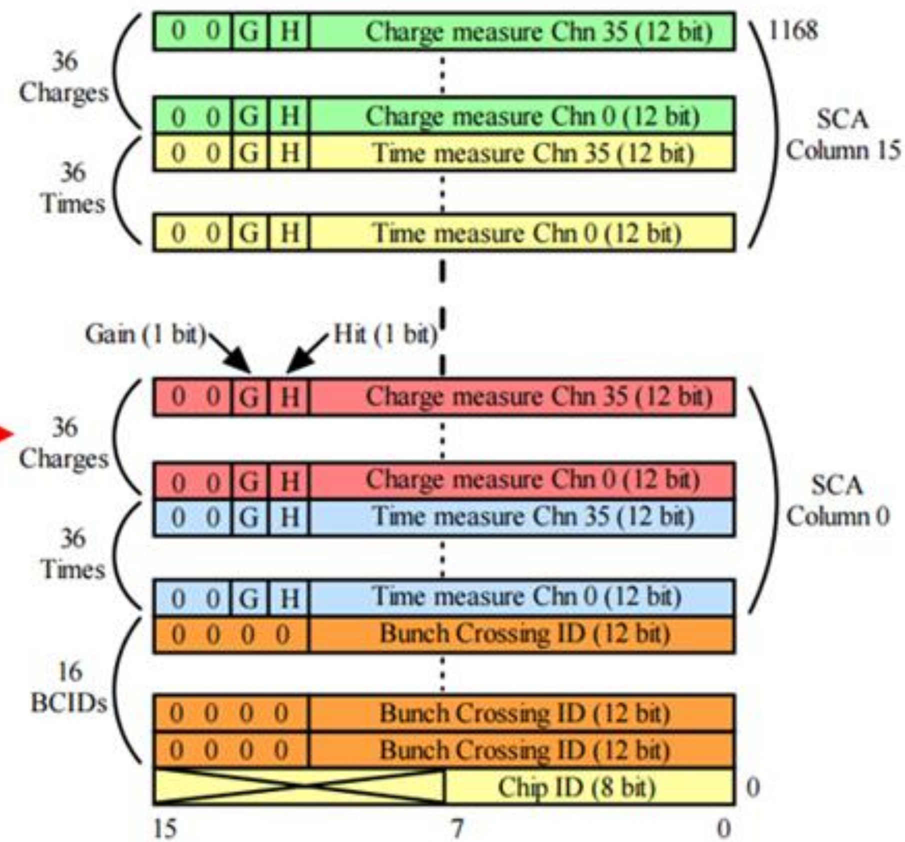
GDCC packet format

Dst MAC	Src MAC	Ethernet Type	GDCC_Type	GDCC_Modifier	GDCC_PktID	GDCC_DataLength	GDCC_Data	PAD	CRC32
6 Bytes	6 Bytes	2 Bytes	2 Bytes	2 Bytes	2 Bytes used for **spill#**	2 Bytes used for **spill flag**	Variable	Pad to Min Ethernet Size	4 Bytes

DIF data format

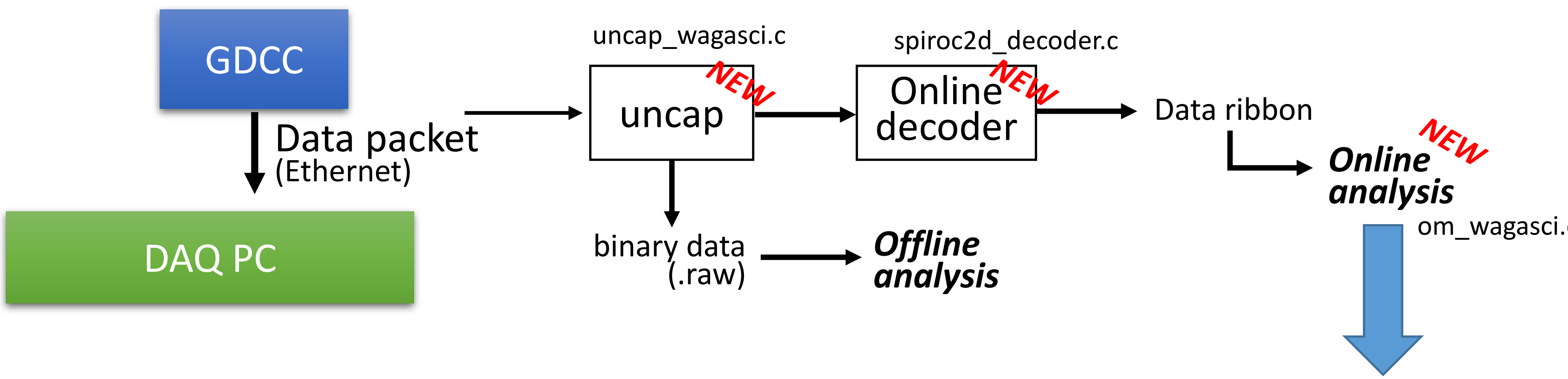
Section	subsection	field	hex	ascii
SPILL header		Marker	0xFFFC	
		<ACQid> msb	....	
		<ACQid> lsb	....	
		Ascii tag	0x5053	"SP"
		Ascii tag	0x4C49	"IL"
		Blank space	0x2020	" "
	CHIP header	Marker	0xFFFD	
		<ID>	0xFF..	
		Ascii tag	0x4843	"CH"
		Ascii tag	0x5049	"IP"
		Blank space	0x2020	" "
		Raw DATA	binary	
	CHIP trailer	Marker	0xFFFE	
		<ID>	0xFF..	
		Blank space	0x2020	
		Blank space	0x2020	
SPILL trailer		Marker	0xFFFF	
		<ACQid> msb	....	
		<ACQid> lsb	....	
		<nb chip>	0x00 ..	
		<ACQid> msb	....	
		<ACQid> lsb	....	
		Blank space	0x2020	

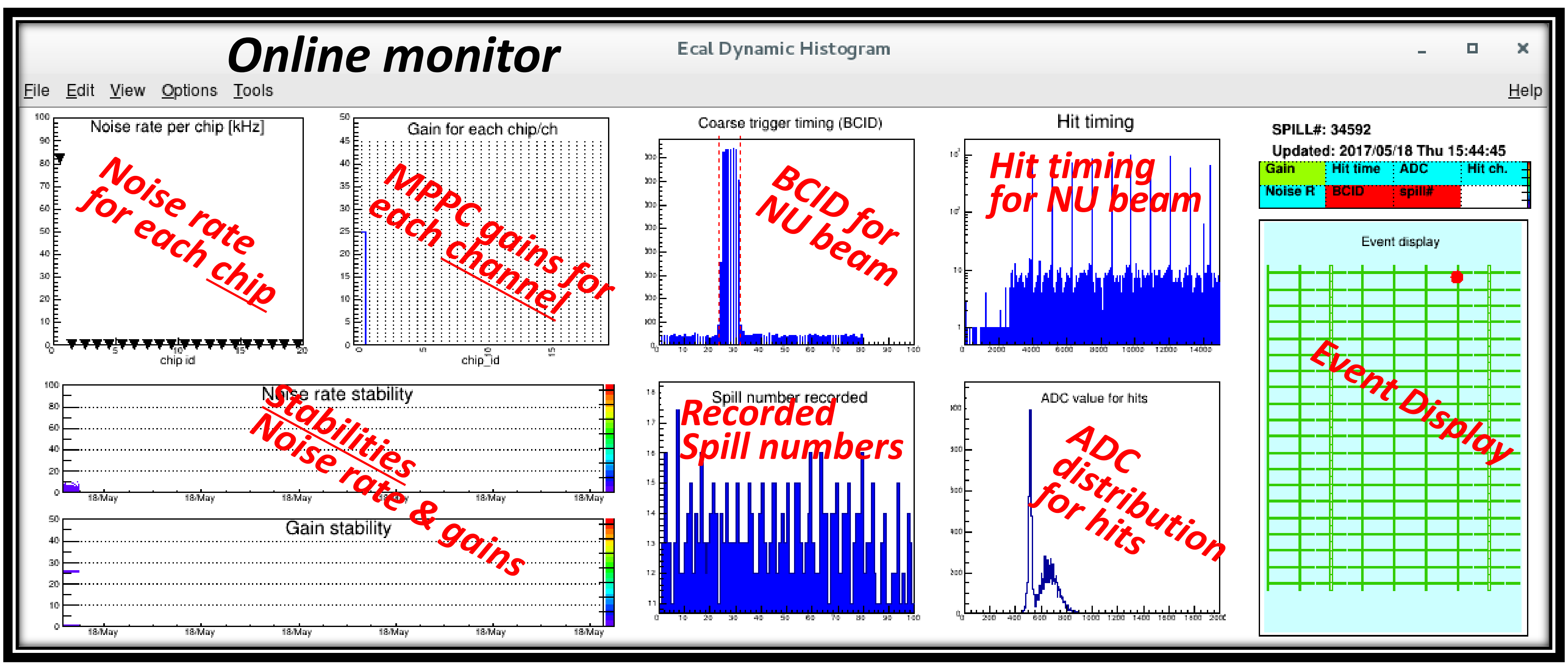
SPIROC data format



*Time/Charge are inversed for SPIROC2D.

Data analysis flow

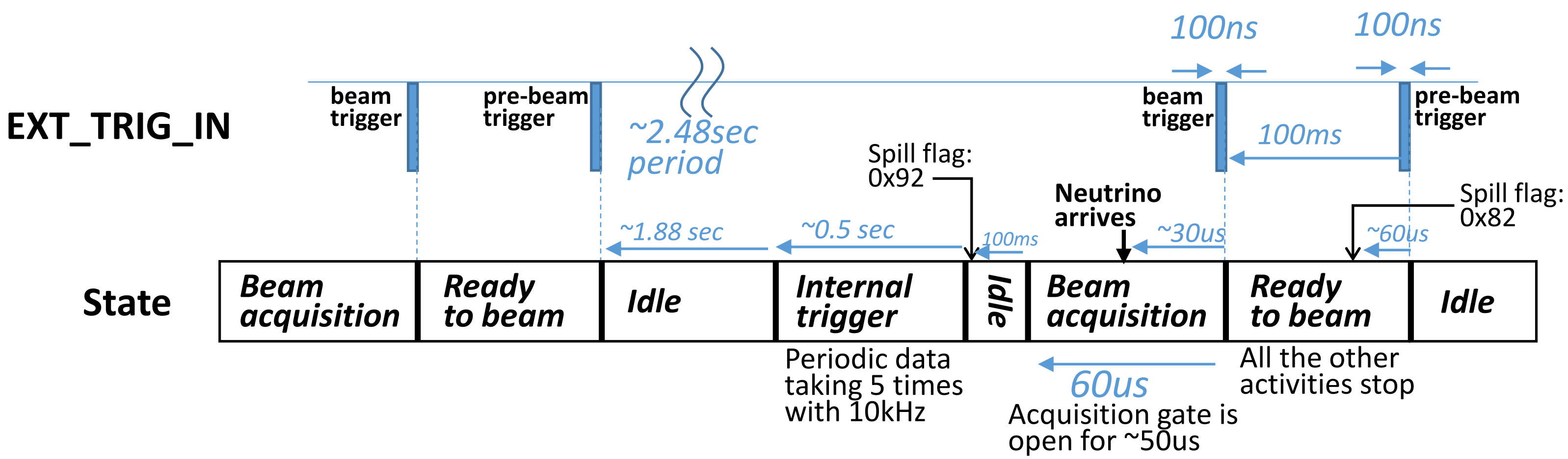


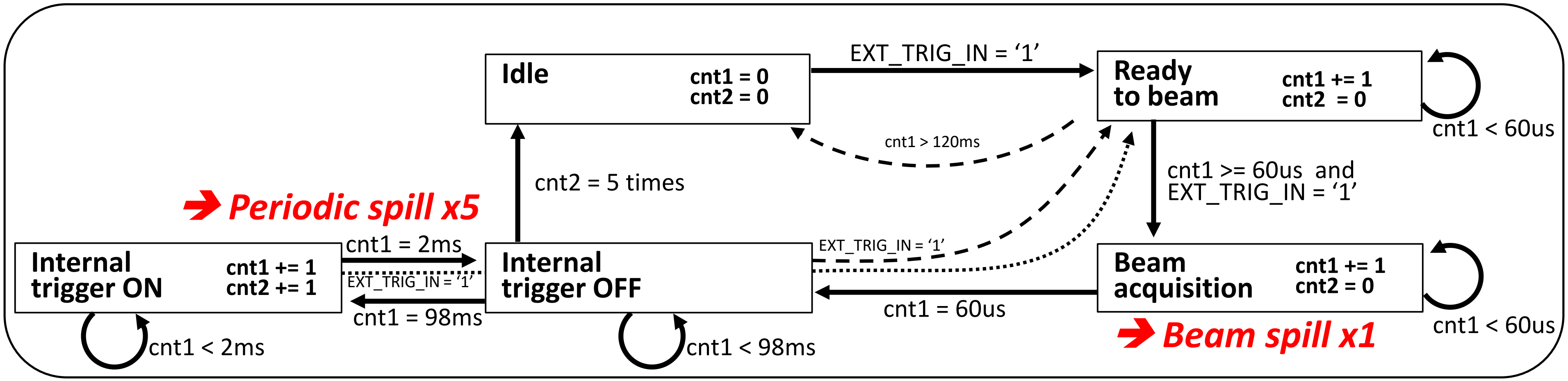


*These test plots are made just with test data.

Acquisition Control to the Beam Trigger

- To generate "spill" signal from the external "beam trigger".



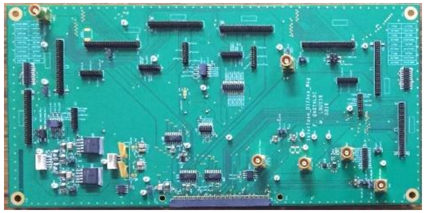


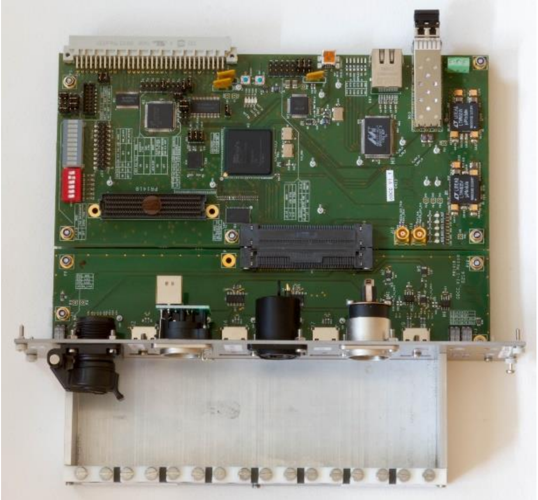
*Spill flags are changed right before the acquisition.

*This state machine works even with 1.3sec period.

Status of electronics boards

- **All boards have been fabricated.**
  - 50 ASUs … Each single board has been checked to correctly work at UTokyo.
    *Up to 4 ASUs are set in parallel/serial, and it works.
  - 4 Interfaces … 2 boards are correctly operated with a single ASU, the others are NOT.
    ➔ Investigated, but no cause found.
  - DIF … 33 boards are checked at LLR.
  - GDCC/CCC … 9 boards (6 GDCC/3 CCC) are OK.





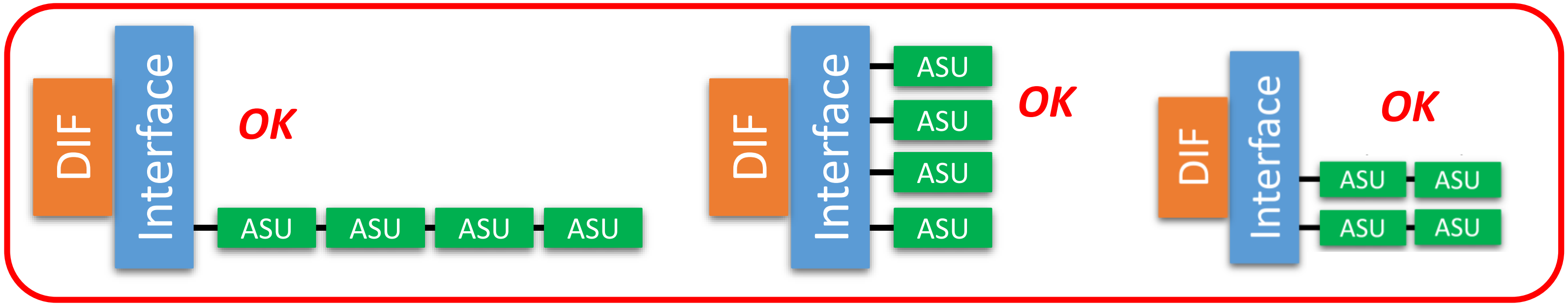
- **Failed to operate with many ASUs.**
  - It fails to configure when ~10ASUs are set on an Interface board.

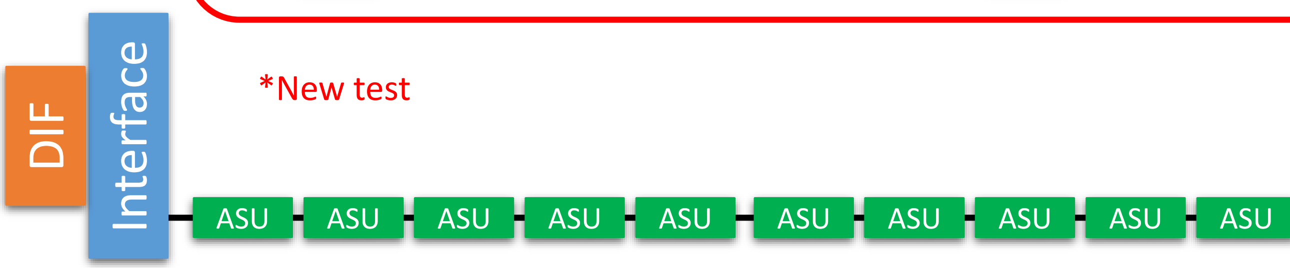
Issue on Readout on Many ASUs

☐ *Under investigation*

- It seems that it fails to configure all ASUs.
- The behavior depends on numbers of ASUs.

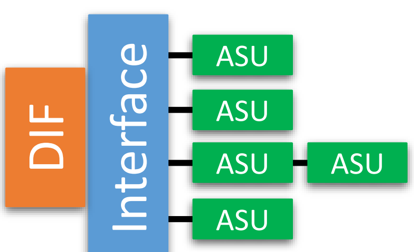
*Test with the first production.





OK w/ 10ASUs → NG w/ 11ASUs

*Other various configurations have been checked.



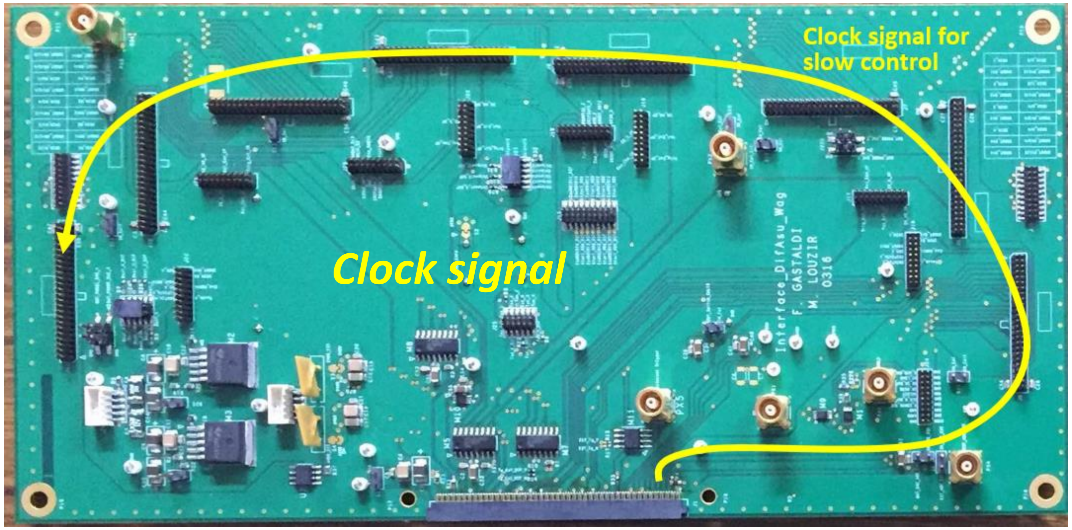
OK or NG

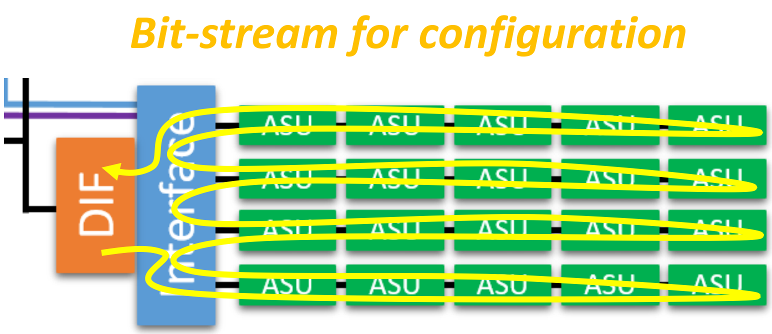
- The behavior seems more unstable when the 2nd to 4th ASU line has more boards.
- Even adding a capacitor or putting a probe pin may sometimes improve the behavior.

Issue on Readout on Many ASUs

Under investigation

- The most probable cause is that
  slow control signals are broken by large capacity of ASUs?
  - ✓ These signals have long paths on the Interface board and ASUs.





- **Possible solution?**
  - ✓ Changing a buffer IC on the Interface board, providing the slow control clock signals for each ASU line?
  - ✓ Lowering the frequency of slow control clock in the DIF firmware?

➔ We need to keep investigation, and if needed, some update will be done on the Interface board.

Plans & Summary

❑ToDo list

- Control/monitor system of power supplies (HV, LV), and water level sensor.
  - ✓ Remote control of ZUP PS units.
  - ✓ Data logger for water level sensor.
- Prepare for offline analysis.
  - ✓ Data storage.
    - ◆KEKCC, Kyoto, or any other?
  - ✓ Other PCs than the front-end node?
  - ✓ Auto-processes codes.

❑Summary

- Spill information implementation has been basically completed.
- The basic plots for online monitors has been built.
- Electronics boards have been ready, but we found a new issue probably on the Interface board.
- This issue is the most urgent point to be solved.

Supplemental slides

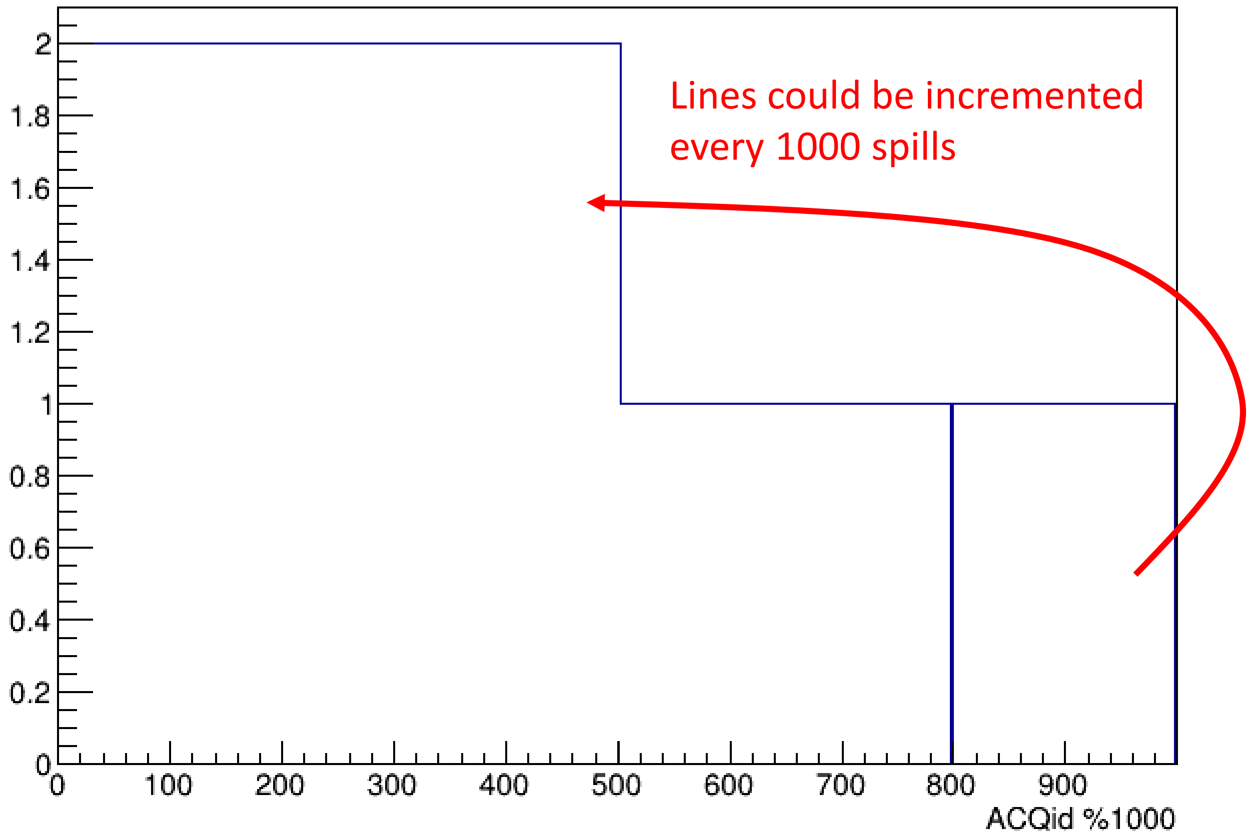
Specification of online monitor plots

1. Acquisition ID plots with good data format

- To monitor if the data taking efficiency is as expected.

* After "spill flag" and "spill number" will be implemented, this plots should be produced <u>only for the "beam spills</u>" with the spill number instead of acquisition ID.

The plot is updated every "beam spill" (~2.48sec).

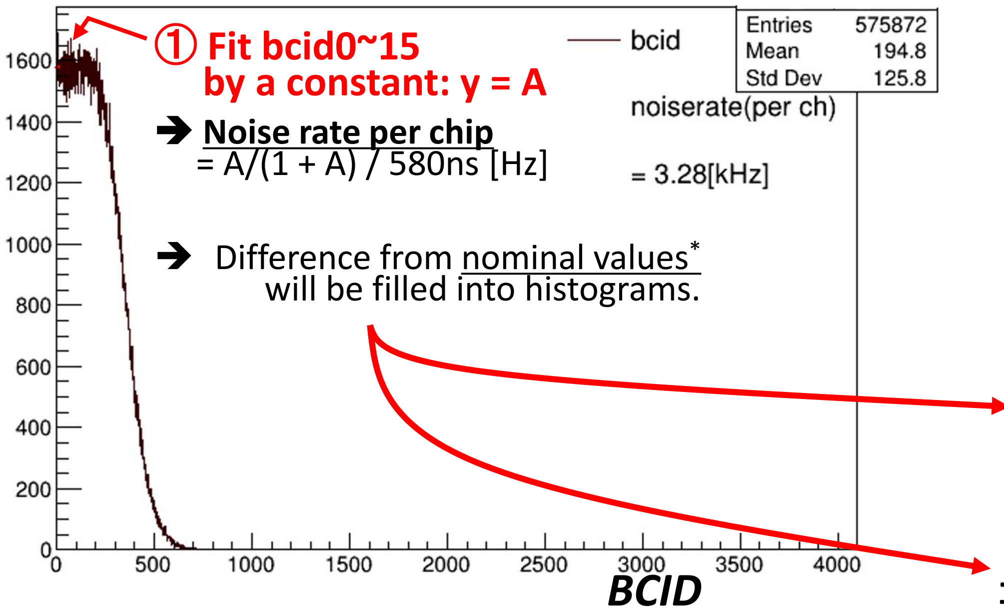


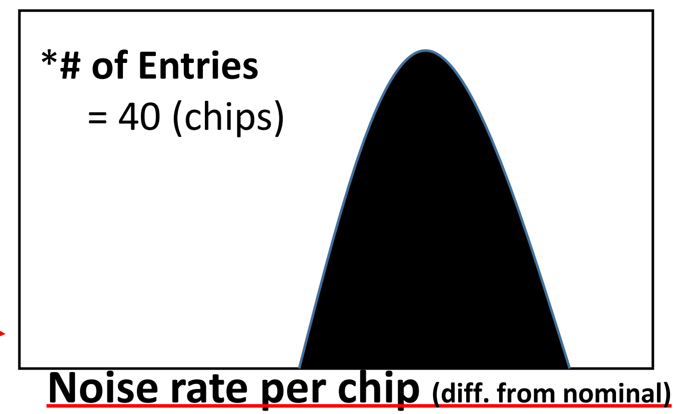
Specification of online monitor plots

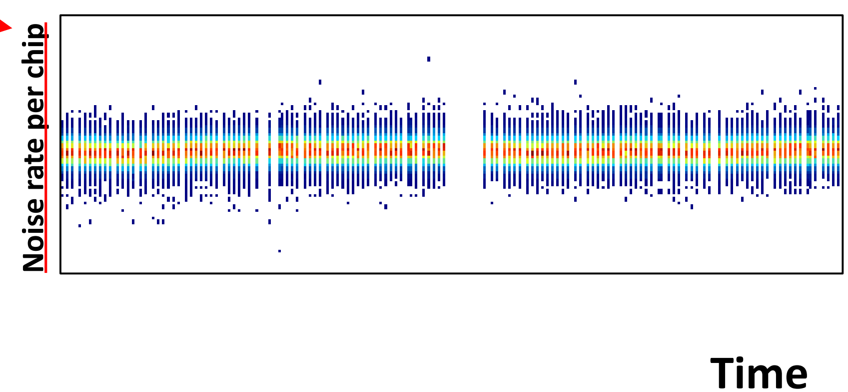
2. Noise rate per chip by BCID

- To monitor if any unexpected noise affects the data taking and if the noise rate corresponds to the MPPC noise rate.

* After "spill flag" and "spill number" will be implemented, this plots should be produced <u>only for the "periodic spills"</u>.







The plots could be renewed every 1600 spills.

* It corresponds to ~100 entries for each bin of the first 16 columns.

*Update period is expected ~6min.

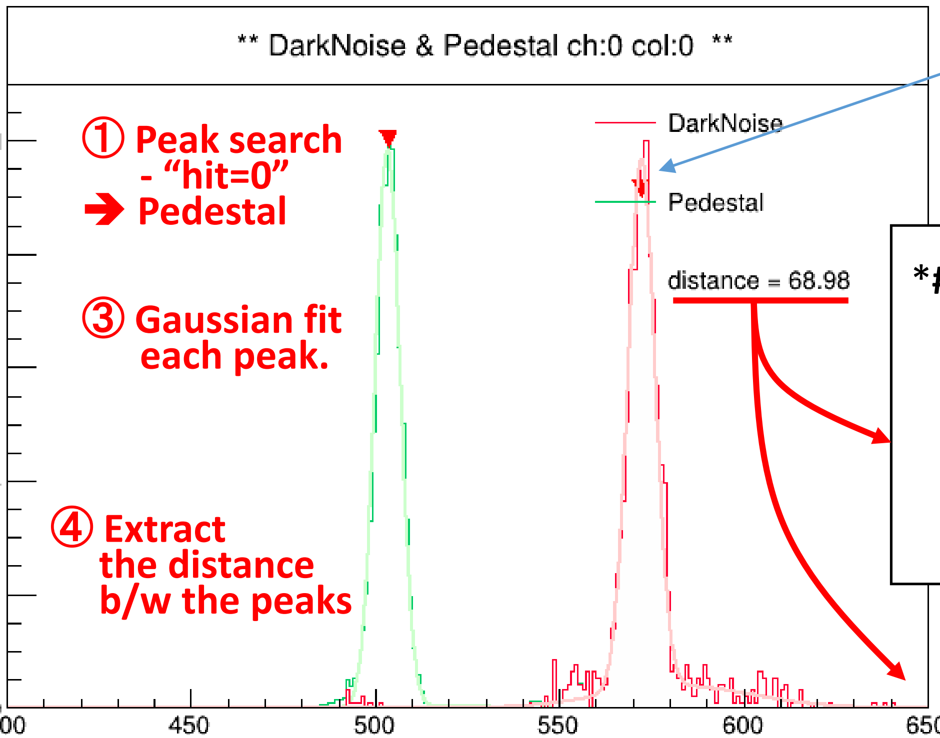
*Nominal value will be measured for each chip.
Temporarily, 3kHz can be used for all chip.

Specification of online monitor plots

3. Distance charge ADC b/w pedestal peak and MPPC dark-noise peak.

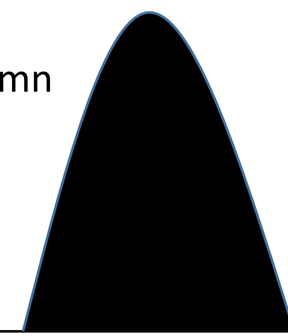
- To monitor the stability of MPPC gain.

*It requires to extract <u>only the "periodic spills"</u> and to remove beam spills, by using "spill flag".
It is ok to merge everything until the "spill flag" will be implemented.

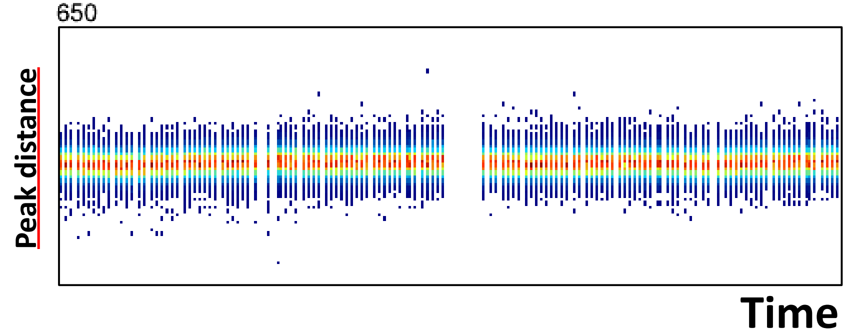


② Peak search
- "hit=1"
➔ Largest peak is from MPPC dark noise.

*# of Entries
= chip x ch x column
= 40 x 32 x 16
= **20480**



Distance = peak1 – peak0



The plot for peak distance could be renewed every 1600 spills.

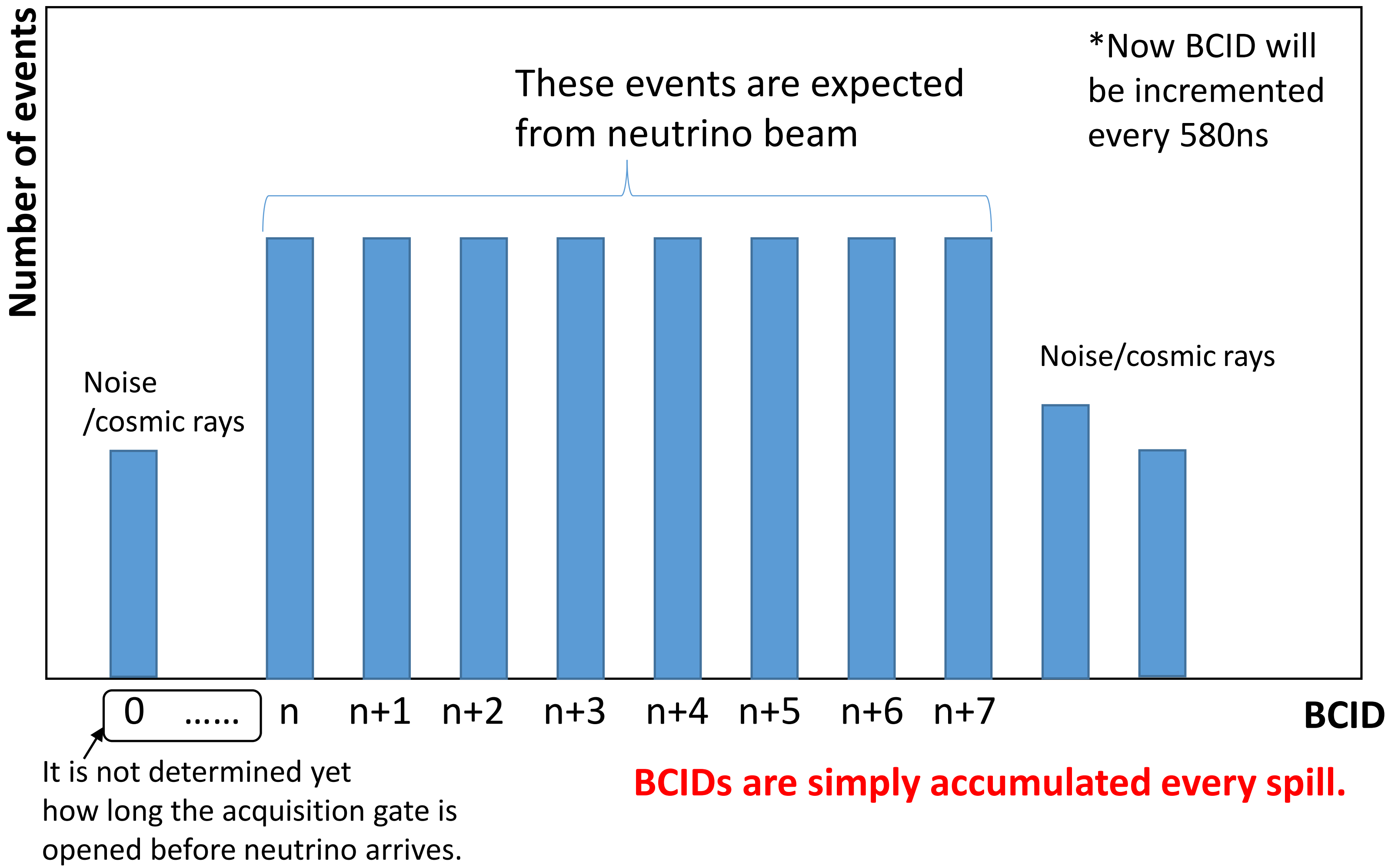
* It corresponds to ~50 events of MPPC dark noise for each ch, col.

*Update period is expected ~6min.

4. Trigger timing plots (coarse) by BCID

- To monitor if the neutrino events are triggered on expected timing.

* After "spill flag" will be implemented,
this plots should be separated by the spill flag and <u>only the "beam spills"</u> should be extracted.

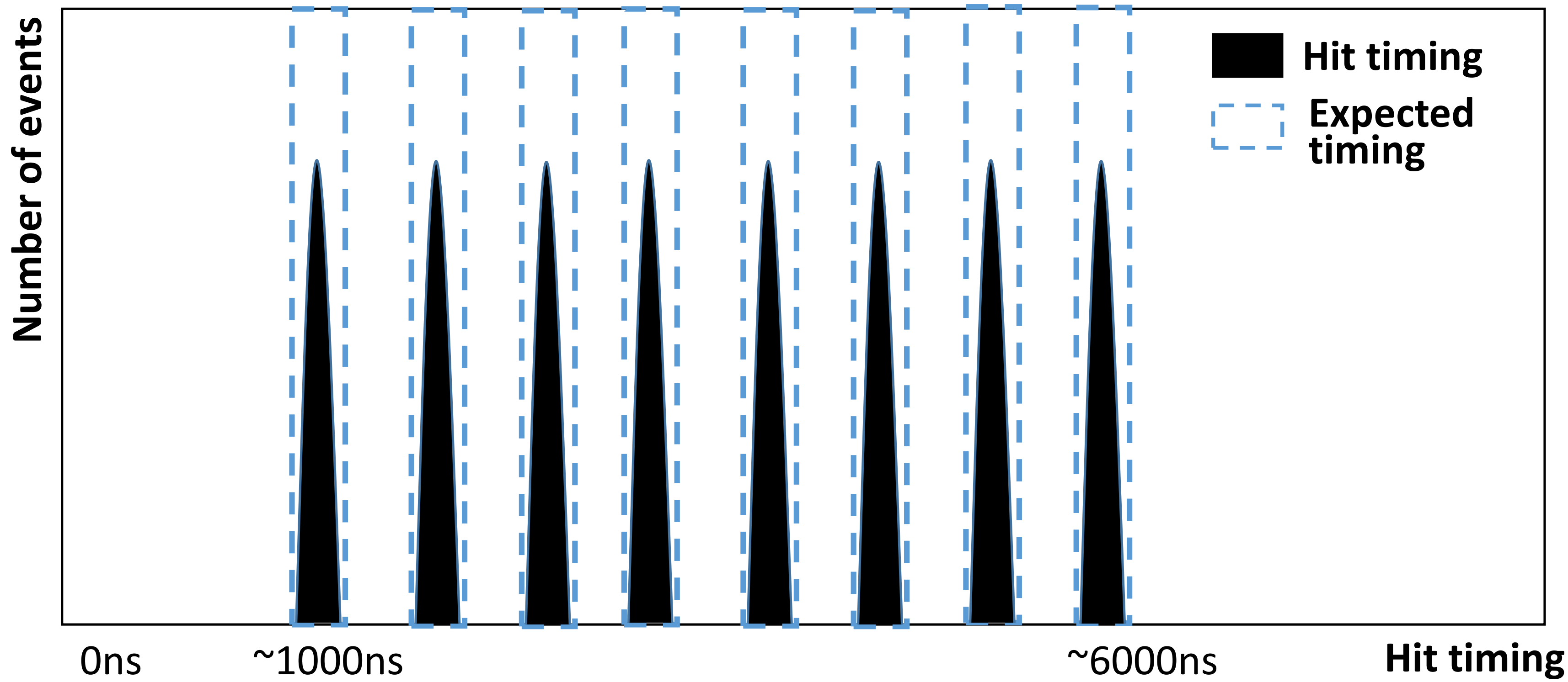


BCIDs are simply accumulated every spill.

5. Hit timing plots (fine) by time measurement

- To monitor the hit timing.

* After “spill flag” will be implemented,
this plots should be separated by the spill flag and only the “beam spills” should be extracted.



Hit timings are simply accumulated every spill.

Hit timing = BCID*580ns
+ (<12-bit TDC> - A)*B ns [when bcid==even]
+ (C - <12-bit TDC>)*D ns [when bcid==odd]

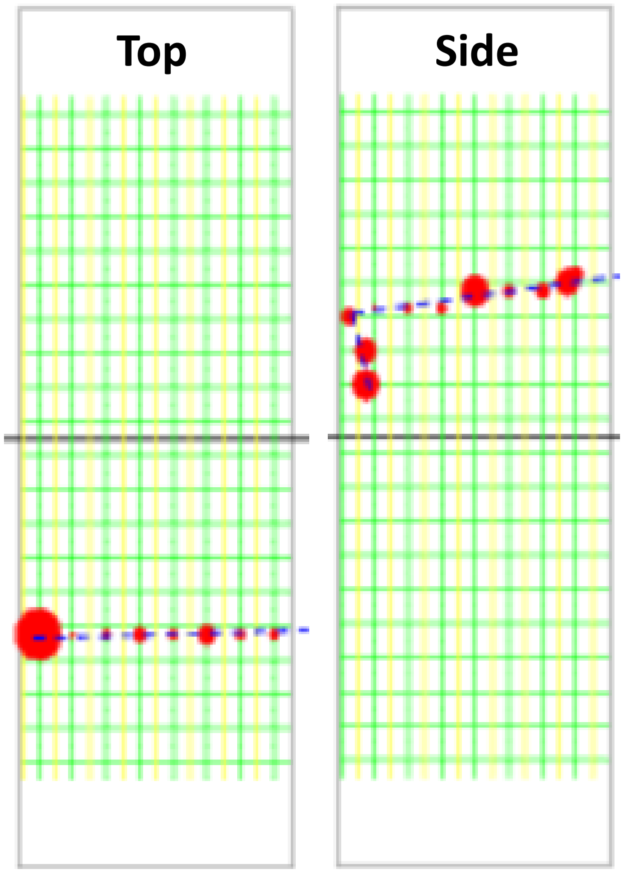
The const A,B,C,D will be measured for each chip/ch/col.

*Temporarily,
A = 500
B = D = 1ns
C = 4096
can be used for all chip/ch/col

Specification of online monitor plots

6. Event display

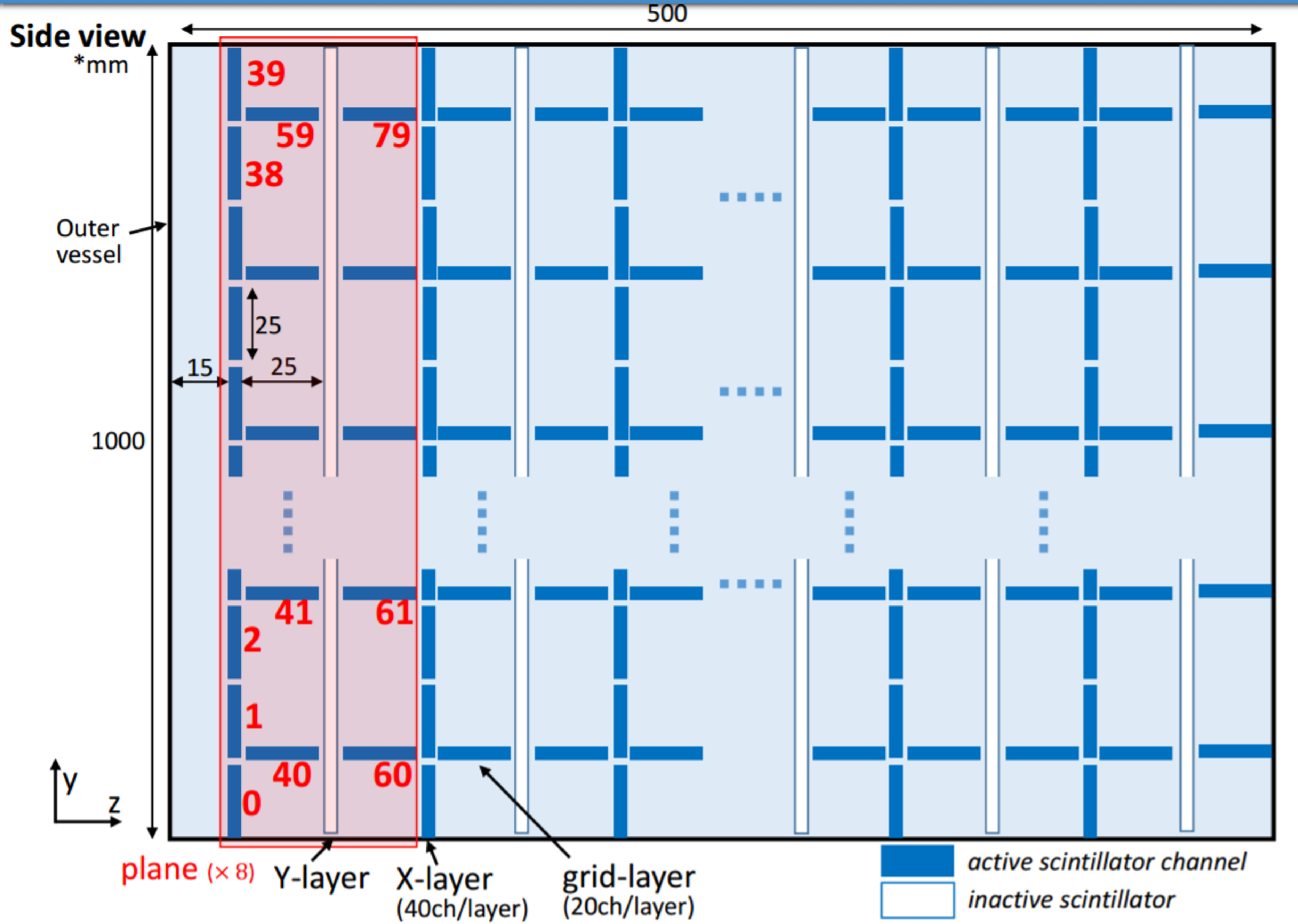
* After "spill flag" will be implemented,
this plots should be separated by the spill flag and <u>only the "beam spills"</u> should be extracted.



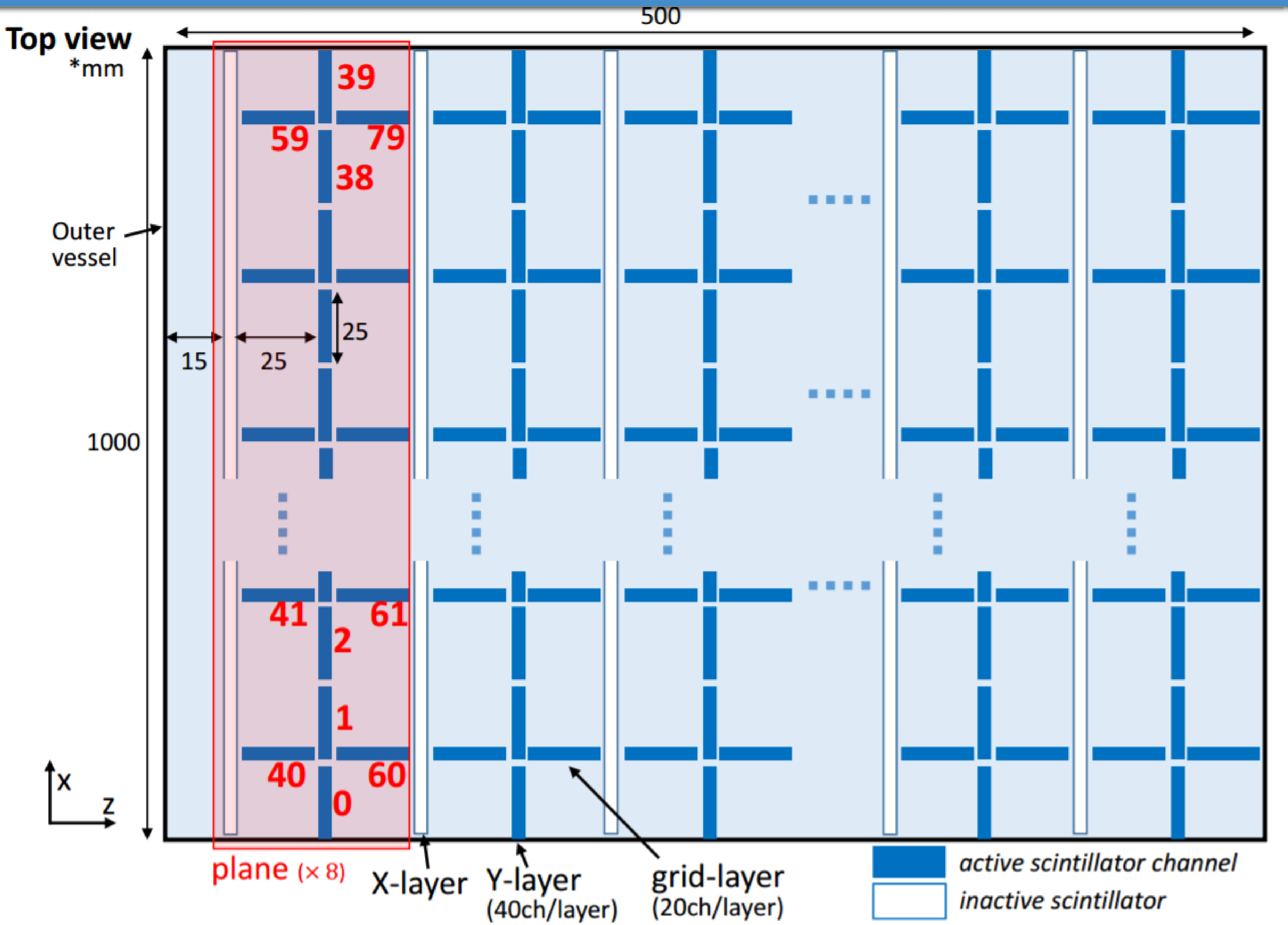
- **Event display can be updated as follows.**
  - Only when it has 3 hits for each view on the same bcid (or ±1), the display can be updated.
  - Once it is updated, it needs to wait for <u>10sec*</u> at least.
  *This 10sec needs to be optimized later.
- **Size of dots can show the corresponding charge value.**
- The correspondence between DIF/ASU and module VIEW/PLN/CH is written in the <u>table</u>*
- The distribution of module VIEW/PLN/CH is written in the next page.

*<u>**Table**</u> : The correspondence between SPIROC chip#/ch# and WAGASCI module view/pln/channel.
http://www-he.scphys.kyoto-u.ac.jp/member/hayashino/B2Water/dokuwiki/lib/exe/fetch.php?media=chikuma:channel_mapping.xlsx
Side view = 0 , Top view=1.

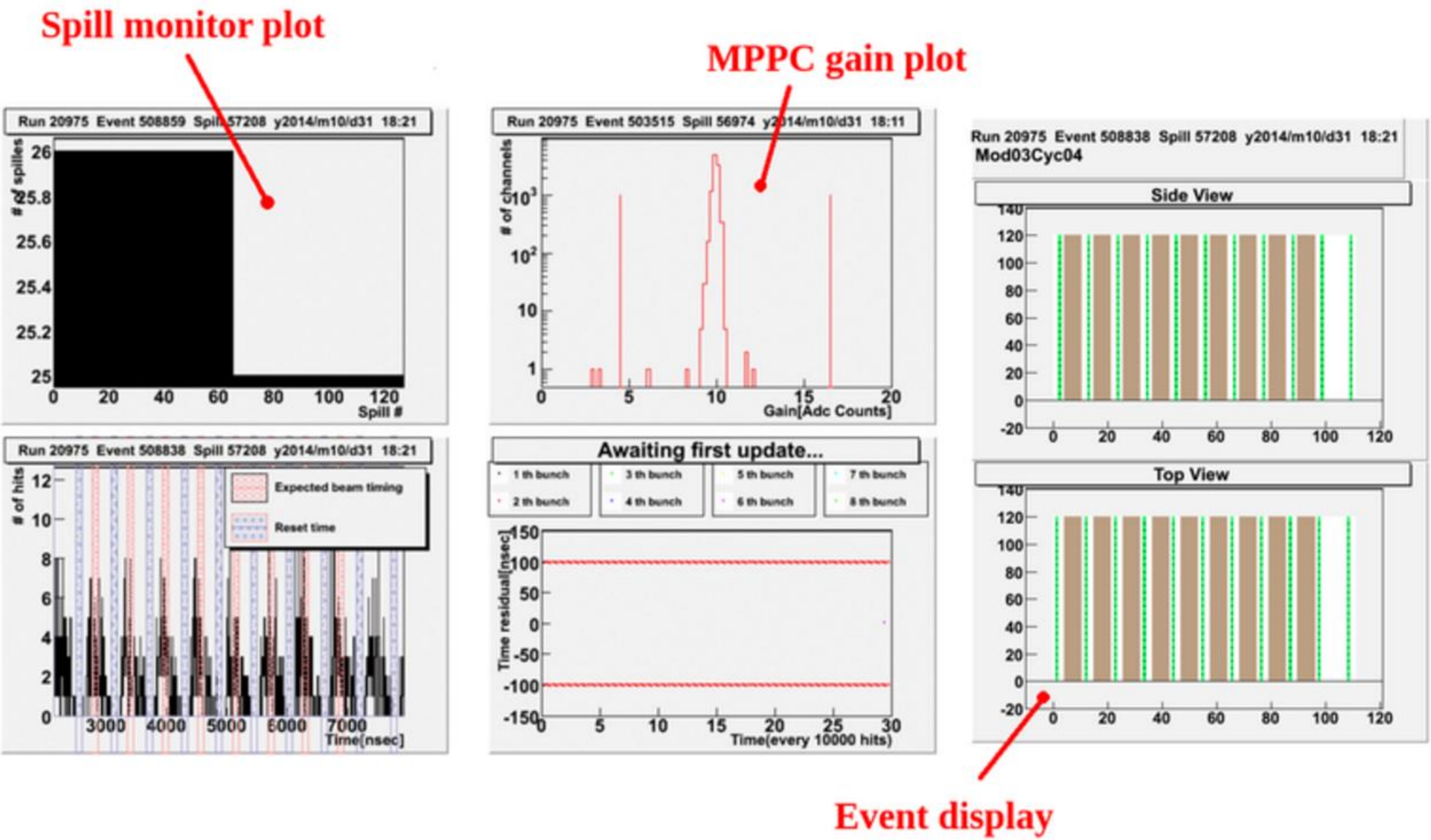
WAGASCI channel mapping



WAGASCI channel mapping

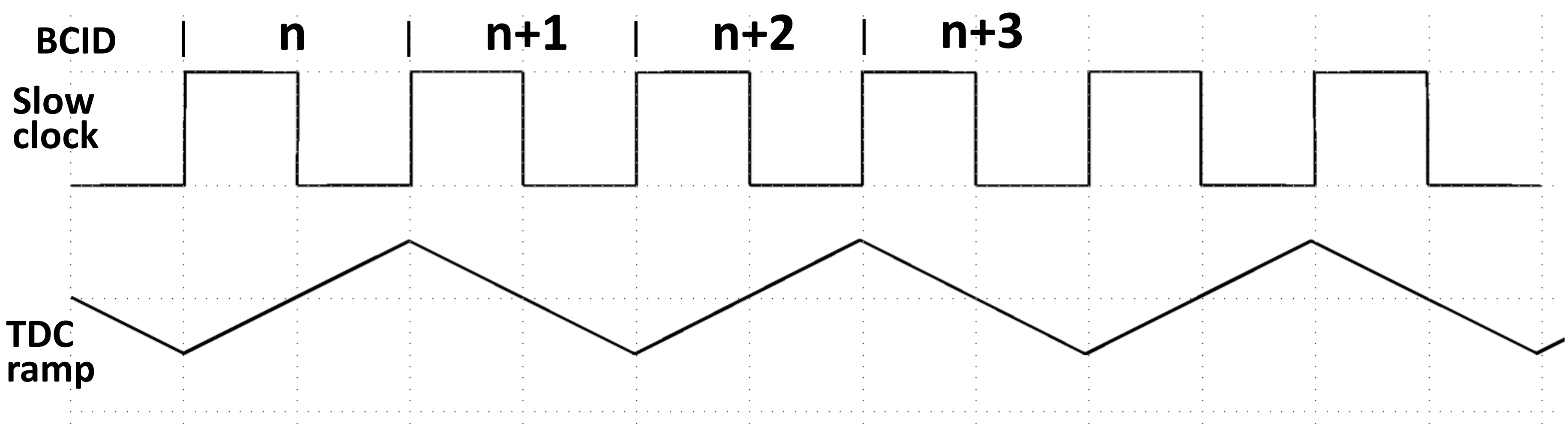


INGRID online monitor



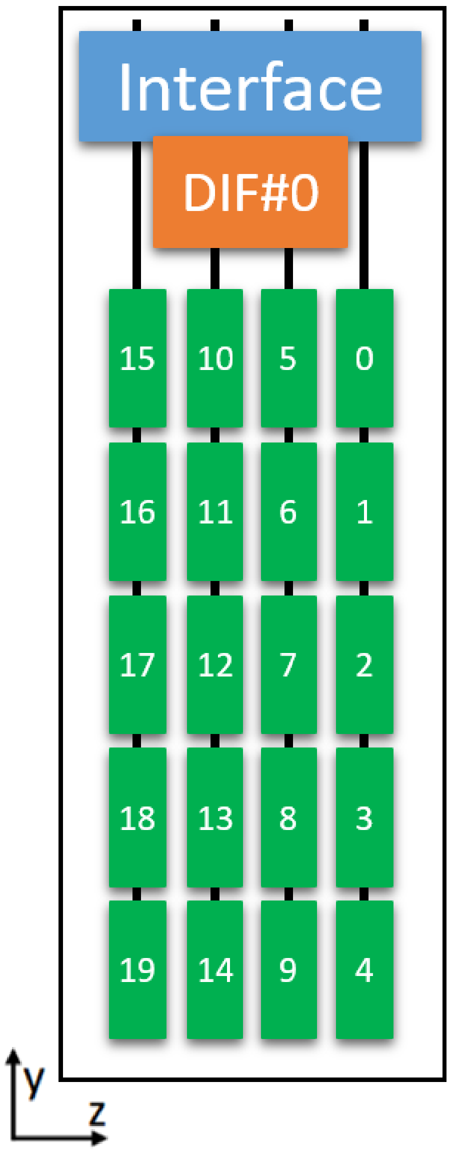
Time measurement in SPIROC2D

- BCID is incremented every slow clock edge.
- Timing is measured by TDC signal with rising and falling ramps.
  - It needs to be inversed by which of even/odd the bcid is.

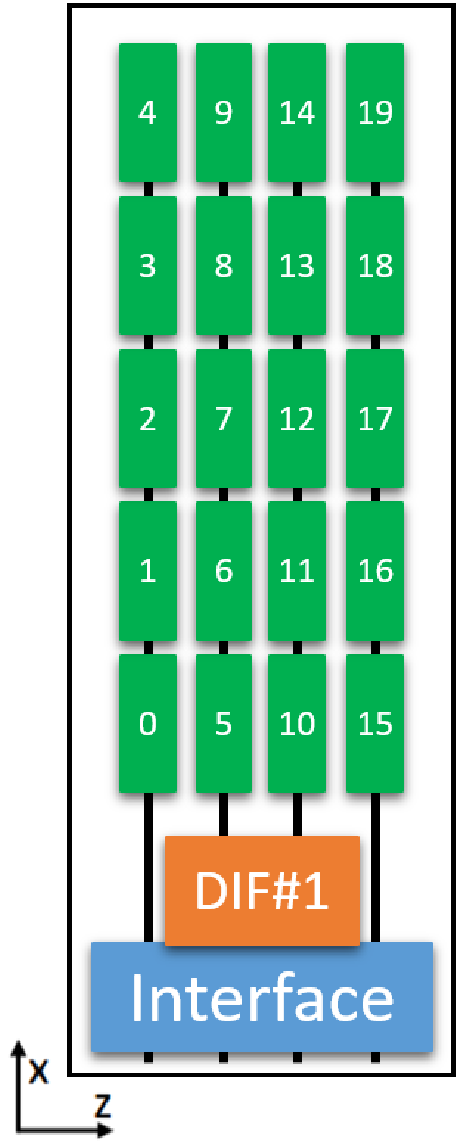


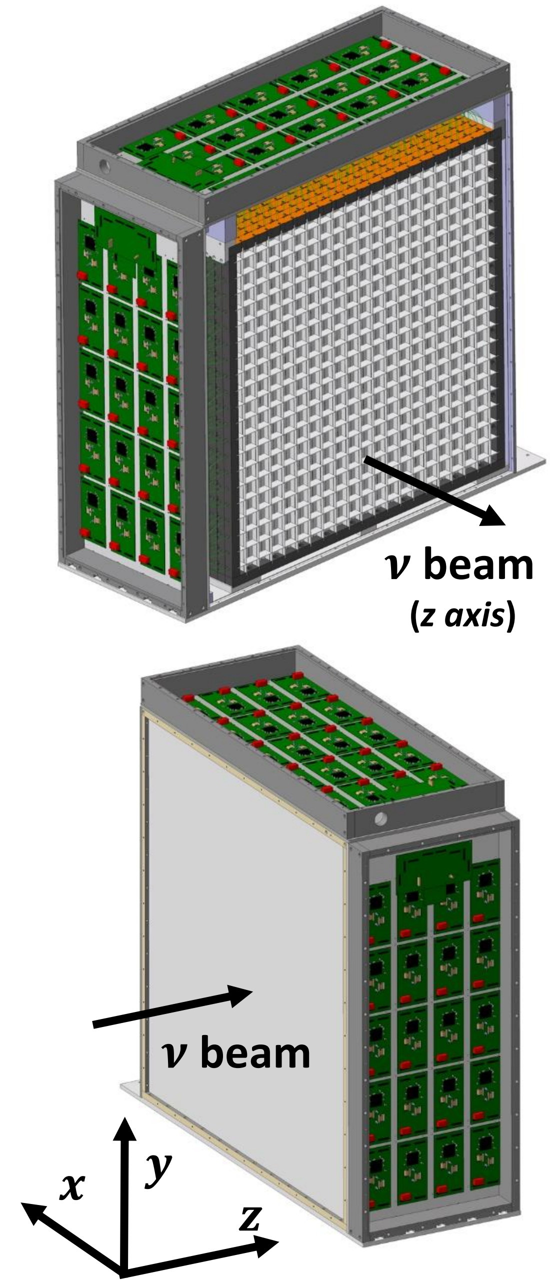
WAGASCI ASU mapping

Side

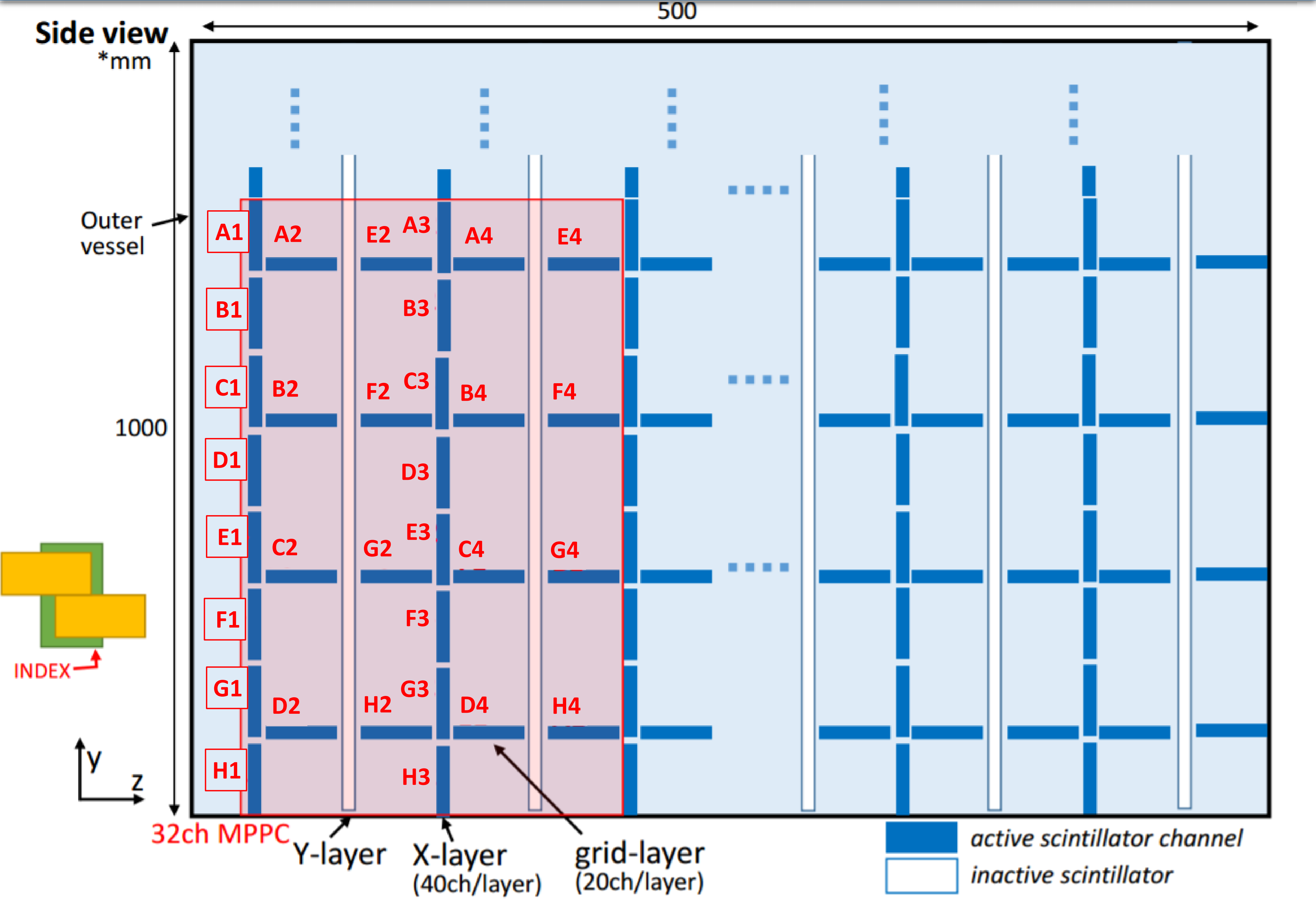


Top

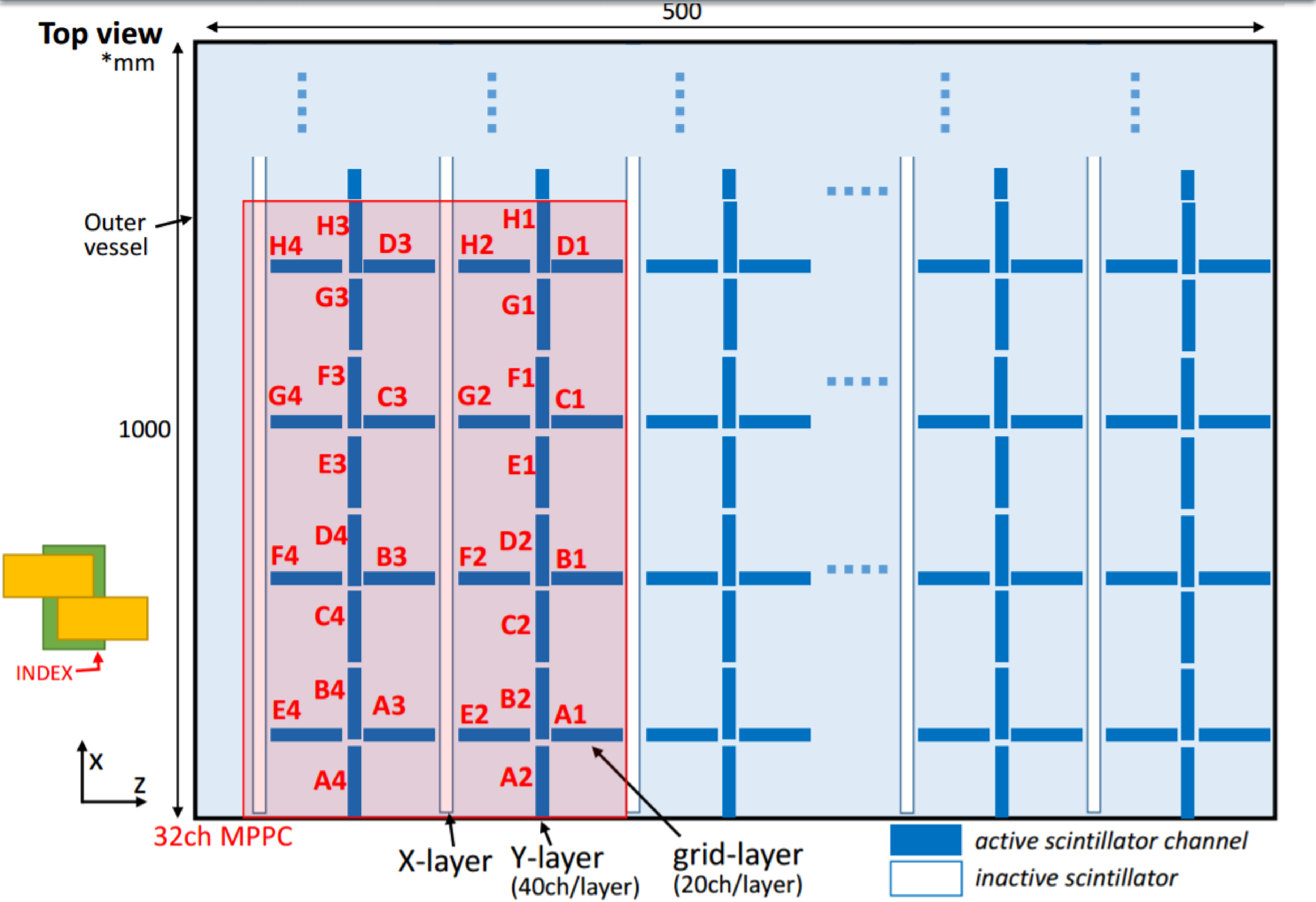




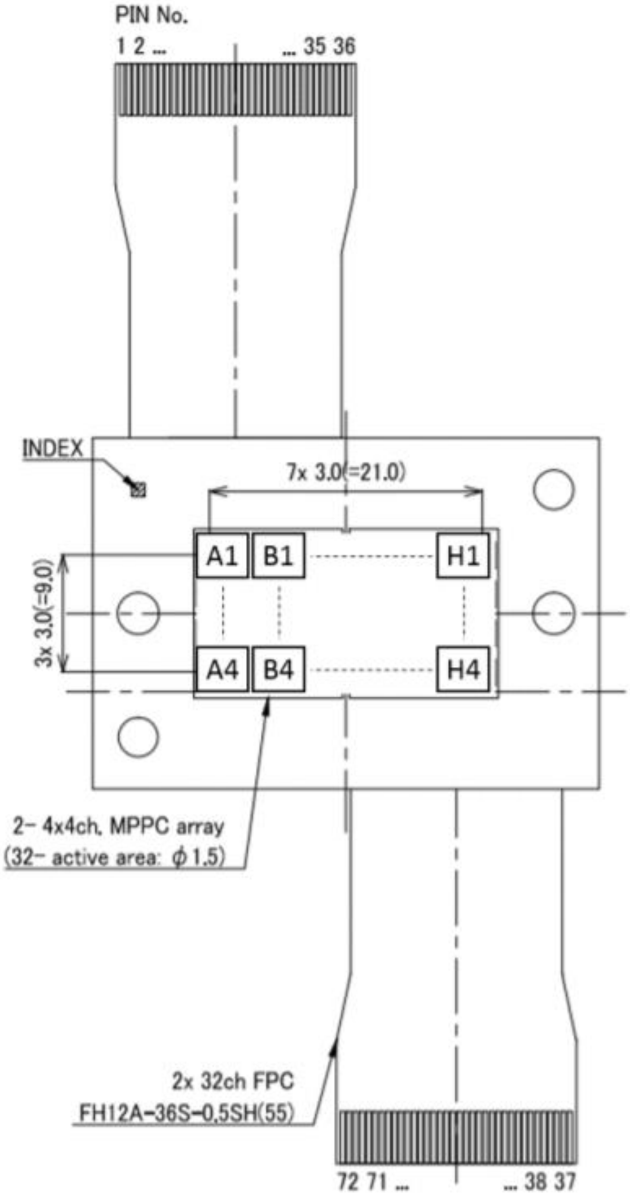
WAGASCI channel mapping



WAGASCI channel mapping



MPPC channel mapping



FPC No.	ch. No.	FPC No.	ch. No.	FPC No.	ch. No.	FPC No.	ch. No.
1	A(A4)	19	A(C4)	37	A(H1)	55	A(F1)
2	A(A3)	20	A(C3)	38	A(H2)	56	A(F2)
3	A(A2)	21	A(C2)	39	A(H3)	57	A(F3)
4	A(A1)	22	A(C1)	40	A(H4)	58	A(F4)
5	A(B4)	23	A(D4)	41	A(G1)	59	A(E1)
6	A(B3)	24	A(D3)	42	A(G2)	60	A(E2)
7	A(B2)	25	A(D2)	43	A(G3)	61	A(E3)
8	A(B1)	26	A(D1)	44	A(G4)	62	A(E4)
9	NC	27	NC	45	NC	63	NC
10	K(A4)	28	K(C4)	46	K(H1)	64	K(F1)
11	K(A3)	29	K(C3)	47	K(H2)	65	K(F2)
12	K(A2)	30	K(C2)	48	K(H3)	66	K(F3)
13	K(A1)	31	K(C1)	49	K(H4)	67	K(F4)
14	K(B4)	32	K(D4)	50	K(G1)	68	K(E1)
15	K(B3)	33	K(D3)	51	K(G2)	69	K(E2)
16	K(B2)	34	K(D2)	52	K(G3)	70	K(E3)
17	K(B1)	35	K(D1)	53	K(G4)	71	K(E4)
18	NC	36	NC	54	NC	72	NC

A: Anode
K: Cathode
NC: No connection