END SEMESTER ASSESSMENT
(ESA) B.TECH. (ECE)
FOURTH SEMESTER

UE22EC251B – DIGITAL VLSI DESIGN

PROJECT

REPORT ON

"4-BIT FULL ADDER USING CMOS LOGIC"

SUBMITTED BY

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4-BIT FULL ADDER USING CMOS LOGIC

ABSTRACT:-

This report details the implementation of a full adder circuit using XOR and AND/OR gates. Full adders are fundamental components in digital circuits, performing binary addition of three bits. The report explains the functionality of XOR gates for generating the sum bit and the combined use of AND and OR gates for determining the carry-out bit. It highlights the advantages and limitations of this approach compared to pre-designed integrated circuits (ICs).

INTRODUCTION :-

Binary addition is a core operation in digital computers. Full adders facilitate this process by adding three binary digits (bits): two input bits (A and B) and a carry-in bit (Cin) from the previous lower-order addition. They produce a sum bit (S) and a carry-out bit (Cout).

Circuit Design:

- **Sum Bit (S):**
  - An XOR gate is used with A, B, and Cin as inputs.
  - The XOR gate outputs 1 when exactly one of its inputs is 1.
  - This directly reflects the sum logic in binary addition, considering A, B, and the carry-in.
- **Carry-Out Bit (Cout):**
  - A full adder requires a more complex approach for carry determination due to two possible scenarios:
    - Both A and B are 1 (regardless of Cin).
    - Only one of A or B is 1, but there's a carry-in (Cin = 1).
  - A common implementation utilises an OR gate with two inputs:
    - The output of an AND gate that takes A and B as inputs (represents the first carry condition).
    - Another AND gate that takes Cin and (A XOR B) as inputs (represents the second carry condition).
  - This OR gate ensures the Cout reflects any situation requiring a carry.

Advantages:

- This design utilising minimal gates to achieve full adder functionality.
- XOR gates offer efficient sum generation.
- Combining AND and OR gates effectively captures all carry scenarios.

Disadvantages:

- Compared to pre-designed full adder ICs, this design might require more physical space due to the use of discrete gates.
- The delay introduced by each gate can slightly impact the addition speed compared to optimised ICs.

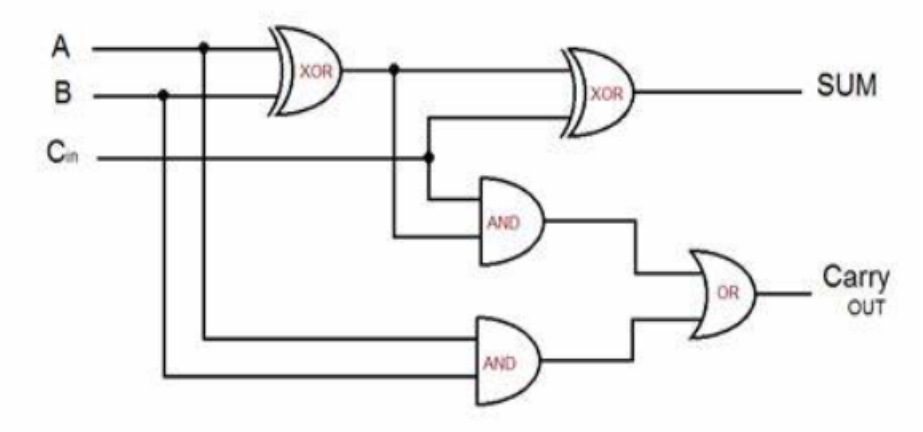

Fig 1: Implementation of full adder using logic gates.

INPUTS			OUTPUTS	
A	B	C_{in}	SUM	CARRY OUT
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

Fig 2: Truth table of full adder.

IMPLEMENTATION OF AN 1 BIT ADDER:-

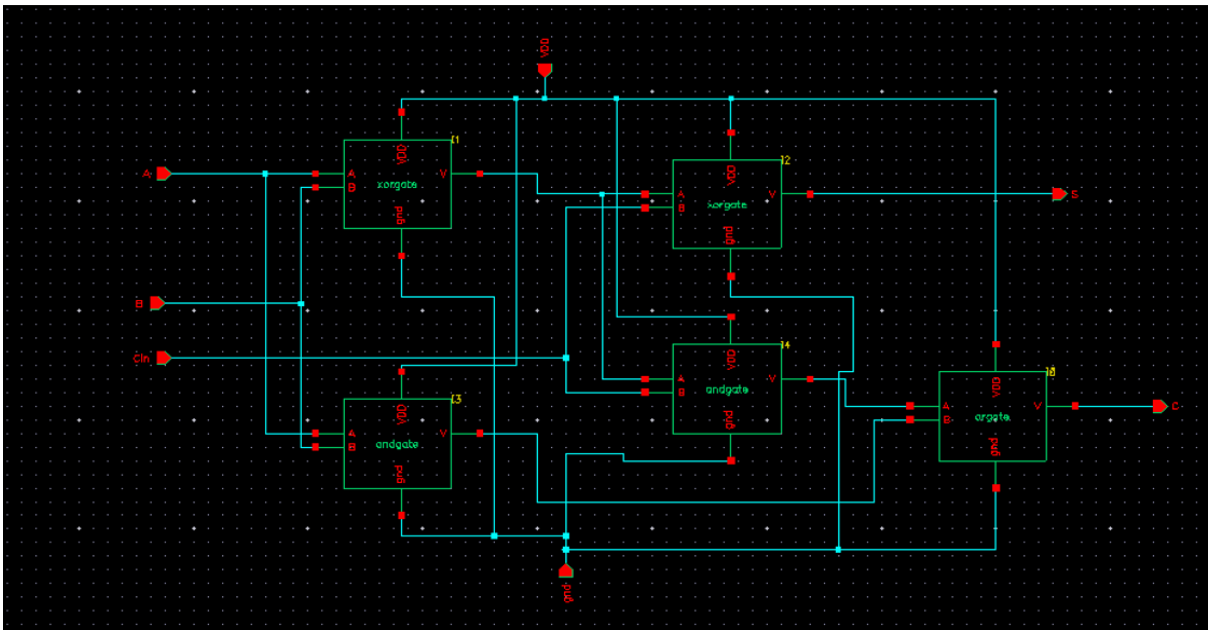

Fig 3: Schematic of full adder using logic gates in cadence.

Here two XOR gate is used to generate the sum and the AND gate & OR gate is used generate carry of a full adder with VDD 1.8V.

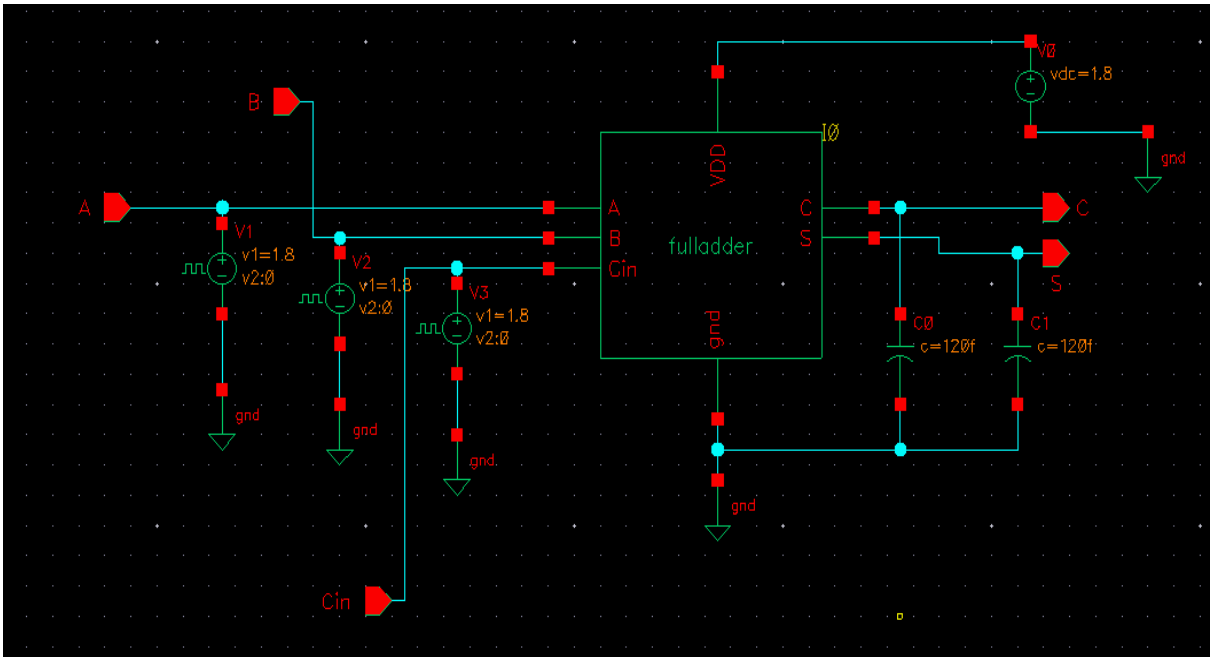

Fig 4: Schematic of full adder circuit using symbols.

In this schematic A,B,C are the input pins S,C are the sum and carry pins of a one bit full adder

WAVEFORM :-

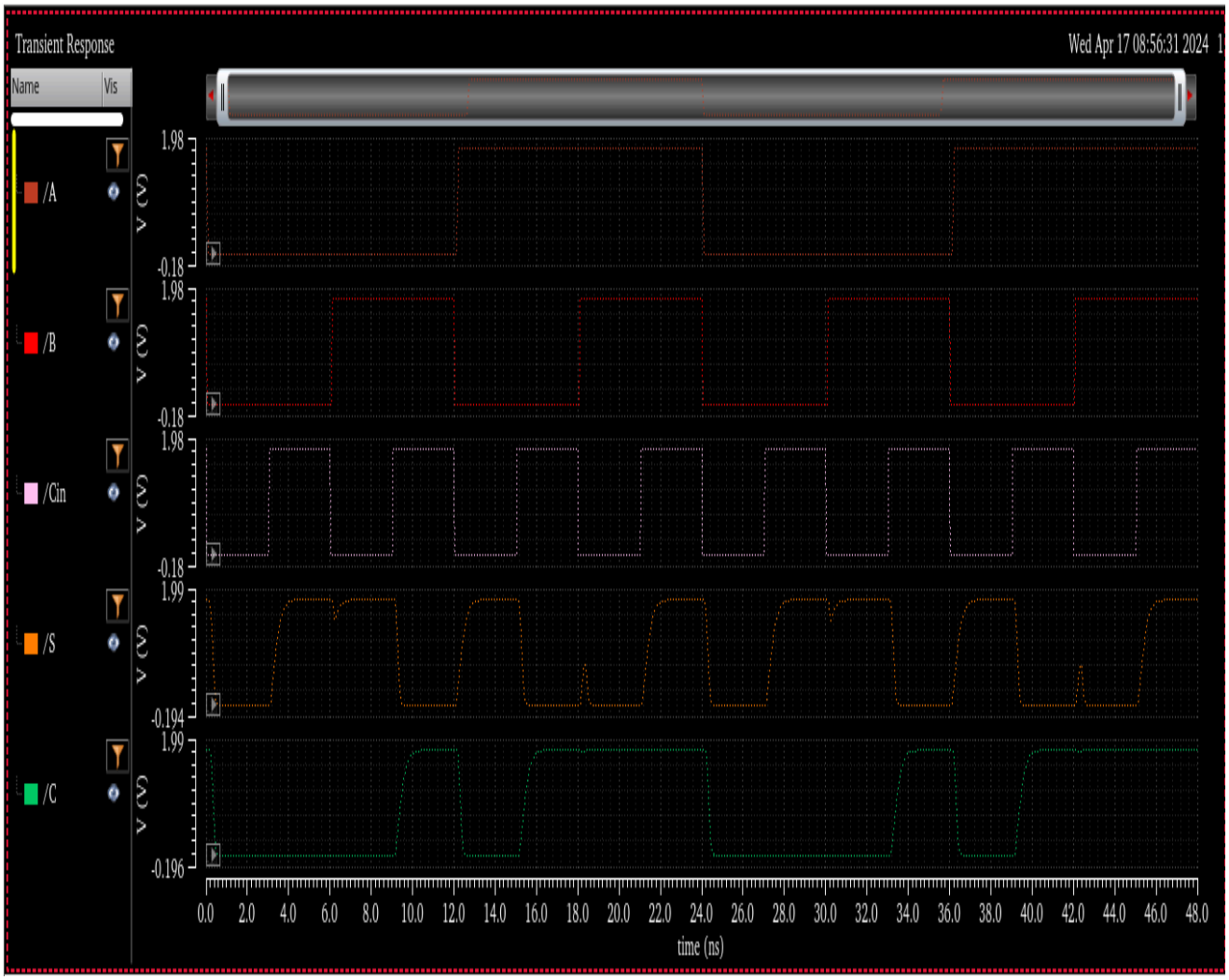

Fig 5: Output waveform of 1 bit full adder.

The above graph represents the waveform of a one bit adder. For the input pins A,B,Cin , the output generated as S for sum and C for carry. When the sum of the bits is odd then output logic of sum is 1 and when the sum of the bits is even(>0) the output logic of carry is 1.

DELAY CALCULATIONS:-

Outputs

	Name/Signal/Expr	Value	Plot	Save	Save Options
1	A		☑	☐	allv
2	B		☑	☐	allv
3	Cin		☑	☐	allv
4	S		☑	☐	allv
5	C		☑	☐	allv
6	A to sum	271.705p	☑	☐	
7	B to sum	301.705p	☑	☐	
8	Cin to sum	316.705p	☑	☐	
9	A to carry	285.318p	☑	☐	
10	B to carry	315.318p	☑	☐	
11	Cin to carry	330.318p	☑	☐	

Fig 6:Delay calculations table 1-bit full adder.

Outputs

	Name/Signal/Expr	Value	Plot	Save	Save Options
1	net1		☑	☐	allv
2	net2		☑	☐	allv
3	V		☑	☐	allv
4	A to V	75.2247p	☑	☐	

Outputs

	Name/Signal/Expr	Value	Plot	Save	Save Options
1	net2		☑	☐	allv
2	net1		☑	☐	allv
3	V		☑	☐	allv
4	or gate delay	4.45687p	☑	☐	

Outputs

	Name/Signal/Expr	Value	Plot	Save	Save Options
1	net1		☑	☐	allv
2	net2		☑	☐	allv
3	V		☑	☐	allv
4	Xor Gate delay	79.8169p	☑	☐	

Fig 6.1:Delay calculations table A)AND GATE B)OR GATE C)XOR GATE.

- Delay refers to the time it takes for a signal to propagate through a circuit and reach its final destination.Delay can be of various types : gate delay, wire delay and fan-out delay. Impact of the delays are glitches,setup time and hold time violations ,clock speed limits. These delays can be minimised by optimising circuit design ,gating of the clock signal and pipelining.
- The above table gives us the information about delay calculations of the full adder circuit where
- A to sum,B to sum and Cin to sum refers to the delay for the generation of sum output and A to carry,B to carry and Cin to carry refers to the delay for the generation of carry output.We can see that maximum delays are from Cin to Carry which can be refferred as the propagation delay of the circuit and A to Sum represents the contamination delay of the circuit.
- From the above table we can verfiy the delay calculations A to sum we have delay of 271.705ps, by the schmatic we can see that we have 2 xor gates from A to sum so the delay of xor gates is 79.81ps
  Delay from A to sum = Delay of the XOR gates + Wire delay
  =2(79.81)+112.085(approx)=271.705ps

IMPLEMENTATION OF 4 BIT ADDER USING 1 BIT FULL ADDER:-

The four-bit adder is built by connecting four full adders in a series ,Each full adder takes two input bits (A0, B0) for the least significant position (LSB), (A1, B1) for the next position, and so on.A carry-in (Cin) is fed into the first full adder, typically 0 for the LSB addition.The carry-out (Cout) from each full adder is then connected to the carry-in (Cin) of the next full adder in the cascade.The final outputs are the sum bits (S0, S1, S2, S3), representing the four bits of the result.

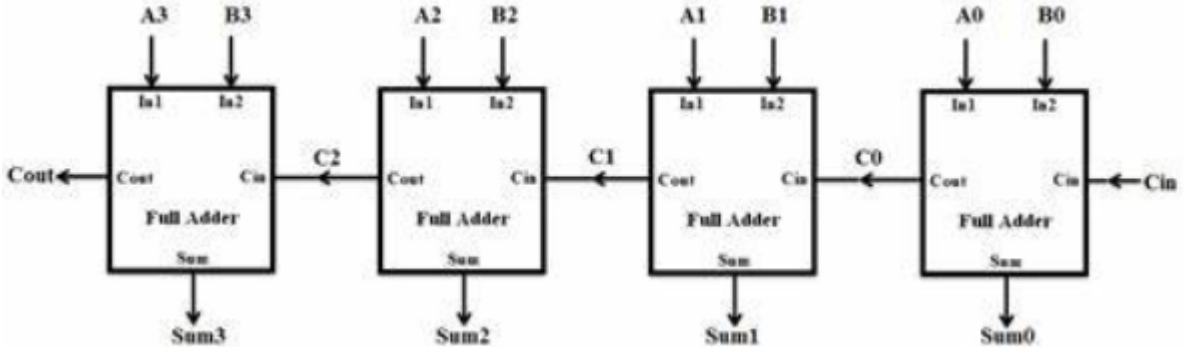

Fig 7:Implementation of 4-bit full adder .

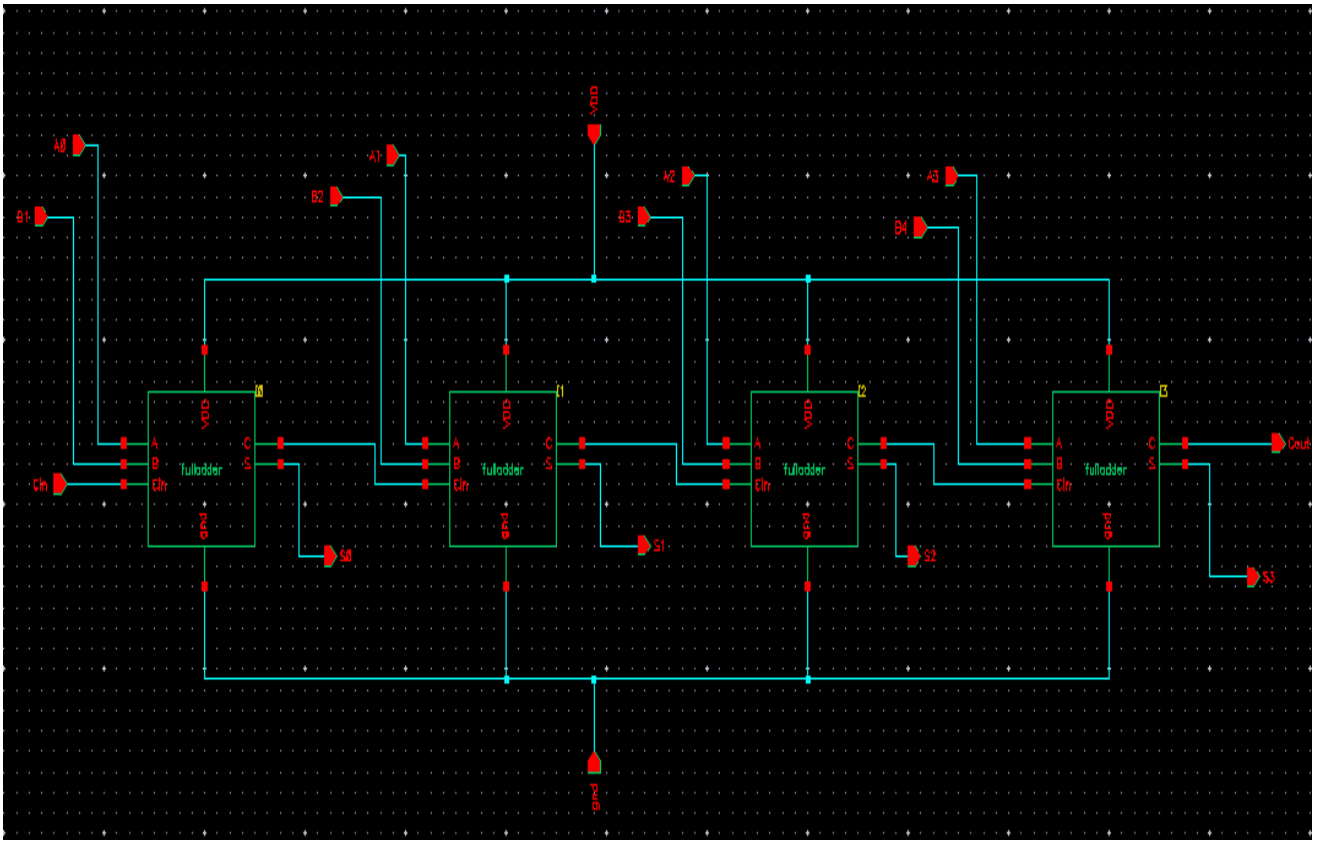

Fig 8:Schematic of 4-bit full adder in cadence.

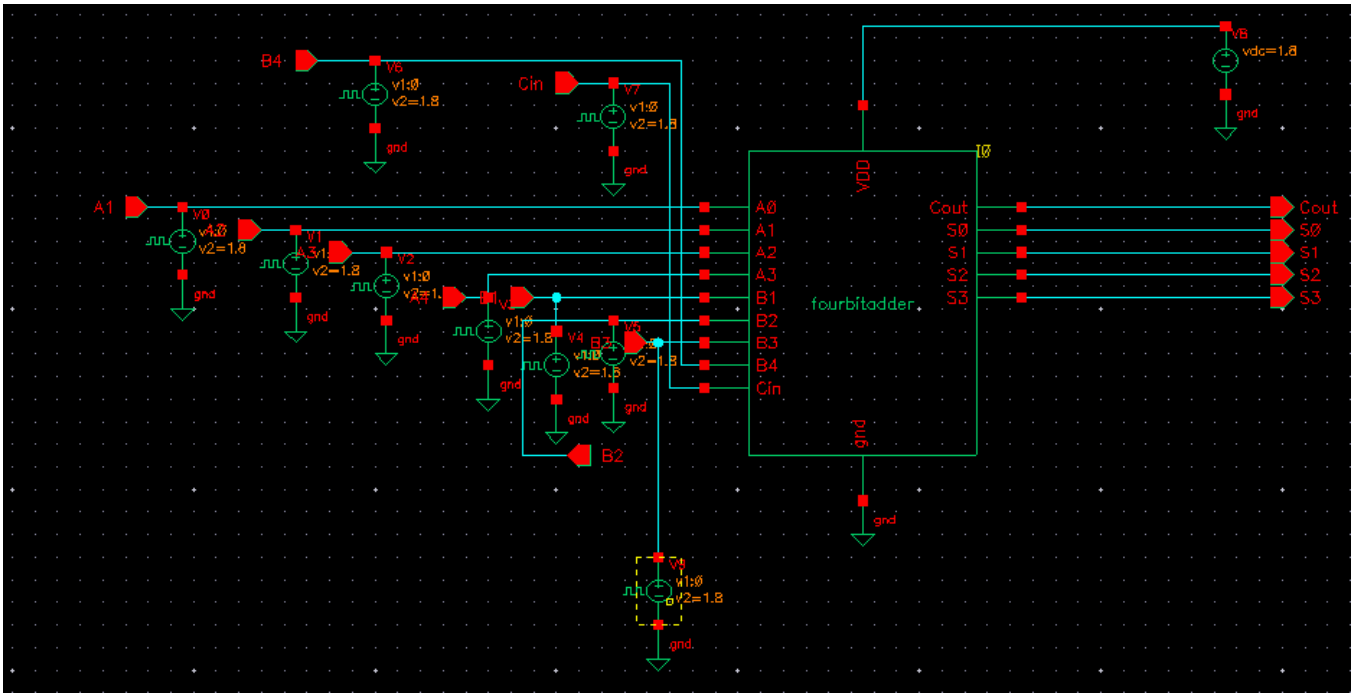

Fig 9:Schmatic of full adders using symbols.

The circuit shown above is black box of a 4 bit full adder with A1,A2,A3,A4,B1,B2,B3,B4 & Cin as input pins and S0,S1,S2,S3 & Cout as output pin with VDD=1.8V .

WAVEFORM:-

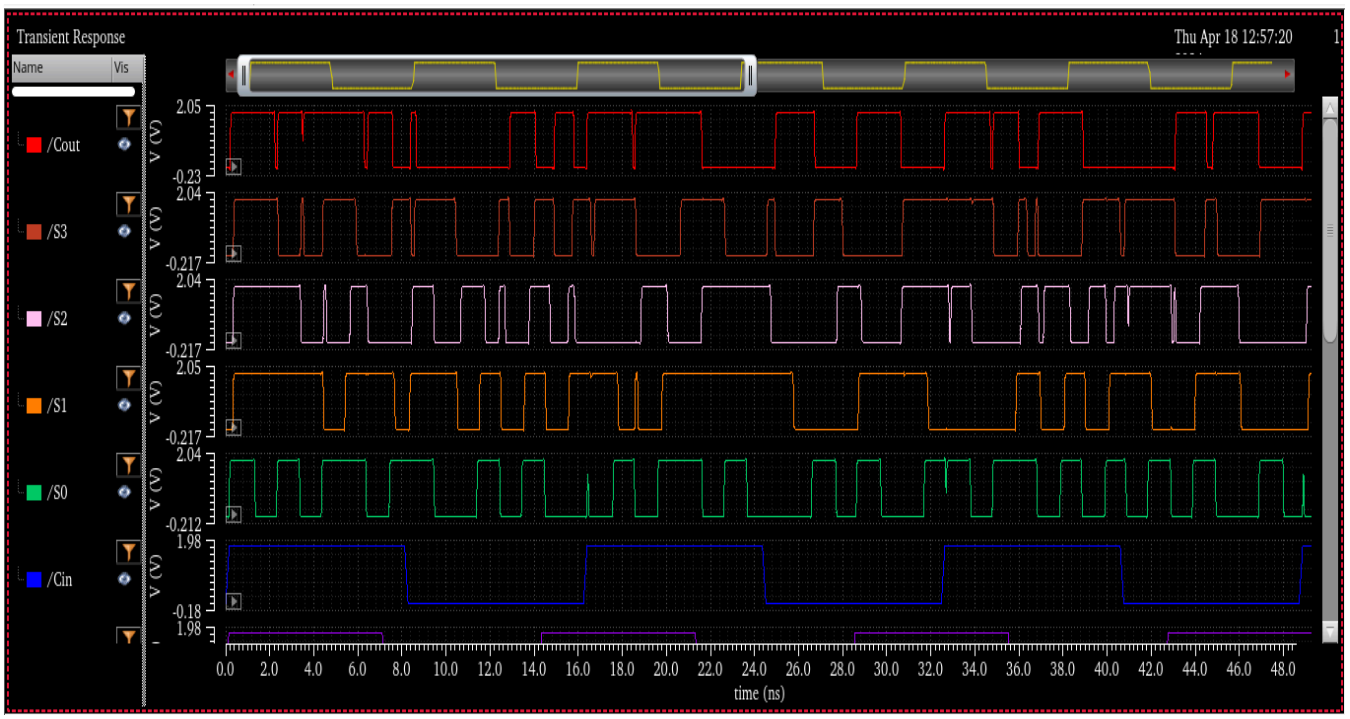

Fig 10a:

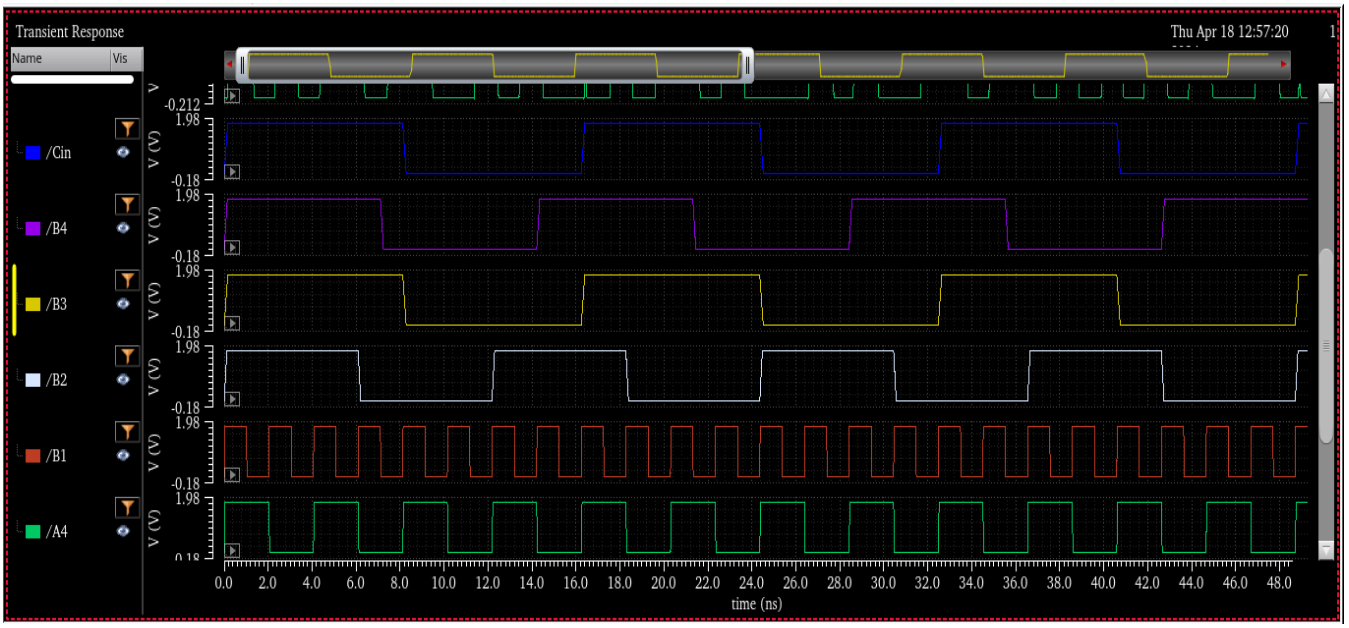

Fig10b:

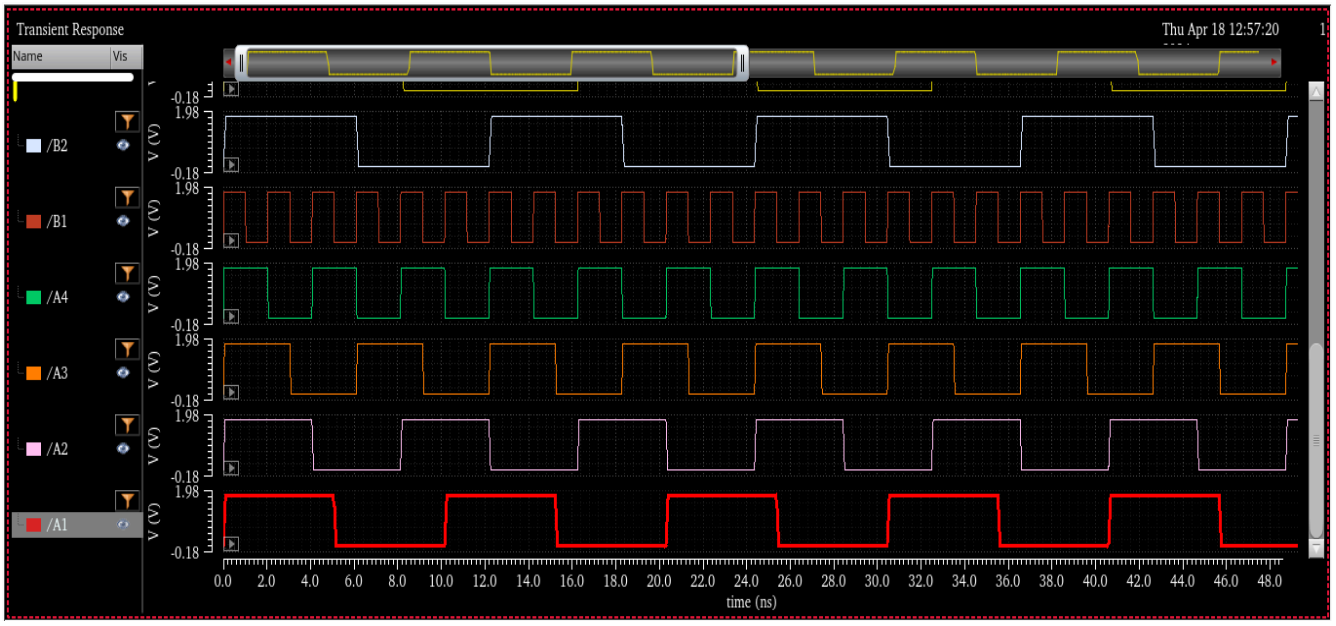

Fig 10c:

Fig 10a,10b,10c are graph represents the transient response of a full bit adder, by this we can verify how the above 4 bit adder works properly checking with outputs high or low. A1,A2,A3,A4,B1,B2,B3,B4,Cin are the input waveforms corresponding to that S0,S1,S2,S3 and Cout are generated.

DELAY CALCULATIONS:-

	Name/Signal/Expr	Value	Plot	Save	Save Options
2	A2		☑	☑	allv
3	A3		☑	☑	allv
4	A4		☑	☑	allv
5	B1		☑	☐	allv
6	B2		☑	☐	allv
7	B3		☑	☐	allv
8	B4		☑	☐	allv
9	Cin		☑	☐	allv
10	S0		☑	☐	allv
11	S1		☑	☐	allv
12	S2		☑	☐	allv
13	S3		☑	☐	allv
14	Cout		☑	☐	allv
15	A to Sum	309.044p	☑	☐	
16	B to Sum	349.044p	☑	☐	
17	Cin to Sum	279.044p	☑	☐	
18	Cin to Cout	131.422p	☑	☐	

Fig 11: Delay calculations table of 4-bit full adder.

The above table represents the delay calculations of the four bit full adder circuit .
A to sum,B to sum and Cin to sum refers to the propagation delay for the generation of sum output.
We can see that maximum delay if from B to Sum which can be referred as the propagation delay of the circuit and Cin to Cout represents the contamination delay of the circuit.

CONCLUSION:-

In conclusion, implementing a full adder circuit using logic gates offers valuable insights into the fundamental building blocks of digital circuits. This approach separates the logic for sum bit generation (using an XOR gate) and carry bit determination (with a combination of AND and OR gates). While achieving full adder functionality with minimal gates (XOR, AND, OR) is beneficial for understanding, it comes with limitations. Compared to pre-designed full adder integrated circuits (ICs), this design occupies more physical space due to the use of discrete gates and may experience slightly slower operation due to individual gate delays. Therefore, while less practical for real-world applications, constructing a full adder with logic gates serves as a valuable educational tool, providing a foundational understanding of the core principles behind binary addition, a critical operation in digital computers.