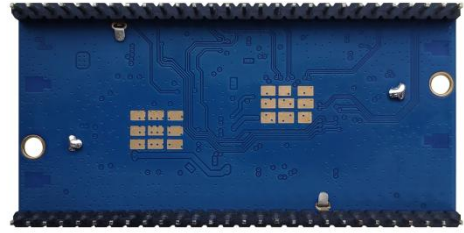# LB-LINK®

BL-M7628AR4

802.11ac 1200Mbps WLAN AP/Router Module Specification

SHENZHEN BILIAN ELECTRONIC CO., LTD

LB-LINK®

(Top View)

(Bottom View)

Module Name: BL-M7628AR4	
Module Type: 802.11a/b/g/n/ac 1200Mbps WLAN AP/Router Module	
Revision: V1.0	
Customer Approval:	
Company:	
Title:	
Signature:	Date:
BL-link Approval:	
Title:	
Signature:	Date:

Revision History

| Revision	Summary	Release Date
0.1	Initial release	2022-12-10
1.0	Officials release	2023-01-31

1、Introduction

BL-M7628AR4 is a highly integrated Dual-band WLAN AP/Router module. It combines 2T2R dual-band WLAN subsystem, 580MHz MIPS·24KEc CPU, 5-port fast Ethernet Switch and PHY, USB2.0 host, SD-XC, I2S/PCM and multiple low-speed IOs in a single module. It compatible IEEE802.11a/b/g/n/ac standard and provides the maximum PHY rate up to 300Mbps(2.4g)+867Mbps(5g), offering feature-rich wireless connectivity at high standards, and delivering reliable, cost-effective throughput from an extended distance.

1.1 Features

- WLAN Operating Frequency: 2.4~2.4835GHz and 5.15~5.85GHz
- WLAN features:

  2.4G Support 2T2R mode with 20/40 bandwidth, maximum PHY rate up to 300Mbps

  5G Support 2T2R mode with 20/40/80Mhz bandwidth, maximum PHY rate up to 867Mbps

  5G Support MU-MIMO and TX/RX Beamformer
- Connect to external antenna through IPEX connector
- Support USB 2.0 host interface allows to add 3G/LTE modem, H.264 ISP for wireless IP camera application
- Support eMMC(8 bits) or SD-XC(4 bits) interface
- Support high quality audio via 192Kbps/24bits I2S interface or VOIP application through PCM interface
- Support peripheral interfaces including I2C, SPI, UART, PWM interface and more GPIOs.
- Support touch panel, Bluetooth Low Energy, Zigbee/Z-Wave and Sub-1 GHz RF for smart home application
- Embedded DDR2 SDRAM 64MBytes(KGD)
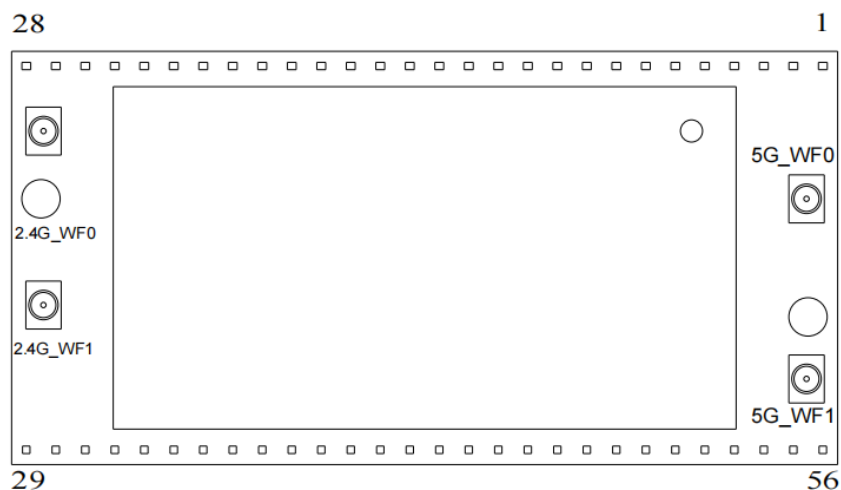- Power Supply: DC 5V±0.25V main power supply

1.2 Block Diagram
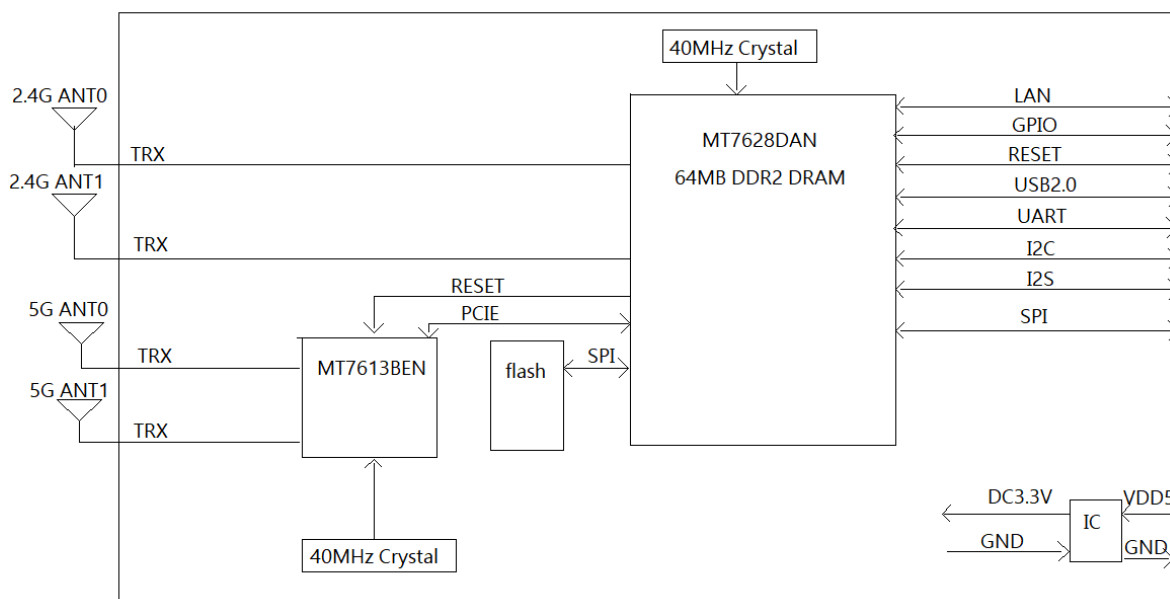
1.3 General Specifications

Module Name	BL-M7628AR4
Chipset	MT7628DAN, MT7613BEN
RAM & ROM	64MB DDR2 / 16MB SPI FLASH
WLAN Standard	IEEE 802.11 a/b/g/n/ac
Web management interface	Web IP: 192.168.16.1, Default password: admin
Work System	OpenWrt
Interface	USB2.0/UART/SPI/I2C/I2S/PCM/SD-XC/eMMC/GPIO
Antenna	IPEX / MHF-1 connector for external WLAN antenna;
Dimension	56.0*28.0*9.7mm(L*W*H)
Power Supply	DC 5.0V±0.25V@2000 mA (Peak)
Operation Temperature	-20℃ to +70℃
Operation Humidity	10% to 95% RH (Non-Condensing)

2. Pin Assignments

(Top View)

2.1 Pin Definition

No.	Pin Name	Type	I/O Level	Module Pin Description
1	GND	P		Ground
2	VIN	P		5.0V Main Power Supply
3	VIN	P		5.0V Main Power Supply
4	GND	P		Ground

5	NC	/		No connection
6	GND	P		Ground
7	5G_WLED	O	3.3V	5G WLAN LED active low output. The LED is always on after WLAN startup, and blinks when data transmission
8	SPI_CS0	O, IPU	3.3V	Default Function1: SPI chip select 0 output. Internal pull high by 4.7K resistor. Already used for on-board SPI NOR FLASH, be careful when connecting externally for other purposes! Function2: GPIO#10
9	SPI_MOSI	O, IPD	3.3V	1: SPI Master output/Slave input. Already used for on-board SPI NOR FLASH, be careful when connecting externally for other purposes! 2: GPIO#8. 3: Bootstrapping Pins (SPI_MOSI, SPI_CLK, SPI_CS1)_CHIP_MODE[2:0]=010: Boot XTAL SPI 3-Byte Addr Internal pull low by 4.7K resistor, do not pull high during power on!
10	SPI_MISO	I	3.3V	1: SPI Master input/Slave output. Already used for on-board SPI NOR FLASH, be careful when connecting externally for other purposes! 2: GPIO#9
11	SPI_CLK	O, IPU	3.3V	1: SPI clock output. Already used for on-board SPI NOR FLASH, be careful when connecting externally for other purposes! 2: GPIO#7. 3: Bootstrapping Pins (SPI_MOSI, SPI_CLK, SPI_CS1)_CHIP_MODE[2:0]=010: Boot XTAL SPI 3-Byte Addr Internal pull high by 4.7K resistor, do not pull low during power on!
12	SPI_CS1	O, IPD	3.3V	1: SPI chip select 1 output. 2: GPIO#6. 3: Reference clock output 0. 4: Bootstrapping Pins (SPI_MOSI, SPI_CLK, SPI_CS1)_CHIP_MODE[2:0]=010: Boot XTAL SPI 3-Byte Addr Internal pull low by 4.7K resistor, do not pull high during power on!
13	PERST_N	O, IPU	3.3V	1: PCIe device reset active low output. Already used for on-board 5G WLAN, be careful when connecting externally for other purposes! 2: GPIO#36. 3: Bootstrapping Pin_XTAL_FREQ_SEL=1: 40MHz

				Internal pull high by 4.7K resistor, do not pull low during power on!
14	REF_CLKO	O, IPD	3.3V	1: Reference clock output. 2: GPIO#37. Internal pull low
15	RST_PBC	I, IPU	3.3V	1: WDT_RST_N, Watchdog reset output. 2: GPIO#38, already used for default configure reset button by the software, active low input, internal pull high by 4.7K resistor.
16	CPU_RST_N	I, IPU	3.3V	System power on reset, active low input. RC reset circuit with 68K resistor and 1uF capacitor integrated in the module. If not use, can be left float!
17	LINK4	O	3.3V	1: 10/100 PHY Port4 Link/ACT LED, active Low output (DBG_JTAG_MODE=1). 2: JTAG_RST_N, JTAG reset active low input (DBG_JTAG_MODE=0). 3: GPIO#39
18	LINK3	O	3.3V	1: 10/100 PHY Port3 Link/ACT LED, active Low output (DBG_JTAG_MODE=1). 2: JTAG_CLK, JTAG clock input (DBG_JTAG_MODE=0). 3: GPIO#40
19	LINK2	O	3.3V	1: 10/100 PHY Port2 Link/ACT LED, active Low output (DBG_JTAG_MODE=1). 2: JTAG_TMS, JTAG test mode selection input (DBG_JTAG_MODE=0). 3: GPIO#41
20	LINK1	O	3.3V	1: 10/100 PHY Port1 Link/ACT LED, active Low output (DBG_JTAG_MODE=1). 2: JTAG_TDI, JTAG test data input (DBG_JTAG_MODE=0). 3: GPIO#42
21	LINK0	O	3.3V	1: 10/100 PHY Port0 Link/ACT LED, active Low output (DBG_JTAG_MODE=1). 2: JTAG_TDO, JTAG test data output (DBG_JTAG_MODE=0). 3: GPIO#43
22	2.4G_WLAN_LED	O	3.3V	1: 2.4G WLAN LED active low output. The LED is always on after WLAN startup, and blinks when data transmission. 2: GPIO#44

23	UART_TXD1	O, IPU	3.3V	1: UART1 Lite TXD, output.
				2: GPIO#45.
				3: PWM0, Pulse Width Modulation channle0 output.
				4: Bootstrapping Pin_
				    DBG_JTAG_MODE=0: JTAG_MODE
				    DBG_JTAG_MODE=1: EPHY_LED (Default, internal pull

				high by 4.7K resistor)
24	UART_RXD1	I	3.3V	1: UART1 Lite RXD, input. 2: GPIO#46. 3: PWM1, PWM channle1 output
25	I2S_SDI	I	3.3V	1: I2S data Input. 2: I2C_SCLK, I2C clock output. 3: GPIO#0. 4: PCMDRX, PCM data receive
26	I2S_SDO	O, IPD	3.3V	1: I2S data output. 2: I2C_SD, I2C serial data I/O. 3: GPIO#1. 4: PCMDTX, PCM data transmit. 5: Bootstrapping Pin_ 　DRAM_TYPE=0: DDR2 (Default, internal pull low by 4.7K 　　resistor, do not pull high during power on!)
27	I2S_WS	O	3.3V	1: I2S word select output. 2: I2C_SCLK, I2C clock output. 3: GPIO#2. 4: PCMCLK, PCM clock output
28	I2S_CLK	O	3.3V	1: I2S clock output. 2: I2C_SD, I2C serial data I/O. 3: GPIO#3. 4: PCMFS, PCM SYNC output
29	I2C_SD	I/O	3.3V	1: I2C serial data I/O (no internal pull high resistor). 2: GPIO#5
30	I2C_SCLK	O	3.3V	1: I2C clock output (no internal pull high resistor). 2: GPIO#4
31	GPIO_0	I/O	3.3V	1: GPIO#11. 2: Ref_CLKO, reference clock output. 3: PERST_N, PCIe device reset active low output
32	UART_RXD0	I, IPD	3.3V	1: UART0 Lite RXD input. UART0 is the default interface for 　software debugging and logging. 2: GPIO#13. Internal pull low by 1K resistor.
33	UART_TXD0	O, IPD	3.3V	1: UART0 Lite TXD output. 2: GPIO#12. 3: Bootstrapping Pin_ 　EXT_BGCK=0: Normal (Default, internal pull low by 4.7K 　　resistor, do not pull high during power on !)
34	RXIP0	AI/O		10/100M PHY Port0 MDI/MDI-X differential pair RXP
35	RXIN0	AI/O		10/100M PHY Port0 MDI/MDI-X differential pair RXN

36	TXOP0	AI/O		10/100M PHY Port0 MDI/MDI-X differential pair TXP
37	TXON0	AI/O		10/100M PHY Port0 MDI/MDI-X differential pair TXN
38	TXOP1	A_I/O	3.3V	1: 10/100M PHY Port1 MDI/MDI-X differential pair TXP. 2: SPIS_CS, SPI_Slave chip select input. 3: GPIO#14. 4: PWM0, PWM channel0 output
39	TXON1	A_I/O	3.3V	1: 10/100M PHY Port1 MDI/MDI-X differential pair TXN. 2: SPIS_CLK, SPI_Slave clock input. 3: GPIO#15. 4: PWM1, PWM channel1 output
40	RXIP1	A_I/O	3.3V	1: 10/100M PHY Port1 MDI/MDI-X differential pair RXP. 2: SPIS_MISO, SPI_Slave serial data output. 3: GPIO#16. 4: UART_TXD2, UART2 TXD output
41	RXIN1	A_I/O	3.3V	1: 10/100M PHY Port1 MDI/MDI-X differential pair RXN. 2: SPIS_MOSI, SPI_Slave serial data input. 3: GPIO#17. 4: UART_RXD2, UART2 RXD input
42	RXIP2	A_I/O	3.3V	1: 10/100M PHY Port2 MDI/MDI-X differential pair RXP. 2: PWM0, PWM channel0 output. 3: GPIO#18. 4: SD_D7, eMMC I/O data7
43	RXIN2	A_I/O	3.3V	1: 10/100M PHY Port2 MDI/MDI-X differential pair RXN. 2: PWM1, PWM channel1 output. 3: GPIO#19. 4: SD_D6, eMMC I/O data6
44	TXOP2	A_I/O	3.3V	1: 10/100M PHY Port2 MDI/MDI-X differential pair TXP. 2: UART_TXD2, UART2 TXD output. 3: GPIO#20. 4: PWM2, PWM channel2 output. 5: SD_D5, eMMC I/O data5
45	TXON2	A_I/O	3.3V	1: 10/100M PHY Port2 MDI/MDI-X differential pair TXN. 2: UART_RXD2, UART2 RXD input. 3: GPIO#21. 4: PWM3, PWM channel3 output. 5: SD_D4, eMMC I/O data4

46	TXOP3	A_I/O	3.3V	1: 10/100M PHY Port3 MDI/MDI-X differential pair TXP. 2: SD_WP, SD/eMMC write protect input. 3: GPIO#22
47	TXON3	A_I/O	3.3V	1: 10/100M PHY Port3 MDI/MDI-X differential pair TXN. 2: SD_CD, SD/eMMC card detection input. 3: GPIO#23
48	RXIP3	A_I/O	3.3V	1: 10/100M PHY Port3 MDI/MDI-X differential pair RXP. 2: SD_D1, SD/eMMC I/O data1. 3: GPIO#24
49	RXIN3	A_I/O	3.3V	1: 10/100M PHY Port3 MDI/MDI-X differential pair RXN. 2: SD_D0, SD/eMMC I/O data0. 3: GPIO#25
50	RXIP4	A_I/O	3.3V	1: 10/100M PHY Port4 MDI/MDI-X differential pair RXP. 2: SD_CLK, SD/eMMC clock output. 3: GPIO#26
51	RXIN4	A_I/O	3.3V	1: 10/100M PHY Port4 MDI/MDI-X differential pair RXN. 2: SD_CMD, SD/eMMC command I/O. 3: GPIO#27
52	TXOP4	A_I/O	3.3V	1: 10/100M PHY Port4 MDI/MDI-X differential pair TXP. 2: SD_D3, SD/eMMC I/O data3. 3: GPIO#28
53	TXON4	A_I/O	3.3V	1: 10/100M PHY Port4 MDI/MDI-X differential pair TXN. 2: SD_D2, SD/eMMC I/O data2. 3: GPIO#29
54	USB_DP	AI/O		USB2.0 Host Port0 differential pair data+
55	USB_DN	AI/O		USB2.0 Host Port0 differential pair data-
56	GND	P		Ground
	2.4G_WF0	RF		2.4GHz RF port0 IPEX connector
	2.4G_WF1	RF		2.4GHz RF port1 IPEX connector
	5G_WF0	RF		5GHz RF port0 IPEX connector
	5G_WF1	RF		5GHz RF port1 IPEX connector

P: Power or Ground;   I/O: In/Output bi-directional;   I: Input;   O: Output;   AI/O: Analog In/Output;

A_I/O: Analog and digital multiplexed I/O;   RF: Analog RF Port or RF Ground;   NC: Not connected;

IPD: Internal Pull Low;   IPU: Internal Pull High;

Note: Some pins are shared with GPIO to provide maximum flexibility for system designers. The module provides up to 41 GPIO Pins. Users can configure GPIO1_MODE and GPIO2_MODE registers in the MT7628 System

Control block to specify the pin function. For more information, see the MT7628 Programmer's Guide. Unless specified explicitly, all the GPIO pins are in input mode after reset.

3. Electrical and Thermal Specifications

3.1 Recommended Operating Conditions

Parameters		Min	Type	Max	Units
*Ambient Operating Temperature		-20	25	70	℃
External Antenna VSWR			1.7	2	/
Supply Voltage	VIN	4.75	5.0	5.25	V

Note: The Dual-Band WLAN AP/Router Module will generate more heat, in order to ensure the module work stably within rated temperature range, additional heat dissipation devices must be added by customers.

3.2 Digital I/O DC Specifications

Symbol	Parameter	Min	Type	Max	Units
VIH	Input High Voltage	3.3V*0.625	--	3.3V+0.3	V
VIL	Input Low Voltage	-0.3	--	3.3V*0.25	V
VOH	Output High Voltage	3.3V*0.75	--	3.3V+0.3	V

3.3 Power On Sequence

Symbol	Description	Min	Max	Unit
tPRST	External Power-on Reset Period	6.0		ms
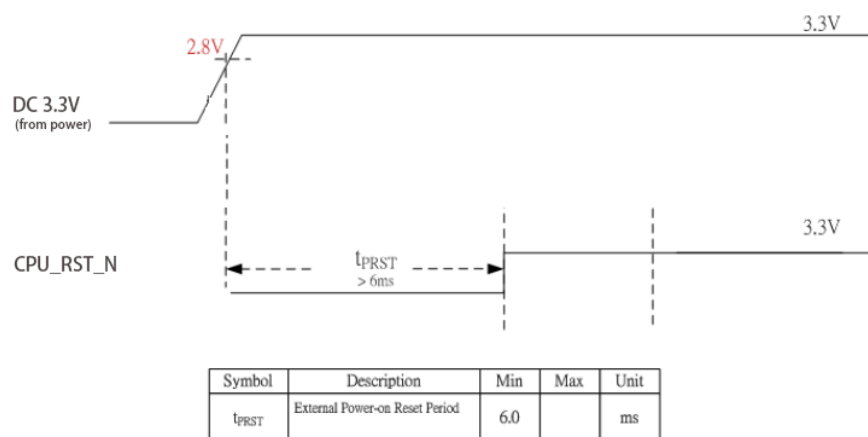
Note: The module integrated DC-DC circuit inputs VIN 5V and outputs DC 3.3V internal power supply.

3.4 Current Consumption

Conditions : VIN=5.0V ; Ta:25℃ ;			
Use Case: Dual-band WLAN AP application with 1 Fast ETH Port	**Current**		
	Typ(I_{RMS})	MAX(I_{Peak})	Units

WLAN Unassociated	340	680	mA
2.4G WLAN UDP throughput TX 90Mbps	597	1260	mA
2.4G WLAN UDP throughput RX 90Mbps	436	880	mA
2.4G WLAN UDP throughput TRX 180Mbps	465	860	mA
5G WLAN UDP throughput TX 90Mbps	539	980	mA
5G WLAN UDP throughput RX 90Mbps	482	1000	mA
5G WLAN UDP throughput TRX 180Mbps	566	960	mA
2.4G+5G WLAN UDP throughput TX 90Mbps	818	1300	mA
2.4G+5G WLAN UDP throughput RX 90Mbps	566	1380	mA
2.4G+5G WLAN UDP throughput TRX 180Mbps	692	1300	mA
2.4G 11b 1MbpsTX@18dBm (1TX RF test)	692	1300	mA
2.4G 11b 11MbpsTX@18dBm (1TX RF test)	570	960	mA
2.4G 11g 54Mbps TX@16dBm (1TX RF test)	436	1000	mA
2.4G 11n HT20 MCS8 TX@17dBm (2TX RF test)	695	1300	mA
2.4G 11n HT40 MCS15 TX@15dBm (2TX RF test)	487	1220	mA
5G 11a 6Mbps TX@18dBm (1TX RF test)	941	1500	mA
5G 11a 54Mbps TX@16dBm (1TX RF test)	780	1400	mA
5G 11n HT20 MCS8 TX@17dBm (2TX RF test)	901	1500	mA
5G 11n HT40 MCS15 TX@14dBm (2TX RF test)	677	1300	mA
5G 11ac VHT 80MHz MCS0 TX@17dBm (2TX RF test)	903	1580	mA
5G 11ac VHT 80MHz MCS9 TX@14dBm (2TX RF test)	696	1380	mA
5G 11ac VHT 80MHz MCS9 RX (2RX RF test)	392	680	mA

4. WLAN RF Specifications

4.1 2.4G WLAN RF Specification

Conditions : VIN=5.0V ; Ta:25℃	
Features	**Description**
WLAN Standard	IEEE 802.11b/g/n
Frequency Range	2.4~2.4835GHz (2.4GHz ISM Band)
Channels	Ch1~Ch13 (For 20MHz Channels)

Modulation	802.11b (DSSS): CCK, DQPSK, DBPSK;
	802.11g (OFDM): BPSK, QPSK, QAM16, QAM64;
	802.11n (OFDM): BPSK, QPSK, QAM16, QAM64;
Data Rate	802.11b: 1, 2, 5.5, 11Mbps;
	802.11g: 6, 9, 12, 18, 24, 36, 48, 54Mbps;
	802.11n (HT20): MCS0~MCS7(1T1R_SISO) 6.5~72.2Mbps;
	802.11n (HT20): MCS8~MCS15(2T2R_MIMO) 13~144.4Mbps;
	802.11n (HT40): MCS0~MCS7(1T1R) 13.5~150Mbps;
	802.11n (HT40): MCS8~MCS15(2T2R) 27~300Mbps;
Frequency Tolerance	≦±20ppm

2.4G Transmitter Specifications (2.4G_WF0&2.4G_WF1)			
TX Rate	TX Power (dBm)	Power Tolerance (dBm)	EVM (dB)
802.11b@1~11Mbps	18	±2	≦-15
802.11g@6Mbps	18	±2	≦-15
802.11g@54Mbps	16	±2	≦-25
802.11n@HT20_MCS0	16	±2	≦-10
802.11n@HT20_MCS7	14	±2	≦-28
802.11n@HT40_MCS0	16	±2	≦-10
802.11n@HT40_MCS7	14	±2	≦-28

2.4G Receiver Specifications (2.4G_WF0&2.4G_WF1)			
RX Rate	Min Input Level(Typ dBm)	Max Input Level(Typ dBm)	PER
802.11b@1Mbps	-95	-10	< 8%
802.11b@11Mbps	-87	-10	< 8%
802.11g@6Mbps	-92	-10	< 10%
802.11g@54Mbps	-75	-10	< 10%
802.11n@HT20_MCS0	-91	-10	< 10%
802.11n@HT20_MCS7	-71	-10	< 10%
802.11n@HT40_MCS0	-89	-10	< 10%
802.11n@HT40_MCS7	-68	-10	< 10%

4.2 5G WLAN RF Specification

Conditions: VIN=5V; Ta:25℃	
Features	Description
WLAN Standard	IEEE 802.11a/n/ac
Frequency Range	5.15~5.25GHz; 5.25~5.35GHz; 5.47~5.73GHz;5.735~5.835GHz (5GHz ISM Band)

Channels	Ch36~Ch48; Ch52~Ch64; Ch100~Ch140; Ch149~Ch165 (For 20MHz Channels)
Modulation	802.11a (OFDM): BPSK, QPSK, QAM16, QAM64; 802.11n (OFDM): BPSK, QPSK, QAM16, QAM64; 802.11ac (OFDM): BPSK, QPSK, QAM16, QAM64, QAM256;
Data Rate	802.11a: 6, 9, 12, 18, 24, 36, 48, 54Mbps; 802.11n (HT20): MCS0~MCS7(1T1R_SISO) 6.5~72.2Mbps; 802.11n (HT20): MCS8~MCS15(2T2R_MIMO) 13~144.4Mbps; 802.11n (HT40): MCS0~MCS7(1T1R) 13.5~150Mbps; 802.11n (HT40): MCS8~MCS15(2T2R) 27~300Mbps; 802.11ac (VHT20): MCS0~MCS8(1T1R) 6.5~86.7Mbps; 802.11ac (VHT20): MCS0~MCS8(2T2R) 13~173.3Mbps; 802.11ac (VHT40): MCS0~MCS9(1T1R)13.5~200Mbps; 802.11ac (VHT40): MCS0~MCS9(2T2R)27~400Mbps; 802.11ac (VHT80): MCS0~MCS9(1T1R)29.3~433.3Mbps; 802.11ac (VHT80): MCS0~MCS9(2T2R)58.5~866.7Mbps;
Frequency Tolerance	≦ ±20ppm

5G Transmitter Specifications (5G_WF0&5G_WF1)

TX Rate	TX Power (dBm)	Power Tolerance (dBm)	EVM (dB)
802.11a@6Mbps	18	±2	≦-10
802.11a@54Mbps	16	±2	≦-25
802.11n@HT20_MCS0	16	±2	≦-13
802.11n@HT20_MCS7	14	±2	≦-28
802.11n@HT40_MCS0	16	±2	≦-13
802.11n@HT40_MCS7	14	±2	≦-28
802.11ac@VHT80_MCS0	16	±2	≦-13
802.11ac@VHT80_MCS9	14	±2	≦-32

5G Receiver Specifications (5G_WF0&5G_WF1)

RX Rate	Min Input Level (Typ dBm)	Max Input Level (Typ dBm)	PER
802.11a@6Mbps	-94	-10	< 10%
802.11a@54Mbps	-77	-10	< 10%
802.11n@HT20_MCS0	-93	-10	< 10%
802.11n@HT20_MCS7	-72	-10	< 10%

802.11n@HT40_MCS0	-90	-10	< 10%
802.11n@HT40_MCS7	-70	-10	< 10%
802.11ac@VHT80_MCS0	-89	-10	< 10%
802.11ac@VHT80_MCS9	-61	-10	< 10%

5. Mechanical Specifications

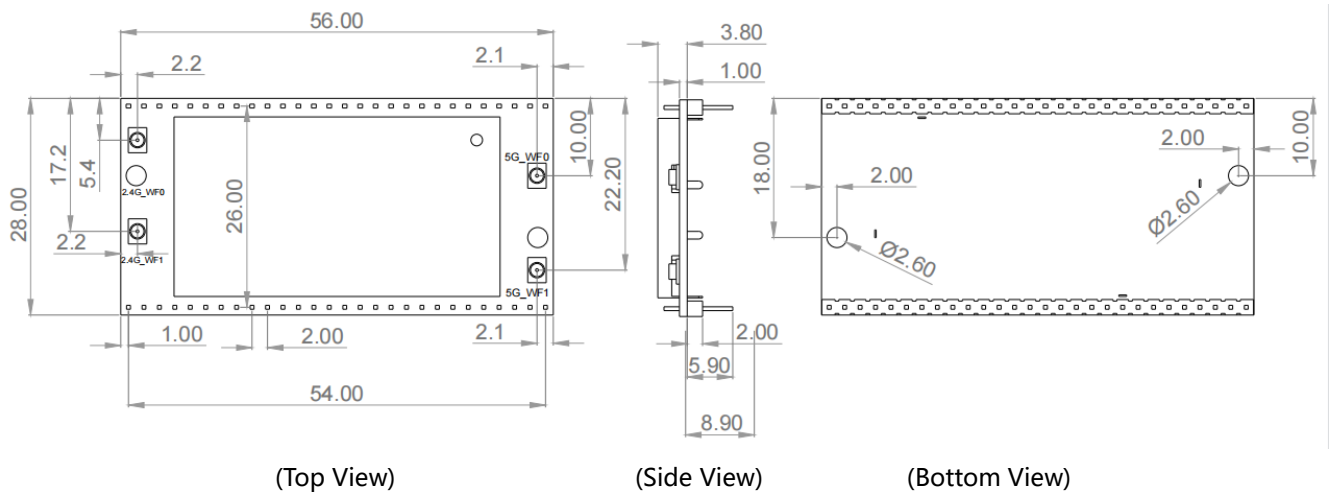## 5.1 Module Outline Drawing(Units:mm)

(Top View)   (Side View)
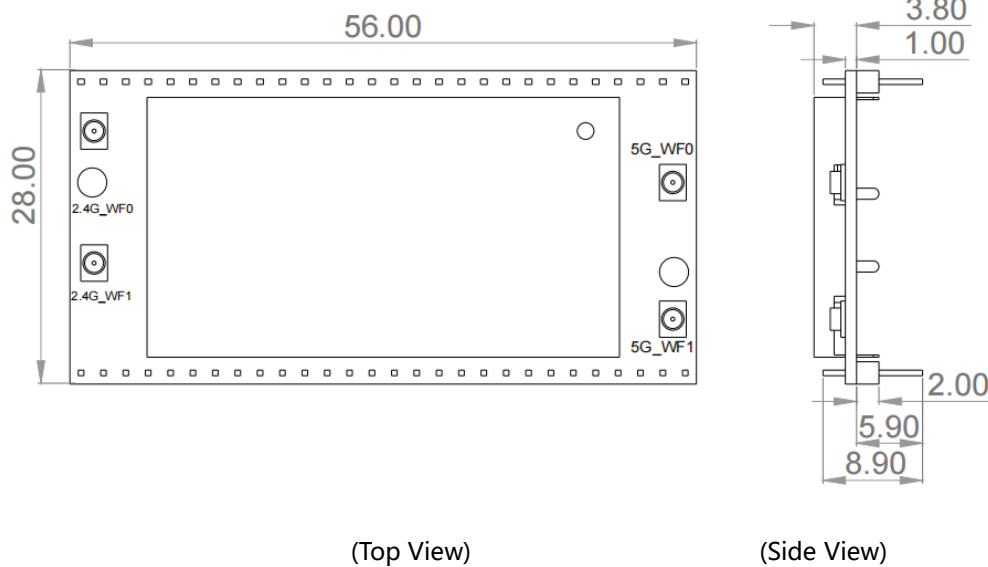
Module dimension: 56.0*28.0*9.7mm(L*W*H; Tolerance: ±0.15mm)
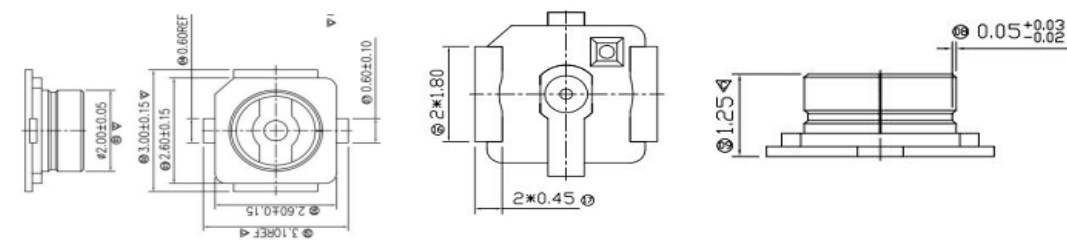
IPEX / MHF-1 connector dimension: 3.1*3.0*1.2mm (L*W*H, Ø2.0mm)

5.2 Mechanical Dimensions(Units:mm)

(Top View)   (Side View)   (Bottom View)

6. Application Information

6.1 Typical Application Circuit
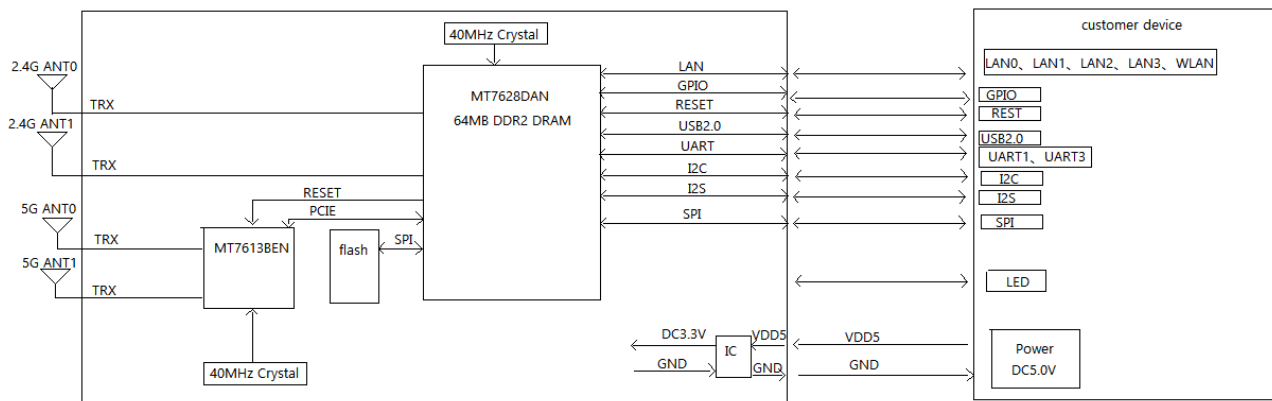
6.2 HW Application Note

6.2.1 External Antenna Isolation

Isolation of RF 2.4G_WF0 and 2.4G_WF1 ≥15dB(2.4G band) for better MIMO Application;

Isolation of RF 5G_WF0 and 5G_WF1 ≥15dB(5G band) for better MIMO Application.

6.2.2 Power requirement

Supply Voltage Range: DC 4.75~5.25V & Max Ripple Voltage <300mV;

Maximum RMS current ≥1500mA and Maximum Peak current ≥2000mA;

For achieve fast transient response, a current mode buck converter recommended.

6.2.3 interface Design Guidelines

A、BL-M7628AR4 supports a USB host port which is fully compliant with USB v2.0 specification.

B、The USB high speed differential pair should be maintain $90\Omega \pm 5\Omega$ differential impedance.

C、USB signal pairs as short as possible, avoid interference from Power and other signals.
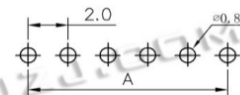
6.3 Recommend PCB Layout Footprint(Units:mm)
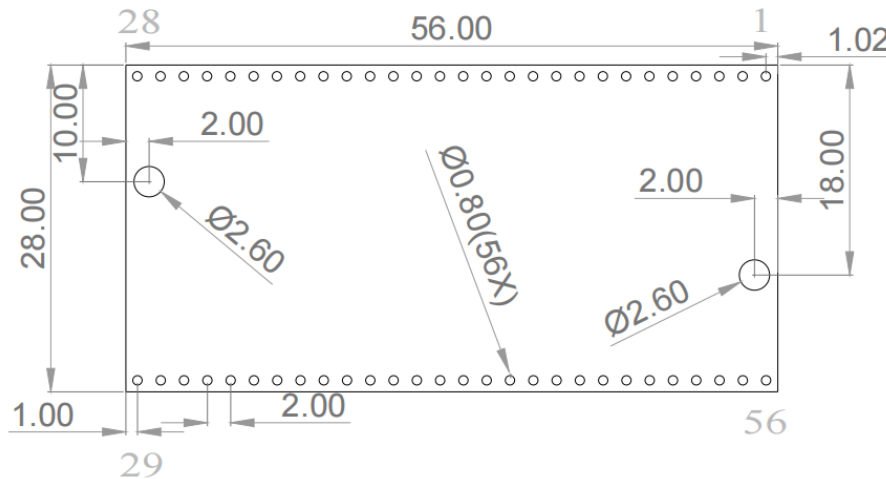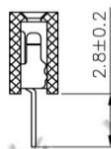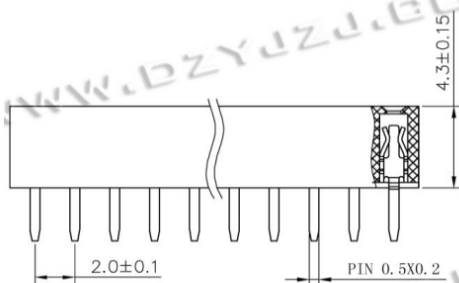

6.3 Recommend Connectors (Units:mm)
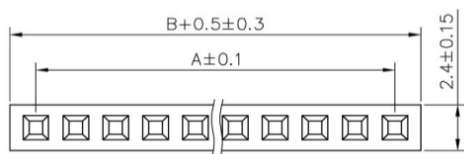
A=54.00
B=56.00
PIN=28

RECOMMEND P.C.B LAYOUT
PCB TOLERANCE:±0.05 (TOP VIEW)

SPECIFICATIONS

Current Rating: 1.5 Amps
Insulation Resistance:1000MΩ Min
Contact Resistance: 20mΩ Max
Withstanding Voltage: AC 500V
Operation Temperature:-40° to+105°
Contact Material: Brass
Standard: PA6T
Insrlator Material: Polyester(UL 94V-0)
Contact Plating: Gold Flash
Max.Processing Temp: 240° C for30-60seconds
(260° C for 5 seconds)

Note: Silicone rubber with high thermal conductivity is used between chipset and shield cover inside the module, it cannot withstand the high temperature of reflow soldering/wave soldering. So the module can be

installed on customer's main board with connectors, or manually soldered the module Pins to through-hole pads of customer's main board.

6.5 Thermal Dissipation

BL-M7628AR4 is designed to work on an extreme temperature range, to make sure the module can work properly for a long time and achieve a better performance on conditions like maximum power or high data transmission. In order to enhance the thermal dissipation capability, it is necessary to add a heat-sink on the shielding cover of the module:

A: Install the module on the customer's main board.
B: Apply thermal conductive silicone grease evenly on shielding cover of the module.
C: Install the heat-sink, the aluminum-extruded heat-sink with four standoffs recommended.
D: Fix the heat-sink with screws.
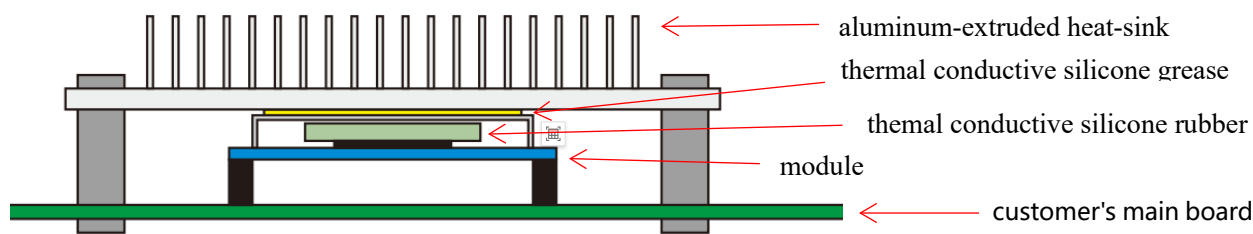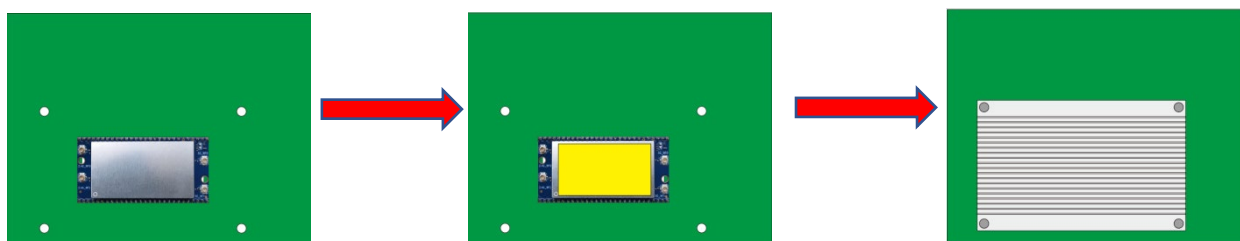
7. Key Components Of Module

No.	Parts	Specification	Manufacturer	Note
1	Chipset	MT7628DAN，MT7613BEN	MediaTek Inc.	
2	PCB	BL_M7628AR4	Shenzhen TieFa Technology CO. LTD	
			Guangdong KINGSHINE ELECTRONICS CO., LTD	
			Qu zhou Sunlord Electronics CO., LTD	
3	Crystal	40MHz	HUBEI TKD ELECTRONICS TECHNOLOGY CO., LTD.	

			LUCKI CM ELECTRONICS CO., LTD	
			HOSONIC ELECTRONIC CO., LTD.	

8. Package and Storage Information

8.1 Package Dimensions

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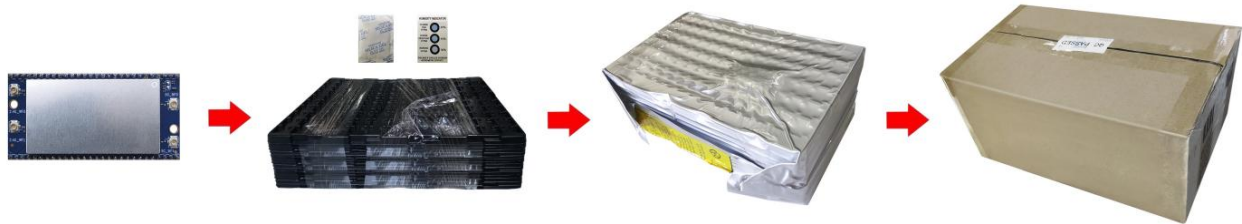
Package specification:
1. 25 modules per blister plate and 200 modules per box.
2. The blister is bound with wire membrane and put into anti-static vacuum bag.
3. Put 1 bag of dry beads (20g) in each anti-static vacuum bag. 1 pcs 3 point humidity card.
4. The outer box size is 35.2*21.5*15.5cm.

8.2 Storage Conditions

Absolute Maximum Ratings:
    Storage temperature: -40℃ to +85℃,
    Storage humidity: 10% to 95 (Non-Condensing)
Recommended Storage Conditions:
    Storage temperature: 5℃ to +40℃,
    Storage humidity: 20% to 90% RH

Please use this Module within 12month after vacuum-packaged.
    The Module shall be stored without opening the packing.
    After the packing opened, the Module shall be used within 72hours.
    When the color of the humidity indicator in the packing changed,
    The Module shall be baked before use.
    Baking condition: 60℃, 24hours, 1time.

ESD Sensitivity:
    ESD Protection: 3KV(HBM ,Maximum rating)
    The Module is a static-sensitive electronic device.
    Do not operate or store near strong electrostatic fields.
    Take proper ESD precautions!

ESD CAUTION