

# 4-Bit Adder and Subtractor with Integrated Chips

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## 1 High level circuit diagrams

Here are some block diagrams that describe the overall components in our circuits and the way they connect with one another. Please note that these do not include the logic used to control various inputs such as shift controls to the shift registers, reset inputs, and the counter clock. See later sections for that information!

The 4-bit adder is a serialized single-bit adder that is fed inputs from shift registers one bit at a time. The flip flop stores carries from one operation to the next, linking together single-bit operations to function appropriately for multiple bits. the output is stored in a "result" shift register one bit at a time, and all timed components are controlled by a clock. A decade counter controls the parallel loading, shifting, and holding capabilities of the shift registers.

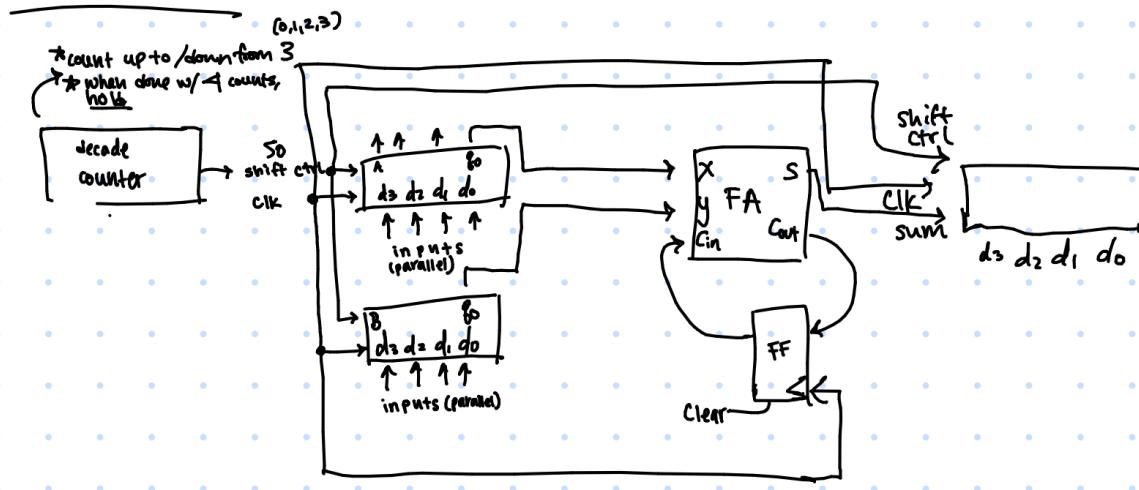


Figure 1: High level adder diagram.

The subtractor uses all the same components as the adder except an additional full adder chip that adds one to the answer. Multiplexers are used to switch between the two cases (adding vs subtracting).

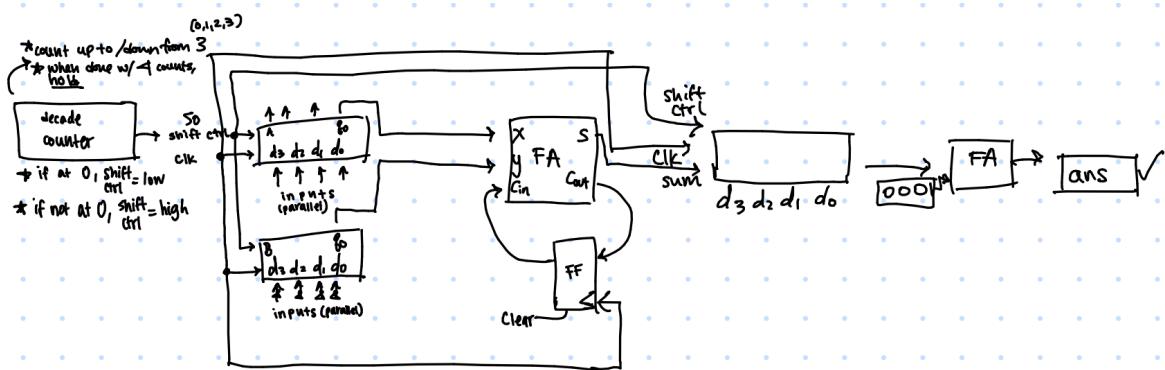


Figure 2: High level subtractor diagram.

## 2 Detailed circuit diagrams

Here are our detailed circuit diagrams, including all logic and reset components. “Tunnel” inputs and outputs with respective labels have been used here to avoid chaotic wiring. (The multiplexer circuit diagram is on page 3 to preserve the size of the figure.)

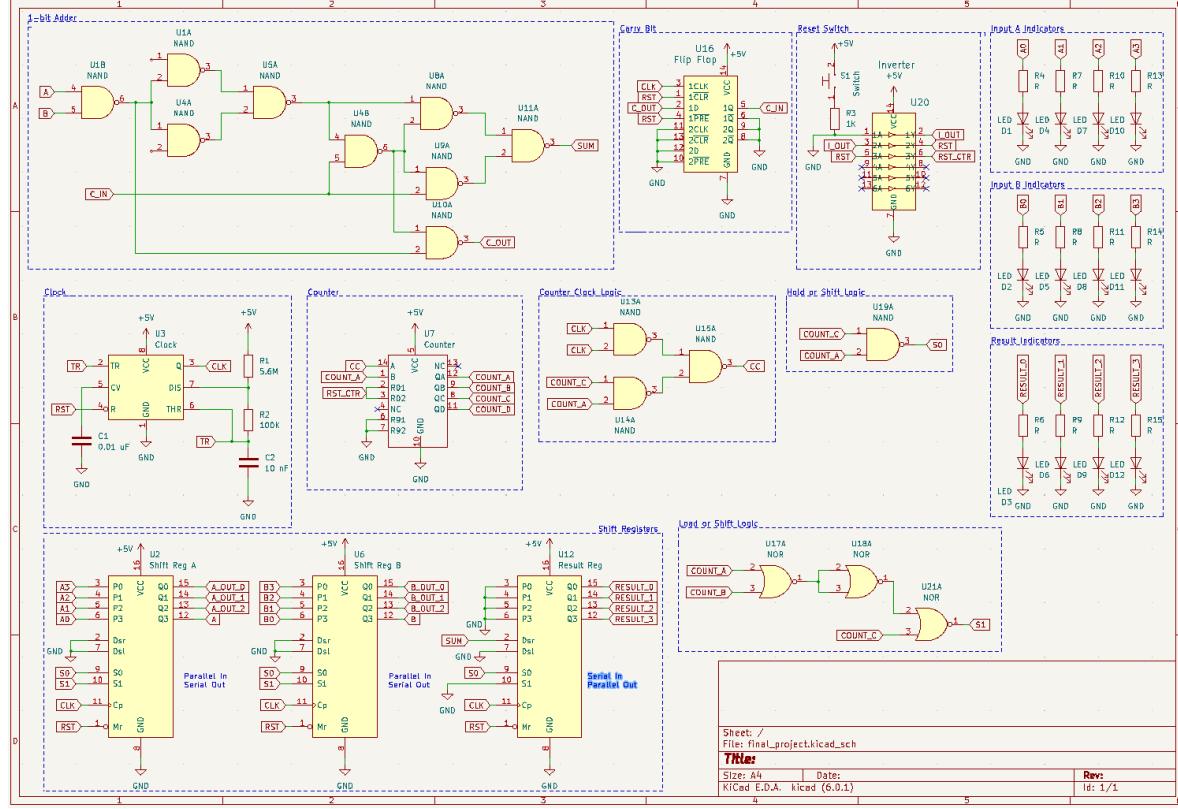


Figure 3: Adder circuit diagram.

## 3 Shift register and counter logic

We used various logic gates to synthesize three phases in which this circuit operates:

1. The parallel load stage (count = 1), where the input bits to the shift registers are loaded in.
2. The shifting and adding stage (count = 1, 2, 3, 4), where shifting and adding of the four bit number (one bit per count) takes place.
3. The hold stage (count = 5), where the counter stops counting and shift registers hold their contents still. This allows users to read the result of the operation and lasts until the circuit is reset.

See figure 5 for the full truth table describing this logic.

## 4 Circuit pictures: full circuit

Before going over the specific components of this circuit, we present a picture of the completed circuit (see figure 6).

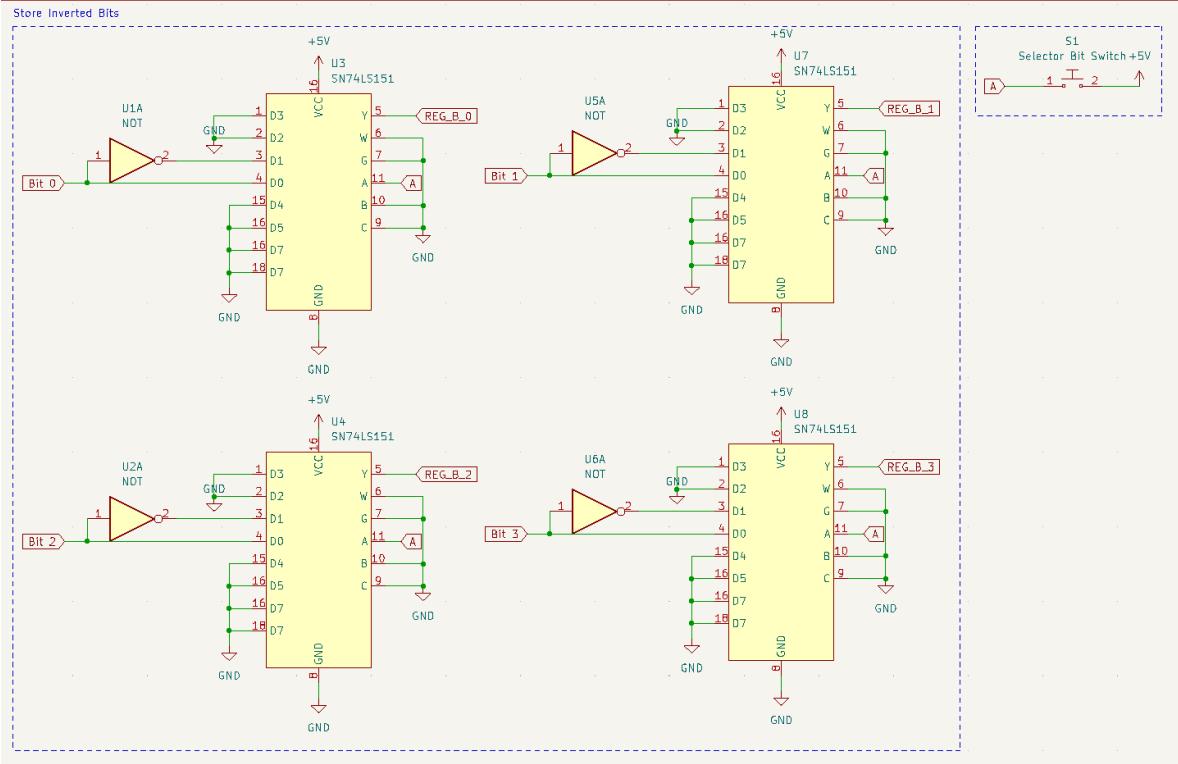


Figure 4: Circuit diagram of the multiplexers that switch between adding and subtracting.

## 5 Circuit pictures: close up

Our 4-bit adder circuit includes a 1-bit adder, input shift registers, output shift registers, a clock, a counter, logic to stop the circuit at a certain time step, and a flip flop to handle the carry and allow multiple bit handling. The subtractor reuses the already-build adder circuit and 2's complement binary to add the 2's complement inverse of a number. For example, calculating  $10 - 5$  would explicitly be  $10 + (-5)$  using this circuit's logic. Converting to 2's complement requires negating all the bits of a number (converting to its 1's complement inverse) and then adding one to it. Our implementation is only able to do the former, and is as consistently off by one while subtracting.

count	Qc	Qb	Qa	clk	ctr clk	so	st	
0	0	0	0	0	0	h	h	{ parallel load }
1	0	0	1	1	0	h	l	add 60
2	0	0	1	0	0	h	l	add b1
2	0	1	0	0	0 → clk or (Qc & Qa)	h	l	add b2
3	0	1	1	0	0	h	l	add b2
3	0	1	1	1	1	h	l	add b3
4	1	0	0	0	0	h	l	add b3
4	1	0	0	1	1	h	l	add b3
5	1	0	1	0	1 when C=1 & A=1	h	l	{ stop! }
5	1	0	1	1	1	h	l	
6	1	1	0	0	/ / / / / /	/ / / / / /		
6	1	1	0	1	/ / / / / /	/ / / / / /		
7	1	1	1	0	/ / / / / /	/ / / / / /		
7	1	1	1	1	/ / / / / /	/ / / / / /		

Figure 5: Truth table for shift register and counter.

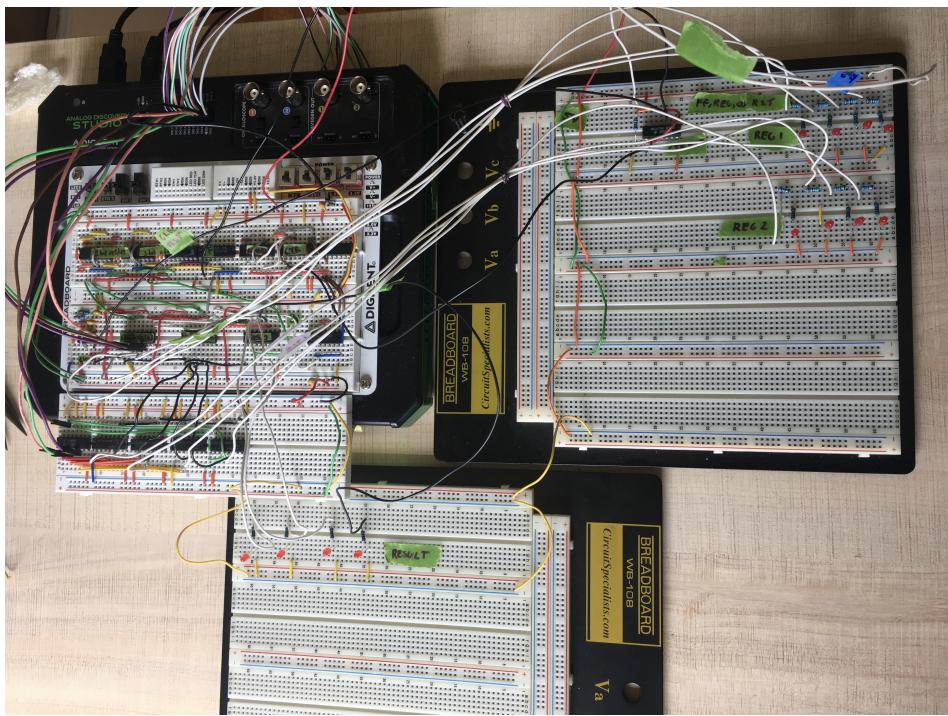


Figure 6: Full circuit diagram.

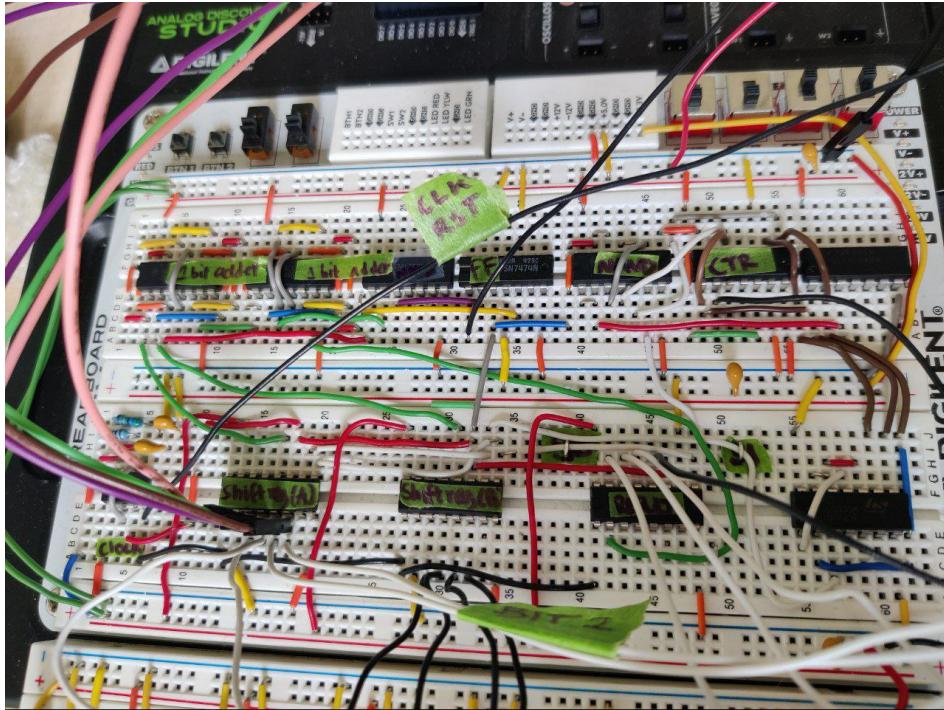


Figure 7: Adder circuit

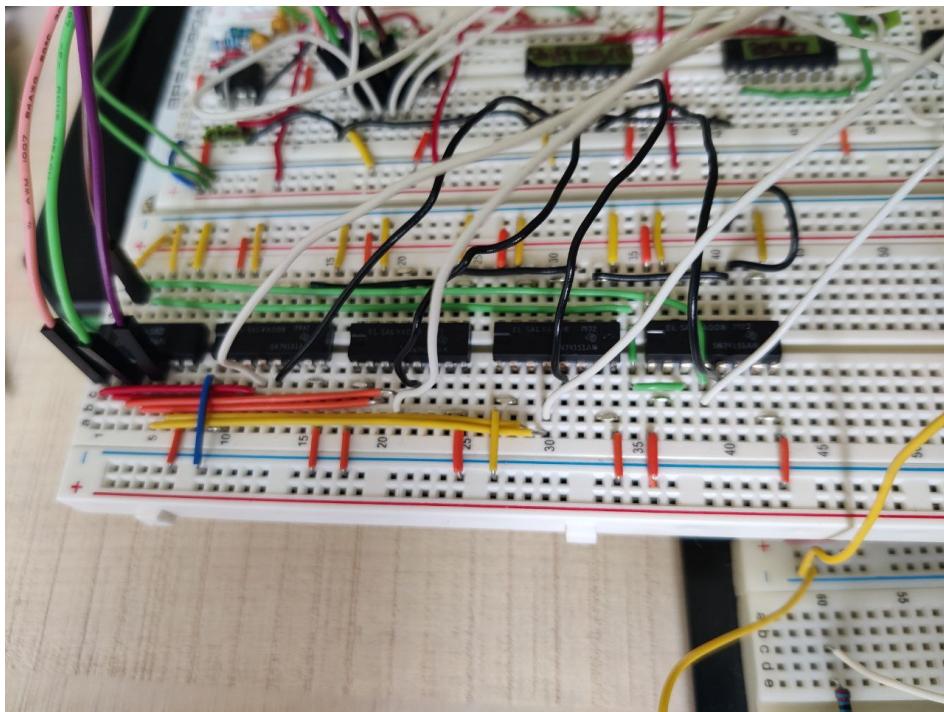


Figure 8: NOT gate chip and multiplexers to accommodate switching between addition and subtraction.

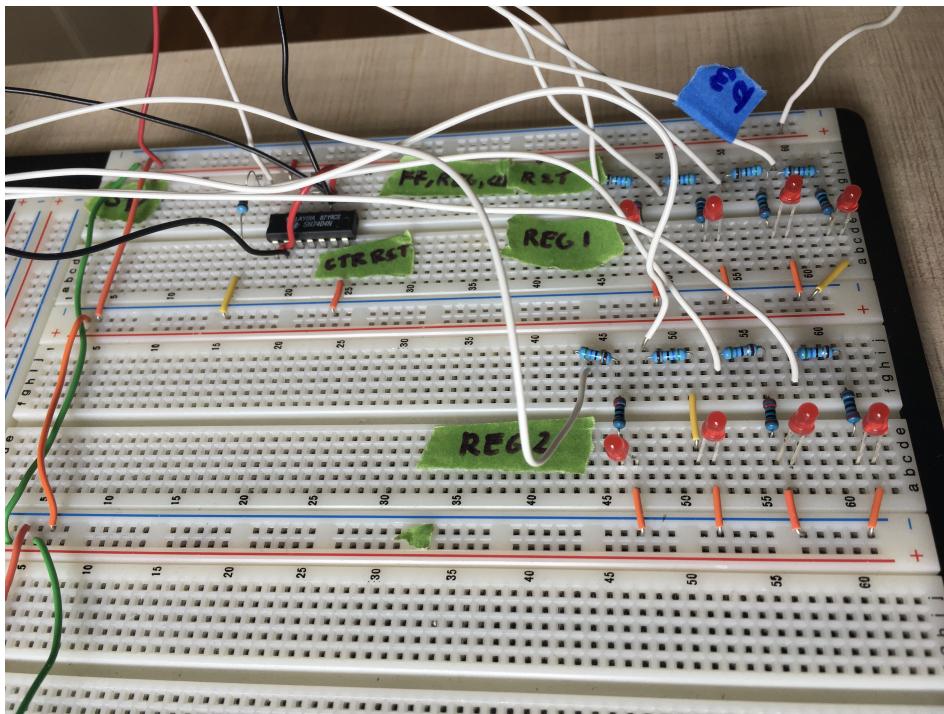


Figure 9: Indicator LEDs and reset switch.

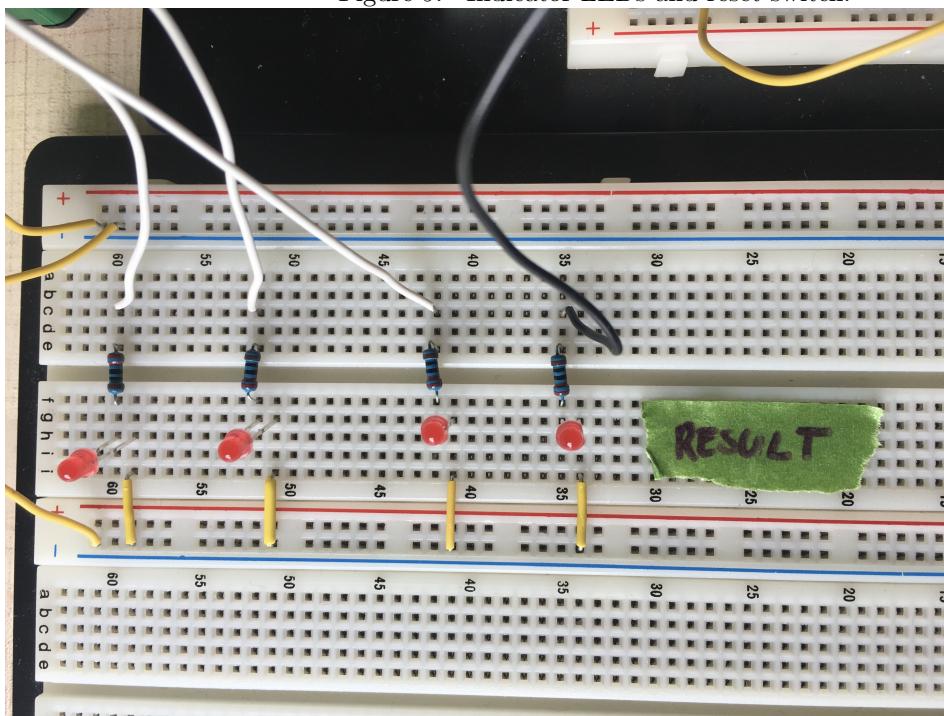


Figure 10: More indicator LEDs.