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CCD TECHNOLOGY

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Abstract. Charge-coupled devices (CCDs) continue to reign supreme in the realm of imaging out to 1 μm, with the steady improvement of performance and the introduction of innovative features. This review is a survey of recent developments in the technology and the current limits on performance. Device packaging for large, tiled focal-plane arrays is also described. Comparisons between CCDs and the emerging CMOS imagers are highlighted in terms of process technology and performance.

Keywords: blooming, charge-coupled device, CMOS, dark current, depletion, electronic shutter, focal-plane array, hybrid sensor, modulation transfer function, noise, orthogonal-transfer array, packages, point spread function, quantum efficiency, radiation tolerance

1. Introduction

In the 36 years since its first demonstration at Bell Laboratories, the charge-coupled device (CCD) has undergone remarkable growth and development. What began as a one-pixel demonstration of charge transfer between three metal gates on an oxidized silicon surface (Amelio et al., 1970) has evolved to devices as large as 66 Mpixels filling a 150-mm silicon wafer (Lesser, 2004). Scientific CCDs are now the largest silicon integrated circuits (ICs), with die areas up to nearly 100 cm^2 compared to $<$4 cm^2 for the largest digital ICs.

In this review we attempt to cover the highlights of current scientific CCD technology. Section 2 is a brief introduction to the structure and functioning of the CCD at the device level and a discussion of wafer processing issues. In Section 3 we survey the performance of current CCD technology in several key areas, including quantum efficiency (QE), noise, charge point spread function (PSF), radiation tolerance, and blooming. In addition, the packaging technology for focal-plane mosaics is reviewed. Section 4 is devoted to a comparison between CCDs and the rapidly evolving CMOS technology, highlighting the differences between them and their comparative strengths and weaknesses. In Section 5 we examine some new concepts under development in CCD technology that are of potentially great interest in astronomy. These include the orthogonal-transfer CCD (OTCCD), electronic shuttering, curved CCDs, and an area of great promise just beginning to be explored, namely, the hybrid combination of CCD and CMOS technologies.

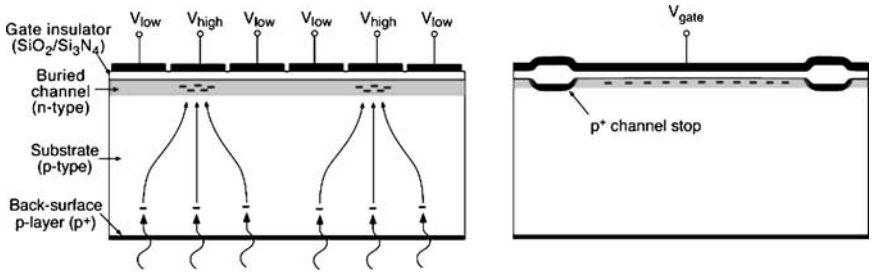


Figure 1. Depiction of the cross section of a three-phase CCD viewed (*left*) across the device gates and (*right*) parallel to the device gates.

2. CCD fundamentals

2.1. Basic CCD structure

Figure 1 depicts the basic elements of an n-channel, back-illuminated CCD; for p-channel CCDs, which have such advantages as greater resistance to space radiation, the labels "n-type" and "p-type" in Figure 1 are interchanged. The starting material is a p-type wafer typically 600–700 μm thick. The n-doped buried channel region at the upper surface is typically no more than 0.1–0.3 μm thick. Photoelectrons are collected and transported to an output circuit within this layer. Its most important function is to ensure that the electrons are kept away from the Si/SiO_2 interface where they could otherwise be trapped by surface states. The wafer surface has a thin layer of SiO_2, and sometimes an additional layer of Si_3N_4, which serves as a gate dielectric, and on top of this layer is a set of electrodes or gates that control the collection and transport of the photoelectrons across the device.

After device fabrication the wafer must be thinned from the back surface to a final thickness typically 10 μm up to 300 μm to enable the CCD to be illuminated from the back. Such so-called back-illuminated devices offer the ultimate in high QE, as will be seen in Section 3, in contrast to conventional CCDs illuminated from the front or circuit side, which suffer from substantial reflection and absorption losses in the gates and dielectric layers. The back surface, however, must be carefully treated to avoid loss of photoelectrons to surface states or traps, and this usually means that a heavily doped p-layer (labeled p^+ in Figure 1) is introduced into the back surface. An antireflection coating on this surface is also required for highest QE.

The process by which an image is formed is as follows. Photons incident on the back surface of the device create electron-hole pairs. Electric fields established by the potentials on the CCD gates draw the photoelectrons into the buried channel. There they are segregated into packets under the gates with the high potential (V_{high} in Figure 1). The neighboring gates at lower potentials (V_{low}) provide electrical isolation between the packets. For a three-phase device, each set of three gates defines

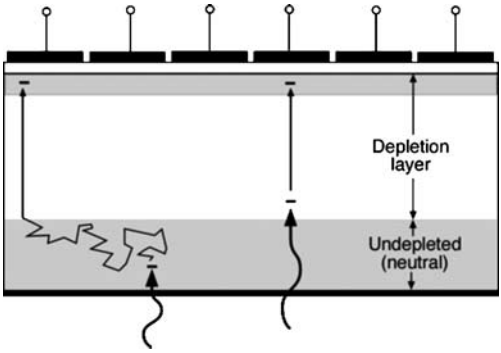


Figure 2. Cross section of a CCD depicting the depletion layer and the neutral undepleted layer at the back surface and its effects on photoelectron charge collection.

a pixel along the direction of charge transport. Charge packets are transported from gate to gate by applying a set of time-varying waveforms to the gates.

In the cross-sectional view of a CCD taken in a direction perpendicular to the charge-transfer direction, shown in Figure 1 (right), the important feature is the channel stops that define the left and right boundaries of a pixel or CCD channel. Typically, these are heavily doped p-type regions, and often the SiO_2 here is thicker than the gate dielectric. The channel stops terminate the edges of the channel. In later sections we will see how modifications of the channel stops are used in two advanced features of CCDs.

An important feature in understanding the image resolution of a CCD is the depletion layer. A depletion layer is depicted in Figure 2 in the upper portion of the p-substrate and the n-buried channel. Here, the fields due to the CCD gates and the buried channel combine to remove the holes to a depth, called the depletion depth, that depends on the gate biases, the doping level and thickness of the buried channel, and the doping level of the p-substrate. In this region the vertical component of the electric field is sufficiently strong to pull photoelectrons fairly quickly (a few ns) into the CCD channel. In the undepleted or neutral portion of the substrate near the back surface, photoelectrons may wander by thermal diffusion over substantial distances before they reach the depletion layer boundary and are swept into the channel. This process clearly degrades imaging resolution, and thus back-illuminated devices must be operated under nearly or fully depleted conditions.

As we will see later in Section 3, it is extremely desirable to make CCDs as thick as possible in order to maximize QE in the near infrared ($\lambda \sim 700$–1000 nm), where photon absorption depth becomes progressively greater and thicker devices are needed to absorb the photons. However, this makes fully depleted operation more difficult.

What are the factors that enable deep depletion depths in a CCD? Raising the gate biases increases the depletion depth, but this approach has its limitations because

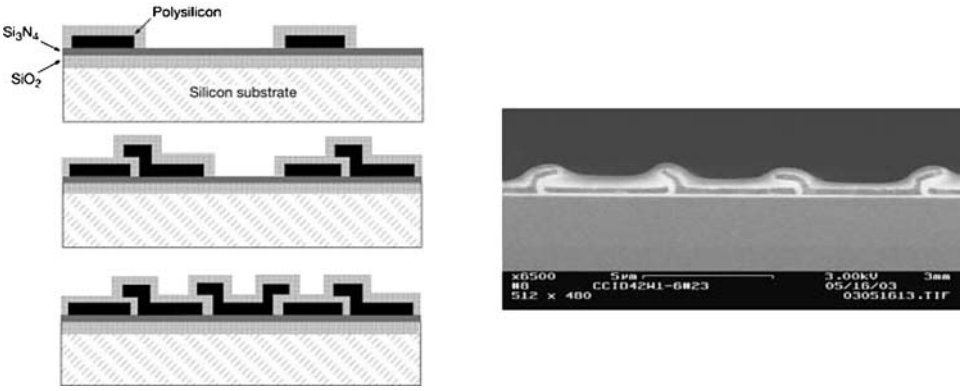


Figure 3. (*left*) Sequence of steps by which CCD gates are fabricated for a three-phase device and (*right*) SEM of a fabricated device.

the higher fields across the device oxide layers lead to spurious charge generation and eventually to catastrophic dielectric breakdown. Another approach is to use lightly doped or high-resistivity substrate material, since depletion depths vary as $N_A^{1/2}$, where N_A is the doping concentration of the substrate (resistivity varies as $1/N_A$). Typical scientific CCDs are made on material having resistivities of the order of 100 Ω·cm or less, resulting in depletion depths of only about 15–20 μm. For better results, some CCDs are made on special material having resistivities of several thousand Ω·cm resulting in depletion depths of 60 μm or more.

The deepest depletion is obtained by combining high-resistivity substrates with a bias applied to the back surface. This approach has been used, for example, by the Lawrence Berkeley National Laboratory group to produce fully depleted p-channel CCDs that are more than 300 μm thick (Holland et al., 2003).

2.2. PROCESSES

The basic process by which scientific CCDs are manufactured is essentially the same as it was 30 years ago. This process for a three-phase device, depicted in Figure 3 together with a scanning electron micrograph (SEM) of a fabricated device, is based on the use of doped polycrystalline silicon, or polysilicon, films for the gate material. Beginning with a substrate wafer, a thin gate dielectric layer(s) is formed on the surface, and a layer of polysilicon is deposited and lithographically defined to produce the first set of gates corresponding to one clocked phase. The wafers are then placed in a thermal oxidation furnace where the thin SiO_2 layer is grown over the polysilicon. For processes that employ a Si_3N_4 layer as part of the gate dielectric this oxidation step leaves the exposed dielectric unchanged, since Si_3N_4 is a barrier to O_2 and H_2O, and prevents the SiO_2 beneath it from becoming thicker. This is an advantage from the point of view of leaving the threshold voltages, and

thus the clock drive voltages, the same for all three phases. For the second and third phases the process is repeated twice, but in each case the gates must overlap slightly the adjacent gates to ensure good control of the electrical potential in the CCD channel below.

2.3. CCD vs CMOS: process comparisons

As CMOS sensors begin to attract more attention, it is worthwhile comparing various aspects of the two technologies. Here, we examine the device processing differences, while later in Section 4 performance is compared.

To understand scientific CCD wafer processing, it is worth noting that for pixel sizes of interest in astronomy ($\sim$10–20 μm) the gate features have dimensions of several μm. In comparison to state-of-the-art silicon IC technology, where feature sizes of $<$0.1 μm are now the norm, these are extremely large geometries. On the other hand, CMOS sensors must have several field-effect transistors and other components placed inside the pixel, along with metal lines, to address, reset, and read out the pixel. This high component density requires the tight sub-μm lithography characteristic of current CMOS wafer fabrication.

The simplicity of the CCD pixel and its readout circuit and its relatively generous design rules enable CCDs to be manufactured with fewer photomasks (typically 10–15) than CMOS (15–30 photomasks) and with less sophisticated (one might say "lagging edge") technology. In addition, scientific CCDs have for the most part kept the relatively thick gate dielectrics (50–100 nm) and polysilicon oxide thicknesses (100–300 nm) from decades ago. By contrast, CMOS processes use gate dielectric thicknesses of the order of 5 nm or less. This, of course, has implications for device yields, since particulates of a size that may produce a fatal short in the gate oxide of a CMOS device may hardly affect a CCD. This fact, combined with the superb cleanliness and extremely low levels of contaminants in the process chemistry of modern wafer fabrication, have enabled high yields for the huge CCD die sizes mentioned in the introduction.

An important distinction between CCD and CMOS fabrication lies in the material requirements. CMOS requires thin epitaxial layers grown on heavily doped (low resistivity) substrates for proper circuit performance, whereas CCDs can be fabricated on almost any substrate, including the highly desirable high-resistivity material needed for deep-depletion depths. Conventional CMOS imagers, therefore, are fundamentally limited to extremely poor near-infrared response. For this reason the only inroads that CMOS can make into the astronomy market will be by hybrid devices, described in Section 5.2.1, in which a separate diode array, made on high-resistivity silicon, is bump bonded to a CMOS readout multiplexer (MUX) (Bai et al., 2000). Whether this can be done in a cost-effective way remains to be seen.

CMOS has always appeared attractive for integrating on chip all of the support functions needed to drive a sensor, such as clock waveform timing and generation, biases, video processing, and analog-to-digital conversion. It is possible, and in

fact has been demonstrated, that a CMOS process can be integrated into a CCD process, but the complications involved are significant and can involve performance compromises and extra costs. A more promising route is to combine CCD and CMOS, either as a bump-bonded hybrid or using newer approaches involving direct wafer bonding (Suntharalingam et al., 2005), to obtain an integrated device with all the support features in one compact sensor. Even a somewhat less integrated approach in which CCD and CMOS reside close to each other in a shared package is attractive in reducing the huge volume and power of the electronics needed to drive the coming generation of Gpixel focal planes. Custom CMOS, unconstrained by CCD process requirements, is now relatively inexpensive compared to large scientific CCDs, so that the case for hybridization is very compelling. Examples of this approach are described in Section 5.

3. Performance areas

3.1. Quantum efficiency

A key performance parameter for an astronomical CCD is QE. CCDs are capable of detecting photons over a wide range, as shown in Figure 4. The figure depicts direct silicon sensitivity, although wavelength-converting materials, e.g., phosphors, are also used. Several factors control silicon sensitivity: (1) High energies (X-rays) have a long absorption length, and sensitivity depends on the thickness of silicon. (2) Short-wavelength ultraviolet photons are absorbed close to the silicon surface and need back side illumination. (3) Photons of wavelength >100 nm are efficiently absorbed in a back side CCD with antireflection coating. (4) Photons of wavelength >400 nm can be detected by a front side illumination; electrodes limit response. (5)

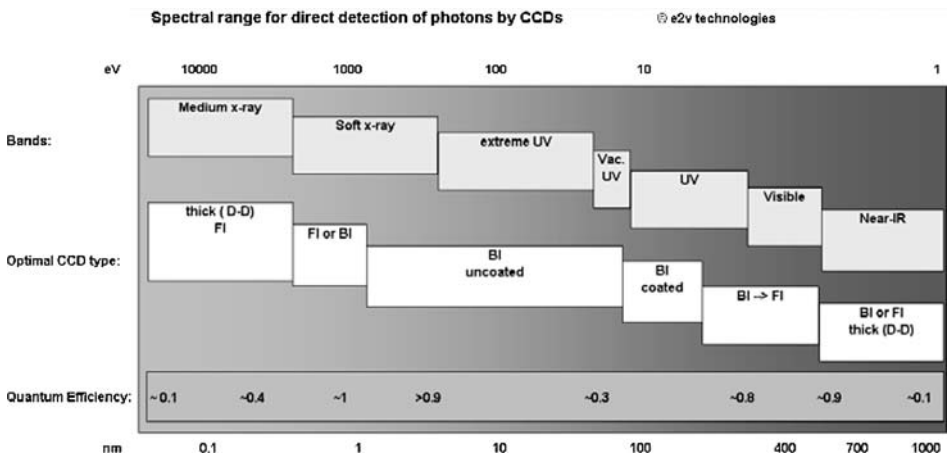


Figure 4. CCD electromagnetic spectral range. Courtesy of e2v technologies.

Photons of wavelength >700 nm have a long absorption length so thicker silicon helps; sensitivity is determined mainly by the thickness of silicon and partly by operating temperature (band gap shifts). (6) Photons of wavelength >1100 nm are not detected because of the silicon band gap limit, which also has a temperature dependence. Most of the following discussion will apply to the range 300–1100 nm, as used for "visible" astronomy.

Charge-coupled devices can be made as front side illuminated devices, but the spectral response is cut off at short wavelengths by absorption in the semitransparent polysilicon electrodes. Peak response is also normally limited to less than 50%. For astronomical use a back-side-illuminated CCD is the default. With careful processing and suitable antireflection coatings, a high spectral response can be obtained over a wide range with a peak approaching 100%. Figure 5 illustrates front-side and back-side illuminated CCD constructions.

A back-side illuminated CCD offers high spectral response, but only if processed carefully. Devices are commonly thinned to a thickness of 10–20 μm, and require back surface treatment to ensure that photons absorbed near the surface are collected. Treatments that have been used include ion implantation followed by laser annealing (http://www.e2v.com), ion implantation followed by furnace annealing, chemisorption charging (Lesser and Iyer, 1998), and molecular-beam-epitaxy/delta doping.

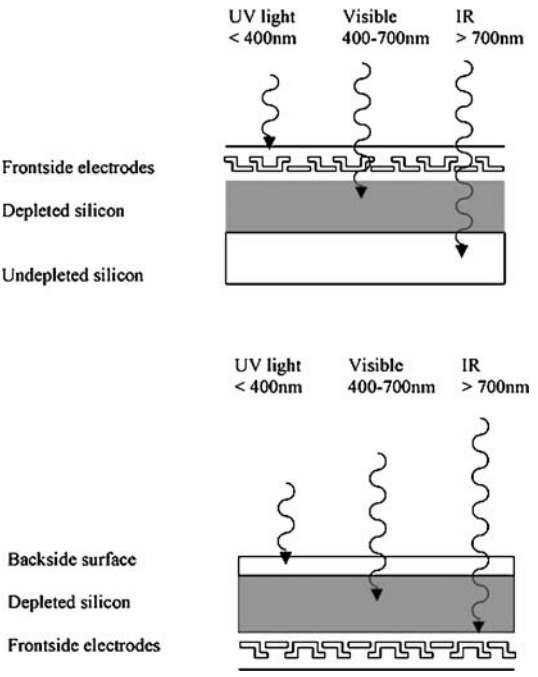


Figure 5. (*top*) Front side and (*bottom*) back side illumination.

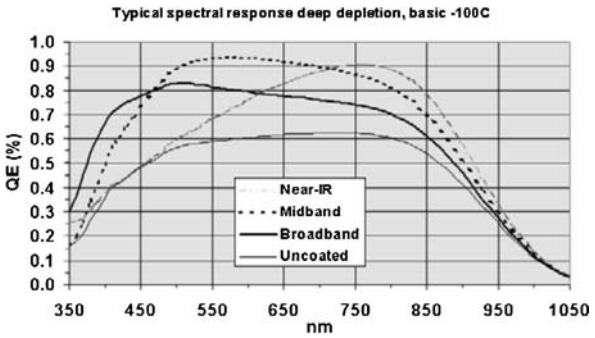


Figure 6. Examples of CCD responses with antireflection coatings optimized for different wavelength regions.

An important requirement for high QE is the use of a suitable antireflection coating because silicon has a high refractive index ($n \sim 4$). The usual material for a single-layer $\lambda/4$ coating is hafnium oxide ($n \sim 2$), which allows near-perfect photon collection especially at midband wavelengths. The curves in Figure 6 illustrate typical spectral responses for different coatings.

For a device of 40 μm thickness, illustrated in Figure 6, a common starting material is 20- or 100-Ω·cm resistivity silicon; after back-thinning and processing the final thickness is typically 10–16 μm. For long-wavelength (red) use, however, the absorption length of these photons exceeds the device thickness (Holland et al., 2003) so not all light is collected. To improve red response some manufacturers offer so-called deep-depletion CCDs; with higher-resistivity silicon, e.g., 1500 Ω·cm, the device may be made with a 40-μm thickness and consequent higher red response.

A possible further step is to make devices even thicker. In this case a so-called "high-rho" device can be made of very high resistivity bulk silicon, e.g., 10,000 Ω·cm. These devices generate larger depletion depths within the silicon and can also be operated with larger voltages to increase it further; a substrate voltage up to 50 V may be used in some cases. Such devices have been championed by the LBNL group (Many LBNL papers available at http://www–ccd.lbl.gov/) and also manufactured by e2v technologies and Lincoln Laboratory (originally for x-ray detection). Such devices can exhibit almost 100% QE at wavelengths around 900 nm, with an eventual reduction as the silicon band gap limit is reached. Figure 7 gives examples of spectral response for different thicknesses of silicon, and measurements (Holland et al., 2003) of LBNL 280-μm-thick samples.

Another performance consideration is fringing. Back-thinned devices of "normal" thickness suffer from internal multipass fringes, which modulate the response at wavelengths longward of 700 nm, where the absorption depth is comparable or longer than the silicon thickness. Devices made of progressively thicker silicon suffer less from this effect (Kelt et al., 2005). The very thick silicon depth causes

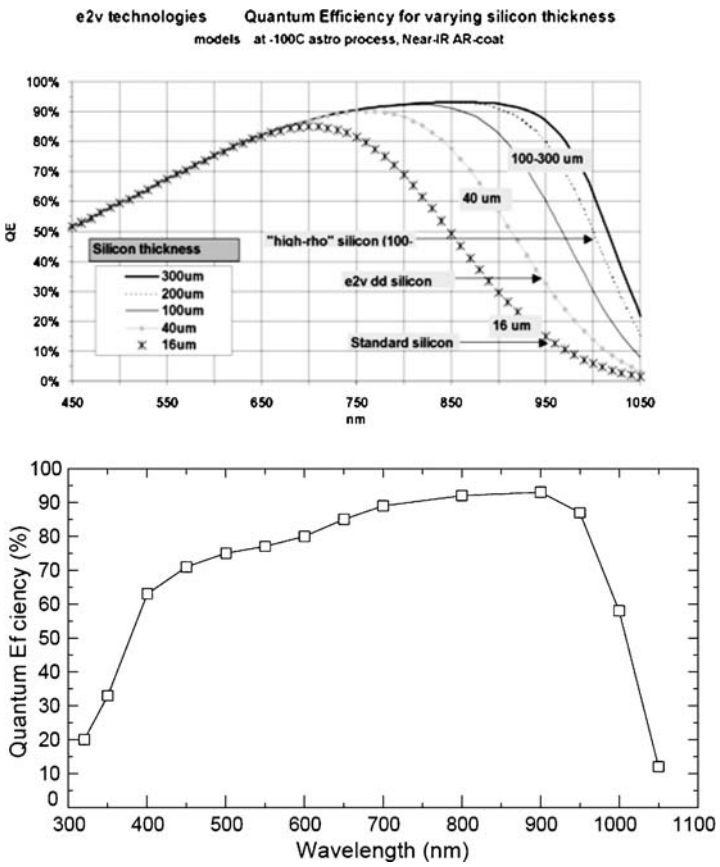


Figure 7. (*top*) Spectral response for different silicon thicknesses; (*bottom*) Lick/LBNL measurements. Courtesy of e2v technologies.

these devices to collect a significantly enhanced number of cosmic ray events. The devices can potentially have a poorer PSF, and so higher operating voltages are normal in order to maximize field strength and achieve good charge confinement.

3.2. Readout noise

Noise is the second parameter that determines the signal-to-noise of recorded data, and a low value of readout noise is often considered essential for low-signal-level astronomical applications. A low noise floor is always important for use at low signal levels, often at low pixel rates. A low noise at higher pixel rates makes the devices useful at higher frame rates, thereby reducing readout time and increasing observing efficiency.

Most scientific sensors utilize a two-stage on-chip output circuit. This allows a small first-stage transistor to couple to a small output node and provides a larger

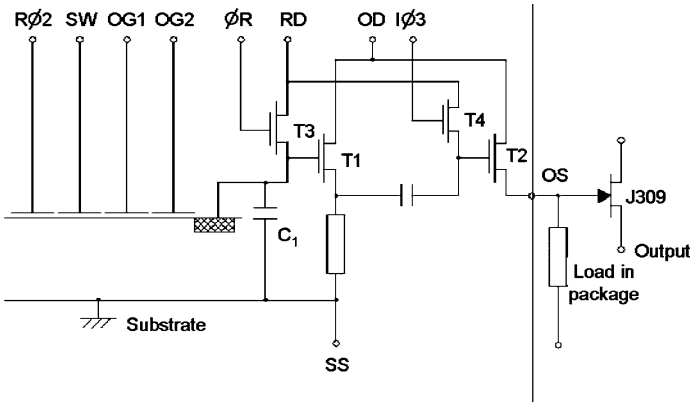


Figure 8. Two-stage CCD output circuit schematic.

second-stage follower to provide reasonable output drive capability. Figure 8 shows an example of a two-stage (e2v technologies) output circuit. Note that an (optional) external junction field-effect transistor buffer is also shown, which is mainly beneficial for driving longer cables with appreciable capacitance.

It is usual to match the designs of the two stages, and one consequence is that very low noise levels need to be traded against the output drive requirements. Large-signal use and high-frequency operation, especially to capacitative loads, require large transistors with a higher noise floor. Figure 9 gives examples for different output amplifier designs.

For scientific use, CCDs are normally expected to have readout noise floors of 2–5 e^- rms, although slightly higher levels are sometimes used. A recent

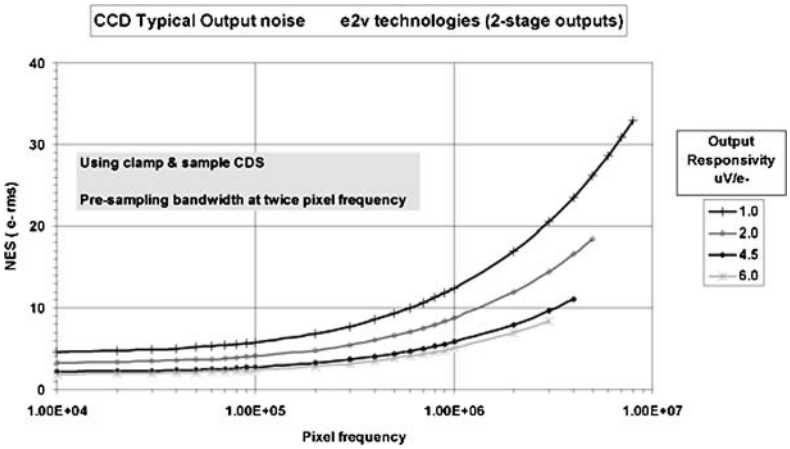


Figure 9. Readout noise vs frequency for different responsivity amplifiers. Courtesy of e2v technologies.

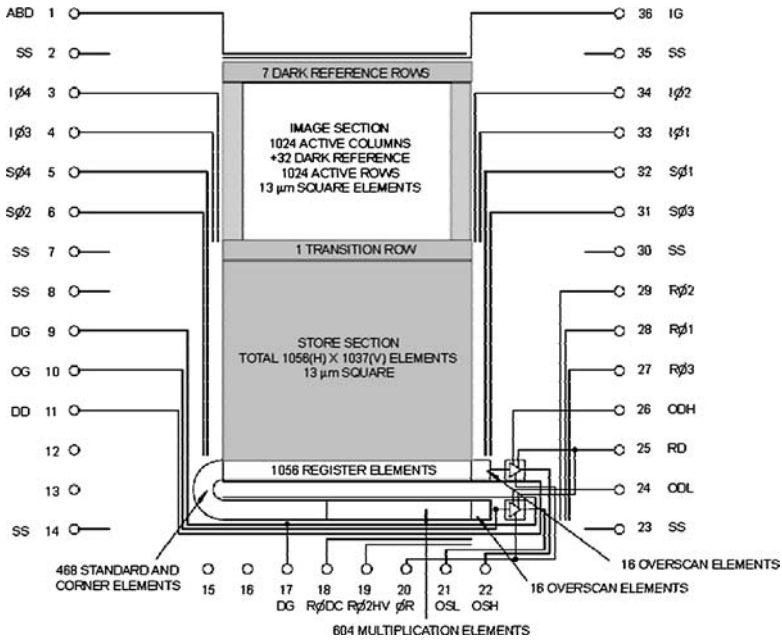


Figure 10. Example of avalanche multiplication structure. Courtesy of e2v technologies.

development of avalanche gain technology (electron multiplication) within CCDs has made subelectron readout noise available. Figure 10 illustrates an example of such a device; applications are discussed in (Tulloch, 2004).

These devices have image areas and an initial serial register that are similar to normal CCDs. However, they utilize an extended serial register with multiple stages (typically ∼500), each of which allows a small probability of electron multiplication when operated with a high-voltage (up to 50 V) clock phase. The result is that the signal at the gain register may be amplified by a factor of 1000 or so before it feeds into the (standard) output stage. Thus, even an output amplifier with a high noise level can give an input-referred readout noise in the subelectron region.

While these devices offer substantially reduced readout noise levels, appreciation of several factors is important for their full use. These include cooling to suppress dark current, control of operating temperature and high-voltage clock level for gain stability, different noise statistics resulting from the stochastic gain process, clock-induced charge at subelectron signal levels, and noise statistics different from the familiar (Gaussian) ones of traditional CCDs.

3.3. DARK CURRENT

Charge-coupled devices collect dark current, which scales strongly with temperature. It has two main components—surface dark current and bulk dark current.

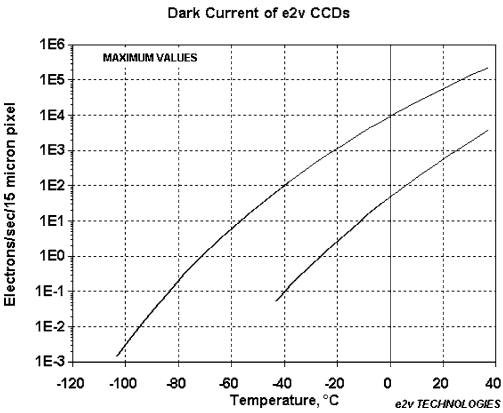


Figure 11. Curves showing (*upper*) surface and (*lower*) bulk dark current. Courtesy of e2v technologies.

The specific magnitude scales with pixel area and can depend on the manufacturing process. Bulk dark current is typically 100 times lower than surface dark current. When multi-phase pinned (MPP) or inverted-mode operation (IMO) is used, devices should achieve bulk dark current levels, as seen in Figure 11.

When the device goes out of inversion, i.e., the clocks are raised above the inversion level, there is a characteristic time before the dark current recovers from bulk to surface levels. This time constant can be appreciable for low temperatures. This means that dark current can be influenced by clocking dynamics. Surface dark current can be reduced by active clocking during integration, i.e., "dither" clocking, and can also be low immediately after a previous readout at low temperatures (Burke and Gajar, 1991; Jorden et al., 2003).

3.4. Modulation transfer function

The primary function of the image sensor is to produce an output that faithfully represents the scene being imaged. The sensor must accurately reproduce all the details in the image, which contains features of varying intensities and spatial frequencies. The resolving power of the sensor is determined by its modulation transfer function (MTF), defined as the response of the sensor to a sinusoidal signal of increasing frequency. The MTF describes the decrease in contrast in the reproduced image as the spatial frequency in the original scene increases. The reduction in modulation (contrast) of closely spaced line pairs results in image blur since the separation between the light and dark lines can no longer be observed. Different methods are used to measure MTF (Dutton et al., 2002). One is to directly measure the sensor response to a sinusoidal input source. Another is to perform the Fourier transform of the PSF, which yields the optical transfer function (OTF). The MTF is the magnitude of the real part of the complex OTF variable.

Modulation transfer function is defined as the ratio of modulation depth of the output signal to the input signal:

$$\text{MTF} = \frac{\text{Modulation (Output)}}{\text{Modulation (Input)}}, \quad \text{where}$$

$$\text{Modulation} = \frac{\text{Signal}_{\text{MAX}} - \text{Signal}_{\text{MIN}}}{\text{Signal}_{\text{MAX}} + \text{Signal}_{\text{MIN}}}.$$

The overall MTF of the instrument is the product of the MTF of each optical component of the system, including the lens, the sensor, the electronics, and the display; however, the MTF of the sensor is usually the limiting factor.

Since the sensor is essentially a spatial sampling device, the highest frequency that it can accurately reproduce is defined by the Nyquist frequency, $f_{\text{Nyquist}} = 1/2p$ where p is the pixel pitch. The finite sampling nature of the sensor is characterized by the sampling MTF, which is directly influenced by the pixel geometry. The MTF of the CCD is further limited by the charge-transfer inefficiency and carrier diffusion.

The overall MTF of a CCD is the product of three components: pixel geometry, charge-transfer inefficiency, and carrier lateral diffusion:

$$\text{MTF}_{\text{CCD}} = \text{MTF}_{\text{s}} \times \text{MTF}_{\text{t}} \times \text{MTF}_{\text{d}}.$$

The discrete spacing of the pixels in the CCD places a fundamental limitation on its performance. The CCD samples the image in spatially discrete steps, and the spatial MTF is given by

$$\text{MTF}_{\text{s}} = \sin(\pi f_{\text{s}} p)/(\pi f_{\text{s}} p) = \text{sinc}(f_{\text{s}} p),$$

where f_{s} is the spatial frequency and p is the pixel pitch. At the Nyquist frequency, MTF_{S} is limited to 0.637.

Imperfect charge-transfer efficiency (CTE) results in a reduction in the output signal, causing a loss in the response amplitude, and

$$\text{MTF}_{\text{t}} = \exp\{-n\varepsilon(1 - \cos 2\pi f/f_{\text{c}})\},$$

where f is the spatial frequency of the signal transferred through the device at f_{c} clock frequency, ε is the charge-transfer inefficiency per transfer, and n is the number of transfers in the CCD. Even with a large number of transfers, the MTF_{t} is usually a minor component in CCDs with high CTE.

Charge carriers that are generated inside the depleted region of the channel are driven by its electric field to the potential wells of the pixels directly above the location where they originated, but those charge carriers that are generated outside

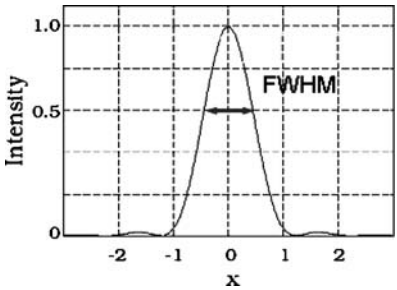


Figure 12. Diameter of PSF where signal intensity at the center of the image is reduced by half.

of the depleted region, in the field-free region, will diffuse randomly in the substrate and carry a high probability of being collected in the neighboring pixels instead. This effect represents the largest component of MTF degradation in the sensor. Since the photon absorption depth increases with wavelength, MTF_d is worse at longer wavelengths in a front-illuminated sensor, but in a back-illuminated sensor, the spatial resolution degradation occurs at the short wavelengths.

3.5. Point spread function

In a well-behaved optical system, a point source of light at the object plane will generate a corresponding spot image in the image plane. The shape of the image formed at the sensor by the point source, the PSF, ideally will have a circular shape and cover only a small region. The size of the PSF is due to spreading of charge carriers, by random diffusion in the field-free region below the pixels. The width of the PSF limits the spatial resolution of the sensor, and a common practice is to report the value at full width at half-maximum (FWHM), which is the diameter of the PSF where the signal intensity at the center of the image is reduced by half, as seen in Figure 12.

Charge diffusion in the field-free region results in enlargement of the PSF, as shown in Figure 13. To narrow the PSF the undesirable effects of charge diffusion must be controlled, either by reducing the size of the field-free region or by widening the depletion depth. The field-free region can be minimized by reducing the thickness of the substrate, but this is an undesirable option since the QE at long wavelengths would suffer. A better approach is to fabricate the devices on high-resistivity material, which helps extend the depth of the depletion region.

3.6. Deep depletion and fully depleted CCDs

To improve the QE response in the red and near infrared, deep-depletion CCDs are fabricated on high-resistivity silicon material, which helps to extend the depth of the depletion layer so that long-wavelength photons are effectively absorbed.

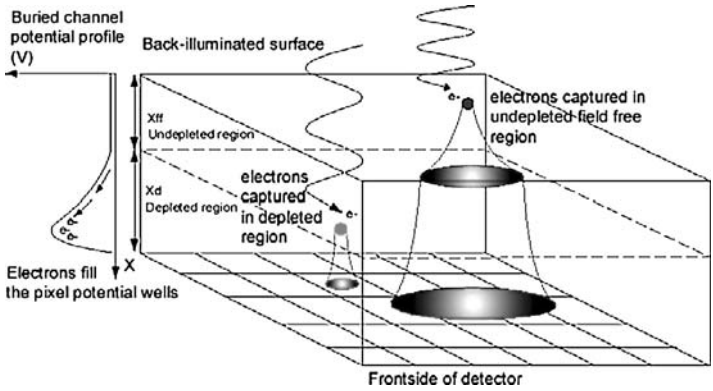


Figure 13. Enlargement of PSF resulting from charge diffusion in the field-free region.

Commercially available devices are produced on 50-μm-thick, high-resistivity material, achieving a depletion depth of about 30 μm under normal operating voltages. Both front-illuminated and back-illuminated devices are offered.

Fully depleted CCDs are fabricated on 200–300-μm-thick silicon material of very high resistivity (10–12 kΩ·cm). An independent bias is applied to the substrate to fully deplete the devices. The devices are back illuminated and yield exceptional QE in the near infrared, thanks to the thick substrate (Holland et al., 2003). With the proper antireflection coating the QE at 1000 nm is about 60%, compared to a maximum of about 16% with a deep-depletion CCD.

The application of the substrate bias purges the mobile majority carriers from the substrate and generates an electric field that extends from the channel to the back side of the device. The electric field pushes the photogenerated carriers to the proper potential wells, inhibiting the lateral charge diffusion that lowers the MTF. The PSF of a 300-μm-thick fully depleted CCD at 400 nm measures 8–10 μm with 40-V substrate bias, and 6 μm when the substrate bias is increased to 77 V (Groom et al., 2000).

3.7. Radiation tolerance

A CCD is normally capable of transferring charge with practically no loss after a very large number of transfers. This requires that the signal paths in the CCD be completely free of charge traps or other defects. When the devices operate in space, continued exposure to energetic particle radiation leads to degraded device performance. The main defect mechanisms are displacement damage and total ionizing dose effects (Pickel et al., 2003). In space applications, displacement damage effects have a stronger impact on CCD performance.

Radiation damage adds new energy levels in the band gap, facilitating the transition of electrons to the conduction band as seen in Figure 14, and increases dark

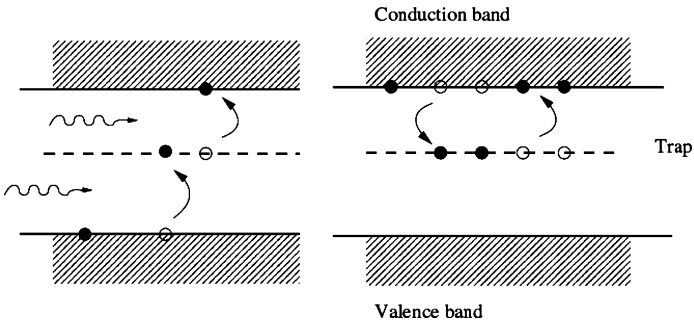


Figure 14. Illustration of effects of radiation damage, which facilitates transition of electrons to the conduction band.

current. These defects can also trap charge and release them after some time constant, degrading the CTE. High-energy protons, neutrons, and electrons produce displacement damage when they collide with the silicon atoms, resulting in atomic defects, such as dislocations, in the crystal lattice, which cause an increase in dark current, generate hot pixels, and lower CTE because of the additional charge-trapping sites.

Ionizing radiation damage results in the buildup of excess positive charge in the gate dielectric, which offsets the flatband voltage, effectively changing the effect of the applied bias and clock voltages. The generation of traps at the SiO_2 interface also results in an increase of dark current and a degradation of CTE.

A number of techniques have been developed to mitigate the effects of radiation damage, shown in Figure 15, and accurate models have been developed to help predict the performance of CCDs following irradiation. Operating the CCD in inverted mode, so that the CCD surface is accumulated with holes, suppresses dark current and improves CTE, since the surface traps are filled and can no longer interact with the signal charge. This technique effectively improves the device resistance to total ionizing dose. The operating temperature and the clock frequencies can also influence the impact of radiation damage, since they affect the time constant of the charge traps and reduce their capture duty cycle. Adding a narrow notch in the CCD channel helps reduce the interaction between the signal charge packets and the trapping sites in the silicon. Introducing a sacrificial "fat zero" charge to all of the pixels in the CCD is another technique used to fill the traps and make them inactive, but this method increases the noise level.

Tests have shown that p-channel CCDs are more radiation tolerant than conventional n-channel devices. Proton irradiation tests performed on n-channel CCDs reveal the presence of traps with energy levels at 0.14, 0.23 and 0.41 eV below the conduction band. The 0.14-eV traps are due to A-centers (oxygen-vacancy complex), the 0.23-eV traps are caused by divacancies, and the 0.41-eV traps are believed to be caused by phosphorus vacancy (P-V) defects. Studies indicate that the P-V defects are responsible for the majority of the traps that degrade CTE

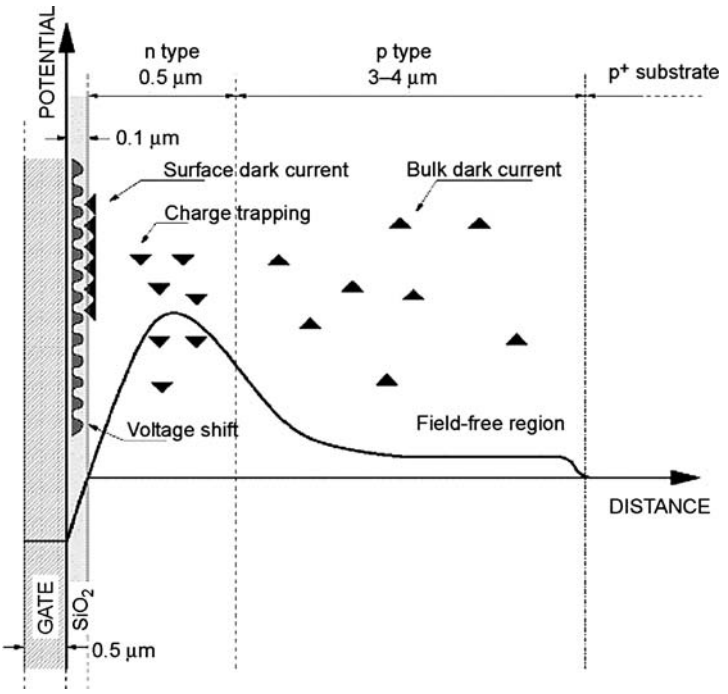


Figure 15. Effects and defect locations from radiation damage due to ionizing and displacement damage. Courtesy of Niels Bassler, University of Aarhus.

performance in n-channel devices since their energy level is near the mid-gap level. These traps become much less effective when the device is cooled down below 180 K. The divacancies are considered to be the main defects that cause increase in bulk dark current. P-channel CCDs are not susceptible to the P-V defects and have demonstrated much greater radiation tolerance than conventional n-channel devices.

3.8. Packaging and Mosaics

Making CCDs is often easy compared to providing suitable packaging for specialized applications like astronomy. For commercial applications a simple ceramic (DIL) package can suffice and provides a cost-effective solution. For applications requiring good device flatness, metal packages are common with various connection schemes available. Large focal planes with high fill factors require the most compact buttable packages, in which a minimum footprint connector is also required. Six typical packages are shown in Figure 16.

Two large multichip applications are shown in Figure 17.

Many applications, especially single chip, employ simpler packages. Development costs often preclude the use in ground-based astronomy of custom packages such as those utilized in space applications. For large focal planes or "ex-

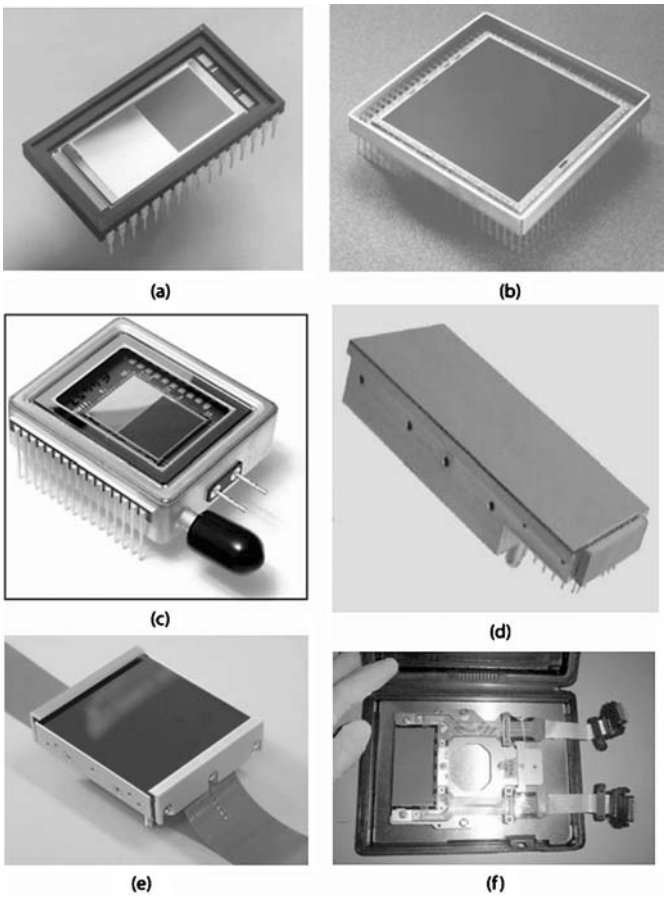


Figure 16. *(a)* Ceramic package (ccd47-20), *(b)* Kovar package (SITe), *(c)* sealed Peltier package, *(d)* three-side buttable metal package, *(e)* four-side buttable + flexprints, *(f)* custom space package. *(a)*, *(c)*, *(d)*, *(e)*, *(f)* Courtesy of e2v technologies.

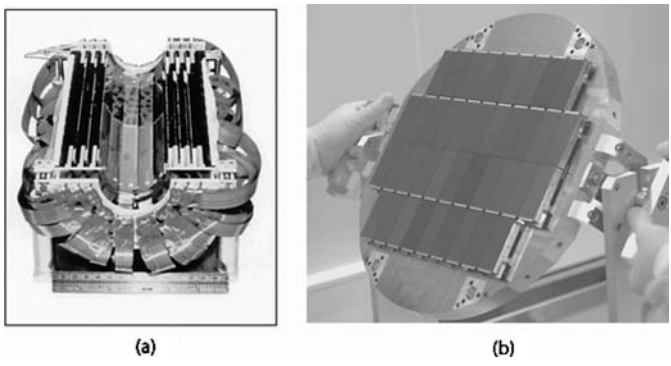


Figure 17. (*a*) Vertex vxd3 detector and (*b*) CFHT Megacam (377 megapix).

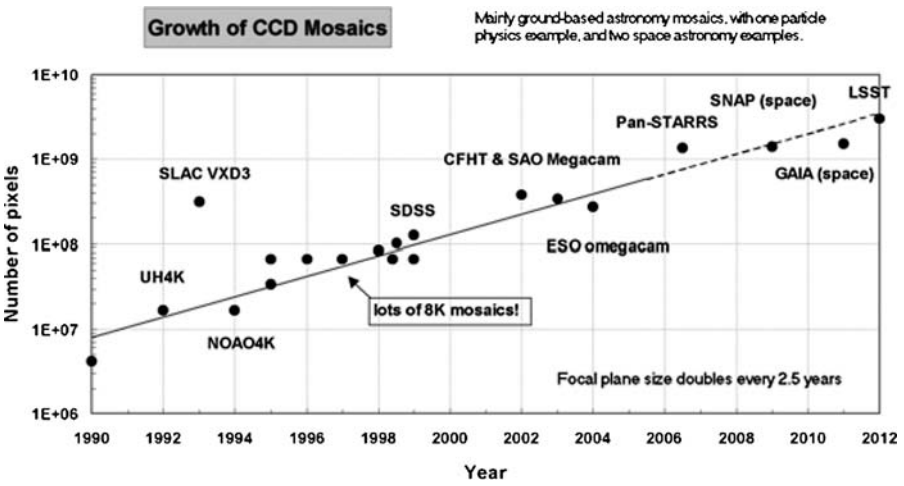


Figure 18. Illustration of large focal-plane sizes with Luppino/Burke "Moore's" law.

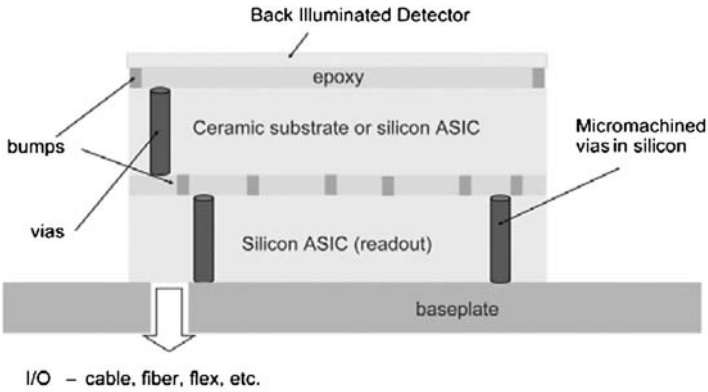
tremely large" telescopes, however, more sophisticated packages become viable. Currently, several observatories have been constructing "megacam" arrays (Jorden et al., 2004), and larger ones are planned such as for the Large-Synoptic Survey Telescope (LSST) Observatory. The routine manufacture of large-area sensors in quantity has made large mosaics feasible for astronomy, which has seen a considerable growth of these within the last decade or so, as illustrated in Figure 18.

Along with the growth of mosaics using "standard" CCD packages, custom packages driven by the requirements of large mosaics have also been developed, as seen in Figure 19.

3.9. Blooming control

Because of the enormous range of object photon flux encountered in astronomy, the problem of pixel saturation, or blooming, inevitably arises in direct sky imaging. In a typical scientific CCD the well saturation causes charge to overflow into adjacent pixels above and below the illuminated pixels and to a much lesser extent across the channel stops into adjacent columns, as illustrated in Figure 20 (left). The reason for this is that the channel stops are at the substrate or ground potential while the CCD channel, even with its gates at the most negative potential, is always a volt or so positive. Thus, there is always a path for electrons into adjacent pixels within a column that is energetically more favorable than across the channel stops. However, when the illumination is so intense that photoelectron current cannot completely drain along this path, the excess electrons will diffuse into the substrate below and be collected by pixels in adjacent columns.

A method of blooming suppression involving dithering of the clock waveforms, called clocked antiblooming (CAB), was described in 1983 (Hynecek, 1983) and



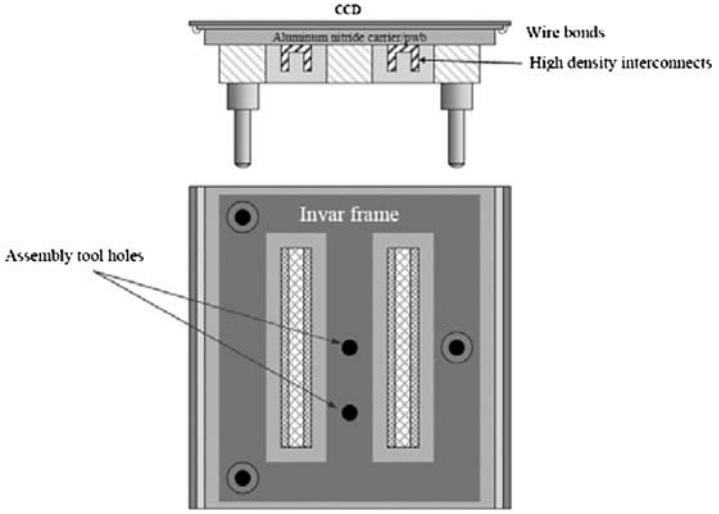


Figure 19. Examples of custom packages: (*top*) Luppino concept package; (*middle*) Lesser application-specific integrated circuit concept for LSST (Lesser and Tyson, 2002); (*bottom*) LSST concept package.

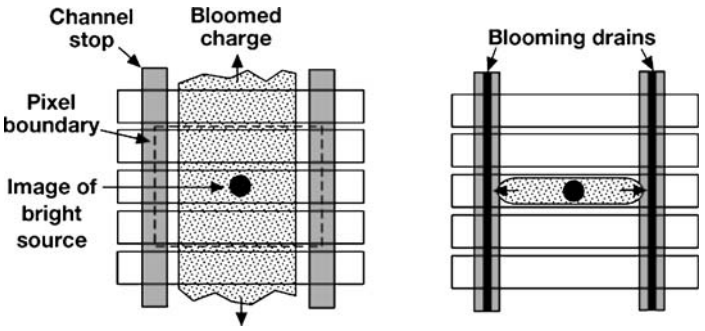


Figure 20. (left) Blooming in a three-phase CCD showing charge overflowing into adjacent pixels within the column, and *(right)* pixel with blooming drains embedded within the channel stops to absorb pixel overload.

can be applied to any buried-channel CCD, except for those that have a built-in charge-transfer directionality, i.e., two-phase CCDs. The technique relies on a phenomenon called charge pumping, in which excess photoelectrons are made to recombine with holes via surface states before the blooming occurs. Charge packets must be transferred back and forth within the pixel, and each transfer results in the recombination, and therefore removal from the charge packet, of electrons equal in number to the surface states at the silicon/oxide interface.

To keep up with the buildup of excess charge, the integrated charge packet must be shifted repeatedly during image integration. The question that the required cycle rate raises is one of the limitations of this method, namely, that it depends on the surface state density of the device technology. Typical values of contemporary technology lie in the low 10^9 cm^{-2}, hence of order 5000 states in a $15 \times 15 - \mu$m pixel. Thus, each forward/backward shift eliminates a quantity of charge that is relatively small compared to a pixel full well. At a 20-kHz back-and-forth shift rate this method can sink about 10 pA of bloomed charge per pixel. Of course, higher surface state densities would clearly be more attractive for this process, but manufacturers take great pains to reduce these states because they are a prime contributor to dark current.

A more attractive approach for the user is the kind of built-in blooming control first developed at what used to be RCA Laboratories (now Sarnoff Corporation) in the 1970s (Sauer et al., 1990). This feature is available from almost all the manufacturers of scientific CCDs, including e2v technologies, Fairchild Imaging, and Semiconductor Technology Associates. Figures 21(a) and 21(b) illustrate the pixel modifications used in this method. The standard p^+ channel stop is modified by placing an n^+ overflow or blooming drain flanked on both sides by n^- regions, whose doping level is carefully controlled to produce a potential barrier or charge "spillway" that allows charge to flow from the well into the blooming drain at some predetermined level. A p^+ photoelectron barrier is placed beneath these regions to

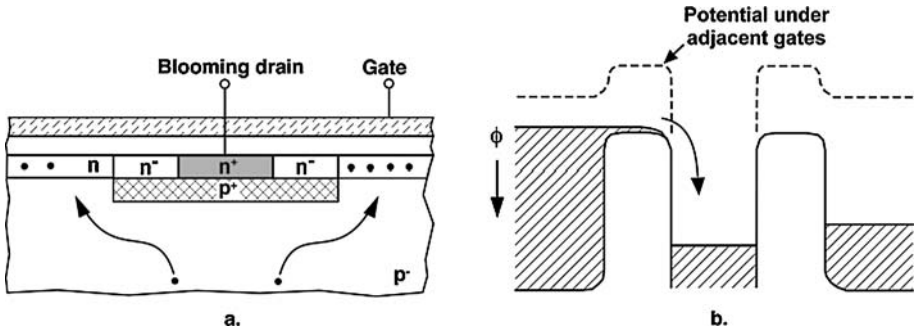


Figure 21. (a) Cross-sectional view of a channel stop modified for blooming control and *(b)* depiction of the potential profiles in the blooming-control structure.

deflect into the wells those photoelectrons that would otherwise be captured by the blooming drain. Figure 21(b) depicts electron potentials and charge flow when the blooming control is active. Clearly, the operation of this feature depends on the low level of the clock phases adjacent to the integrating phase in order to establish a blocking potential.

The pixel modifications are not difficult from a process point of view, nor are they regarded as having a significant impact on device yield. The blooming control depicted here does occupy greater width than a standard channel stop and therefore results in some penalty to the full well. While standard channel stops have widths 1.5–3 μm (after lateral diffusion of the p-dopants and the bird's beak encroachment), the blooming control as fabricated at Lincoln Laboratory (Burke et al., 1998) occupies about 4 μm. Data at Lincoln Laboratory on a 2k $\times$ 4k, 15-μm-pixel device has shown that the blooming control can handle currents of at least 1 nA from a pixel before blooming sets in, or about 100$\times$ higher than charge pumping.

4. CCD, CMOS, what's it all about. . .?

4.1. CCD AND CMOS TRADEOFFS

We've all heard about the imminent doom of the CCD technology, but it continues to thrive, and in many cases it is still the best approach when image quality is the most important criterion. The CCD is a straightforward device. The imaging section consists of an array of capacitors with overlying gate electrodes biased to create regions of high electrical potential in the pixels where charge carriers can be collected. Once the photogenerated charge has been accumulated in the potential wells, the signal is physically moved from one pixel to the next by alternating the bias voltage levels to shift the charge packets across the array. The pixels perform both the function of charge capture and of charge readout. To produce an image,

the signal in the imaging region is shifted to the serial shift register—a single row of pixels dedicated to transfer the charge to the output amplifiers—a line at a time. Then the data are transferred, pixel by pixel, to a precharged output sense node that is connected to the output amplifier to convert the charge to a voltage signal.

The relatively simple structure of the CCD facilitates the fabrication of very large area sensors with very uniform pixel response. The CCD is capable of delivering exceptionally clean signals since the charge-transfer process is noise-free, and the design of the output amplifier can be optimized for low noise performance with little restriction in silicon real estate. On the other hand, CCD fabrication requires specific materials and processes that are not supported by high-volume silicon foundries geared for CMOS logic and memory devices. For example, the CCD multilayer overlapping polysilicon gate electrode arrangement is a unique requirement that involves special processes to avoid catastrophic electrical shorts.

The strengths of CMOS imagers include low power, high speed, and inclusion of more functionality on chip (Fossum, 1997). With increasing demands on their imaging performance, however, the fabrication of high-quality CMOS sensors can no longer share the same recipes originally intended for standard digital products. CMOS image sensors require processes tailored for analog and mixed-signal circuits that are more or less similar to the CCD fabrication process.

4.2. CCD vs CMOS: IMAGING PERFORMANCE COMPARISONS

Next, we compare CCD and CMOS sensors in terms of the following features: charge generation, charge collection, signal readout, signal measurement, and optical characteristics.

4.2.1. *Charge generation*

Charge-coupled device and CMOS sensors detect light by the photoelectric effect. Incident photons with energy greater than the band gap of silicon ($E_g = 1.12$ eV at 300 K) create electron-hole pairs as they penetrate the material. The absorption depth in silicon is proportional to $1/\alpha$. The absorption coefficient α is lower at longer wavelengths, so a larger volume of material is required to capture these photons. At 400 nm more than 80% of the photons will be absorbed within 0.2 μm of the silicon surface, while at 700 nm 10 μm of material is needed to absorb the same amount. CCDs are typically fabricated on 20-μm-thick epitaxial silicon, which is a custom thickness in a CMOS process. The higher doping concentration in the CMOS material, necessary to reduce short-channel effects, lowers the minority carrier diffusion length and reduces QE.

4.2.2. *Charge collection*

In an ordinary slab of silicon, the mobile carrier concentration stays in equilibrium. As a result the photogenerated carriers recombine at the same rate that they are created, and no measurable signal can be produced unless the photogenerated

electron-hole pairs can be separated and the resulting charge carriers collected in the potential wells. In CCD and CMOS sensors light detection is performed with a photodiode or a photogate. The electric field in the depletion region of the structures separates the electron-hole pairs and causes the charge carriers to drift to the potential wells, or regions with the highest electrostatic potential, where they accumulate. In a photogate CCD the fill factor of the pixel can be as high as 100%, but a CMOS pixel (photodiode or photogate) must include three or more opaque transistors, which reduces their sensitivity, and full-well capacity. The low-voltage operation of CMOS circuits combined with the low-resistivity epitaxial silicon results in shallow depletion depths, $\sim$0.5 μm, which degrades QE. The effective collection volume in a CMOS sensor is small compared to the CCD, where the depletion depth is typically $\sim$5 μm.

4.2.3. *Signal readout*

Here lies the fundamental difference between CCD and CMOS imagers. In a CCD the signal charge in the pixel must be transferred across the entire array before it is converted to a voltage by one or a few amplifiers. CCDs are designed to transfer charge with practically no loss, routinely achieving 99.9999% CTE in scientific grade devices. The limited number of amplifiers yields very high output uniformity. To achieve high data rates, however, high-bandwidth amplifiers are required, and the amplifier noise may become a limiting factor. In a CMOS sensor the signal is converted to an output voltage in the pixel and is then read out directly by row and column selection. This architecture significantly reduces the amplifier bandwidth requirements, but the variations in threshold voltage and gain cause undesirable fixed-pattern noise, photoresponse nonuniformity, and temporal noise. Photogate and pinned photodiode CMOS sensors mimic CCD operation since the photocharge must be transferred to an output sense node to be converted to a voltage. In fact, the pixel design is identical to the final stage of a CCD register. Charge transfer is a difficult task to perform at low voltages, because of the weak fringing fields, and requires careful optimization of the doping profiles.

4.2.4. *Signal measurement*

This is the final step where the photocharge in the pixel is converted to a voltage. In a CCD, when the signal charge is transferred to the sense node, its preset voltage level is reduced, and the voltage change is detected by the source-follower output amplifier, yielding an output voltage that is linearly proportional to the signal level. The noise source due to the uncertainty in the reset level of the sense node, due to the kTC noise of the reset FET, can be removed by performing correlated double sampling (CDS). The technique involves reporting the output signal as the difference between the video signal and the immediately preceding reset signal, so the reset noise is canceled out. In a CMOS sensor CDS requires additional sample-and-hold capacitors and extra switches in the pixel, impacting the fill factor, but without these components CMOS sensors will be limited by the kTC noise. To improve the fill

TABLE I
Summary comparison of CCD and CMOS technologies

CCD Technology	CMOS Technology
Highly optimized for optical detection, special fabrication requirements	Benefits from advances in manufacture of high-volume digital products
Very high signal-to-noise	Noise typically higher
Low photoresponse nonuniformity (PRNU), low fixed-pattern noise (FPN)	High PRNU, high FPN, improved by gain and offset correction
Low dark current	Dark current typically higher
High power dissipation	Low power consumption
Complex driver electronics, no on-chip logic and digitization	Single power supply operation, digital output
Serial readout, no windowing capability	Random addressing capability

factor, tighter design rules can be implemented, but the junction depths and voltage swings are also scaled down, lowering the dynamic range of the sensor.

4.2.5. *Optical characteristics*
Differences between the architectures of CCD and CMOS sensors affect their optical performance. The entire area of a CCD pixel can be designed to be photosensitive, compared to a CMOS active pixel sensor, where every pixel must contain at least three transistors that are optically insensitive. The fill factor is the ratio of the sensitive area to the total pixel area, and the effective QE is reduced by the fill factor $QE_{eff} = FF \times QE$. In addition, the multilayer metallization process used in CMOS design results in the active area of the pixel being located inside of a deeply recessed opening in the metal layers, causing undesirable optical artifacts in fast optical systems such as light scattering and crosstalk.

4.2.6. *CCD vs CMOS summary*
As summarized in Table I, CCD technology and CMOS technology each has its strengths and drawbacks. While the CCD can approach near ideal imaging performance, CMOS can offer higher circuit integration, lower power, and higher-speed operation.

5. Special features and new device concepts

5.1. Electronic shuttering

Mechanical shutters are a perennial problem for astronomers, all the more so in this era of ever larger focal-plane arrays (FPAs). Thus, an electronic solution to this problem would seem to be enormously attractive. Interline-transfer devices

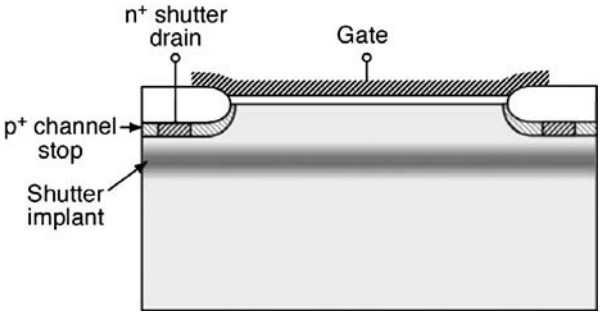


Figure 22. Cross-sectional view of a CCD with the principal features needed for the electronic shutter.

have an effective shuttering capability but only for front-illuminated formats where the charge can be shifted into the readout registers that have been covered with a thin-film light shield.

An electronic shuttering feature for back-illuminated CCDs has been demonstrated by Reich et al. (1993) on imagers developed for adaptive-optics applications. The modifications to the device needed to implement the shutter are depicted in Figure 22.

Two new features have been added to the pixel. The first is a deep p-type implant, called the shutter implant, which lies about 1.5 μm below the surface. This layer creates a potential barrier to photoelectron flow from the back surface, which can be modulated by the gate voltage. The second feature is an n^+ region within the channel stop whose function is to collect photoelectrons when the shutter is closed. The shutter operation is illustrated in Figure 23.

To open the shutter the imaging-array gates must be set to a relatively high potential, typically 18 V. The E-field set by the gate overcomes the potential barrier established by the shutter implant, and the depletion region is pushed all the way to the back surface. At the same time the shutter drain is biased to a relatively low potential. Under these circumstances all the photoelectrons are collected in the

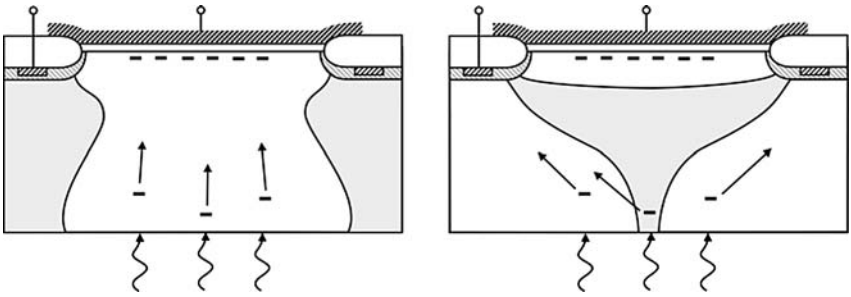


Figure 23. Operation of the shutter: *(left)* gate voltage is high and the shutter drain low, allowing photoelectrons to be collected; *(right)* gate voltage is at a lower setting for readout and the shutter drain high.

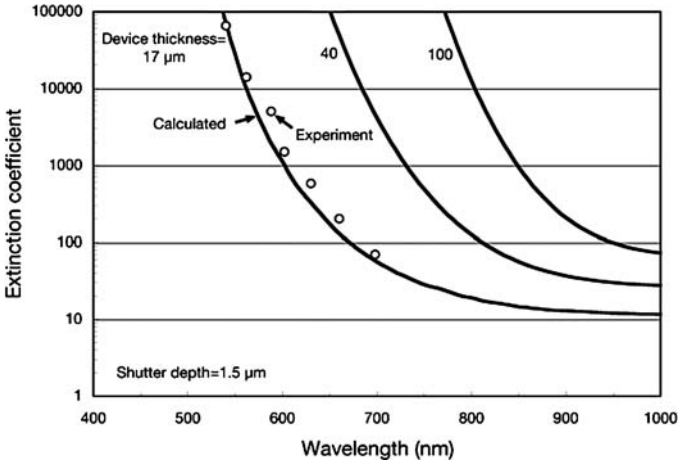


Figure 24. Measured and calculated extinction coefficients. Data and curve for 17-μm-thick device is for T = 20°C, while the 40- and 100-μm calculated extinction is for T = −80°C.

CCD wells. To close the shutter and read out the integrated charge the imaging gates are returned to lower levels, typically <8 V for the high state, in which case the depletion layer collapses to the depth of the shutter implant. To collect photoelectrons while the shutter is closed, the shutter-drain potential is raised to the point where it establishes its own depletion layer and collects photoelectrons.

An important performance metric for the electronic shutter is the extinction ratio, that is, the fraction of photoelectrons collected when the shutter is off. This is principally a problem in the near infrared, where deeply penetrating photons can be absorbed in the surface region above the shutter implant. Figure 24 shows the calculated extinction coefficient at −80°C for back-illuminated devices of various thicknesses and a shutter depth of 1.5 μm. Clearly, a thick device is essential for good extinction out to 1000 nm.

5.2. HYBRID DETECTORS

Hybrid detector arrays exploit the benefits of a detector structure optimized for optical detection combined with a processing circuit to read out the signal. The detector array is dedicated to detecting the incident photons, while the readout circuit controls the operation and produces a suitable output. Infrared detectors are typically hybrid arrays consisting of a detector array fabricated in the proper material and mated to a multiplexer readout circuit. Hybrid detectors are somewhat more complex to build, but the technology effectively addresses some of the limitations of monolithic sensors, such as low fill factor and process incompatibilities between the detector array and the readout multiplexer. A variety of visible hybrid arrays have been developed with different technologies implemented in the detector array.

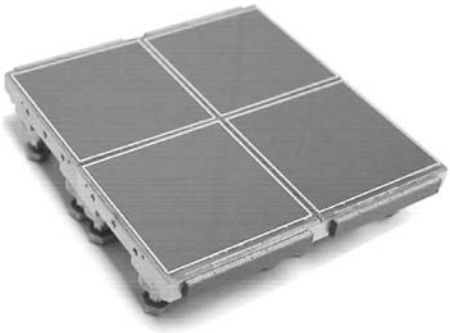


Figure 25. Mosaic array of 2k × 2k PIN hybrid FPAs. Courtesy of Yibin Bai, Rockwell Scientific.

5.2.1. *Silicon p-i-n detector arrays*

The p-i-n detector array consists of a thick (∼185 μm) active region of high-purity silicon sandwiched between regions doped p-type and n-type (Bai et al., 2000). An example of this type of array is shown in Figure 25. The illuminated side is implanted n-type, and the side bonded to the readout circuit is doped p-type.

A high reverse bias is applied to the device, resulting in a strong electric field that separates the electron-hole pairs created by the photons absorbed in the high-resistivity region. The bulk of the detector array is nearly fully depleted, delivering excellent QE at long wavelengths and good MTF characteristics (Kozlowski et al., 2002) since the diffusion crosstalk is negligible. The back-illuminated detector array is bump bonded to a CMOS multiplexer with a bump in each pixel. Noise levels comparable to CCD performance are achievable using Fowler's multiple sampling technique.

5.2.2. *CCD/CMOS hybrid FPAs*

The CCD/CMOS hybrid FPA combines the imaging qualities of the CCD with the high-speed, low-power, and low-noise capabilities of a dedicated CMOS readout integrated circuit (ROIC). An example of this array is shown in Figure 26. In a front-illuminated device, the FPA consists of two CMOS ROICs bump bonded to a CCD detector (Liu et al., 2005). Each readout circuit is an array of capacitive transimpedance amplifiers (CTIAs) that are connected to each end of the CCD columns with indium bumps. A significant advantage of this configuration is that the fabrication process is simplified since fewer bump connections are required, and the design of the readout electronics is not restricted to the area contained within a pixel, which is the case in a conventional hybrid detector. Without the conventional serial shift register and on-chip output amplifiers, the hybrid CCD operates with much lower power while maintaining excellent imaging performance. The column parallel readout architecture reduces the effective output bandwidth and provides sufficient silicon real estate in the ROIC to implement sophisticated amplifier circuit designs that dramatically reduce the readout noise. The CCD power consumption is

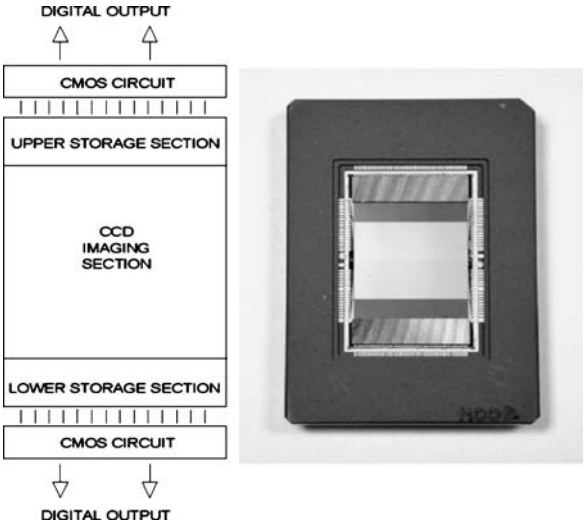


Figure 26. Prototype CCD/CMOS hybrid FPA. Courtesy of Fairchild Imaging.

also reduced, as a result of the elimination of high-speed serial clocking and high-current output amplifiers. This parallel readout arrangement dramatically improves the total frame rate and significantly reduces the noise floor, since the amplifier bandwidth is considerably lower than the level necessary for a conventional CCD with fewer output ports.

5.2.3. *CMOS/CMOS hybrid FPAs*

In CMOS/CMOS hybrid FPAs, a CMOS detector array fabricated for back illumination and biased for deep depletion is combined with a dedicated CMOS readout circuit (Janesick, 2003). A column-wise connection similar to the CCD/CMOS approach described above reduces the number of bump interconnects, lowers power dissipation, and increases speed.

5.2.4. *SOI arrays*

Although relatively new, silicon-on-insulator (SOI) arrays show promising prospects. The devices are fabricated with two silicon layers separated by an insulating oxide layer. The readout circuitry is built in the top "device" layer and the photodiode in the bottom "handle" layer. Separate grounding for each layer eliminates substrate bounce and clock coupling. The resistivity of each layer can be tailored for best performance (Suntharalingam et al., 2004).

5.3. Curved CCDs

It has always been tacitly assumed that image sensors must of necessity be flat, and that optical system designers must therefore take whatever pains and expense are necessary to provide a flat image plane. This assumption is no longer valid,

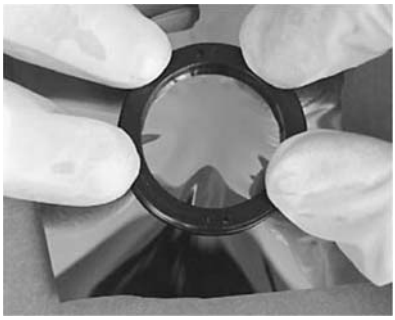


Figure 27. Deformation and buckling of a 20-μm Si membrane over a 175-mm-radius spherical section.

and in fact curved CCDs are now a reality, as evidenced by recent work at Sarnoff (Swain and Mark, 2004) and Lincoln Laboratory (Gregory et al., 2000). Figure 27 is a simple demonstration of silicon deformability in which a 20-μm-thick silicon membrane is pressed down on a 175-mm-radius spherical section.

The mechanical limitations on deformability can be estimated from a simple formula. Consider a circular silicon membrane of radius r deformed to a spherical cap of radius R. The maximum strain is at the center of the cap and is given approximately by $(r/R)^2/6$, assuming the silicon thickness is much smaller than r. For a 60-mm CCD (e.g., a 4k $\times$ 4k, 15-μm-pixel device) and a 1-meter radius of curvature, the maximum strain is $\sim 6 \times 10^{-4}$, which is well below the mechanical limit of $\sim$1% for silicon. The effects of strain on the performance of CCDs have not been thoroughly examined at this point, but preliminary results show the main effect to be an increase in dark current that arises from the decrease in band gap energy E_g. Measurements at Lincoln Laboratory show a dark-current increase that is consistent with a decrease in E_g of 80 meV/(% strain), compared to the theoretical value of 115 meV/(% strain). These numbers can be related to actual dark-current changes using well-known formulas for dark current in silicon (Janesick, 2001).

5.4. Orthogonal-transfer CCD

The orthogonal-transfer CCD (OTCCD) is a unique device in its ability to shift charge in all directions. Figure 28 illustrates a conventional three-phase pixel layout on the left and one of two OTCCD pixel layouts on the right. The unit cell of the OTCCD consists of four phases, and the layout shown here is a symmetrical arrangement of four triangular gates. With the phase-4 gates biased low, phases 1–3 can be clocked to shift charge vertically, while with either phase-1 or phase-3 blocking the remaining phases can shift charge horizontally.

The obvious application of this device in astronomy is to perform electronically the tip-tilt correction to compensate for atmosphere-induced wavefront tilt and telescope shake. Results from a small prototype device (512 $\times$ 512 pixels) were

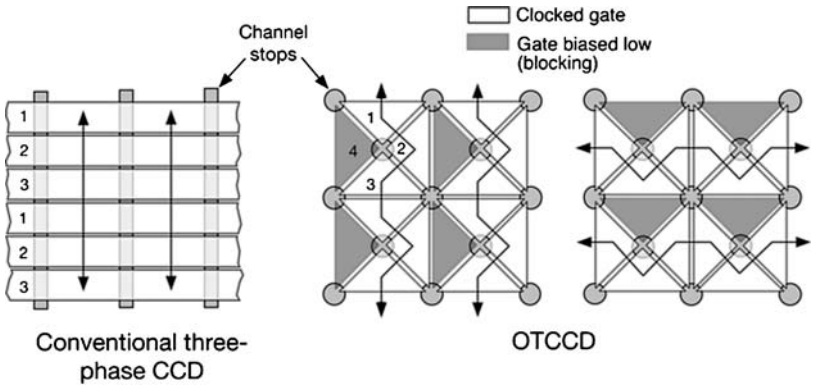


Figure 28. (left) Illustration of a conventional three-phase CCD and *(right)* one of two OTCCD pixel designs.

reported at this conference in 1996 (Tonry and Burke, 1998) and later in more detail (Tonry et al., 1997).

The effectiveness of the device for correcting wavefront tilt is limited to angular distances on the sky of a few milliarcseconds. For wide-field imaging such a device would clearly lose its effectiveness, and a different approach with multiple OTCCDs is needed. Such a device, the orthogonal-transfer array (OTA) (Burke et al., 2004), is now under development for the Panoramic Survey Telescope and Rapid Response System (Pan-STARRS) program. Figure 29 illustrates the basic elements of the OTA under development. The device consists of an 8×8 array of OTCCDs or cells, each comprising about 500×500 pixels. The parallel clocks and the readout amplifier are under the control of a small block of NMOS logic that enables each cell to be controlled and read out independently. In this way each cell can be clocked in a manner that is optimum for the local image motion. Prototype devices have been demonstrated, and the first test results are described elsewhere in these proceedings (Tonry et al., 2005).

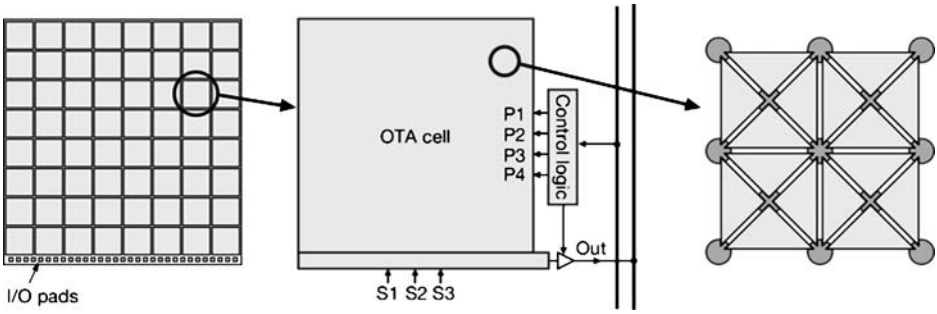


Figure 29. Principal elements of the OTA: *(left)* overall chip layout comprising an 8×8 array of OTCCD cells, *(center)* OTA cell with control logic, and *(right)* one of the OTCCD geometries.

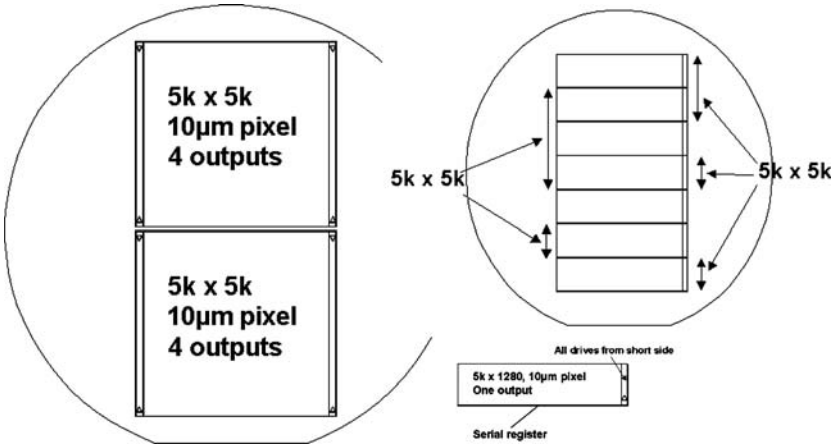


Figure 30. Example of concept for large device (5k × 5k unit from 5k × 1.25k components). Courtesy of e2v technologies.

5.5. CHIP AND PIXEL SIZES

The size of a device is limited by wafer size (∼6 in. is typical for specialist CCD manufacturers), lithography, and yield. Device size is increasing, with 4k × 4k (k = 1024) format becoming available from several manufacturers. For large cost-effective mosaics, special approaches can be adopted to increase yield, e.g., sub-dividing a device into functional units and integrating within the package, such as illustrated in Figure 30.The requirement for a 5k × 5k monolithic device is that there be no fatal defects across the whole area. It is possible to make 5k × 1.25k units on a wafer, select them by probing, and then use special packaging techniques to construct a 5k × 5k unit device with minimal gaps between units. The unit components could be 1.25k, 2.5k, 3.75k, or 5k in height depending on the yield of each wafer.

The size of a pixel is limited by issues of lithography, process, and performance, e.g., full-well capacity. Pixel size is decreasing, with ∼10 μm available from several manufacturers. In many cases, lithography and process developments allow smaller features to be made. Four-phase pixels may become more common in order to help maintain full-well capacity as pixels shrink in size.

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