

# Skipper-in-CMOS: Non-Destructive Readout with Sub-Electron Noise Performance for Pixel Detectors

Agustin J. Lapi, Miguel Sofo-Haro, Benjamin C. Parpillon, Adi Birman, Guillermo Fernandez-Moroni, Lorenzo Rota, Fabricio Alcalde Bessia, Aseem Gupta, Claudio Chavez Blanco, Fernando Chierchie, Julie Segal, Christopher J. Kenney, Angelo Dragone, Shaorui Li, Davide Braga, Amos Fenigstein, Juan Estrada, Farah Fahim

**Abstract**—The Skipper-in-CMOS image sensor integrates the non-destructive readout capability of Skipper Charge Coupled Devices (Skipper-CCDs) with the high conversion gain of a pinned photodiode in a CMOS imaging process, while taking advantage of in-pixel signal processing. This allows both single photon counting as well as high frame rate readout through highly parallel processing. The first results obtained from a  $15 \times 15 \mu\text{m}^2$  pixel cell of a Skipper-in-CMOS sensor fabricated in Tower Semiconductor’s commercial 180 nm CMOS Image Sensor process are presented. Measurements confirm the expected reduction of the readout noise with the number of samples down to deep sub-electron noise of  $0.15\text{e}^-$ , demonstrating the charge transfer operation from the pinned photodiode and the single photon counting operation when the sensor is exposed to light. The article also discusses new testing strategies employed for its operation and characterization.

## I. INTRODUCTION

Skipper-CCDs have an output readout stage with a floating gate that allows multiple non-destructive sampling of the charge packet for each pixel. After averaging the multiple samples, it is possible to achieve an extremely low readout noise of  $0.068 e_{rms}^-/\text{pixel}$ , reaching the absolute theoretical limit of silicon of 1.1 eV in energy threshold. This technology has been recently proved in [1], and its development has been motivated to provide the technology needed to build the next generation of dark matter and neutrino experiments

This work was funded by the DOE Office of Science Research Program for Microelectronics Codesign through the project “Hybrid Cryogenic Detector Architectures for Sensing and Edge Computing enabled by new Fabrication Processes” (LAB 21-2491), with support from DOE’s KA25 Advanced Technology R&D program.

A. Lapi is with the Instituto de Inv. en Ing. Eléctrica “Alfredo Desages” (IIIE), CONICET, with the Universidad Nacional del Sur (UNS), Bahía Blanca 8000, Argentina, and with the Fermi National Accelerator Laboratory, Batavia, IL, USA (e-mail: lapiagustijnavier@gmail.com).

C. Chavez Blanco is with Facultad de Ingeniería de la Universidad Nacional de Asunción (UNA), San Lorenzo, Paraguay, with Universidad Nacional del Sur (UNS), Bahía Blanca, Argentina, and with Fermi National Accelerator Laboratory, Batavia, IL, USA.

F. Chierchie is with Instituto de Inv. en Ing. Eléctrica “Alfredo Desages” (IIIE), CONICET and Universidad Nacional del Sur (UNS), Bahía Blanca, Argentina.

D. Braga, J. Estrada, F. Fahim, S. Li, G. Fernandez-Moroni, B. C. Parpillon are with Fermi National Accelerator Laboratory, IL, USA.

A. Gupta, C. J. Kenney, J. Segal, L. Rota, and A. Dragone are with SLAC National Accelerator Laboratory, CA, USA.

F. A. Bessia is with Centro Atomico Bariloche, Rio Negro, Argentina.

M. Sofo-Haro is with Universidad Nacional de Córdoba (UNC), Córdoba, Argentina.

A. Birman and A. Fenigstein are with Tower Semiconductor, Migdal Haaemek, Israel.

that will be at the forefront of exploring physics beyond the Standard Model [2][3][4][5]. The *Sub-Electron Noise Skipper-CCD Experimental Instrument* (SENSEI) has produced world-leading constraints on low mass dark matter searches [6]. The extremely low readout noise of Skipper-CCD allows the detection of single photons in the optical and near-infrared range. Unlike other silicon detectors with an avalanche gain, with Skipper-CCDs it is possible to directly count the exact number of electrons per pixel and therefore the number of photons that interacted on each pixel, being only limited by the Fano noise [7][8]. Skipper-CCDs have therefore been identified as a powerful tool for quantum information science, giving access to entangled measurements in momentum and spatial variables for single photons and motivating their use for new physics searches [9].

Skipper-CCDs are fabricated in a dedicated facility using a customized process for scientific CCDs [10]. This process is required to produce the overlapping of the gates structures needed to achieve high charge transfer efficiency between pixels. Due to the very low demand of scientific CCDs, compared to commercial CMOS imagers, the number of facilities dedicated to scientific CCDs has reduced to only a few in the world today, and this number is expected to continue dropping [11]. On the other hand, imagers fabricated in CMOS process have dominated the market of high-demand consumer cameras, and therefore several fabrication facilities with many processing options are available. The scaling of CMOS technology to deep submicron has also allowed the implementation of pixels with a very low capacitance, and therefore, high sensitivity and low noise ( $1-2\text{e}^-$ ) at room temperature and high frame rates (50-100 fps) [12][13].

There are therefore a number of compelling reasons to implement Skipper-CCDs in CMOS. The idea can be traced to [14][15], and was more recently revisited in [16][17]. While previous works have successfully implemented CCDs in different single-poly CMOS fabrication technologies achieving high charge transfer efficiencies [18][19][20][21], this article demonstrates the operation of non-destructive charge readout of a n-channel Skipper-in-CMOS image sensor fabricated in Tower Semiconductor TS18 180nm fabrication process. This effort aims to demonstrate low-noise imagers for single-photon detection, leveraging state-of-the-art commercial CMOS processes for ease of manufacture, but also to allow massively parallel readout by hybrid integration with a dedicated readout ASIC including analog-to-digital parallel processing and high bandwidth data transmission. The development could provide

the next generation of detectors for future dark-matter and neutrino experiments, astronomy, and quantum imaging that require single-photon resolution and high readout speed.

The next section describes the architecture of the characterized pixel. Section III addresses first the noise performance of the readout stage and the charge transfer efficiency. Then, the structure is exposed to light to evaluate the charge transfer from the active volume of the pixel and to show the single photon counting capability. A discussion on future work and outlook concludes the article.

## II. PIXEL ARCHITECTURE

The pixel schematic with its critical components is presented in Fig. 1. The primary active region for ionized carrier ion is the Pinned Photo Diode (PPD), on the left it is connected via the PD reset (PDrst) gate to the photodiode drain (PD<sub>drain</sub>). The main purpose of this path is to discharge the PPD and reset it to a known reference voltage.

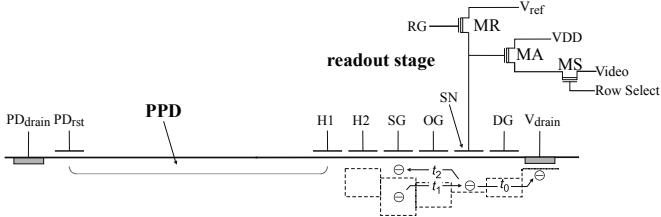


Fig. 1. Schematic of the pixel architecture with main components labeled. The dashed lines provide a qualitative view of the potential in the channel of the output stage during the readout operation.

On the right side, the PPD is capacitively connected to two transfer gates, denoted as H1 and H2. H1 and H2 work in tandem to create a potential barrier when set low; thereby isolating the PPD from the output readout stage. When a new charge packet within the PPD requires measurement, H1 and H2 are operated sequentially facilitating the drift of electrons from the PPD to the Summing Gate (SG). The series SG and Output Gate (OG) are responsible for the back-and-forth charge transfer to the floating Sense Node (SN). Finally the Dump Gate (DG) and the V<sub>drain</sub> are located to the right of the SN.

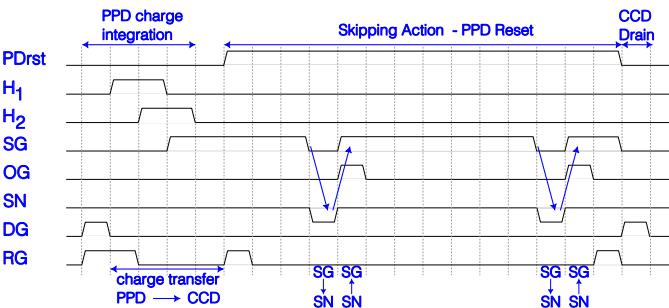


Fig. 2. Timing diagram and charge transfer dynamic for the Skipper-in-CMOS pixel. The CCD gates (SG, OG, SN, DG) are operated as a 3-phase CCD.

The timing diagram for operating the pixel is shown in Fig 2, involving the following phases.

*Initial reset phase:* Resetting the pixel removes the previous charge packet from the PPD. Subsequently, SN is reset to V<sub>ref</sub> through the MR transistor using the Reset Gate (RG) (at time t<sub>0</sub> in Fig. 1). The readout system then measures this reference potential known as the pedestal level.

*Charge transfer to the summing node SG, via the transfer gates H1 and H2.*

*Charge sensing and skipping:* The back-and-forth charge transfer occurs between the summing and sensing nodes SG and SN (at t<sub>1</sub> and t<sub>2</sub> in Fig. 1). The charge packet moves to SN by lowering SG and OG below V<sub>ref</sub>, establishing a barrier between the SG and SN, similar to the standard Skipper CCD operation [22]. The new potential value of the SN is the signal level. A Dual Slope Integration (DSI) technique [23] is used by the readout system to measure the charge in the pixel by subtracting the signal level from the pedestal level. Following the completion of the charge measurement, non-destructive readout can be performed by transitioning OG and SG to high voltage levels, allowing the charge to be drawn back underneath the SG.

The voltage signal in the SN is read out via the n-type source follower transistor MA, designed and optimized for low noise performance, with the assistance of the row-select transistor MS. In the interim periods between charge measurements, SN is reset to the V<sub>ref</sub> potential through the MR reset transistor.

*CCD reset:* Eventually, after several charge measurements, when no further sampling is required, DG is raised high, prompting the movement of the charge to the ohmic contact at V<sub>drain</sub>, connected to an external bias voltage.

Designing the pixel at the device level necessitates the optimization of each component individually through layout and implant schemes tailored to its specific role. The readout source follower MA should be optimized for low noise using a combination of device implant and size, favoring larger sizes for improved performance. However, this comes with a tradeoff, as the capacitance of MA affects the conversion gain of SN. Despite being optimized for noise, a surface channel is employed to achieve higher gain.

The length of DG requires optimization to ensure the isolation of the read node from the drain. H1 and H2 should exhibit perfect transfer, which, in turn, trades off with the isolation of the PPD during integration to prevent the leakage of collected electrons into the CCD device. Optimization of CCD phases, including SG, OG, and SN, is crucial for various performance parameters, with trade-offs between full well (FW) and conversion gain. A larger FW is associated with higher capacitance and lower conversion gain.

To prevent parasitic light sensitivity of the CCD during multiple read stages, a p-type implant under the CCD is essential. However, this poses a challenge to charge transfer efficiency (CTE), even in a short CCD register with multiple read activities. The use of a buried channel CCD becomes crucial for maintaining CTE, ensuring no loss of charge occurs during the repeated movement of charge between the

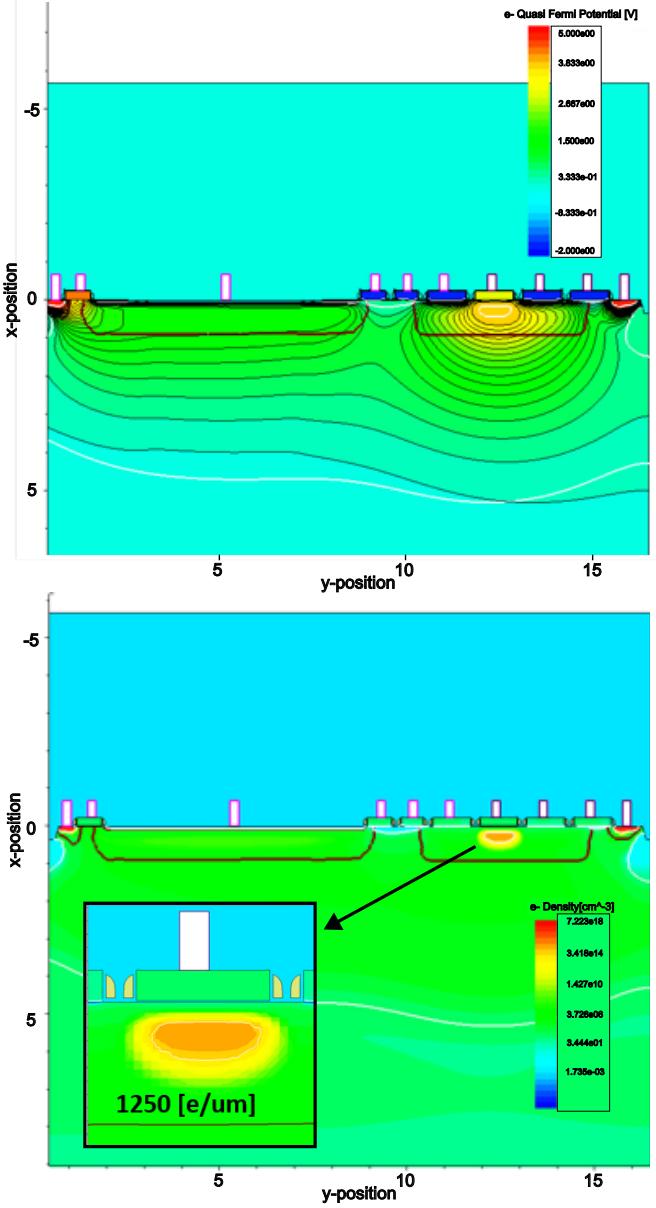


Fig. 3. 2D simulation of the pixel after the transfer of the charge packet (under the output gate OG), for the potential at the top, and the electron density at the bottom. In the latter, the zoomed-in view of the output gate shows the concentrated charge packet.

CCD phases. Detailed TCAD simulations were conducted to optimize these requirements.

Fig. 3 presents 2D simulations of the pixel, illustrating equipotential curves (top) and electron density (bottom) for charge already transferred to the CCD phase. The buried channel filled with charge is distinctly observed in the simulation results.

### III. EXPERIMENTAL RESULTS

A  $5 \times 5$  mm $^2$  Skipper-in-CMOS prototype chip bonded to a PCB board is shown in Fig. 4. The chip includes a matrix of  $200 \times 200$  pixels of  $15 \mu\text{m}$  pitch, along with additional test structures. The inset image shows a smaller test structure

matrix of  $3 \times 3$  pixels. While the test measurement of the large main pixel matrix is currently underway, the central pixel within the smaller matrix was extensively characterized and its detailed results are presented in this paper.

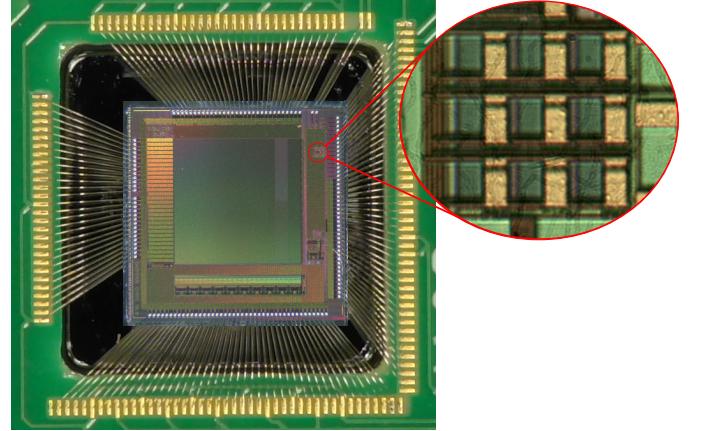


Fig. 4.  $5 \times 5$  mm Skipper-in-CMOS prototype packaged at Fermilab. While the performance of the  $200 \times 200$  pixel matrix is currently under study, this article exclusively showcases results obtained from the test structures highlighted in the zoomed-in view, which contains a  $3 \times 3$  matrix of  $15 \mu\text{m}$  pixels. These pixels have been instrumented to generate the results presented in this article. Specifically, measurements were conducted on the central pixel.

The detector is glued to a silicon substrate, which is then securely attached to the PCB. The silicon substrate possesses identical thermal conductivity, mitigating the risk of die breakage during thermal cycles. The chip is positioned within a square cutout and wire bonded to the PCB. The experimental configuration, as depicted in Fig. 5, involves housing the sensor in a vacuum-sealed, light-tight dewar, positioned on a cold plane connected to a cryocooler and a temperature control system. A constant temperature of 118 K was selected to minimize dark current generation and reduce single electron generation, which facilitates the pixel measurement in low light conditions and enables operation in the single photon regime. Within the controlled chamber, a strategically placed LED illuminates the sensor from the front side, ensuring controlled light exposure.

The PCB sensor board is connected through a flex cable to a feedthrough connector as seen in Fig. 5. Discrete analog electronics bias the MA amplifier in a source follower configuration with  $15\mu\text{A}$  of biasing current. The resulting output video signal is fed to a front-end electronic board, which is connected to the Low Threshold Acquisition (LTA) readout system (both of these are referenced in [24]). The LTA provides clocks and biases for the sensor, digitizes the video signal, and performs digital post-processing to obtain the pixel value through a digital Double Sampling Integrator (DSI).

An important feature of the readout architecture is the utilization of a clock signal, instead of a bias voltage, to set the  $V_{\text{ref}}$  signal of the MR transistor. Setting the correct voltage at RG will put the MR transistor in conduction. Applying a small square pulse signal around the biasing point to  $V_{\text{ref}}$  allows the identification of the correct biasing of the output transistor MA. This process allows for the measurement of

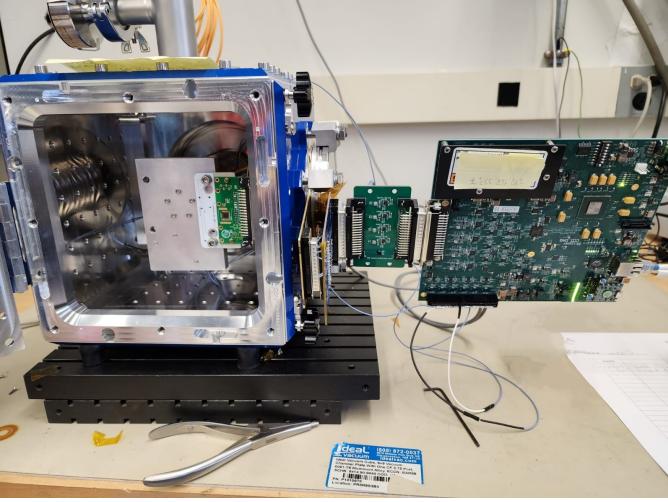


Fig. 5. Experimental setup, where the Skipper-in-CMOS can be seen attached to a cold plate, connected through a cable to an interface board and the LTA readout controller outside of the cryocooler.

the gate gain from the Sense Node (SN) to the input of the ADC in the readout controller (located at the end of the video chain). The sensitivity of the node in ADU/e<sup>-</sup> is instead calibrated in absolute terms based on the single electron peaks. Furthermore, the LED is controlled by the LTA in synchronization with the readout sequence.

Several specific and novel tests were developed to experimentally demonstrate the operation and performance of the proposed pixel architecture with non-destructive readout. Since a single pixel of the test structure is instrumented, the PPD and the output stage were operated in different modes to reveal the diverse capabilities of the pixel. Throughout this article, multiple pixel measurements refer to the repetition of measurements on the same single pixel.

#### A. Multiple non-destructive measurements

The first step involved characterizing the noise reduction capability with varying numbers of non-destructive samples (NSAMP). To achieve this, the readout stage was isolated from the PPD by maintaining H1 and H2 at a low voltage to mitigate potential noise sources from charge collection. Multiple pixel measurements were recorded in this mode, where no charge contribution was expected. This provided noise information from the output transistors and the readout chain. The procedure was iterated for different NSAMP values per pixel.

Fig. 6 displays the noise standard deviation ( $\sigma$ ) for the group of pixels at each NSAMP value. The noise, presented in equivalent carrier units using an absolute calibration method (described in the following section), is depicted by the black line with asterisks. The green line represents the theoretically expected noise starting from the first measurement at NSAMP = 1. As per the  $1/\sqrt{N}$  law, where N is the number of measurements, the noise reduction should follow a decreasing trend with increasing NSAMP. As evident in Fig. 6, the measured noise aligns with this behavior, up to the maximum

tested NSAMP of 3025. The last point indicates a deep sub-electron noise performance of  $0.18e^-$ , crucial for resolving single electrons in subsequent tests. The integration time employed in this case is  $4.6\ \mu s$ . The single sample noise, approximately  $11e^-$ , is higher than expected, which can be attributed to the lack of optimization of the testing setup. Preliminary measurements on standalone transistors within the chip demonstrated lower noise performance.

Using the technique aforementioned, a square signal is applied to  $V_{ref}$ . This signal amplified is measured at the input of the ADC, allowing to compute the gain in terms of V/ADUs. Finally, the noise is measured in the flat areas of this square signal, above and below, to obtain the noise of the stand-alone transistor. The noise of the stand-alone MA source follower transistor was measured at  $0.2e^-$  using this technique.

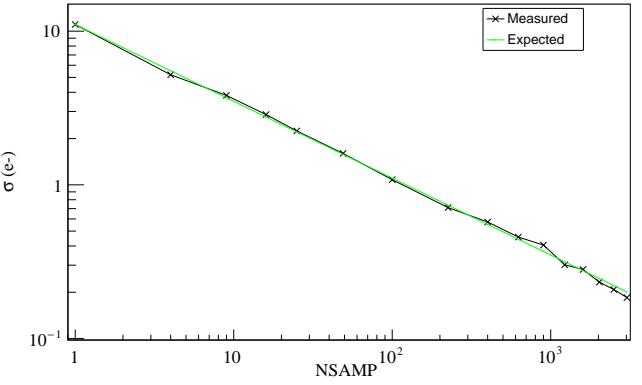


Fig. 6. Noise in electrons as a function of NSAMP. The black line with asterisks is the measured noise, while the green line is the theoretical expected value.

#### B. Charge transfer process in the output stage

After demonstrating that the noise can be reduced with the number of samples NSAMP, another key parameter of the output stage is the transfer efficiency between the SG and the SN nodes. Once the noise is reduced below the expected signal from a single carrier, any charge collected by the readout stage should be seen as a discrete jump in a temporal series of consecutive measurements. If the charge is not dumped, the consecutive pixels should give the same discretized charge information. Following this concept, multiple measurements are taken by repeating the voltage sequence to move the charge back and forth from the SN to SG without dumping the charge into the drain contact. To prevent any extra noise contribution the output stage is isolated from the PPD keeping H1 and H2 at low potential.

Fig. 7 shows an example of the collected measurements grouped in pixels (each point in the figure) with NSAMP = 3025 samples to obtain deep sub-electron noise. The pixel values are in Analog to Digital Units (ADUs). The jumps observed in the series have similar amplitude suggesting quantized increments from the successive charge collected. The points remain constant until the next electron is collected.

This behavior reflects a good transfer efficiency of the charge packet in the output. A positive dependence of the rate of collected carriers in the output stage with the biasing current of the source follower transistor was observed, suggesting transistor luminescence [23]. The biasing current used here is larger than the target design parameter, expecting a further reduction of this rate in future tests.

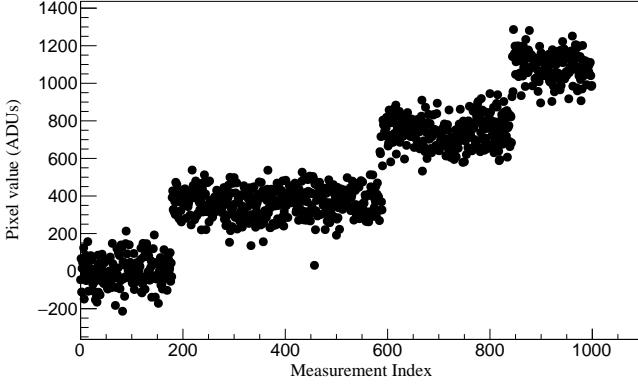


Fig. 7. Continuous measurements charge packet in the output stage when isolated from the PPD. Each measurement corresponds to an average of NSAMP = 3025 samples. Single electron steps are observed.

### C. PPD charge collection and transfer to the output stage

In the final stage of characterization, the sensor's response to an external signal is determined. During this process, the chip is exposed to light for a specific duration while the output stage is maintained at a steady state. Synchronized with the pixel's control sequence, the LED is turned off, while the charge is transferred from the PPD to the output stage for readout. The initial readout corresponds to the light collected by the pixel. To calibrate the pixel reference value for measurements with no charge, multiple readings of the empty PPD were conducted before light exposure. The average of these readings is subtracted from the pixel value with light.

Fig. 8 shows one set of measurements following this protocol. The initial nineteen samples are acquired before light exposure, and their average value serves as the reference for empty pixels. Subsequently, the LED is activated for a designated exposure time, and multiple measurements of the collected charges are recorded before charge dumping. The first measurement after LED exposure is utilized as the light-collected information, adjusted by subtracting the reference value from zero-charge pixels. This process is iterated multiple times to gather statistics from the single pixel.

To plot Fig. 9, the above experiment is repeated with varying exposure times ranging up to 2.66ms. The red dots in the plot show the measured signal, while the blue data were taken with the H clocks low to block the charge flow from the PPD to the output stage. Each data point represents the average value of the collected charge from ten exposures, utilizing non-destructive measurement with NSAMP = 3000.

These results illustrate that, under normal operation, there is successful charge collection in the PPD, which is efficiently

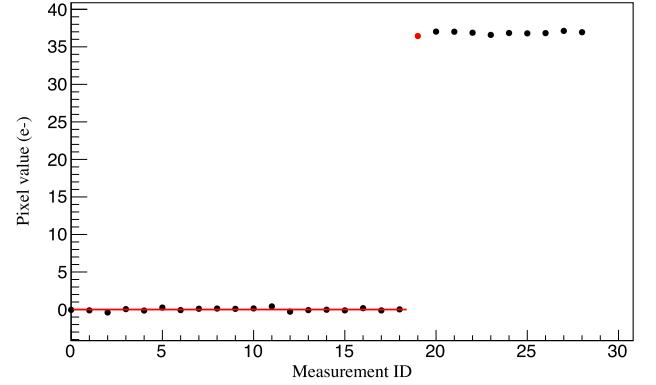


Fig. 8. One set of measured pixels to see the contribution of exposing the device to light. The red dot represents the pixel value when the structure is exposed to light. The red line is the average value of the pixels that are used as the reference value for empty pixels. Since there is no charge dumping, charge accumulation is observed (after ID=18).

transferred through the gates to the output stage. When the clocks act as a barrier, the PPD remains isolated from the output stage. However, a slight dependence on exposure time (approximately  $3e^-$  at 2.66 ms) is observed for the latter scenario, attributed to light directly collected by the output stage. These preliminary tests utilized a standard, non-calibrated LED light source.

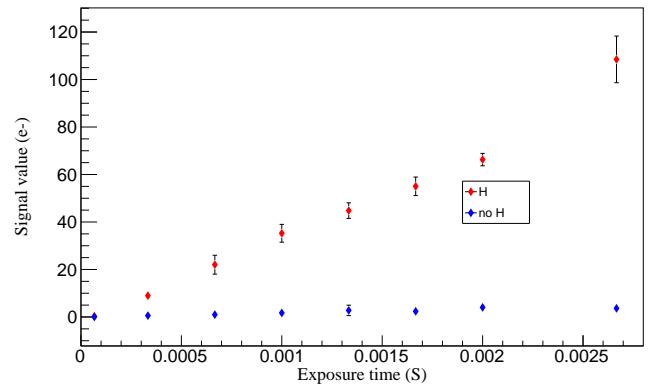


Fig. 9. Light response of the pixel structure for two operating conditions: transferring the charge towards the output stage in red dots, using the H clocks as barriers to isolate the output stage from the PPD in blue dots.

### D. Single photon counting

The experiment performed in section III-C is repeated 3000 times to evaluate the pixel architecture's single electron counting capability when exposed to light. Fig. 10 shows a histogram of the measured charge packets for (top)  $33\mu s$  and (bottom)  $100\mu s$  of LED exposure. Both histograms clearly show the single photon counting resolution with very deep subelectron noise. Intermediate events between peaks could be attributed to charge generation in the output stage during the readout process of the pixel, producing intermediate charge levels. Some preliminary measurements suggest this charge

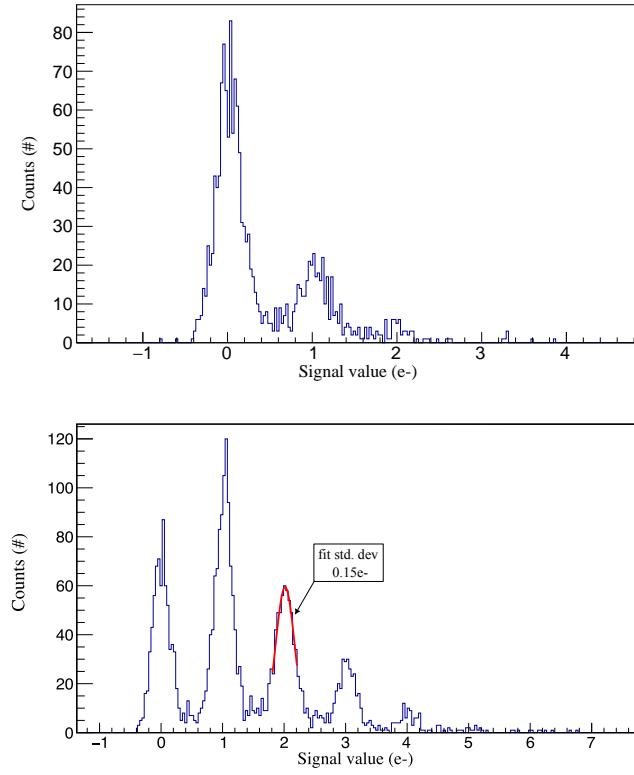


Fig. 10. Charge discretization for two different LED time exposures,  $33\mu\text{s}$  (top) and  $100\mu\text{s}$  (bottom). The Poisson goodness-of-fit values are 1.002 and 1.034 respectively. The bottom figure also shows a normal distribution fit to the  $2e^-$  peak, resulting in a noise deviation of  $0.15e^-$ .

generation is correlated with the biasing current of the source follower transistor and will be part of future analysis and optimization of the sensor.

The ratio between the mean and standard deviations of these distributions are 1.002 and 1.034, respectively, evidencing good matching between the expected Poisson statistical behavior of the photons arriving to the PPD. The bottom of Fig. 10 also shows a normal distribution fitted to the  $2e^-$  peak, the fitted noise is  $0.15e^-$ , matching the expected noise value ( $0.18e^-$ ) for a 3000 NSAMP value, from previous measurements, as indicated in Fig. 6. This was repeated for all the peaks in the image, presenting a similar standard deviation.

#### IV. DISCUSSION AND FUTURE WORK

To the best of the authors' knowledge, the results presented in this paper mark the first experimental demonstration of a CMOS image pixel with non-destructive readout achieving deep sub-electron noise, enabling single electron and photon detection. Various techniques and measurements were developed and tested to assess and showcase the pixel's performance, yielding promising results for the continued advancement of this technology.

Future endeavors will focus on optimizing the pixel's performance and fully instrumenting the entire matrix. The pixel utilized in this study represents only one of six different fabrication splits, each with distinct doping profiles, obtained

from the initial prototype run. Additionally, the  $200 \times 200$  pixel matrix is divided into groups of 10 columns, with each of these 20 groups featuring different pixel characteristics (e.g., transfer gate width, length, etc.) or flavors.

The assessment of different splits and flavors, coupled with the spatial information provided by the two-dimensional pixel array, will aid in optimizing several parameters, including: 1) Single sample noise improvement: Preliminary measurements of the pixel output transistor noise suggest that the total noise before averaging could be significantly reduced. 2) Detailed study of transfer inefficiencies observed in the output stage of the pixel. 3) Utilization of alternative designs for the dump gate and the drain bias voltage structures to optimize the charge dumping process in the output stage. 4) Reduction of significant intrinsic charge generation observed at the output stage by lowering the biasing current of the output transistor. Applying this reduced current biasing to the pixel matrix is expected to substantially decrease charge generation while maintaining similar performance. 5) Exploration of operation at different temperatures to assess sensor performance at higher and room temperatures. 6) Calibration of different amplifiers, exploration of performance, assessment of correlated noise contributions and crosstalk, and implementation of mitigation techniques.

#### V. CONCLUSIONS

The initial results of a pinned photodiode (PPD) fabricated in CMOS technology with a Skipper output stage showcased several key findings. It was demonstrated that charge collection in the PPD was efficiently transferred to the output stage and successfully read out. The PPD was effectively isolated from the output stage via the transfer gates. The multiple non-destructive readouts of the Skipper output stage resulted in the expected  $1/\sqrt{N}$  noise reduction, making it possible to achieve a sub-electronic noise level of  $0.15e^-$ . Single electron counting capability was also demonstrated by the observation of discrete steps at the output stage. Finally, statistical data collection with charged pixels was found to follow the expected Poisson distribution.

These results demonstrate that the development of a Skipper-in-CMOS image sensor in a commercial CMOS process has great potential for applications that require fast readout with single electron counting capability.

#### VI. ACKNOWLEDGMENTS

This manuscript has been authored by Fermi Research Alliance, LLC under Contract No. DE-AC02-07CH11359 with the U.S. Department of Energy, Office of Science, Office of High Energy Physics. This research has been partially supported by Guillermo Fernandez Moroni's DOE Early Career research program.

#### VII. AUTHOR DECLARATIONS AND CONTRIBUTIONS

The authors have no conflicts to disclose.  
Conceptualization: FF, JE, MSH, AD, CK, AF. Supervision, Project Administration: DB, GFM, SL, FF, BP, LR. Funding

acquisition JE, FF, AD, DB, GFM. Investigation, Methodology, Formal Analysis, Visualization (Pixel Simulations): AB, MSH, JS. Investigation, Methodology, Formal Analysis (ASIC design): BP, FAB, LR, AG, MSH. Investigation, Methodology, Formal Analysis, Data Curation, Visualization (Instrumental development and sensor characterization): AJL, GFM, MSH, FAB, CCB, FC. Writing – original draft: AJL. Writing – review & editing: DB, FF, GFM, FC.

## REFERENCES

- [1] J. Tiffenberg, M. Sofo-Haro, A. Drlica-Wagner, R. Essig, Y. Guardincerri, S. Holland, T. Volansky, and T.-T. Yu, “Single-electron and single-photon sensitivity with a silicon Skipper CCD,” *Phys. Rev. Lett.*, vol. 119, no. 13, p. 131802, 2017.
- [2] L. Barak, I. M. Bloch, M. Cababie, G. Cancelo, L. Chaplinsky, F. Chierchie, M. Crisler, A. Drlica-Wagner, R. Essig, J. Estrada, E. Etzion, G. F. Moroni, D. Gift, S. Munagavalasa, A. Orly, D. Rodrigues, A. Singal, M. S. Haro, L. Stefanazzi, J. Tiffenberg, S. Uemura, T. Volansky, and T.-T. Yu, “SENSEI: Direct-detection results on sub-gev dark matter from a new Skipper CCD,” *Phys. Rev. Lett.*, vol. 125, p. 171802, Oct 2020.
- [3] A. Aguilar-Arevalo, F. A. Bessia, N. Avalos, D. Baxter, X. Bertou, C. Bonifazi, A. Botti, M. Cababie, G. Cancelo, B. A. Cervantes-Vergara, N. Castello-Mor, A. Chavarria, C. R. Chavez, F. Chierchie, J. M. D. Egea, J. C. D’Olivo, C. E. Dreyer, A. Drlica-Wagner, R. Essig, J. Estrada, E. Estrada, E. Etzion, G. Fernandez-Moroni, M. Fernandez-Serra, S. Holland, A. L. Barreda, A. Lathrop, J. Lipovetzky, B. Loer, E. M. Villalpando, J. Molina, S. Perez, P. Privitera, D. Rodrigues, R. Saldanha, D. S. Cruz, A. Singal, N. Saffold, L. Stefanazzi, M. Sofo-Haro, J. Tiffenberg, C. Torres, S. Uemura, and R. Vilar, “The oscura experiment,” 2022.
- [4] A. Aguilar-Arevalo, X. Bertou, C. Bonifazi, G. Cancelo, A. Castañeda, B. Cervantes Vergara, C. Chavez, J. C. D’Olivo, J. a. C. dos Anjos, J. Estrada, A. R. Fernandes Neto, G. Fernandez Moroni, A. Foguel, R. Ford, J. Gonzalez Cuevas, P. Hernández, S. Hernandez, F. Izraelevitch, A. R. Kavner, B. Kilminster, K. Kuk, H. P. Lima, M. Makler, J. Molina, P. Mota, I. Nasteva, E. E. Paolini, C. Romero, Y. Sarkis, M. Sofo Haro, I. a. M. S. Souza, J. Tiffenberg, and S. Wagner, “Exploring low-energy neutrino physics with the coherent neutrino nucleus interaction experiment,” *Phys. Rev. D*, vol. 100, p. 092005, Nov 2019.
- [5] J. C. D’Olivo, C. Bonifazi, D. Rodrigues, and G. F. Moroni, “vIOLETA: Neutrino Interaction Observation with a Low Energy Threshold Array,” in *XXIX International Conference in Neutrino Physics*, poster 521, Jun. 2020.
- [6] O. Abramoff et al., “SENSEI: Direct-Detection Constraints on Sub-GeV Dark Matter from a Shallow Underground Run Using a Prototype Skipper-CCD,” *Phys. Rev. Lett.*, vol. 122, no. 16, p. 161801, 2019.
- [7] J. Janesick, T. Elliott, R. Bredthauer, C. Chandler, and B. Burke, “Fano-Noise-Limited CCDs,” in *X-Ray Instrumentation in Astronomy II*, L. Golub, Ed., vol. 0982, International Society for Optics and Photonics. SPIE, 1988, pp. 70 – 95. [Online]. Available: <https://doi.org/10.1117/12.948704>
- [8] D. Rodrigues, K. Andersson, M. Cababie, A. Donadon, A. Botti, G. Cancelo, J. Estrada, G. Fernandez-Moroni, R. Piegaia, M. Senger, M. S. Haro, L. Stefanazzi, J. Tiffenberg, and S. Uemura, “Absolute measurement of the fano factor using a Skipper-CCD,” *Nuclear Instruments and Methods in Physics Research Section A: Accelerators, Spectrometers, Detectors and Associated Equipment*, vol. 1010, p. 165511, 2021.
- [9] J. Estrada, R. Harnik, D. Rodrigues, and M. Senger, “Searching for dark particles with quantum optics,” *PRX Quantum*, vol. 2, p. 030340, Sep 2021. [Online]. Available: <https://link.aps.org/doi/10.1103/PRXQuantum.2.030340>
- [10] Teledyne-DALSA. CCD Foundry services, 2019.
- [11] K. Dawson, S. Holland, and D. Schlegel, “Maintaining capabilities in ccd production for the astronomy community,” 2019.
- [12] C. Ma, Y. Liu, J. Li, Q. Zhou, Y. Chang, and X. Wang, “A 4MP high-dynamic-range, low-noise CMOS image sensor,” in *Image Sensors and Imaging Systems 2015*, R. Widenhorn and A. Dupret, Eds., vol. 9403, International Society for Optics and Photonics. SPIE, 2015, p. 940305. [Online]. Available: <https://doi.org/10.1117/12.2083085>
- [13] B. Fowler, C. Liu, S. Mims, J. Balicki, W. Li, H. Do, J. Appelbaum, and P. Vu, “A 5.5Mpixel 100 frames/sec wide dynamic range low noise CMOS image sensor for scientific applications,” in *Sensors, Cameras, and Systems for Industrial/Scientific Applications XI*, E. Bodegom and V. Nguyen, Eds., vol. 7536, International Society for Optics and Photonics. SPIE, 2010, p. 753607. [Online]. Available: <https://doi.org/10.1117/12.846975>
- [14] E. R. Fossum, “Active pixel sensors: Are ccds dinosaurs?” in *Charge-Coupled Devices and Solid State Optical Sensors III*, vol. 1900, SPIE, 1993, pp. 2–14.
- [15] S. K. Mendis, B. Pain, R. H. Nixon, and E. R. Fossum, “Design of a low-light-level image sensor with on-chip sigma-delta analog-to-digital conversion,” in *Charge-Coupled Devices and Solid State Optical Sensors III*, vol. 1900, SPIE, 1993, pp. 31–39.
- [16] K. D. Stefanov, M. J. Prest, M. Downing, E. George, N. Bezawada, and A. D. Holland, “Simulations and design of a single-photon cmos imaging pixel using multiple non-destructive signal sampling,” *Sensors*, vol. 20, no. 7, p. 2031, 2020.
- [17] Y. Zhou, Y. Qu, Q. Zang, B. Wei, J. Wu, G. Peng, Y. Chang, and Y. Liu, “A low readout noise cmos pixel based on the skipper technology,” in *2022 23rd International Conference on Electronic Packaging Technology (ICEPT)*. IEEE, 2022, pp. 1–6.
- [18] P. Boulenc, J. Robbelein, L. Wu, L. Haspeslagh, P. D. Moor, J. Borremans, and M. Rosmeulen, “High speed TDI embedded CCD in CMOS sensor,” in *International Conference on Space Optics — ICSO 2016*, B. Cugny, N. Karafolas, and Z. Sodnik, Eds., vol. 10562, International Society for Optics and Photonics. SPIE, 2017, p. 105622P. [Online]. Available: <https://doi.org/10.1117/12.2296149>
- [19] J. Crooks, B. Marsh, R. Turchetta, K. Taylor, W. Chan, A. Lahav, and A. Fenigstein, “Kirana: a solid-state megapixel uCMOS image sensor for ultrahigh speed imaging,” in *Sensors, Cameras, and Systems for Industrial and Scientific Applications XIV*, R. Widenhorn and A. Dupret, Eds., vol. 8659, International Society for Optics and Photonics. SPIE, 2013, p. 865903. [Online]. Available: <https://doi.org/10.1117/12.2011762>
- [20] O. Marcelot, M. Estribeau, V. Goiffon, P. Martin-Gonthier, F. Corbière, R. Molina, S. Rolando, and P. Magnan, “Study of ccd transport on cmos imaging technology: Comparison between sccd and bccd, and ramp effect on the cti,” *IEEE Transactions on Electron Devices*, vol. 61, no. 3, pp. 844–849, 2014.
- [21] K. Fife, A. E. Gamal, and H.-S. P. Wong, “Design and characterization of submicron ccds in cmos,” *International Image Sensor Workshop*, 2009.
- [22] G. Fernandez Moroni, J. Estrada, G. Cancelo, S. Holland, E. Paolini, and H. Diehl, “Sub-electron readout noise in a Skipper CCD fabricated on high resistivity silicon,” *Experimental Astronomy*, vol. 34, 07 2012.
- [23] J. R. Janesick, *Scientific charge-coupled devices*. SPIE press, 2001, vol. 83.
- [24] G. I. Cancelo, C. Chavez, F. Chierchie, J. Estrada, G. Fernandez-Moroni, E. E. Paolini, M. S. Haro, A. Soto, L. Stefanazzi, J. Tiffenberg, K. Treptow, N. Wilcer, and T. J. Zmuda, “Low threshold acquisition controller for Skipper charge-coupled devices,” *Journal of Astronomical Telescopes, Instruments, and Systems*, vol. 7, no. 1, pp. 1 – 19, 2021.