2.5D Interposers and Advanced Organic Substrates Landscape: Technology and Market Trends

A. Ivankovic, T. Buisson, S. Kumar, A. Pizzagalli, J. Azemar, R. Beica
Yole Developpement
75 cours Emile Zola
Villeurbanne, 69100 France
Ph: +33-472-830-196; Fax: +33-472-830-183
Email: ivankovic@yole.fr

Abstract

This work focuses on the analysis of recent developments and future trends of organic substrates and 2.5D interposers. In the sub 10 µm line/width space, substrate manufacturers are pushing towards traditionally foundry level Si processing dimensions. Latest R&D shows organic substrates with L/S capability down to 2/2 µm. Organic substrates and 2.5D interposers can be in many cases separated in two different groups, however certain solutions propose a combination of the two, such as embedded interposers or fine extension layers of organic substrates acting as interposers. These substrate and interposer architectural solutions are analyzed. Furthermore, organic processing options and latest feature sizes are discussed. Dielectric build up material options with low dielectric constant (D_k) and low tangent loss (D_f) are analyzed and their expected thermo-mechanical property trends presented, including the coefficient of thermal expansion (CTE), Young's modulus (E) and glass transition temperature (T_g). Coreless substrates and their advantages, disadvantages, industry readiness and future development are also addressed. Furthermore, 2.5D interposer options are analyzed by type of material: Si, glass and organic. A qualitative and quantitative comparison of their features and market status is done and their future development is extrapolated. Final conclusions are made on the sub 10 µm line/width advanced substrate application space and the market interaction of organic substrates and 2.5D interposers

Key words

Substrate, Organic, Interposer, 2.5D, market, technology trends

I. Introduction

The semiconductor industry is facing a new era in which device scaling and cost reduction will not continue on the path they followed for the past few decades, with Moore's law in its foundation. Advanced nodes do not bring the desired cost benefit anymore and R&D investments in new lithography solutions and devices below 10nm nodes are rising substantially. In order to answer market demands, the industry seeks further performance and functionality boosts in integration. While scaling options remain uncertain in the shorter term and continue to be investigated, the spotlight is turned to advanced packages [1-4].

Emerging packages such as fan-out wafer level packages and 2.5D/3D IC solutions together with more conventional but upgraded flip chip BGAs or SiPs aim to bridge the gap and revive the cost/performance curve while at the same time adding more functionality through integration.

Future advanced packages need to tackle the explosion in information exchange translating to high number of I/Os and be able to support heterogeneous integration. This puts particular pressure on die to board interconnects. Technologies to fill the void created in diverging PCB versus IC feature sizes are constantly under development.
In the sub 10 µm package substrate line/width space (L/S), substrate manufacturers are pushing towards traditionally foundry level Si processing dimensions. Latest R&D shows organic substrates with L/S capability down to 2/2 µm. This work focuses on the analysis of recent developments of organic substrates and 2.5D interposers and their technology and market trends.

Firstly, the application space in which advanced substrates are competing is introduced, followed by recent architectural solutions. Subsequently, advantages and disadvantages of interposers by material type and coreless substrates are analyzed. Lastly, latest organic substrate

feature sizes are discussed and build up dielectric material options and characteristics for high performance organic substrates analyzed.

II. Advanced substrate application space

As substrate feature sizes are decreasing, the sub 10 µm line/width area is becoming a competitive playground where both substrate and foundry level manufacturers see business potential, promoting their solutions. Figure 1 visualizes the area of interest. PCB design rules reign above 10 µm line width/space while the stronghold of wafer level foundry processes is below 1 µm line width/space. The gap between 1 µm and 10 µm represents an area where different materials, processes and architectures are competing today. Organic substrates are scaling L/S below 10 µm towards foundry features while Silicon substrates have the ability to expand into coarser territory above L/S 1 µm.

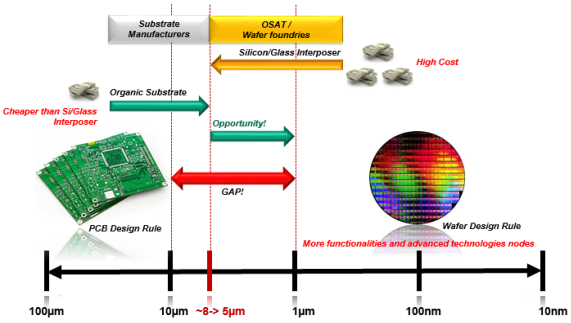

Fig. 1: Substrate technology gap between 10 µm and 1 µm entered by both substrate manufacturers and foundries

III. Recent substrate architectures

Organic substrates and 2.5D interposers can be in many cases separated in two different groups, however the distinction is becoming less clear with time. Certain solutions propose a combination of the two, such as embedded Si interposers in an organic substrate or fine extension layers of organic substrates, acting as traditional substrate and interposer in one. Furthermore, options such as interposer directly on board are also explored.
Figures 2-5 present some of the possible solutions proposed today. Figure 2 a) represents a illustration of a Si interposer on an organic substrate, while figure 2 b) depicts the same structure, with a glass interposer. In figure 2 c) the Si interposer is embedded within the organic substrate.

Figure 3 shows the approach of fine organic extension layers on a traditional organic substrate. Figure 4 represents an approach with an organic interposer either stacked on a traditional build up substrate or standalone, connected directly to the board. Figure 5 visualizes a coreless organic substrate, which does not necessarily compete directly in the interposer space, but is representative for the advanced flip chip substrate mono die space.

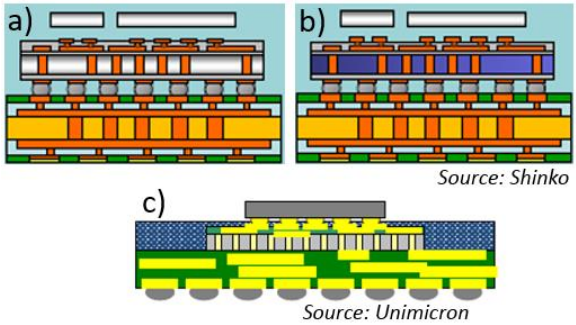

Fig. 2: Recent interposer architectures, a) Si interposer on organic substrate, b) Glass interposer on organic substrate and c) Si interposer embedded in organic substrate

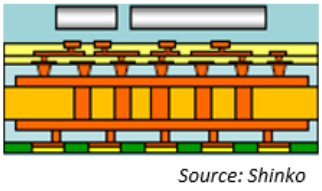

Fig. 3: Integration of interposer as fine pitch organic extension layers.

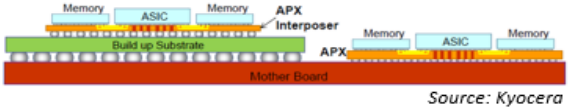

Fig. 4: Organic interposer either stacked on a traditional build up substrate or standalone connected directly to the board

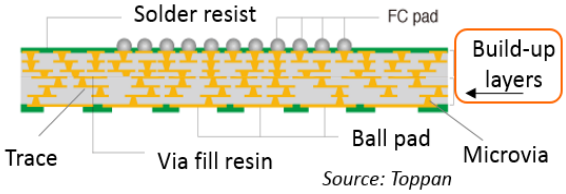

Fig. 5: Coreless substrate, competing primarily in the advanced flip chip substrate space with opportunity to extend to interposer space

Si interposers are already in production while other developed structures are commercially available or production ready. An example for the embedded Si interposer would be Unimicron's embedded interposer carrier (EIC), for the fine organic extension layers Shinko's i-THOP and for an organic interposer Kyocera's APX.

The solutions can be segmented by type of connectivity and base substrate material, as summarized in table 1.
By material, an interposer can be Si, glass or organic based. In the case of an interposer on the organic substrate, the interposer target material is usually Si or glass. In an embedded interposer case, organic materials encapsulate the Si interposer or build up extension of fine organic layers act as an embedded organic interposer. Si, glass and organic interposers directly on board are also investigated.

By type of connectivity, an interposer can be stacked on an organic substrate, embedded within the organic substrate (embedded Si interposer or organic extension layers on organic substrate) or placed directly on the board. An organic interposer directly on board is essentially a flip chip substrate which may or may not be coreless. Coreless substrates are put in a separate category as they mostly aim smaller dimensions comprising one die due to potential warpage control difficulties.

Table 1: Interposer solutions segmented by connectivity and material

Advanced substrate segmentation	
BY CONNECTIVITY	BY MATERIAL
• Interposer on substrate • Embedded interposer • Interposer directly on board • Coreless substrate	• Si • Glass • Organic

IV. Interposer comparison

The benefit of embedding a Si interposer would be eliminating solder joints between interposer and substrate, possible layer and cost reduction by integration, only 2 testing steps (interposer alone and within substrate) and no change in infrastructure. A fine layer extension would essentially provide the same benefits with potential disadvantage in large substrate size for thin film process.

Furthermore, an organic interposer could match performance at lower cost than Si or glass, but potential warpage issues need to be addressed. Glass interposers can provide good performance and they have cost down potential, but the technology is still immature with via formation still being challenging and some concerns present on glass brittleness. Process complexity, yield and cost will remain crucial questions in all cases.

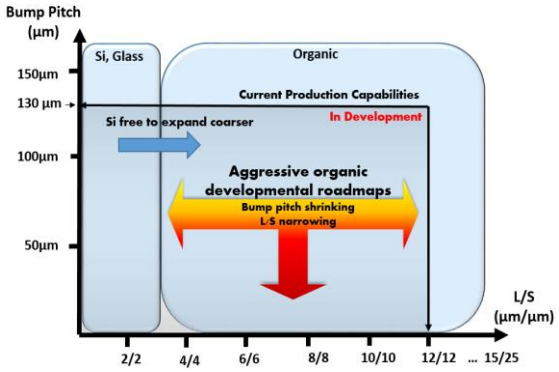

Fig. 6: Substrate line width/space and bump pitch expectations for Si/glass interposers versus organic substrates/interposers.

Coarse Si interposers seem to be still the first choice for lower end products. Organic sub 10 µm substrates are generally promising, but need to have a more clear cost reduction path to enable this sector.

Figure 6 visualizes the bump pitch and substrate line width/space for Si and glass interposers versus organic substrates/interposers. The sweet spot for coarse Si interposers could be up to 3/3 µm while substrate manufacturers announced R&D prototypes going down to 2/2 µm, with 3/3 µm possibly commercially available already end of this year. Si interposers are free to expand coarser.

Table 2: Interposer applications by base material

HIGH END PRODUCTS	MID RANGE PRODUCTS	LOW COST PRODUCTS
Networking, servers	Gaming, Graphics, HDTV, Adv. tablets	Lower end tablets, Smartphones
>25k bumps	~10k bumps	~2k bumps
Si IP	Si IP Glass IP	Si IP Glass IP Organic IP

Table 2 estimates interposer applications by base material. High end products such as networks and servers with more than 25k bumps will necessitate Si interposers. Mid range products related to gaming, graphics, HDTV, advanced tablets, with around 10k bumps might also extend to glass interposer. Coarse Si and glass interposers might be suitable for low cost products as well, however this should be the main target of organic interposers.

V. Coreless substrates

Taking the substrate core out can bring many performance benefits, primarily making the substrate thinner and enabling higher via density with plated through holes out of the picture. Furthermore, this brings certain cost reduction and boosted electrical performance with less parasitics and better high speed transmission. Figure 7

illustrates the thickness reduction and wiring flexibility from BGA substrates over CSP substrates to coreless substrates.

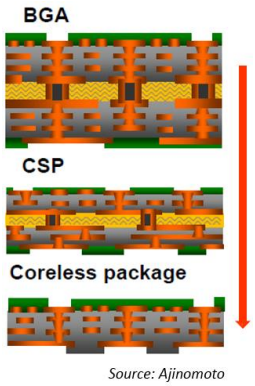

Fig. 7: Illustration of thickness and wiring flexibility from BGA over CSP to coreless substrates.

Coreless substrates do not directly compete in the interposer arena and are aiming at high performance mono die packages. Wafer level packages would present primary competition. The primary limitation of a coreless substrate is its warpage and therefore allowed overall size. However careful choice of dielectric material and warpage mitigation solutions such as metal capping stiffeners can increase the size of the substrate, potentially allowing them to hold multiple dies.

Other disadvantages include easily occurring laminate chipping and the necessity for new manufacturing infrastructure.

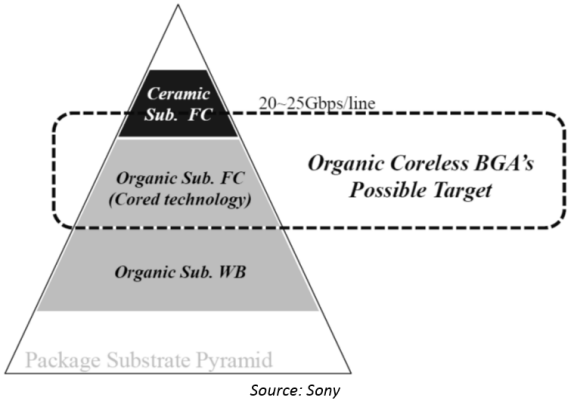

Fig. 8: Potential application space of coreless substrates.

Due to the technical improvement, the main target of coreless substrates could be all flip chip organic substrates, while lower cost potential could turn them towards parts of the ceramic substrate market, as shown in figure 8. With warpage under control they could also target the market with interposer connected directly to the board, however interest in Si interposers directly on board and particularly fan-out multi chip solutions is high.

VI. Organic materials

The electrical and thermo-mechanical performance of a package as a whole highly depends on the properties of the substrate dielectric material. In a coreless substrate, with the substrate core removed, build up dielectrics have a crucial impact on signal propagation and package warpage.

Within the scope of high performance coreless substrates, advanced materials are constantly under investigation. Figure 9 presents a non-exhaustive segmentation of dielectric materials for standard and high performance applications. Standard dielectric materials involve epoxy based products such as FR4 and BT. The advanced dielectric material space (non-exhaustive) can be divided into epoxy based materials, fluoropolymers and polyamides.

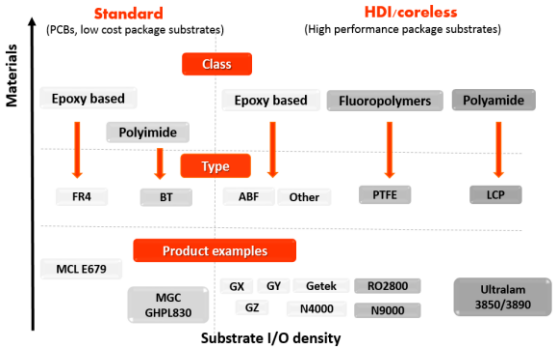

Fig. 9: Non-exhaustive segmentation of potential dielectric build up materials for advanced substrates.

A typical epoxy based representative widely used in advanced substrates is Ajinomoto build up film (ABF). Polytetrafluoroethylene (PTFE) and liquid crystal polymers (LCP) are materials that have existed for a long time, but have had limited adoption within substrates, although they can exhibit superior properties compared to current ABF.

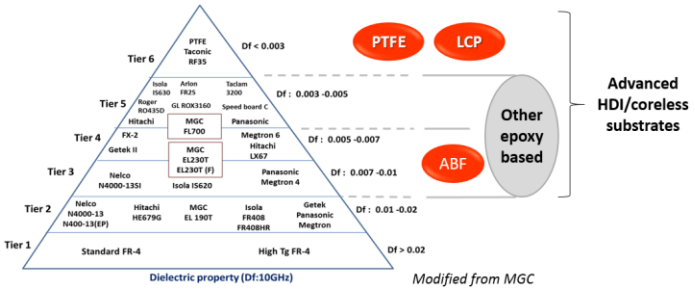

Fig. 10: Advanced substrate dielectric build up materials according to loss tangent

When ranked according to the loss tangent (D_f), as in figure 10, PTFE and LCP are on the top of the pyramid, above epoxy based materials, with loss tangent values below 0.003.

Table 3: Comparison of potential dielectric build up materials for advanced substrates by CTE, D_k and D_f

Attribute	Standard	HDI/coreless		
	Epoxy Glass or polyimide	ABF	LCP	PTFE
CTE [ppm/°C]	19	18	17	12
Dk	4.1	3.4	2.9	2.7
Df	0.011	0.0057	0.0025	0.0017

In table 3, the 3 high performance candidates in discussion and epoxy based materials are compared based on their dielectric constant (D_k), tangent loss (D_f) and coefficient of thermal expansion (CTE). LCP and PTFE have potentially lower expansion and better electrical performance capabilities than current ABF.

Table 4 summarizes the current status of advanced organic substrate dielectric properties for high performance applications.

Table 4: Current status of advanced organic substrate dielectric properties for high performance applications

Parameter	Symbol	Unit	Typical low value	Trend
Dielec. constant	Dk	-	3	↘
Loss tangent	Df	-	0.005	↘
Coeff. thermal exp.	CTE x-y	[ppm/°C]	12	↘
Coeff. thermal exp.	CTE z	[ppm/°C]	40	↘
Glass trans. Temp.	Tg	[°C]	210 *	→
Young's modulus	YM	[GPa]	5	—
Dielectric thickness	td	[µm]	25-30	↘
Trace width	L	[µm]	10	↘
Trace space	S	[µm]	10	↘
Microvia diameter	D	[µm]	50	↘

*maximum value

VII. Conclusions

A clear substrate technology gap exists in the substrate line/width space between 10 µm and 1 µm, as shown in figure 1. This competitive area is entered both from substrate manufacturer side with PCB based processes and foundry side with wafer based processes. While foundries typically propose coarse Si or glass interposers, substrate manufacturers propose organic based solutions or integration of the Si/glass interposer within an organic substrate. Figures 2 and 3 summarize the current proposed architectures while table 1 segments the options by connectivity and base material used.

Coarse Si interposers seem to be still the first choice for lower end applications. Organic sub 10 µm substrates are generally promising, but need to have a more clear cost reduction path to enable this sector. Table 2 summarizes possible product applications for Si, glass and organic interposers.

From a feature size viewpoint, organic substrates might find their sweet spot down to 3/3 µm. Announcements have been made for first 3/3 µm substrates scheduled end of this year, while 2/2 µm feature sizes are in R&D phase. Coarse Si interposers are expected to cover feature sizes below 3/3 µm.

Coreless substrates can enable thinner packages with higher density interconnects, while providing better electrical performance due to lower parasitics and propagation time, at lower cost. Their primary target is mono die packages, but as solutions arise for warpage control they might be looking into application opportunities in multi die systems directly on board. However, the competition in this area is fierce especially with fan-out wafer level packages making significant progress and interest in Si interposers directly on board.

Regarding dielectric build up materials for high performance organic substrates, progress is being made in both electrical performance, with D_k below 3 and D_f below 0.003 and thermo-mechanical performance, with CTE reaching 10 ppm/°C in x-y direction and below 40 ppm/°C in z direction. ABF is a widespread dielectric in use, while PTFE and LCP exhibit potential with superior properties to current ABF.

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