

# CMOS sensors

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# Introduction

- ASIC-Design and Detector Technology Group at the Karlsruhe Institute for Technology
- KIT = unified University of Karlsruhe and the Research Centre Karlsruhe



University of Karlsruhe

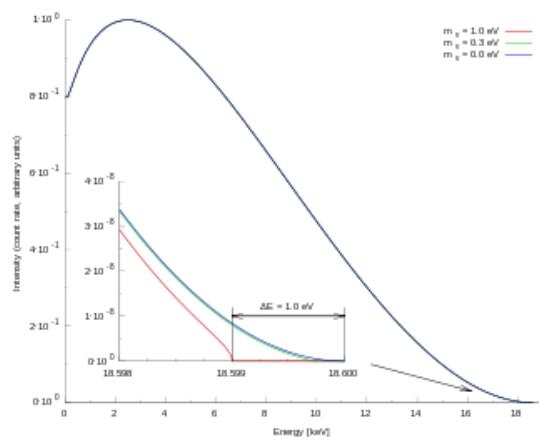


Research Centre Karlsruhe

- Neutrino Experiment KATRIN, synchrotron source ANKA, proton irradiation facility

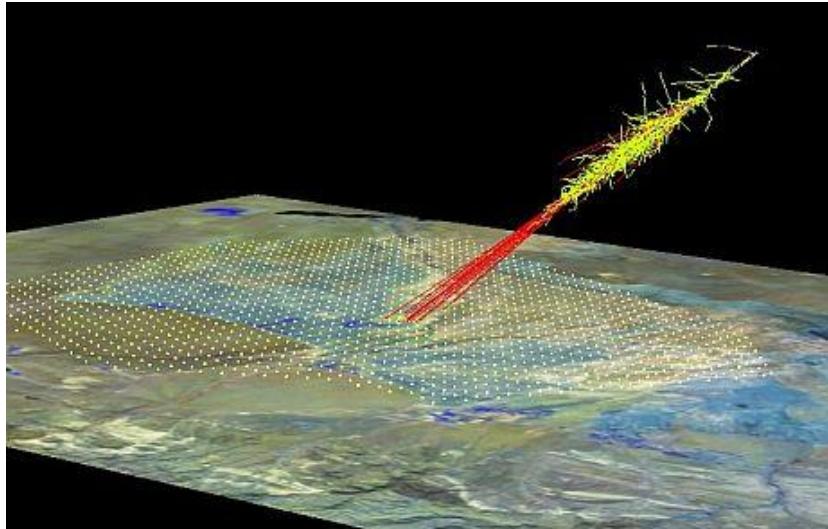


KATRIN



ANKA

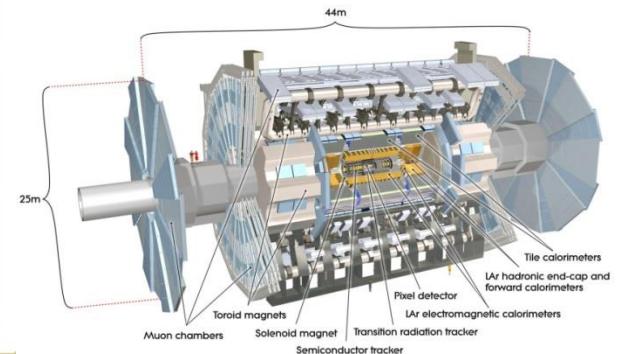
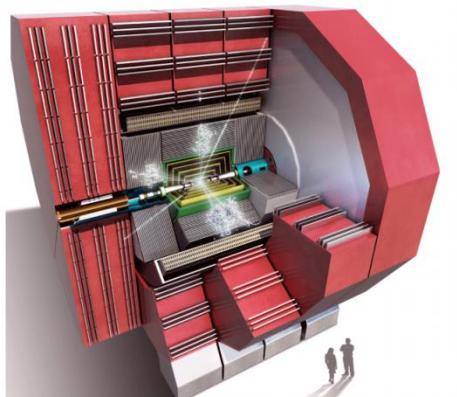
- IPE – Institute for Data Processing and Electronics



Auger Telescope



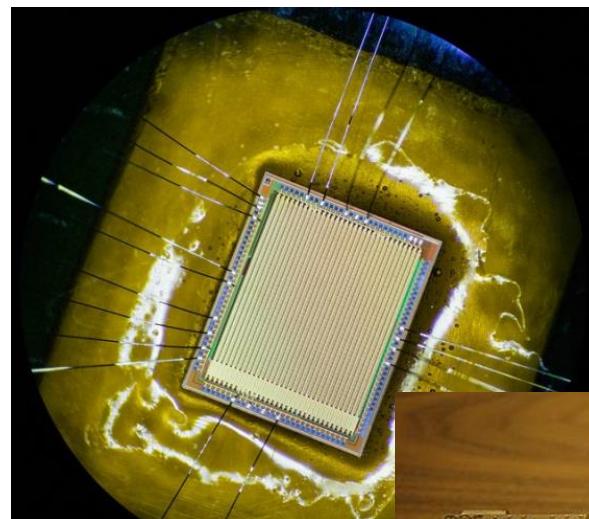
3D ultrasound imager



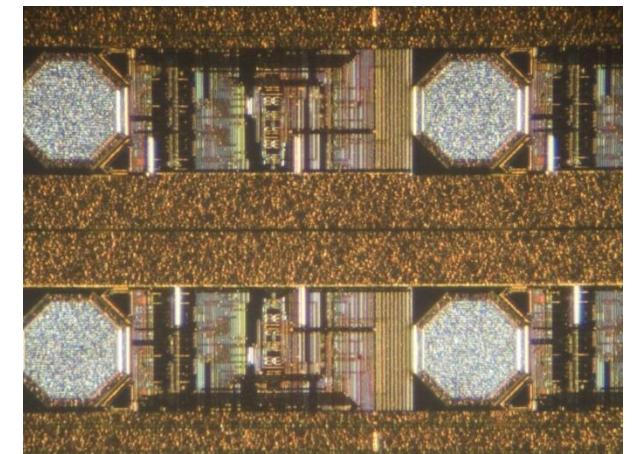
- Studies: Electrical Engineering at the University of Belgrade in Serbia
- PhD studies: Bonn
- University of Mannheim, Heidelberg, KIT
- Research themes
- Pixel readout chip for ATLAS – FEI3
- Design of high voltage driver- and readout chips for the DEPFET detector (Belle II KEK)
- Hybrid sensors for medical imaging
- SiPM readout for PET
- HVCmos sensors



PET



Mu3e (HVCmos)



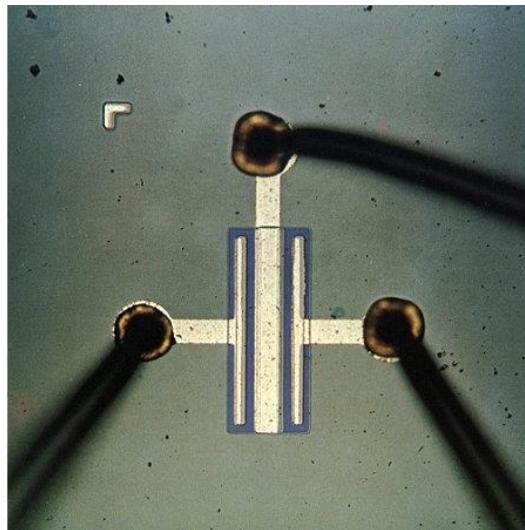
Belle II PXD



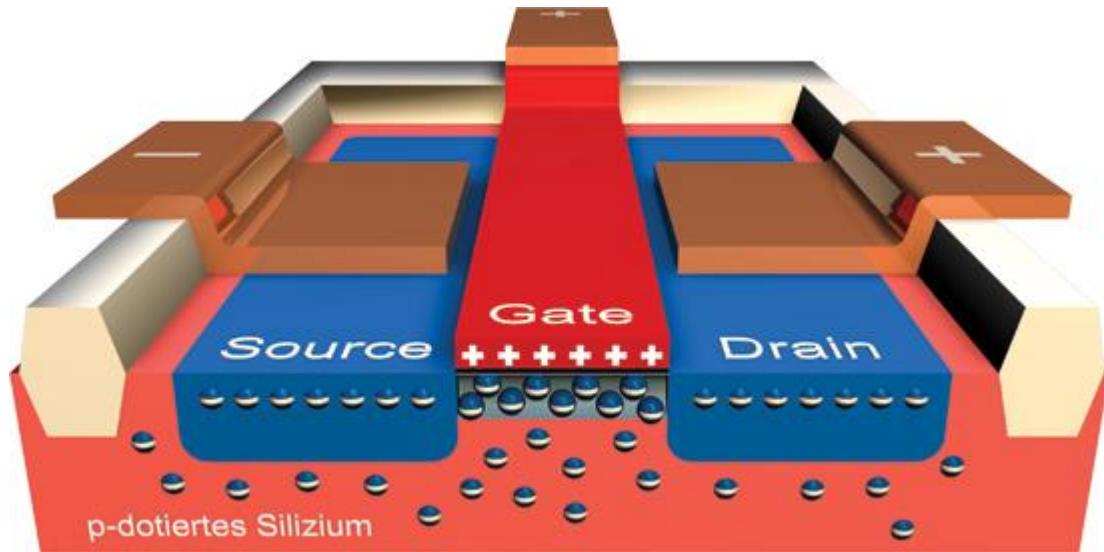
PXD mockup

# CMOS

- The CMOS stays for the complementary metal oxide semiconductor transistor
- A type of field effect transistor.
- Idea since 1925 by Julius Edgar Lilienfeld - change of the conduction in presence of E-field
- First MOSFET was realized in 1959 Dawon Kahng and Martin M. Atalla.



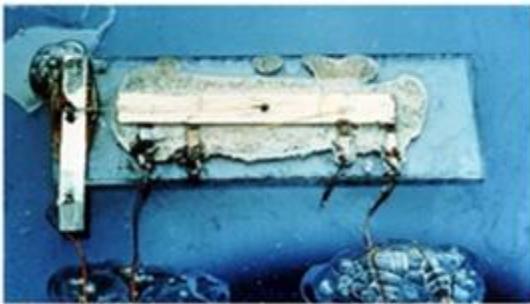
First MOSFET



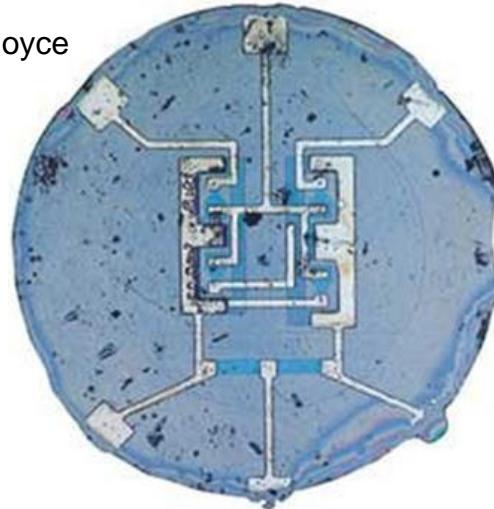
# MOS technology

- With development of ICs the MOSFET took the main role in electronics
- We are already producing  $10^{18}$  transistors per year - enough to supply every ant on the planet with ten transistors.
- Twenty years from now, if the trend continues, there will be more transistors than there will be cells in the total number of human bodies on Earth

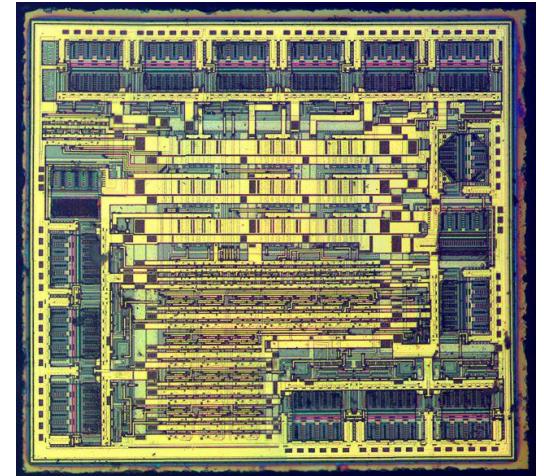
First IC - Kilby



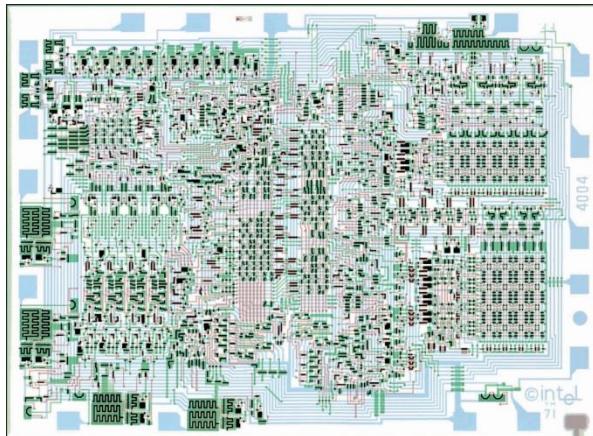
Planar IC Noyce



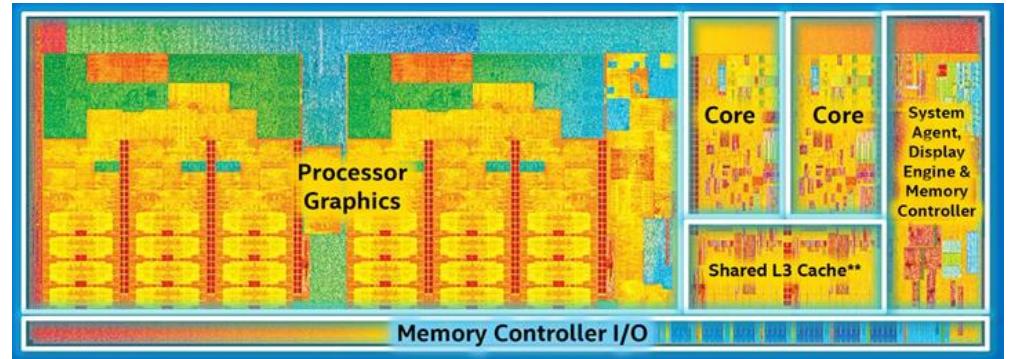
CMOS IC



First microprocessor

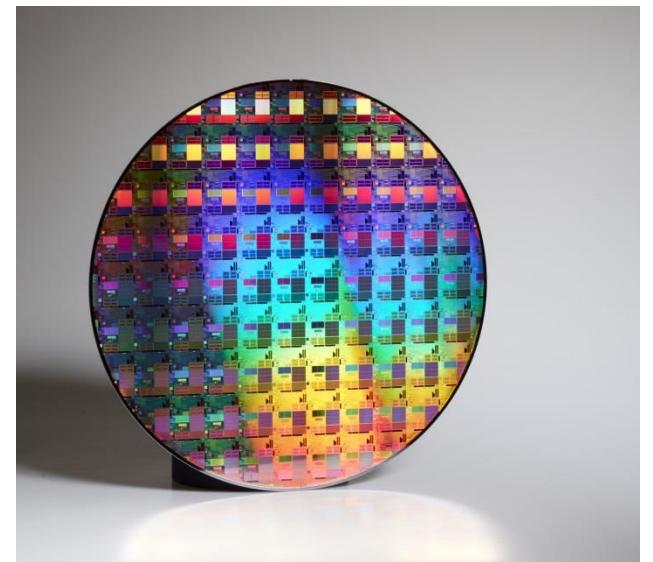


Modern intel processor



# CMOS Sensors

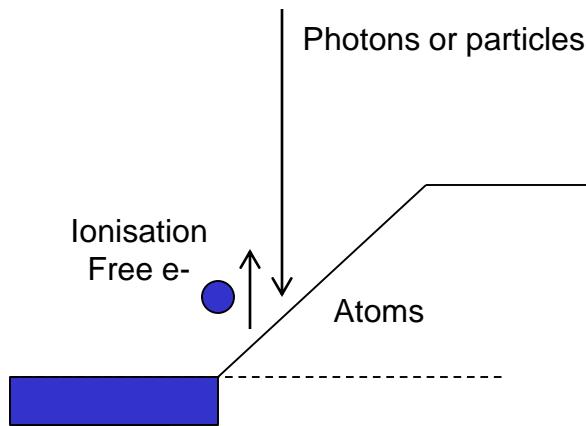
- Principle of CMOS sensors (Eric R. Fossum et all. IEEE transactions on electron devices. vol. 41, no. 3, march 1994)
- Sensor element - a pn junction
- N-region (called n-well or n-diffusion) in a p-substrate
- Potential well for electrons
- In some implementation n-region is entirely depleted -pinned photodiode



Samsung 32nm process

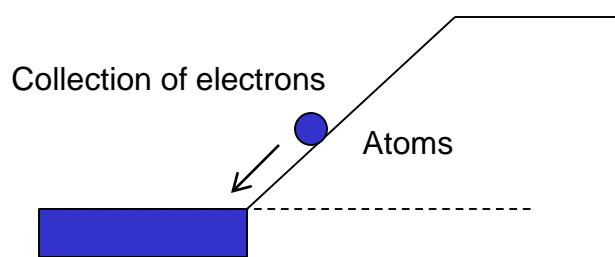
# PN junction as sensor of radiation

- The pn-junction is reversely biased - depleted region, potential change, here depicted as the slope
- 1. step - ionization



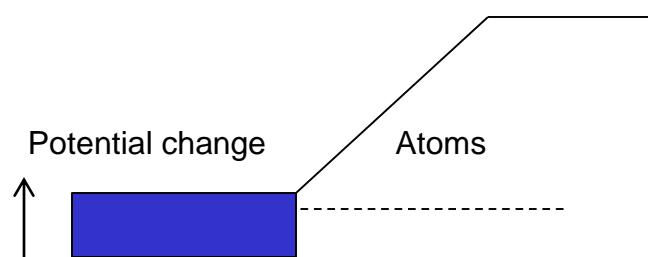
# PN junction as sensor of radiation

- 2. step – charge collection
- Two possibilities for charge collection – drift (through E-force) and by diffusion (density gradient)



# PN junction as sensor of radiation

- 3. step – charge to voltage conversion
- Collection of the charge signal leads to the potential change

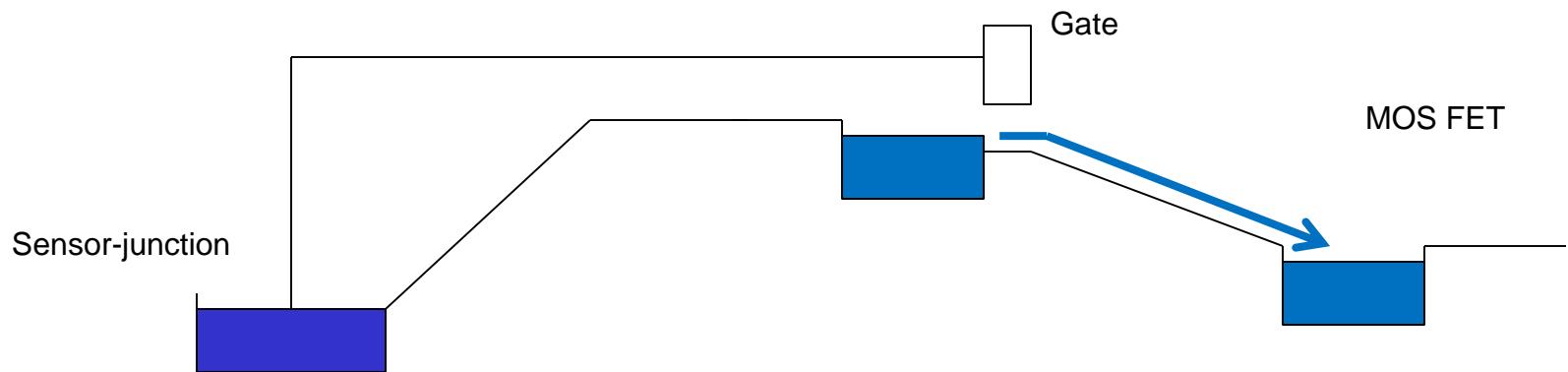
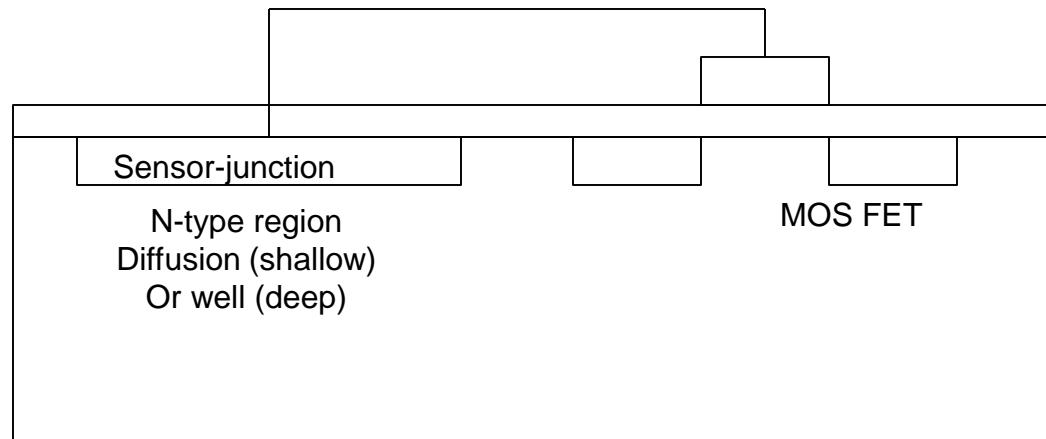


# MOS technology

- CMOS imaging sensors ,or CMOS pixel sensors, almost always contain at least one transistor inside a pixel. This transistor is acting as an amplifier

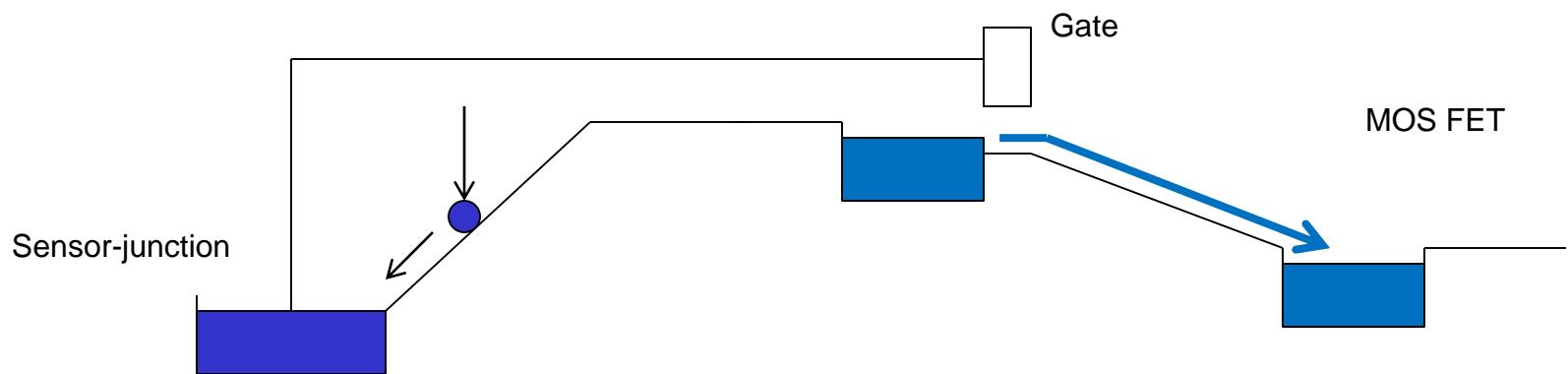
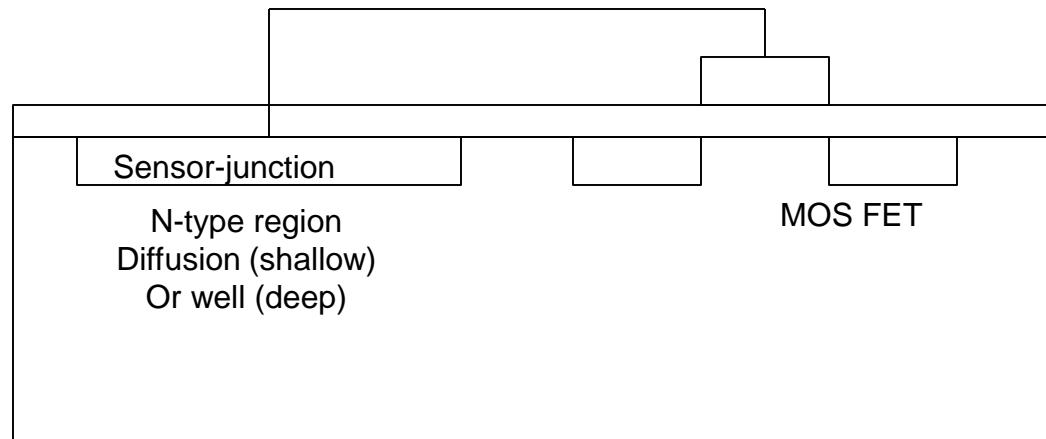
# CMOS pixel

- Connection between the n-region (charge collecting electrode) and the gate of the transistor



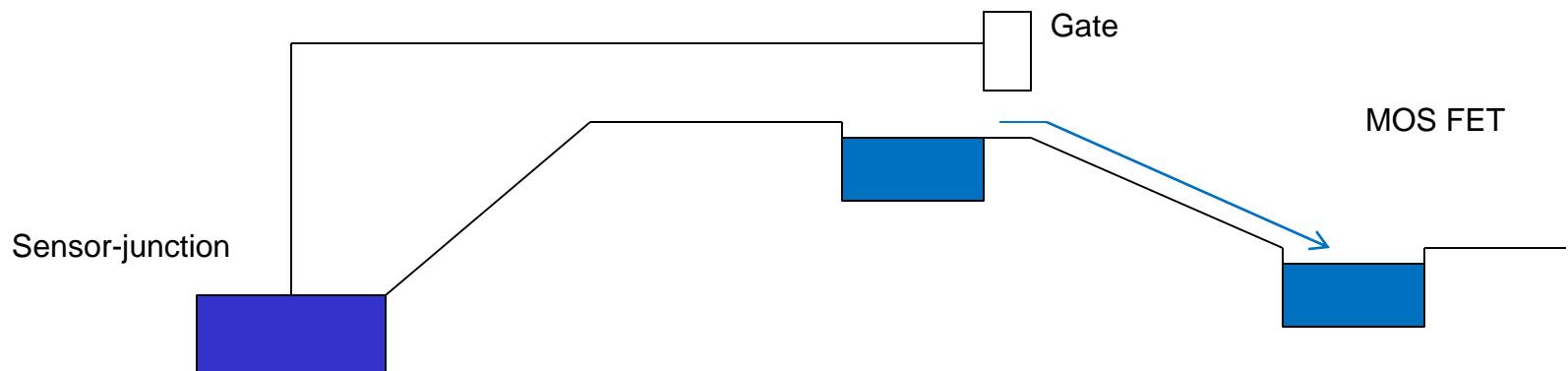
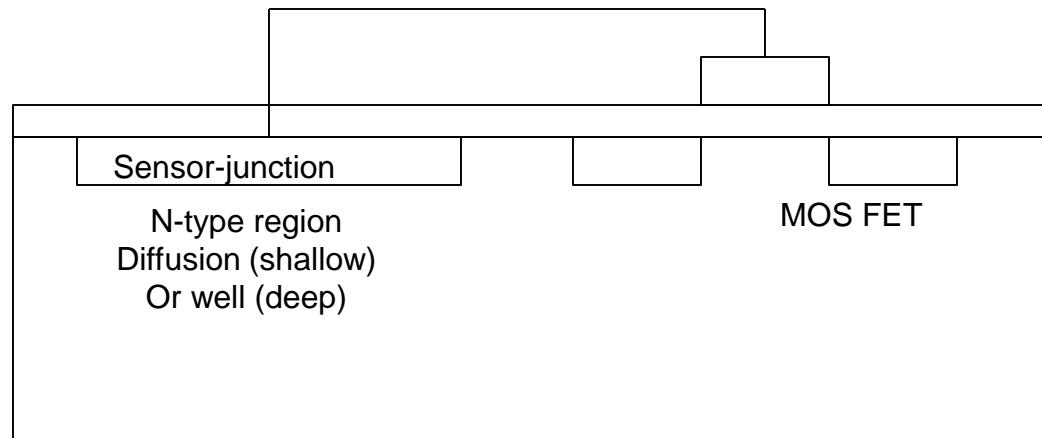
# CMOS pixel

- N in P diode acts as sensor element – signal collection electrode



# CMOS pixel

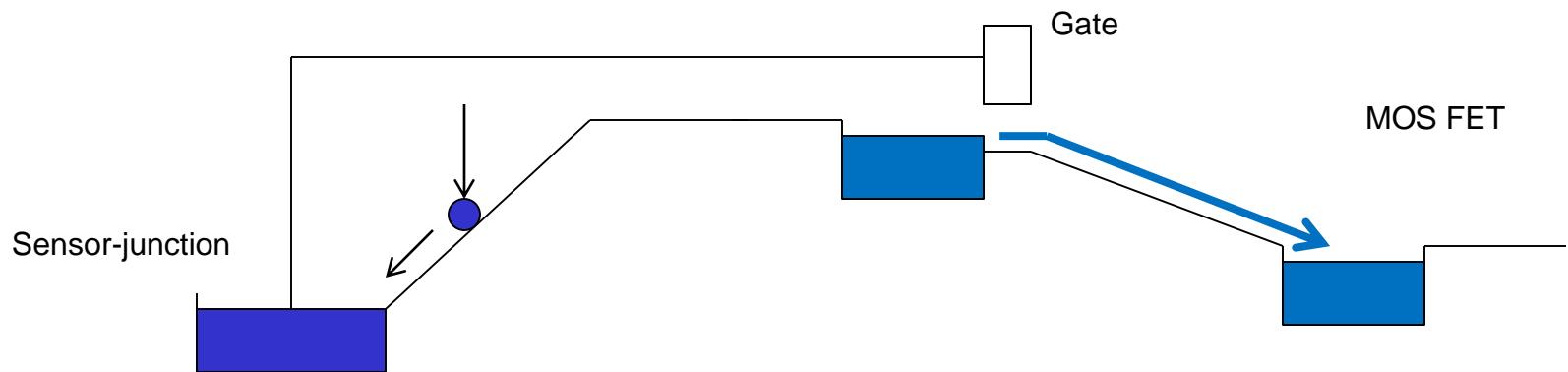
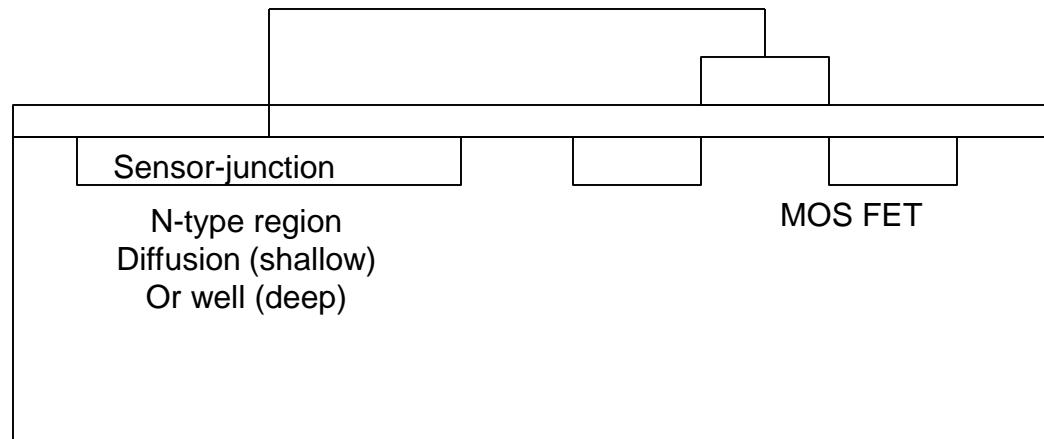
- Charge generated by ionization is collected by the N-diffusion
- This leads to the potential change of the N-diffusion
- The potential change is transferred to transistor gate – it modulates the transistor current
- A small charge generated by particles or photons produces much larger current flow or current change



# Drift and Diffusion

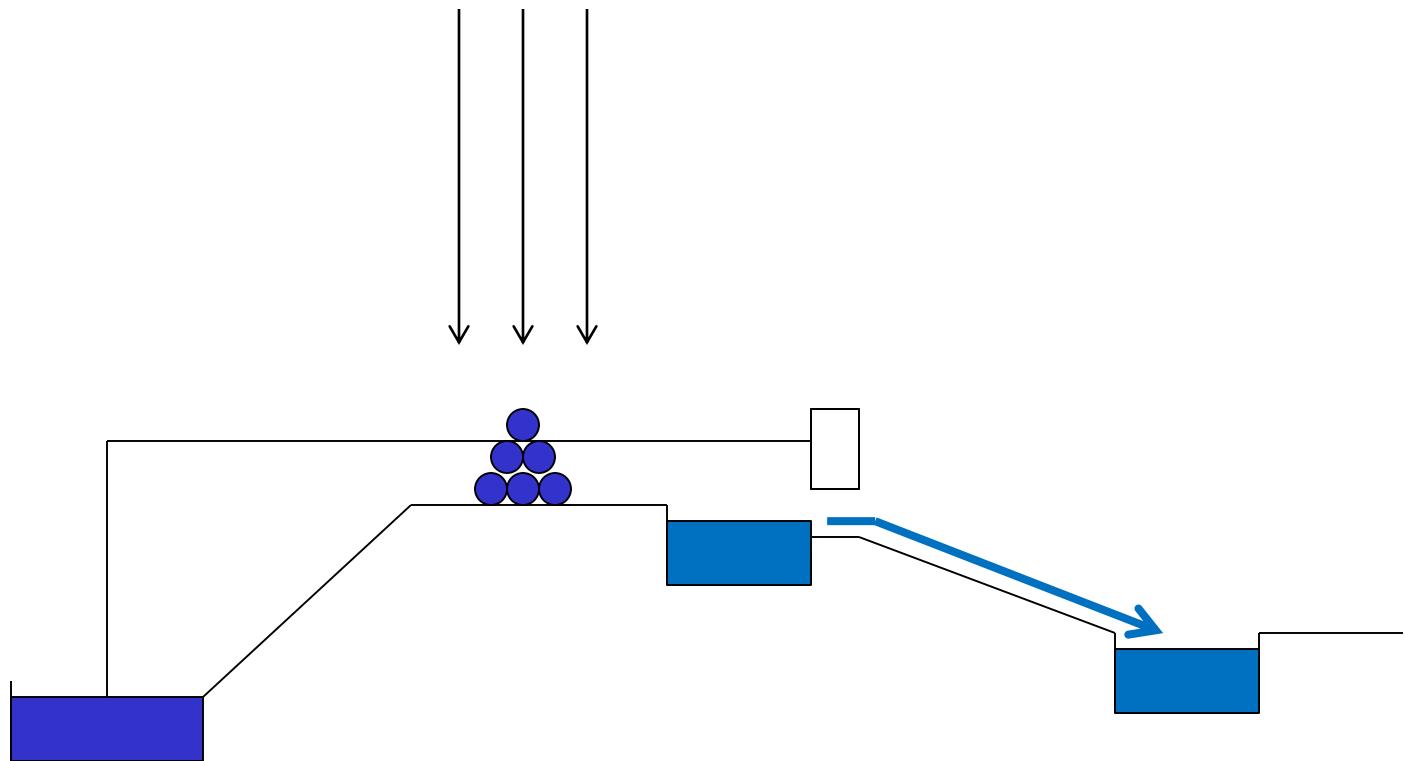
# CMOS pixel

- Charge generated in depletion region
- Charges experience high field and holes are separated from electrons. Electrons move by drift and are collected by the n-region



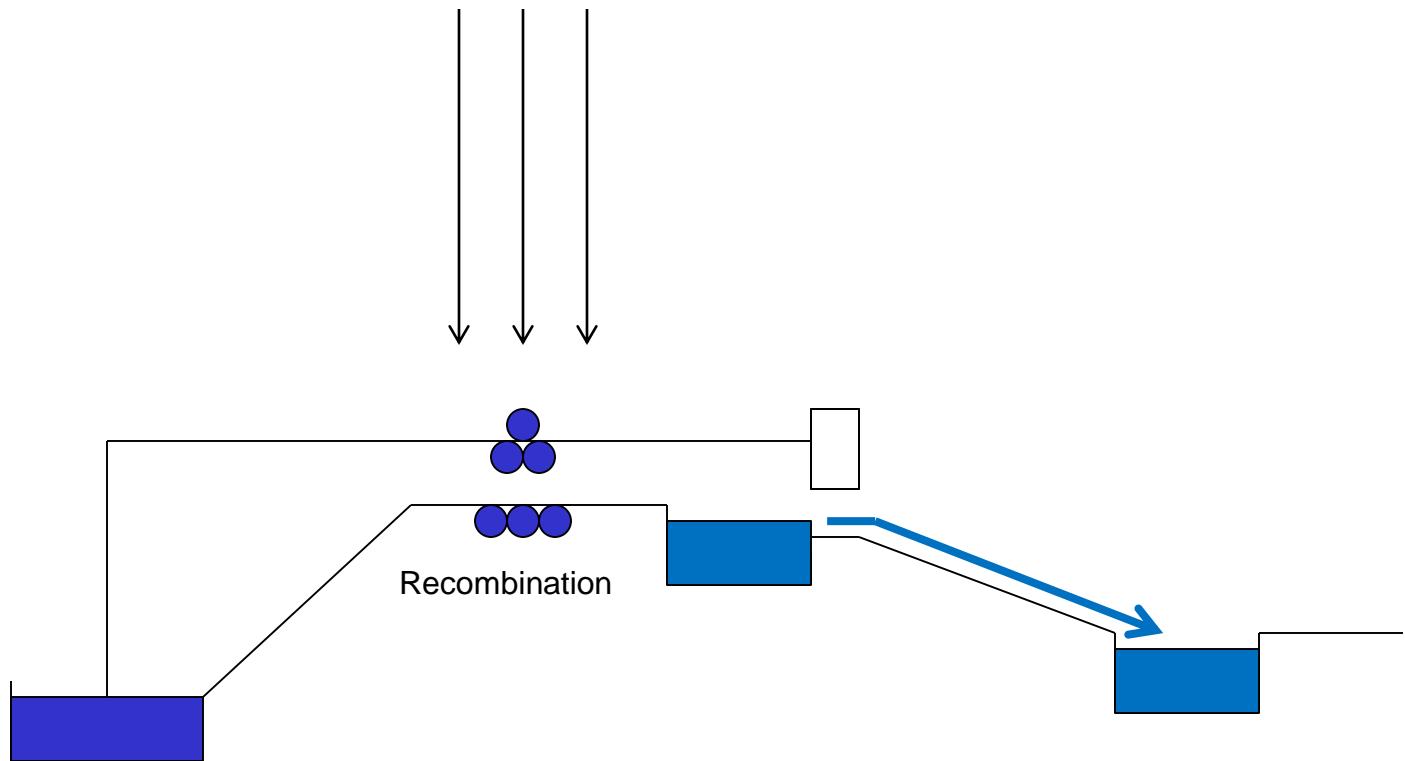
# CMOS pixel

- Partial signal collection in the regions without E-field



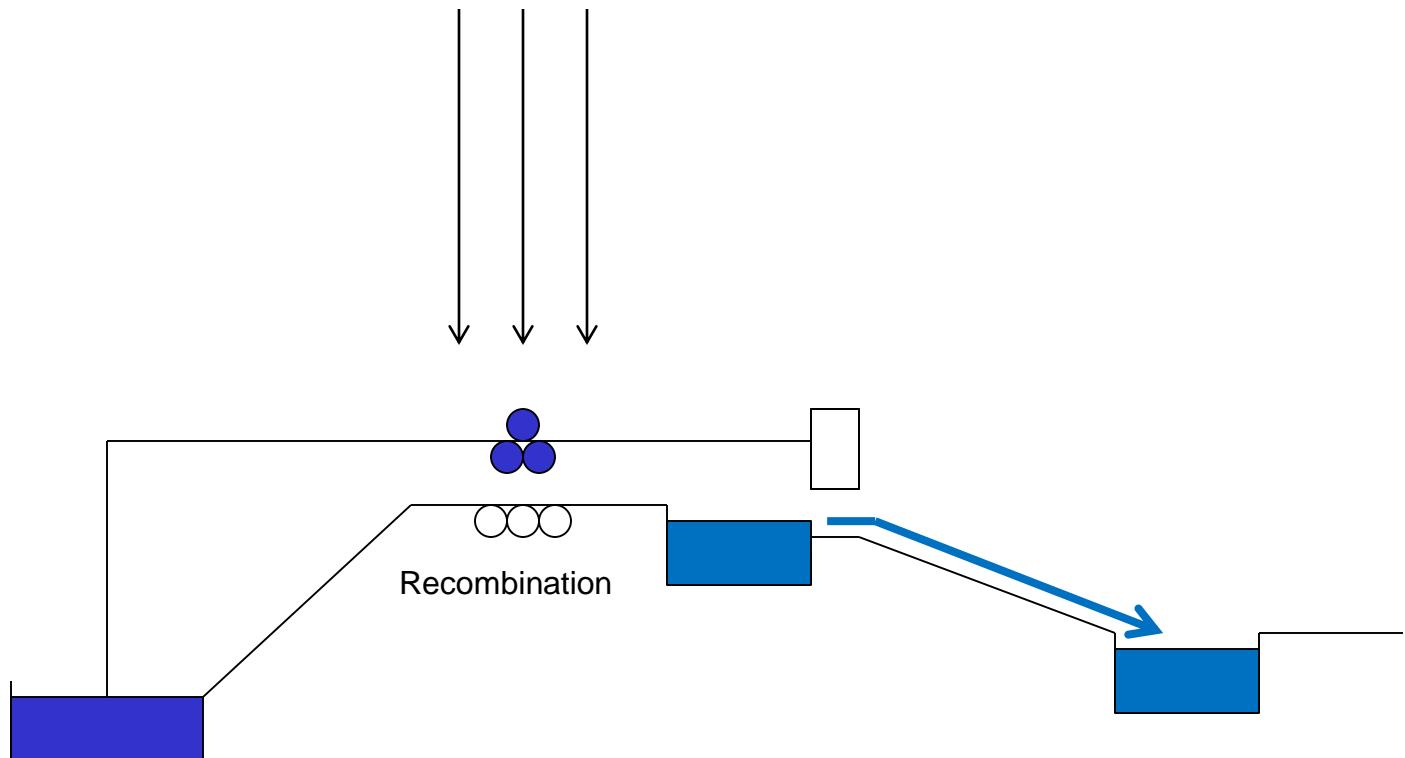
# CMOS pixel

- Partial signal collection in the regions without E-field



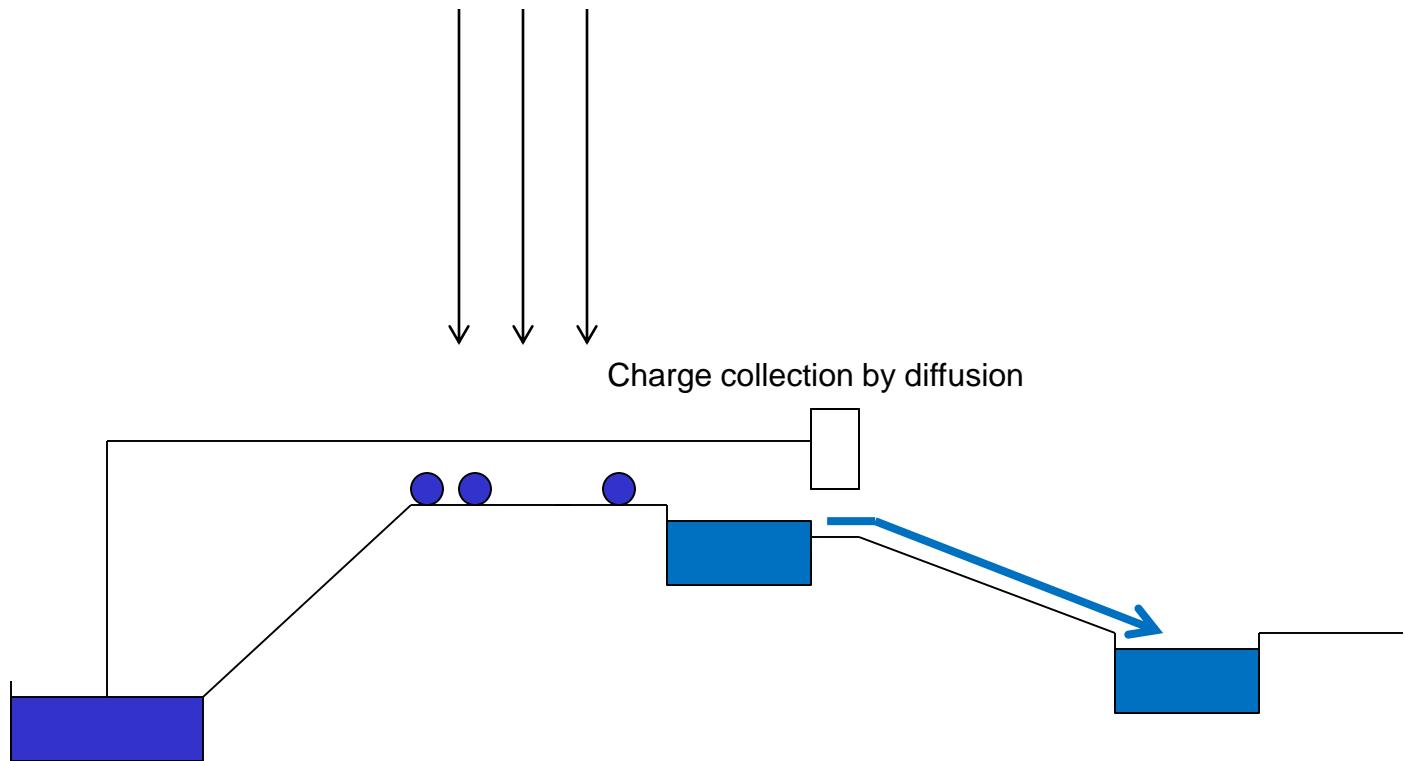
# CMOS pixel

- Partial signal collection in the regions without E-field



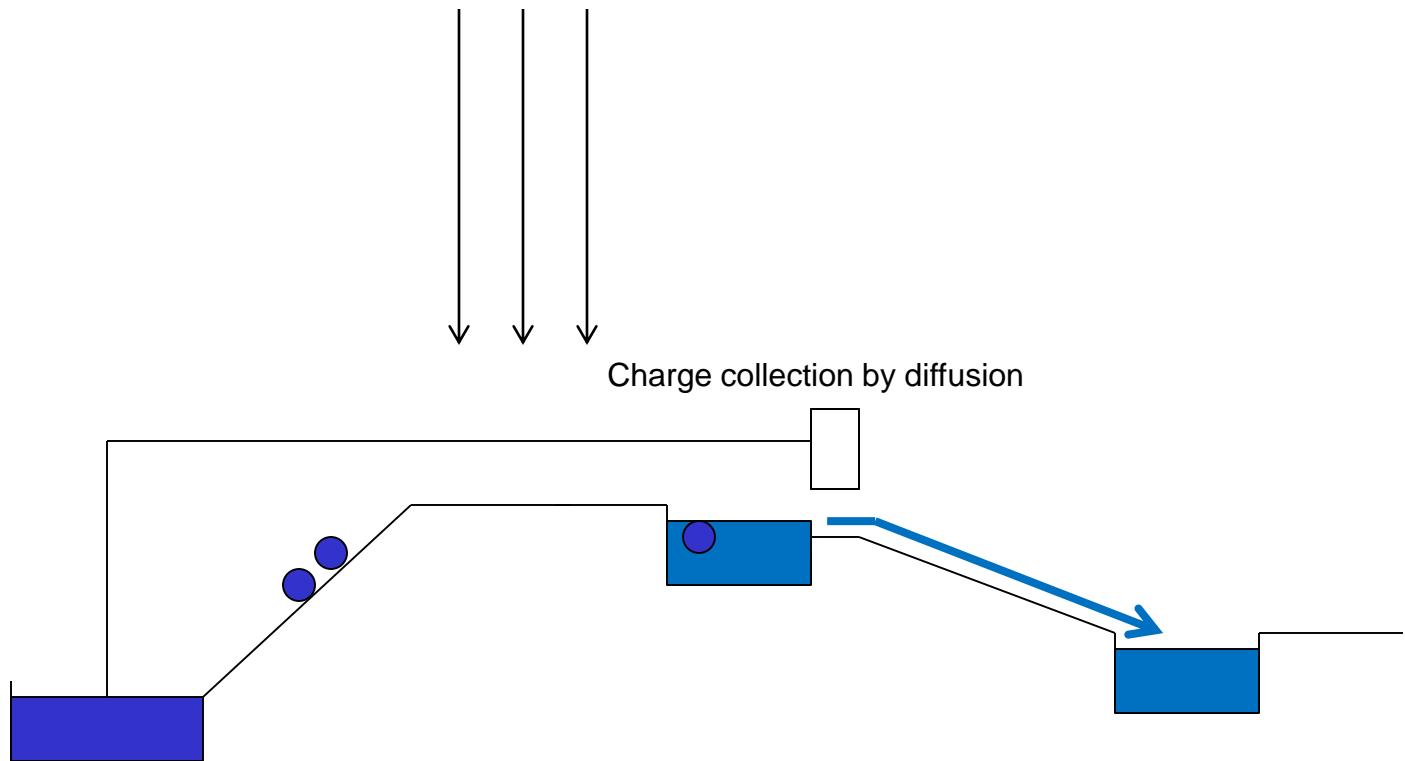
# CMOS pixel

- Partial signal collection in the regions without E-field

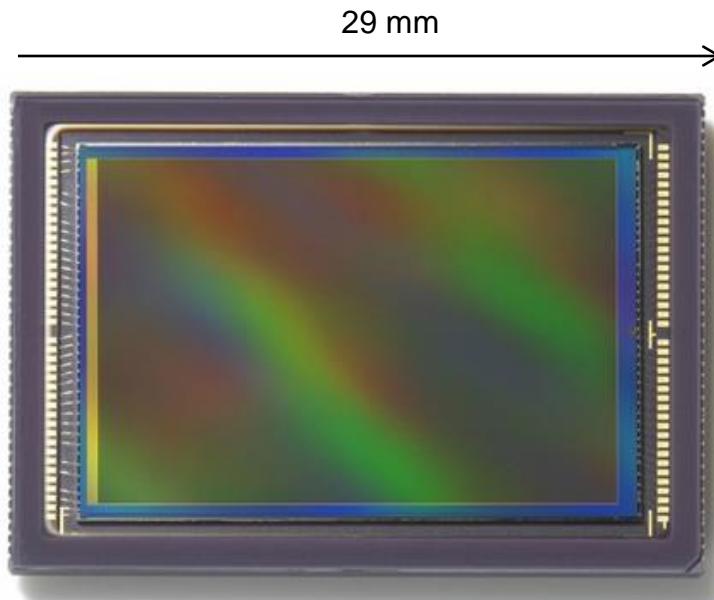


# CMOS pixel

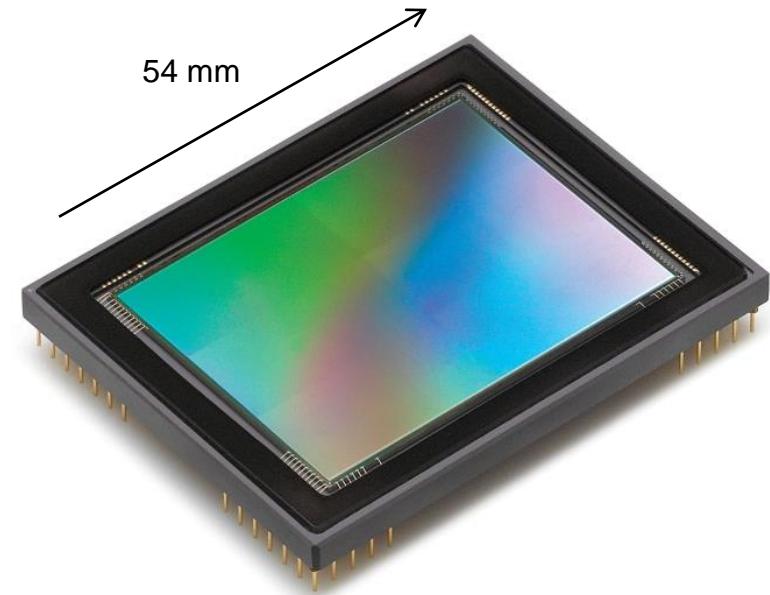
- Partial signal collection in the regions without E-field



- Differences versus the CCDs:
- In CMOS, there is a charge to voltage conversion in every pixel. This conversion occurs at the collection electrode
- Important parameter: the capacitance of the collection electrode (detector capacitance)
- Active element (amplifier) in every pixel
- The output signal of the CMOS pixel is already amplified. CCD pixel output -> original signal
- CMOS signal is stronger, but
- Output signal may be distorted by imperfect charge to voltage conversion and amplification.
- Noise in time and space (mismatch or FPN)
- Nonlinearity



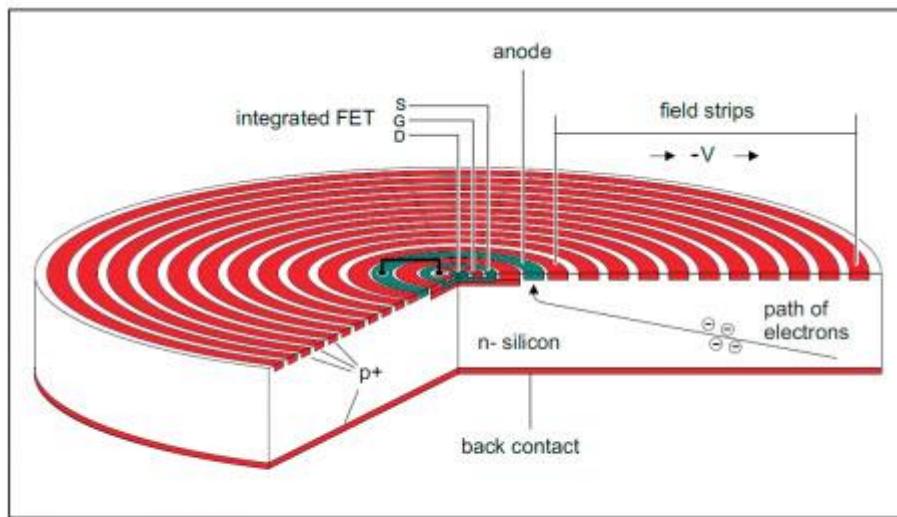
Canon 120 M pixels, 2um pixel size



Teledyne DALSA 60 M pixels CCD, 6um pixel size

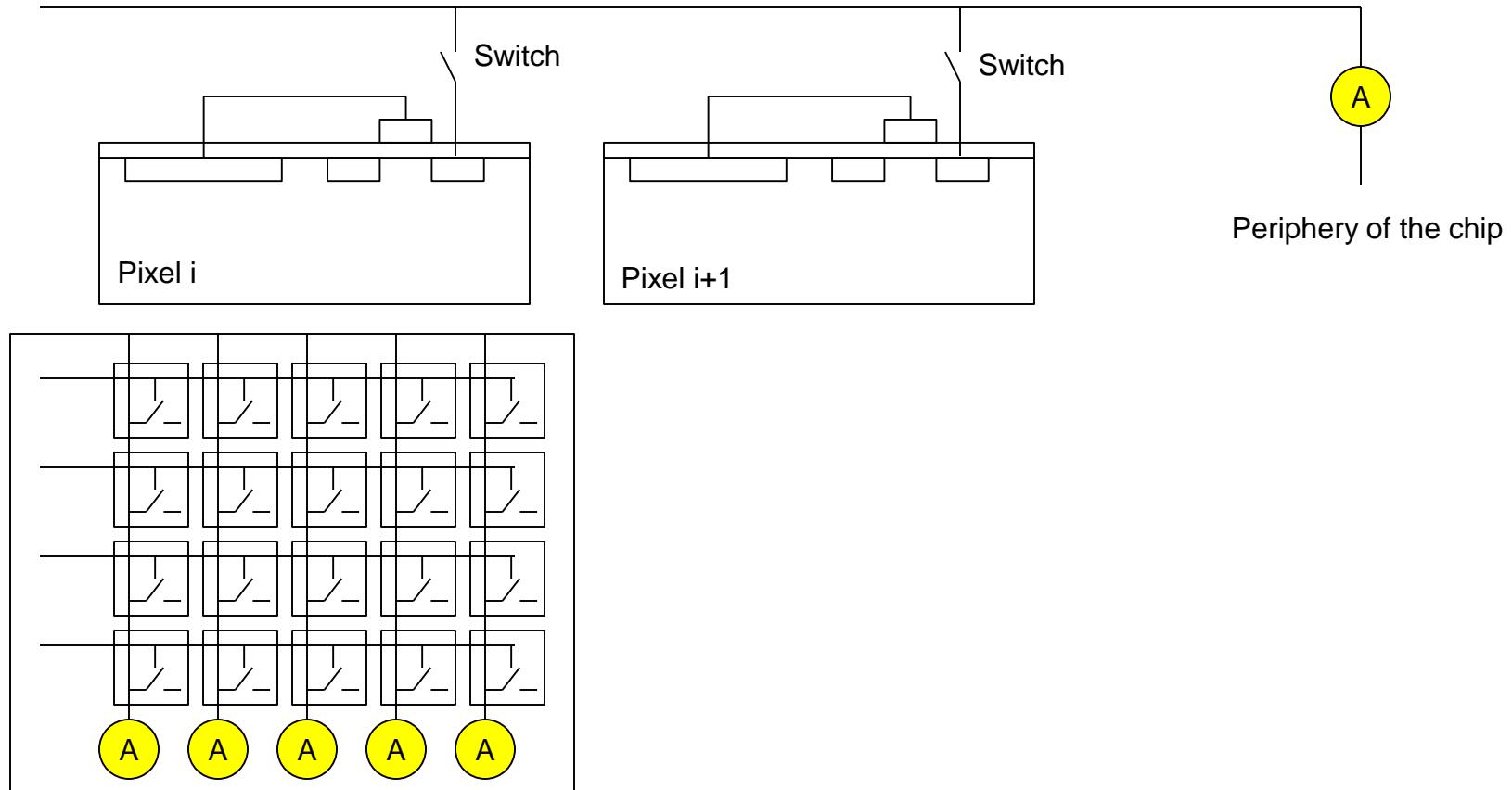
# MOS technology

- If the detector capacitance is smaller, the gain of the pixels is bigger and the sensor SNR is better

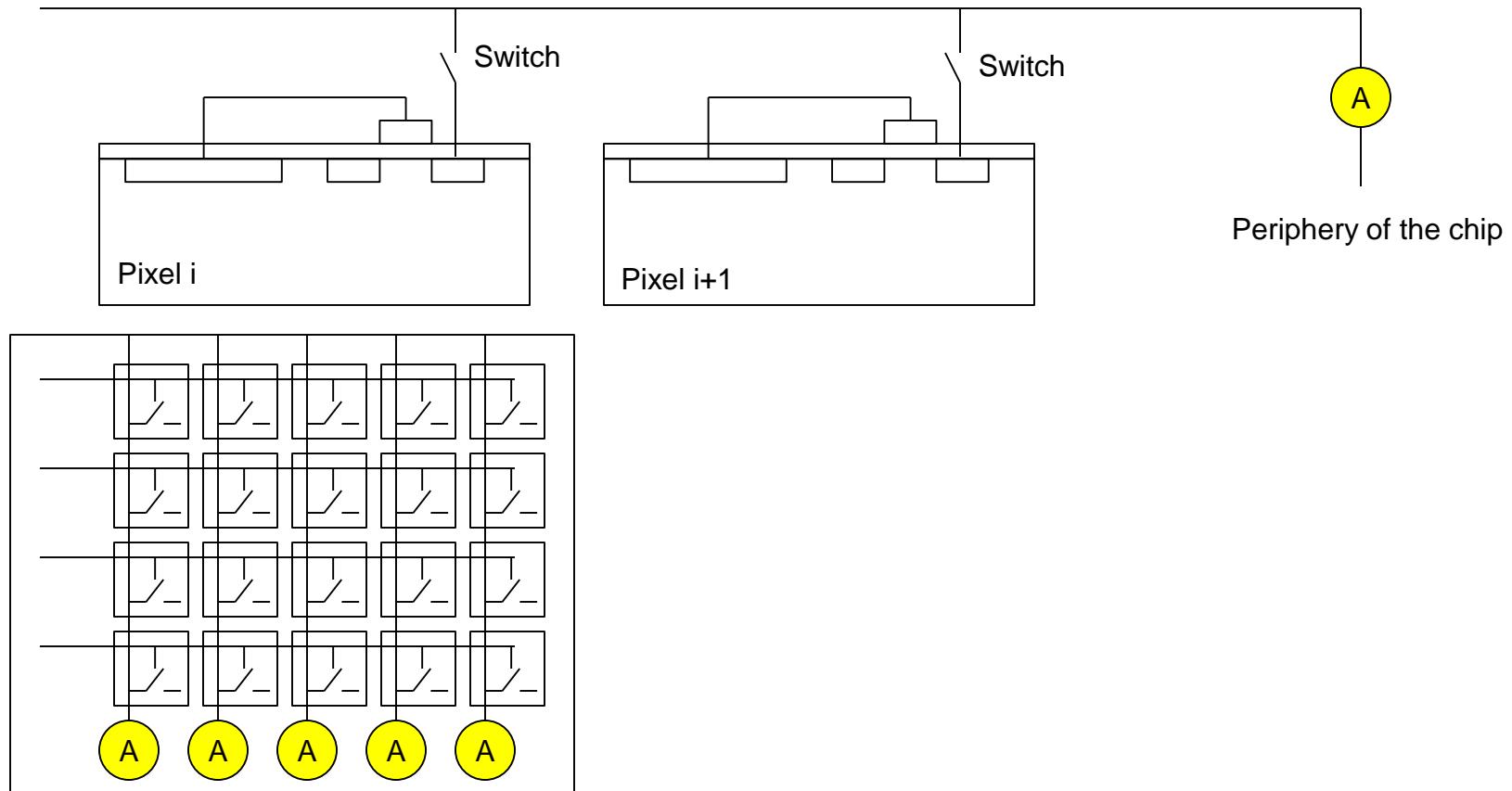


Example SDD detector design

- Differences between CMOS imaging sensors and CMOS particle sensors
- CMOS imaging sensors are now the mostly used sensor type for digital cameras
- Rolling shutter principle

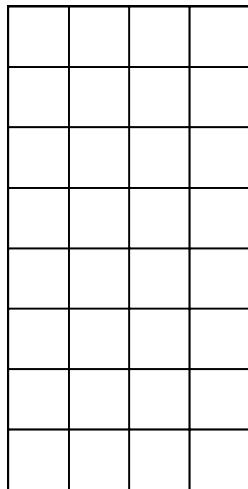
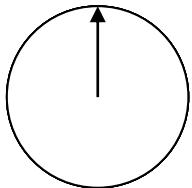


- Pixels of the same column share the same column line.
- The gates of the switches are connected row-wise
- For the readout of whole matrix we need  $n$  steps, where  $n$  is the number of rows.
- Proper concept for imaging



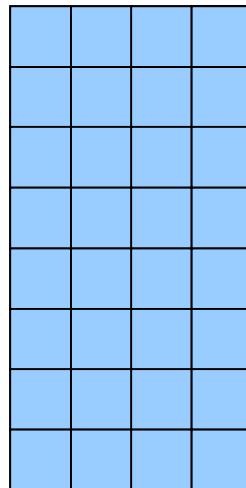
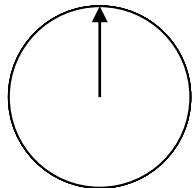
# CMOS Sensors for Particle Physics

- Rolling shutter is not always the optimal readout concept for particle physics, although there are many CMOS particle sensors that work in this way



- Simple pixels
  - Signal and leakage current is collected
  - No time information is attached to hits
  - The whole frames are readout
- ☺ Small pixels
- ☺ Low power consumption
- ☺ Slow readout

- Particle tracking: To measure the time and the position of particle hit. Particles produce enough charge and can be distinguished from the noise
- In the case of LHC experiments, the required time resolution is 25ns.



- Intelligent pixels
- FPN is tuned inside pixels
- Leakage current is compensated
- Hit detection on pixel level
- Time information is attached to hits
- ⌚ Larger pixels
- ⌚ Larger power consumption
- ⌚ Fast (trigger based) readout

- Imaging sensors: efficiency 80% ok
- Particle sensors: efficiency >99% required

- Solution - smart pixels
- Output is the time information of the particle hit
- Output of the CCD-pixel - collected charge
- Output of CMOS imaging sensor pixel - amplified charge signal
- Output of CMOS particle sensor pixel (a smart pixel) - time information of (the triggered) hit

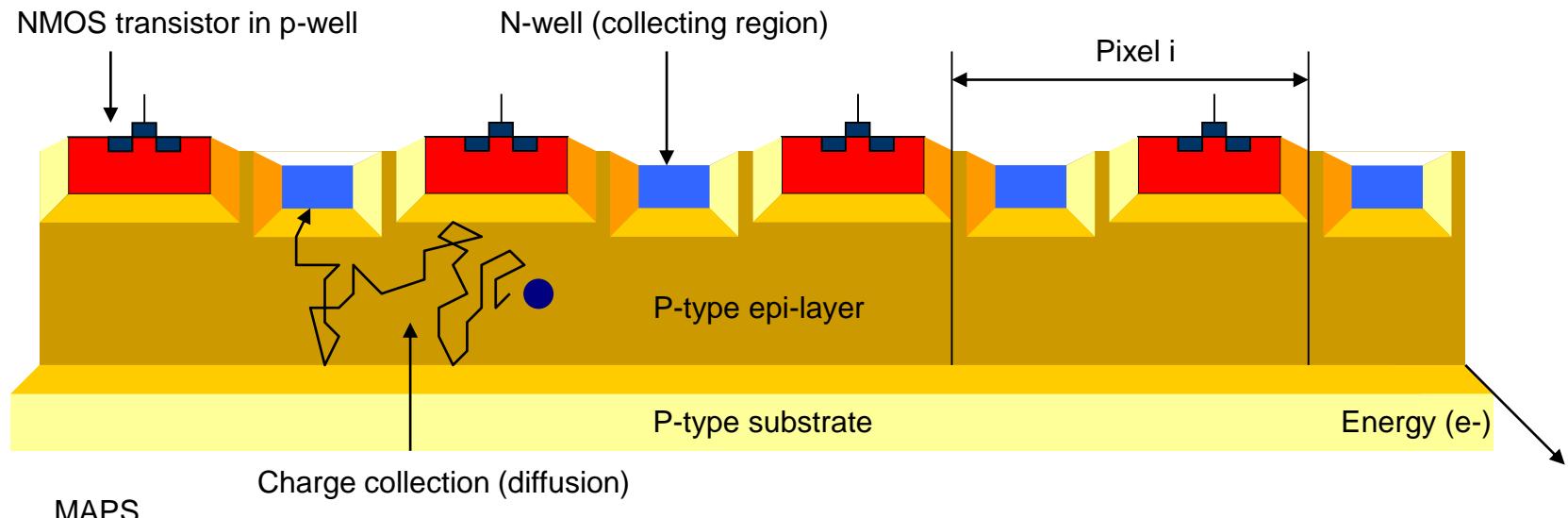
- A complex signal processing requires many (>2,3) transistors
- Both CMOS transistor types – n-channel and p-channel are required
- Complication:
- PMOS is placed in a local n-substrate (n-well). N-well is placed in the p-substrate. The same p-substrate is used as sensor volume
- N-well and the collecting electrode are competing → charge loss

# CMOS Sensors Types

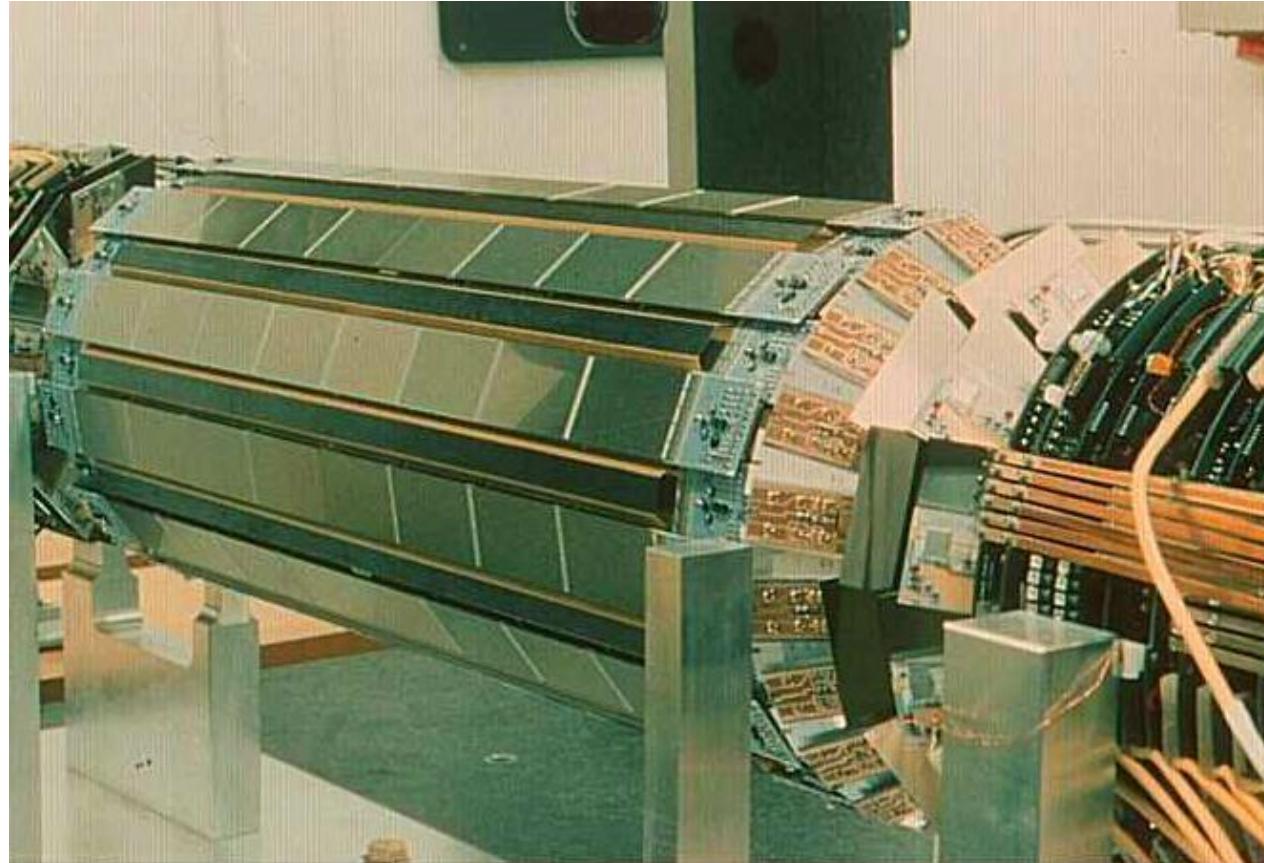
# MAPS

# MOS pixel sensor with 100% fill factor - MAPS

- The collection electrode is near the electronics.
- The charge collection is by diffusion.
- Standard process.
- Disadvantage: introduction of PMOS transistors lead to a charge loss
- Radiation tolerance
- Still, very successful



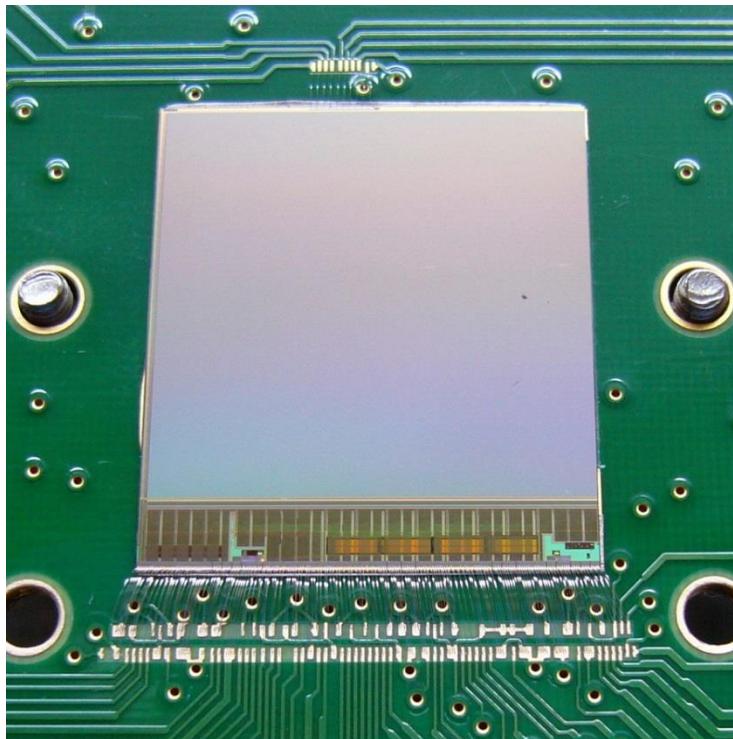
- IPHC Strasbourg (PICSEL group)
- Family of MIMOSA chips
- Applications:, STAR-detector (RHIC Brookhaven), Eudet beam-telescope



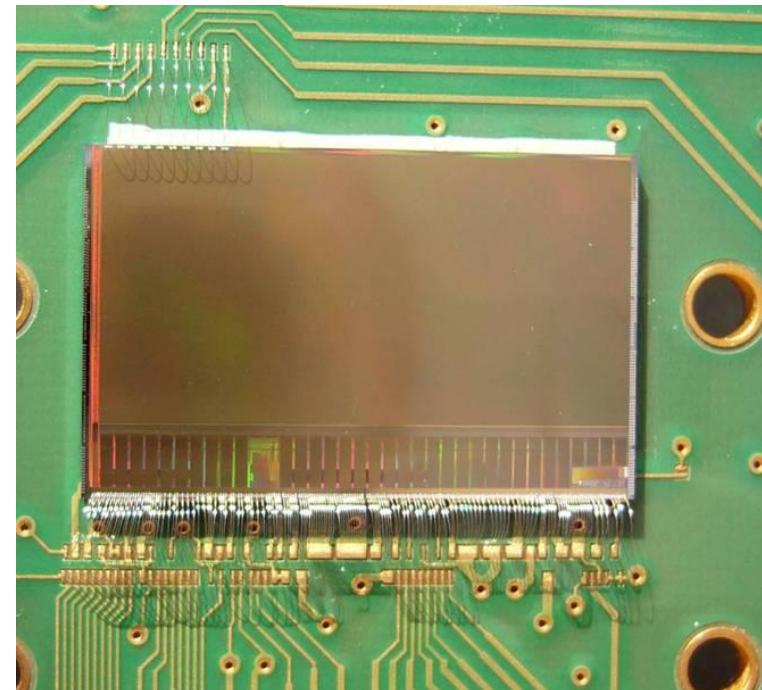
<http://www.iphc.cnrs.fr/Monolithic-Active-Pixel-Sensors.html>

# MAPS

- Although based on simple MAPS principle – epi layer and NMOS electronics – MIMOSA chips use more complex pixel electronics
- Continuous reset and double correlated sampling



Ultimate chip for STAR

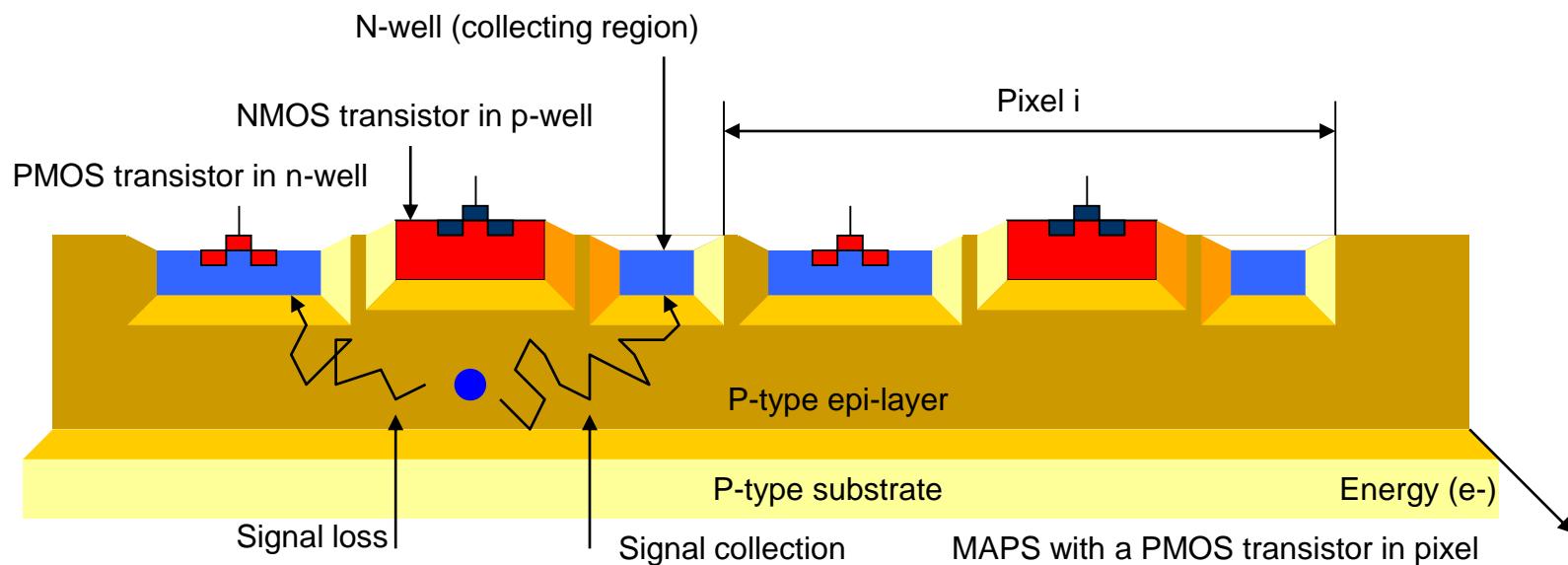


MIMOSA 26 for Eudet telescope

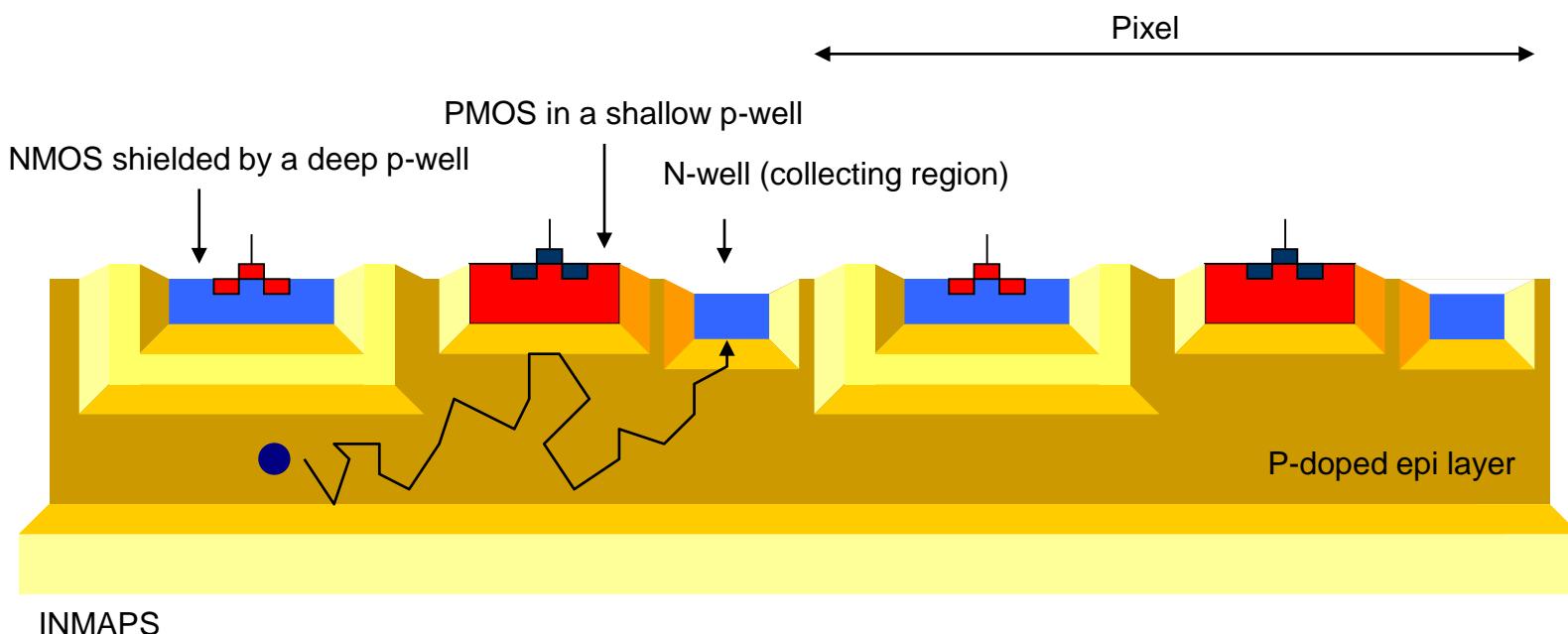
<http://www.iphc.cnrs.fr/Monolithic-Active-Pixel-Sensors.html>

# MAPS structure with CMOS pixel electronics

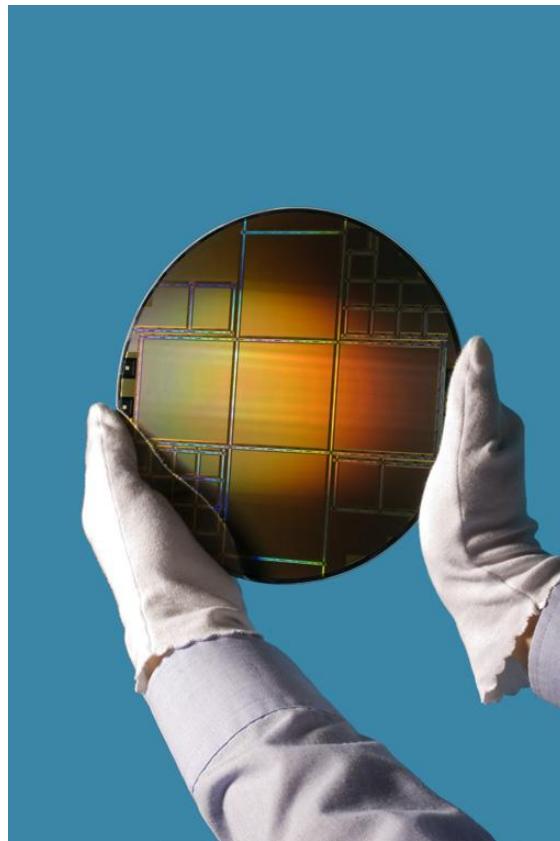
- If PMOS transistors are introduced, signal loss can happen



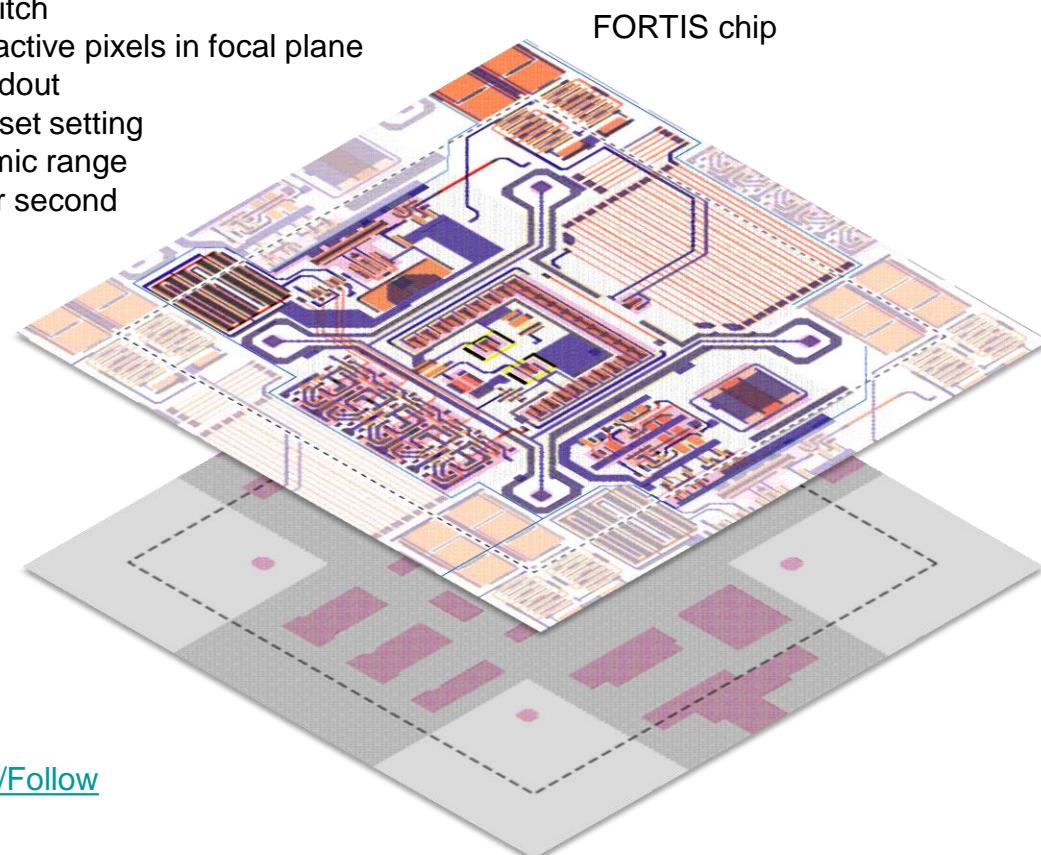
- Deep P-layer is introduced to shield the PMOS transistors from epi layer
- No charge loss occurs
- Not a CMOS standard process
- Disadvantages are slow charge collection by diffusion and less radiation tolerance. Another disadvantage is very limited number of producers and non-standard CMOS process



- INMAPS Tower Jazz process is gaining popularity in particle physics community
- It was originally developed by the foundry and the *Detector Systems Centre*, Rutherford Appleton Laboratory

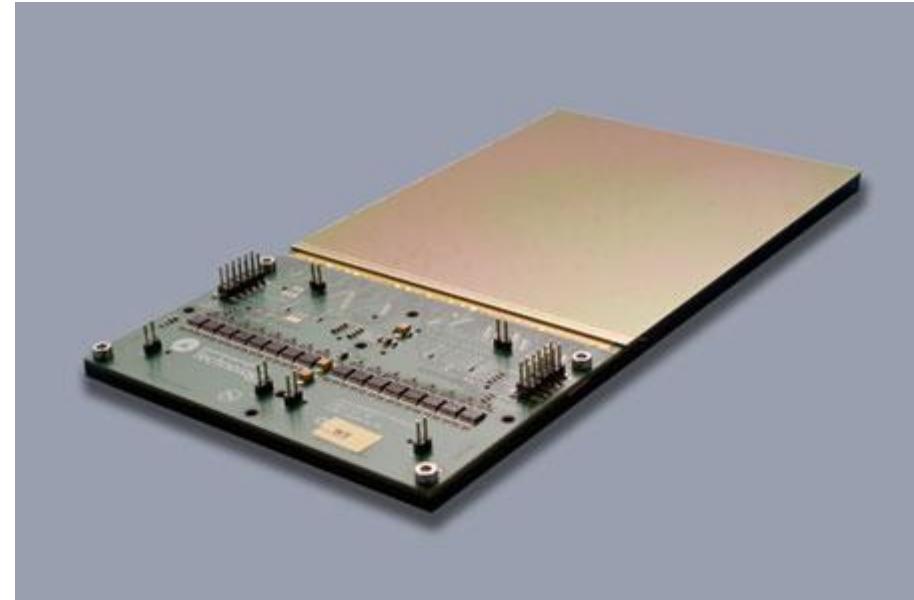
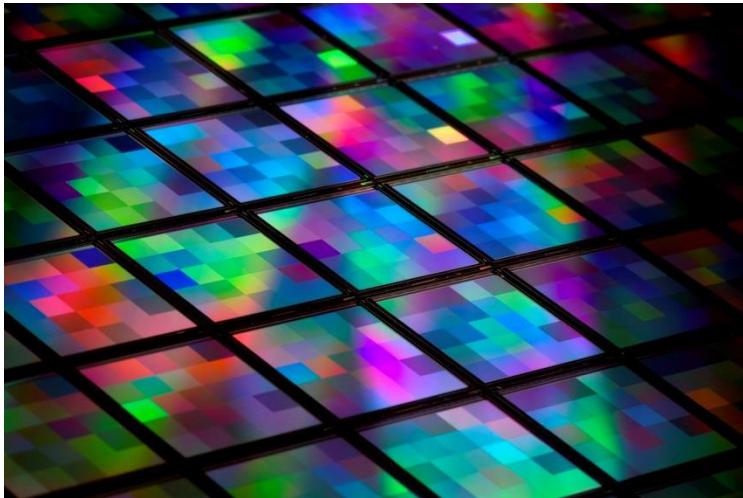


2 Megapixels, large area sensor  
Designed for high-dynamic range X-ray imaging  
40 µm pixel pitch  
1350 x 1350 active pixels in focal plane  
Analogue readout  
Region-of-Reset setting  
140 dB dynamic range  
20 frames per second



<http://dsc.stfc.ac.uk/Capabilities/CMOS+Sensors+Design/Follow+us/19816.aspx>

- Detector Systems Centre, Rutherford Appleton Laboratory – some examples



Wafer scale 120 x 145 mm chip for medical imaging

<http://dsc.stfc.ac.uk/Capabilities/CMOS+Sensors+Design/Follow+us/19816.aspx>

# Depleted CMOS

# Depleted INMAPS - HRCMOS

- In depleted sensors charge is collected by drift -> faster signals
- One of the first ideas is described in the PhD thesis of Walter Snydes: „A new integrated pixel detector for high energy physics“

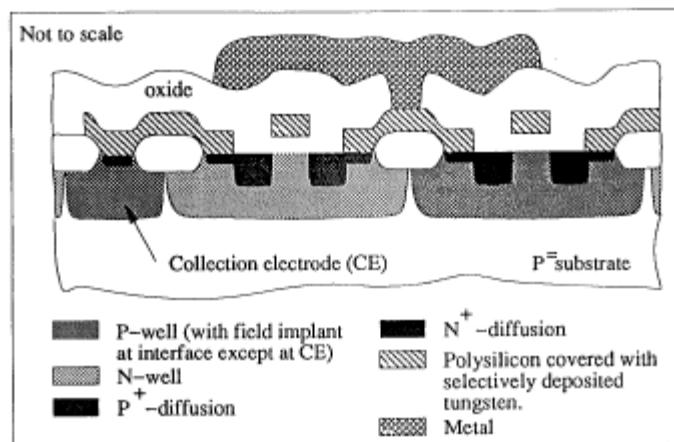


Figure 3.1. Schematic overview of the structures on the front side of the wafer after processing.

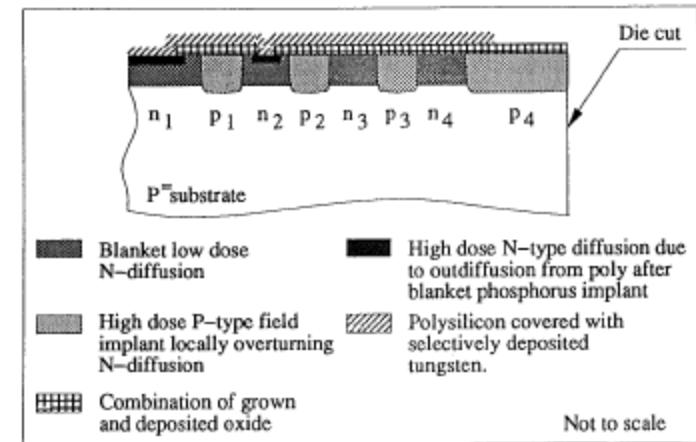
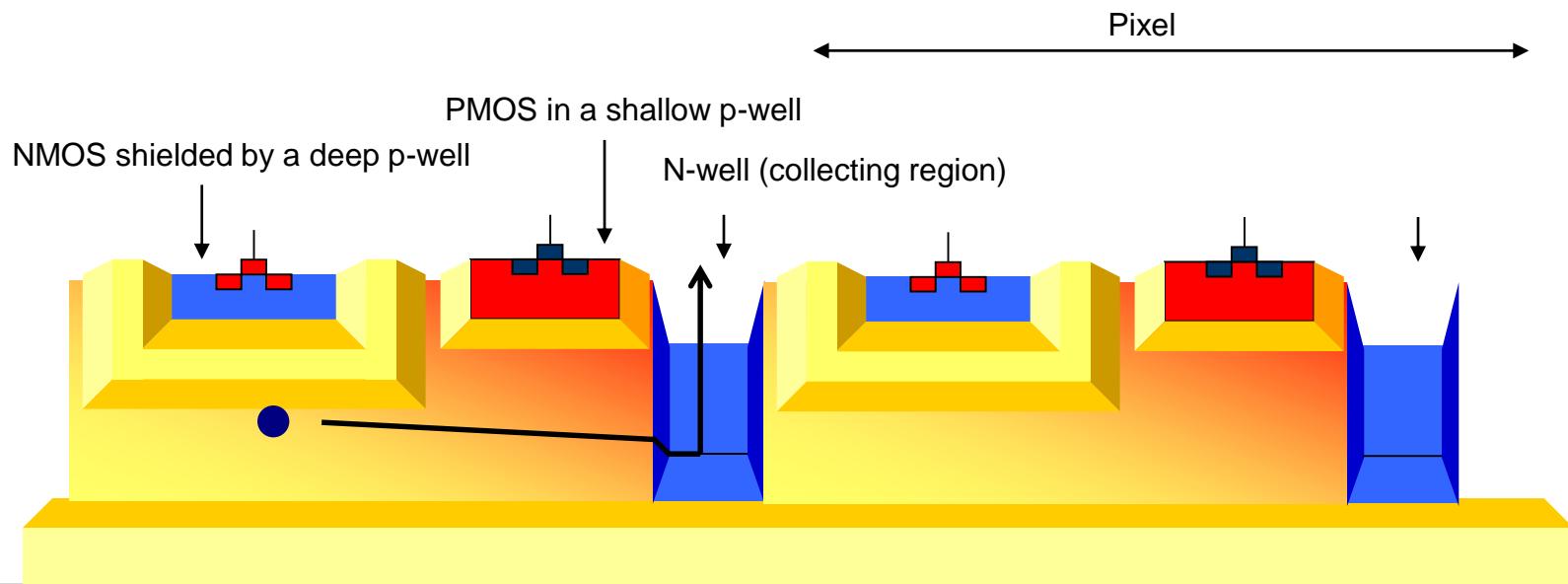


Figure 3.2. Schematic overview of the back side structure after processing.

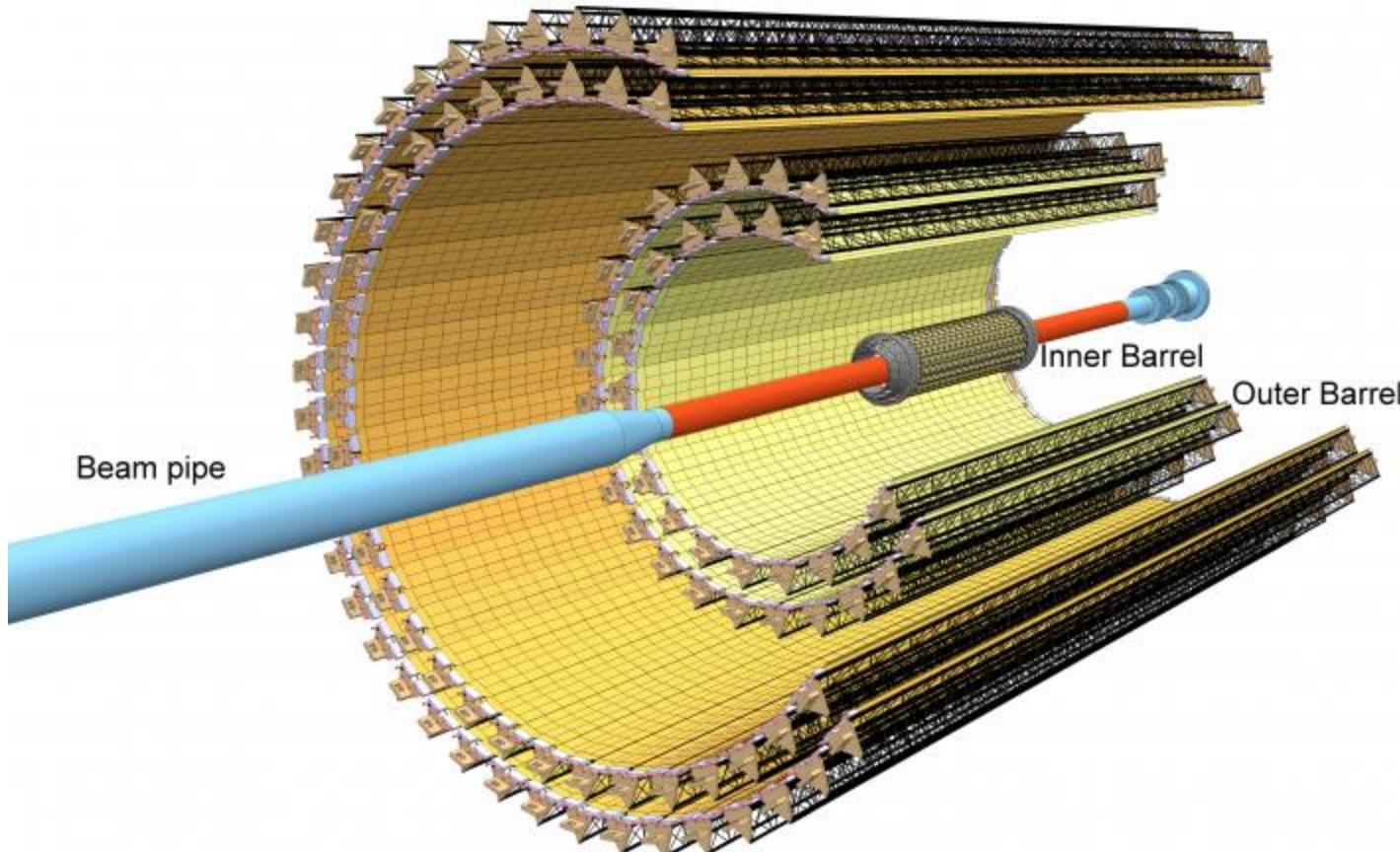
# Depleted INMAPS

- Improved version of INMAPS. Here a high voltage is used partially deplete the region underneath the electronics.
- Nonstandard CMOS



# Depleted INMAPS

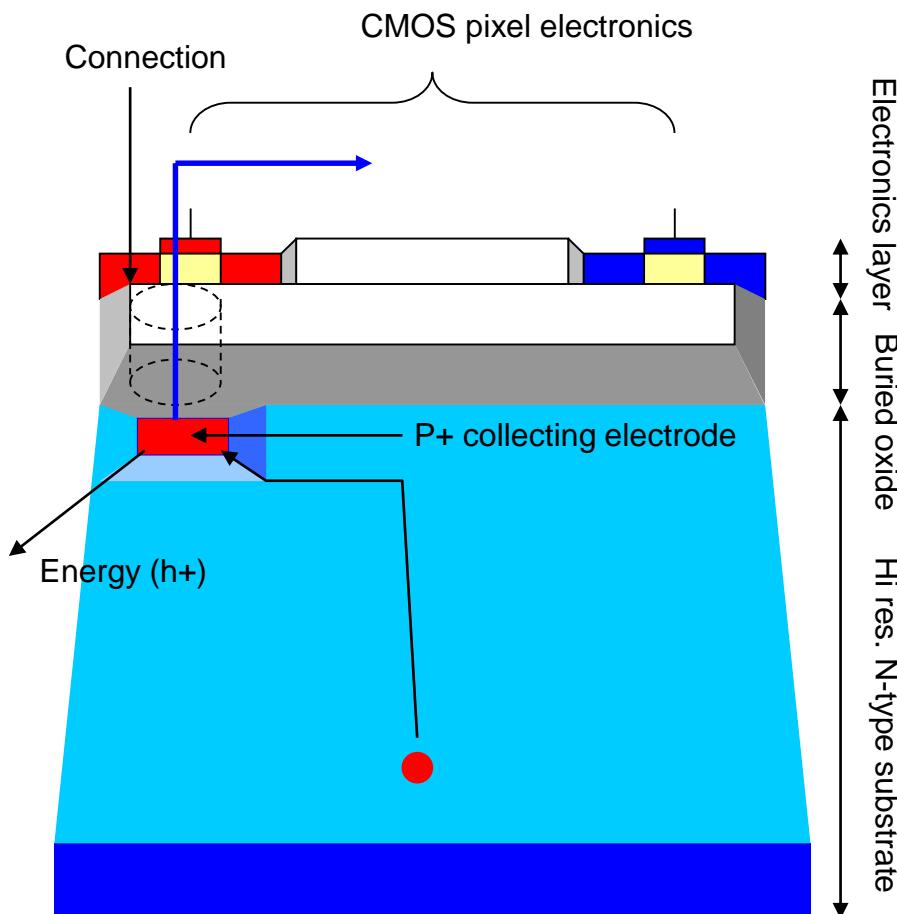
- Application: ALICE Upgrade



# SOI technology

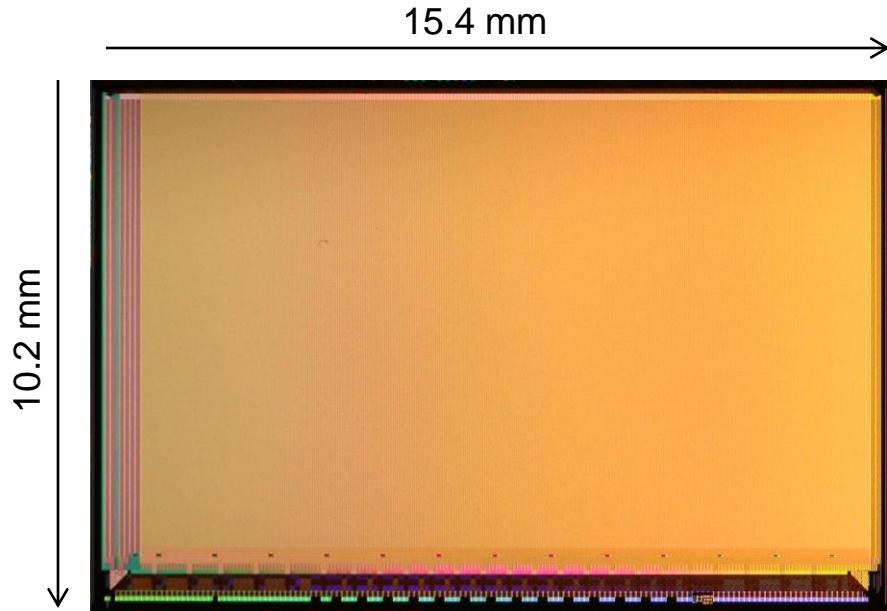
- Originally developed at University of Krakow
- The development continued in collaboration with industry (OKI and Lapis)
- The collaboration is now led by KEK, Japan

- Sensor part and the electronics are separated by oxide. The sensor has the form of a matrix of pn junctions, the collecting regions are p-type diffusion implants in the n-substrate. A connection through the buried oxide is made to connect the readout electronics with electrodes. SOI sensors can use CMOS, the charge collection is based on drift. The disadvantage is a complex process.

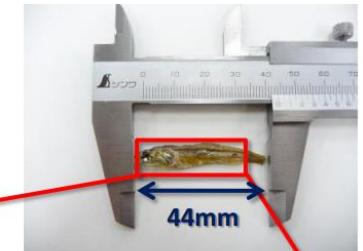
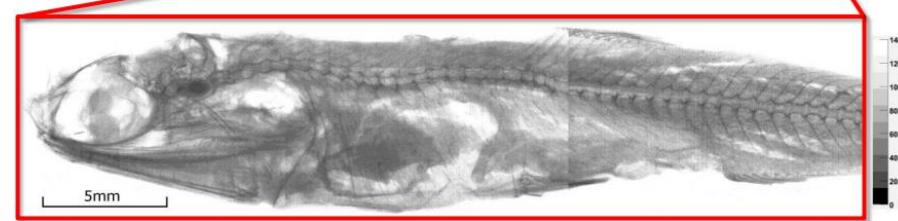


# SOI technology

- SOI technology can be used for x-ray detection thanks to its thick sensitive region
- Example of an x-ray detector: INTPIX4



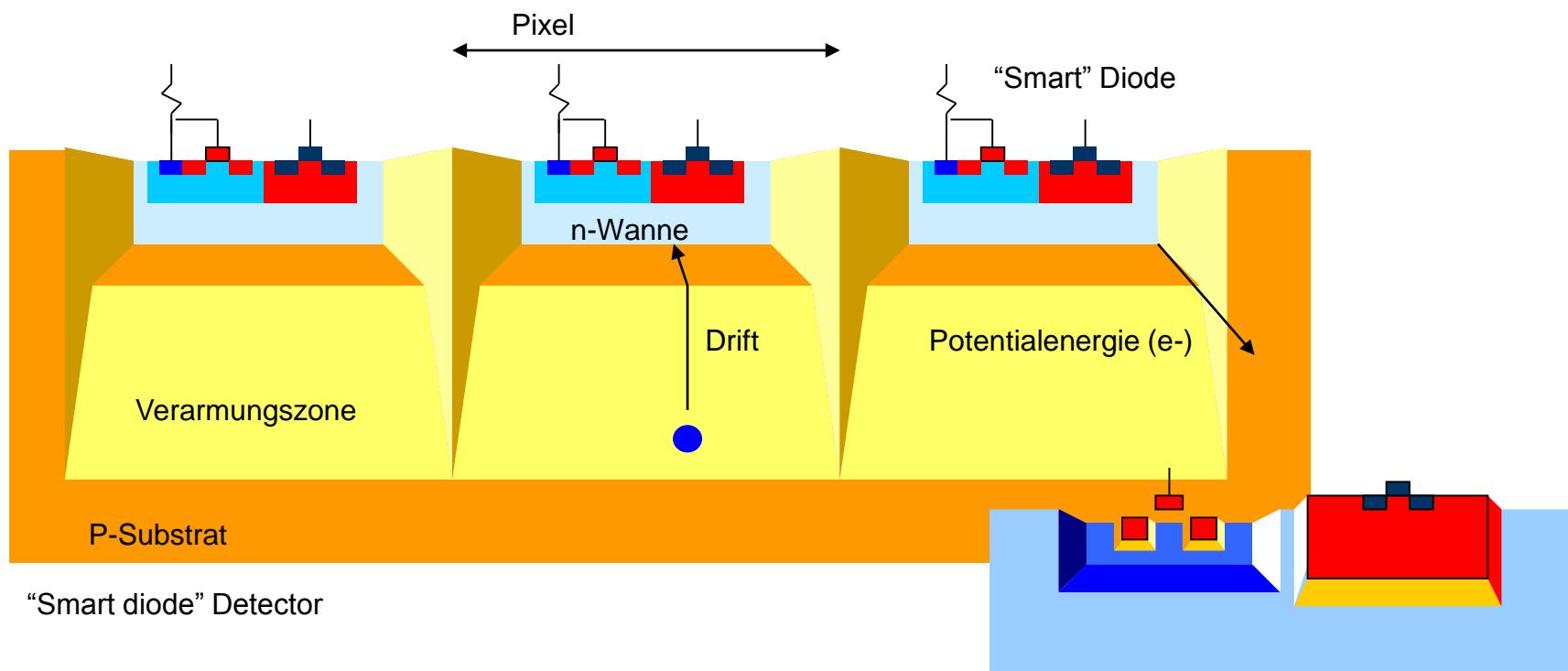
**250  $\mu$ s Int. x 500 fr**  
\* It is clear even by 100 fr.  
\*\* It depends on the number of photons.



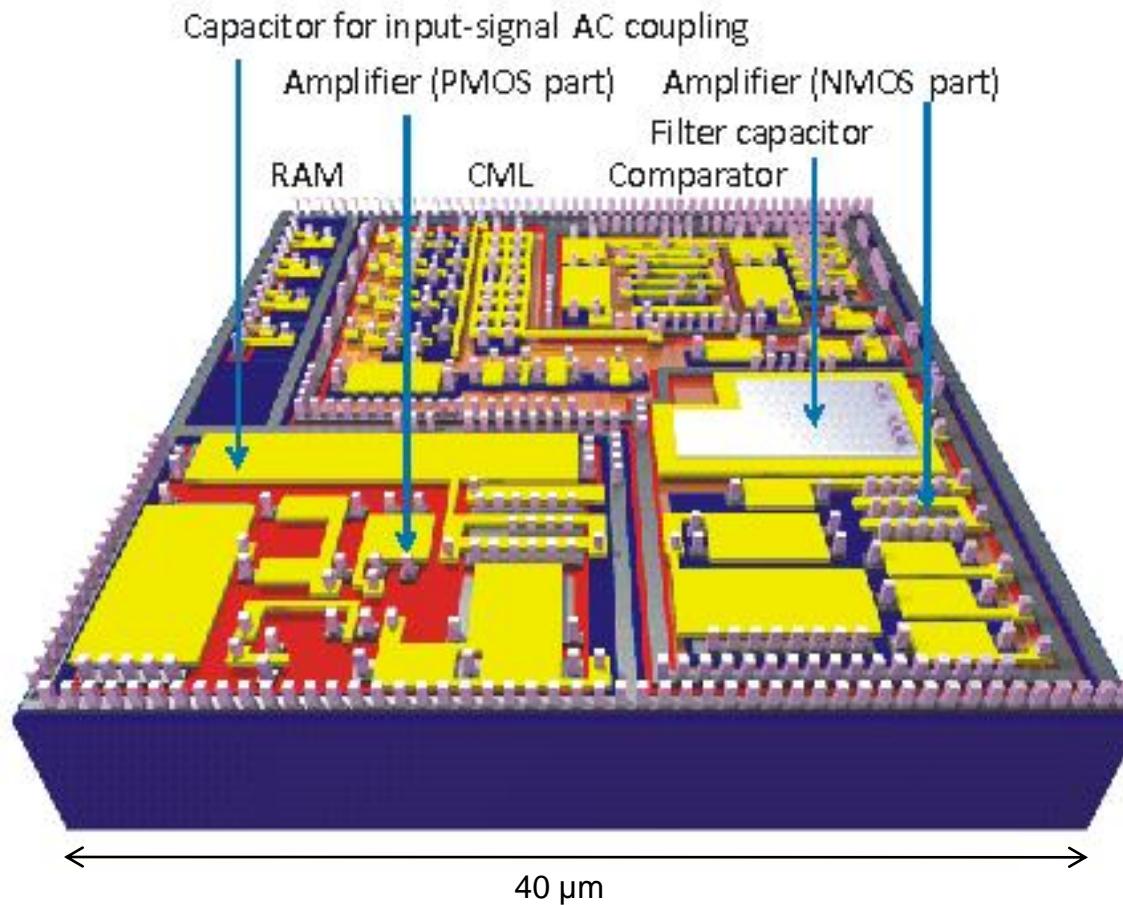
# HVCMOS

# HVCMOS (HVMAPS)

- HVCMOS is an attempt to implement CMOS depleted sensors in a standard process.
- HVCMOS uses one trick; the electronics is placed directly inside the collecting electrode. Transistors sense the tiny voltage change in their environment
- Since electronics is placed in the n-well the substrate is decoupled from the electronics
- It can be put on high negative potential and a large drift field is induced.
- This makes HVCMOS sensors very radiation tolerant.
- HVCMOS are based on a standard process. They are therefore cheap

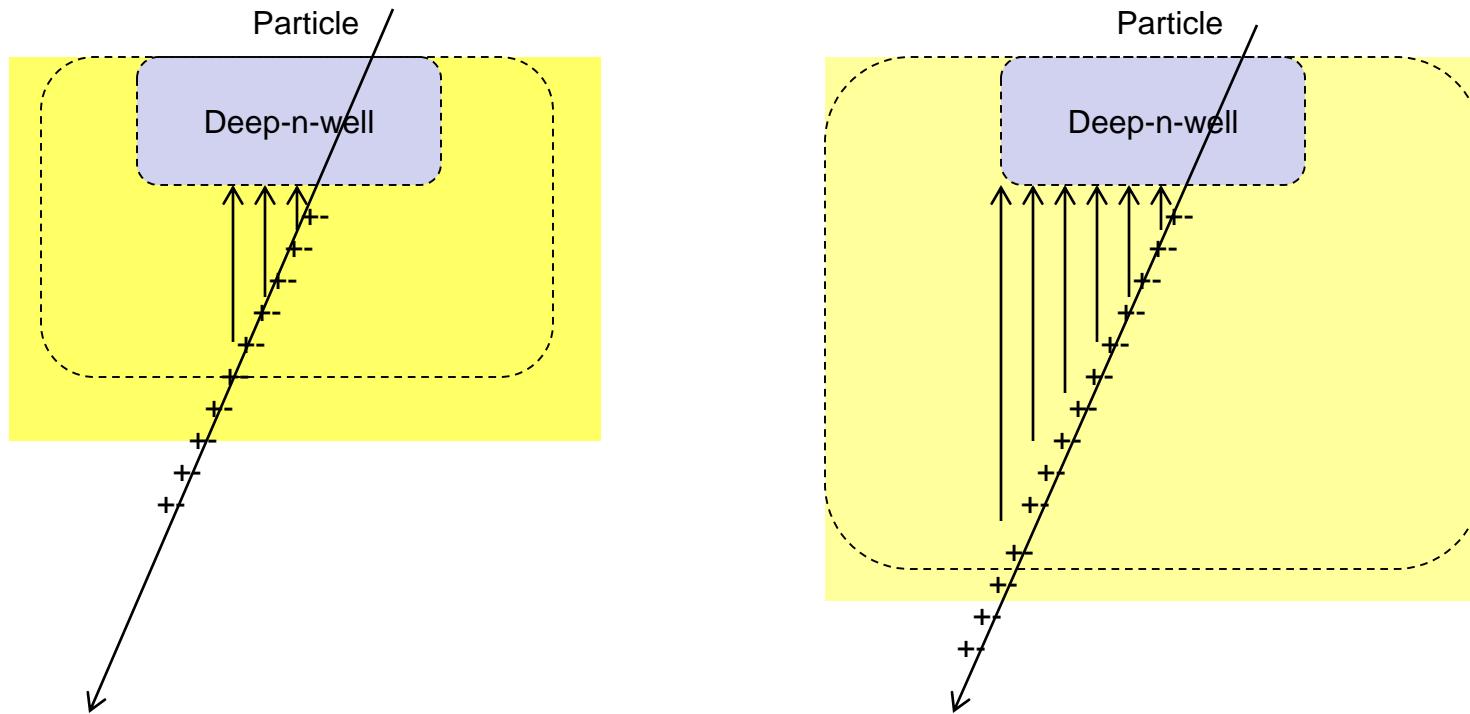


# 3D layout of a “smart diode”



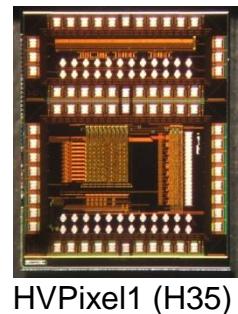
3D layout generated by GDS2POV software

- Further improvements of HVCmos
- Substrates of higher resistivity can be used to increase the depleted region size

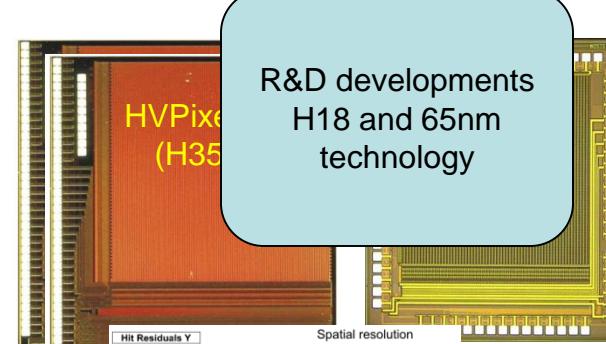
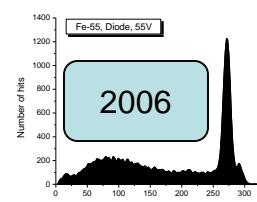
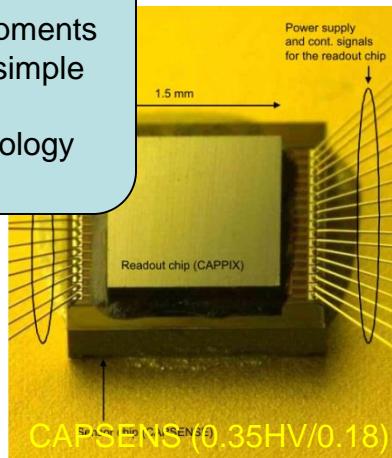


- Further improvements of HVCmos
- Substrates of higher resistivity can be used to increase the depleted region size
- Better PMOS isolation |

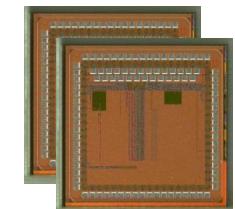
# HV CMOS detectors developed by our group



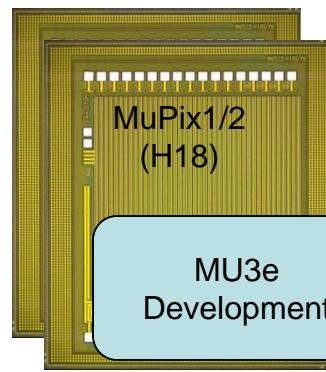
R&D developments  
Smart and simple pixels  
H35 Technology



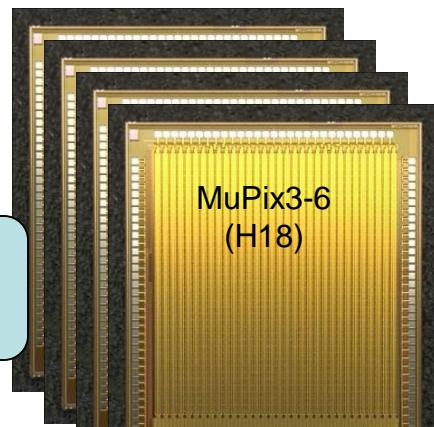
R&D developments  
H18 and 65nm technology



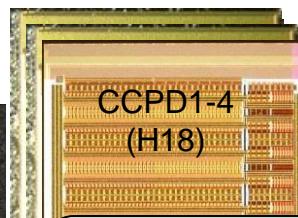
SDS (65nm)



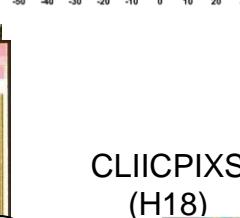
MU3e Development



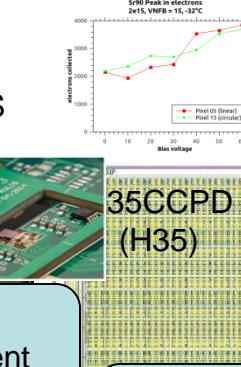
MuPix3-6 (H18)



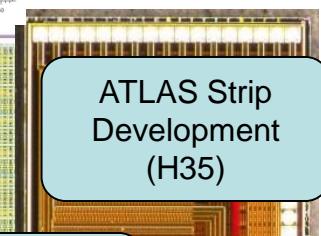
ATLAS Pixel Development CCPD (H18)



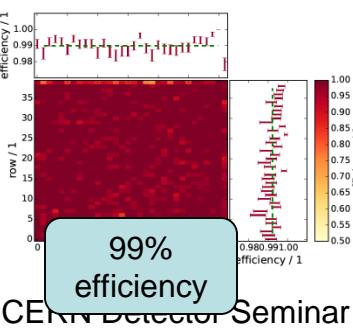
CLICPIX (H18)



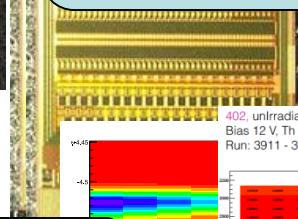
HVStrip (H35)



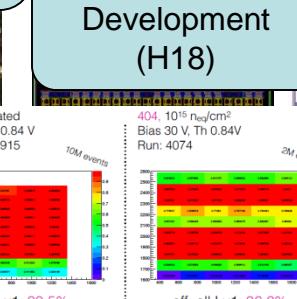
ATLAS Strip Development (H35)



Thinned chips



Irradiated chip

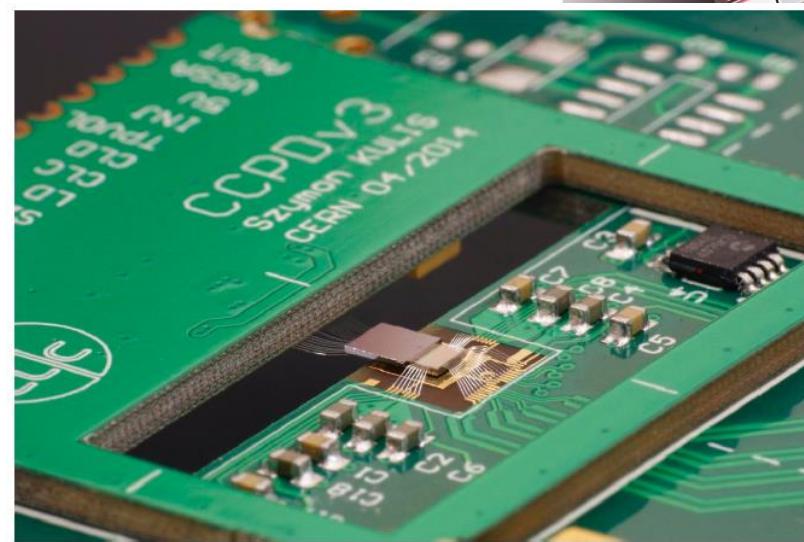
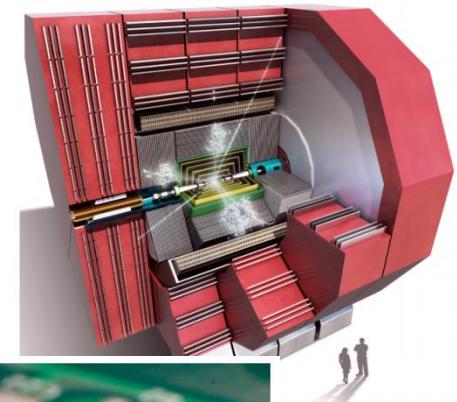
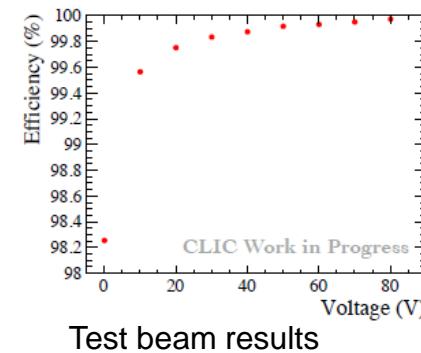
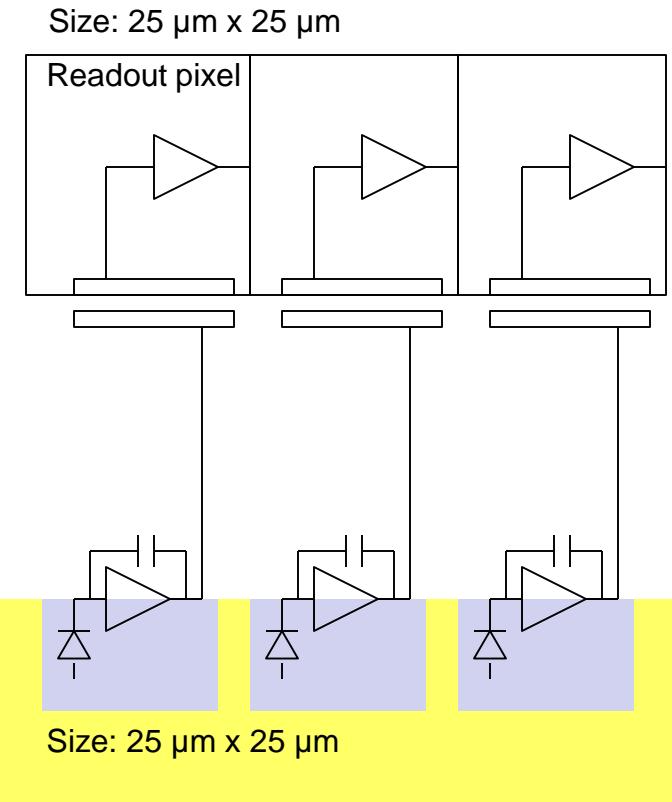


ATLAS Pixel Development (H35)

- The development of HVCMOS sensors started as a small project.
- Now they are developed within several collaborations:
- Mu3e collaboration (Heidelberg, PSI, KIT, University ETH Zuerich)
- ATLAS CMOS demonstrator collaboration
- ATLAS CMOS strip collaboration
- CLIC detector R&D group
- ATLAS HVMAPS collaboration

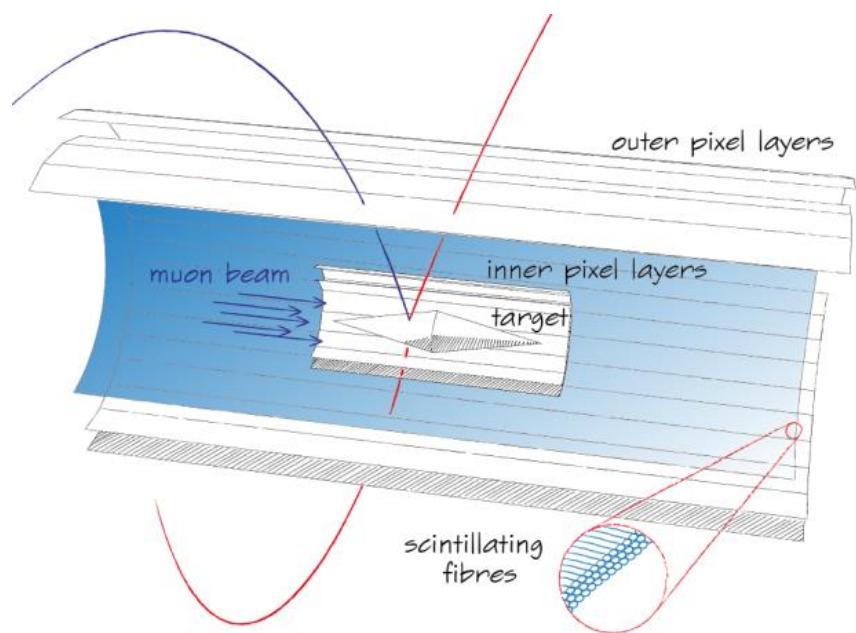
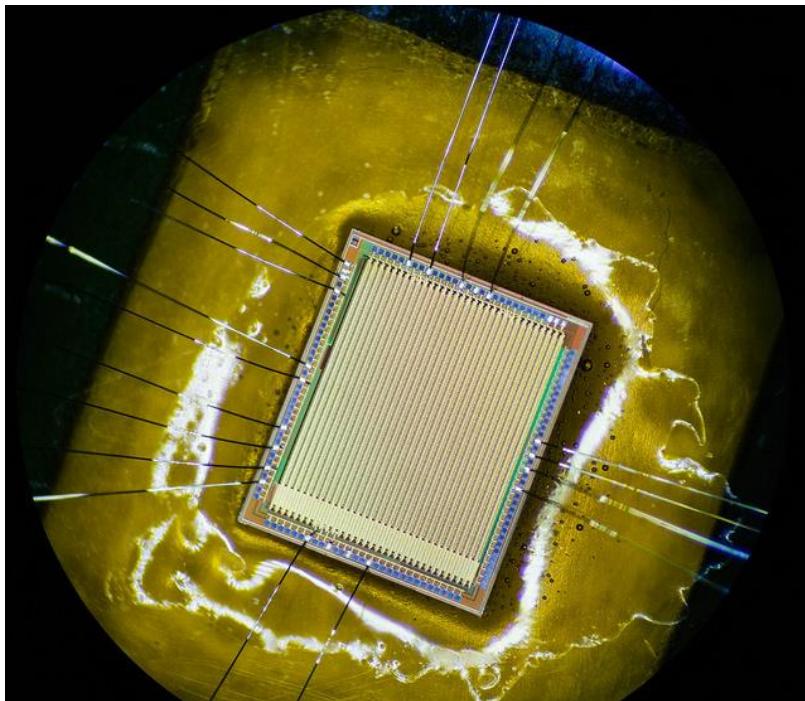
# CLIC

- CLIC
- 25um x 25um HVCmos pixels.
- The sensor is capacitively coupled to the CLIC pix ASIC
- Good results - detection efficiency is better than 99%.
- The pixels on the CLIC HVCmos contain only amplifiers – the output is analog.

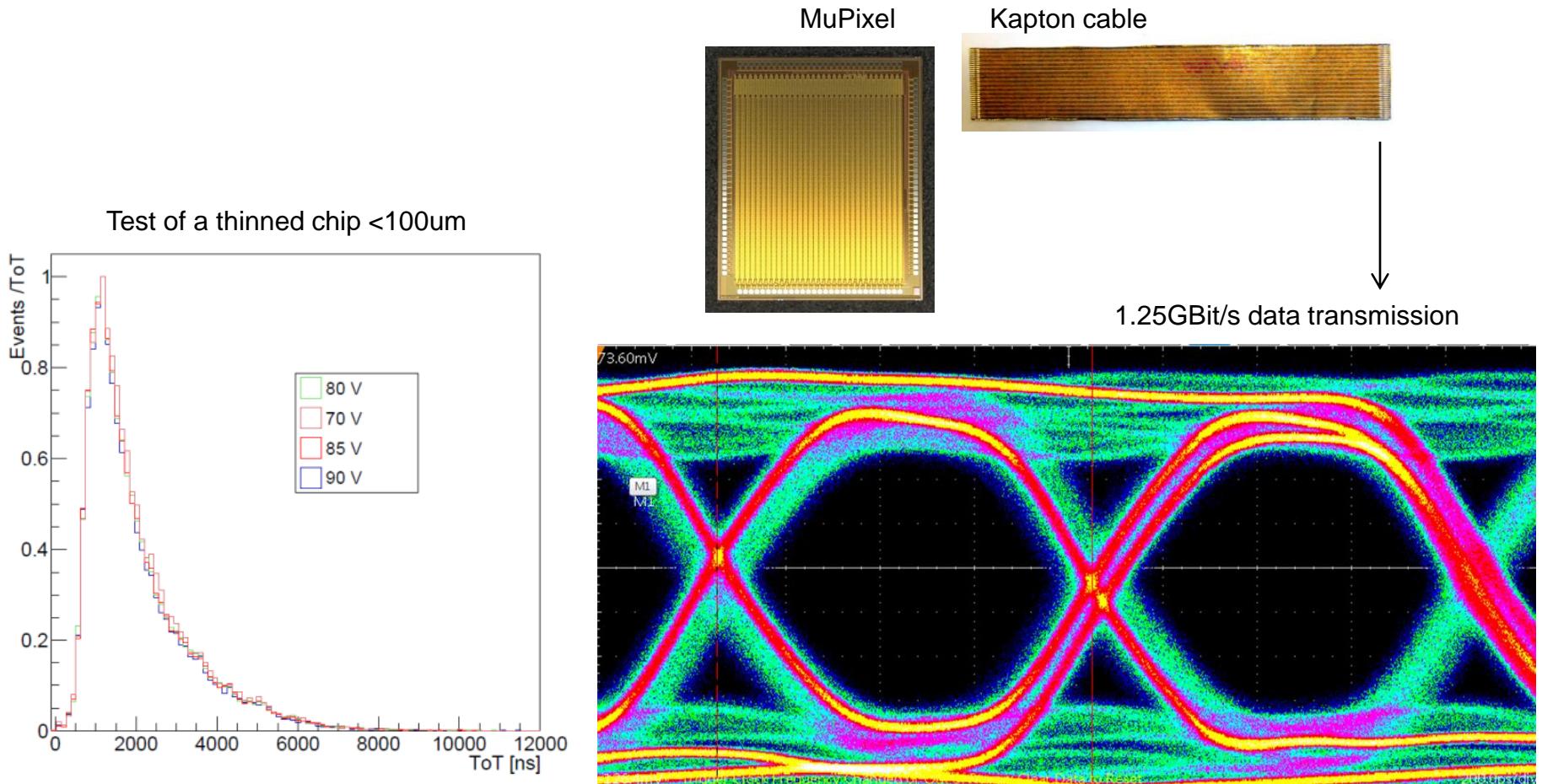


# Mu3e

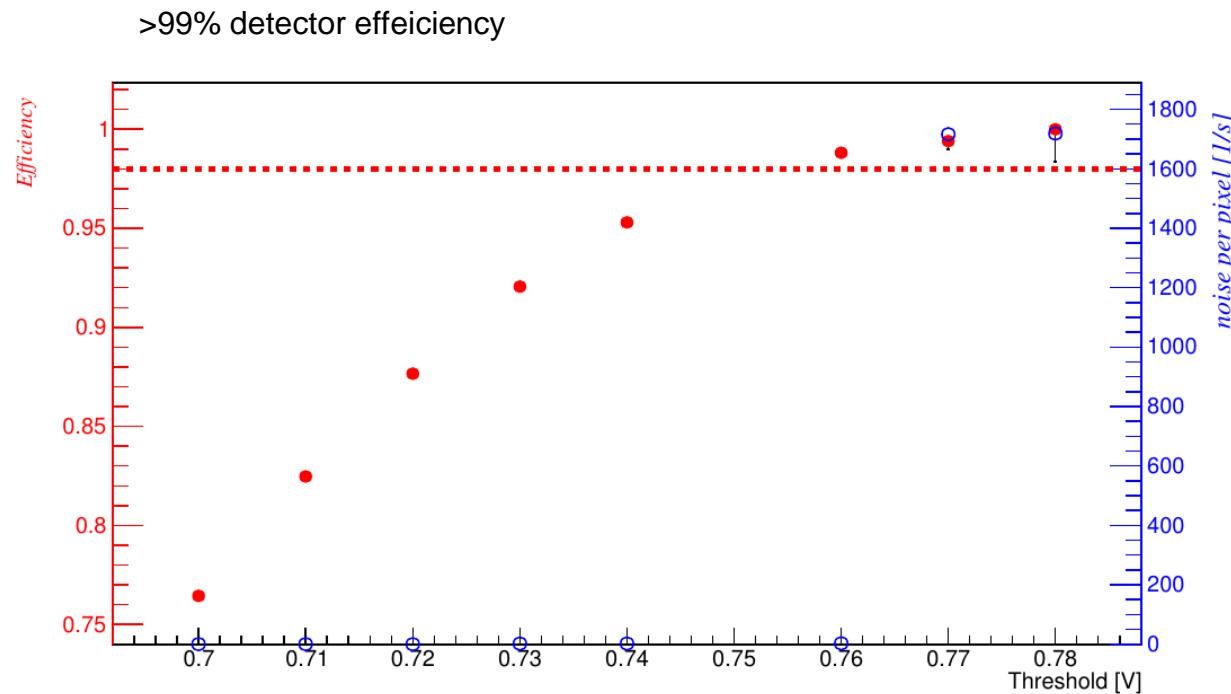
- The Mu3e is a proposed experiment at PSI.
- Search for the muon decay to three electrons
- The Mu3e detector should consist of three pixel layers with a total area of  $2\text{m}^2$ .
- Low electron momentum -> thin detectors are required.
- Time resolution of at least 100ns is required in the pixels.



- We have developed within several iterations a monolithic pixel sensor. It is a system on a chip - the readout electronics is placed on the same chip as the sensors. The signals are directly sent to FPGAs via GBit links. We measure 99% efficiency in beam tests
- Thinned chips successfully tested



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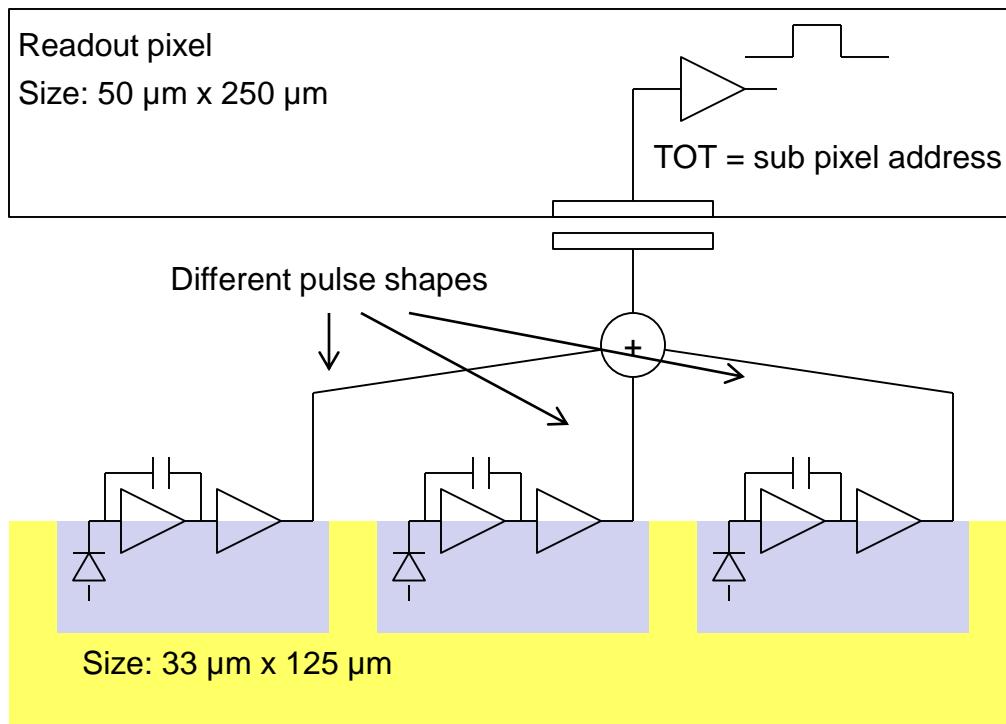


# ATLAS

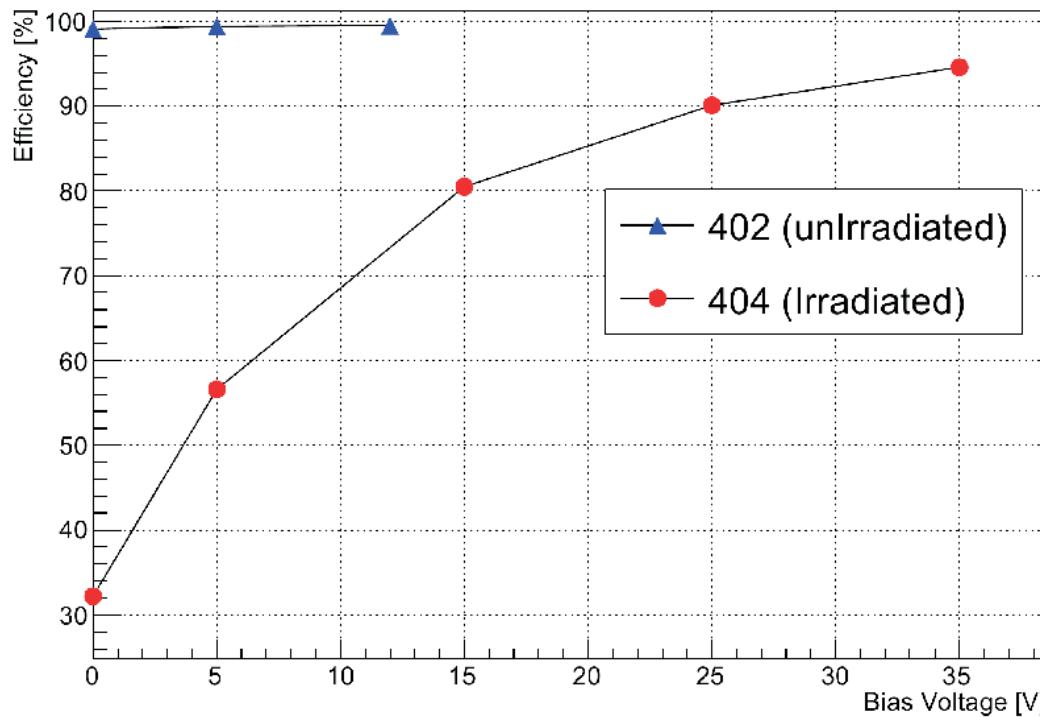
- HVCmos is also investigated for ATLAS upgrade, both for pixel and strip layers.
- Two concepts
- 1. The more conservative concept is to keep the existing readout chips, with slight modifications, and to replace the existing planar pixel or strip sensors with so called smart HVCmos sensors
- 2. Monolithic sensors

# CCPD Pixels

- Several smaller pixels connected to one readout cell of FEI4.
- Increased spatial resolution.
- Signals can be then capacitively transmitted from the sensor to the readout chip.
- No need for bump bonding



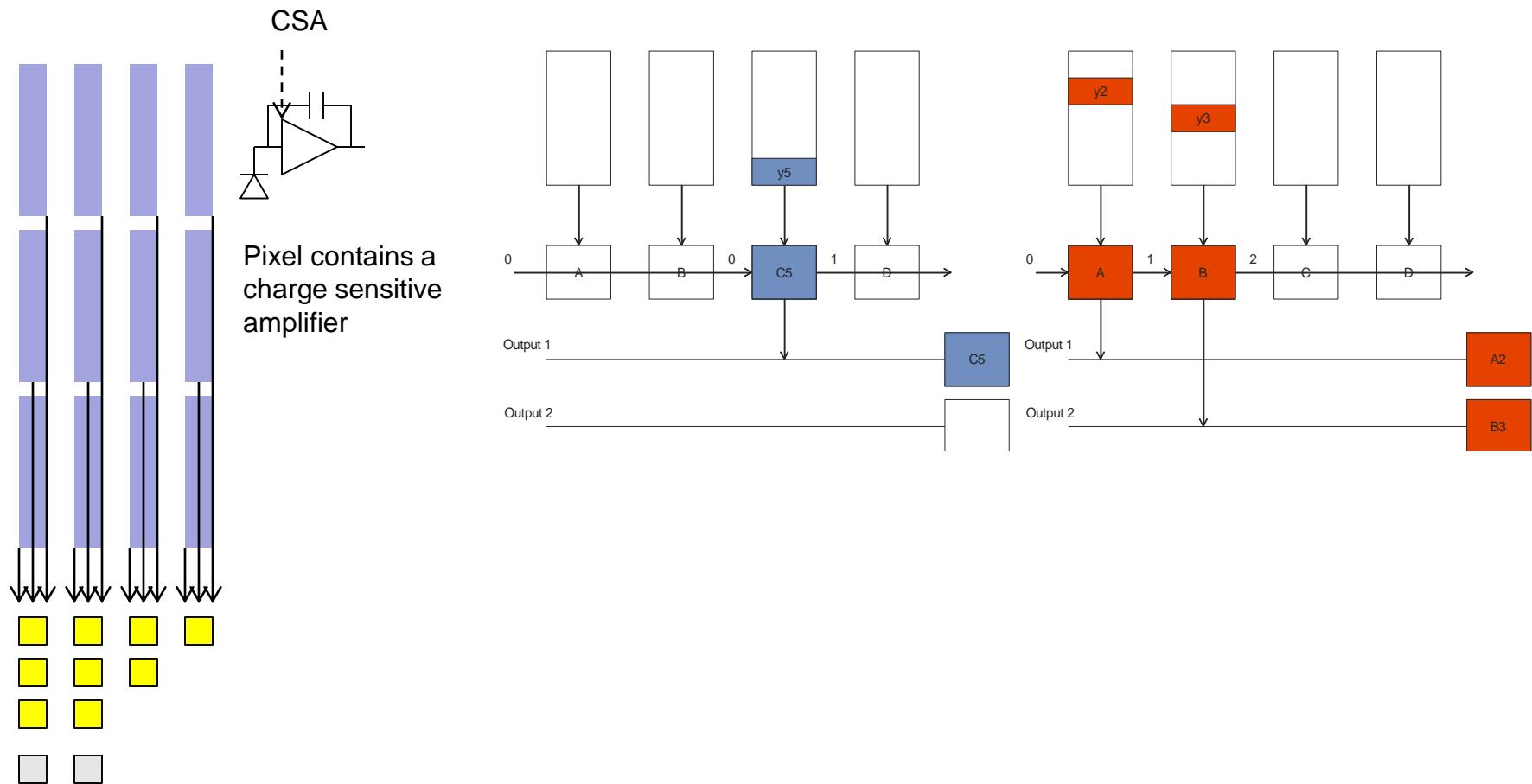
- >99% detection efficiency before irradiation
- Several chips irradiated with neutrons at Jozef Stefan institute in Ljubljana.
- Detection efficiency with an irradiated chip (fluence  $10^{15} n_{eq}$ ) 96%
- Bias voltage was reduced – 12V



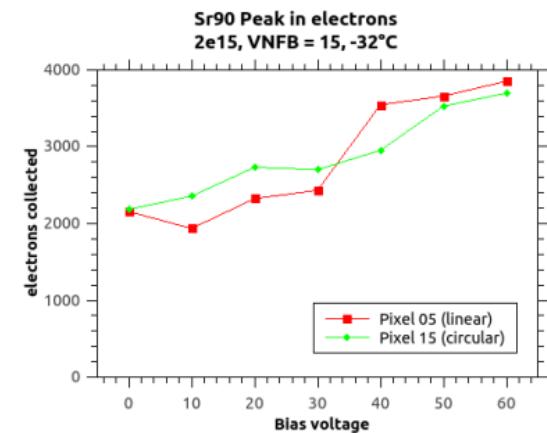
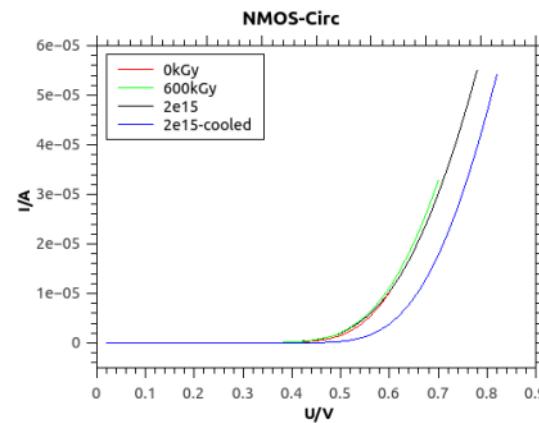
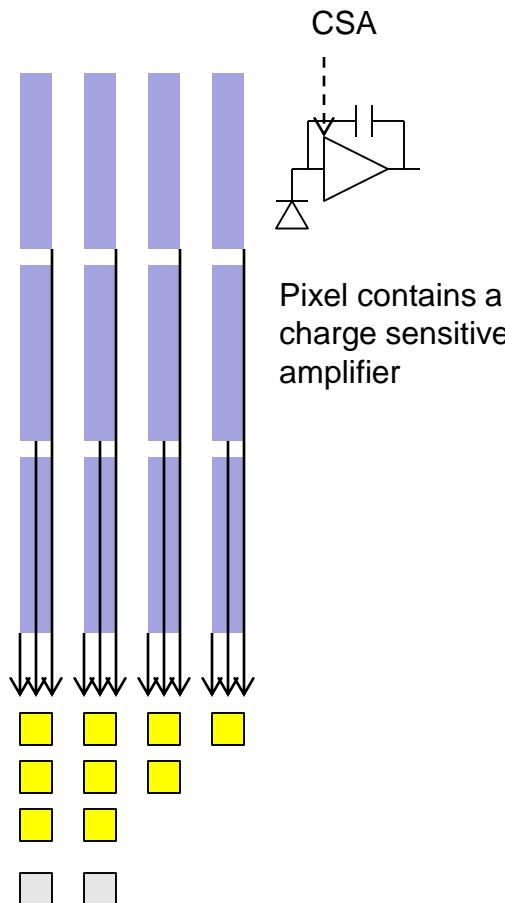
Efficiency of more than 99 % has been measured by University of Geneva with unirradiated chips and 96% with the chips irradiated to  $10^{15} n_{eq}/cm^2$  with neutrons

# CMOS Strips

- In the case of strips, hit data are sent in digital format to the external chip that does the triggering. HVCmos replacement for the strip sensor is actually a pixel sensor with long pixels.
- The advantages over the present concept is the z-resolution with one layer, less number of wire bonds between the sensor and the digital readout chip, and a simplified readout chip which is only digital.



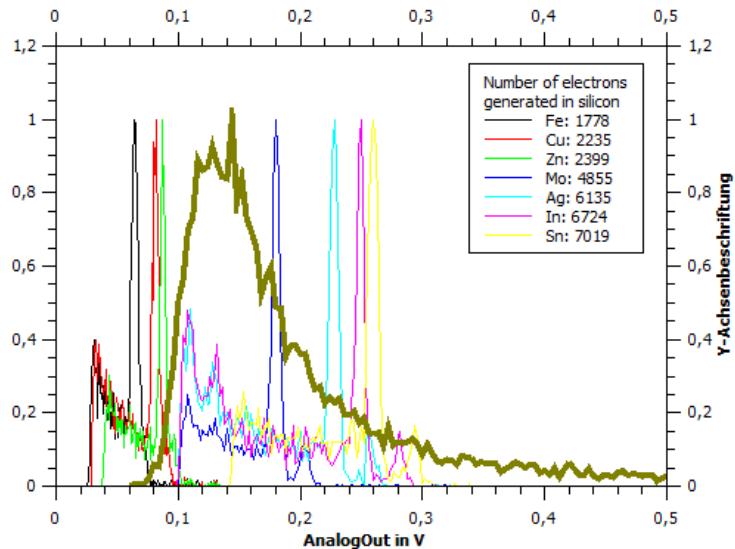
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**HVStripV1, irradiated to  $2 \times 10^{15} n_{eq}/cm^2$  - MPW of Sr-90 spectrum vs. sensor bias.**

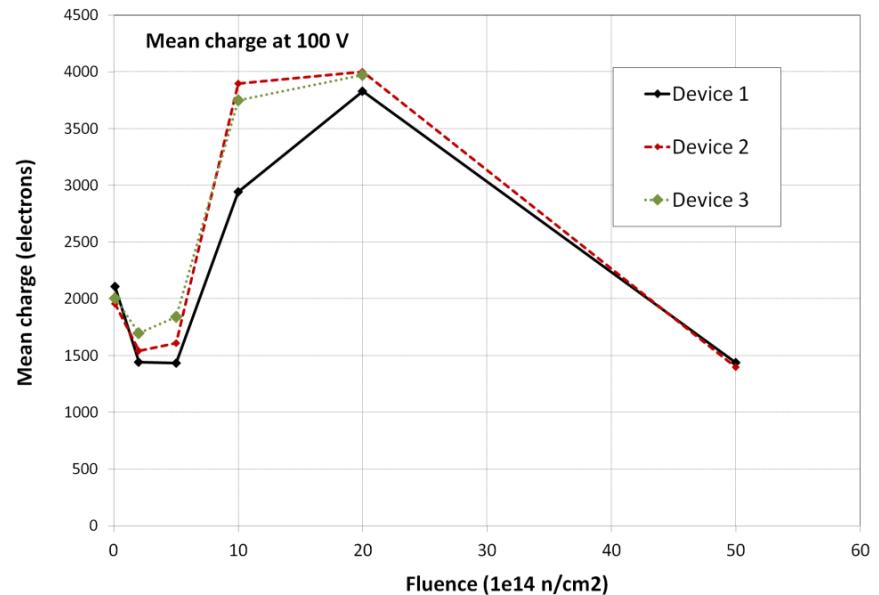
# Radiation Tolerance

- Radiation tolerance



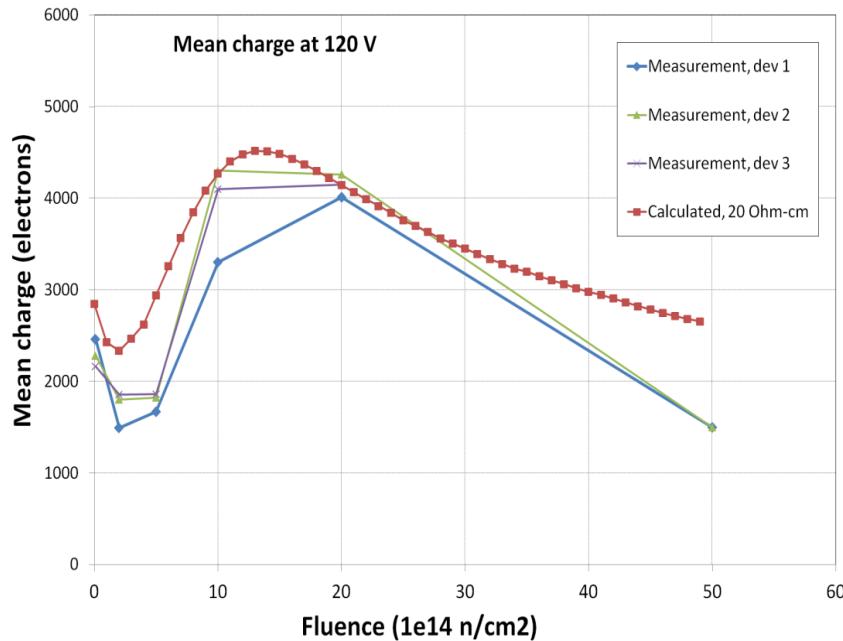
*Spectrum of beta particle signals when a HVStripV1, irradiated to  $2 \times 10^{15} n_{eq}/cm^2$  is exposed to Sr-90 source. Calibration x-ray spectra are also shown.*

Strontium-90 signal after proton irradiation to  $2 \times 10^{15} n_{eq}/cm^2 \sim 3600e$ . Signal to noise ratio after proton irradiation  $\sim 20$ .

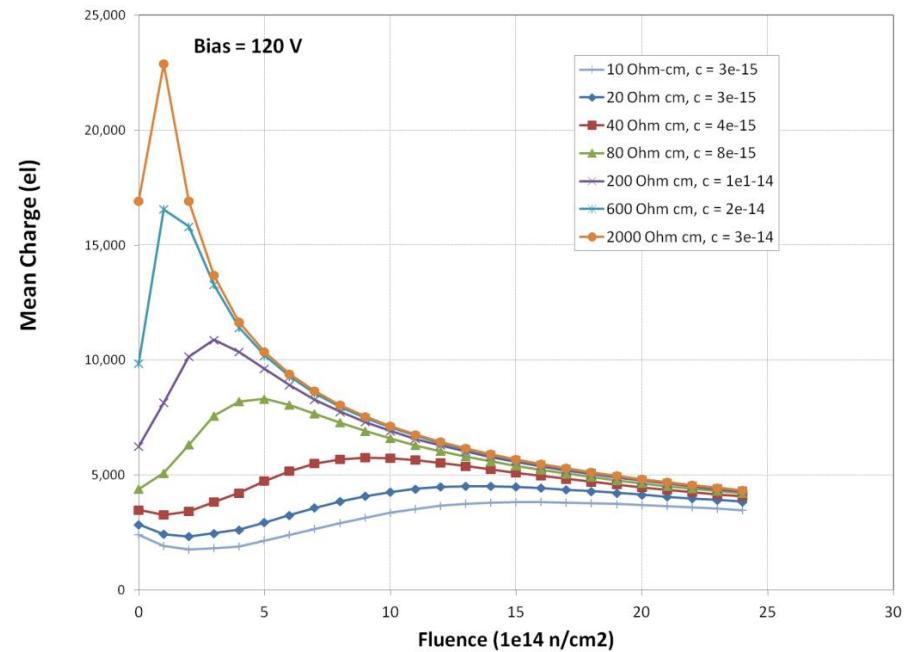


Charge vs. fluence

- Radiation tolerance



Compare measured/calculated

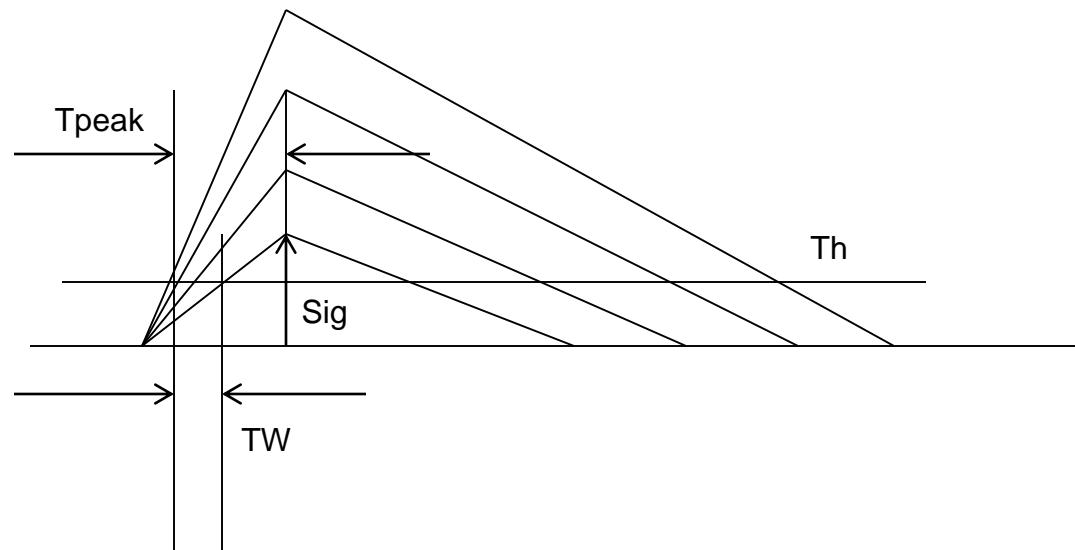


After a certain dose, we expect that all substrates behave similarly  
 200 Ohm cm probably the best choice

# Time Resolution

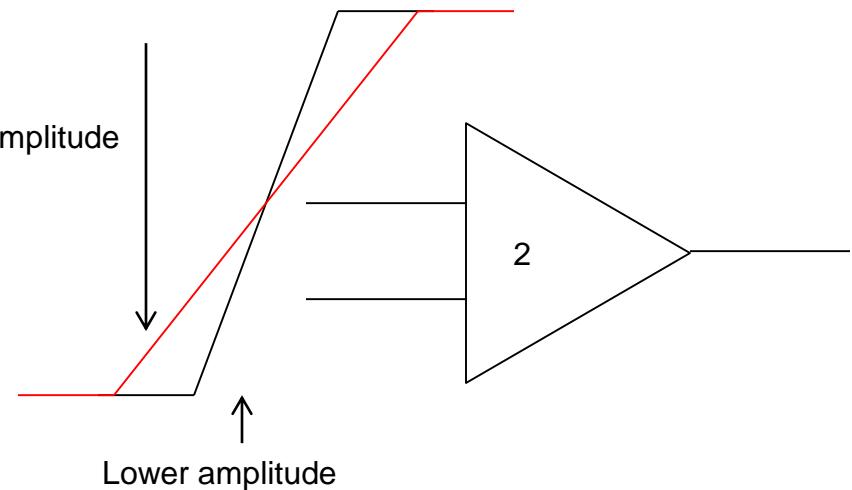
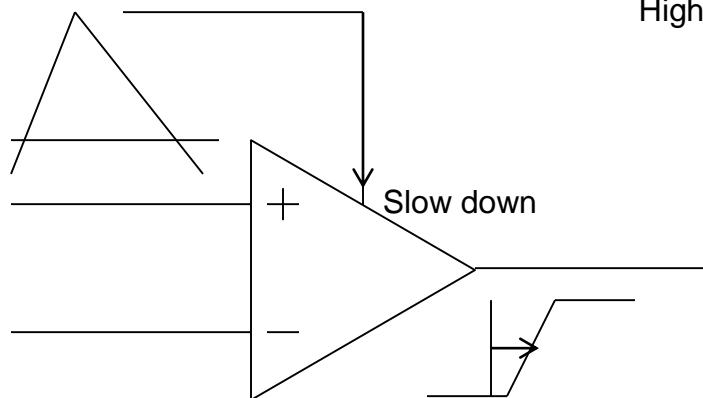
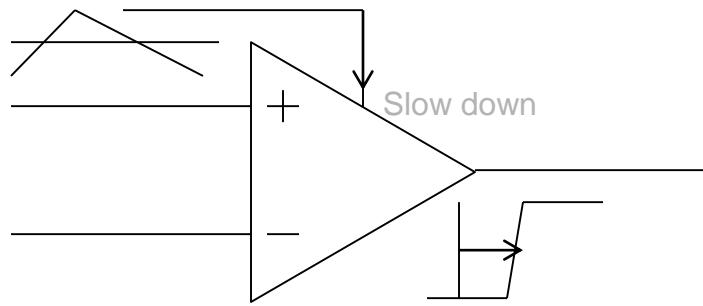
# Time resolution

- Time resolution in test beam measurements was about 100ns – we need 25ns
- This time uncertainty is mostly caused by the time walk effect
- The problem is that the preamplifier is designed to have a peaking time  $> 100\text{ns}$ .
- Using of long peaking time allows us to operate the detector in low-power mode – long peaking time reduces noise for an equal bias current (power). However if the signal spread is large (landau distribution), we will have a time walk – time skew.

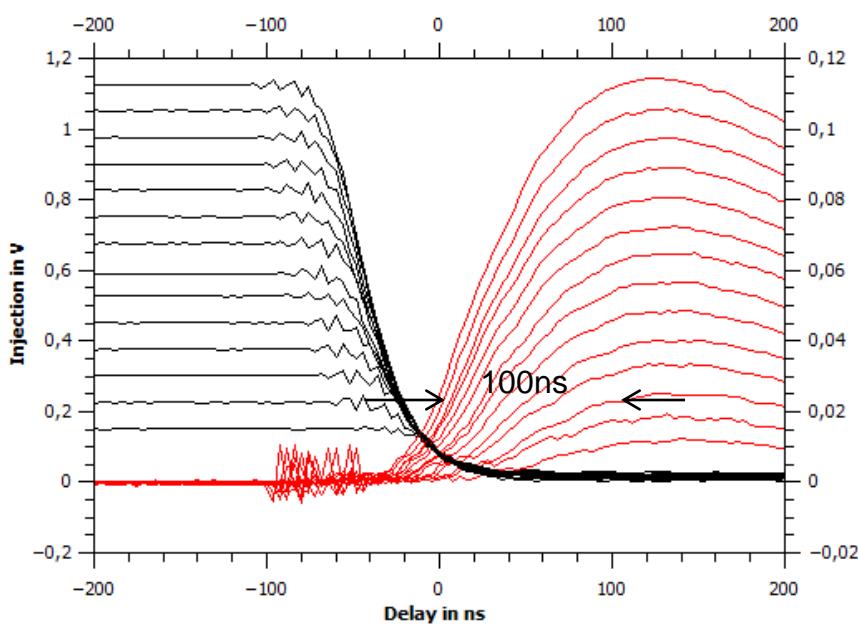


- There are a few way to improve time resolution
- One is to make the amplifier faster. This is possible, however it increases the noise. If we make amplifier faster we will probably need to increase the signal – which can be done by using high resistive substrate.
- More elegant way to improve the timing - compensation
- Bases of the fact that the time walk is proportional to the signal amplitude

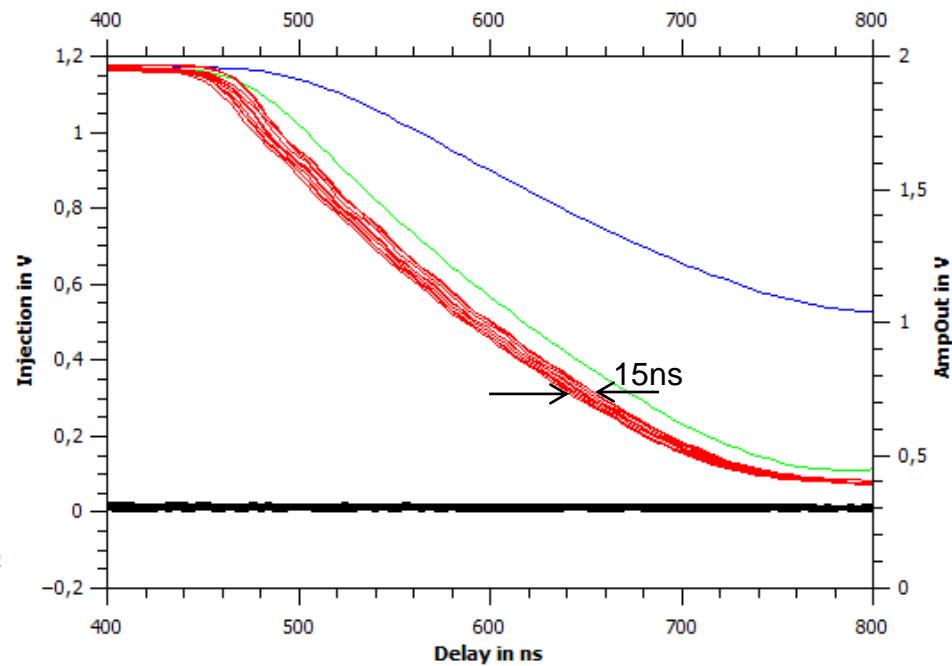
- Idea: time walk compensating comparator. Rise time is longer for signal with high amplitudes. This means a signal with higher amplitude has a faster threshold crossing, but the comparator output is slower.
- A signal with lower amplitude has a later threshold crossing but the comparator output is faster. As consequence of this the comparator outputs for all amplitudes can cross in one point. By adding another comparator we can make the response time independent of amplitude.



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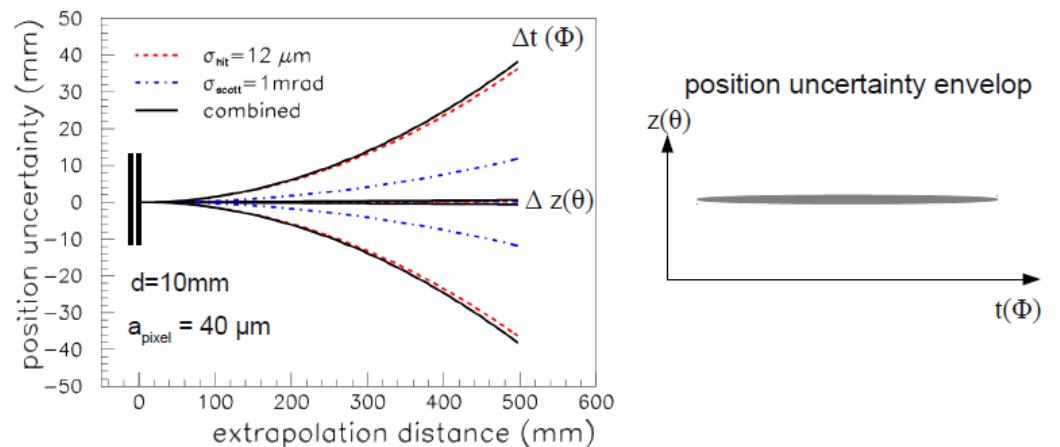
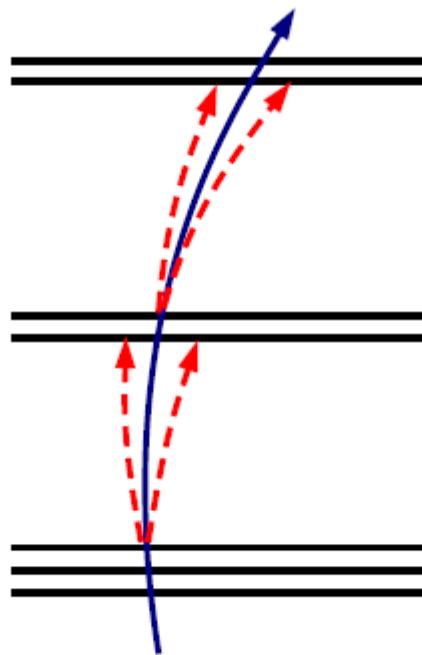
*Amplifier response to signals from 1000e to 3800e*



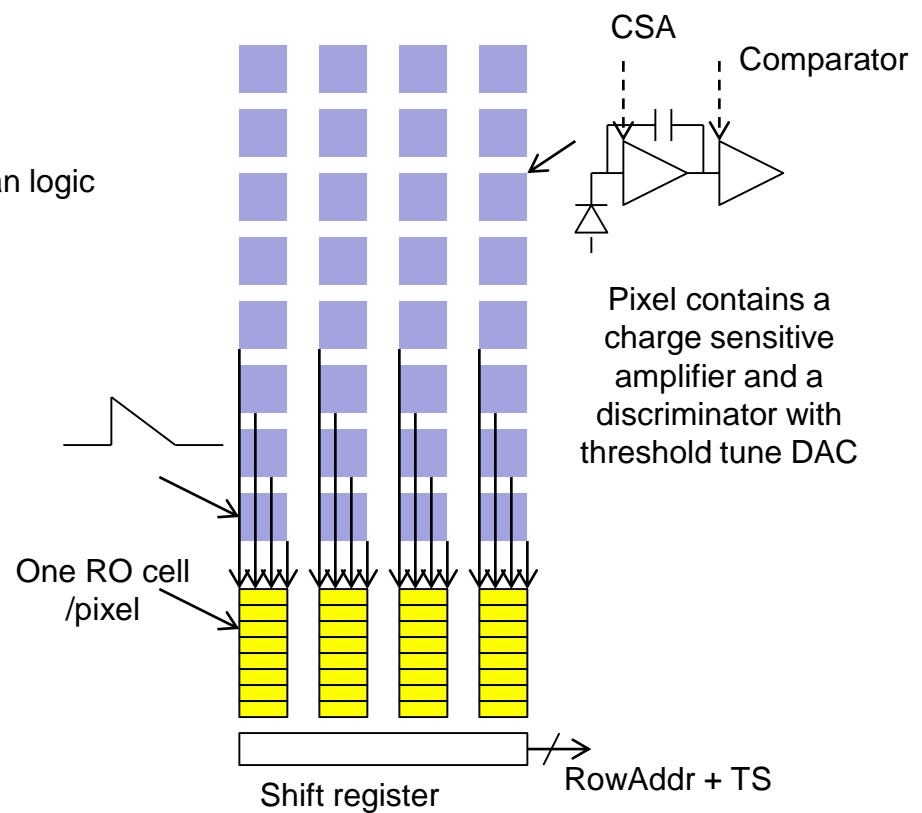
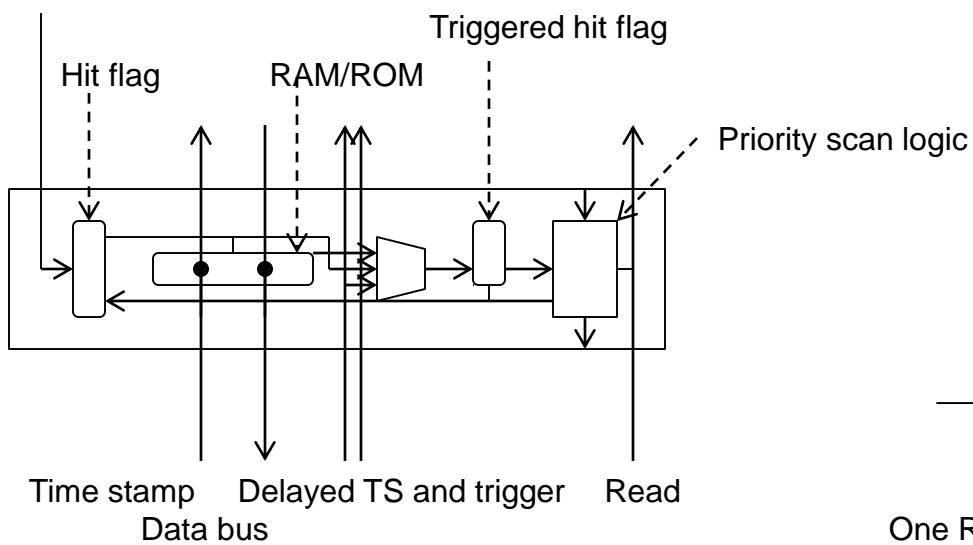
*Comparator response to signals from 1000e to 3800e*

# HVMAPS

- Another concept is the fully monolithic one. As in the case of Mu3e sensors, we would have the sensor and the readout part on the same chip.
- What are the advantages?
- We expect a better and easier track reconstruction if we used the rectangular pixels or e.g. 50  $\mu\text{m}$  x 50 $\mu\text{m}$  seize



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Thank you