Low-Noise Preamplifier Design Considerations for Large Area High Capacitance Solid-State Neutron Detectors

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***Abstract*—In this paper, the design of a low noise charge sensitive preamplifier, suitable for high capacitance solid-state neutron detector arrays, is described. Noise considerations related to arraying multiple detectors in either series or parallel are also presented. Using the designed preamplifier, an energy resolution of 12 keV FWHM in Si is achieved with 1 nF equivalent detector capacitance and 10 μS shaping time. Additionally, a novel preamplifier topology, which utilizes a capacitance canceling input stage, is presented. Detailed analysis of the capacitance cancelling stage is discussed with special consideration given to its use with a charge sensitive preamplifier. Up to a 15% decrease in noise is demonstrated using the capacitance cancelling technique.**

***Index Terms*—Low-noise amplifiers , noise, nuclear physics instrumentation, solid-state neutron detectors.**

I. Introduction

NEUTRON detectors are used in a number of applications including detection of special nuclear materials for homeland security. Historically, helium-3 gas filled tubes have been considered the standard approach for neutron detection due to their high efficiency, low gamma sensitivity, and large detection area [1]. However, with the increasing costs of helium-3 gas, recent research efforts have focused on finding a low cost alternative [2]. Solid-state detectors, in the form of microstructured p-n junction diodes combined with a suitable converter material, are one possible alternative.

In our previous work, we have demonstrated such solid-state neutron detectors (SSND) which provide low gamma sensitivity, thermal neutron detection efficiency up to 28%, and have the capability to be scaled up to 16 cm^2 in area with minimal loss in efficiency [3], [4]. Scaling to a larger detection area can be achieved through combining individual 16 cm^2 panels, each connected to its own electronic readout channel. However, for a large number of channels, the cost and power consumption of the associated electronics is of increasing concern. Additionally, the electronic noise of the amplification system must be minimized given that it is the primary factor affecting the detection efficiency. Minimizing this noise is complicated by the large capacitance of the developed detectors ($>$ 4 nF for a 1 cm^2 area) and leads to a number of unique challenges in the electronics design. A major goal of this research effort is to develop detectors and their associated readout electronics for portable and hand-held detection systems. For such applications, the electronic readout system must be low noise, compact, low power, and inexpensive. Commercial low-noise preamplifiers for high capacitance detectors exist [5], [6], however they do not adequately address all of the previously mentioned design criteria. For these reasons, it is necessary to develop low noise and low power custom readout electronics that are optimized for very high capacitance detectors.

The paper is organized as follows; Section II provides a brief introduction to microstructured solid-state neutron detectors in terms of their fabrication and operating principle. Section III gives the design considerations from an electronics perspective for large area detector arrays. A detailed analysis of an extremely low noise charge sensitive preamplifier suitable for high capacitance detectors is presented in Section IV. Section V proposes a novel preamplifier topology, utilizing a capacitance canceling stage to lower electronic noise, while conclusions are drawn in Section VI.

II. Microstructured Solid-State Neutron Detectors

A. Device Fabrication

In order to overcome the low efficiency of conventional planar detectors (^{10}B, or ^{6}LiF coated on top of planar p-n junction) [7], [8], most of recent solid-state neutron detectors (SSND) utilize three-dimensional (3D) silicon p-i-n diodes with different microstructures: hexagonal holes in honeycomb pattern, micro pillars, or deep trenches [9]–[12]. The basic principle involved is the same, having deep holes or trenches in Si whereby these trenches are filled with converter materials such as ^{10}B or ^{6}LiF. This microstructure design is thick enough to absorb neutrons (40 μm of ^{10}B absorbed $> 90\%$ of thermal neutrons at 0.0253 eV) and allows daughter products to escape the boron with enough energy to deposit appreciable energy in the Si p-n junction. One of the main challenges in fabricating

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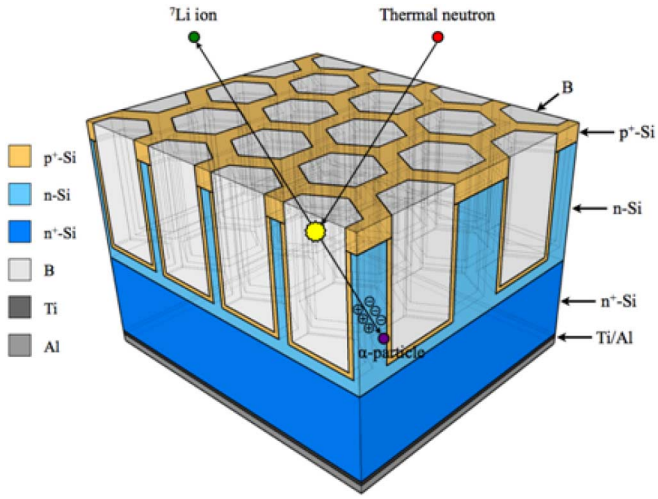

Fig. 1. Schematic of a honeycomb solid-state neutron detector (SSND) [3].

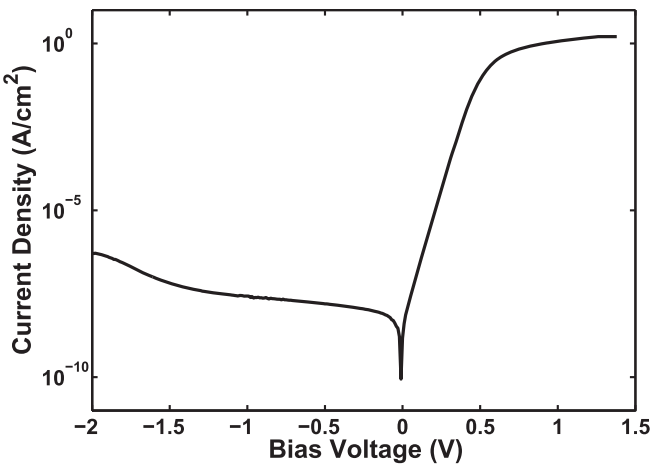

Fig. 2. Leakage current vs. bias voltage for a 1 cm² honeycomb SSND.

such microstructure diode is to keep the leakage current low enough so that the pulse generated by neutron absorption is above the noise level of the device. To achieve low leakage current, a novel technique of continuous p-n junction formation over the entire surface of the microstructure was developed as explained in our earlier publications [12], [13]. A schematic of such detector is shown in Fig. 1.

A typical leakage current vs. bias voltage of our 1 cm^2 honeycomb detector is shown in Fig. 2. The reverse leakage current density at -1 V for the fabricated device is 3×10^{-8} A/cm^2. A relatively low leakage current indicates that the continuous p-n junction formation after DRIE and prior to boron filling process is a crucial step to reduce surface recombination in the etched sidewalls. Further discussion of leakage current reduction may be found in our earlier publication [3]. Additionally, honeycomb structure even with 1 μm Si wall is so robust that the stress caused by boron deposition does not create any micro cracks in the structure; otherwise, significantly higher leakage current is expected from such cracks.

Fig. 3. shows the capacitance as a function of bias voltage for a 6.25 mm^2 detector. The detectors are operated with zero bias voltage so the capacitance is roughly 280 pF for a single 6.25 mm^2 device. Larger than 1 cm^2 detectors are formed through a parallel array of sixteen smaller detectors and therefore have $\approx$ 4480 pF of capacitance.

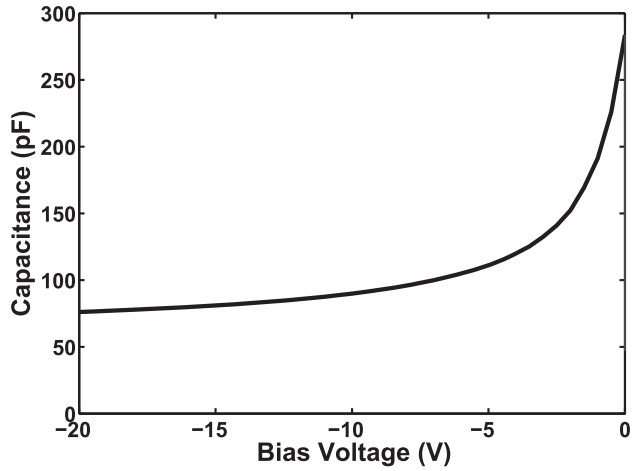

Fig. 3. Detector capacitance vs. bias voltage for a 6.25 mm² detector.

B. Principle of Operation

Neutrons are neutral particles, thus they don't directly ionize a detection material. Instead, neutrons are detected in a multi-step process, beginning with the conversion of a neutron into high-energy, charged particles. ^{10}B is chosen as the neutron converting material because of its high neutron cross section and compatibility with silicon. The neutron absorption reaction for ^{10}B can be given as

$$ {}^{10}_{5}B + {}^{1}_{0}n \begin{cases} 94\% : {}^{7}_{3}Li(0.8MeV) + {}^{4}_{2}\alpha(1.4MeV) \\ 6\% : {}^{7}_{3}Li(1.015MeV) + {}^{4}_{2}\alpha(1.777MeV) \end{cases} \quad (1) $$

The resulting ^7Li and $^4\alpha$ ions are emitted in opposite directions and can escape the micron-size boron region, entering the silicon region with a fraction of their initial kinetic energy. The residual energy is deposited in the charge-collecting silicon p-n junction, which is contacted with sputtered metal. Subsequent amplification, pulse shaping, and discrimination of the signal allow for neutron events to be identified if the pulse height is greater than the electronic noise level.

The noise level of the detection system has a direct impact on the neutron efficiency. Using a commercial ORTEC 142AH preamplifier, the honeycomb devices have demonstrated an intrinsic thermal (E = 0.0253 eV) neutron efficiency up to 28% [4]. The development of a customized preamplifier with a lower noise level for multiple device arrangements is presented in the following sections.

III. Large Area Detector Arrays

The detectors are processed as 1 cm^2 dies each of which contains 16 individual 2.5 mm $\times$ 2.5 mm (6.25 mm^2 area) detectors. Fig. 4(a). shows the detectors after processing. The individual 6.25 mm^2 devices are connected in parallel and bonded to a copper substrate as shown in Fig. 4(b). In order to create even larger area detectors, multiple 1 cm^2 devices may be connected

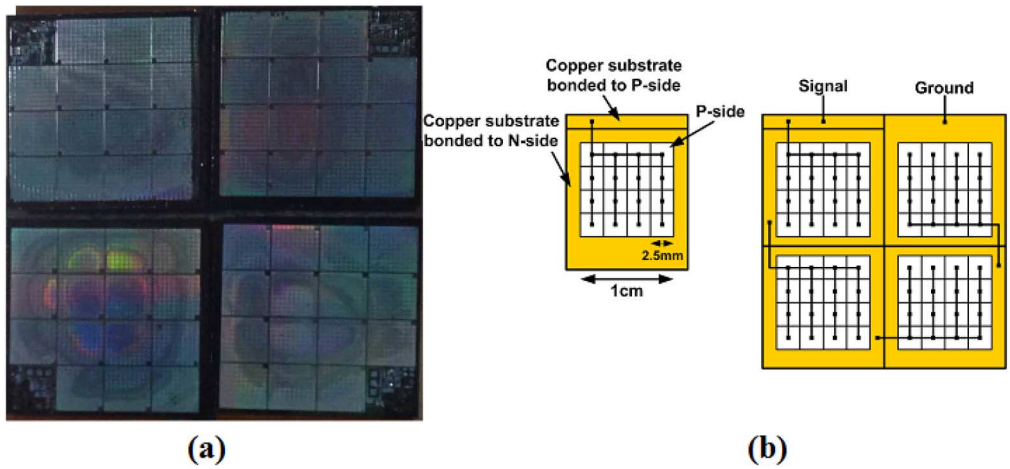

Fig. 4. (a) Photograph of individual 1 cm² detectors, and (b) connection diagram of 1 and 4 cm² detectors.

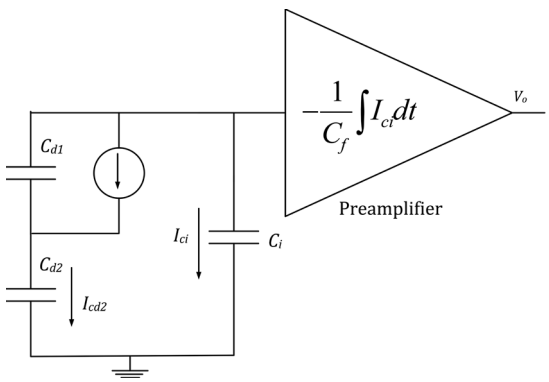

Fig. 5. Charge collection with series connected SSDNs. C_{d1} and C_{d2} are the two detector capacitances. I_{d1} is the signal current in the first detector, I_{cd2} and I_{ci} are the current shunted to the second detector capacitance and preamplifier dynamic input capacitance respectively. For charge collection efficiency calculations, only the amplifier input capacitance is considered, since the input resistance would mainly affect the rise time and not the collection efficiency [14].

either in series or in parallel [3]. However, such configuration negatively impacts the signal to noise ratio (SNR) at the output of the preamplifier. To illustrate this effect, consider a generic preamplifier which has an unloaded noise level e_{n0} (eV) and a noise slope of N_s (eV/pF), interfaced with an array of n detectors each with an intrinsic capacitance C_d (pF). By connecting the detectors in series, the capacitance seen by the preamplifier is decreased from C_d by a factor n. The total output noise E_n for the series configuration can be given as:

$$E_n = \frac{N_s C_d}{n} + e_{n0} \tag{2}$$

However, the output signal from the detector is also decreased by the same factor n. Fig. 5 illustrates this effect, where the preamplifier is represented as a gain block proportional to the integral of the current in the preamplifier dynamic input capacitance C_i [14] which is much larger than the detector capacitances, C_{d1} and C_{d2}. Note that the preamplifier gain given in Fig. 5 is simplified to that of an amplifier with infinite bandwidth and thus, any signal rise time is not considered. When a neutron interacts with the first detector, the signal current will circulate in the impedance of C_{d1} and the series combination of C_{d2} and C_i. Assuming $C_{d2} = C_{d1}$, the current in C_i is exactly half of the signal current. Therefore, the voltage at the output is half compared to a single detector. For n detectors, the response to an energy signal ϵ_s for a preamplifier with gain A_ϵ is $\epsilon_s A_\epsilon / n$. Using (2), the signal to noise ratio (SNR) of the series array can be derived as:

$$SNR = \frac{\frac{\epsilon_s A_\epsilon}{n}}{\frac{N_s C_d}{n} + e_{n0}} \tag{3}$$

Comparing the above to the SNR of a single detector ($n = 1$ in (3)), yields a measure of the relative SNR for the array for the series connection.

$$SNR_S = \frac{e_{n0} + C_d N_s}{n e_{n0} + C_d N_s} \tag{4}$$

From (4), it is clear that the SNR is always less than 1, indicating that the effective noise level at the preamplifier output increases for a series connected detector array.

For parallel connected detectors, the capacitance seen by the preamplifier is increased by a factor n and the total output noise can be given by:

$$E_n = N_s C_d n + e_{n0} \tag{5}$$

Using the same procedure described above, the relative SNR for the parallel connection can be derived as:

$$SNR_P = \frac{C_d N_s + e_{n0}}{n C_d N_s + e_{n0}} \tag{6}$$

Note that the above expression does not account for the increased leakage which results from connecting the detectors in parallel. A higher detector current leads to an increased amount of shot noise at the preamplifier input and will decrease the actual SNR from that predicted in (6). Fig. 6. plots equations (4) and (6) using parameters from the Ortec 142AH preamplifier [15]. Comparing the two plots, it is clear that for high capacitance detectors, a series connection will always provide superior SNR. However, the reduction in the signal amplitude might

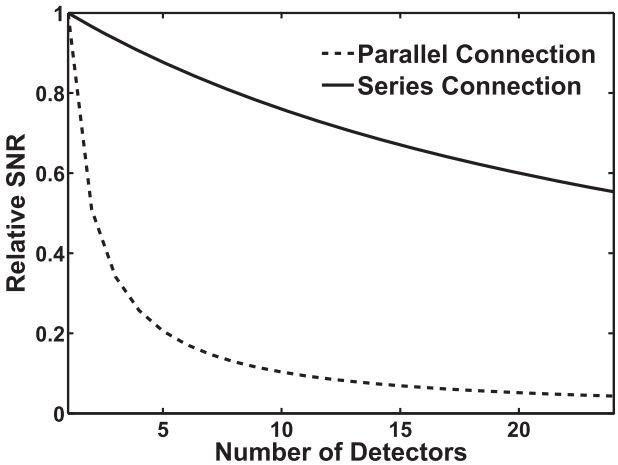

Fig. 6. SNR for series (4) and parallel (6) connected detectors. The parameters $e_{n0} = 1.55$ keV, $N_s = 18$ eV/pF, and $C_d = 4.4$ nF are obtained from the Ortec 142AH preamplifier [15].

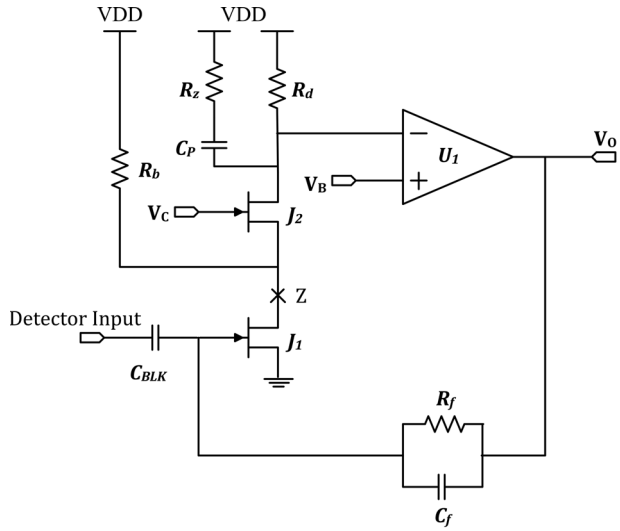

Fig. 7. Schematic of the designed preamplifier.

be unacceptable for certain applications and would require increased gain/noise requirements from the following amplification stages as will be shown in Section IV.

IV. Preamplifier Design

Numerous charge sensitive preamplifier topologies have been covered in the literature, the majority of which focus on silicon integrated CMOS technology for low capacitance detectors [16]–[19]. The analysis of such amplifiers has been covered in great detail with different design approaches for low noise optimization [17]–[19]. However, published art is limited for detectors with capacitance around several hundred pico-farads, examples of which include the work presented in [20]–[22]. When designing a charge amplifier to interface with large area, high capacitance detectors, several additional factors have to be considered. First, the product of the open loop gain of the amplifier and the feedback capacitor has to be sufficiently high to ensure that the dynamic input capacitance of the amplifier, C_i in Fig. 5, is much larger than the detector capacitance. Second, to ensure a fast response time, either the preamplifier must have a high open loop bandwidth or, alternatively, large values of feedback capacitors may be used. The latter decreases the charge to voltage gain of the circuit, necessitating an additional amplification stage. Third, as the dominant noise source is the series voltage noise, the transconductance of the input stage must be made relatively high. This is achieved by increasing the input stage current, using multiple parallel devices or a combination of the two.

Fig. 7 shows the schematic of the designed charge amplifier. While the topology is similar to that presented in [23], the large area specifications completely change the design methodology. The detector is AC coupled to the input of the preamplifier at the gate of J_1 through a short coaxial cable to minimize added parasitic capacitance. Since the cable length is minimal, a termination resistor is not used in the circuit however, if longer cables were needed, a termination resistance at the gate of J_1 should be used in order to prevent signal reflection between the detector and amplifier. In the schematic J_1 and J_2 are composite devices consisting of a number of JFETs connected in parallel to achieve lower noise. For a fixed amount of drain current, and assuming the transistors operate in the saturation region, doubling the number of parallel connected devices increases the effective transconductance by a factor of $\sqrt{2}$, while lowering the channel thermal noise by a factor of $\sqrt[4]{2}$ [24]. Additionally, the flicker noise is reduced by a factor of $\sqrt{2}$. In the presented design, six parallel devices are used with a total drain current of 15 mA; thus the achieved transconductance is approximately 250mS. With such high gain in the first stage, and with a large number of parallel devices, the capacitance reflected to the input from multiplication of the drain to gate capacitance due to the Miller effect will be significant. This multiplication increases the preamplifier rise time constant, $\tau_i = R_i C_t$. Here R_i is the bandwidth dependent 'cold resistance' of the preamplifier [25], and C_t is the total physical capacitance present at the preamplifier input including the detector, feedback, and any other parasitic capacitance. To mitigate the Miller effect, a cascode transistor J_2 is added to the circuit as shown in Fig. 7.

The circuit is designed to have an open loop gain greater than 100 dB, which is large enough to ensure that all of the detector charge is amplified. Due to the high gain, resistor and capacitor R_z and C_p are necessary to stabilize the circuit. The addition of these components creates a pole at approximately $1/(C_p(R_z + R_d))$ and a zero at $1/(C_p R_z)$, which decreases the loop gain by roughly $20log_{10}(1 + R_d/R_z)$ dB with no net phase shift. The ratio of R_d to R_z can be used to adjust the unity gain frequency of the preamplifier to a point that provides sufficient phase margin.

R_b is used to fold additional current into the input stage without increasing the needed supply voltage. The feedback loop ensures that the drain voltage of J_2 is held at a bias voltage V_B. To ensure both sets of transistors operate in the saturation region, the bias voltage must be around 2 V which limits the amount of current possible through R_d, particularly at lower supply voltages. Decreasing the bias current through R_d limits the maximum achievable transconductance. To overcome this limitation, extra current is supplied through R_b. The addition

of this resistor has a negligible effect on the circuit noise particularly if the transconductance, g_{J1}, is high. It should be noted that the extra resistance must be selected so as to not increase the capacitance due to Miller effect at the input. The gate to drain capacitance of J_1 is multiplied by the voltage gain from the input node to the drain of J_1, approximately $1 + g_{J_1}/g_{J_2}$, and appears at the input of the preamplifier. By decreasing the current through J_2 and increasing it through J_1, the gain term is increased, leading to a higher effective capacitance at the input. This can be offset using multiple parallel cascode transistors and carefully choosing the ratio of the current in J_1 to J_2.

A. Noise Analysis

The equivalent noise charge (ENC) of the preamplifier determines the smallest signal which can be reliably detected. Signals below the ENC level cannot be distinguished from the background noise and must be discarded. In neutron counting applications, the ENC determines the minimum discriminator threshold and influences the overall system efficiency. Additionally, the preamplifier ENC varies depending on the specific detector being used; thus it is important that the system is optimized for a given detector. To determine the ENC of the circuit shown in Fig. 7, the various noise sources are analyzed.

In general, the total ENC is given by:

$$ENC_T = \sqrt{ENC_d^2 + ENC_f^2 + ENC_o^2} \tag{7}$$

Where the three different contributions ENC_d, ENC_f, and ENC_o represent thermal, flicker and shot noise, respectively [19]. The contribution due to flicker noise is strongly dependent on the transistor technology used. For submicron MOSFET amplifiers, the flicker noise corner, the point at which flicker noise equals the thermal noise, may be several hundred kilohertz [17]. In this case, the flicker noise presents a sizable contribution to the total ENC. Conversely for discrete JFET's, the flicker noise corner may be lower than 10 Hz [26]. For this case, the flicker noise introduces a negligible contribution to the total ENC. Since the designed preamplifier utilizes JFET transistors, ENC_f from (7) will be neglected in the following analysis.

Fig. 8. introduces the various noise sources of the preamplifier, while Table I lists their contributions to the total input referred noise. Since the noise sources add in rms fashion, only the noise from J_1 and the detector leakage current will have a meaningful impact on the total noise. The degree to which the detector leakage contributes to the overall noise is heavily dependent on the shaping time used. A general expression for the equivalent noise charge after shaping is given in [18] and [27] as:

$$ENC_T = \sqrt{(C_d+C_i+C_f)^2 \frac{4kT\gamma}{g_{m1}} \frac{a_w}{\tau_p} + a_p \tau_p 2q(i_d+i_{Gj1})} \tag{8}$$

Here C_d is the detector capacitance, C_f and C_i are the preamplifier feedback and input capacitance, τ_p is the shaping amplifier peaking time, i_d is the detector leakage current, i_{gm1} is the input JFET gate leakage current g_{m1} is the input JFET transconductance, and a_w and a_p are numeric constants dependent on the shaper [18]. Since C_d is large, the current noise component will only have a meaningful contribution to the total noise at long shaping times, as seen in (8).

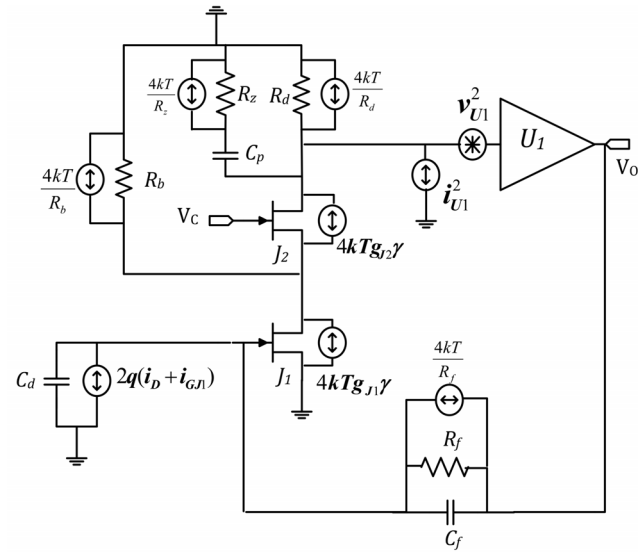

Fig. 8. Noise sources of the preamplifier.

TABLE I
INPUT REFERRED NOISE CONTRIBUTIONS

Component	Input Referred Voltage Noise
J_1	$\frac{4kT\gamma}{g_{m1}}$
J_2	$\frac{4kT\gamma}{g_{m2}g_{m1}^2R_B^2}$
R_D, R_B, R_Z	$\frac{4kT}{(R_D\|\|R_B\|\|(R_Z+\frac{1}{sC_P}))g_{m1}^2}$
U_1	$\frac{V_{U1}^2}{g_{m1}^2R_D^2} + \frac{I_{U1}^2}{g_{m1}^2}$
Detector and JFET Leakage	$\frac{2q(i_d+i_{Gj1})}{s(C_d+C_i+C_f)^2}$
R_F	$\frac{4kT}{R_Fs(C_d+C_i+C_f)^2}$

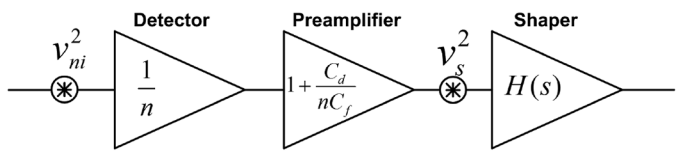

Fig. 9. Shaping amplifier noise gain.

For a large number of detectors in series, the noise of the shaping stage following the preamplifier should also be considered. To determine this contribution, the noise transfer function is plotted in Fig. 9. The preamplifier is represented as a voltage gain block equal to its noise gain. Here C_d is the capacitance of a single detector, C_f is the feedback capacitor, and n is the number of detectors. The series connection is represented as an attenuator with an attenuation factor $1/n$ to account for the signal loss described previously. In order to determine the shaper contribution to the input referred noise, the inverse of the

voltage gain squared from v_{ni}^2 to v_s^2 is multiplied by the shaper noise. Assuming that $C_d/nC_f >> 1$, the input referred noise contribution due to the shaper is given by:

$$v_{ni}^2 = \frac{C_f^2}{C_d^2} n^4 v_s^2 \tag{9}$$

Now, (8) can be revised to include this contribution and account for the series connection.

$$ENC_T = n\sqrt{\left(\left(\frac{C_d}{n} + C_i + C_f\right)^2 \frac{4kT\gamma}{g_{m1}} + n^2 C_f^2 v_s^2\right)} + \sqrt{\frac{a_w}{\tau_p} + a_p \tau_p 2q(i_d + i_{Gj1})} \tag{10}$$

Given that, for high capacitance detectors, C_f is generally greater than 2 pF to ensure fast preamplifier rise time, the contribution due to v_s^2 may become significant as n increases.

In order to assess the effect of v_s^2, measurements were taken using the designed preamplifier followed by two custom built shaping amplifiers. The first shaper was designed using LM6171 op-amps which have input referred noise density of 12 nV/$\sqrt{Hz}$ and are on the borderline of what is considered 'low noise' (generally $<$ 10 nV/$\sqrt{Hz}$). The second shaper was built using the LMP8671 which has a much lower input referred noise density of 2.5 nV/$\sqrt{Hz}$. For a preamplifier with 2.2 pF feedback capacitor and a 16 cm^2 area detector, the noise floor was roughly 5% less using the lower noise shaper.

B. Measurement Results

The preamplifier of Fig. 7 has been built and tested. Six BF862 JFETs were used for the input stage and a low noise AD8021 Op-Amp was used for the second amplification device. The feedback network consisted of an 100 MΩ resistor and 2.2 pF capacitor. The drain current for the input stage was set at 12 mA with 5 mA being supplied by bias resistor R_B. A supply voltage of $+/-5$ V was used and the total power consumption was approximately 150 mW.

To test the preamplifier gain and bandwidth, a capacitor was connected to the input to simulate the detector and a voltage pulse was then applied through a separate test capacitor. Fig. 10. presents the measured response for the unloaded preamplifier, and the preamplifier with 1 nF and 4.7 nF connected at the input. The measured rise times, from 10% to 90% of the steady state value, were 48 ns, 53 ns, and 100 ns, respectively. Additionally there was no measured deviation in amplitude for the 4.7 nF test case, indicative of very high open loop gain.

Fig. 11. presents the measured noise vs. input capacitance in units of keV FWHM. To take this measurement, the preamplifier was connected to a 10 μs pulse shaper and the system gain was calibrated by injecting charge through the test capacitor. The RMS voltage at the output of the shaping amplifier was then measured for various values of the input capacitor and converted to equivalent energy in a Si detector. Applying a line of best fit to the measured data, a noise slope of approximately 4 eV/pF (RMS) was obtained.

Finally the amplifier was characterized when connected to a number of different area detectors. For comparison to our previously published results, data was also taken using an Ortec-142AH preamplifier. Fig. 12. shows the pulse height spectrum taken with a 4 cm^2 detector exposed to a Cf-252 source when using the custom built preamplifier and the Ortec 142AH. Also

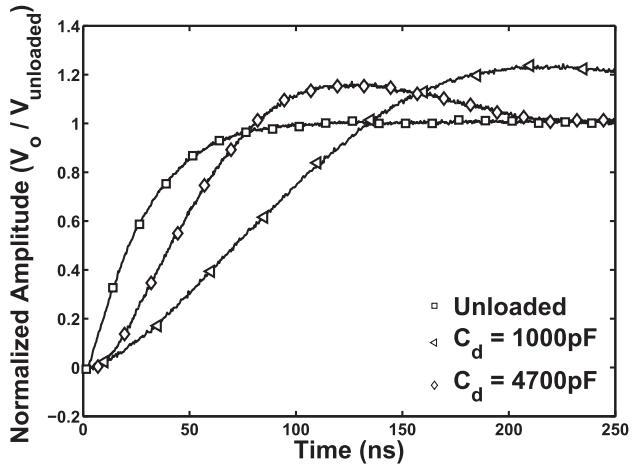

Fig. 10. Preamplifier response to injected charge for various capacitance values. The amplitude of each measurement has been normalized to that of the unloaded response.

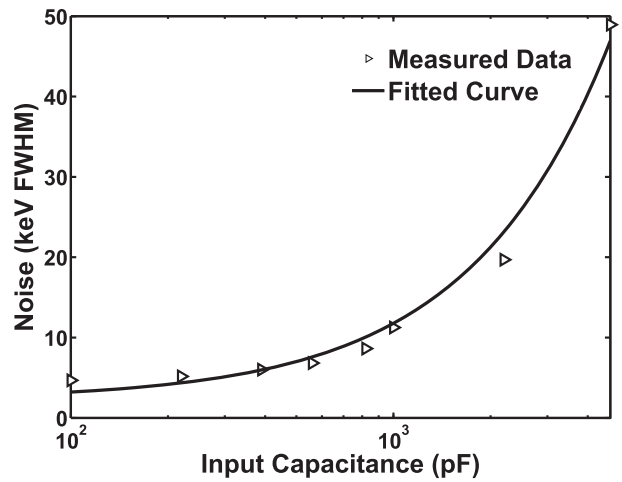

Fig. 11. Measured noise for varying input capacitance with a shaping time of 10 μs.

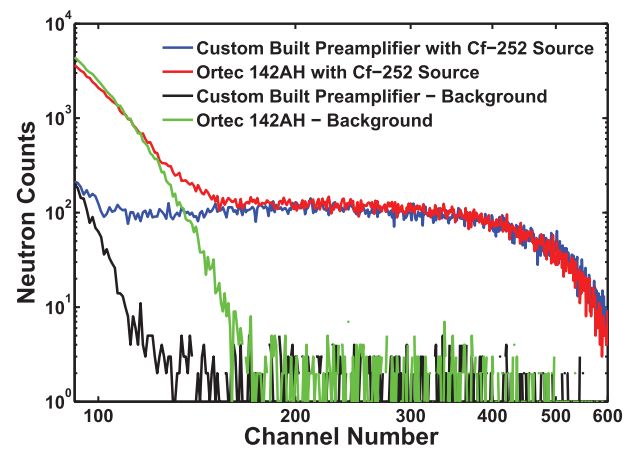

Fig. 12. Measured pulse height spectrum using a 4 cm^2 detector with both the Ortec 142AH and the custom built preamplifier.

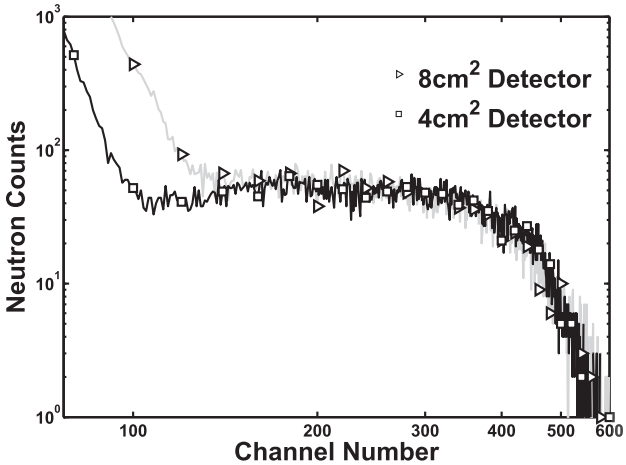

Fig. 13. Measured energy spectrum when detectors of 4 cm^2 and 8 cm^2 were exposed to a Cf-252 neutron source. When measuring the 8 cm^2 detector the signal gain was set to twice that of the 4 cm^2 detector.

TABLE II
MEASURED NEUTRON COUNTS PER SECOND

Detector Area	Ortec 142AH Counts/Second	Designed Preamplifier Counts/Second
16cm^2	292.5	335.5
12cm^2	217.7	254.6
8cm^2	144	168.4
4cm^2	78.3	90.5

shown is the intrinsic background noise taken without the neutron source. In each case, the detectors are set at a precise fixed distance from the source such that the neutron flux is kept constant between each trial. Additionally, the measurement time is kept constant and the gains of the two amplifiers are matched. In order to compare the efficiencies of the two systems, an effective low level discriminator (LLD) is determined using the background noise such that all channels above the LLD only contain neutron counts. The total number of counts above the LLD is calculated and then divided by the measurement time in order to determine the effective counts per second (CPS) when using each amplifier. This process was repeated for a number of different area detectors, the resulting CPS are presented in Table II. It can be seen that the designed preamplifier registered approximately 15% more CPS for an expected efficiency increase of 4.2%, from 28% to 32.2% intrinsic efficiency, over the previously published results [4]. It may be noted that, except for the transition from 4 to 8 cm^2 detectors, based on the data of Table II, the detector efficiency does not decrease as area increases. For example, the ratio of CPS for the 16 cm^2 detector compared to the 8 cm^2 detector was very close to two. However, based on (4) and previous work in [3], the expected ratio would be lower than this measured value. Potential causes for this include variations in the efficiencies of individual detectors as well as variation in the neutron flux over the surface area of the larger detector. Fig. 13. shows the measured energy spectrum for the 4 cm^2 and 8 cm^2 detectors which were used to calculate the CPS listed in Table II. In order to correlate the x-axis of the two measurements, the amplifier gain was doubled when the 8 cm^2 data was taken. The increase in noise floor is clearly visible as the detector area increases.

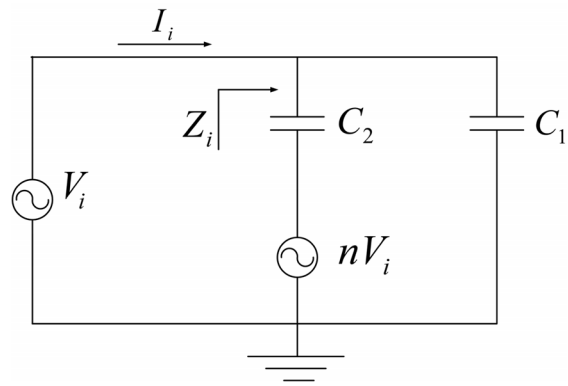

Fig. 14. Idealized implementation of a negative capacitor.

V. PREAMPLIFIER WITH CAPACITANCE CANCELING STAGE

A. Design Principle

As shown in the previous sections, the presence of a large detector capacitance negatively impacts both the noise and response time of the charge sensitive preamplifier. For this reason, a negative impedance converter (NIC) is proposed to cancel out a portion of the detector capacitance. In theory, by using a noiseless NIC to generate a negative capacitor at the preamplifier input, the capacitance seen by the preamplifier decreases, decreasing the noise and increasing the response time. To illustrate the principle of the negative capacitance, let us consider the circuit of Fig. 14. Here, a voltage source supplies current to two capacitors C_1 and C_2. The bottom plate of C_2 is held at a potential which is a multiple of V_i. To determine the impedance seen by the source V_i, we will first find the input current I_i which is given by:

$$I_i = \frac{V_i\left(\frac{1}{j\omega C_2}(1-n)+\frac{1}{j\omega C_1}\right)}{\frac{1}{j\omega C_1}\frac{1}{j\omega C_2}} \tag{11}$$

The input impedance is defined as the input voltage V_i divided by the input current I_i such that

$$Z_i = \frac{1}{j\omega\left(C_2 + C_1\left(1-n\right)\right)} \tag{12}$$

For $n > 1$, the input impedance appears as a capacitor of some value smaller than C_1. Thus, the addition of C_2 and the controlled voltage source V_2 effectively creates a negative capacitor. The right hand side of the circuit in Fig. 14 can then be represented by a single capacitor with value $C_1 - (n-1)C_2$. The controlled voltage source can be implemented in a generic manner using the circuit of Fig. 15, the input impedance of which is:

$$Z_{in} = -\frac{R_2}{R_1}\frac{1}{j\omega C_n} \tag{13}$$

To analyze the effect of the addition of the NIC on the preamplifier noise, consider the voltage noise of the simplified preamplifier circuit given in Fig. 16. It can be shown that the output voltage noise is given by:

$$V_o^2 = V_{ni}^2\left(1+\frac{C_d}{C_f}\right)^2 \tag{14}$$

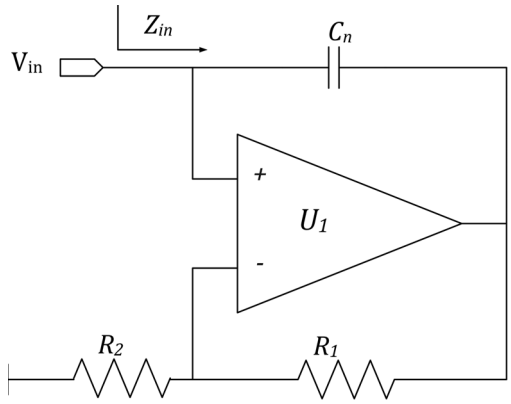

Fig. 15. Generic circuit which implements a negative capacitor.

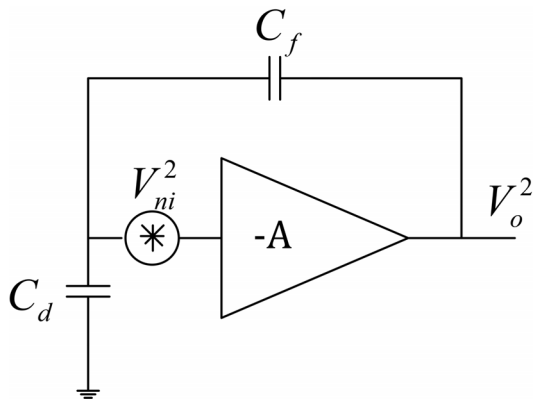

Fig. 16. Noise model of a charge sensitive preamplifier.

which illustrates how the detector capacitance influences the output noise of a charge sensitive preamplifier. In (14), the term multiplying V_{ni}^2 is referred to as the circuit noise gain and, in this example, is equal to the square of the closed loop voltage gain. If the NIC of Fig. 15 is coupled to the preamplifier input, the capacitance seen by the preamplifier is reduced and the total output noise is now given by:

$$V_o^2 = V_{ni}^2\left(1 + \frac{C_d - \frac{R_1}{R_2}C_n}{C_f}\right)^2 \tag{15}$$

From the above it can be seen that the noise gain term is decreased relative to that of a standard preamplifier given in (14). Note that (15) is only valid if the NIC is noiseless, full consideration of the noise due to both the preamplifier and NIC circuit will be presented in the following section.

B. NIC Circuit Design Considerations

The previous section showed that the preamplifier noise may be reduced with an idealized NIC circuit. In order to determine the effectiveness of this technique with a real circuit, it is necessary to calculate the noise introduced by the NIC itself, as well as the frequency range over which the input impedance acts as a negative capacitor.

To determine the effective bandwidth, the frequency dependent input impedance of the circuit of Fig. 15 is derived. It will be assumed that the amplifier U_1 has a frequency dependent gain

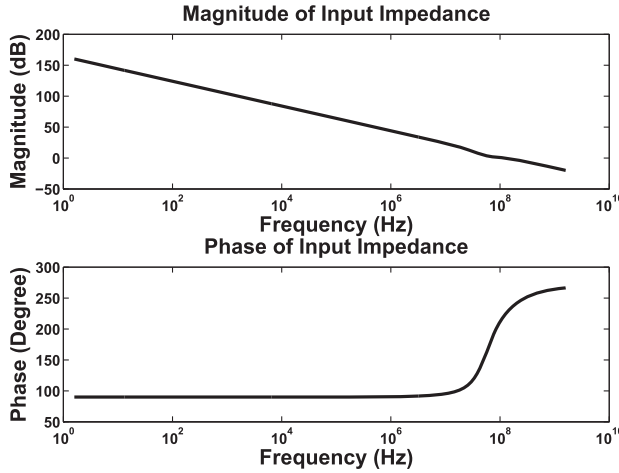

Fig. 17. Magnitude and phase of the NIC input impedance generated using 16. Parameters used were, $R_1 = R_2 = 100\ \Omega$, $C_p = 50$ pF, $C_n = 1$ nF, $a_0 = 10^5$, and $\omega_b = 1$ kHz.

$a(j\omega)$, a dominant pole at ω_b and a DC gain a_0. Also considered is the effect of any parasitic capacitance C_p at the inverting terminal of U_1. The frequency dependent input impedance can be given as:

$$Z_{in} = -\frac{1}{j\omega C_n} \times \frac{R_1 + R_2 + R_1R_2C_pj\omega + a(j\omega)R_2}{R_1 + R_2 + R_1R_2C_pj\omega - a(j\omega)R_1(1 + R_2C_pj\omega)} \tag{16}$$

Which at low frequency simplifies to (13). Fig. 17. plots the magnitude and phase of (16) for a set of representative values. It can be seen that at some frequency, the phase of the input impedance will shift upward from the idealized value of 90°. Additionally the magnitude response experiences a dip at higher frequencies which is due to the parasitic capacitor C_p. If the parasitic capacitor is ignored then a metric may be introduced to estimate the frequency at which the phase deviates fully 90° from the ideal response.

$$\omega_{90^\circ} = a_0\omega_b\frac{\sqrt{R_1R_2}}{R_1 + R_2} \tag{17}$$

Equation (17) shows that the maximum bandwidth is achieved when R_1 equals R_2.

Equation (16) is used to determine the effect the NIC has on the stability of the preamplifier. The preamplifier feedback factor β is given by the impedance divider formed by the detector capacitance C_d in parallel with the NIC input impedance Z_{in} and the feedback capacitor C_f.

$$\beta = \frac{C_f}{C_d + C_f + Z_{in}} \tag{18}$$

Note that for $Z_{in} = 0$, β^{-2} is equal to the noise gain of the circuit V_o^2/V_{ni}^2 as given in (14). It is also equivalent to the noise gain given in (15) with Z_{in} set to (13).

Substituting for Z_{in} by (16), it can be seen that the feedback factor has a pole at

$$\omega_p = \frac{\omega_b a_0 R_2(C_d + C_f - C_n\frac{R_1}{R_2}) + (R_1 + R_2)(C_d + C_n)}{(R_1 + R_2)(C_d + C_n)} \tag{19}$$

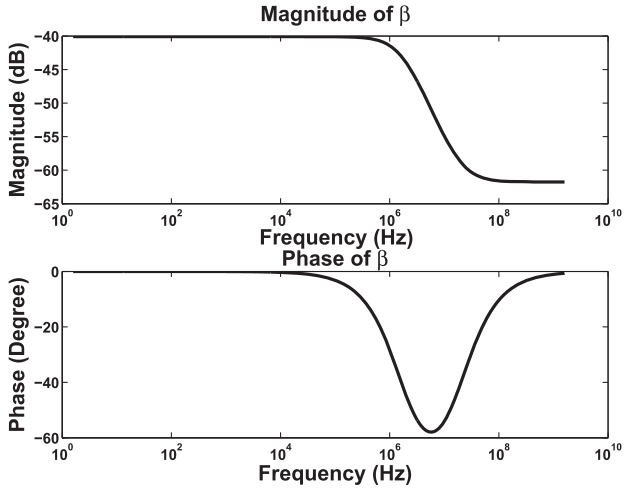

Fig. 18. Magnitude and frequency of the preamplifier feedback factor with negative capacitance circuit. Parameters used were; $C_d = 1$ nF, $C_f = 1$ pF, $R_1 = 100\ \Omega$, $R_2 = 400\ \Omega$, $C_n = 245$ pF, $a_0 = 10^5$, and $\omega_b = 1$ kHz.

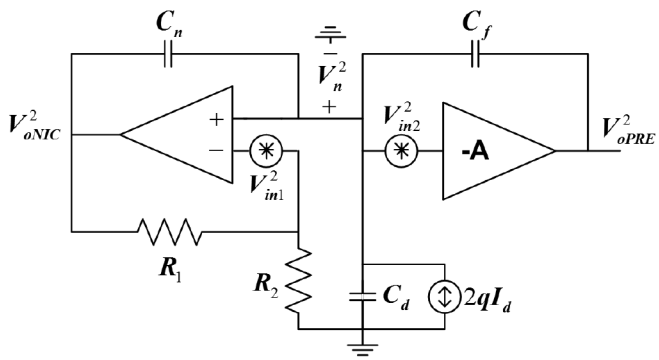

Fig. 19. Noise model accounting for the coupling of NIC noise to the preamplifier output.

A zero at

$$\omega_z = \frac{\omega_b a_0 R_2}{R_1 + R_2} \tag{20}$$

With a DC value of

$$A_\beta = \frac{C_f a_0 R_2}{a_0 R_2 (C_d + C_f - C_n \frac{R_1}{R_2}) + (R_1 + R_2)(C_d + C_n)} \tag{21}$$

Combining (19)–(21) into a single equation yields

$$\beta(j\omega) = \frac{A_\beta (1 + \frac{j\omega}{\omega_z})}{1 + \frac{j\omega}{\omega_p}} \tag{22}$$

Fig. 18. plots the magnitude and phase of β for a set of representative values. The frequency dependence of the NIC input impedance introduces an extra pole and zero in the preamplifier transfer function which degrades the phase margin in the range between ω_p and ω_z. Additionally, as seen in Fig. 18, β decreases at high frequencies which leads to an increase in the preamplifier noise gain. The bandwidth of the shaping stage preceding the preamplifier should be sufficiently below the frequency at which the noise gain increases.

It is also necessary to determine the amount of noise which will be coupled from the NIC circuit to the preamplifier. A model of the various noise sources of the coupled amplifiers is shown in Fig. 19. First consider the contribution of V^2_{in1} to

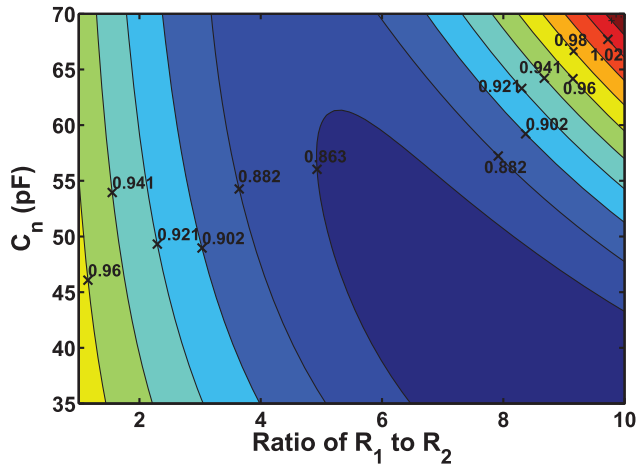

Fig. 20. Preamplifier noise with NIC connected calculated using (25). Parameters used were $V^2_{in1} = 2V^2_{in2}$, and $C_d = 1$ nF. The plot is normalized to a preamplifier with input referred noise V^2_{in2} with the same feedback and detector capacitance.

V^2_{oPRE}, the NIC noise gain is given by the difference in the feedback factor of the negative and positive feedback paths and the output noise due to V^2_{in1} can be given as

$$V^2_{oNIC} = V^2_{in1}\left(\left(1 + \frac{R_1}{R_2}\right)^{-1} - \left(1 + \frac{C_n}{C_d}\right)^{-1}\right)^2 \tag{23}$$

A portion of the noise is fed back to the non-inverting terminal of the NIC, leading to a noise voltage V^2_n

$$V^2_n = \left(1 + \frac{C_n}{C_d}\right)^{-2} V^2_{oNIC} \tag{24}$$

This voltage is coupled to the input of the preamplifier and the total input referred noise is therefore $V^2_n + V^2_{in2}$. Combining (23), (24), the preamplifier noise gain given in (15), and the input referred noise of the preamplifier V^2_{in2}, yields (25) as the total preamplifier output noise. Fig. 20. plots (25) for varying values of C_n and the ratio of R_1 to R_2 for C_d of 1nF. Additionally V^2_{in1} was set to be twice that of V^2_{in2}. The plot is normalized to (14) with $V^2_{ni} = V^2_{in2}$ and the same detector and feedback capacitance. It is also assumed that the NIC bandwidth extends well past the preamplifier bandwidth which allows for direct normalization of the two equations. From Fig. 20 it can be seen that up to a 15% decrease in noise is possible when using the NIC circuit.

$$V^2_{oPRE} = \left(V^2_{in1}\left(\left(1 + \frac{R_1}{R_2}\right)^{-1} - \left(1 + \frac{C_n}{C_d}\right)^{-1}\right)^2 \times \left(1 + \frac{C_n}{C_d}\right)^{-2} + V^2_{in2}\right)\left(1 + \frac{C_d - \frac{R_1}{R_2}C_n}{C_f}\right)^2 \tag{25}$$

The previous analysis neglected the contribution of shot noise in the detector to the total preamplifier noise. For a standard preamplifier, the detector noise current, $2qI_d$ in Fig. 19, circulates in the detector capacitance generating voltage noise at the input equal to:

$$V^2_{nI_d} = 2qI_d\left(\frac{1}{\omega C_d}\right)^2 \tag{26}$$

Multiplying by the preamplifier noise gain (14), gives the voltage noise at the output:

$$V_{noI_d}^2 = 2qI_d\left(\frac{1}{\omega C_f}\right)^2 \tag{27}$$

(27) is valid assuming that the input impedance of the preamplifier is large and C_d is significantly larger than the feedback capacitor C_f. Adding the NIC circuit to the preamplifier input provides a parallel impedance, C_n, for the noise current to flow in. Accounting for this, the input referred voltage noise due to detector leakage is given by:

$$V_{nI_d}^2 = 2qI_d\left(\frac{1}{\omega\left(C_n + C_d\right)}\right)^2 \tag{28}$$

Additionally, the noise gain of the preamplifier is lowered, as shown in (15), and the voltage noise at the output is given by:

$$V_{noI_d}^2 = 2qI_d\left(\frac{C_d - \frac{R_1}{R_2}C_n}{\omega\left(C_n + C_d\right)C_f}\right)^2 \tag{29}$$

(29) is always less than (27) implying noise due to detector leakage current is decreased with the addition of the NIC circuit.

C. NIC Implementation and Measurements

The circuit of Fig. 21 has been designed to implement the NIC based on the aforementioned design criteria. A differential JFET amplifier was used as a very low noise input stage. Devices Q_1 and Q_2 are biased at the same current as the preamplifier JFET's. This was done in order to have the NIC input referred voltage noise approximately twice that of the preamplifier such that the assumptions used to generate Fig. 20 are accurate. Resistor and capacitor R_z and C_p are used to stabilize the circuit at high frequencies. Finally, BJT's Q_5 and Q_6 provide a means to cancel any voltage offset due to mismatch in the input JFET's.

As shown in the previous section, it is expected that the preamplifier bandwidth and rise time will be varied by the magnitude of the negative capacitance. To test this assumption, the rise time of the preamplifier was measured for varying values of the negative capacitance and compared to the rise time with the NIC disconnected. Fig. 22. presents the measured rise times for negative capacitance values of 400, 600, and 800 pF. In each case, a 1.1 nF capacitor was connected at the input to simulate a detector. It can be seen that as the value of the negative capacitor increases, the preamplifier rise time decreases as expected. For very large values of the negative capacitor, the preamplifier phase margin is eroded as indicated by the significant ringing present in the 800 pF test case of Fig. 22.

Using Fig. 20 as a guideline, the NIC was configured such that the noise minimum could be attained. Two configurations were tested, with C_n of Fig. 21 set to 47 pF and 68 pF. From Fig. 20 it was expected that a 15% improvement would be attained when the total negative capacitance (C_n multiplied by the ratio of R_1 to R_2) was around 400 pF and 500 pF for C_n equal to 47 pF and 68 pF respectively. Fig. 23. presents the measured noise for the two setups using a 3 and 5 μs pulse shaper. In each case, the

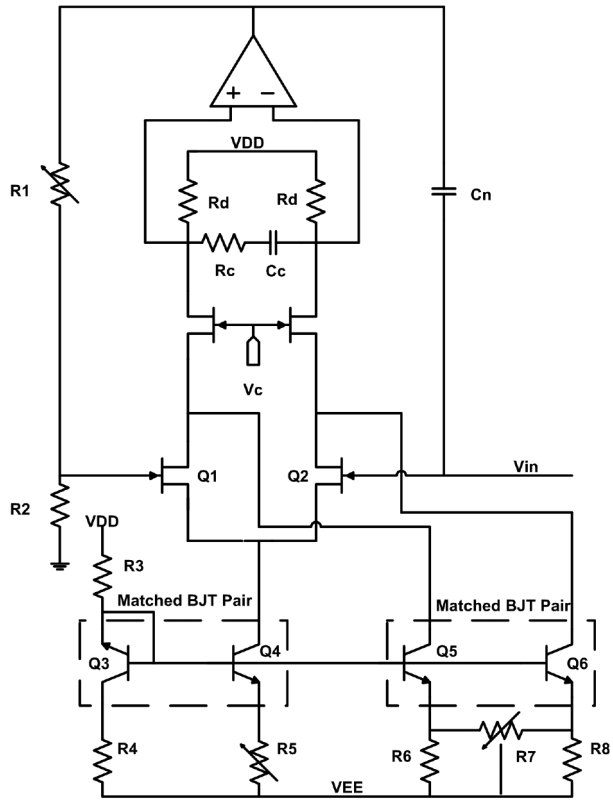

Fig. 21. Circuit implementation of the negative impedance converter.

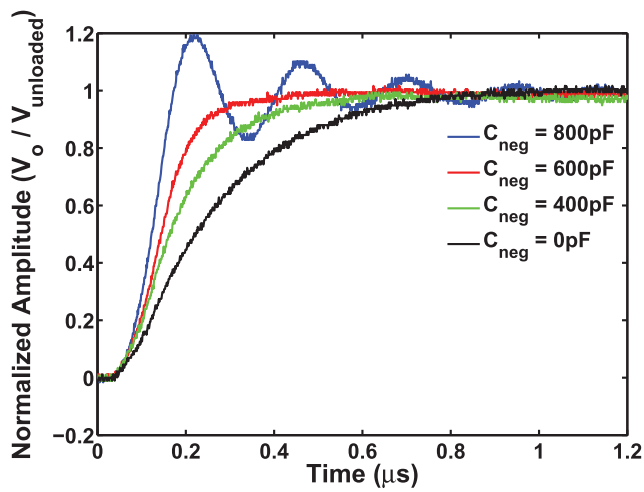

Fig. 22. Preamplifier rise time with various negative capacitance settings. In each case the input capacitance was set at 1.1 nF. The amplitude of each measurement was normalized to that of the unloaded response.

measurements were normalized to the noise of the same preamplifier and shaper with the NIC disconnected. When using the 5 μs shaper a greater than 15% decrease in noise is obtained, whereas the improvement is slightly less with the 3 μs shaper. The discrepancy between the two cases is due to the increase in noise gain at higher frequencies explained previously. Faster shaping times require greater bandwidth so the increased high frequency noise will be attenuated less as the shaping time decreases. Comparing the measured data in Fig. 23 to the predictions of Fig. 20, it can be seen that the attained noise minimum

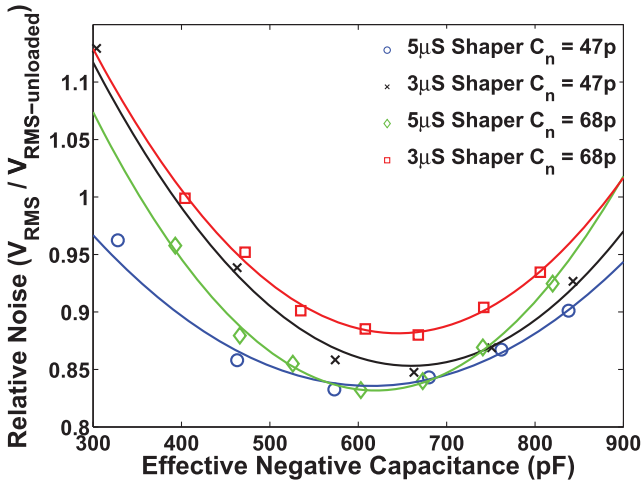

Fig. 23. Measured noise of the preamplifier with NIC circuit after shaping. The measurements are normalized to the same preamplifier with the NIC disconnected. For each case the input capacitance is set at 1.1 nF. Solid lines indicate the best fit curve to the measured data.

is at a somewhat higher negative capacitor value than predicted. Additionally, the improvement in noise is slightly greater than expected. Both of these effects are most likely due to the NIC input referred noise being less than twice that of the preamplifier input referred noise, which was the assumption used to generate Fig. 20. In this case, the minimum predicted by (25) will be shifted towards larger values of the negative capacitor.

VI. Conclusions

Design considerations for applications involving high capacitance detectors are presented. In particular, the effect of arraying multiple detectors is addressed and relationships are given for calculating the noise increase due to either parallel or series connection. Formation of large area detector arrays with superior efficiency has been shown to be possible through combining detectors in a series manner. Since the signal is reduced with the series connection of detectors, a revised ENC equation has been presented to account for the signal reduction and increased noise contribution from the shaping stage following the preamplifier. The techniques outlined in this paper have been used to design a low noise preamplifier which has been tested with a variety of detector arrays up to 16 cm^2 in area. The designed circuit has been shown to have a low noise floor, and fast response time, for detector capacitances up to several nano-Farads. Additionally, using the presented preamplifier, we have measured a 15% increase in thermal neutron detection efficiency of our honeycombed SSND compared to previous publications. Compared to commercially available preamplifiers optimized for high capacitance detectors, such as [5], [6], the designed preamplifier achieves a comparable noise performance with a power consumption less than half that of the commercially available units for neutron detectors with capacitance exceeding or equal to 1 nF. Additionally, the preamplifiers have been designed on 1 inch square PCB's giving them a very compact form factor. The improvements in power consumption and size for the developed electronics compared to commercial solutions presents a major step towards enabling battery powered, and portable solid-state detection systems.

Finally, a novel preamplifier topology, utilizing a NIC for lower noise operation, is presented. Design considerations and noise modeling of the NIC coupled to a charge sensitive preamplifier are presented and have been confirmed through measurement. Experimental results have shown that a 15% reduction in noise is possible by utilizing the described techniques.

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