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Interposer Technologies for High-Performance Applications

Ahmad Usman, Etizaz Shah, Nithanth B. Satishprasad, Jialou Chen, Steven A. Bohlemann, Sajjad H. Shami, Ali A. Eftekhar, and Ali Adibi

***Abstract*— This paper explores the current state of the art in silicon, organic, and glass interposer technologies and their high-performance applications. Issues and challenges broadly encompassing electrical, mechanical, and thermal properties of these interposer technologies are discussed along with the proven and under research solutions pertaining to these challenges. An evaluation of high-performance applications for these three technologies provides a useful insight into the role of interposers for such applications. This paper is an effort to evaluate and compare the viability of silicon, organic, and glass interposer technologies for high-performance applications. This paper also discusses the future trends, promising advancements, and market requirements with special emphasis on glass interposer technologies as evaluated to be the most viable option for the future high-performance applications.**

***Index Terms*— Glass interposers, high-performance applications, interposers, organic interposers, packaging, silicon interposers.**

NOMENCLATURE

APX	Advanced package-X.
BEOL	Back end of line.
BWD	Bandwidth density.
CPW	Coplanar waveguide.
CST	Computer simulation technology.
CTE	Coefficient of thermal expansion.
CTT	Copper trace transfer.
DRAM	Dynamic random access memory.
EIC	Embedded interposer carrier.
EMIB	Embedded multidie interconnect bridge.
FEM	Finite-element modeling.
FOWLP	Fan-out wafer-level packaging.
FPGA	Field programmable gate array.
FR-4	Flame retardant-4.
GPU	Graphics processing unit.
HBM	High bandwidth memory.
HMC	Hybrid memory cube.
IC	Integrated circuit.
IoT	Internet of Things.
i-THOP	Integrated thin-film high-density organic package.
JEDEC	Joint Electron Device Engineering Council.
KGD	Known good die.
LCP	Liquid crystalline polymers.
MEMS	Micro electromechanical systems.
MFI	Mechanically flexible interconnect.
PDN	Power delivery network.
PTE	Photo trench etching.
RDL	Redistribution layers.
RF	Radio frequency.
RFIC	Radio frequency integrated circuit.
RFID	Radio frequency identification.
SAP	Semiadditive plating.
SOP	System on package.
TGV	Through glass via.
TPV	Through package via.
TSV	Through silicon via.
VIA	Vertical interconnection access.
WLP	Wafer-level packaging.

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I. INTRODUCTION

THE demand for ultraminiaturization and megafunctional smart systems has been rapidly increasing. Different SOP realizations have been envisioned and proposed by researchers. Many different material platforms are under consideration for a complete SOP realization. This ultraminiaturization and megafunctionality has led to the increased demand for high density and high bandwidth interconnections, especially between logic and memory chips. The concept of 2.5-D and 3-D IC integration and package is a key component in realization toward a complete high-performance SOP solution and the concept itself is incomplete without "interposers."

An "interposer" is an electrical interface (substrate) used for routing between one socket or connection to another socket or connection. In a broader sense, the purpose of an interposer is to spread a connection to a wider pitch or to reroute a connection to a different connection with a different pitch. In the packaging domain, it is an electronic substrate having through VIA interconnections at the same input–output (I/O) pitch as an IC on one of its sides (fine I/Os) and the same I/Os as of packages or boards on the other side (coarse I/Os compared to IC side), to facilitate better integration of multiple chips in a package [1].

Interposers are mainly used for high performance especially high-bandwidth applications, e.g., connecting logic chips

to memory chips. This is made possible by the ultrahigh number of I/O connections available using interposers. Similarly, these are used to develop heterogeneous integration of multiple ICs on a single platform/package. Interposers also allow dense 2-D and 3-D integration of ICs on a package or board especially when it comes to extremely small I/O pitch and line spacing in the ICs (less than 40 μm). The trend is more toward high-performance applications, which, in a broader sense, require these current interposers technologies to have high I/Os at an extremely fine pitch, high dimensional stability, extremely low warpage, high temperature stability, and low CTE mismatch.

In this paper, we discuss the role of silicon, organic, and glass interposers toward realization of high-performance applications. Section II provides a detailed overview of silicon interposer technologies for high-performance applications, while Sections III and IV provide similar detailed literature reviews for organic and glass interposers. Section V discusses the future trends of these technologies, and Section VI provides a concise conclusion of this paper.

II. Silicon Interposers

Increases in bandwidth, reduced latency, high-performance, and lower power consumption are the major thrusts behind the advancements in electronics. The silicon interposers have been used to help progress toward this goal. A silicon interposer is the central component in realizing 2.5-D and 3-D packaging. A key advantage of the silicon interposer is its fine-pitch wiring, which results in progress toward the goal of high bandwidth off-chip signaling for the chips assembled on the silicon interposer. Silicon interposers were developed in the 1980s by IBM and Bell Labs to allow the designers to put dies next to each other and pursue the potential of high BWD signaling, low-latency configuration, and heterogeneous integration of logic, memory, microelectromechanical systems, and optoelectronics [2], [3]. To analyze interposer material technology, it is important to consider the mechanical, thermal, and electrical characteristics of the resulting device.

Mechanical issues in silicon interposers mainly arise with thermal stresses during wafer processing, TSV formation, and misalignment of TSVs. The CTE mismatch between bulk silicon and through silicon (e.g., copper) vias is another reason of the thermal stress, which can become worse with larger and deeper via structures [4]. In typical TSV formation, these stresses can cause structure and substrate cracking. Different FEM-based techniques have been developed to understand and mitigate these thermomechanical stresses in silicon [5]. To practically address the thermomechanical stress conditions, different fabrication processes have been developed. One such process called “trenched air-gap etching” is widely employed. In this process, trenches are fabricated by silicon etching around copper TSV to relieve thermomechanical stresses across the TSV structures [6]. MFIs are being used to improve alignment for multiple silicon interposers setup [7], [8]. As a result, better alignment between interposer and package substrate is achieved. This compensates for nonplanarity during packaging, and allows for movable interposer configurations

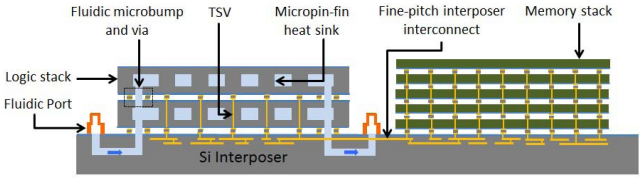

Fig. 1. High-performance computing system based on a silicon interposer platform utilizing microfluidic cooling. A side view of a logic stack and a memory stack heterogeneously integrated on a silicon interposer [3].

and a platform for dense electrical and photonic links between interposers without using package-level interconnects [9].

Thermal management is a major issue for high-performance devices. Power consumption in different on-chip components results in localized temperature variation on the device. Silicon interposer being a carrier component of these devices is directly affected by this variation in temperature gradient. It has high conductivity and the CTE is approximately matched to the connected silicon-based ICs and components. The localized variation in temperature results in different thermal-related stresses on the silicon interposer itself and can cause thermal runaway of the device. Therefore, the access buildup of heat needs to be countered using different effective heat removal and thermal management mechanisms. A frequently employed mechanism is the formation of distributed TSV arrays for effective heat dissipation across the silicon interposer. FEM-based simulation analysis and fabrication of this mechanism showed effective thermal management in silicon interposers [6], [10]–[12]. It was also observed that the thermal stresses in silicon interposers are much lower as compared to the organic interposers [6]. A similar approach for thermal management employs ultrahigh I/O interposers, which do not require TSVs in the logic IC as in the 3-D stack [13]. A major drawback of these techniques is the thermal stress resulting from the fabrication of such devices.

Recently, a microfluidic cooling-based novel approach for thermal management of silicon interposer has been proposed. The scheme is much more advantageous compared to only air-based cooling mechanism for silicon interposer-based designs. The proposed technique results in better temperature control and thermal isolation as compared to its counterpart technologies [3]. It is a logic die with an embedded microfluidic heat sink and fluidic I/Os on the silicon interposer. The fluid/coolant is pumped through the fluidic channels in the interposer and is routed to the heat sink through the fluidic microbumps and vias [3]. This allows for shorter interconnects between dies resulting in improvement in signals all while maintaining low temperature. An example of silicon interposer platform using microfluidic cooling is shown in Fig. 1.

Electrical performance is another important parameter for silicon interposers. Silicon is a low-resistivity substrate and TSVs are key toward realization of silicon as an interposer material for 2.5-D and 3-D packaging. Electrical signals are allowed to transmit vertically through these TSVs, and for high-frequency applications, the loss is considerably high, which results in poor RF performance [6], [14]. The capacitance of these TSVs also increases with the increase in TSV

diameter, which adds to poor RF performance [15]. Design parameters, such as shape, length, diameter, pitch, oxide liner thickness (dielectric constant), material properties, bump size, and shape, are optimized for TSVs to achieve the desired high-efficiency performance. Detailed design evaluations from dc to higher frequencies have been performed to improve the electrical performance parameters, such as capacitance, inductance, resistance, crosstalk, insertion loss, and return loss for these TSVs [6], [15].

It was observed that the reduction in the size (thickness) of the silicon interposer (length of TSV) improves the transmission coefficient for the TSVs, thus improving the overall RF performance. It was also observed that having coaxial shape TSVs also improves the transmission coefficient. Such TSVs require smaller inner conductor diameter, high-K dielectric material in between the inner and outer conductor and thinner silicon substrates for high-efficiency performance. These coaxial-type TSVs also result in better performance in low-resistivity silicon substrate [14]. Performance can also be increased by using high-resistibility silicon substrates, but those substrates are expensive and have different fabrication issues [6]. Polycrystalline silicon has also been used as interposer substrate material instead of the conventional crystalline silicon substrate. TSVs, RDLs, and CPW lines were fabricated and characterized. It was observed that the insertion loss is much lower in polycrystalline silicon compared to crystalline silicon [16].

Another novel approach to address the electrical parasitics is to use polymer-clad TSVs, which results in significant dielectric capacitance reduction [17]. Furthermore, optical TSVs can be created along with the polymer-clad TSVs using almost similar fabrication methodologies. These optical TSVs are capable of handling much more data rates compared to their electrical counterparts and are considered extremely useful in high-performance and high-bandwidth communication applications [17].

Power delivery is a major concern in silicon interposer-based high-performance applications. Fabrication of TSVs, RDLs, and longer power delivery paths between logic and memory components results in crosstalk and resonance effects, which lead to loss of information signal. These effects are more dominant at higher frequencies and are a major concern for high-performance applications. Different solutions for these problems have been proposed in the literature. One method includes optimized multiple metal layers for power and ground integrated within the interposer. This results in lower resistance path for the signals [13], [18]. Embedded decoupling capacitors to reduce the resonance and switching noise effects have been proposed to improve the performance of PDNs over the silicon interposers [19], [20]. FEM-based techniques and methods showing interesting correlation with fabricated devices have also been reported in the literature, which can be employed to optimize electrical performance of silicon interposers [21], [22].

One of the few high-performance commercial products using the silicon interposer with TSVs was the Xilinx's Virtex-7 2000T FPGA. Apart from the silicon interposer technology, the new packaging technology employed in this product resulted in an FPGA that allowed reduced system cost and increased performance with lower power consumption [23]. There have been a number of demonstrations for different high-performance devices and applications such as a 3-D HMC with a bandwidth of 128 Gb/s, compared to 12.8 Gb/s for DRAM applications demonstrated by Micron [24], [25]. A similar 3-D HBM device has been demonstrated by SK Hynix for high-performance graphics and network applications [26], [27], and recently, AMD has announced that it has created the world's first ever 3-D IC combining DRAM and GPU with TSVs and silicon interposer [28].

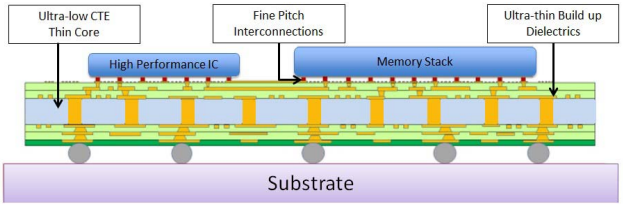

Fig. 2. Concept of ultrathin low-CTE organic interposer [33].

Silicon interposers are well positioned with current manufacturing and supplier environments as silicon is an established material technology used in many industries. Its high-performance characteristic is central to its continued use. The costs for silicon interposer fabrication are still relatively high with bulk of the cost related to the Damascene process, front pad and backside bumping, TSV fabrication, and via filling (∼69%) [29]. Extensive work has been going on to lower the costs and explore different materials to achieve this.

III. Organic Interposers

In the search for low-cost interposer technology, organic is one promising candidate. It is typically manufactured by the conventional wet etching process, which is comparatively easy and low-cost compared to silicon and glass interposer technologies [30]. Organic interposers also have the added advantage of a stable supply chain over the silicon and glass technologies [29]. They have the capability to solve certain problems faced by silicon and glass interposer technologies, but it will be quite hard to effectively balance the mechanical, thermal, and electrical performance issues for a complete SOP high-performance application.

Mechanical reliability in organic interposers results from different material and processing aspects. Fortunately, fabrication stability has been improved for organic interposers to produce fine-pitch patterns compared to silicon interposer. The minimum line and spacing of 2 μm has been achieved in the traditional organic multichip package allowing some organic interposers-based functionalities, but below this value, it is still a constraint [31]. This restricts extremely dense integration and number of I/Os on an organic interposer compared to silicon or glass interposers.

Organic interposers consist of a low CTE and high modulus organic material as a core, while dielectric layers are buildup over the core substrate, as shown in Fig. 2. These are inherently more rigid as compared to silicon and glass. Therefore, when a chip is mounted on an organic interposer,

either using wire-bonding or flip-chip technique, the solder balls on the package will give some stand-off to the components that will result in improved reliability [31], [32]. The organic interposers also allow some flexibility toward better reliability of solder joints. However, this flexibility may lead to an increased risk of connection failure inside packages. Layer-to-layer misalignment during copper-polymer RDL fabrication owing to thermomechanical instability issue causes warpage during chip assembly on thin core organic substrates [33].

Thermal management is critical for all types of interposers, especially when thermal conductivity of most organic materials is relatively low. The heat dissipation for organic interposer is supposed to be worse than that of silicon and glass interposers. To obtain better thermal efficiency, "thermal vias" could be a solution because of its much higher conductivity like in silicon and glass interposer technologies [34]. Relocating thermal vias and increasing the number of the vias can be considered as an option for thermal management in organic interposers. For these thermal vias, it is vital to analyze the energy load scale of each heat source. Lasers are the only viable option to etch through organic vias [29]. The use of heat sink close to heat generating sources on the interposer can also be a viable option [34]. Thermal simulation technologies are now quite mature, and commercial finite element software, such as FloTHERM, Icepak, Fluent, CST, and COMSOL, have been extensively used in microsystem cooling and thermal simulations [35].

Organic interposers have high CTE mismatch compared to silicon and glass, resulting in a severe CTE mismatch between a die and the interposer substrate [36]. It is extremely important to buffer the differences in thermal expansion between different materials. Using low CTE and high modulus organic materials is necessary in order to mitigate the CTE mismatch. On the other hand, thermal problems also lead to reliability concerns because of the CTE mismatch and warpage limits [37], [38]. These issues can be easily resolved and materialized by employing low CTE, high strength, and modulus organic materials. A core/polymer doping using glass fiber has been considered to reinforce organic interposers in this aspect [33]. Ultrathin low-CTE organic interposer has also been reported in [33], which is an effort to solve the warpage issues and to achieve the goal of 40-μm I/O pitch with less than 200-μm-thick organic interposers.

A typical organic material (consisting of epoxy and filler) has lower relative dielectric constant than silicon dioxide [39]. Such organic property potentially takes electrical advantage of circuit design under condition of keeping characteristic impedance on transmission line with small signal transmission loss. By minimizing die–die spacing for shorter communication path, the challenges from increased signal loss and dispersion at long signal length can be further solved. Moreover, the organic interposer also has the potential to become the high-density interposer substrate [31]. Switching noise, crosstalk interference, and resonance effects are also major problems for realizing PDNs over organic substrates. Thin-film and embedded decoupling capacitors have been employed to mitigate these issues [40].

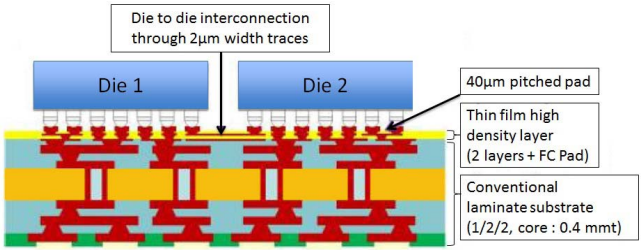

Fig. 3. Schematic cross-sectional image of i-THOP [41].

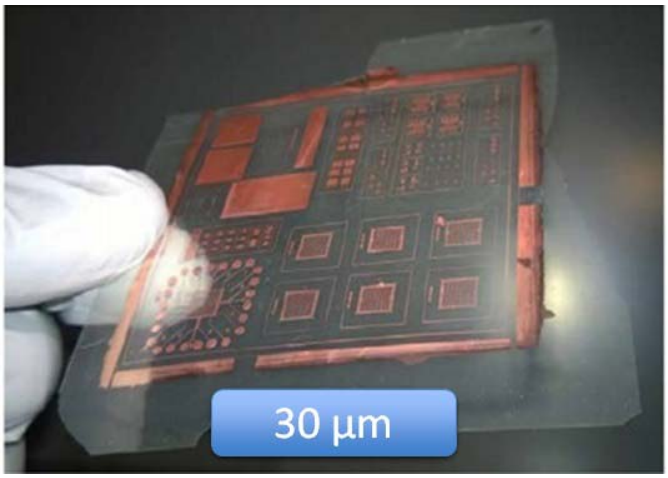

Fig. 4. Demonstration for 30-μm-thick glass interposer developed in collaboration with the Georgia Institute of Technology (Image courtesy of Schott Glass).

The 2.5-D and 3-D packaging of ICs for high-performance applications, such as logic-memory integration, large CPUs/GPUs, and application specific integrated circuit, can benefit from these advancements in the organic interposer technology. Demonstrations using organic interposer technologies with line/space (L/S) of up to 5 μm and through via holes of less than 30 μm, such as APX from Kyocera SLC Technologies and i-THOP (organic interposer i-THOP) from Shinko Electric Industries, have been reported recently [41], as shown in Fig. 3.

High-performance RF applications are available over organic substrates, and organic substrates, such FR-4, LCPs, and laminates by companies such as "Rogers Corporation," have given numerous demonstrations of high-performance RF applications [42]. However, organic interposers need to replicate such applications for the next generation of high-performance applications.

IV. Glass Interposers

Along with silicon and organic, glass has been proposed as a highly efficient material for high-performance interposer applications (Fig. 4). Glass as a substrate material for interposer applications allows excellent dimensional stability, closely matched and tailorable CTE to the silicon die, high thermal stability, high electrical resistivity, low panel cost, and availability in large ultrathin panel sizes [36]. These properties have made glass material to be considered among the emerging substrate technologies for interposers.

Apart from these benefits, glass-based interposer presents numerous challenges toward complete realization of

high-performance systems. Glass is amorphous in nature, which results in surface defects during processing. Localized cracking and complete substrate cracking have been observed during glass processing. The thermal conductivity of glass is poor as compared to silicon. This results in substrate heating, which causes decrease in overall performance of high-performance devices. The formation of extremely small-diameter and low-pitch TGVs or TPVs is another challenge, and the formation of these vias also decreases the overall strength of glass substrate [43].

In order to exploit the advantages and to mitigate the challenges, different mechanisms and techniques have been proposed in the literature. The cost and performance issues have been addressed by a panel-based approach. Large panels of glass substrates are manufactured and used for processing, resulting in eight times yield compared to silicon interposers [36]. Different dry and wet etching techniques along with laser-based etching are employed for TGVs formation. It was found that excimer-based lasers are best suited for almost 90° via drilling. RXP4 polymer has been employed to reduce the surface defects during the laser drilling/etching process and results in a crack-free via drilling. It was also observed that the use of RXP4 polymer also resulted in better vertical ablation of the vias compared to the case when it is not used [36]. TGVs fabricated up to 10 μm diameter can be found in the literature [44]. TGVs of finer diameters are still an important challenge faced by the researchers.

Metallization of glass is another key aspect in realizing high-performance applications using glass interposers. SAP layer techniques are perceived to be limited to 5 μm (width of metal/conductive traces), but demonstrations for smaller sizes can also be seen in the literature. A similar approach is employed for metallization with electroless copper seed layer and electroplating for the fabrication of up to 1-μm-wide traces. Embedded traces up to 1.5 μm have also been reported in the literature for different high-performance applications using different process flows, such as CTT and PTE [45].

In order to have RDL on glass, sputtering is the most commonly applied technique. These RDLs provide lateral interconnection between different components on the glass interposer, thus making a complete set of 3-D PDN and signal network along with TGVs, which are responsible for vertical power and signal delivery. Copper is the most commonly used metal in this process. Titanium adhesion layer is used for copper deposition over glass. A polymer layer is also used as an adhesive layer for deposition of copper over glass substrate. TGV metallization/filling is usually done in a two-step process. A seed layer formed (electroless copper deposition or sputtering) and copper electroplating is done to complete via formation [36].

Fabrication of TGVs and RDLs is required for the PDN over a glass substrate. This causes resonance issues in glass substrate, which results in loss of electrical signal at certain resonant frequencies. These frequencies are more dominant in the high frequency regime and, therefore, are unacceptable for high-performance applications. Different techniques to mitigate the effect of these resonances have been proposed. Optimized signal and ground layers are deployed in the substrate along with TGVs (shielded and unshielded) for mitigating the effect of resonance frequencies. Actual measurement results of glass interposer with and without TGVs have been demonstrated [46] and are shown in Fig. 5. On-chip decoupling capacitors have also been employed [47]. A recent detailed overview and demonstration for suppression of resonances in glass substrates has been presented in [46] and [48].

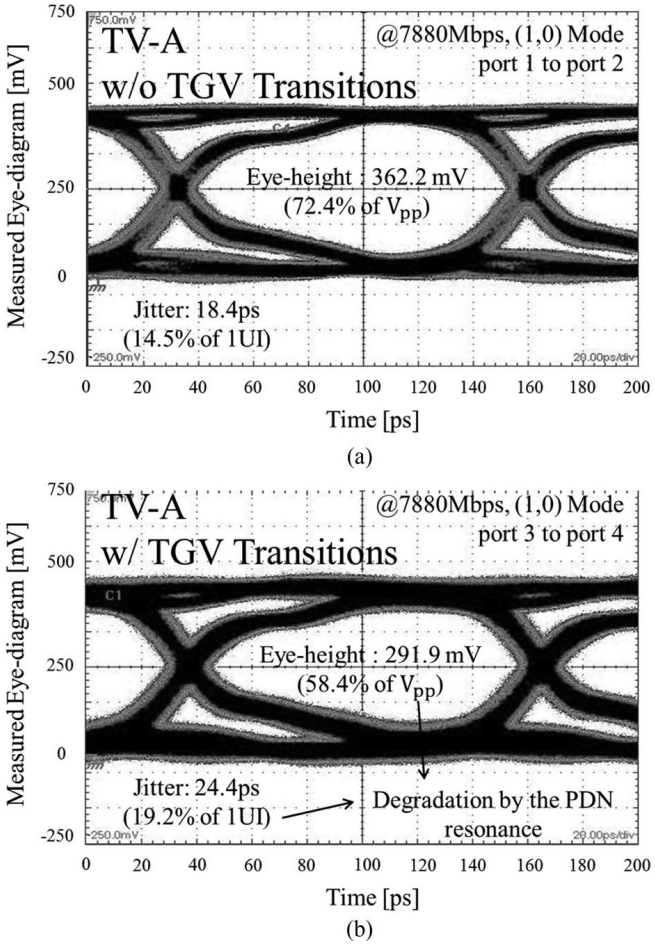

Fig. 5. Measured eye diagrams of the glass interposer channel with and without TGV transitions are shown. PRBS signal with a data rate of 7880 Mb/s that corresponds to PDNs (1, 0) mode resonance frequency is injected. (a) Without TGV transitions. (b) With TGV transitions. In the channel with TGV transitions, eye diagram is degraded at the resonance frequency due to high insertion loss of the channel [46].

Glass as a material has low thermal conductivity. Thermal management of glass interposer is a considerable challenge faced by researchers. Different approaches have been adopted to combat the issue. One of the most successful approaches of incorporating copper structures in the interposer is given in [49]. Copper TGVs are fabricated in glass interposers and are found to be effective sources of heat management. RDLs, printed circuit board, and metallic traces are also deposited in an optimized manner to manage the overall thermal performance [49]. Warpage and cracking of ultrathin glass interposers are a key issue. Cracking is mainly attributed to the defects during glass thinning, dicing, and TGV fabrication. Different optimized polymer layers and glass compositions

TABLE I
COMPARISON AMONG SILICON, GLASS, AND ORGANIC INTERPOSERS (* = GOOD, O = SATISFACTORY, AND X = POOR)

Material	Properties						
	Electrical	Mechanical	Thermal	Physical	Supply Chain	Cost	Commercial Applications
Silicon	O	O	*	*	O	X	*
Organic	*	X	X	O	*	O	O
Glass	*	O	O	*	X	*	X

are usually employed to avoid glass cracking and to ensure improved handling. The polymer layer also reduces CTE mismatch between the metal layers and glass interposer, thus reducing warpage effects. Different schemes explored in the literature and industry can be found in [50]–[54].

Glass as an interposer substrate material is not yet used in major high-performance industrial applications. Researchers have demonstrated different individual and independent high-performance devices, which hold the key toward incorporation of glass as the next-generation interposer substrate material. Passive RF components (inductors and capacitors) and filters, such as low pass and bandpass, have been demonstrated with good return and insertion loss characteristics for high-performance applications [55], [56]. Similarly, high-data-rate optoelectronic applications using glass and polymer-based optical components have been demonstrated recently. Different novel and innovative ideas for polymer processing over glass substrate have been presented, which can pave the way for high-end communication and biomedical applications over glass substrate [44], [57], [58].

The use of glass interposer for high-performance memory/logic applications is another key aspect for the glass interposer technology. Some recent demonstrations have used glass as an interposer for JEDEC HBM applications [59]. Six layers of metallization have been demonstrated with 3 μm of linewidth and space width [60]. Such demonstrations hold the key for future high-performance HBMs and HMCs. Hybrid schemes such as EIC using glass interposer in organic package have been demonstrated for high-performance applications [61].

V. COMPARISON OF SILICON, ORGANIC, AND GLASS INTERPOSER TECHNOLOGIES

Table I summarizes the overall market penetration of silicon, organic, and glass interposer technologies for high-performance applications. It compares the performance aspects, which are responsible for the penetration of each of these technologies in the commercial market. Table I also shows major strengths and weaknesses present in each of these technologies, which provide fruitful information about the open issues and research challenges currently associated with these technologies. The aspects considered for analysis include electrical, mechanical, thermal, and physical properties of these technologies, along with the supply chain, cost, and current penetration level in commercial market.

Electrical properties of both glass and organic interposers are found to be much better as compared to silicon interposers. The electrical loss in silicon for high-performance applications is much higher as compared to the other two technologies. At higher frequencies, the loss in silicon is much more prominent than organic and glass. Moreover, glass and organic interposers have much higher resistivity compared to silicon interposers. These are considered as the main reasons for relatively weaker performance of silicon as far as electrical performance is concerned. Apart from these aspects, the realization of dense electrical structures, interconnects, and less than 5 μm L/S using organic interposers is still a challenge and requires much innovation. This aspect gives glass interposers edge in comparison when considered for high-performance applications.

Mechanical properties such as strength and modulus of elasticity of neither of these technologies can be considered as very good. The organic interposers are found to have poor performance when it comes to these factors, whereas the performance of silicon and glass is satisfactory. This is a major issue that affects the reliability of the interposer when employed for high-performance applications.

CTE mismatch and ability of thermal conduction are key parameters for thermal evaluation of the interposer technologies. It was observed that the silicon interposers had the least possible CTE mismatch with the ICs/die as silicon is the material employed by the ICs/die itself. The organic interposers are found to have the most CTE mismatch and are thus considered as the worst among the three. The glass interposer's performance is satisfactory in this domain as it may not provide the best CTE matching to the ICs/die as of the silicon, but the performance is much better compared to the organic technology.

Physical properties, such as surface finish and roughness, and availability of extremely thin and large panels for processing, are key aspects considered for these three interposer technologies. The organic process technology is lacking in this regard compared to the silicon and glass process technologies. Both the silicon and glass interposers have achieved ultrathin dimensions, and glass is also available in large panels for processing, while the organic interposers have not yet achieved such ultrathin dimensions.

Supply chain of the organic technology is the most widespread and mature. One of the main reasons for that is the usage of organic material for other commercial applications is much older compared to the silicon and glass technologies. The supply chain for silicon is also widespread but is not as large as that of organic while that for glass is in its infant stage. The supply chain for glass is one of the main hindrances in its widespread adoption for the next generation of interposer technologies for high-performance applications.

Cost is a major factor associated with research and commercialization in any of the technologies. It was observed that the cost of glass is the least among the three interposer technologies. Silicon is still costly, while the organic technologies are considered to be lower in cost compared to silicon and competitive to glass. The availability of glass and organic interposers in large panels also makes them cost-effective compared to silicon. The limited wafer size of silicon and fabrication cost associated with it make it an expensive choice, while the fabrication challenges in achieving less than 5 μm L/S and mechanical reliability issues in organic substrates render them expensive for realization of next generation of high-performance applications. These are a few of the key factors driving the ongoing research in the glass interposer and perhaps can be considered as the main reason for reduced interest of the research community toward organic interposers and silicon interposers.

Both silicon and organic interposers have been employed, by far most, for the current high-performance applications, while there is not yet any ground-breaking demonstration employing glass interposers. The silicon interposers have recently been incorporated at the high-end products such as high-performance GPUs, CPUs, FPGAs, and HBMs, while the midrange commercial products such as basebands, processors, RFICs, mobile phones, and power management modules have a greater share of organic interposers—the primary reason for it being the cost involved in processing of silicon interposers.

VI. Future Trends

It has become obvious that each interposer substrate material has its advantages and disadvantages. In order to achieve ultimate SOP high-performance applications, both industry and academia have to address the disadvantages in all these technologies to come up with a best possible solution. Both silicon and organic interposers have considerable share in the industrial-grade high-performance demonstrations, while glass is still in the academia on a research scale. Although Qualcomm presented some recent demonstrations using larger glass panels, still people in academia and industry are striving and looking forward to a larger scale penetration of glass in the upcoming years.

In order to realize low-cost high-performance SOP IoT applications and consumer electronics, high-density wafer-level packing techniques are currently employed in industry with good success. One of the key enabling variations of these technologies is high-density FOWLP. This technology is intended to provide high level of integration and larger number of I/O connections. It enables "substrateless integration" resulting in thin package footprint, small form factor, and reduced cost compared to silicon interposer-based integration. Along with these, it also provides improved thermal (less warpage and better coplanarity) and electrical performance (smaller interconnects and less parasitics) [62], [63].

In high-density FOWLP, a KGD is embedded in a low-cost material (epoxy mold compound) with provision allocated for additional I/O connections. This reduces the use of expensive silicon real state for interconnection purposes. The RDLs are then developed over the top of the die followed by the ball grid array. Fine L/S has been achieved, allowing better routability along with finer pad pitch for flip-chip assembly. The technique also allows batch processing similar to WLP techniques. The process has yield, capacity, and flexibility issues. It also employs the die-first scheme, which requires additional testing setup before the process. The technology has readily been incorporated in high-performance consumer electronics, such as mobile phones and tablets, in high-performance RF applications, and in some CPUs and GPUs packaging [62], [63].

A recent development by Intel called "EMIB" has been considered a breakthrough in the 2.5-D packaging approach. The technology has been specifically designed for the future high-performance applications. It allows high-density interconnections and wiring between heterogenous dies on a single organic package. It employs small pieces of silicon, with multilayer BEOL interconnects, instead of large and expensive silicon interposer with TSVs. These silicon pieces are specifically embedded in the substrates to enable localized dense interconnects where required. The technology allows no limits on the dies size and employs the standard manufacturing assembly line. The overall process is cost-effective as it avoids the use of costly silicon interposers with TSVs, and has less silicon area but is considered to add further complexity to the organic substrate manufacturing capability [64].

In terms of the organic interposers, efforts are required to increase thermal conductivity (or heat sinking capability) and improving thermomechanical strength. The glass interposers have surface finish and thermal management issues especially for HBMs. The availability of glass along with the handling and reliability is a key issue that needs to be addressed for the glass interposers. The supply chain of glass needs improvement in order to have bigger market share and penetration. The issues of electrical loss in the silicon interposers associated with its semiconducting properties and the cost associated with TSV fabrication are key aspects where extensive research has been going on. It has been estimated that approximately 44% of the cost of manufacturing of the silicon interposer is attributed to the TSV filling process. This aspect needs to be addressed [29]. The issues of thermal management in organic interposers and electrical loss in silicon interposers have paved the way for glass as the next major potential interposer candidate for the future realization of high-performance applications.

Technologies are evaluated in the form of an S-curve. They start off slow with a low rate of adoption, and reach inflection point, and from there onward they takeoff. For the next few years, these technologies remain in the market and reach a level of saturation. It is at this point that the market tends toward newer technologies. Using this approach, we have observed that both silicon and organic interposers are existing technologies that are in the market, whereas glass is still in its early stages. Based on the trends, we can extrapolate a great deal of research emerging in glass interposers. Organic and silicon, on the other hand, will continue at about the same pace as it is progressing, with interesting new high-performance devices expected to emerge. It may not reach saturation, but will move closer to that. Glass, therefore, has a

huge potential in both research and market provided that the conditions remain conducive in the upcoming years.

Industrial trends in accepting glass interposer as "the next big thing" for the high-performance applications are encouraging. As mentioned earlier, Qualcomm's demonstration of 1-m^2 large panel for the high-performance interposer applications is a proof of that. Corning recently debuted their latest glass substrate material, which is said to be stiffer, with a lower than ever surface roughness and a wide range of tailorable CTE [65]. It has also been pointed out that the material shall be extremely suitable for high-performance RF and MEMS applications with extremely low insertion loss and greater hermetic sealing properties. Corning is pushing the bar for this technology and is undoubtedly among the technology leaders. It was also seen that in 2013, Triton Microtech., whose parent company is Asahi Glass, received a U.S. $3.2 million investment in order to ramp up glass interposer manufacturing. Asahi predicts that they will achieve 2-μm line and space by 2019. This glass also has roll-to-roll process compatibility, which allows for even less manufacturing time and costs. In 2014, NGK/NTK was seen demonstrating a polymer-coated glass substrate for better warpage control [66]. Since the material properties of glass can be tailored, it can be fairly deduced that in the coming years, we can expect better glass interposer substrates, which will be capable of higher thermal conductivity as well.

Future applications and demonstrations, such as microfluidic cooling technologies for the glass interposers, will be of critical importance especially when it comes to HBMs. The technique can provide more efficient thermal management, especially for high-power, communication, and data-intensive interconnect applications. Similarly, a demonstration, such as EMIB using glass, can also result in an interesting and much cheaper option compared to silicon. Other high-performance applications where glass is highly suitable are related to the on-chip optoelectronics and the optical interconnects. These particular applications have the potential to unlock extremely high-bandwidth computing applications and could result in realization of quantum and optical computing devices. Apart from these technologies, high-performance RF- and RFID-based applications are also possible using glass. It is just a matter of time when such demonstrations are announced.

VII. Conclusion

We have discussed silicon, organic, and glass interposer technologies for high-performance applications in this paper. We have provided a detailed overview of the associated issues and challenges for the widespread commercialization along with the future trends for these technologies. Silicon and organic technologies for interposers are quite mature, while glass technology is in its early stages. In our opinion, the glass interposers have the potential to be adopted for the high-performance applications in the near future with initially having more concentration in midrange products and later in the high-end high-performance devices, provided that the current interest and conducive market environment carries on. Organic and silicon will remain in the industry in the upcoming years, but soon a major portion of silicon will be replaced by glass, especially as an interposer material for many of its high-performance computing applications. Organic on the other has much deeper penetration in the packaging industry, but as an interposer material, glass has added advantages over organic substrates to become the next interposer material platform for high-performance technologies.

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