Low-Cost Thin Glass Interposers as a Superior Alternative to Silicon and Organic Interposers for Packaging of 3-D ICs

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***Abstract*— Interconnecting integrated circuits (ICs) and 3-D-ICs to the system board (printed circuit board) are currently achieved using organic or silicon-based interposers. Organic interposers face several challenges in packaging 2-D and 3-D-ICs beyond the 32-nm node, primarily due to their poor dimensional stability and coefficient of thermal expansion (CTE) mismatch to silicon. Silicon interposers made with back-end of line wafer processes can achieve the required wiring and I/O density, but their high-cost limit them to high-performance applications. Glass is proposed as a superior alternative to organic and silicon-based interposers for packaging of future ICs and 3-D-ICs with highest I/Os at lowest cost. This paper presents for the first time a novel thin and large panel glass interposer capable of scaling to 700 mm and larger panels with potential for significant cost reduction over interposers made on 200-mm or 300-mm wafers. The formation of small through vias at high speed has been the biggest technical barrier for the adoption of glass as an interposer and system substrate; and this paper describes pioneering research in via-formation in thin glass substrates, using a novel "polymer-on-glass" approach. Electrical modeling and design of through package vias (TPVs) in glass is discussed in detail, and the feasibility of 50-μm pitch TPVs in 180-μm thin glass substrates has been demonstrated. The excellent surface finish and low CTE of glass leads to increased I/O density, and increased functionality per unit area leading to system miniaturization.**

***Index Terms*— Panel processing, system-on-package (SOP), thin glass interposer, through package via (TPV), wet metallization.**

I. Introduction

THE CURRENT approach to interconnecting integrated circuits (ICs) and 3-D-ICs is primarily based on organic interposers between the IC and printed circuit board [1], [2]. However, there are two major shortcomings with this approach namely: 1) difficulty in achieving high I/Os at fine pitch because of poor dimensional stability of organic substrates, thus requiring large capture pads for layer-to-layer registration and 2) warpage that results as the number of layers are increased [3], [4]. Although, silicon interposers are being developed to overcome these challenges [5], they face a different set of challenges, such as high cost due to limited wafer size (200–300 mm) from which to yield large number of interposers and the added cost of via liners for electrical isolation of via conductors. The high cost is also attributed to single side re-distribution layer (RDL) processes, need to back-grind and polish to achieve thin interposer, expensive back-end of line (BEOL) process technologies, such as physical vapor deposition, chemical vapor deposition, and Bosch reactive ion etching (RIE) for through silicon via (TSV). This paper presents an entirely different approach, using large panel sizes to achieve fine pitch metalized through vias and copper conductors, at reduced cost per I/O than either organic or silicon interposers. Glass as a substrate material has several merits, namely: excellent dimensional stability, closely-matched and tailorable coefficient of thermal expansion (CTE) to silicon die, excellent electrical resistivity with low loss, high thermal stability and more importantly, the availability of glass substrates in large and thin panel sizes. Large panel liquid crystal display (LCD) glass substrates are widely used, and thus most of this infrastructure can be used to manufacture glass interposers at low cost. The glass interposer is not free of challenges, and presents two primary challenges: 1) low-cost formation of small through package vias (TPVs) and 2) lower thermal conductivity than silicon. Both silicon and glass are prone to failure due to the presence of defects or cracks. In case of silicon, crack failures occur mainly along the crystallographic planes. Because glass is amorphous, cracks are initiated due to surface defects. The addition of TPVs or TSVs decreases the inherent strength of these materials. The fracture toughness of plain glass and silicon wafers has been studied, and shows comparable values [6]. Glass shows better and repeatable performance in terms of fracture strength. In case of cracks (especially on the surface), the proposed "polymer on glass" approach serves as a stress buffer layer, preventing crack propagation.

The reduction in cost with glass mainly comes from two factors: 1) the use of large area panels, resulting in yielding about 8X more interposers than with silicon wafers (Fig. 1) and 2) the use of low-cost materials and processes for TPVs and multiple RDLs. The material and process factors that lead to lower cost glass interposers include: 1) dry film, nonvacuum, and high throughput package processes as opposed to

Manuscript received July 12, 2011; revised March 30, 2012; accepted May 13, 2012. Date of publication July 18, 2012; date of current version August 31, 2012. Recommended for publication by Associate Editor S. Tonapi upon evaluation of reviewers' comments.

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Digital Object Identifier 10.1109/TCPMT.2012.2204392

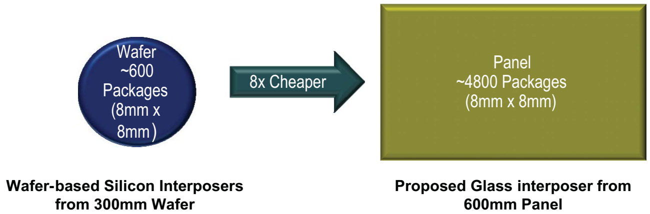


Fig. 1. Cost advantage from increased panel size, yielding more components per panel.

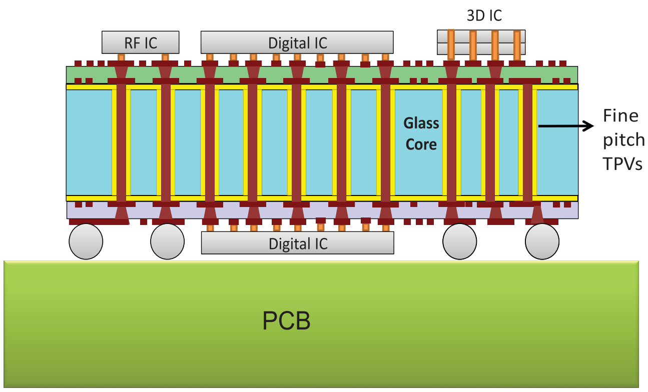


Fig. 2. Schematic of glass interposer and package with TPVs, wiring, and I/Os on both sides for digital, RF, and 3-D-IC assembly.

expensive wafer-based BEOL processing; 2) simplified double-side process flow for reduced number of steps; 3) no chemical-mechanical polishing; 4) low temperature dry film polymer TPV liner and build-up dielectrics; and 5) small lines and RDL vias for minimum routing layers on both sides of the glass interposer.

Glass substrates with through glass vias using different lasers and surface metallization have been studied [7]–[11]. Hutt *et al.* [12] have examined laminated glass substrates for interconnecting ICs and photonic devices. The use of glass wafers with metalized tungsten-plugged vias, which provide electrical connection and hermetic sealing have also been demonstrated [13]. Photo-sensitive glass has also been studied for micro-fluidic applications, owing to their parallel processing capability [14].

In summary, this research presents a holistic and integrated-system approach toward exploring glass interposers for the best combination of electrical properties and interconnection density at lowest cost, including the first demonstration of a thin glass interposer with potential for large panel manufacturing.

Fig. 2 shows the cross-section schematic of a glass interposer with TPVs, wiring, and I/Os on both sides, which facilitates double-side active and passive component mounting, leading to reduced interposer size. As part of this effort, initial research on TPV hole formation and metallization as well as embedding of radio frequency (RF) components have been reported [8], [15]. This paper uses the fundamental concepts from the previous work with the following enhancements:

1) theoretical study of via feasibility in thin glass;
2) analysis of TPVs with and without polymer coating.

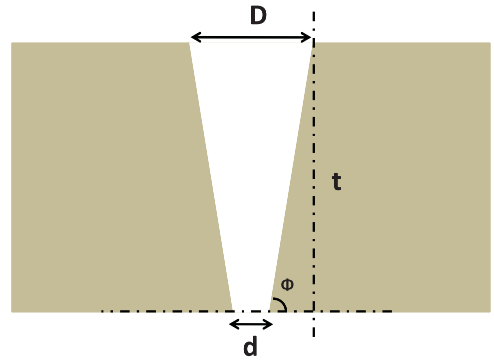


Fig. 3. Schematic cross section of a glass TPV.

This paper has four supporting sections. Section II discusses a mathematical model that relates the substrate thickness to via side wall angle and entrance/exit via diameters. This analysis is useful in designing TPVs to meet certain electrical specifications. Section III describes materials and processes involved in TPV hole formation and metallization. Electrical modeling for signal integrity is discussed in Section IV, and Section V discusses an integrated process approach for the initial glass interposer demonstrator.

II. Theoretical Analysis of TPV

Low cost via formation in glass is the biggest challenge for achieving small-pitch interconnections. A simple mathematical model is proposed to act as a guideline to select glass via size and substrate thickness. Equation (1) relates the via exit diameter to the entrance diameter, glass thickness, and the effective via side-wall angle

$$d = D - \frac{2t}{\tan \Phi} \qquad (1)$$

where

d exit diameter of via;
D entrance diameter of via;
t substrate thickness;
Φ effective via side-wall angle.

The effective via side-wall angle is obtained by connecting the edges of the vias on the entrance and exit sides. Via dimensions are process-dependent (aspect ratio achievable) and the value of Φ is approximated independent of the side wall shape (Fig. 3). Via drilling speed and smallest diameter achievable depend on the glass composition. From (1), it is evident that for $\Phi = 90°$ (vertical via side wall), the entrance and exit via dimensions are equal. A negative value of d indicates that via is not drilled through the substrate (blind-via). Fig. 4 shows the variance of the exit via diameter as a function of glass substrate thickness. The slide wall angle was kept constant ($\Phi = 87.8°$), while the entrance diameter (D) was varied from 20 to 150 μm. The choice of angle 87.8° was based on the laser process capability of excimer laser (Fig. 9). It is observed that in order to achieve a 20 μm through via, the glass substrate thickness needs to be less than 250 μm for the given process ($\Phi = 87.8°$).

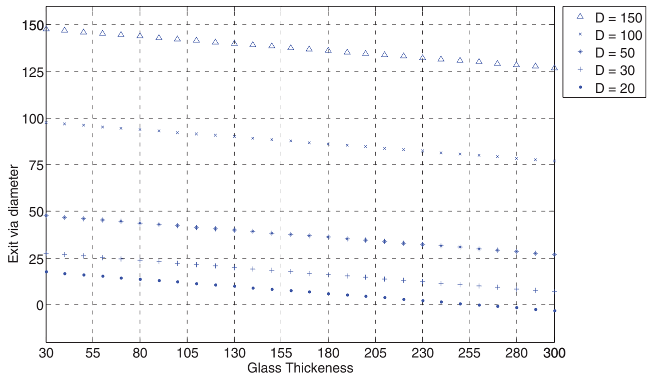


Fig. 4. Exit via diameter as a function of glass thickness with fixed via side-wall angle ($\Phi = 87.8°$) and variable D.

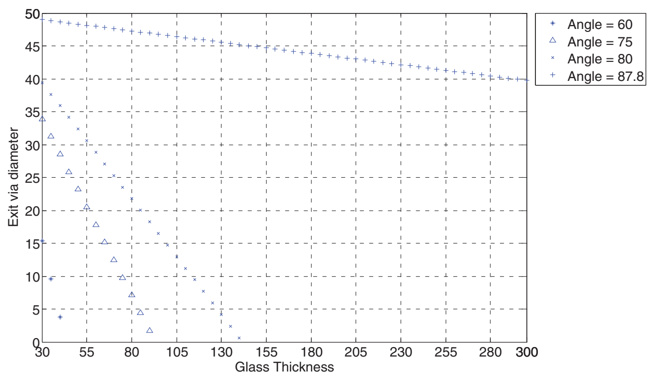


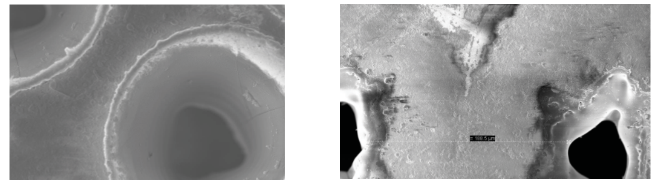
Fig. 5. Exit via diameter as a function of glass thickness with fixed D ($D = 50$ μm) and variable Φ.

Similarly, the exit via diameter was obtained as a function of glass thickness (Fig. 5) by keeping the value of D constant (50 μm) and varying the side-wall angle Φ from 60° to 87.8°. Side-wall angle close to 90° is preferred for achieving smaller through vias in thicker glass substrates. Ultrathin glass substrates (<100 μm) need to be used for achieving through vias ($D = 50$ μm) using a process that results in a side wall taper of 75°. The theoretical model gives via diameters achievable for a given glass thickness and process. It has been reported that the TPV profile affects the electrical performance [7]. Vertical vias are preferred over tapered TPVs especially while operating at higher frequencies. Thus, one can choose the appropriate process and glass thickness to meet a specific TPV requirement leading to desired performance. Also from a process standpoint, the theoretical model helps to define design rules based on process feasibility.

III. TPV Materials and Processes

A. TPV Hole Formation

TPV fabrication consists of two parts: 1) TPV hole formation; and 2) metallization. The primary barrier for a glass interposer is the formation of ultrafine pitch TPV at low cost. Via formation in glass using lasers, wet etching, and mechanical processes was explored to address this barrier. Borosilicate glass (BSG) having thickness between 100 and 700 μm were used in these experiments. The choice of BSG glass may be attributed to widespread use in the LCD display industry, silicon matched CTE (3 ppm/°C) and availability in large panel formats. Two approaches were used for TPV formation: 1) via in bare glass and 2) via formation in glass, which was laminated with polymer films on both sides. Polymer lamination on glass facilitates handling of large panels during processing, acting as a stress buffer on the glass surface, and helping in metallization of the glass interposer. Wet etching of glass can also be considered for TPV hole formation but is relatively difficult compared to silicon. Although wet processing yields higher etch rates (approximately 10 μm/min), the isotropy of etch profile is unfavorable for through vias in thick substrates. Deep RIE and inductive coupled plasma have also been studied and demonstrated for achieving a greater degree of anisotropy, but they exhibit lower etch rates (approximately 0.7 μm/min) [16]–[18]. Laser ablation technique using excimer laser is a feasible approach, which is scalable to parallel via formation, by adopting a mask projection approach [19].



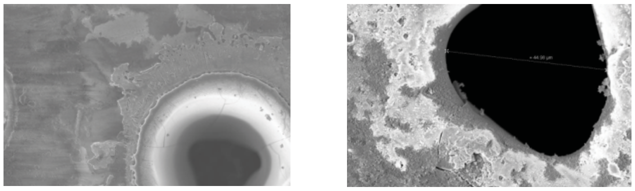
(a) (b)

Fig. 6. SEM image of via using CO_2 laser ablation on BSG. (a) Entrance side. (b) Exit side [8].

BSG samples with 175 and 500-μm thickness were subjected to CO_2 laser ablation. Initial results from CO_2 laser yielded large via diameter (125-μm diameter at the entrance), and a highly tapered via profile with micro-cracks along via edges. CO_2 lasers operate at higher wavelength (10.6 μm) and the ablation mechanism involves heating of the glass due to atomic vibrations. Since glass has low thermal conductivity (1 W/mK), the heat affected zone creates thermal stresses in glass leading to cracks along via edges. The scanning electron microscope (SEM) images of the vias ablated using CO_2 laser are shown in Fig. 6(a) and (b). In this sample, via entrance diameter was 125 μm, while the exit diameter was 50 μm at a pitch of 175 μm. The micro-cracks were minimized by the use of transverse-excited-atmosphere CO_2 laser for drilling at a slightly larger pitch (250 μm), which yielded fewer defects.

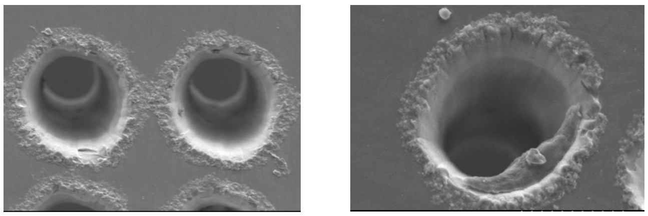
To achieve smaller-pitch vias, UV laser operating at a wavelength of 266 nm was used for TPV formation. The results obtained were comparable to CO_2 lasers. The TPV pitch achieved was 250 μm, with entrance and exit diameters of 100 and 50 μm, respectively. In comparison to CO_2 laser, UV lasers cause less thermal damage since the ablation is based on a combination of thermal ablation and breaking of chemical bonds within the glass matrix [Fig. 7(a) and (b)].

ArF-based excimer lasers operating at 193 nm were found to be more effective, inducing minimum thermal stress during the ablation process. Smaller diameter and smaller pitch TPVs were achieved in 175-μm thin glass, using excimer laser with entrance and exit diameters of 35 and 22 μm, respectively,



(a) (b)

Fig. 7. SEM image of vias formed by 266-nm UV laser. (a) Entrance side. (b) Exit side [8].



(a) (b)

Fig. 8. SEM images of via entrance using excimer laser ablation at different magnifications (a) 1.2 K and (b) 1.8 K [8].

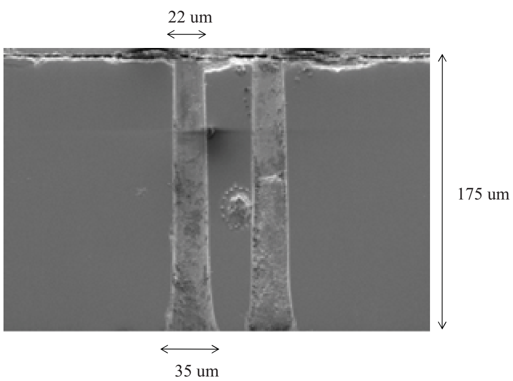


Fig. 9. SEM cross section view of 50-μm pitch TPV formed using excimer laser.

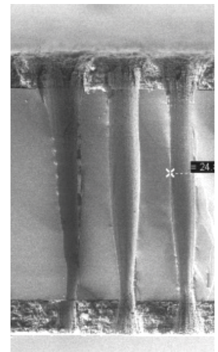


Fig. 10. SEM image of cross section of excimer via on cleaved glass sample laminated with polymer.

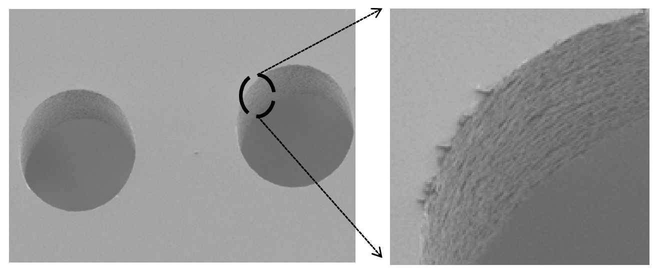


Fig. 11. SEM image of mechanically processed via [8].

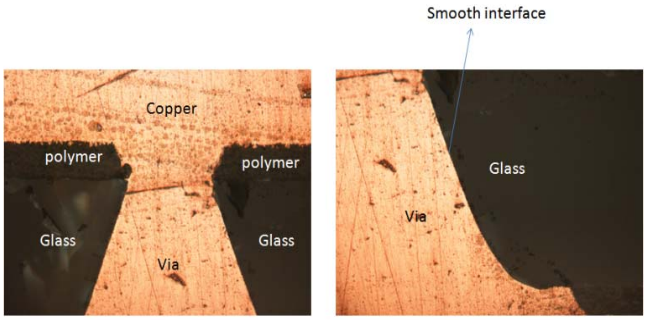
at a pitch of 50 μm. The laser energy used was 7–12 mJ per pulse, with a repetition rate of 25–200 Hz. No micro-cracks were observed on the glass surface or along the side wall after laser ablation. Glass has very high absorption at 193 nm (ArF). Hence, almost 95% of the laser energy is utilized to break the chemical bonds within the glass matrix. A small part of the laser fluence is converted into heat energy, which is minimal, and thus the thermally induced stress is also minimal.

A cross-section study showed a smooth via side wall profile. SEM imaging was carried out to study the via side wall profile and ablation debris around via entrance. Via side wall surfaces undergo slight modifications due to laser impingement, which may be favorable for seed metal adhesion onto the glass surface. Laser ablation on bare glass resulted in debris around via periphery, as can be seen in the SEM images in Figs. 8 and 9. Wet chemical etching using buffered hydrofluoric acid was used to remove the residues that remained after ablation.

TPV hole formation with laminated polymers is described in this section. A hot press-lamination tool was used for the lamination of RXP4 polymer onto the glass surface. The glass surface was initially cleaned using acetone, methanol, and isopropyl alcohol followed by rinsing with deionized water. The samples were then baked in an oven at 100 °C for 30 min to remove absorbed moisture from the glass surface. For a 6$''$ square glass sample with a thickness of 180 μm, a pressure of 140 psi was applied for 1 hour at a temperature of 200 °C. Excimer laser ablation of TPV was carried out after polymer lamination. It was observed that the TPV profile was different on bare glass when compared to polymer-laminated glass sample. Fig. 10 shows a cross-section SEM image of an excimer laser ablated via in polymer-laminated glass. Via profile is almost vertical with minimum side wall taper. The funnel shape via profile in case of bare glass is attributed to laser reflections at TPV entrance. However, by using a polymer coating on glass prior to laser ablation, the reflections are minimized. This attributes to a more vertical via profile with sharp edges. Vertical via profiles are desirable for fine-pitch, high density interconnections, and also for good electrical design and signal integrity.

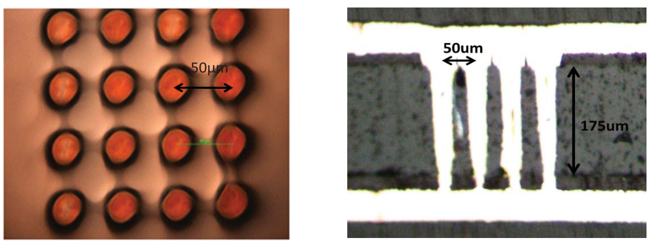
BSG substrates of 200 and 500-μm thickness were used to explore via formation by mechanical process. The glass samples were 2.7$''$ squares and the design had variable via diameters from 100 to 250 μm with a step increment of 50 μm. The TPV pitch was kept constant at 375 μm. Glass TPV using mechanical technique yielded large via diameters compared to excimer lasers.

The vias obtained by this process have a vertical profile, almost 90° slant angle and a crack-free surface. Fig. 11 shows the SEM images of the mechanically processed TPV. The rough nature of via side wall may be favorable for metal adhesion during seed layer deposition.



(a) (b)

Fig. 12. Cross section of metalized TPV with polymer buffer layer on the glass surface. (a) Exit side of via. (b) Slanted via side wall [8].



(a) (b)

Fig. 13. Optical image of metalized vias (50-μm pitch). (a) Top view. (b) Cross section [8].

B. TPV Metallization on Glass

Direct metallization on glass is a significant challenge due to glass surface chemistry and CTE mismatch at the metal–glass interface. Surface modification techniques have been reported [20], [21] to enhance direct metal adhesion on glass, but formation of thick metal liner on glass results in delamination. The use of polymer buffer layer helps to solve the metal adhesion problem to the glass surface. TPV metallization was a two-step process: 1) seed layer formation followed by and 2) via metallization using copper-electroplating. Two approaches for seed layer formation were used: 1) electroless copper deposition and 2) sputtering.

Electroless copper is a fast and low cost wet-processing technique, which is scalable to large panel sizes. The 175-μm thin glass substrate with polymer and TPVs was first subjected to a plasma desmear process using CF_4 and O_2 (1:4) for 5 min. Plasma desmear removes debris (due to laser ablation) from the periphery of via, and also roughens the polymer surface, thereby facilitating seed layer adhesion. The sample was thoroughly rinsed post-plasma treatment and subjected to seed layer metallization. Electroless copper metallization was carried out for 30 min, resulting in a seed layer thickness of around 0.1–0.5 μm. Copper electroplating was carried out after the seed layer deposition.

In order to study the compatibility of glass interposer fabrication using wafer-based processes, sputtering was explored as an alternate option to achieve a metal seed layer. Sputtering of Ti-Cu on polymer laminated glass with TPV was carried out, with Ti thickness of 50 nm and copper thickness of 1 μm. The sputtered seed layer showed good adhesion to the polymer surface. After sputtering the TPVs were electroplated

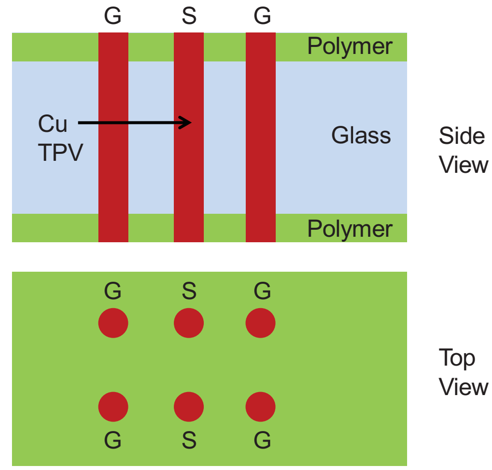


Fig. 14. Schematic of the TPV structure.

TABLE I
TPV DIMENSIONS

TPV formation process	TPV diameter (μm) – top	TPV diameter (μm) – bottom	TPV pitch (μm)
Mechanical drilling	100	100	250
CO_2 laser	125	50	250
UV laser	100	50	250
Excimer laser	35	22	250

(with copper) to achieve complete via fill. For the TPVs processed by CO_2 laser ablation, complete via fill was achieved as shown in Fig. 12. A smooth interface (with no cracks) was observed between glass and metal. The tapering via profile on the exit side of via could act as a via-interlock structure, which can be beneficial in minimizing thermo-mechanical related via reliability failures.

TPV metallization of smaller fine-pitch vias (ablated using excimer lasers) was also carried out using sputtered and electroless seed layer followed by copper electroplating. A top view and cross-section image of metallized TPVs at ultrafine pitch is shown in Fig. 13(a) and (b).

IV. ELECTRICAL DESIGN OF GLASS TPVS

In this section, TPVs in glass interposer are electrically modeled and simulated. CST Microwave Studio, a 3-D full-wave electromagnetic solver, was used to simulate the TPV structures as shown in Fig. 14. The structure is comprised of two signal TPVs (marked as "S") and four ground TPVs (marked as "G"). The glass interposer was 180 μm in thickness with a 20-μm thick polymer liner layer on its top and bottom surfaces. The physical parameters of the TPVs formed by different processes are outlined in Table I.

Fig. 15 shows the insertion loss plots of the TPVs. It is observed from Fig. 15 that the TPVs in glass interposer have low insertion loss. The loss is higher in smaller TPVs (formed by excimer laser), because they have higher inductances than the other TPVs. The mechanically drilled TPVs have a cylindrical structure with 100-μm diameter. Due to its cylindrical

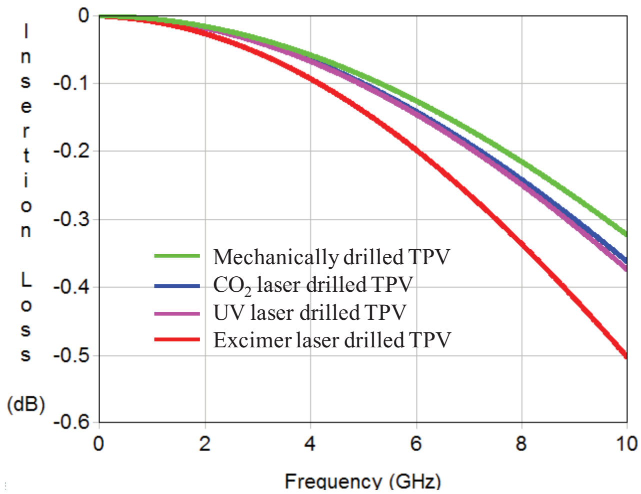


Fig. 15. Insertion loss comparison of TPVs in glass interposer.

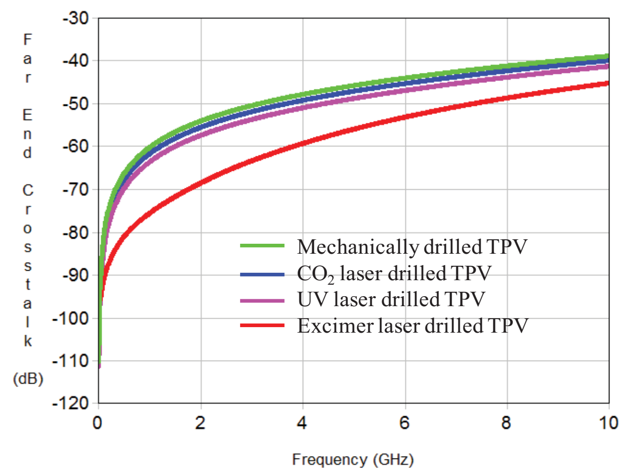


Fig. 16. Far end crosstalk comparison of TPVs in glass interposer.

shape and larger diameter, it has the lowest loss among the four TPV structures. The loss for the CO_2 laser drilled TPV and the UV laser drilled TPV is similar due to their almost identical via dimensions. However, the UV laser drilled TPV has slightly higher loss due to the smaller top diameter as compared to the CO_2 laser drilled TPV.

The crosstalk plots of the TPVs are shown in Fig. 16. It is observed that the smaller TPVs have lower crosstalk as compared to the larger TPVs. The TPV pitch was constant in the four models that were compared. The smaller TPVs have larger separation between the signal vias, which leads to lower crosstalk. The crosstalk in TPVs in glass interposers is less than −38 dB at 10 GHz.

V. Glass Prototype Fabrication

Fig. 17 shows a typical process flow for a four-metal layer glass interposer. A double-side nonvacuum-based process was used for the lamination of polymer onto the glass surface prior to TPV formation. Laser ablation was used for the formation of fine pitch TPVs, followed by wet electroless copper seed layer deposition. TPV metallization and formation of small line and space features was achieved by copper electroplating, using

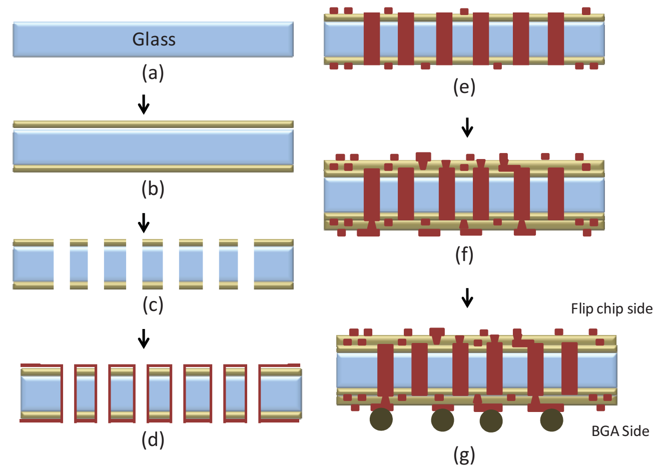


Fig. 17. Glass interposer fabrication process flow schematic [22]. (a) Glass sample. (b) Double side polymer lamination. (c) TPV formation. (d) Electroless seed layer deposition. (e) TPV metallization and wiring. (f) Build-up layer redistribution. (g) Four metal layer glass interposer.

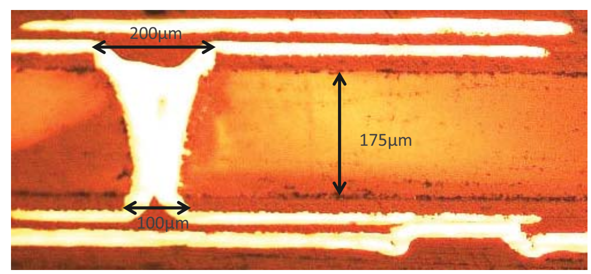


Fig. 18. Cross section of four-metal layer glass interposer [15].

a semi-additive-plating approach. Double-side polymer build-up lamination and metallization of micro-vias was carried out to realize a four-metal layer glass interposer as shown in Fig. 17(g). An optical cross-section image of a four-metal layer glass interposer is shown in Fig. 18. This four-metal layer structure was part of a RF filter design on glass, which was fabricated and characterized [15]. The use of panel-based double-side wet processing techniques coupled with low-cost materials has great potential for minimizing the cost per I/O of the glass interposer.

VI. Conclusion

This paper reported the first demonstration of a thin glass interposer and package with TPVs as a compelling alternative to wafer-based silicon interposers with TSVs. The glass interposer was targeted at reducing the cost of high density interposers by a factor of ten over silicon interposers, enabled by large panel size of 450–700 mm and beyond, and using low-cost large panel package process as opposed to conventional wafer-based BEOL process. The excellent surface finish, dimensional stability, and tailorable CTE of thin sheet glass core leads to highest interconnect density and high reliability at lowest cost. A new method for handling of thin and ultrathin glass panels for TPV formation, metallization, and RDL fabrication was demonstrated in a four-metal layer glass substrate. The most significant challenge of glass as an interposer, namely, formation of small TPVs, has been addressed and ultrafine pitch TPV with an entrance diameter of 35 μm and exit diameter of 22 μm at 50-μm pitch was demonstrated in 180-μm thin glass substrates. Metalized TPVs in glass were fabricated using electroless and sputtered seed layer followed by copper electroplating. Electrical modeling of TPVs in glass showed the potential for achieving less than 0.5-dB insertion loss up to 10 GHz. This new approach of panel-based ultrathin glass interposers has a great potential in enabling future low-cost packaging technology for integrating 3-D-ICs and other components requiring highest I/O density at lowest cost.

Acknowledgment

The authors would like to thank the member companies of the Silicon and Glass Interposer (SiGI) consortium at the 3-D Systems Packaging Research Center (PRC), Georgia Institute of Technology, Atlanta, for their support and technical guidance. The authors also thank J. Bishop and V. Sridharan from GT-PRC for assistance with the glass interposer prototype fabrication. Finally, they thank and acknowledge the supply chain partner companies of the SiGI consortium for their tool and material support.

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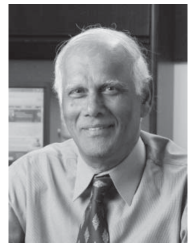

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