Everywhere you imagine. RENESAS

SCAN TECHNIQUE

Renesas Design Viet Nam Co., Ltd.
Design Engineer Division
Logic Implementation Technology
Group

04/17/12

Confidential

OUTLINE

Purpose of Scan design
Outline of Scan design
Basic concepts of Scan
Scan operation
Design operation in Scan mode/User mode
Scan design constraints
Scan ATPG
Scan Fault models
Fault assumption and categories

OUTLINE

Purpose of Scan design

Outline of Scan design

Basic concepts of Scan

Scan operation

Design operation in Scan mode/User mode

Scan design constraints

Scan ATPG

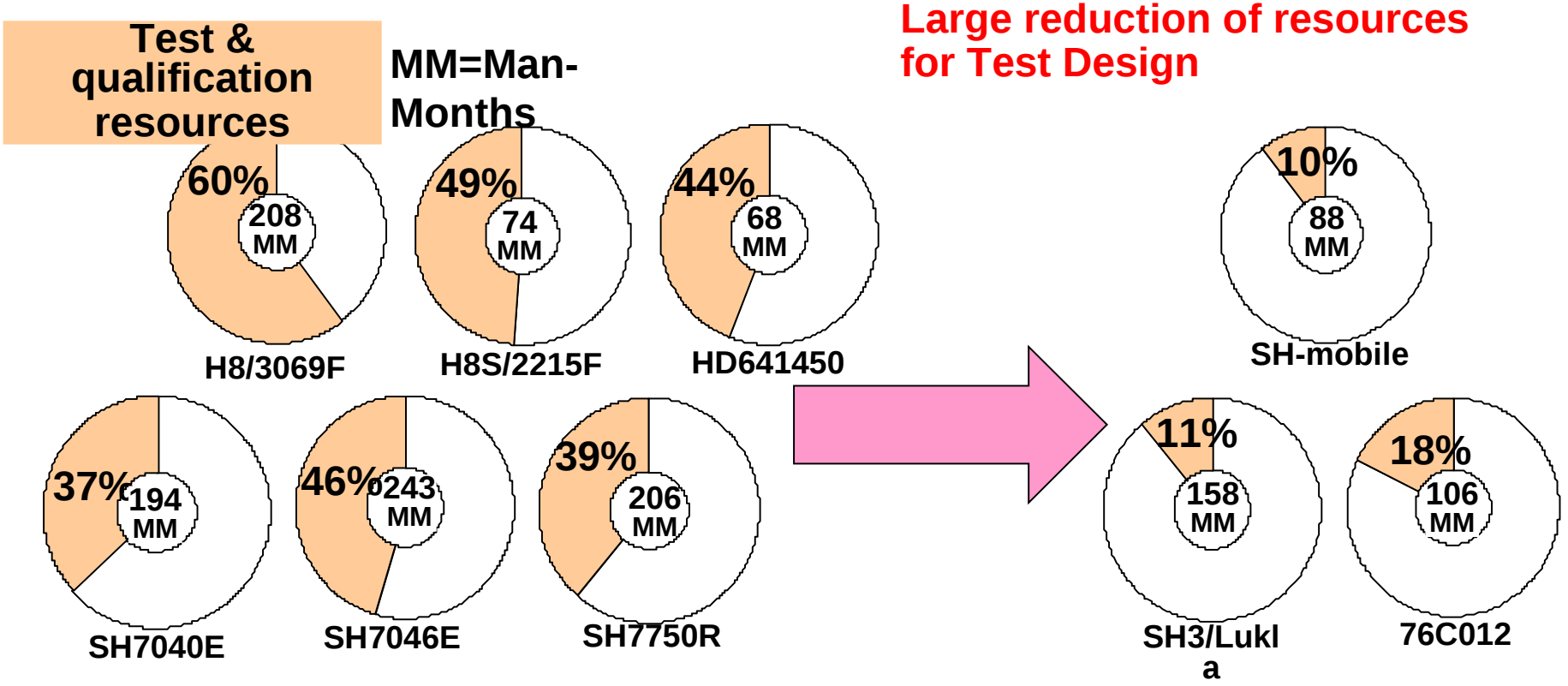
Scan Fault models

Fault assumption and categories

Purpose of Scan design (1)

Resource reduction for test design

(A limitation of function test pattern generation)



Purpose of Scan design (2)

A limitation of test quality evaluation method for function test base design

Test type	Function test	Scan test
Fault model (quality)	Only stuck-at fault	Stuck-at fault, transition fault, short fault, path delay fault
Test coverage	no increase	continuous increase as additional model
Pattern generation	Manual generation (Depends on designers' skill and experience)	Automatic generation by ATPG (An additional model may be supported by ATPG if the model is a

ATPG : Automatic Test Pattern Generation tool

OUTLINE

Purpose of Scan design

Outline of Scan design

Basic concepts of Scan

Scan operation

Design operation in Scan mode/User mode

Scan design constraints

Scan ATPG

Scan Fault models

Fault assumption and categories

Outline of Scan design

Basic concept

A difficulty for automatic test pattern generation

-> need to manage internal states

“Removal of internal states” is the solution.

Treat FFs with internal states as virtual input-output ports.

Changing the entire logic circuit to a combination circuit without states

-> Easy to generate test patterns automatically by DA (Design Automation)

To treat FFs as virtual input-output ports

Connect all FFs as if “shift registers, besides usual logic.

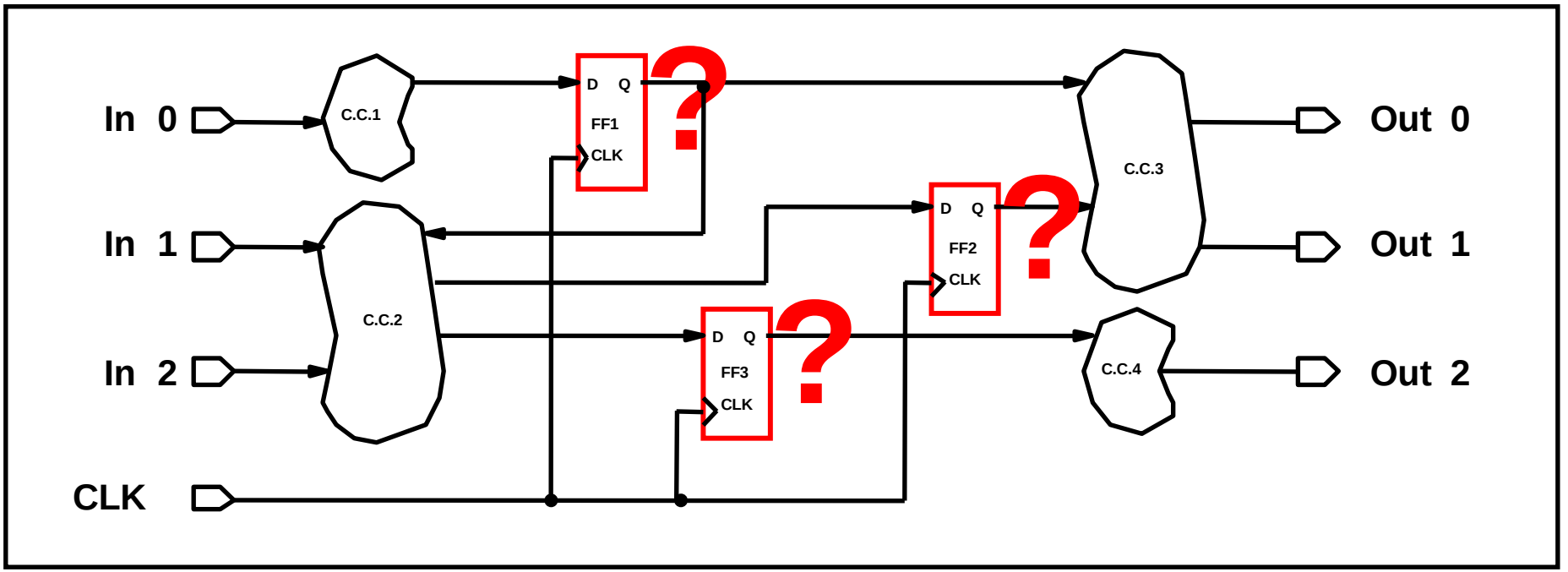
Use input-output ports of FFs to control and observe data

Call the operation to transfer data as if shift registers do “a scan”.

Example of Scan (Original circuit)

Example of original netlist (has 3 FFs)

We can not test if we control FF as sequential circuit.

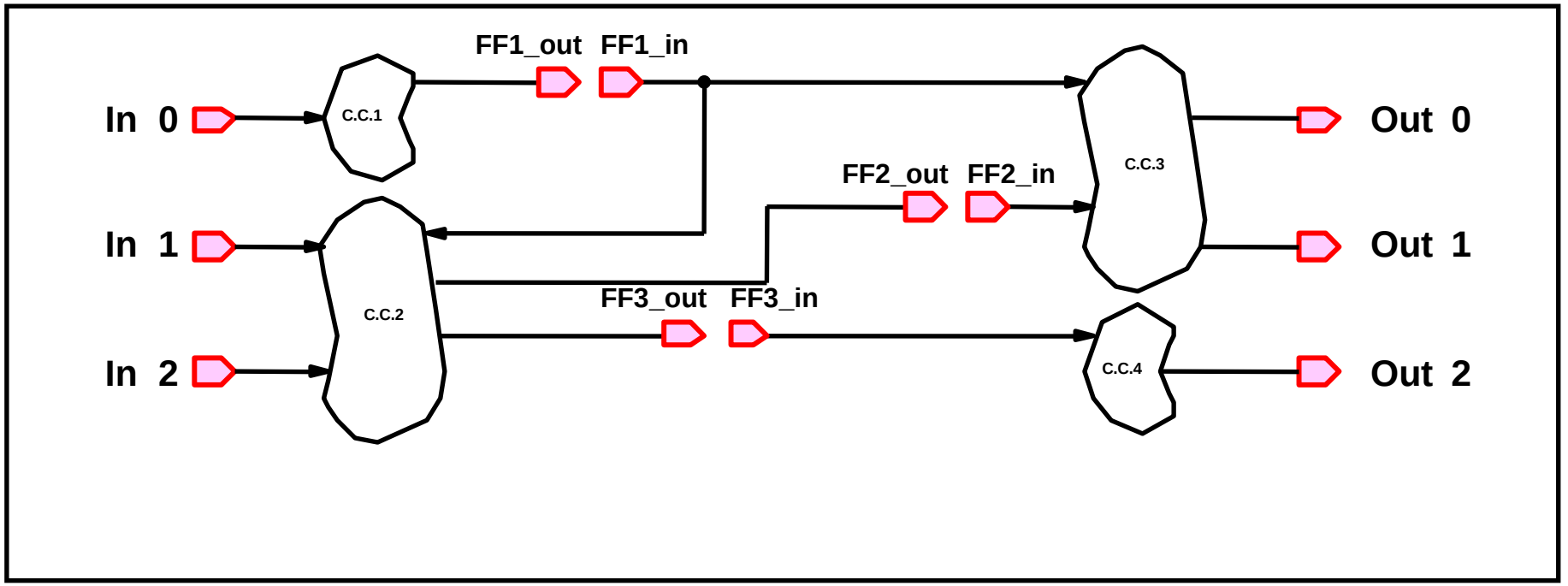


Testability is lowered because flip-flop(FF1,FF2 and FF3) is a memory unit.

Example of Scan (Virtual port)

Treat FF as virtual input/output port

--> Combinational circuit without internal states

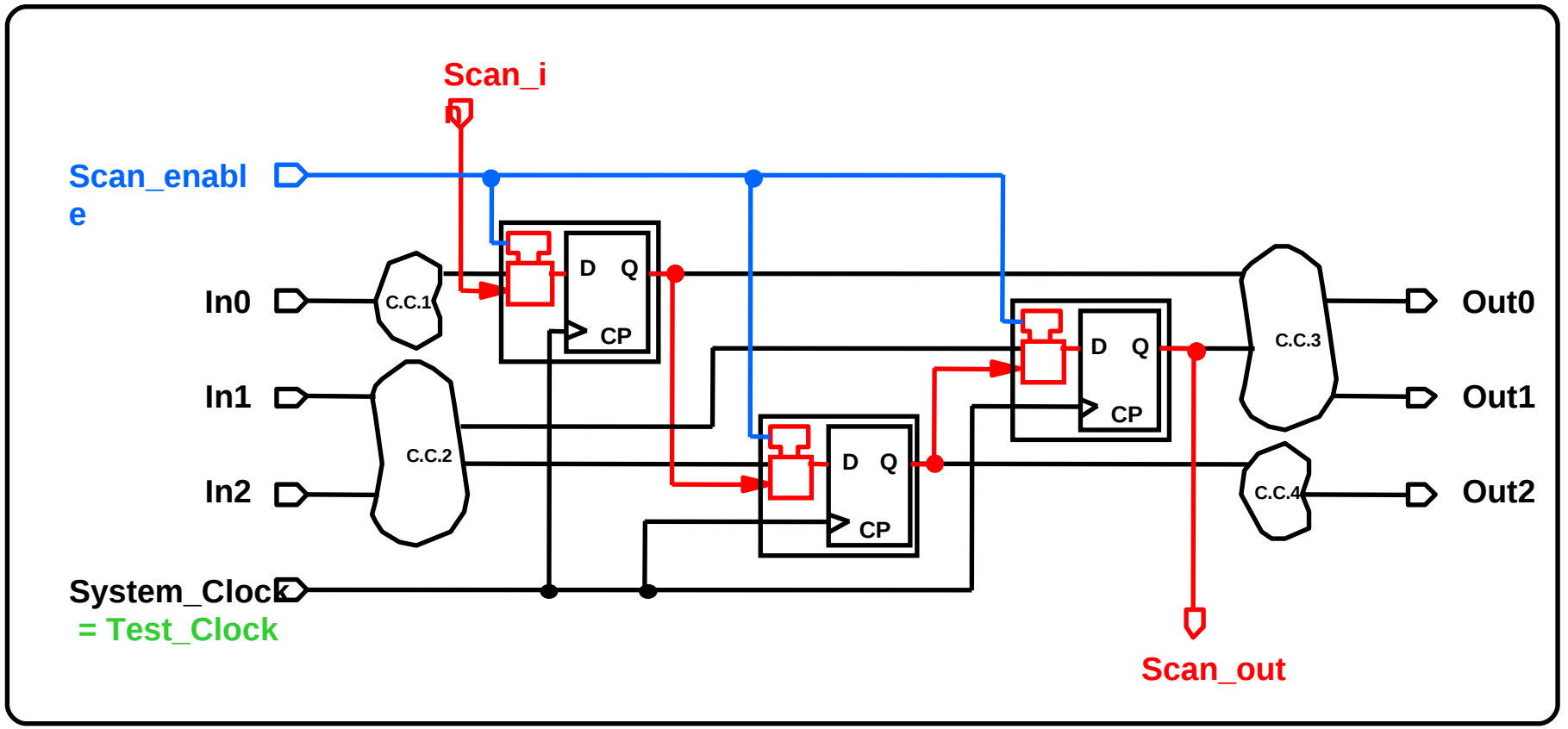


Treat FF1~FF3 as virtual input-output ports and handle the entire circuit as combination circuit.

Example of Scan (Actual circuit)

Blue:Normal operation/Scan operation switching circuit

Red :Scan circuit



04/17/12

Renesas Design Viet Nam Co., Ltd.

Confidential

OUTLINE

Purpose of Scan design

Outline of Scan design

Basic concepts of Scan

Scan operation

Design operation in Scan mode/User mode

Scan design constraints

Scan ATPG

Scan Fault models

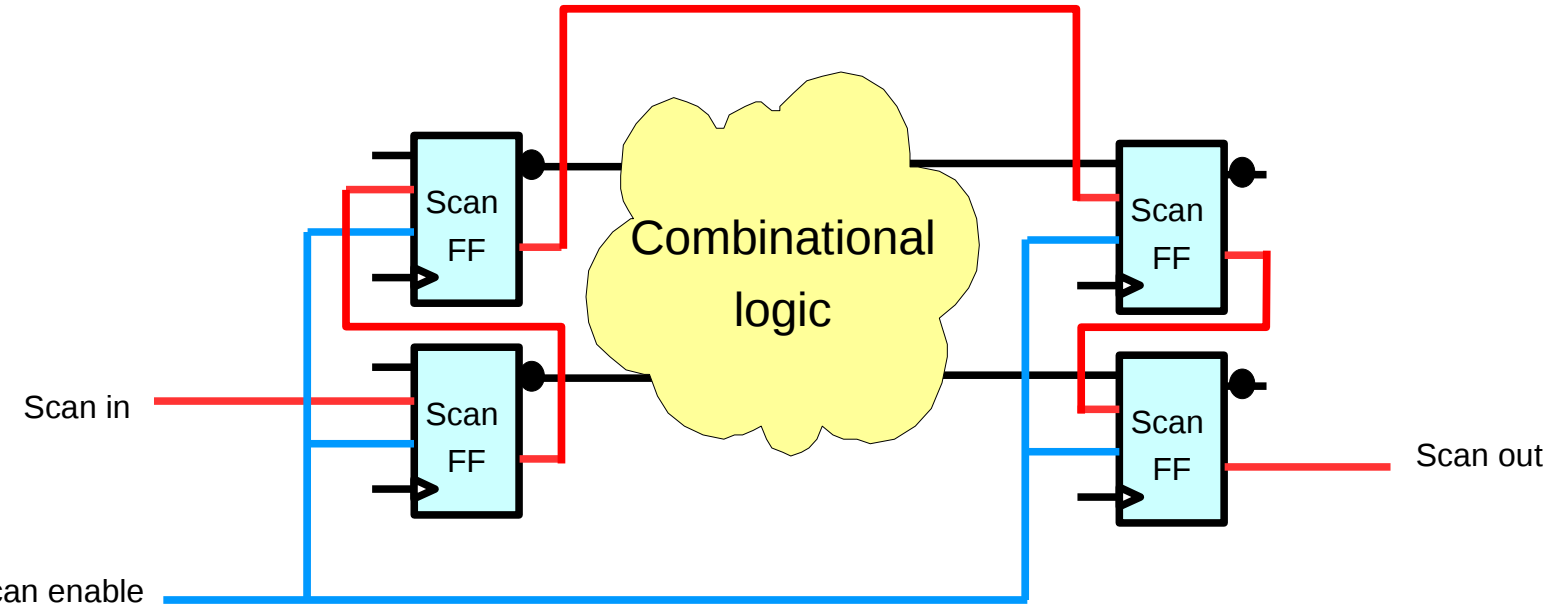
Fault assumption and categories

Basic concepts of Scan (1)

What is scan?

Scan is a technique used in Design For Test.

In scan testing, sequential elements of devices are connected into chains and used as primary inputs and primary outputs for testing purposes.



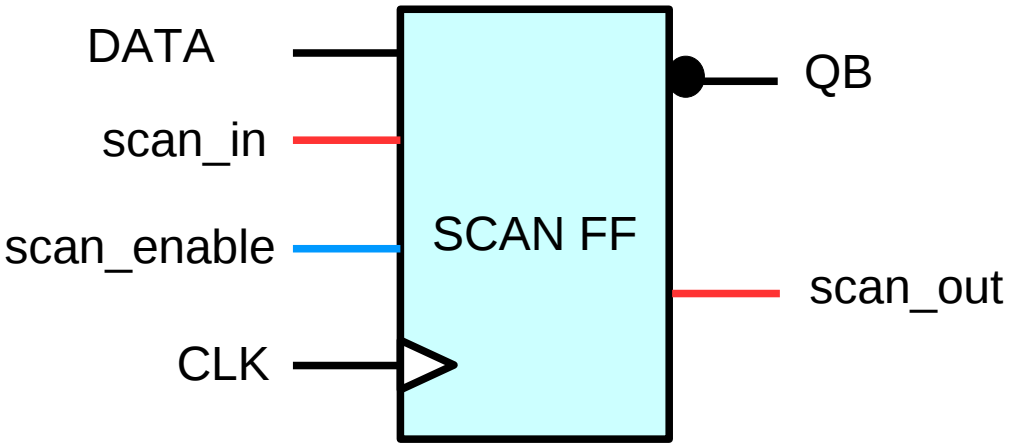
Basic concepts of Scan (2)

Operation of scan FF

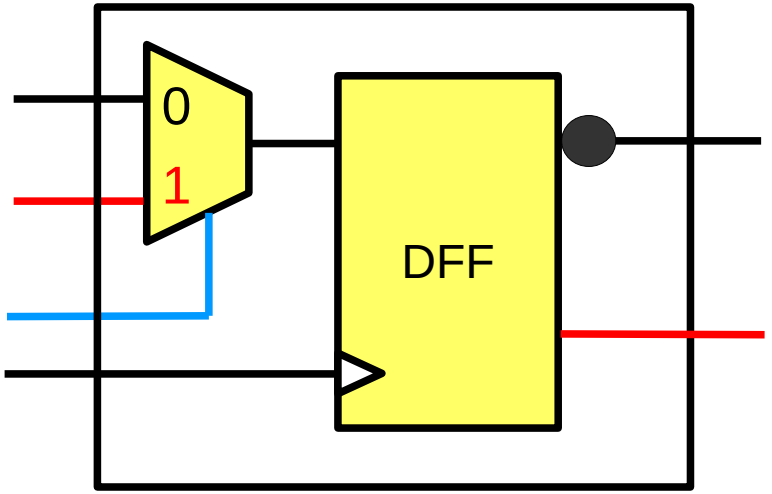
When scan_enable is 0, scan FF operates same as normal FF

When scan_enable is 1, scan FF operates as a shift register

Scan FF block view



Scan FF equivalent model



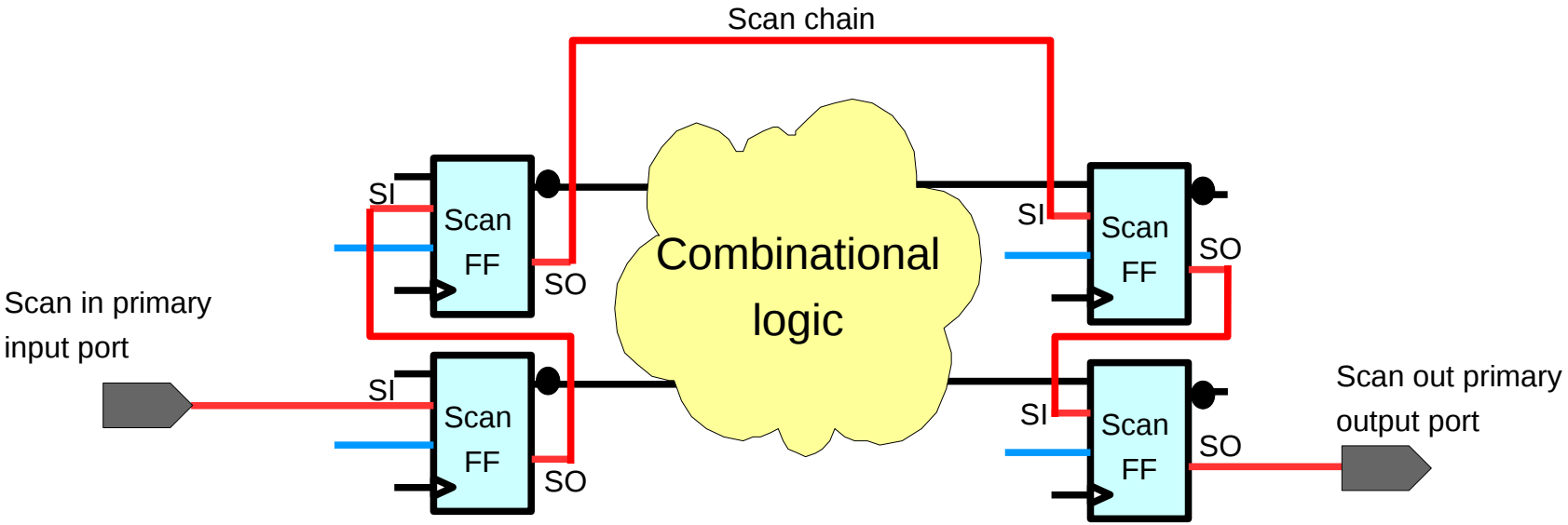
04/17/12

Renesas Design Viet Nam Co., Ltd.

Basic concepts of Scan (3)

What is scan chain?

Scan chain is a chain from primary input go through scan_in/scan_out pins of scan FFs to primary output



Basic concepts of Scan (4)

Types of scan

Full-scan:

All sequential elements in design are built to scan FFs.

Partial-scan:

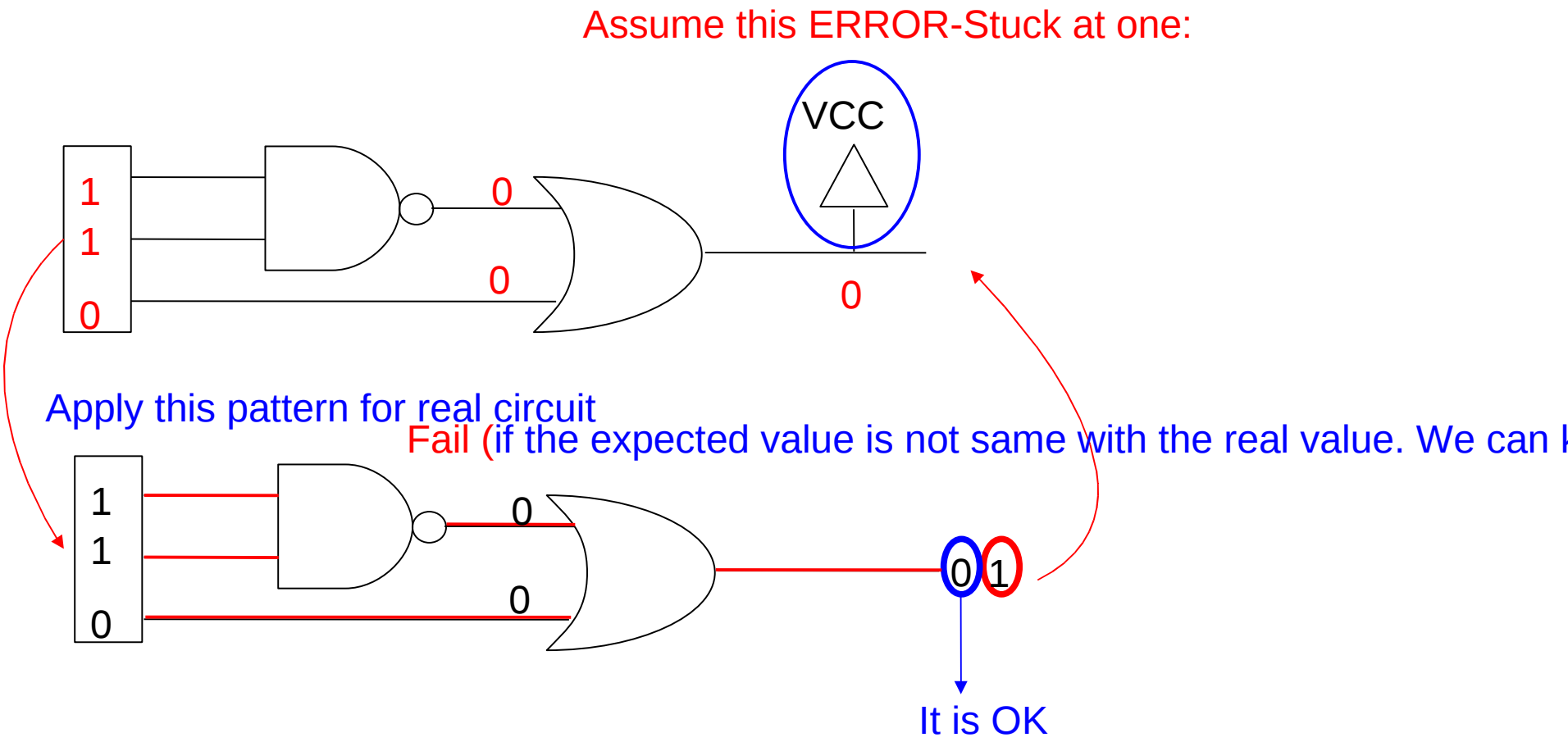
Sequential elements of some modules in design are built to scan FFs.

Almost-scan: Except some special sequential elements in design, all others are built to scan FFs

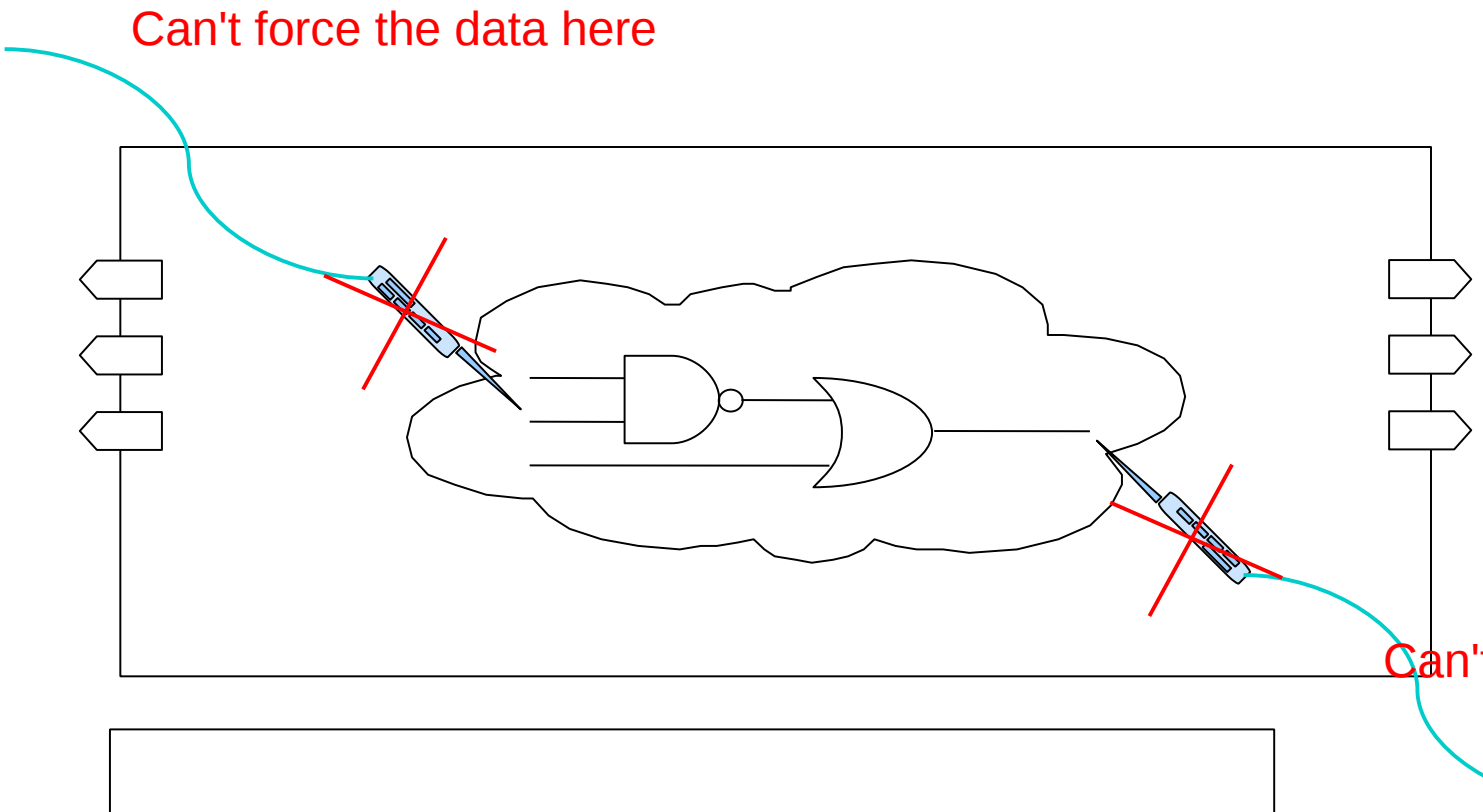
OUTLINE

Purpose of Scan design
Outline of Scan design
Basic concepts of Scan
Scan operation
Design operation in Scan mode/User mode
Scan design constraints
Scan ATPG
Scan Fault models
Fault assumption and categories

Scan operation – How to create pattern

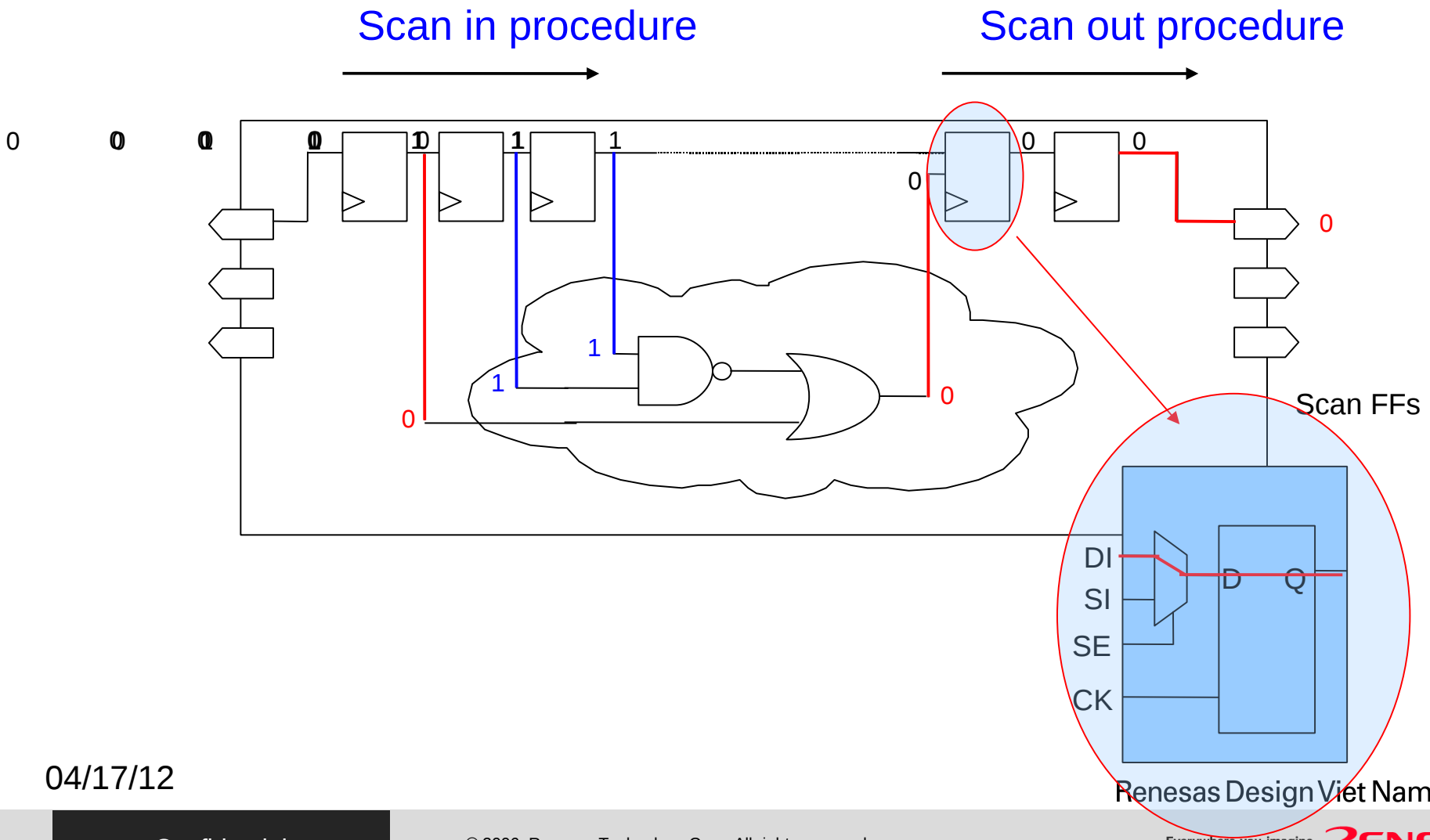


Scan operation – Why scan_chains are necessary to support ATPG



he game: Tester access to Device-Under-Test (DUT) is only allowed through its **primary** I/O port

Scan operation – Why scan_chains are necessary to support ATPG



04/17/12

Renesas Design Viet Nam Co., Ltd.

Scan operation – Scan test procedure

There are 3 procedure:

- Load: is shifting stimulus data from primary input ports through scan chains to right before test target logics.
- Capture: is loading data and waiting responded values at test target logics, then taking them to scan chains
- Unload: is shifting responded values through scan chains to primary output ports

OUTLINE

Purpose of Scan design
Outline of Scan design
Basic concepts of Scan
Scan operation
Design operation in Scan mode/User mode
Scan design constraints
Scan ATPG
Scan Fault models
Fault assumption and categories

Design operation in Scan mode

Set external pins to activate scan_mode (setup test_decoder)

In scan_mode, there is the controlled signal “scan_mode/test_mode” which is always active.

All clock/set/reset signal will be controlled directly from external ports.

All data will be feed and probed through scan_in/scan_out ports.

Scan_enable signal control scan test protocol. It control to switch between shift and capture data.

All clock gated cells, latch cells will be active to pass clock through them.

Design operation in User mode

Set external pins to activate user_mode (setup test_decoder)

In user_mode, the controlled signal “scan_mode/test_mode” which is always inactive.

All clock/set/reset signal will be controlled by user logic.

All scan_in/scan_out/scan_enable signal will be disabled.

All clock gated cells, latch cells will be controlled by user logic.

All test circuits (inserted by SCAN) will be disabled.

OUTLINE

Purpose of Scan design
Outline of Scan design
Basic concepts of Scan
Scan operation
Design operation in Scan mode/User mode
Scan design constraints
Scan ATPG
Scan Fault models
Fault assumption and categories

Scan design constraints (1)

Features of SCAN method:

- Suitable for a synchronous design circuit with edge-trigged FFs
- Small area overhead
- Delay overhead is caused only by an increase in set up time
- Scan clock is shared with system clock

Fundamental design constraints

- Feedback loop that consists only of combinational circuit is prohibited
- Only edge-triggered type FF is available
- Each clock/set/reset for each FFs must be controllabe directly from the outside of the chip
- An hold time error between Ffs must not occur during scan shift

Scan design constraints (2)

Design constraints and actions

No.	Design Rule	Example of Violation		Tools' Action	Influence
1	Feedback-Loop that consists only of combination circuits is prohibited	Feedback-Loop that consists only of combination circuits exists.	1-1	Input "X" to the loop	Fault coverage decreases considerably.
2	Only edge-triggered FFs can be used.	Level latch is being used.	2-1	the gate can be controlled: handled as a buffer	Fault coverage decreases slightly.
			2-2	the gate cannot be controlled: handled as a BlackBox	Fault coverage decreases considerably.
		A FF that is not compatible with a Mux FF is being used.	2-3	handled as a BlackBox	Fault coverage decreases considerably.
3	Clocks of all the FFs must be externally controllable.	Gated-Clock is being used. Frequency divider or PLL (Bypass mode modeling/not set) is being used. Reversed-phase clock FF is being used.	3-1	non scan object: Regard the FF supplied with clocks as a BlackBox	Fault coverage decreases considerably.
			3-2	scan object: unsupported	Test impossible
4	All the FFs must be capable of being set/reset externally, or must not operate during scan.	Asynchronous set/reset is generated in a internal logic.	4-1	non scan object: handled as a BlackBox	Fault coverage decreases considerably.
			4-2	scan object: unsupported	Test impossible
5	Hold time violation between FFs must not occur during a scan shift.	Clock skew exceeds FF delay.	5-1	unconsidered the violation	Test impossible
6	Hold time violation must not occur on all paths (including false path) during a test	Hold time violation occurs on false path	6-1	unconsidered the violation	Test impossible
7	Only a single bus can be active during a test.	Internal logic controls bus	7-1	the generated patterns which cause conflicts are excluded	Fault coverage decreases slightly.
8	Treatment of a BlackBox	RAM or ROM is used.	8-1	handled as a BlackBox	Fault coverage decreases considerably.
9	Crystal I/O cannot be used during a test.	Crystal I/O is used as the scan clock.	9-1	unconsidered the violation	Test impossible

Scan design constraints (3)

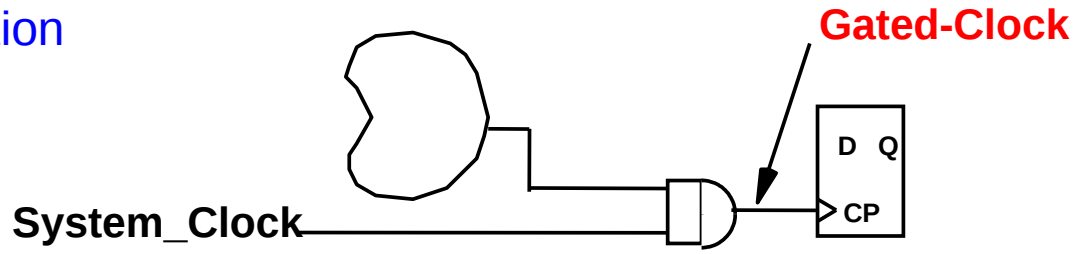
Constraints for clock/set/reset signal and actions

- Clock/set/reset signals must be controllable from external ports
- Any FFs that are not supplied with specified clocks are excluded from scan objects
- Any FFs that are not compatible with scan cell models are also excluded from scan targets
- Any FFs that has uncontrollable set/reset signal are excluded from scan objects
- All non-scanable FFs are treated as BlackBox

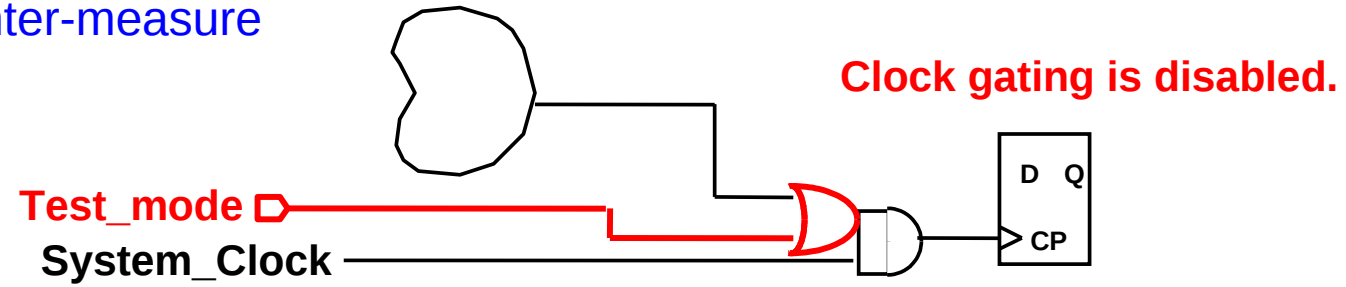
Scan design constraints (4) - Example

Clock of all FFs should be controlled directly from the outside

Example of violation



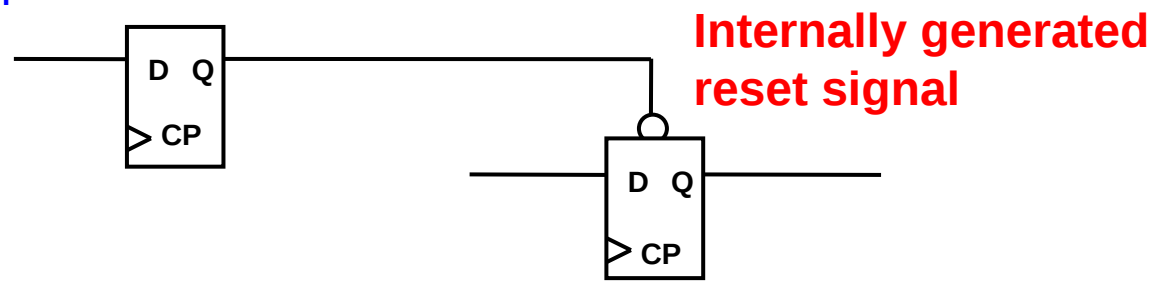
Example of counter-measure



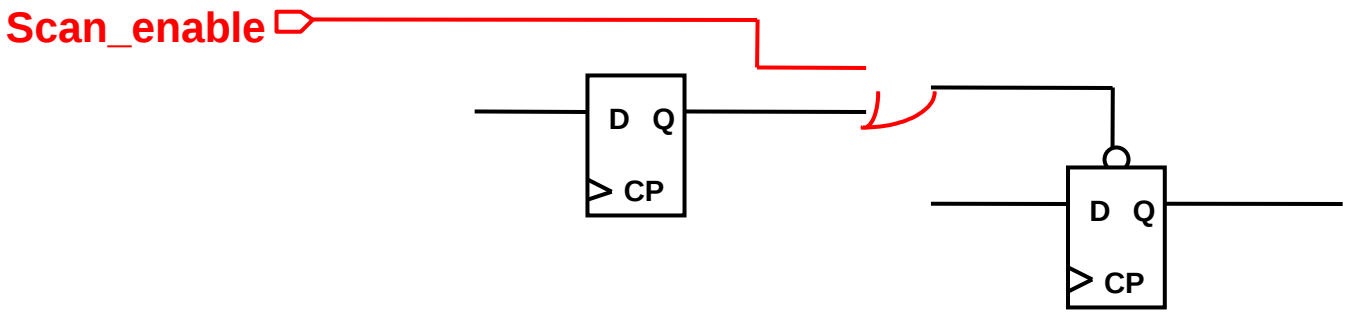
Scan design constraints (5) - Example

Set/reset of all FFs should be controlled directly from the outside or not be operated during SCAN

Example of violation



Example of counter-measure



OUTLINE

Purpose of Scan design
Outline of Scan design
Basic concepts of Scan
Scan operation
Design operation in Scan mode/User mode
Scan design constraints
Scan ATPG
Scan Fault models
Fault assumption and categories

What is ATPG

- ATPG stands for Automatic Test Pattern Generator.
- The tool to generate test patterns automatically.
- ATPG is executed to the logic to which Scan is inserted.
- ATPG for combination circuits (practical technology)
  - ATPG that can handle only combination circuits
  - Test patterns are generated assuming that they are applied to Full Scan circuits.

Scan ATPG – ATPG modes

APTG modes (base on test frequency)

DC (direct current) mode:

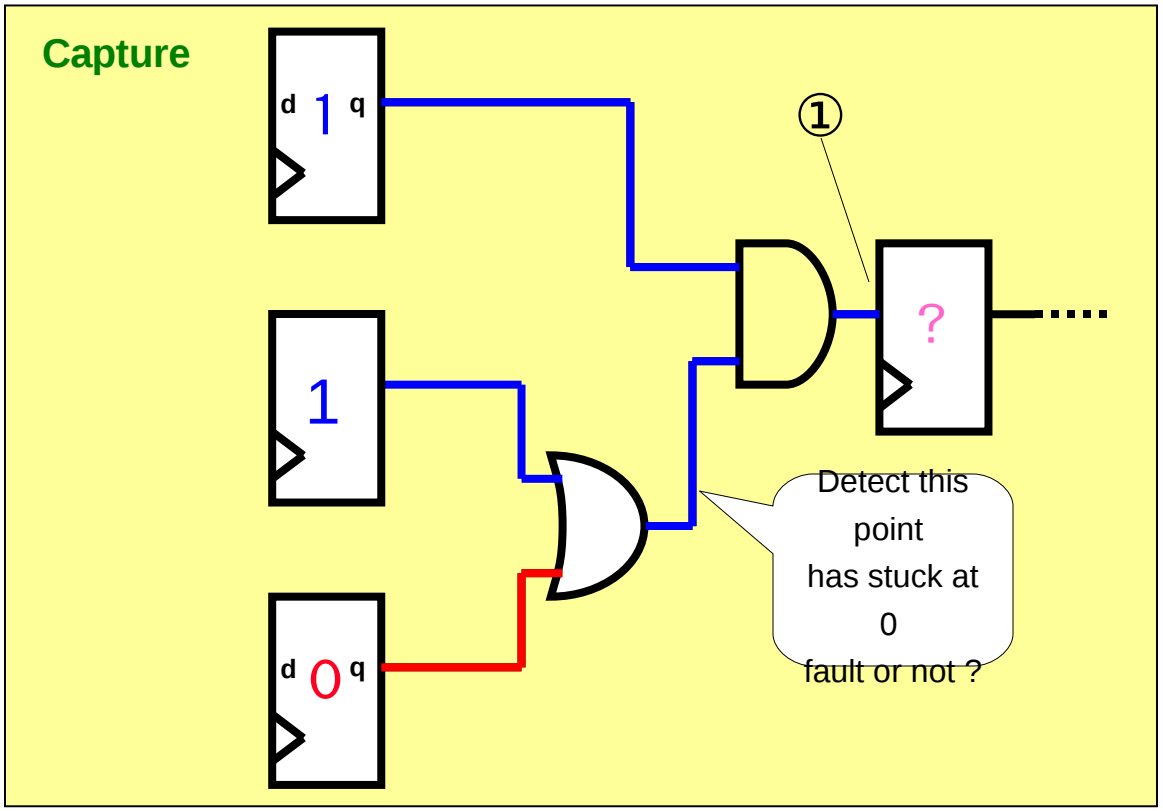
- Stuck-at fault detection
- Using slow clock to capture data

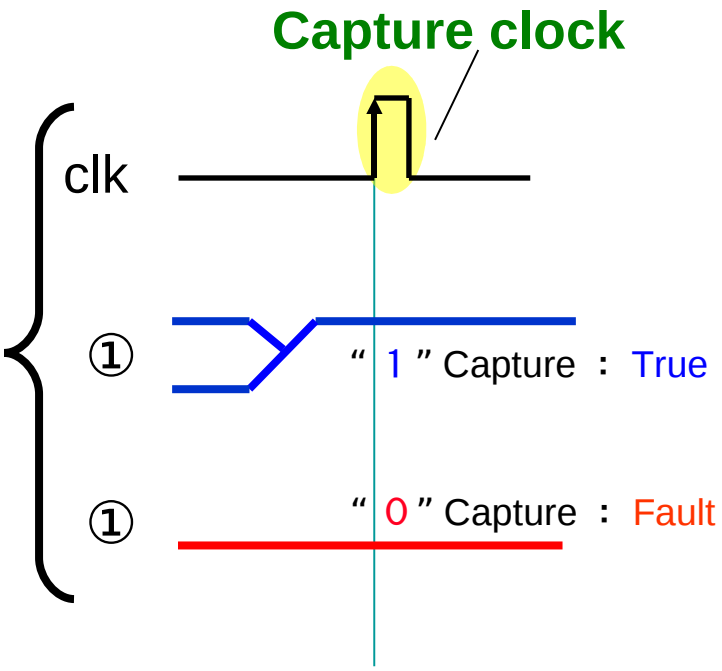
AC (alternating current) mode:

- Transition fault detection
- Using at-speed clock to capture data

Scan ATPG – DC Scan mode

DC mode (stuck-at fault detection)

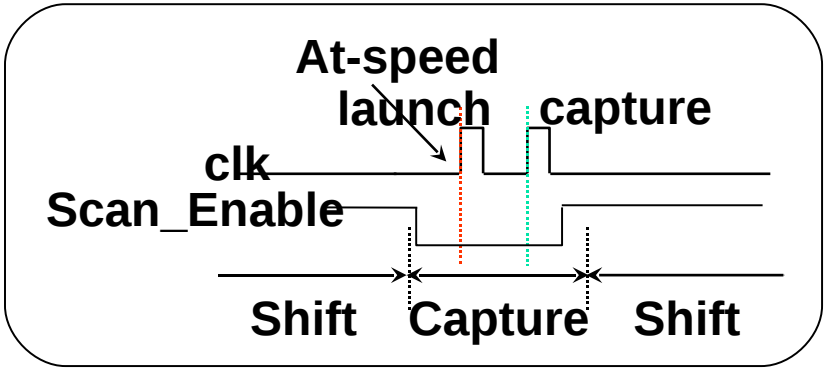




Scan ATPG – AC Scan mode (1)

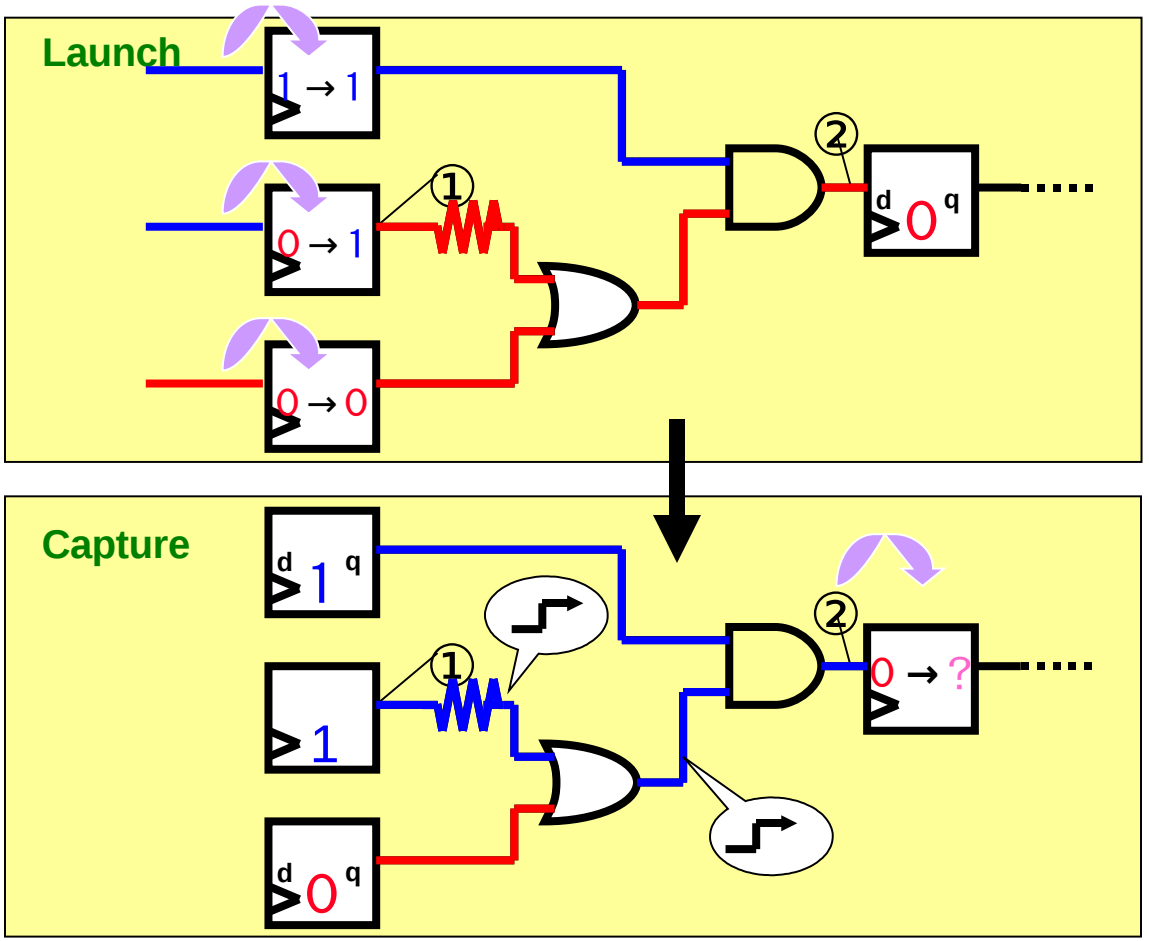
- **Delay-induced failure increases due to miniaturization**
  - Difficult to detect it using stuck-at failure model
  - Minimal delay failure causes critical problems in high-speed LSI

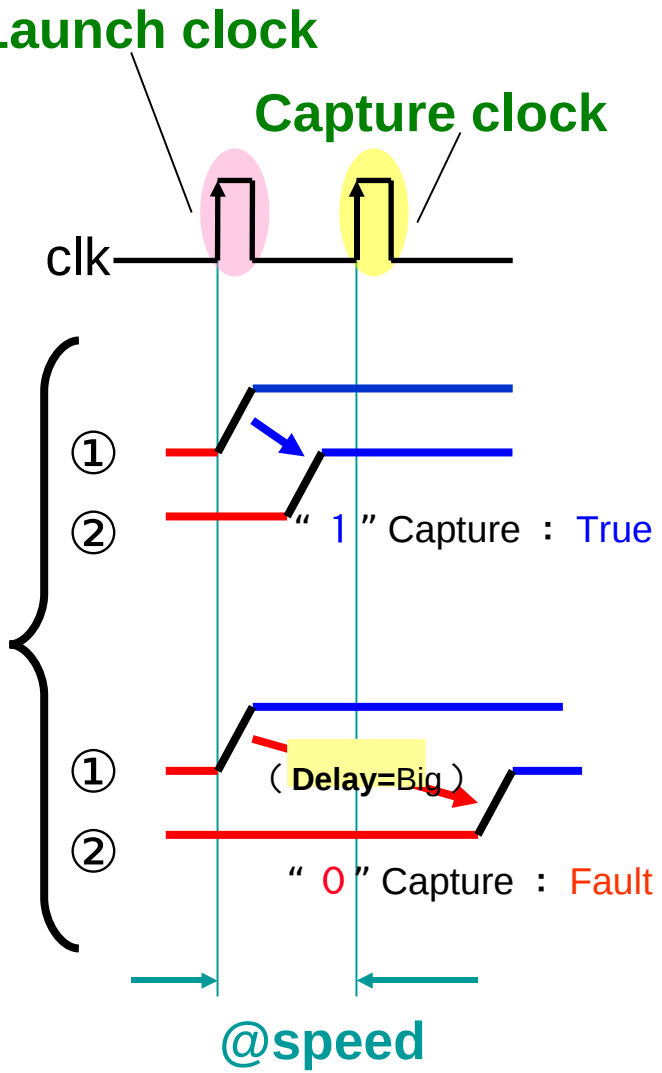
- **Apply AC scan test**
  - Adopt MUX scan test method
  - Use transition failure model
  - Input the test pattern and observe at speed
  - Test pattern generation methods
    (a) Launch-off-Shift (LOS)
    (b) Launch-off-Capture (LOC)



Scan ATPG – AC Scan mode (2)

AC mode (transition fault detection)





04/17/12

Renesas Design Viet Nam Co., Ltd.

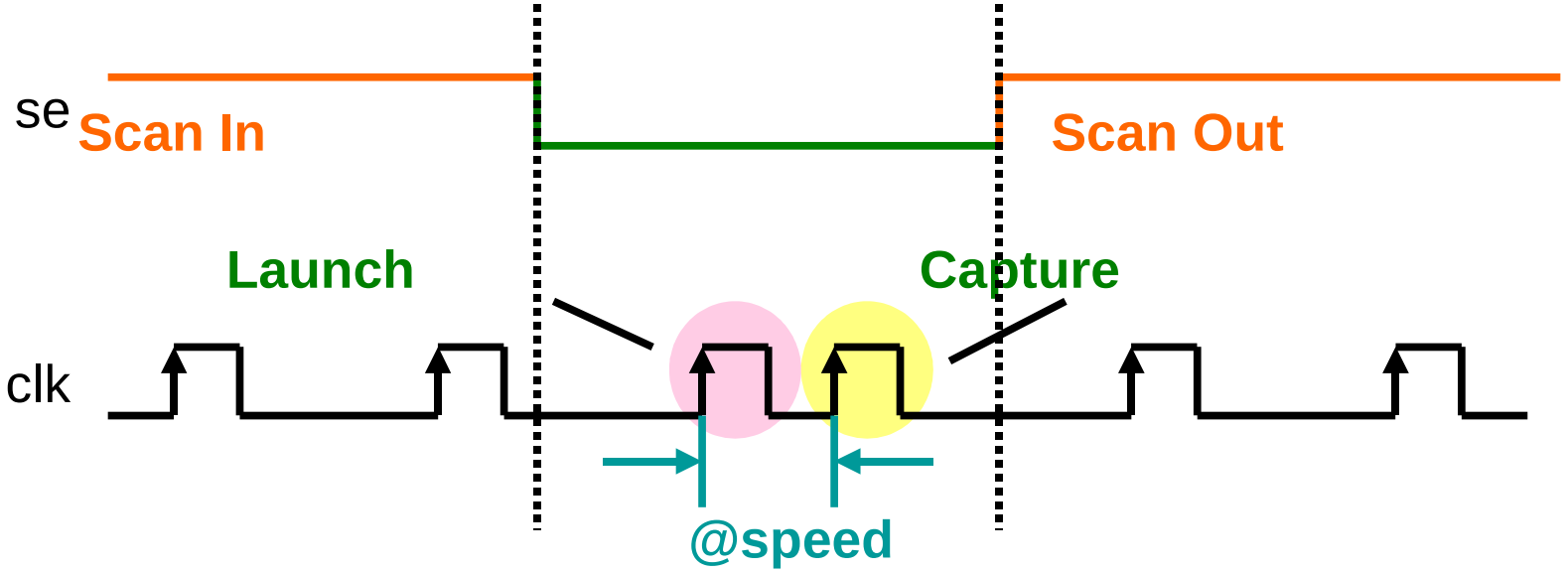
Scan ATPG – Pattern generation methods (1)

AC – Broad-side :

Launch/Capture operates in System mode.

Easy to control timing of scan_enable signal

Test coverage not higher than expected



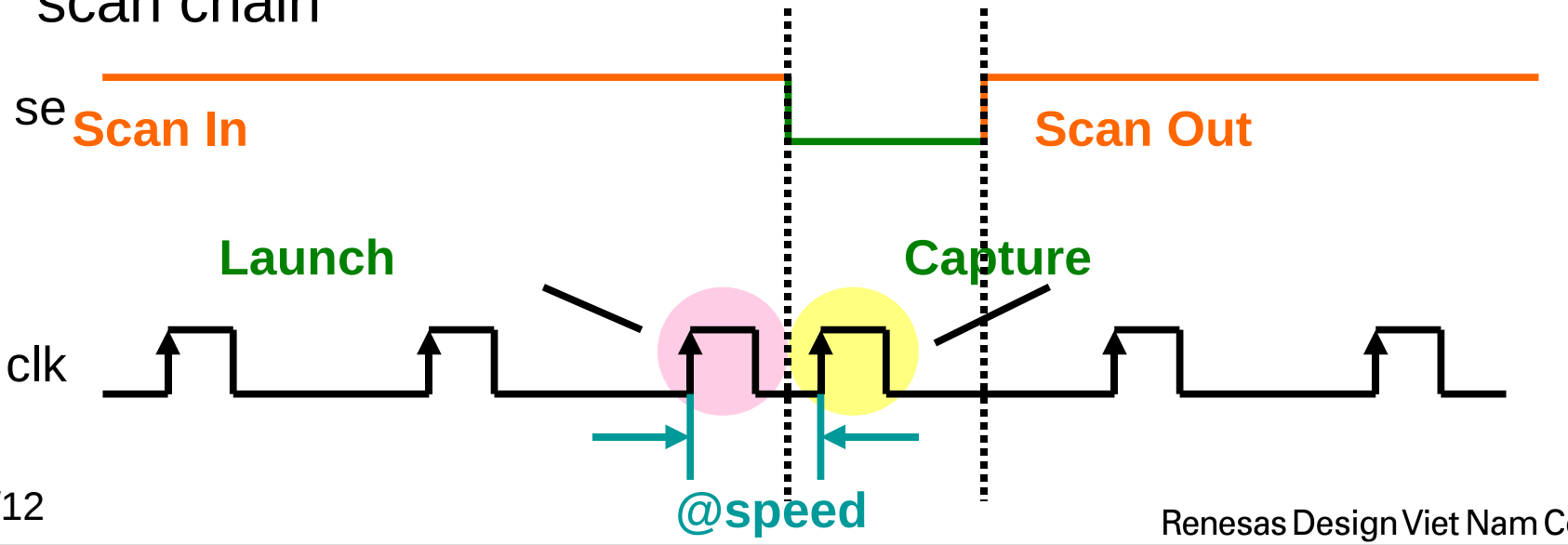
Scan ATPG – Pattern generation methods (2)

AC – Skewed-load :

Launch pulse is in Scan mode, Capture pulse is in System mode.

Difficult to control timing of scan_enable signal

Enable to set pattern for higher test coverage directly through scan chain



OUTLINE

Purpose of Scan design
Outline of Scan design
Basic concepts of Scan
Scan operation
Design operation in Scan mode/User mode
Scan design constraints
Scan ATPG
Scan Fault models
Fault assumption and categories

Scan Fault models (1)

There are 3 models which are applied in RVC

- Stuck-At Fault model
- Transition Fault model
- Path-Delay Fault model

Scan Fault models (2)

Stuck-At fault

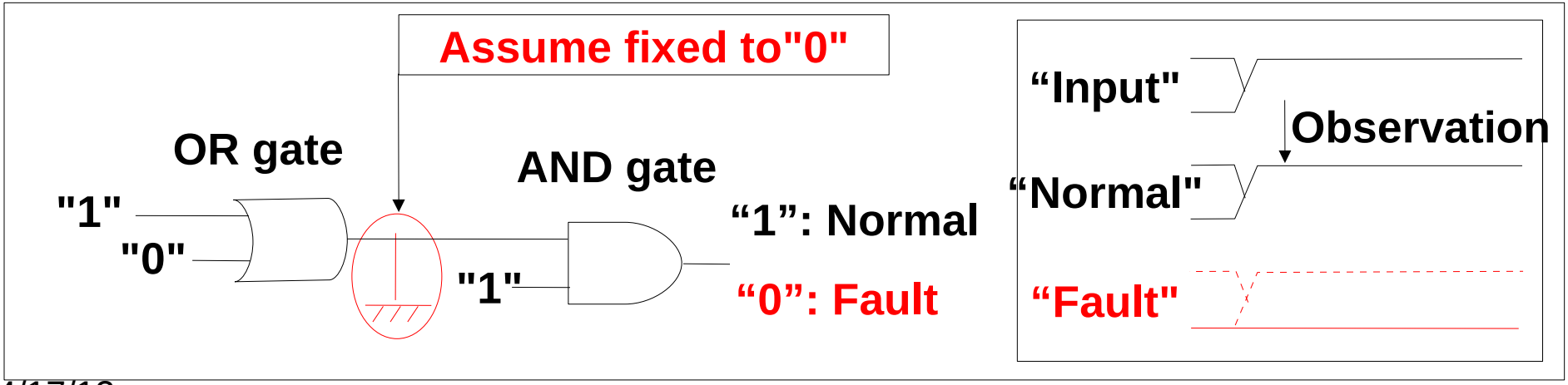
Fault assumption :

- Assuming 1/0 fault to all pins of a cell, and make report without reduction
- There exists logically equivalent faults.

Fault detection :

1) Set reverse value of 1/0 at the position where 0/1 fault is assumed.
2) If the change is observed at the observation point (output pin or Scan FF), then the fault can be detected.

Only one line in the circuit is faulty at a time.



Scan Fault models (3)

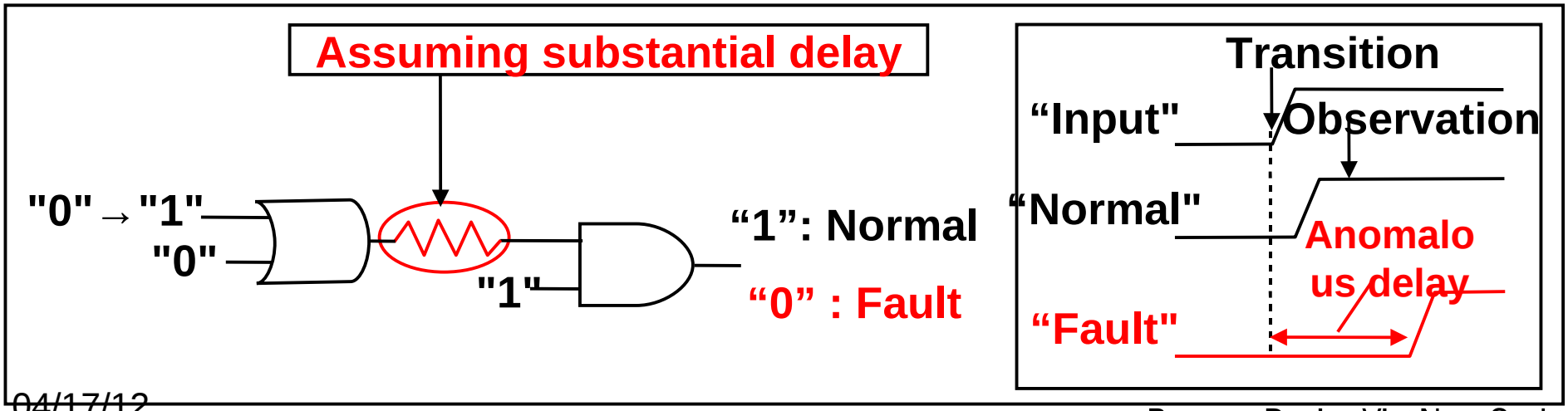
Transition fault

Fault assumption :

Assume a large delay that can not be propagated within one clock cycle at all pins of a cell. The equivalent faults are reduced by a tool.

Fault detection :

1) Creating transition (0->1,1->0) at the position where the delay fault is assumed
2) If transition is 0->1, observing “1” is OK, observing “0” is fault detected.
   If transition is 1->0, observing “0” is OK, observing “1” is fault detected.



04/17/12

Renesas Design Viet Nam Co., Ltd.

Scan Fault models (4)

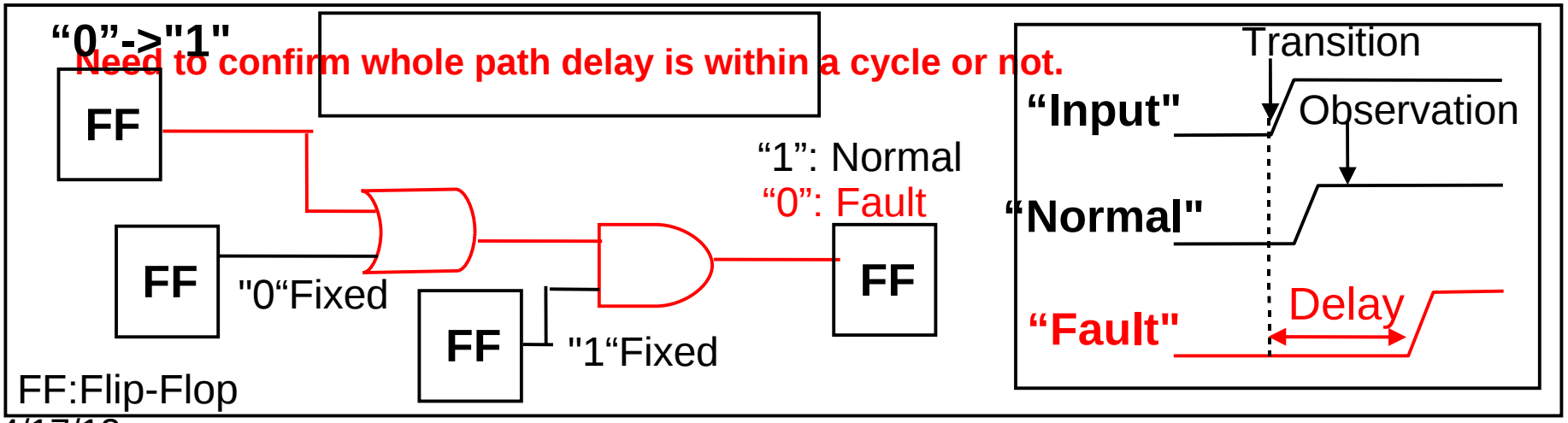
Path delay fault

Fault assumption :

Assuming a fault to a specific path by considering the result of STA (Static Timing Analysis) and critical paths

Fault detection :

Maintaining that the whole path is not affected by other signal changes during test, and evaluate that the signal transition is transferred through the tested path within a cycle.



Scan Fault models (5)

Measurement condition

	Stuck-at	Transition	Path delay
Test frequency	SLOW CLOCK	AT-SPEED CLOCK	AT-SPEED CLOCK
The selection of target path for test	ALL PATHs	EXCEPT false paths and multicycle paths	FORCUS TO user-defined paths and worst paths in STA

NOTE :

At-speed clock is clock that has the same frequency as operating clock of product.

OUTLINE

Purpose of Scan design
Outline of Scan design
Basic concepts of Scan
Scan operation
Design operation in Scan mode/User mode
Scan design constraints
Scan ATPG
Scan Fault models
Fault assumption and categories

Fault assumption and categories (1)

Fault assumption:

0/1 fault assumptions are set to all the cells (defined in the library) and all the pins (including inputs, outputs, inouts) at the top level.

Formula:

Total fault assumptions = (all pins in all cells + all pins at top level) x 2

Example:

BUF has 1 input pin and 1 output pin

→ Total stuck at fault of BUF cell = 4

- Stuck at 0 at input
- Stuck at 1 at input
- Stuck at 0 at output
- Stuck at 1 at output

Fault assumption and categories (3)

Fault categories

FU (Full): total fault assumption

Detectable

UD (Undetected) = UC + UO

UC (Uncontrolled), UO (Unobserved)
Specifies the faults that the patterns to detect are failed to generate. (including the cases that ATPG is closed out or bus contention)

DT (Detected) = DS + DI

DS(Detected-simulation), DI (Detected-Implication)
Specifies the faults that the patterns to detect are successfully generated

Fault assumption and categories (4)

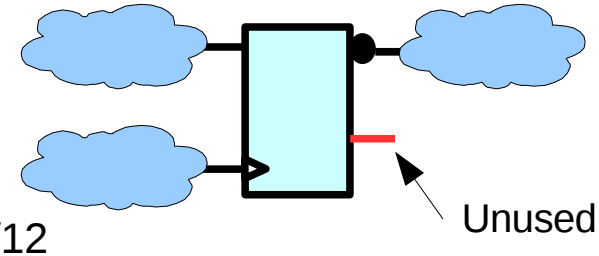
Fault categories (cont.)

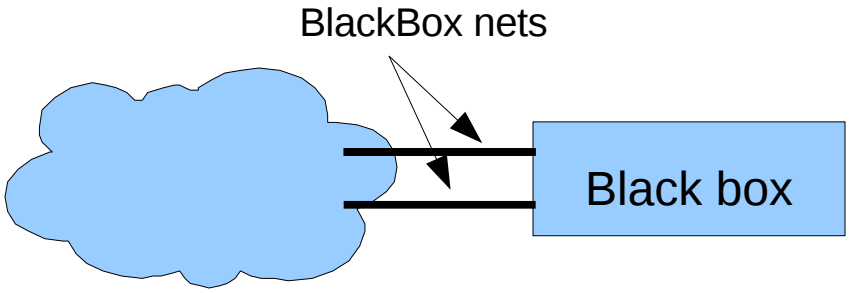
Undetectable

PD (Possible-detected) = PU + PT

PU (Possible-detected untestable), PT (Possible-detected testable)
Specified faults which can not be detected because of propagation of “X”. This category includes the faults effect become “Z”.

UU (Unused)
Specified faults which can not be detected because pin is NOT USED. (unused in/out/input pins, nets connecting to BlackBox)





Fault assumption and categories (2)

Fault collapse:

In total fault, there are many equivalent faults. Fault collapse is the number of faults after collapsing equivalent faults in total amount.

Example:

BUF Stuck at 0 at input <=> Stuck at 0 at output
Stuck at 0 at input <=> Stuck at 1 at output
→ fault collapse = 2

Fault assumption and categories (5)

Fault categories (cont.)

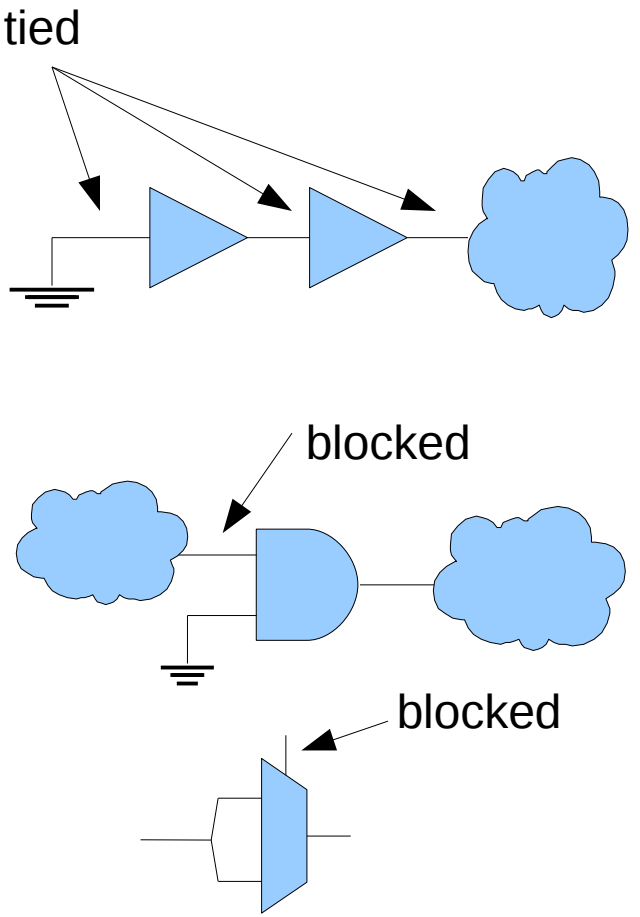
Undetectable

TI (Tied)

Specified faults which can not be detected because of fixing HIGH/LOW in netlist. The pin constraints when running ATPG are not included.

BL (Blocked)

Specified faults which can not be detected because of blocking by fixing HIGH/LOW. This category included the select pins where the same inputs are feed. The pin constraints when running ATPG are not included.



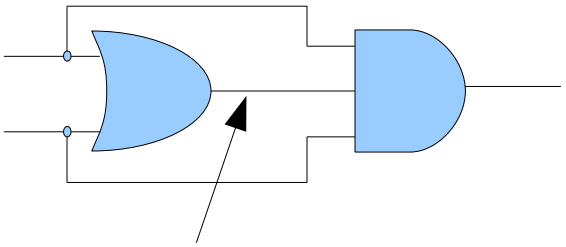
Fault assumption and categories (6)

Fault categories (cont.)

Undetectable

RE (Redundant)

Specified faults which can not be detected because of redundant logics.



AU (ATPG untestable)

Specifies faults that can not be detected because of APTG configuration. This category includes pin constrains and output pin connected to BlackBox.

Fault assumption and categories (7)

Statistics report

fault class	#faults (coll.)	#faults (total)
FU (full)	20191964	33163676
UC (uncontrolled)	44876	77000
DS (det_simulation)	16809954	28390205
DI (det_implication)	2922933	4089178
PU (posdet_untestable)	922	1355
UU (unused)	202003	295564
TI (tied)	62540	100083
BL (blocked)	38176	48372
RE (redundant)	94754	129802
AU (atpg_untestable)	15806	32117
test_coverage	99.69%	99.66%
fault_coverage	97.73%	97.94%
atpg_effectiveness	99.78%	99.77%
#test_patterns		6997
#basic_patterns		4247
#clock_sequential_patterns		2750
#simulated_patterns		6997
CPU_time (secs)		28368.8

UD = UC + UO

DT = DS + DI

PD = PU + PT

$$\text{Test coverage} = \frac{DT}{FU - (UU + TI + BL + RE)}$$

$$\text{Fault coverage} = \frac{DT}{FU}$$

Renesas Design Viet Nam Co., Ltd.