Everywhere you imagine. RENESAS

Compressed SCAN

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Confidential

OUTLINE

Why Compressed Scan

What is Compressed Scan

Where Compressed Scan in design flow

How to implement Compressed Scan

When apply Compressed Scan

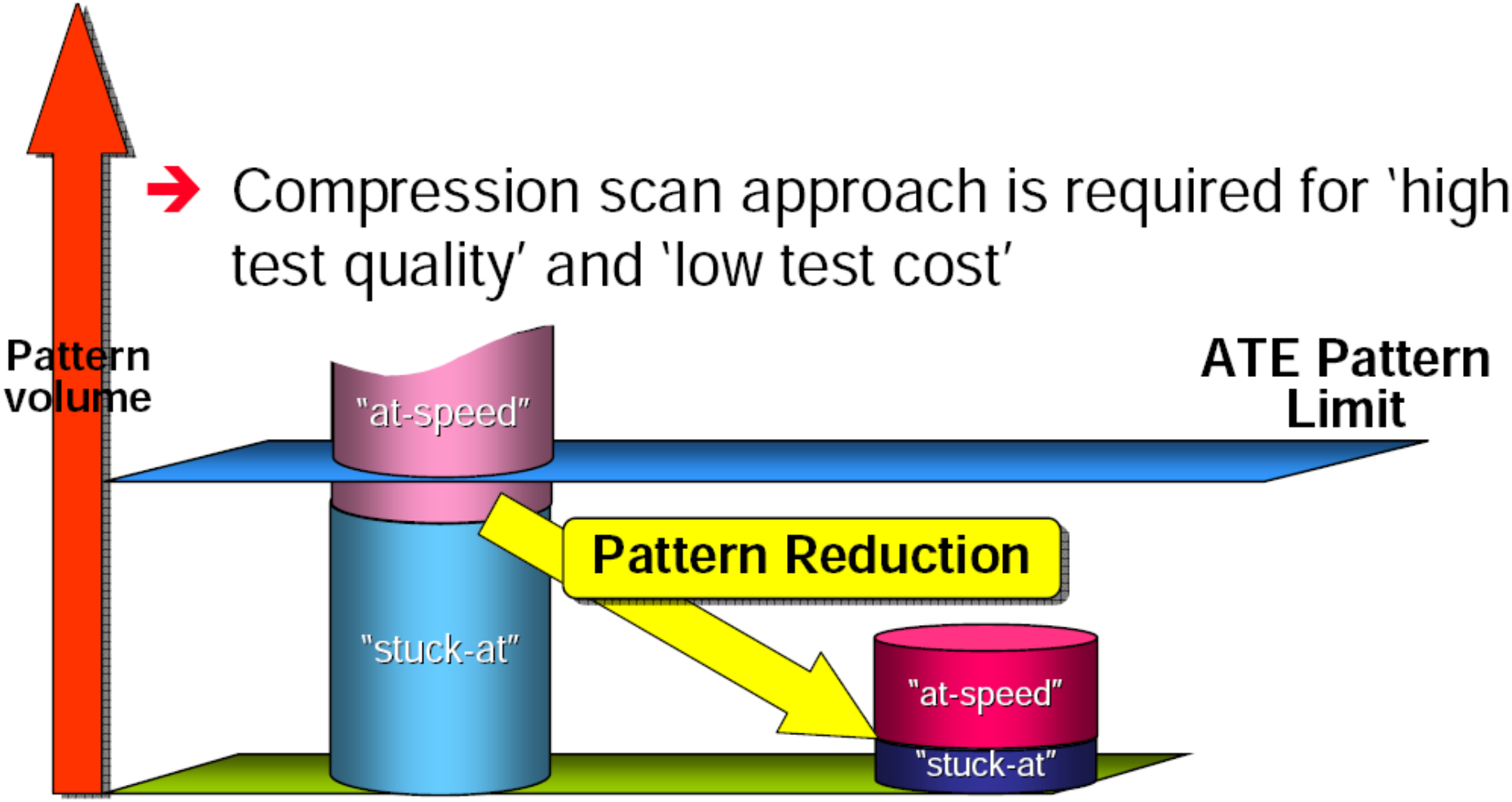
Why Compressed Scan (1)

Problems with NORMAL SCAN test

- Test data problem:
  - Chip size: increase
  - Chip function: increase
  - → increasing test pattern volume, test time
- Tester's memory problem:
  - Big patterns → using more expensive ATE
  - Pattern volume exceeds the memory size in ATE
  - → Increasing test cost, chip cost

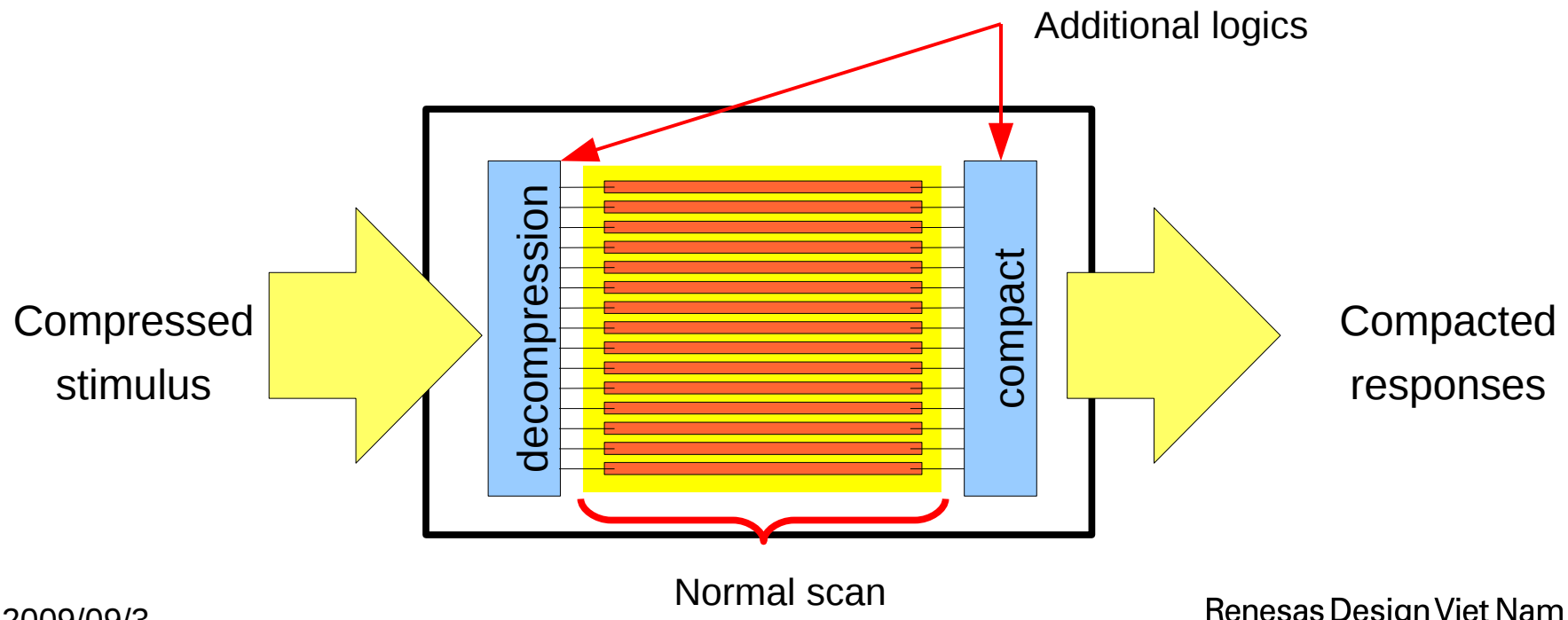
Why Compressed Scan (2)

Effective solution

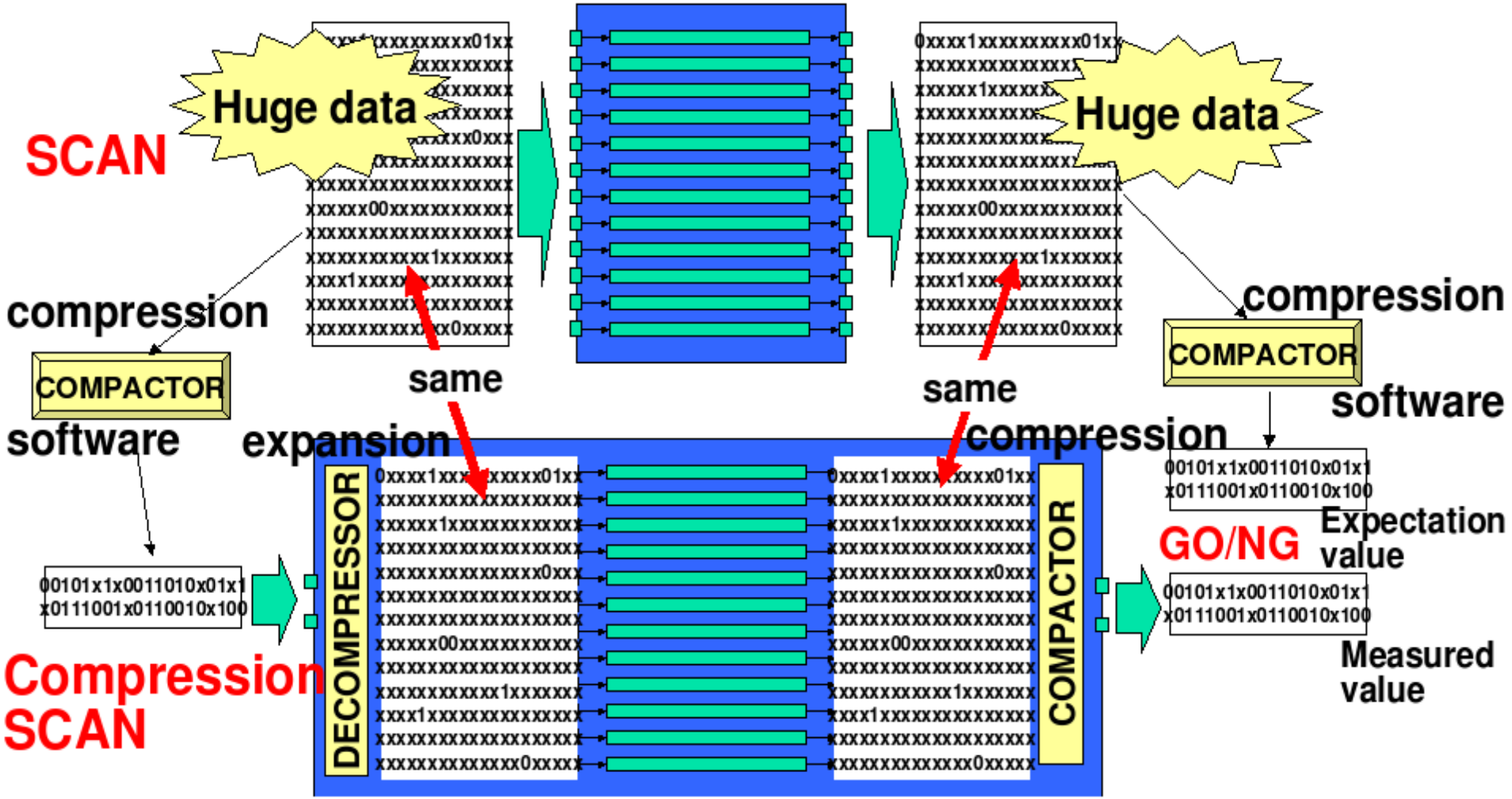


What is Compressed Scan (1)

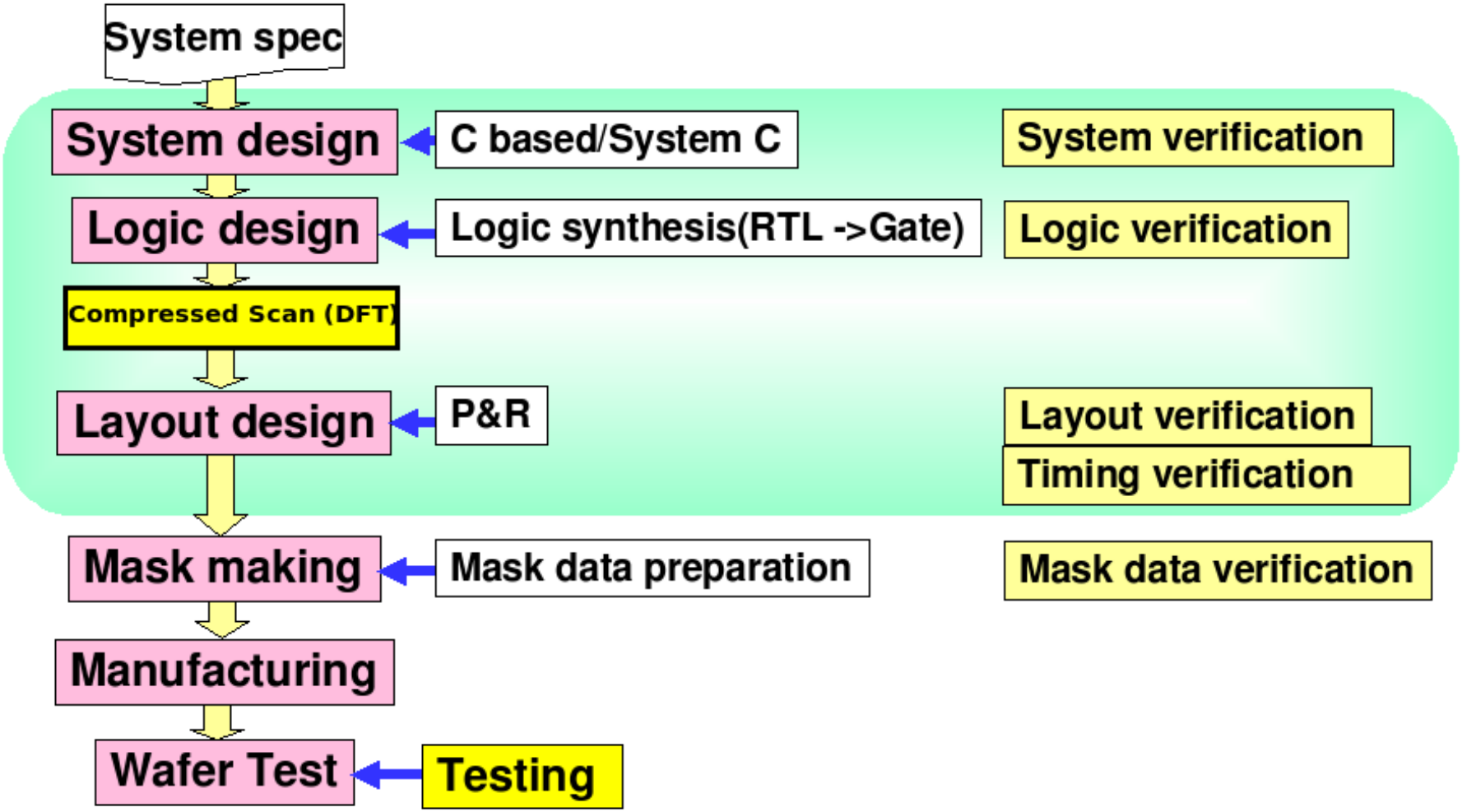
It is a method used to reduce the pattern volume when running ATPG for normal scan designs by adding additional logics inside those designs.



What is Compressed Scan (2)



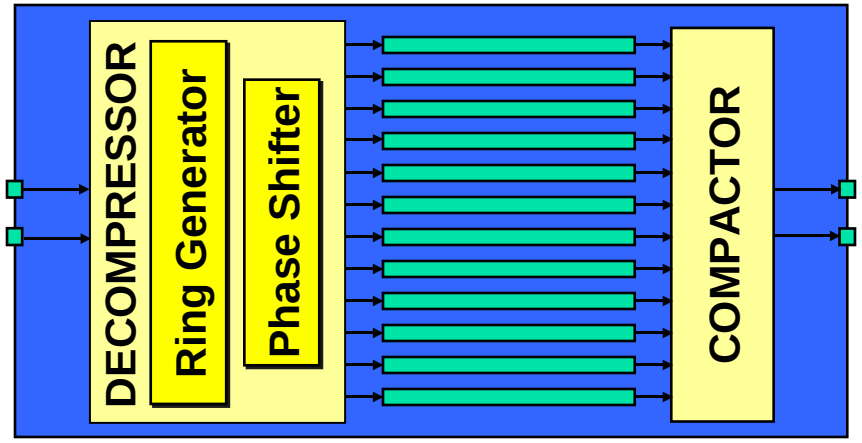
Where Compressed Scan in design flow



How to implement Compressed Scan (1)

TestKompress (Mentor)

- Ensure the same fault coverage as the normal ATPG
- Enable pattern generation for stuck-at, transition, and path delay faults
- Automatically insert SCAN + Compression/Expansion circuit IP
  - Decompressor : Ring Generator (LFSR) + phase shifter (EXOR)
  - Compactor : EXOR-Tree (with Indefinite and aliasing block function)
  - Circuit overhead : about 17Gate per an internal chain
- Realize about 1/100 of pattern compressibility

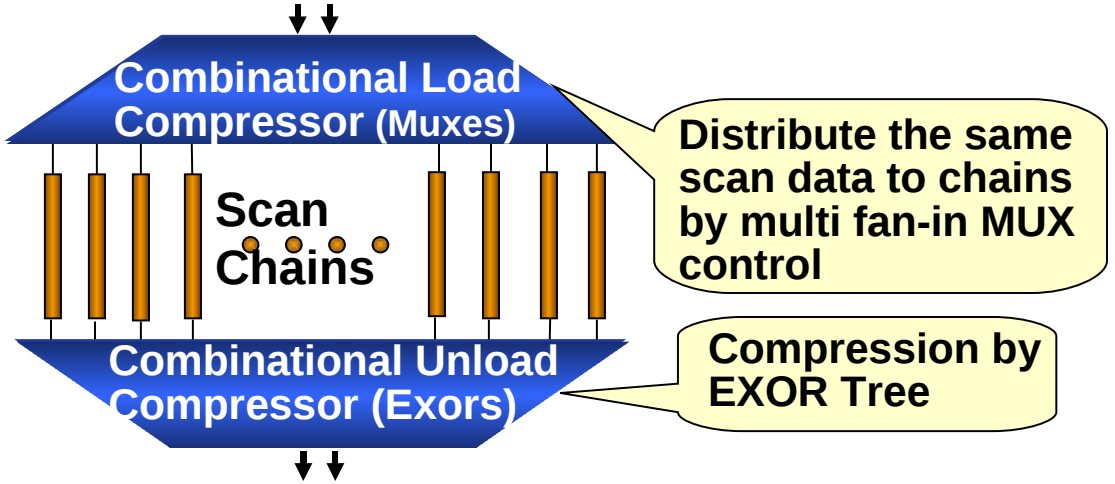


LFSR : linear feedback shift register

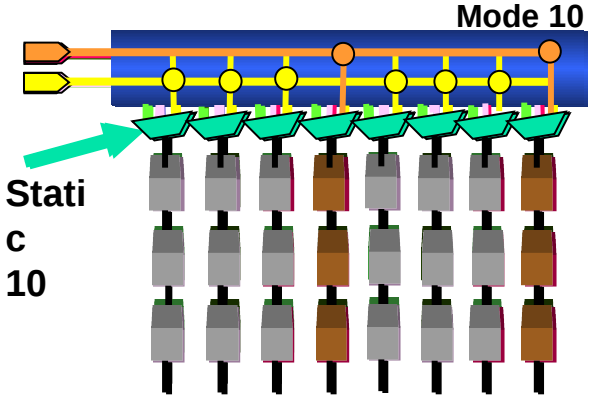
How to implement Compressed Scan (1)

DFTMAX (Synopsys)

- Ensure the same fault coverage as the normal ATPG
- Enable pattern generation for stuck-at, transition, and path delay faults
- Automatically insert SCAN + Compression/Expansion circuit IP
  - Decompressor : multi fan-in MUX control (Illinois scan method)
  - Compactor : EXOR-Tree (with Indefinite and aliasing block function)
  - Circuit overhead : about 13Gate per an internal chain
- Realize about 1/60 of pattern compressibility



Input-side compactor principle



When apply Compressed Scan

Tool	FastScan TetraMAX	DFTMAX	TestKompress	singen
Methodology	Scan	Compression Scan	Compression Scan	LBIST
Design Size	<1M Gate	<2M Gate	<20M Gate	20M Gates<
Design Constraint	Easy (MUX-Scan)	Easy (MUX-Scan)	Easy (MUX-Scan)	Hard
Area Overhead	Scan	Scan + Adaptive Scan (0.1%-0.5%)	Scan + EDT (0.3%-1.0%)	Scan + LBIST + TP (2.0%)
Compression ratio	1	10x-60x	10x-260x	100x-1000x
Low Pin Test	Not available	Not available	Available	Available
At-Speed Test	Single clock domain	Single clock domain	Multiple clock domain (<3clock domain)	Multiple clock domain

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