

OPENCAD

Renesas Advanced Design Platform

**MuxScan/LogicBist/MemoryBist
DFTcheck User's Guide V2.28**

Renesas System Design Corp.
Elemental Technology Development Division 1
Design Automation Dept.
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[Release Notes]

• v2.28 Dec.24 2016

- (1) In DFT305-1, NMA 6bit correspondence was added.
- (2) In DFT307-1, TE5 pin was added.

• v2.27 Sep.24 2016

- (1) DFT023-02 was added.
- (2) The function of -CANCEL_CHECK_VMC option was expanded.
- (3) The function of Collared_memory_extra command was expanded.
- (4) DFT021-8 was added.
- (5) DFT021-9 was added.
- (6) -Unknown_External_Pin option was added.
- (7) The unconnected net was added to target of DFT021-2 check.
- (8) The Note of DFT018 was added.
- (9) The functions of DFT021 were expanded.
- (10) set_strings command (OBSERVE_type) was added.

• v2.26 Mar.24 2016

- (1) DFT023 was added.
- (2) DFT004-6/7 was added.
- (3) Clock sequential test correspondence (DFT Shift_register)
- (4) Tessent new feature correspondence

• v2.25 Sep.24 2015

- (1) -CANCEL_SELECT_DC option was added to set_strings command (POST_DFT).
 - (2) Chapter 6 was revised.
 - (3) SENGGEN of the soft module was added as check target.
 - (4) DFT021 was added.
 - (5) DFT022 was added.
- v2.24 Mar.24 2015
- (1) set_strings command (Cancel_DFT002_01_async_reset_check) was added.
 - (2) DFT501-4 was added.
 - (3) Unknown_External_Pin was added.
 - (4) Since TCL debug command has the equal function, the following options were abolished.
-TRACE_FROM/-TRACE_TO/-TRACE_GATE_INFO/-TRACE_DETAIL/-TRACE_LIMIT

• v2.23 Nov.24 2014

- (1) Error level of DFT014-1 was changed.
- (2) Name rules of Collared_memory were added.
- (3) Specifications were changed for Tessent LBIST.
- (4) -PROCESS option was added.
- (5) set_strings command (Cancel_wrapper) was added.
- (6) DFT307-2 was added.

• v2.0 March. 31 2006

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1. Overview

This manual describes the method for executing DFTcheck by command lines. Figure 1.1 shows an execution flowchart.

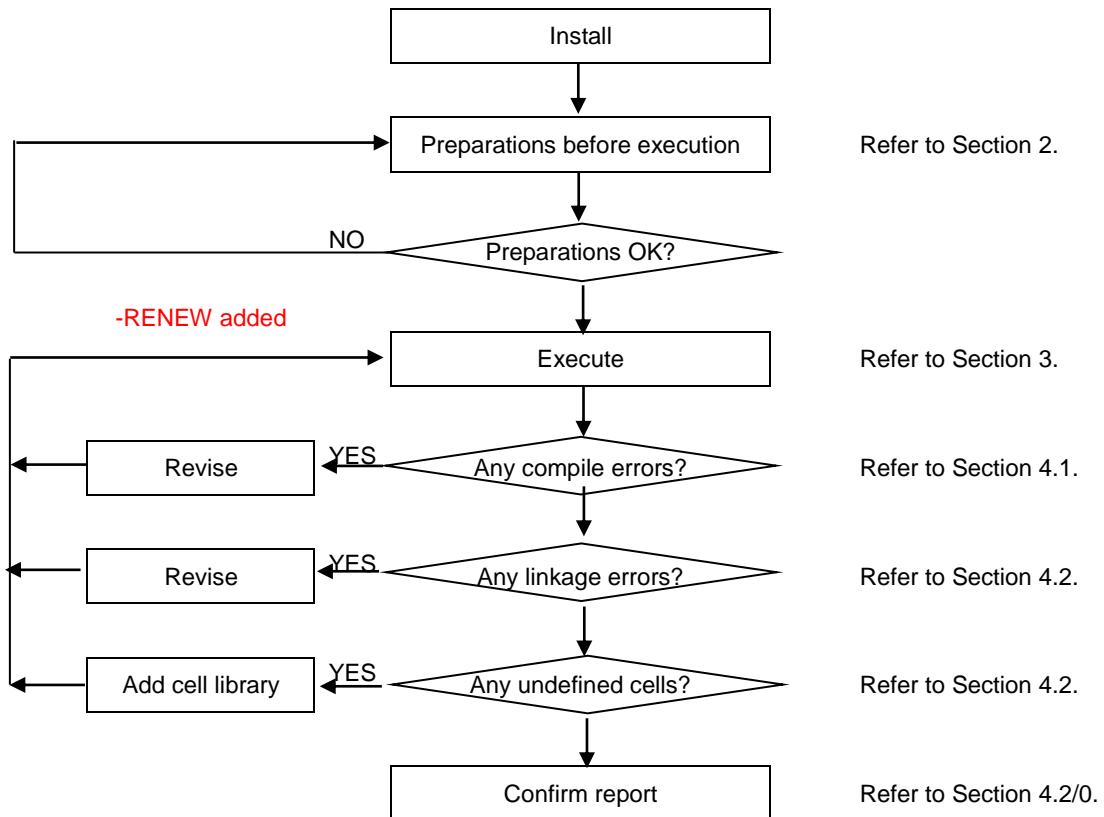


Figure 1.1 Execution Flowchart

2. Preparations before Execution

The following information is required in order to execute DFTcheck. These information elements must always be prepared before implementing this function.

- (1) LSI top block name (described in ‘module’ text of Verilog-HDL or ‘entity’ text of VHDL)
Required to indicate object of check.
- (2) PT shell for PrimeTime
Required in order to set test mode (set_case_analysis) and to set the clock (create_clock).
Please refer to 2.1.
- (3) NetWalker library
This is the cell library including black box and PLL functions. **If not specified, then correct results cannot be obtained in circuits containing block box and PLL functions.**
Refer to 2.2 for information on creating a user cell library.
- (4) Verilog-HDL/VHDL
Circuit descriptions and libraries defined in Verilog-HDL or VHDL are required.
- (5) Work directory
Work directory required when DFTcheck is performing tasks.

Explanation of each terminal in MuxScan

Table 2.1 Pin Descriptions in MuxScan

I/O pin for Scan	Description	Operating State			Shared for normal I/O
		Normal	Scan	Capture	
Scan_in	- Entry to data necessary to operate ScanFF as shift register during scan. - If Scan_Chain is more than one, the same number of Scan_in is required.	Unused	Used	Unused	Shared
Scan_out	- Exit of data necessary to operate ScanFF as shift register during scan. - If Scan_Chain is more than one, the same number of Scan_out is required.				
Scan_enable	- Control the switch over between normal path for input to ScanFF and Scan path.	Normal side	Scan side	Normal side	Shared if the IOs are used in test mode.
Test_mode	- Evade the constraints for design during scan and capture operations.	Normal side	Test side		Disabled
Scan_Clock (System_Clock)	- Clock driven FF This pin is used by using System_Clock for normal and scan operations.	Used			Shared with system clock (Only IO with one direction)
Normal IO pin	This pin is used during normal operation.	Used	Unused	Used	-

The scanned FF has a value freely set by ATPG during scan. Therefore, design for going to test mode depending on the internal state is not accepted. Test mode must be controlled directly by an external I/O pin.

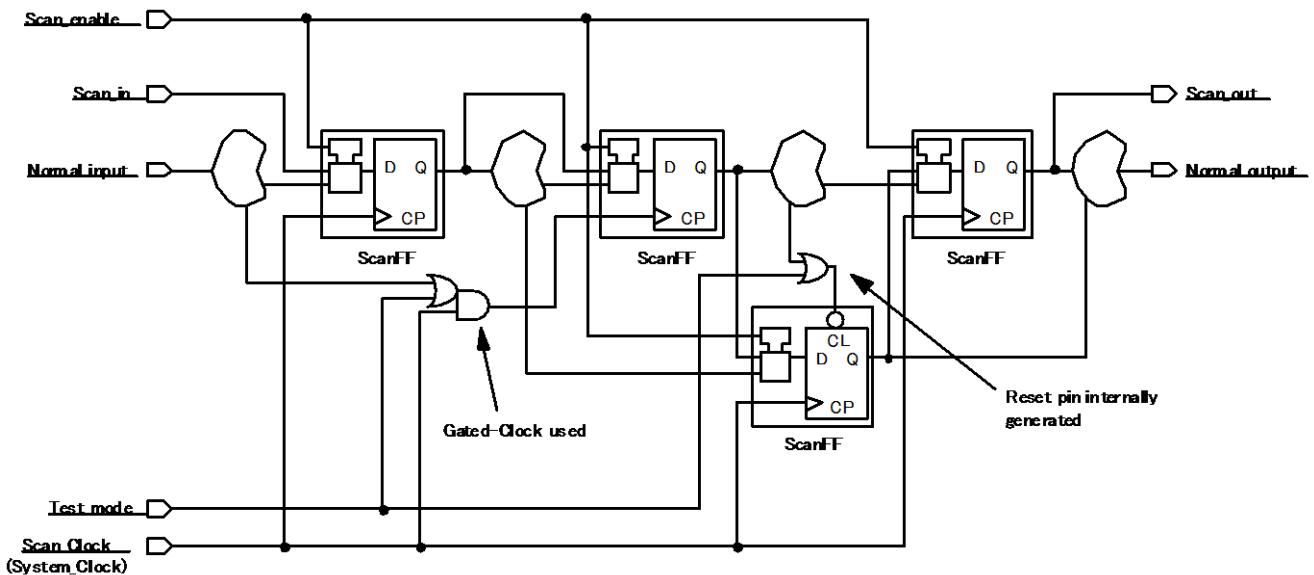
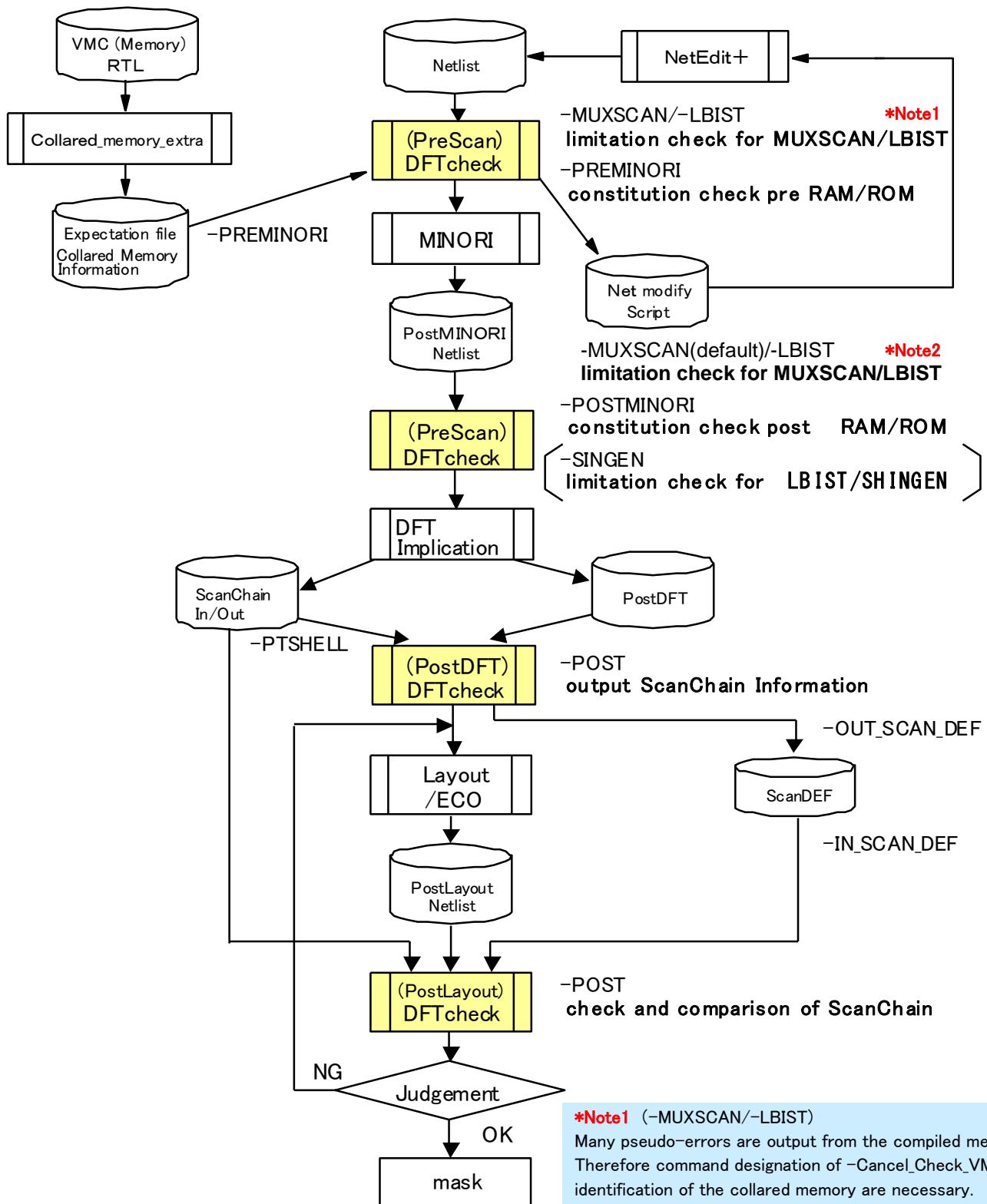


Figure 2.1 Block Diagram in MuxScan

DFTcheck application flow



(Note)

Please specify the clock and logic fixation information in –PTSHELL.

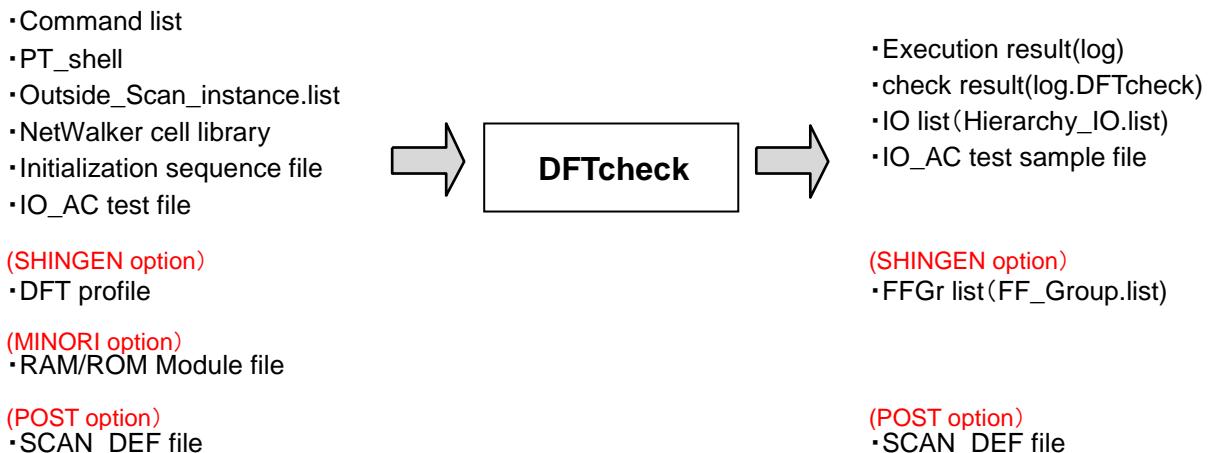
*Note1 (-MUXSCAN/-LBIST)

Many pseudo-errors are output from the compiled memory. Therefore command designation of –Cancel_Check_VMC and identification of the collared memory are necessary. For identification of the collared memory, please specify Collared_type_out.f by –FILE, or specify CollaredMEM variable by –FILE/–PTSHELL. Please refer to a commentary of DFT304-2 for the details.

*Note2 (-MUXSCAN/-LBIST)

Please check the compiled memory(V2.0) after POSTMINORI. Otherwise, the check of the right clock is not possible.

Input/Output Files



<Descriptions>

No.	Name	Contents
1	Command list	: Input command for DFTcheck
2	PT_shell	: Specify the following items in PT-shell format. - Clock start point - Fixed value during test
3	Initialization sequence file	: Specify the initialization pattern file by –PATTERNM.
4	Nega edge signal file	: Specify the Nega edge clock of the initialization sequence file by –PATTERNMN.
5	Outside_Scan_instance.list	: Specify the instance of the outside for Scan.
6	NWCELL Library	: Cell library in NWCELL format And specify a black box module such as divider in.
7	DFT profile (SINGEN option)	: Specify to check the input/output peripheral devices.
8	RAM/ROM module file (MINORI option)	: Specify the RAM/ROM module name for MINORI check.
9	SCAN_DEF input file (POST option)	: Specify pre Layout Scan DEF.
10	log	: Store a execution result of DFTcheck.
11	log.DFTcheck	: Store a check result of DFTcheck.
12	Hierarchy_IO.list	: List for IO port and connection cell instance
13	FF_Group.list (SINGEN option)	: FF list each clocked domain
14	SCAN_DEF output file (POST option)	: Scan DEF for the input netlist
15	IN_IOAC_FILE	: Input file for IOAC test check
16	OUT_IOAC_FILE	: Candidate output file for IOAC test check

2.1 PT shell

PT shells which can specify with DFTcheck are as follows:

create_clock for creating a clock, set_case_analysis for analyzing cases, tcl command, and condition setting commands.

(1) Creating a clock (create_clock)

Only one create_clock shell appears on the clock line, and principally defines top-level clock input to be used and the input/output port. The clock source name is the same as the clock name.

If not specified, then the correct results cannot be obtained.

```
create_clock -period period_value [-name clock_name] [-waveform edge_list] [port_pin_list]
    -period period_value : Specify clock period in library time units.
    -name clock_name : Specify clock name.
    -waveform edge_list : Specify rising and falling edges of clock waveform in one period.
        In DFTcheck, only two edges are usable.
    port_pin_list : Specify clock source port or pin.
```

Example)

```
create_clock -period 8 -name VCLK -waveform { 2 5 } top/CLKGEN/CLK
```

Note) The case which specifies a same clock name with create_clock

There is the tool that the last specification of example1 becomes effective. But example1 is the same as example2 in DFTcheck.

Example1) several line

```
create_clock -name SET_RESET rst1
create_clock -name SET_RESET rst2
```

Example2) list

```
create_clock -name SET_RESET {rst1 rst2}
```

(2) Analyzing cases (set_case_analysis)

"set_case_analysis" fixes the signal to "1" or "0" and propagates the signal value as much as possible, for the following purposes:

If not specified, then correct results cannot be obtained.

- (i) Selecting test mode/normal mode.
- (ii) Specifying set/reset supplied from external source. This setting is used to check that a correct shift operation is performed for the set/reset operations in each FF.
- (iii) Canceling gate loop by being fixed the signal to a value.
- (iv) Changing to through status by being set the latch to ON.

```
set_case_analysis [1 | 0 | rising | falling] object_list
    1 : Fix the signal to 1.
    0 : Fix the signal to 0.
    rising/falling : Not usable with DFTcheck.
    object_list : Specify either pin or port.
```

(3) Input terminal condition (set_input_delay)

Defines the clock for input terminal.

```
set_input_delay delay_value -clock clock_name object_list
    delay_value : Specify delay value.
        (Because DFTcheck does not use this, specify the suitable number)
    -clock clock_name : Specify clock name.
    object_list : Specify input port name. get_ports and all_inputs are usable.
```

Example)

```
set_input_delay 4.4 -clock CLK1 { IN1 IN2 }
set_input_delay 4.4 -clock CLK1 { [ get_ports INX* ] }
set_input_delay 1.2 -clock CLK2 [ all_inputs ]
```

Example 1) Selecting test mode / normal mode

```
create_clock -period 8 -name CLK -waveform { 2 5 } System_clock
set_case_analysis 1 { "test_mode" }
```

The fixed value is propagated as illustrated Figure 2.2 . At the same time, the function also changes.

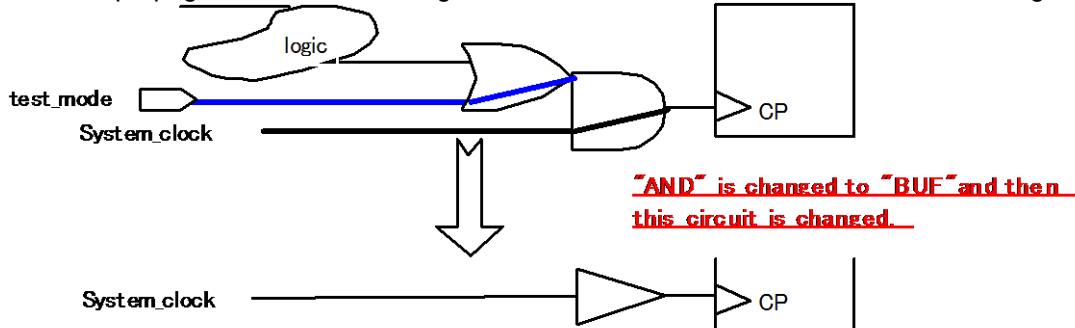


Figure 2.2 Example 1

There are two methods for controlling the set/reset pins directly from external devices. One method involves handling them in the same way as clocks or assigns them a fixed signal that will not set or reset the device during test. Example 2 shows that the set/reset pins are handled the same way as clocks in test mode. The *clock_name* to be specified is fixed to "SET_RES" in order to discriminate against ordinary clocks. Set it to "SET_RES~" for low active.

Example 3 describes a method to fix the signal by using "set_case_analysis".

Example 2) Being reset pin handled the same way as clock in test mode

```
create_clock -period 8 -name CLK -waveform { 2 5 } System_clock
create_clock -name "SET_RES" -waveform {0 50} -period 100 clr_b
create_clock -name "SET_RES~" -waveform {0 50} -period 100 clr_a
```

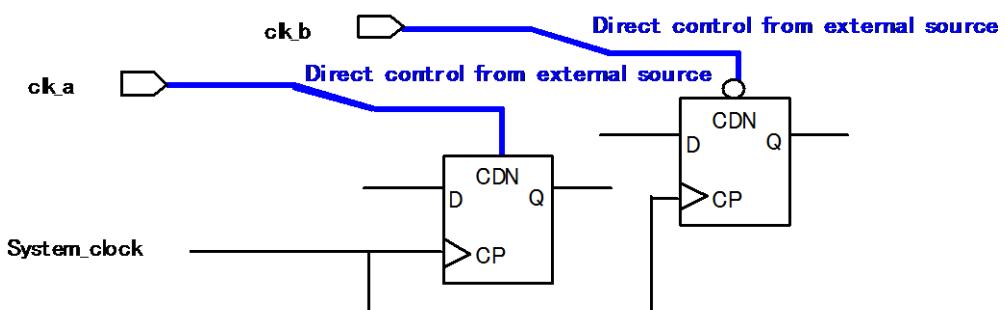


Figure 2.3 Example 2

For FFs with asynchronous set/reset pins, either pin cannot be handled the same way as clocks. Assign either or both of pins a fixed signal that will not set or reset the device during test.

Example 3) Assigning fixed signal not to set or reset during test

```
create_clock -period 8 -name CLK -waveform { 2 5 } System_clock
set_case_analysis 1 { "test_mode" }
```

By making this setting, it is checked that the set/reset pin of each FF can be controlled directly.

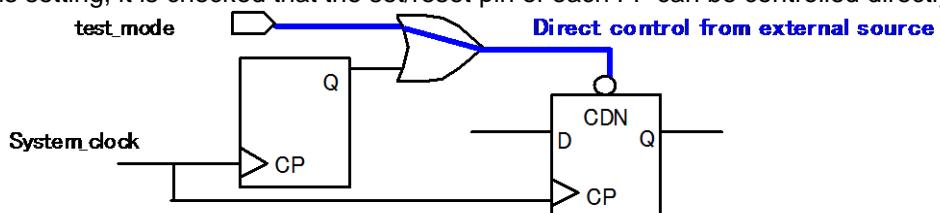


Figure 2.4 Example 3

Example 4) Canceling gate loop by test mode pin

The gate loop can be canceled by specifying the pin for a circuit not to be occurred a gate loop during test.

```
set_case_analysis 1 { "test_mode" }
```

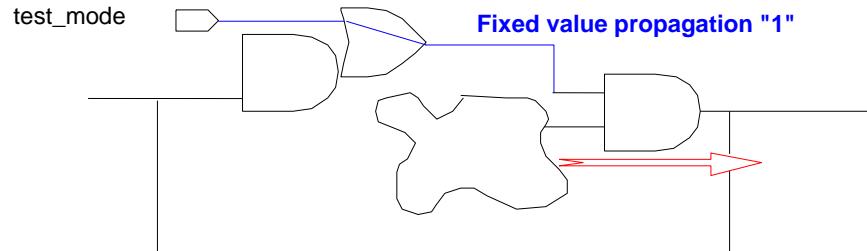


Figure 2.5 Example 4

Example 5) Putting latch through by test mode pin

A circuit can be handled the same way as buffers by being fixed the latch to enable during test.

```
set_case_analysis 1 { "test_mode" }
```

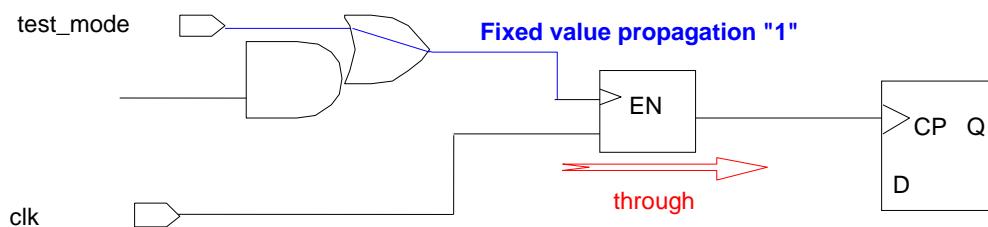


Figure 2.6 Example 5

If the latch is put through by a test mode pin, there is a possibility of causing a gate loop similar to the one shown Figure 2.7 .

The following can be checked by DFT001.

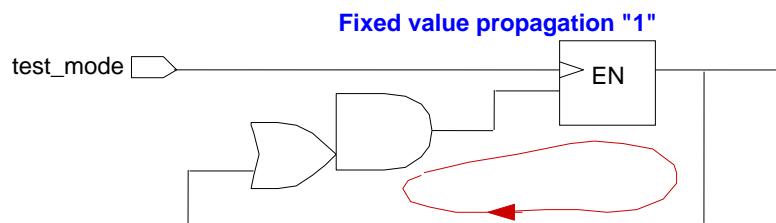


Figure 2.7 Example 6

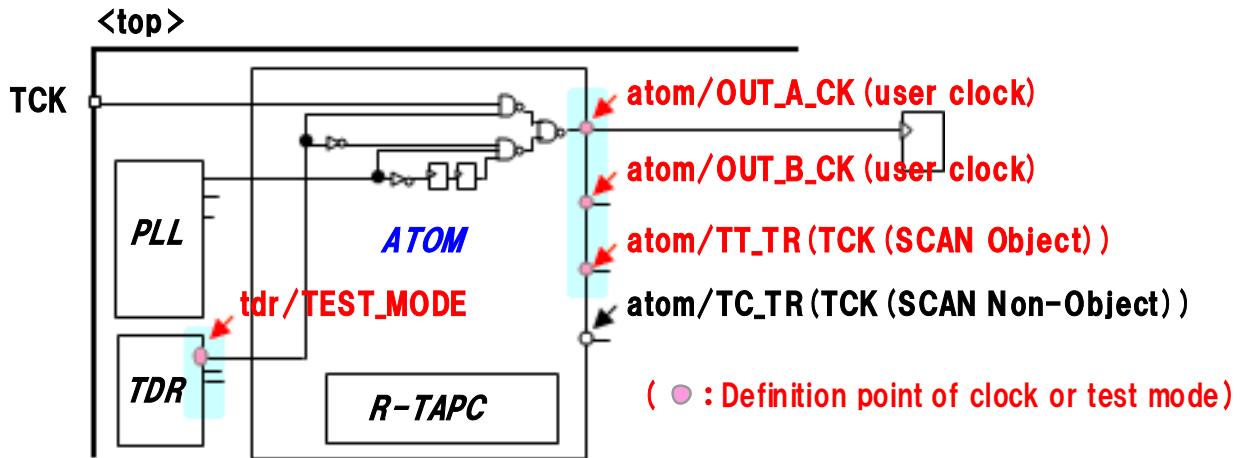
Example 6) Clock control by test clock controller (ATOM)

```

create_clock -period 50 -name A_CK -waveform { 20 45 } atom/OUT_A_CK
create_clock -period 50 -name B_CK -waveform { 20 45 } atom/OUT_B_CK
create_clock -period 50 -name TCK -waveform { 20 45 } atom/TT_TR

set_case_analysis 1 { tdr/TEST_MODE }
set_case_analysis 0 { tdr/MBIST_MODE }
set_case_analysis 1 { tdr/TK_MODE }
set_case_analysis 0 { tdr/TK_ATSPEED }
set_case_analysis 0 { tdr/LBIST_MODE }
set_case_analysis 0 { tdr/mode[0] }
set_case_analysis 0 { tdr/mode[1] }

```



(4) tcl commands

- {} (list) : Usable
- [] (command) : Usable
- Wildcards : Only "*" usable. "?" may be not used.
- ¥ (carriage return) : Usable

(5) set_strings (Condition setting command for DFTcheck)

(5-1) option_dft305_permit_not_direct option

The path disconnection check is executed in NMA connection check (DFT305) if "yes" was specified. Please refer to 5.4.5 for the details.

Example)

```
set_strings option_dft305_permit_not_direct yes
```

(5-2) NMA_TEST option

Specify the input condition of DFT305.

Input condition is "*Mode_name Three start point nets Port define(signal_name and H/L) \$*". "\$" means the end. Please refer to 5.4.5 for the details.

Example)

Mode is A2. The start point nets are penc0, penc1 and penc2. As for the pin define, nma_pin_sel is L, and A is H. In the case of this condition, specify it as follows.

```
set_strings NMA_TEST A2 penc0 penc1 penc2 nma_pin_sel L A H $
```

The start points are 3 nets by default. If those are 6 nets, switch those by the following options.

```
set_strings NMA_6BIT_MODE yes
```

(5-3) DFT013_CANCEL_GCK_INS option

Specify the instance name of GCK cell excludes from check in DFT013. Wildcard specifications are possible. When -hier was specified, all the low rank hierarchies are excluded. Specify the argument by "{}".

Example)

```
set_strings DFT013_CANCEL_GCK_INS INS1/A*;
```

```
set_strings DFT013_CANCEL_GCK_INS {-hier INS1/B*} {INS2/C};
```

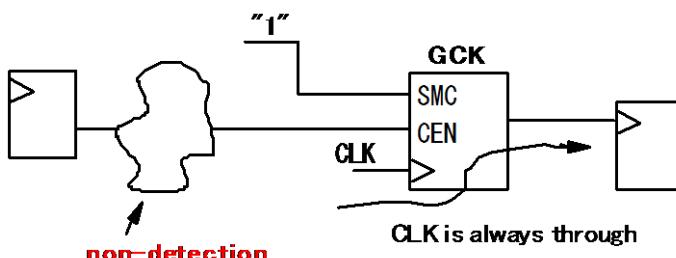
(5-4) DFT013_05_UNDETECT_FAULT_CHECK option

The number of the input terminals causing the fault detection fall is outputted in DFT013-05.

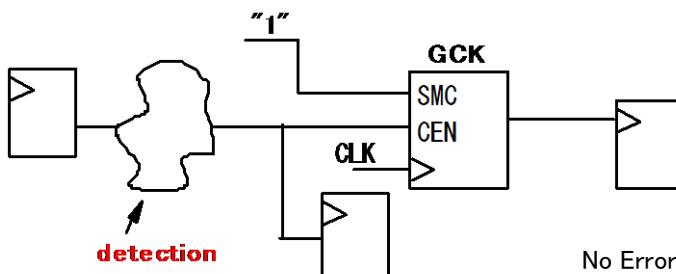
When observation F/F was connected, it is no error.

Example)

```
set_strings DFT013_05_UNDETECT_FAULT_CHECK ;
```



The undetected fault number is estimated.



No Error

(5-5) PATTERN_MONITOR_SIGNAL option

In initialization sequence processing, the logic value after the processing is displayed.

And it is used at the time of expectation check.

Format: `set_strings PATTERN_MONITOR_SIGNAL <signal name> <expectation value>;`

Specify the signal and the expectation value. When expectation is different, it is checked in DFT000-2.
The expectation value is 'H', 'L', '1' or '0' or 'NOCHECK'.

When check is unnecessary, please specify NOCHECK.

Example)

```
set_strings PATTERN_MONITOR_SIGNAL itdr(mbist_mode);
```

(5-6) SCAN_EN option

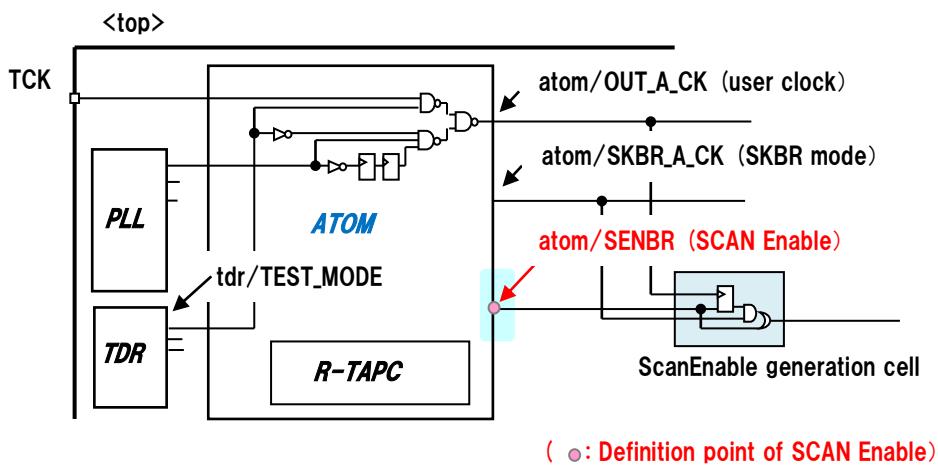
Specify the scan enable signal. Please fix the signal to shift mode (High). The value is 'H', 'L', '1' or '0'.

The specification by the -SCAN_EN option is same.

Format: `set_strings SCAN_EN <scan enable signal name> <value>;`

Example)

```
set_strings SCAN_EN scan_en 1;
```



(5-7) POST_DEF option

Specify the port name or signal name of Scan-in/Scan-out.

Format: `set_strings POST_DFT <Scan-In name> <Scan-Out name>`

`[-PARTITION { <partition name> | NONE }] [-PRT] [-CANCEL_SELECT_DC];`

-PARTITION <partition name>

The partition identifier name of the target scan chain is replaced with the specified name.

The naming rule of <partition name> is <identifier name of partition>_<clock name>.

Default of <identifier name of partition> is "partition".

-PARTITION NONE

PARTITION definition of the target scan chain does not output.

-PRT

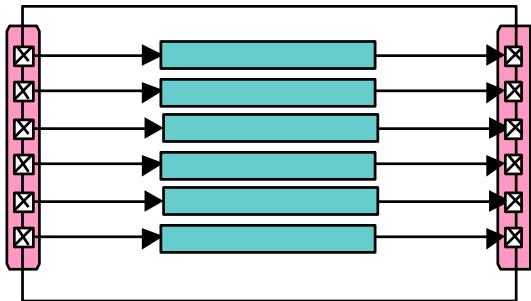
The debug information file of the target scan chain does output.

The file name is "<current directory>/DFT401_debug.f".

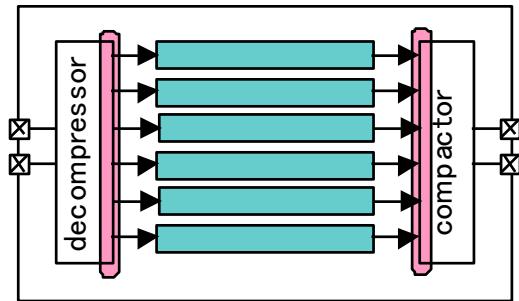
-CANCEL_SELECT_DC

When FF on the scan chain is controlled with the supplied clock from MUX of different SELECT_DC, the chain not to separate is outputted to SCAN_DEF file.

In addition, this scan chain is excluded from DFT401-7.



MuxScan method



Compression scan method

(: Scan-in/Scan-out)

Example 1)

```
set_strings POST_DFT scan_in1 scan_out1 ;
set_strings POST_DFT scan_in2 scan_out2 ;
```

Example 2) replacement of the partition identifier name

```
set_strings POST_DFT scan_in1 scan_out1 -PARTITION partA ;
```

```
<SCANDEF>
- chain_1_1
+ START ud3 SO
+ FLOATING
ud2 ( IN SIN ) ( OUT SO )
+ STOP ud1 SIN
+ PARTITION partA_clk1 MAXBITS 1 ;
```

Example 3) PARTITION definition does not output.

```
set_strings POST_DFT scan_in1 scan_out1 -PARTITION NONE ;
```

```
<SCANDEF>
- chain_1_1
+ START ud3 SO
+ FLOATING
ud2 ( IN SIN ) ( OUT SO )
+ STOP ud1 SIN ;           ←PARTITION is not output.
```

Example 4) The debug information file does output.

```
set_strings POST_DFT scan_in1 scan_out1 -PRT ;
```

```
< DFT401_debug.f >
=====
= Scan_in = scan_in1
= Scan_out = scan_out1
=====
+ 0 ud3.SIN(TH5KDFFAQXC)
+ 0 ud3.Q(TH5KDFFAQXC) net() CLK(clk1)
+ 0 ud3.SO(TH5KDFFAQXC) net(net1) CLK(clk1)
    + 1 ud2.SIN(TH5KDFFAQXC)
    + 1 ud2.Q(TH5KDFFAQXC) net() CLK(clk1)
    + 1 ud2.SO(TH5KDFFAQXC) net(scan_out1) CLK(clk1)
        + 2 ud1.SIN(TH5KDFFAQXC)
```

(5-8) POST_DEF_ORDERED option

Specify the instance to define ORDERED. The instance estimated to be FLOATING is replaced with ORDERED. Wildcard specifications are possible.

Format: `set_strings POST_DFT_ORDERED <instance name>;`

Example)

```
set_strings POST_DFT_ORDERED ud1 ;
```

```
<SCANDEF>
- chain_1_1
+ START ud6 SO
+ FLOATING
ud5 ( IN SIN ) ( OUT SO )
ud2 ( IN SIN ) ( OUT SO )
+ ORDERED
ud1 ( IN SIN ) ( OUT SO )
+ FLOATING
mem1 ( IN SIA ) ( OUT SOA ) ( BITS 7 )
+ STOP mem2 SIA
+ PARTITION partition_clk1 MAXBITS 10 ;
```

(5-9) SCANDEF_PARTITION_NO_PRT option

PARTITION definition of all scan chain does not output.

```
set_strings SCANDEF_PARTITION_NO_PRT "yes" ;
```

```
<SCANDEF>
- chain_1_1
+ START ud3 SO
+ FLOATING
ud2 ( IN SIN ) ( OUT SO )
+ STOP ud1 SIN ;           ←PARTITION is not output.

- chain_2_1
+ START ud7 SO
+ FLOATING
ud6 ( IN SIN ) ( OUT SO )
ud5 ( IN SIN ) ( OUT SO )
+ STOP ud4 SIN ;           ←PARTITION is not output.
```

(5-10) RS_TEST option

Specify the user signal controlling the RS (Resume Standby) terminal of CRAM.

Wildcard specifications are possible.

Format: `set_strings RS_TEST <signal name>;`

Example)

```
set_strings RS_TEST IN1 ;
```

```
set_strings RS_TEST IN2 ;
```

(5-11) DFT013_CANCEL_PORT option

Specify the port which does not cause the unknown in DFT013.

The CEN pin of GCK cell connecting to external port is error in DFT013-2.

When the chip is checked, the pattern for tests is added to the enable signal. However error is detected because the racing happens from timing problem.

When the module is checked, error is detected to consider that the unknown is propagated to the external port. Specify the port to exclude from these error conditions.

Format: `set_strings DFT013_CANCEL_PORT <port name>;`

(5-12) test_coverage option

Specify the block which reports the fault rate of detection in test coverage.

Default is the module in the top hierarchy.

A hierarchy just under specified module instance is reported.

Wildcard specifications are possible, but it is summarized in one.

Format: `set_strings test_coverage <module instance name>;`

(5-13) outside_test_coverage option

Specify the block which does not report the fault rate of detection in test coverage.

Wildcard specifications are possible.

Format: `set_strings outside_test_coverage <module instance name>;`

(5-14) test_coverage_detail option

The detailed information of detected fault is output in test coverage.

File is output to the current directory. File name is "TEST_COVERAGE_DETAIL.f".

Format: `set_strings test_coverage_detail "yes";`

(5-15) NOCLOCK_MUXFF_is_BB option

Specify FF to treat as a hard module because a clock does not arrive in test_coverage.

Format: `set_strings NOCLOCK_MUXFF_is_BB "yes";`

(5-16) DFT307_01_TYPE option

Specify the upper module of the memory cell to check in DFT307_01.

Format: `set_strings DFT307_01_TYPE <module name>;`

Example)

`set_strings DFT307_01_TYPE module_name1 ;`

(5-17) DFT_CONTROL_REG option

Specify the register controlling MuxScan.

That register does not cause the unknown In DFT008 or DFT013 or DFT401.

Specify the instance name of module or register.

Wildcard specifications are possible.

Format: `set_strings DFT_CONTROL_REG <instance name of module or register>;`

Example)

`set_strings DFT_CONTROL_REG {AAA} ;`

`set_strings DFT_CONTROL_REG {BB*} ;`

(5-18) SELECT_DC option

Specify the clock selection signal and the logic value to bypass in DFT017.

DFT017 is checked by specified value. The other checks are checked by the reverse value of specified value.

Format: `set_strings SELECT_DC <signal name> <value> <clock name>;`

Example)

```
set_strings SELECT_DC {tdr/select_dc} 1 TCK ;
```

(5-19) DFT501_MBIST_RS option

Time sharing movement in constant memory bit is necessary to prevent the malfunction caused by Peek electric current flowing at the return from RS(Resume Standby) mode.

The chain list of RS is output.

Example)

```
create_clock -period 8 -name CLKS -waveform { 2 6 } clks ;
set_numerical_value RS_MAX_BIT 150000 ;           ← default is 560K
set_strings DFT501_MBIST_RS MODEREG(mbist_rs) ;   ← start signal of the chain
```

(5-20) DFT501_MBIST_RS_PATH option

Specify the signal names of start and end points pairwise, in DFT501-4.

Format: `set_strings DFT501_MBIST_RS_PATH <start_signal> <end_signal>;`

Example)

```
set_strings DFT501_MBIST_RS_PATH mbist/rs_chain_in mbist/rs_chain_out ;
```

(5-21) CollaredMEM option

Specify the module name of the collared memory for DFT302-1 and DFT304-2.

Example)

```
set_strings CollaredMEM {b*c_cr*} {b*c_cm*} {b*c_co*} {b*c_cn*} {vmc_pipeline_wrapper_*} ;
```

(5-22) UIF_MEM option

Specify UIF (UserIF) module of VMC which exclude check by -CANCEL_CHECK_VMC option.

Example)

```
set_strings UIF_MEM {mem_*} ;
```

(5-23) ALREADY_SCAN_MODULE option

Specify the module name after SCAN. This module is not the unknown outbreak source.

This function is same as -OUTSIDE_SCAN_INS.

Wildcard specifications are possible.

Format: `set_strings ALREADY_SCAN_MODULE <module_name>;`

Example)

```
set_strings ALREADY_SCAN_MODULE {AL*} ;
```

(5-24) CANCEL_DFT017_06 option

Specify the FF which exclude check in DFT017-06.

Wildcard specifications are possible.

Format: `set_strings CANCEL_DFT017_06 <instance name of register>;`

Example)

```
set_strings CANCEL_DFT017_06 {-hier AAA/*} ;
```

(5-25) TPI_EN option

Specify the TPI enable signal. FF which output was cut by TPI enable signal is recognized to be TPI-FF.
TPI-FF is not checked in DFT017-06.

Format: **set_strings TPI_EN <signal name> <value>;**

Example) set_strings TPI_EN tpi_en 1;

(5-26) ADD_SENGEN option

Specify the module instance that SENGGEN circuit is inserted.

SENGEN insertion script for Shingen is created in DFT017. If plural modules were specified, the script is created by the deep module order of the hierarchy.

Format: **set_strings ADD_SENGEN <instance name of module>* ;**

Example)

set_strings ADD_SENGEN {A/B A/B/C A/D} ;

(5-27) SENGGEN_CELL option

Specify the module name of SENGGEN circuit.

When SENGGEN insertion script for Shingen is created in DFT017, it is output as the module name of SENGGEN circuit to script. Default is "SENGEN_EOS".

Format: **set_strings SENGGEN_CELL <cell name> ;**

Example)

set_strings SENGGEN_CELL SENGGEN_EOS ;

(5-28) CHK_DFT013_10 option

DFT013-10 is executed by yes.

Format: **set_strings CHK_DFT013_10 yes ;**

(5-29) DC_TEST_MODE option

DC test in DFT013-10 is executed by yes.

Format: **set_strings CHK_DFT013_10 yes ;**

(5-30) SCANEN_CONNECT option

Specify the instance of register controlled by every scan enable signal in DFT401_5.

Wildcard specifications are possible.

Format: **set_strings SCANEN_CONNECT <instance name1> <instance name2> ;**

instance name1 : Specify instance name of register.

instance name2 : Specify the instance name of F/F cell or the exclusive cell which outputs the scan enable signal.

Example)

set_strings SCANEN_CONNECT ins0/* ins0/scan_en ;

(5-31) Cancel_wrapper option

ScanFF using as Wrapper cell of the module border is excluded from DFT401-5 check.

Format: **set_strings Cancel_wrapper yes ;**

(5-32) OUTSIDE_SCAN_INS option

Specify the block and F/F instance which excludes SCAN. Wildcard specifications are possible.

Format: **set_strings OUTSIDE_SCAN_INS <instance name>** ;

Example)

```
set_strings OUTSIDE_SCA_INS abc/def/* ;
```

(5-33) MASKED_FOR_AC option

Because timing is not guaranteed on AC scan test, specify the instance of register which masks.

The specified register is not checked in DFT013-9 and DFT401-5.

Format: **set_strings MASKED_FOR_AC <instance name of register>** ;

Example)

```
set_strings MASKED_FOR_AC blk1/ff2 ;
```

(5-34) INFO_DFT306_2 option

Specify the user signal which controls RS terminal of CRAM.

Format: **set_strings INFO_DFT306_2 <signal name>** ;

Example)

```
set_strings INFO_DFT306_2 MODEREG(mbist_rs ;
```

(5-35) IOAC_PORT option

Specify the output clock port in DFT019-03.

Format: **set_strings IOAC_PORT <port name>** ;

Example)

```
set_strings IOAC_PORT CKO;
```

(5-36) Cancel_lcsc option

Specify the control signal to pass GCK cell in DFT013-13.

Format: **set_strings Cancel_lcsc <signal name> <value>** ;

Example)

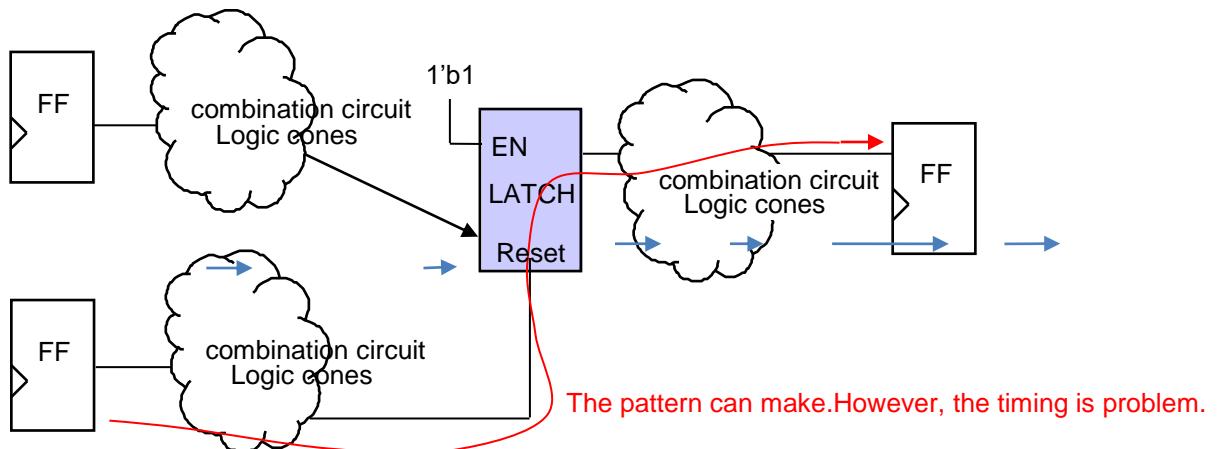
```
set_strings Cancel_lcsc lcsc_stop 1 ;
```

(5-37) Cancel_DFT002_01_async_reset_check option

When the enable of LATCH is active, the test tool (tessent) generates a pattern via data and reset. But, when “timing_enable_preset_clear_arcs false” was specified in timing verification (Prime Time), the path via reset is excluded from an evaluation and causes a problem. In this case, DFTcheck treats LATCH as BlackBox and outputs a message of DFT002 as a default. If the timing does not have a problem, please specify this. Check of set and reset is excluded.

Example)

```
set_strings Cancel_DFT002_01_async_reset_check yes ;
```



(5-38) Unknown_External_Pin option

When you check every IP (FieldBist, etc.), DFT cannot control the external port. If the external port is treated as unknown, please specify this.

Example)

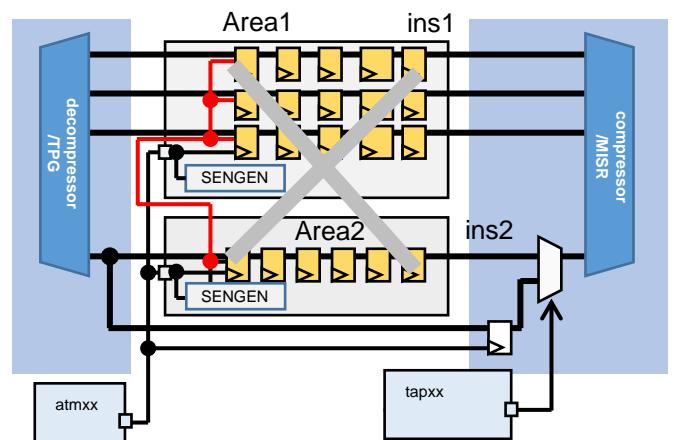
```
set_strings Unknown_External_Pin yes ;
```

(5-39) DFT023_AREA option

Specify area information in DFT023-02. In the case that mass production LBIST is mixed with FieldBist, connection must be closed in each area. When the area of the SENG恩 circuit is different from register (or GCK cell), error is detected by the following designation. When specification is omitted, this is checked as NULL.

Example)

```
set_strings DFT023_AREA ins1/* Area1 ;
set_strings DFT023_AREA ins2/* Area2 ;
```



SENG恩 circuit in Area2 connects with F/F in Area1.

(5-40) DFT021_cancel_cw2mw option

Conversion from Control Wrapper to Mask Wrapper is prohibited in DFT021.

When there is only buffer or inverter between input port and register, it is converted. If the rate of detection decreases by logic fixation of this time, please appoint this.

Format: `set_strings DFT021_cancel_cw2mw yes ;`

(5-41) DFT021_permit_gate option

When Control Wrapper is converted into Masked Wrapper in DFT021, the cell except inverter and buffer is admitted.

Format: `set_strings DFT021_permit_gate yes ;`

(5-42) DFT021_insert option

Wrapper circuit is inserted in DFT021.

Wrapper circuit is inserted for chosen port from CSV file.

Default is for all ports.

Example)

`set_strings DFT021_insert a 2 3 ;`

out1,output,Y,0,s1,,1, out2,output,Y,1,s1,,2, out3,output,Y,1,s1,,3, out4,output,Y,1,s1,,4, out5,output,Y,1,s1,,a, out6,output,Y,1,s1,,b,	Choice of the port to insert 	out2,output,Y,1,s1,,2, out3,output,Y,1,s1,,3, out5,output,Y,1,s1,,a,
--	--	--

(5-43) Wrapper_xx option

Specify the cell to insert as wrapper circuit in DFT021.

Default is the temporary cell.

Format: `set_strings Wrapper_xx [<value> <Key>]*`

<Key>	<Meaning>
@cell	cell name
@th_in	input pin
@th_out	output pin
@en	enable pin
@ff	pin to connect to F/F of CW
@data	data pin of F/F
@clk	clock pin of F/F
@fix0	pin of 0 fixation
@fix1	pin of 1 fixation

Example)

```
set_strings Wrapper_m0 INR2D1BWP7T40P140UHVT @cell A1 @th_in B1 @en ZN @th_out  
set_strings Wrapper_m1 OR2D0BWP7T40P140UHVT @cell A1 @th_in A2 @en Z @th_out  
set_strings Wrapper_cw2 MUX2D0BWP7T40P140UHVT @cell I0 @th_in S @en Z @th_out I1 @ff  
set_strings Wrapper_eor XOR2D1BWP7T40P140UHVT @cell A1 @th_in A2 @en Z @th_out  
set_strings Wrapper_ob SDFQCK1LPD0BWP7T40P140UHVT @cell D @data CP @clk Q ¥  
@th_out SI @fix0 SE @fix0
```

(5-44) OBSERVE_type option

Specify observation F/F to insert in FFR point in DFT020.

Format: `set_strings OBSERVE_type ¥`

```
<cell name> @cell ¥  
<data pin> @data ¥  
<clock pin> @clk ¥  
<port name> @port ¥  
<clock signal> @clk_net ¥  
<output file name> @out_file
```

Example)

```
set_strings OBSERVE_type ¥  
TH5KDFFAQXCU_fall @cell ¥  
DATA @data ¥  
CLKB @clk ¥  
CLKP @port ¥      ←Specify port name which is made when clock goes through module.  
clk @clk_net ¥  
out.v.gz @out_file
```

(5-45) OUTPUT_VERILOG_FILE option

An output Verilog file name is changed in DFT020 and DFT021.

Default is out.v. In addition, if the last of file name is ".gz", it is compressed.

Format: `set_strings OUTPUT_VERILOG_FILE <file name>`

Example) `set_strings OUTPUT_VERILOG_FILE out.v.gz`

(5-46) PREFIX option

The naming rule of the inserted gate is changed in DFT020 and DFT021.

Format: `set_strings PREFIX <keyword> <Reference name to change>`

Example) `set_strings PREFIX MW1 mask_1 ;`

Masked Wrapper (fixation 1)	:MW1 (default is mask_1)
Masked Wrapper (fixation 0)	:MW0 (default is mask_0)
Control Wrapper	:CW (default is cntl)
Observation F/F	:OBFF (default is ob_ff)

(5-47) DFT401_fanout_SI option

When SI pin is connecting even if data pin of FF or SCAN_FF connects with the divergence net on the SCAN chain, trace is continued. Default is interruption of the trace.

Format: `set_strings DFT401_fanout_SI yes ;`

(6) set_numerical_value (Environmental setting command for DFTcheck)

(6-1) POST_DFT_MAX_BITS

MAXBITS value of all scan chain is replaced with the specified value. But if the scan chain length exceeds the specified value, it is not changed. At the time of omission, BIT number of that chain is output.

Format: **set_numerical_value POST_DFT_MAX_BITS <MAXBITS value>;**

Example)

```
set_numerical_value POST_DFT_MAX_BITS 5 ;
```

```
<SCANDEF>
```

```
- chain_1_1
+ START ud3 SO
+ FLOATING
ud2 ( IN SIN ) ( OUT SO )
+ STOP ud1 SIN
+ PARTITION partition_clk1 MAXBITS 5 ;

- chain_2_1
+ START ud7 SO
+ FLOATING
ud6 ( IN SIN ) ( OUT SO )
ud5 ( IN SIN ) ( OUT SO )
+ STOP ud4 SIN
+ PARTITION partition_clk1 MAXBITS 5 ;
```

(6-2) RS_MAX_BIT

Time sharing movement in constant memory bit is necessary to prevent the malfunction caused by peek electric current flowing at the return from RS (Resume Standby) mode.

The number of the steps beyond specified memory bit is displayed.

Example)

```
set_numerical_value RS_MAX_BIT 150000 ; ← Default is 560K.
```

(6-3) limit_nFFR

An upper limit value of FFR can change.

Example)

```
set_numerical_value limit_nFFR 1000 ; ← Default is 2000
```

(6-4) Minimum_percentage

In FFR check, a parameter value to decide a lower limit value to split can change.

Example)

```
set_numerical_value Minimum_percentage 30 ; ← Default is 50
```

(6-5) DFT021_gate_number

When Control Wrapper is converted into Masked Wrapper in DFT021, the number of steps of the gate is changed. Default is less than 8.

Example)

```
set_numerical_value DFT021_gate_number 10 ; ← default is 8.
```

(7) set_cell_term_property option

(7-1) Scan Chain length

The scan chain length of module is changed.

The value specified by this command is given priority to over the NetWalker library.

Format: **set_cell_term_property <cell name> <input pin name> ScanL <scan chain length>;**

Example)

```
set_cell_term_property BDPA25P202041ZZAZZ SIA ScanL 7 ;
```

```
<SCANDEF>
```

```
- chain_1_1
+ START ud6 SO
+ FLOATING
ud5 ( IN SIN ) ( OUT SO )
mem1 ( IN SIA ) ( OUT SOA ) ( BITS 7 )
+ STOP mem2 SIA
+ PARTITION partition_clk1 MAXBITS 8 ;
```

(8) connect_direct option

This is command to assume that net and instance pin are connected at the time of a check.

This function is command corresponding to the following setting of DFTAdvisor.

```
setup clock gating <gated clock circuit> -port_to_connect <port name> -driver <test terminal>
```

When the gate terminal is floating, it is connected to specified test port. Or it is similar when the logic is fixed. When the terminal connects to other gates, it is not connected. In addition, when there is not the test port on the net, it is generated automatically

**Format: connect_direct -gate <instance name> | -cell <cell name> | -type <type name> ¥
-pin <pin name> -driver <test pin name>**

-gate : Specify instance name of gate. Module can not specify.

-cell : Specify cell name.

-type : Specify type name of NetWalker. The type of GCK cell is "NO_HAZARD".

Example1) Case which connects test port (SEN1) to the test pin (SMC) of the gated clock circuit

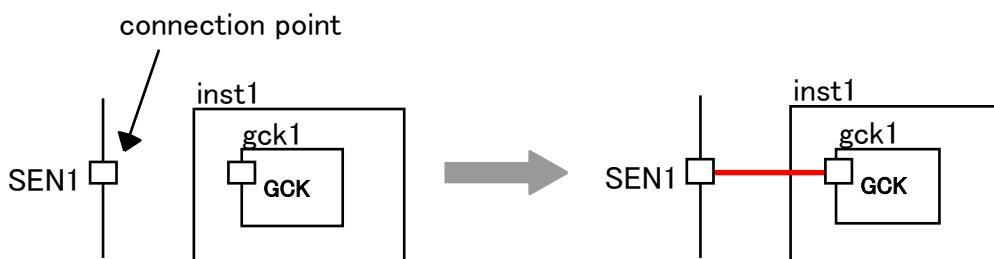
connect_direct -gate {inst1/gck1} -pin SMC -driver SEN1

or

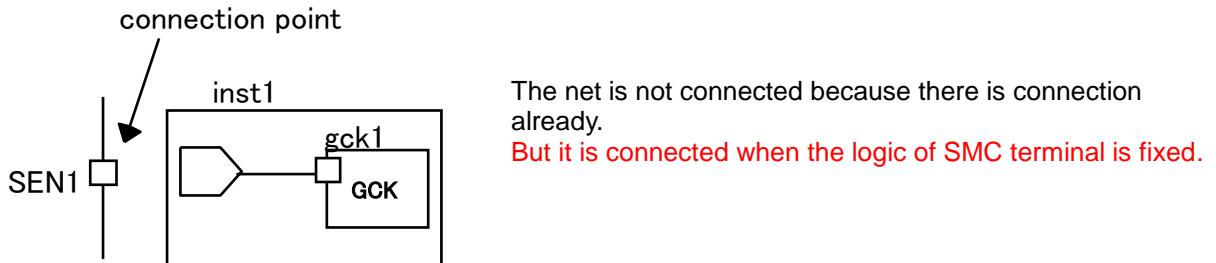
connect_direct -cell {TH5GTDPXH} -pin SMC -driver SEN1

or

connect_direct -type {NO_HAZARD} -pin SMC -driver SEN1



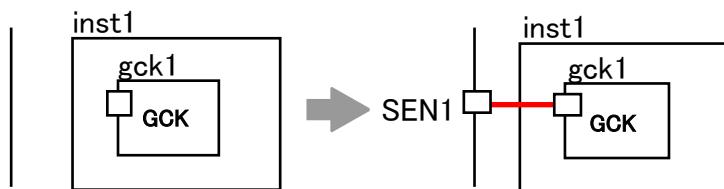
Example2) Case which is not connected



Example3) Case without a test terminal

connect_direct -gate {inst1/gck1} -pin SMC -driver SEN1

If there is not SEN1, the port is generated automatically.



Object_list/port pin list usable with DFTcheck

The following general commands can be used with DFTcheck:

- get_pins : No parameter/-hierarchical
- get_ports : No parameter
- all_inputs : No parameter

Note: Plural wildcards cannot be placed. (ab*cd*)

Handling of the special character

The special character should be escaped with a backslash at the beginning and terminating with a white space. The delimiter is "/".

Example: Please specify the instance name of Verilog-HDL as follows.
 \$abc/aaa .bbb.\$ddd/ccc -> {\${abc/aaa /bbb/\$ddd/ccc}}

When a name including the special character is specified in object_list, even one name has to surround it with curly brace.

Example1: set_false_path -from { \${abc/aaa /bbb/\$ddd/ccc} }

In addition, the description that took off backslash and space as follows is possible. In this case because there is not a blank between, it is not necessary to surround it with curly brace. But interpretation takes time.

Example2: set_false_path -from { abc/aaa/bbb/ddd/ccc }

Note: Wildcard is not placed in the name including the special character. (\$abc/a* /bbb/\$ddd/ccc)

Note: Example2 is effective for only create_clock and set_case_analysis and get_pins.

Wild card

The wild card specified by set_strings etc. cannot express "." of the hierarchy divider by "*".

Example: Specification about {\$b01/aa .ff1}
 "*.ff*" is effectively.
 "*ff*" is invalidit.

2.2 User Cell Library

The method for defining a user cell library is described below. In DFTcheck, there are restrictions relating to **PLL** and **black box**. If using a circuit containing **PLL** or **black box** functions, these should be defined by referring to the following examples. In addition, please define it like the next page when there is the hard module of after Scan.

2.2.1 NWCELL (black box) Format

```
## LIBRARY NAME = XBOX
phased {type=MODULE;
        }
pll {type=MODULE;
      }
## END LIBRARY
// End
```

} (1)

(1)

A black box module, such as divider, is specified by the above description. This means that two modules, "Phased" and "pll", are black boxes. The indeterminate value propagation is checked from the output pin of module specified in this description.

* RAM cell,etc, has already defined for black box by NWCELL library.

2.2.2 NWCELL (PLL) Format

```
PLL hpla8a1 {type=PLL;posi(rfclk->clk0a);
               function(clk0a=tm2?rfclk:clk0a);
}
```

Enable : tm2 and at 'High', clock from rfclk to clk0a is bypassed.

2.2.3 NWCELL (Scan module in POSTDFT)

<Scan path is one.>

```
HD { type=MODULE,REG,DFT;
    pin(CLK=CK;SIA=SI;SOA=SO);
    connect( CLK(direction=input;);

        S (direction=input; related_pin=CLK; type=rise;);

        SI A (direction=input; related_pin=CLK; type=rise; ScanL=5;);

        SOA (direction=output; related_pin=CLK; type=rise;);

        :

        function(shift=S);
```

}

"DFT" is added at the type of module.

The pin attribute of S-In/S-out defines at pin. The attribute name is "SI" or "SO".

The clock of SI/SO pin defines at related_pin.

ScanL of SI is the number of chain steps in that module.

shift at function is the scan mode signal.

The basics are the same as the single port CRAM. (However the type of module is not "DFTMEM".)

If library does not have information, the addition is possible at time of execution. Specify as follows in the PT_SHELL file.

```
set_cell_type      HD  DFT ;
change_cell_term_name HD  SIA SI ;
change_cell_term_name HD  SOA SO ;
set_cell_function   HD  {shift=S} ;
set_cell_term_property HD  SIA ScanL 5 ;
```

< Scan path is multiple.> Example1: S-In or S-out pin is a single bit.

```
HD { type=MODULE,REG,DFT;
    pin(CLK=CK;SIA=SI;SOA=SO;SIB=SI;SOB=SO);
    connect( CLK (direction=input;);

        TCLKA (direction=input;);

        TCLKB (direction=input;);

        TESTS (direction=input;);

        SA (direction=input; related_pin=CLK; type=rise;);

        SB (direction=input; related_pin=CLK; type=rise;);

        SIA (direction=input; related_pin=CLK; type=rise; ScanL=5; ramport=portA;);

        SOA (direction=output; related_pin=CLK; type=rise; ramport=portA;);

        SIB (direction=input; related_pin=CLK; type=rise; ScanL=5; ramport=portB;);

        SOB (direction=output; related_pin=CLK; type=rise; ramport=portB;);

        :

        function(shiftA=SA; shiftB=SB;
                chA=(TESTS?TCLKA:CLK); chB=(TESTS?TCLKB:CLK);)
```

}

The scan chain is recognized by ramport of the SI pin. In the case of SIA, it is "portA". Top "port" is reserved word, and the key to scan chain is "A".

The SMC pin of this scan chain is "SA" acquired by "shift"+key(A)="shiftA".

The clock is acquired by "ch"+key(A)="chA". And user clock "CLK" and test clock "TCLKA" are chosen by test mode signal (TESTS).

< Scan path is multiple.> Example2: S-In or S-out pin is bus bit (1).

```
HDB { type=MODULE,REG,DFT;
    pin (CLK=CK;SIA=SI;SOA=SO);
    connect ( CLK (direction=input;);
        S      (direction=input; related_pin=CLK;type=rise;bit_from=1;bit_to=0;);
        SIA   (direction=input; related_pin=CLK;type=rise;bit_from=1;bit_to=0;
            ScanL[0]=10;ScanL[1]=9;);
        SOA (direction=output;related_pin=CLK;type=rise;bit_from=1;bit_to=0;)) ;
        :
        function(shift=S);
    }
```

The case which is related to the bit information of the bus signal can easily describe it as above.
SIA [0] corresponds to SOA[0] and S[0].

If all ScanL is 10, ScanL=10. But when it is different every bit, please specify as above.

< Scan path is multiple.> Example3: S-In or S-out pin is bus bit (2).

```
HDB { type=MODULE,REG,DFT;
    pin (CLKA=CK;CLKB=CLK;SIA=SI;SOA=SO;SIB=SI;SOB=SO);
    connect ( CLK (direction=input;); CLKA (direction=input;);
        CLKB (direction=input;); SEL (direction=input; ) ;
        SA   (direction=input; related_pin=CLKA;type=rise;bit_from=1;bit_to=0;);
        SIA  (direction=input; related_pin=CLKA;type=rise;bit_from=1;bit_to=0;
            ScanL[0]=8;ScanL[1]=7;ramport=portA;);
        SIO  (direction=output;related_pin=CLKA;type=rise;bit_from=1;bit_to=0;ramport=portA;);
        SB   (direction=input; related_pin=CLKB;type=rise;bit_from=1;bit_to=0;);
        SIB  (direction=input; related_pin=CLKB;type=rise;bit_from=1;bit_to=0;
            ScanL[0]=10;ScanL[1]=9;ramport=portB;);
        SOB (direction=output;related_pin=CLKB;type=rise;bit_from=1;bit_to=0;ramport=portB;)) ;
        :
        function(shiftA=SA;shiftB=SB;chA=(SEL?CLK:CLKA);chB=(SEL?CLK:CLKB););
    }
```

The scan chain is comprised of the combinations of SA,SIA,SIO and SB,SIB,SOB.

The bit information of the bus signal is related. SIA [0] corresponds to SOA[0] and S[0].

When S-In pins are more than two, the linkage with S-Out pins are necessary by ramport.

2.2.4 NWCELL (NetWalker Library) Format

(1) Regular expression of user cell library format

```

<cell definition> ::= < <cell name> <process> >+
<process> ::= [<process 1>?<process 2>?<process 3>?<process 4>?<process 5>?<process 6>?]
<process 1> ::= type = <type name> <, <type name>>* ;
<process 2> ::= pin (<pin name> = <pin name replaced> ; >+ ) ;
<process 3> ::= posi (< <pin name> -> <pin name> ; >+ ) ;
<process 4> ::= nega (< <pin name> -> <pin name> ; >+ ) ;
<process 5> ::= none (< <pin name> -> <pin name> ; >+ ) ;
<process 6> ::= connect (<pin name> (<process 1>? < <property title> = <property value> ; >+ ) : >+

```

(2) Meaning of user cell library keywords

Process	Keyword	Meaning	Use examples
1	type	Type name	type=REG, FF;
2	pin	Change of pin name	pin(cp=CK);
3	posi	Positive	posi (cdn->q);
4	nega	Negative	nega(sdn->q);
5	none	Unknown	none(cp-.qn);
6	connect	Internal connection information	connect (I1(type=LATCH;));
7	function	Function	function(z=a1&a2);

(3) Example of User cell library definition

Normal gate	an02d1 {type=GATE,AND;posi(a1->z; a2->z;); function(z=a1&a2;);}	(1),(2)
Complex gate	aoi211d0 {type=GATE,COMP,2;nega(b->zn;c->zn;a1->zn;a2->zn;); function(zn!=((a1&a2) b c);)}	
MUX	mi21d0 {type=GATE,MUX,1;pin(s=S);nega(i0->zn;i1->zn);none(s->zn;); function(zn!=((i0&!s) (i1&s));)}	(3)
3-state gate	it02d4 {type=3SBUF,fall; pin(i=D;oen=CK);nega(i->zn;);none(oen->zn;); function(zn=oen?Hiz!:i;)}	(4),(5)
IO cell	pc3b02un {type=IO;pin(i=D;oen=CK;pad=D);posi(pad->cin;); function(pad=oen?Hiz:i;cin=pad;);}	
F/F cell	dgctnq0 {type=REG,MUX_FF,FF,RES,EN;pin(cp=CK;en=CK;d=D;cdn=RES);posi(cdn->q;); none(en->q; cp->q;); function(q=\$\$1;clocked_on=en&cp;state=d;clear=!cdn;);}	(6),(7)
PLL	hpla8a1 {type=PLL;posi(rfclk->clkoa); function(clk oa=tm2?rfclk:clk oa);} }	(8)
Black box	black_box {type=MODULE; connect(io0(type=3SBUF,rise;EN=rd_en;)); function(io0=rd_en?io0:Hiz;);}	(9)
ROM/RAM	sp003204 {type=MODULE,REG;}	

- (1) Prepared functions : AND, NAND, OR, NOR, INV, BUF, EOR, ENOR
- (2) Designate that the signal path from pin "a1" to "z" is changed to positive.
- (3) Set selector meaning to pin function : "S".
- (4) Indicate enable active. If none, then rise : fall/rise
- (5) Add meaning to pin function. Enable : "CK" ; data : "D"
- (6) Remove MUX_FF from F/F cells which cannot be used in MuxScan**
- (7) RES : Clock with reset ; SET : Clock with set; EN : Clock with enable
- (8) Enable : tm2 and at 'High', clock from rfclk to clk0a is bypassed.
- (9) "io0" is connected to 3-state gate and operates at rising edge of enable rd_en

2.3 Initialization sequence file

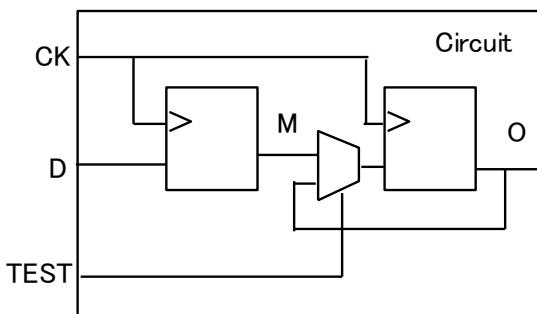
The initialization sequence can confirm correctness.

The state after the initialization of the register in the LSI was specified conventionally by set_case_analay sis of the PT-Shell file. But initialization is possible by execution of the simulation. Please specify the initialization pattern file of Mentor format by -PATTERNM option.

In addition, Mentor format cannot express the clock of Nega edge. In this case please specify the signal which is the clock of Nega edge by -PATTERNMN option.

A register is initialized by an initialization pattern, but the register who is not necessary must be returned to unknown value. On this account the signal input by the initialization pattern is set unknown and simulates it again. Therefore, please fix in PTSHELL file the logic of the register that reset is not necessary.

Example) O signal is 1



	step1	step2	step3
CK	0	0	X
D	1	1	X
TEST	0	1	1
M	1	1	X
O	1	1	1

<< Flow at the time of the initialization sequence specification >>

<step1> The values of CK, TEST, M and O are set by initialization pattern.

```
procedure test_setup = timeplate RUNTEST ;
cycle = force TEST 0 ; force D 1 ; force CK 0 ; end;
cycle = pulse CK ; end;
cycle = pulse CK ; end;
cycle = pulse CK ; end;
end;
:
```

<step2> The logic of a necessary signal is fixed.

PTSHLL file

```
set_case_analysis 1 TEST ;
set_strings PATTERN_MONITOR_SIGNAL M NOCHECK ;
set_strings PATTERN_MONITOR_SIGNAL O 1 ;

```

signal name expectation value
 (NOCHECK: output only for signal value)

<step3> D and CK set by the initialization pattern except signal fixed in PTSHELL are set to unknown value and simulate it again.

<step4> If set_strings was specified as follows, the logic value is output in log file. Please confirm whether it matches expectation. -1 is unknown value.

```
set_strings PATTERN_MONITOR_SIGNAL
```

When expectation was different, please confirm the initialization pattern in simulator.

When a result of the simulation is different from expectation specified by PATTERN_MONITOR_SIGNAL, it is error in DFT000-2.

Log file

```

moniter signals M
moniter signals O
<< Initialization : Simulation time 0 >>
:
<< Initialization : Simulation time 195 >>
[ case net is s1 (1) ]           result and expectation of simulation
PATTERN_MONITOR_SIGNAL is M -1
PATTERN_MONITOR_SIGNAL is O 0 expect(1)
<< set Register for Simulation >>
inst3.Q(TH5DFFQZIXP) [line 1:7] net(O) value(1)           register list which logic was fixed

```

<step5> Expectation sets again, and the later processing is executed.

<< Initialization sequence is not used >>

PTSHELL file
set_case_analysis 1 O ;

<< Example of Mentor format : -PATTERNM >>

```

set time scale 10.0 ns;
set strobe_window time 0;
alias TCK = JTAG_TCK;           ← alias
alias TRST = JTAG_TRST;
alias TMS = JTAG_TMS;
alias TDI = JTAG_TDI;
timeplate RUNTEST =             ← Defines clock etc to use.
    period 10; force_pi 0; measure_po 8; pulse TCK 4 5; pulse CLK 5 5;           The below does not use.
end;                           force_pi <input delay>;
                                measure_po <observation point>

procedure test_setup = timeplate RUNTEST ;
cycle = force TRST 1 ; force TCK 0 ;force TMS 0 ; force TDI 0 ; end;
cycle = force TRST 0 ; force TCK 0 ;force TMS 0 ; force TDI 0 ; end;
cycle = force TRST 1 ; pulse TCK ; force TMS 0 ; force TDI 0 ; end;
cycle = force TRST 1 ; pulse TCK ; force TMS 1 ; force TDI 0 ; end;
cycle = force TRST 1 ; pulse TCK ; force TMS 1 ; force TDI 1 ; end;
apply SUB_REFCLK 3 ; end ;       ← Subroutine is executed 3 times.
end;

procedure sub_procedure SUB_REFCLK =           ← Subroutine
    timeplate RUNTEST ;
    cycle = pulse CLK ;
    end;
end;

```

<< Example of Nega clock specification : -PATTERNMN >>

When signals (JTAG_TCK and CLK) are Nega clock in the above example, specify those as follows.

JTAG_TCK
TCK

2.4 DFT Profile for SINGEN Option

This file is specified with **-SINGEN** command option. IO area is checked.

```
DFT(Environment){  
    Control(BS_Gen){  
        EXTEST : (<port name1>,<port name2>, ...);  
        NOBS : (<port name1>,<port name2>, ...);  
    }  
}
```

- (1) EXTEST : Set port to apply the fixed value in BIST mode.
(2) NOBS : Set pin which is not added BS. (Because I/O test becomes difficult, please do not use it as much as possible.)

2.5 Specify the instance of the outside for SCAN Option

Specify the block and F/F instance of the outside for a scan with **-OUTSIDE_SCAN_INS** command option. Please specify one instance as one line, and enclose in ".

A comment is treated as a comment, when // is in the 1st and 2 columns.

"**" can be used. "**" can be specified as the beginning of an instance name, and the last.

Example) abs.x* a*.bbb abs.*xx abs.*

The example of use

```
// comment1  
"abc.def.*"  
"abc.def.a*"  
"abc./aa[1] .abx"  
// comment2
```

2.6 RAM/ROM module file for MINORI check

Specify RAM/ROM module for MINORI check with **-MINORI** command option.

Please specify one instance as one line. A comment is treated as a comment, when // is in the 1st and 2nd columns.

The example of use

```
// comment1  
BSPA33P204103ZZ0ZZ CLK  
BSPA33P204123ZZ0ZZ CLK  
C16164XU3ZGEUZZ T1  
C16164XU3ZGEUZZ T0  
// comment2
```

2.7 SCAN_DEF input file for POST check

This file is specified for POST command option.

Specify the file by -IN_SCAN_DEF option.

It is checked whether the specified SCAN_DEF file is the same as the construction of the netlist.

Scan Chain : ScanIn → SI-1 / ScanOut → SO-1

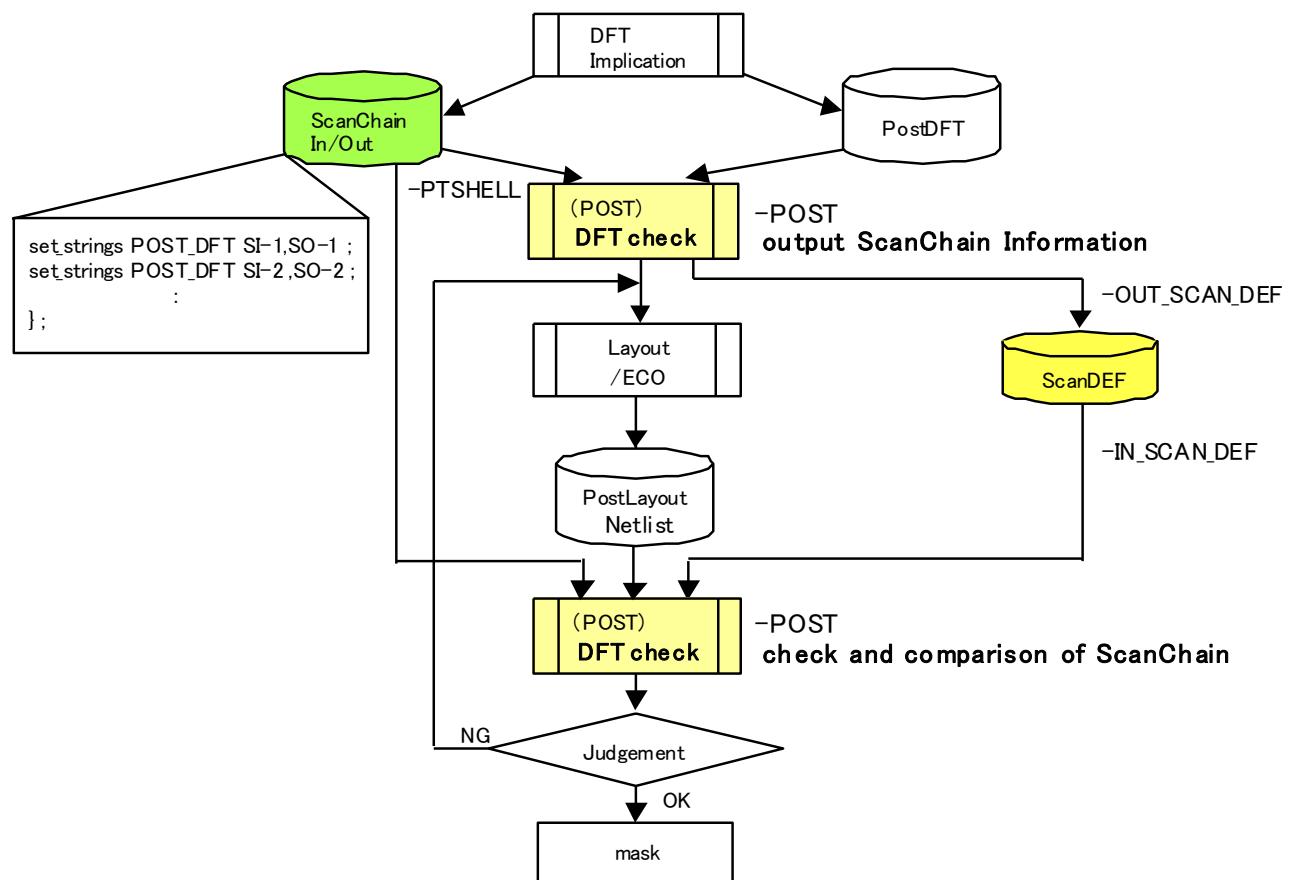
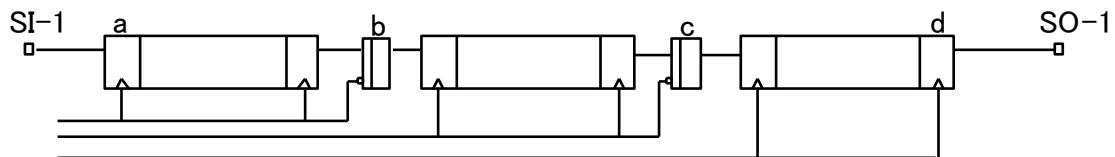


Figure 2.8 Flow of POST mode

3. Executing Procedure

The following command line is entered to execute DFTcheck.

```
DFTcheck
<< basic command >>
-TOP top_module
-WORK work_directory
[ -LANG <VERILOG / VERIRTL / VHDL> ]
[ -VHDL ]
[ -F command file ] *
[ -RENEW ]
[ -ONLYCMP ]
[ -PTSSHLL pt_shell_script ]
[ -NWCELL netwalker_cell ]*
[ -MAXERR number ]
[ -LOG file_name ]
[ -CHECK_RESULT file_name ]
[ -PROCESS process_number ]
verilog / vhdl_command

<< mode select (default: MUXSCAN) >>
[ -MUXSCAN |
-LBIST |
-SINGEN singen_DFT_profile |
-MINORI RAM_ROM_module_file |
-COLLARED_EXTRA |
-PREMINOR |
-POSTMINOR |
-POST
-FIELD ]

[ -SCAN_EN scan enable pin value ]*
[ -CHECK_EXCLUSION_MODULE module_name ] *
[ -CANCEL_WARNING ]
[ -CANCEL_PRIMARY ]
[ -CHECK_001 ]
[ -CHECK_008-1 ][ -CHECK_008-2 ]
[ -CANCEL_008-5 ]
[ -CHECK_010 ]
[ -CANCEL_013-5 ]
[ -CANCEL_013-9 ]
[ -CANCEL_013-12 ]
[ -CANCEL_015 ]
[ -CANCEL_018 ]
[ -CHECK_020 ]
[ -CHECK_303 ]
[ -CHECK_305_2 ]
[ -CANCEL_401-5 ][ -CANCEL_401-6 ]
[ -CHECK_601 ]
[ -CANCEL_CHECK_VMC]
[ -ALREADY_SCAN_INS module_name ]*
[ -OUTSIDE_SCAN_INS file_name ]
[ -DFT010_01_PRT_NUM number ]
[ -TESTCOVERAGE ]
[ -Unknown_External_Pin ]

<< SHINGEN check (-SINGEN) >>
<< POST check (-POST) >>
[ -IN_SCAN_DEF scan_def_file ]
```

```

[ -OUT_SCAN_DEF scan_def_file ]
[ -DFT401_DEBUG_NOSPACE ]
[ -DFT401_OLD_SCANDEF_MODE ]

<< Collared memory logic extraction (-COLLARED_EXTRA) >> Refer to 5.4.3 and 5.4.4.

<< debug >>
[ -DETAILED_008_5 ]
[ -TRACE_FROM signal_name ]
[ -TRACE_TO signal_name ]
[ -TRACE_GATE_INFO gate_instance_name ]*
[ -TRACE_LIMIT limit number ]
[ -TRACE_DETAIL ]
[ -TCL debug_script_file ]
[ -TCLD ]

<< DFTclean cooperation >>
[ -DFTCLEAN dftclean_file ]
[ -DFTCLEAN_DFT008_5 ]

<< output suppression >>
[ -OUTPUT_CONTROL output_control_file ]*
[ -REVIEW_DELETE_FILE review_delete_file ]

<< checkers control file >>
[ -FILE checkers_control_file ]

<< Initialization sequence check >> Refer to 2.3
[ -PATTERNM Mentor_format_file ]
[ -PATTERNMN Nega_edge_clock_file ]
[ -CHECK_EXPECT ]

<< IOAC scan test>> Refer to DFT019
[ -IN_IOAC_FILE check_file ]
[ -OUT_IOAC_FILE template_file ]

```

EX)

```
DFTcheck -WORK ./work -TOP top -NWCELL Lib.nw -PTSHELL ¥
ptshell1.pt lsi.v -f verilog.path
```

Cautions: Limitations

(1) Verilog-HDL and VHDL

Input languages are gate level and RTL of Verilog-HDL and VHDL.

When ROM/RAM etc. is written by description of behavior, it is necessary to treat the block as a black box.

Please inform a system technology development department for details.

When description is RTL, it cannot perform by HP machine.

(2) The compressed file (gzip) of the Verilog description can input. VHDL is non-support.

(3) Once Compile has been executed, DFTcheck does not perform Compile again unless the work directory has been deleted. If a linkage error occurs and Compile is executed again, “-RENEW” should be added to the command line.

(4) VHDL

The file sorted according to the dependence of the file must be input. Otherwise error occurs.

<< basic command >>

-TOP <i>top_module</i>	: Specify a top module block name described module text in Verilog-HDL.
-WORK <i>work_directory</i>	: Specify a work directory for stored file to run DFTcheck. (Default: "work")
-LANG VERILOG/VERIRTL/VHDL	: VERIRTL is specified when a synthesizable RTL description of Verilog is included. In addition, VERIRTL is specified when Verilog/VHDL mixture netlist is input. VHDL is specified when Gate or a synthesizable RTL description of VHDL is included. (Default: VERILOG)
-VHDL <i>vhdl_file</i>	: When there are netlists of both Verilog and VHDL, specify -VHDL in front of VHDL files. Multiple specifications are impossible. Specify several VHDL files in a mass.

<< Example1: VHDL only >> *** -VHDL uselessness ***
DFTcheck -LANG VHDL blk1.vhd blk2.vhd blk3.vhd blk4.vhd

<< Example2: Verilog/VHDL mixture netlist (Top is VHDL) >>
DFTcheck -LANG VERIRTL blk2.v blk3.v -VHDL blk1.vhd blk4.vhd blk5.vhd

<< Example3: Verilog/VHDL mixture netlist (TOP is Verilog) >>
DFTcheck -LANG VERIRTL blk1.v blk2.v blk3.v -VHDL blk4.vhd blk5.vhd

[Note: Verilog/VHDL mixture netlist]

(1) large letter / small letter

distinguishes large letter and small letter, but VHDL assumes it the same name.

■ Top is VHDL, lower hierarchy block is Verilog

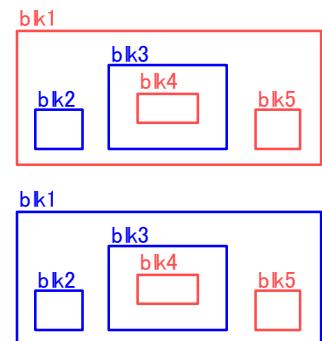
The
large letter and small letter is not distinguished. When different names of large letter and small letter are used in Verilog and VHDL, they become the same name.

■ Top is Verilog, lower hierarchy block is VHDL

The
large letter and small letter is distinguished. When different names of large letter and small letter are used in Verilog and VHDL, they are disagreement.

(2) escape character

Verilog
and VHDL are different in escape character. When escape character is used, please be careful because correspondence is not taken.



[Image of the VERIRTL specification]

```
always @(posedge ck1)
  w1<=d1;
always @(posedge ck2)
  w2<=w1;
always @((w2 or d2)
  o1=w2&d2;
```

synthesis

```
VERIFIC_DFFRS i7 (.d(w2), .clk(ck2), .s(1'b0), .r(1'b0), .q(w2));
VERIFIC_AND i6(o1, d2, w2);
VERIFIC_DFFRS i5 (.d(d1), .clk(ck1), .s(1'b0), .r(1'b0), .q(w1));
```

* RTL is synthesised temporarily. (But it is not optimized.)

The input pin floating by this result may be left. And this is detected as error.

-F <i>command_file</i>	: Specify a command file for DFTcheck. Multiple specifications are possible.
-RENEW	: Specify to compile a file and check it again. If the file has once been compiled without -RENEW specified, only check is executed.
-ONLYCMP	: Specify to check Verilog description and Verilog command.
-PTSHELL <i>pt_shell_script</i>	: Specify a PT shell for PrimeTime. Multiple specifications are possible.
-NWCELL <i>netwalker_cell</i>	: Specify a Netwalker library. Multiple specifications are possible.
Verilog / vhdl_command	: Specify a verilog command. The verilog commands, -f, -v, -y and +libext+, are supported.
-LOG <i>file_name</i>	: Specify a execution result file. (Default: "log")
-CHECK_RESULT <i>file_name</i>	: Specify a check result file. (Default: "log.DFTcheck")
-MAXERR <i>Max_Error_Number</i>	: Specify the number of error output for one error. (Default: 1000) All errors are output by appointing 0.
-PROCESS <i>number 1,2,3</i>	: Specify the numbers of the process (machine), if you execute by multi-processing. (Default is 1. Maximum is 3.) [Note] When the numbers of the process (machine) are not specified by -n option of bs command, execution may dump core because of memory lack.
-Unknown_External_Pin	: External port is treated as the unknown at testing time. (for Field Bist test)

<< mode select command >>

-MUXSCAN	: Checks the item for MuxScan. (Default)
-LBIST	: Add a check item for LogicBist. Refer to Chapter 5.2. This command checks items for MuxScan + LogicBist.
-SINGEN <i>DFT_profile</i>	: Add a check item for SINGEN. This command checks items for MuxScan + LogicBist + SINGEN-specific. ※Specify the scan modules such as DFTRAM in Verilog library (*.vs). Do not specify it in the NetWalker library. (This is because FF information in DFTRAM is necessary for the output of FFGr list.) In addition, specify the scan module by -ALREADY_SCAN_MODULE option.
-MINORI <i>RAM_ROM_module_file</i>	: This command checks items for MINORI-specific. Specify RAM or ROM module to check in the <i>RAM_ROM_module_file</i> . The check item only for MINORI is checked.
-POST	: This command checks ScanChain and compares ScanChain of pre and post Layout.
-PREMINORI	: This command checks that it is MINORI lady state before MINORI is executed.
-POSTMINORI	: This command checks the net of PostMINORI is right.
-COLLARED_EXTRA	: To compare the logic of the collared memory before and after the logic composition, the copybook file which extracted the logic of collared memory beforehand is made. Refer to Chapter 5.4
-FIELD	: Checks Wrapper insertion sheet. Please refer to 5.2.20 for the details.

<< checkers control file command >>

-FILE <i>checkers_control_file</i>	: Specify the collared memory of DFT304. Wildcard specifications are possible. string CollaredMEM[] = { "collar*", "COLLAR*" } ;
------------------------------------	---

<< output suppression command >>

-OUTPUT_CONTROL <i>output_control_file</i>	: Specify the file used to prevent the re-output of check-result messages.
-REVIEW_DELETE_FILE <i>review_delete_file</i>	: Specify a file to which the messages deleted by the check-result output control file are output.

<< exclusion / specify command >>

-CHECK_EXCLUSION_MODULE	: Specify a module name not to be checked at MUXSCAN or LBIST mode. (Module for M-BIST, etc)
-SCAN_EN <i>scan enable pin value</i>	: Specify an enable pin/terminal during scan. This is used for output of DesignCompiler script. Scan mode is assumed for "High" and normal mode for "Low". A value is "H" "L" "1" "0". Fix this to become ("High") in shift mode.
-CANCEL_WARNING	: Specify to cancel check for warning message.
-CANCEL_PRIMARY	: Specify this if unknown does not propagate from external port in DFT013 check.
-CHECK_001	: Specify to check of DFT001 at POST mode. (DFT001 is default check at other mode.)
-CHECK_008_1	: Specify to check of DFT008-1.
-CHECK_008_2	: Specify to check of DFT008-2.
-CANCEL_008_5	: Specify to cancel check of DFT008-5.
-DETAIL_008_5	: Specify to report the check details of DFT008-5.
-CHECK010	: Specify to check of DFT010.
-CANCEL_013_5	: Specify to cancel check of DFT013-5.
-CANCEL_013_9	: Specify to cancel check of DFT013-9. [Pre scan net] : Specify this before inserting ScanEnable generation circuit. [Post scan net] : When AC-SCAN is executed only by Broadside method, specify this.
-CHECK_013_12	: Specify to check of DFT013-12.
-CANCEL_015	: Specify to cancel check of DFT015.
-CANCEL_018	: Specify to cancel check of DFT018.
-CHECK_020	: Specify to check of DFT020.
-CANCEL_021_VERILOG	: Specify this if the net that Wrapper was inserted is unnecessary at DFT021.
-CHECK303	: Specify to check of DFT303.
-CHECK305_2	: Specify to check of DFT305-2. RAM without the NMA pin is reported.(INFO_DFT305_2.f)
-CANCEL_401_5	: Specify to cancel check of DFT0401-5.
-CANCEL_401_6	: Specify to cancel check of DFT0401-6.
-CHECK601	: Specify to check of DFT601.

-CANCEL_CHECK_VMC
 : In the MUXSCAN or LBIST mode before MINORI, many pseudo errors are output from VMC(CRAM_). Specify to exclude this message of VMC.
 In addition, the specifications about GCK cell of VMC were changed. Because GCK cell is put in the outside (UIF module) of VMC hierarchy, pseudo errors are output. Specify to exclude this.

<Specified method of VMC>
 File (Collared_type_out.f) which Collared_memory_extra command generated for DFT304-3

(1) Description of -FILE file as follows:

(1-1) Collared_memory

```
string CollaredMEM[] = { "b*c_cr*", "b*c_cm*", "b*c_co*", "b*c_cn*", "vmc_pipeline_wrapper_*",
  "e*c_cr*", "e*c_cm*", "e*c_co*", "e*c_cn*",
  "w*c_cr*", "w*c_cm*", "w*c_co*", "w*c_cn*",
  "o*c_cr*", "o*c_cm*", "o*c_co*", "o*c_cn*",
  "amcip*c_cr*", "amcip*c_cm*", "amcip*c_co*", "amcip*c_cn*"};
```

(1-2) UIF module

```
string UIF_MEM[] = { "mem_*" };
```

(2) Description of -PTSHELL file as follows:

(2-1) Collared_memory

```
set_strings CollaredMEM {b*c_cm*} {b*c_co*} {b*c_cn*} {vmc_pipeline_wrapper_*};
set_strings CollaredMEM {e*c_cm*} {e*c_co*} {e*c_cn*} ;
set_strings CollaredMEM {w*c_cm*} {w*c_co*} {w*c_cn*} ;
set_strings CollaredMEM {o*c_cm*} {o*c_co*} {o*c_cn*} ;
set_strings CollaredMEM {amcip*c_cr*} {amcip*c_cm*} {amcip*c_co*} {amcip*c_cn*};
```

(2-2) UIF module

```
set_string UIF_MEM { "mem_*" };
```

Please refer to DFT304-2 for the details.

This module is considered to be the scan module. However, the clock of this is not checked in DFT003.

-ALREADY_SCAN_MODULE
module

: Specify the module which already SCAN.
 This module is not an unknown outbreak source.
 This is used in clock check of DFT003.

-OUTSIDE_SCAN_INS *file*

: Specify the instance of the outside SCAN.

-DFT010_01_PRT_NUM *value*

: Specify the number of non-detection pin. (Default: 1)

<<TestCoverage estimate command>>

-TESTCOVERAGE

Specify to estimate the test coverage in MUXSCAN mode.

<< DFTclean command >>

-DFTCLEAN *dftclean_file*

: The errors of DFTcheck are correctable in DFTclean automatically. Necessary information for DFTclean is output.

-DFTCLEAN_DFT008_5

: The script of NetEdit which inserts F/F in the signal which observation F/F is not connected to is output. Output file name is "DFTCLEAN_DFT008_5.tcl".
 Refer to Chapter 5.2.8.

<< POST check >>

-IN_SCAN_DEF *scan_def_file*

: Specify a SCAN_DEF file to compare the scan chain at POST mode.
 (Default: Scan chain is not compared.)

-OUT_SCAN_DEF *scan_def_file*

: SCAN_DEF file is output at POST mode. (Default: File is not output.)
 If there is the error of DFT401-0, DFT401-1 or DFT401-2, the file is not made correctly.

-DFT401_DEBUG_NOSPACE

: The debugging file is output without the indent. (File name is "DFT401_debug.f".)

-DFT401_OLD_SCANDEF_MODE : The format of SCANDEF file in POST mode is changed. START/END points become the instance pin names of the first FF/end FF on the scan chain.
 (Default: START/END points become the signal names specified by POST_DFT command.)

<< initialization sequence processing >>

-PATTERNM	:Specify the input pattern of the initialization sequence.
<i>Motor_format_initialization_file</i>	
-PATTERNMN	: Specify clock of the inversion edge. Refer to Chapter 2.3.
<i>Nega_edge_clock_file</i>	
-CHECK_EXPECT	: Set expectation value is transmitted. (Default: Expectation value is set, but it is not transmitted.)

<< debug command >>

Note: In cases where -TRACE_FROM/-TRACE_TO/-TRACE_GATE_INFO were specified, check is not executed. The propagation of clock and fixed value is executed. Refer to Chapter 0 for the details.

-DETAI_008_5	: Specify to get the number of cells more than two input that were not detected.
-TRACE_FROM	: Specify a search start signal.
-TRACE_TO	: Specify a search end signal.
-TRACE_GATE_INFO	: Specify a gate instance.
gate_instance	
-TRACE_LIMIT	: In cases where -TRACE_FROM or -TRACE_TO was specified, specify a search limit number. (Default: 30)
limit_number	
-TRACE_DETAIL	: If you want to get detail informations, specify it.
-TCL tcl_script_file	: Specify the tcl debug script file.
-TCLD	: If you want to debug Interactively, specify it.

<< verilog command >>

-f
 (command argument file option)

Verilog-HDL commands define circuit descriptions

Syntax: -f <file name>

This option directs DFTcheck to execute with the command options written in a text file. This file may contain a source text file name and other DFTcheck command options that include -f option. Though the nesting levels in this option are conceptually infinite, 1024 characters are assumed as a maximum to trap the recursive -f option.

Example: DFTcheck -f vfile.list

< vfile.list >
netlist.v
-v lib.v

-v
 (library file option)

Syntax: -v <file name>

To incorporate library files, the command line option -v should be specified with the library file name.

Example: DFTcheck netlist.v -v lib.v

Syntax: -y <directory name>

This command option specifies a library directory. The option takes a directory name as the argument as shown below.

Example: DFTcheck netlist.v -y / files1/home/DFTcheck/lib

Syntax: +libext+<extension 1>+<extension 2>+...<extension N>

The file name extensions for the library directory are specified by using the plus command option. To specify file name extensions for the library directory, enter +libext+ on the command line immediately followed by the characters of extensions.

Example: DFTcheck netlist.v -y / files1/home/DFTcheck/lib +libext+.v+

<< verilog command relation >> for VERIRTL

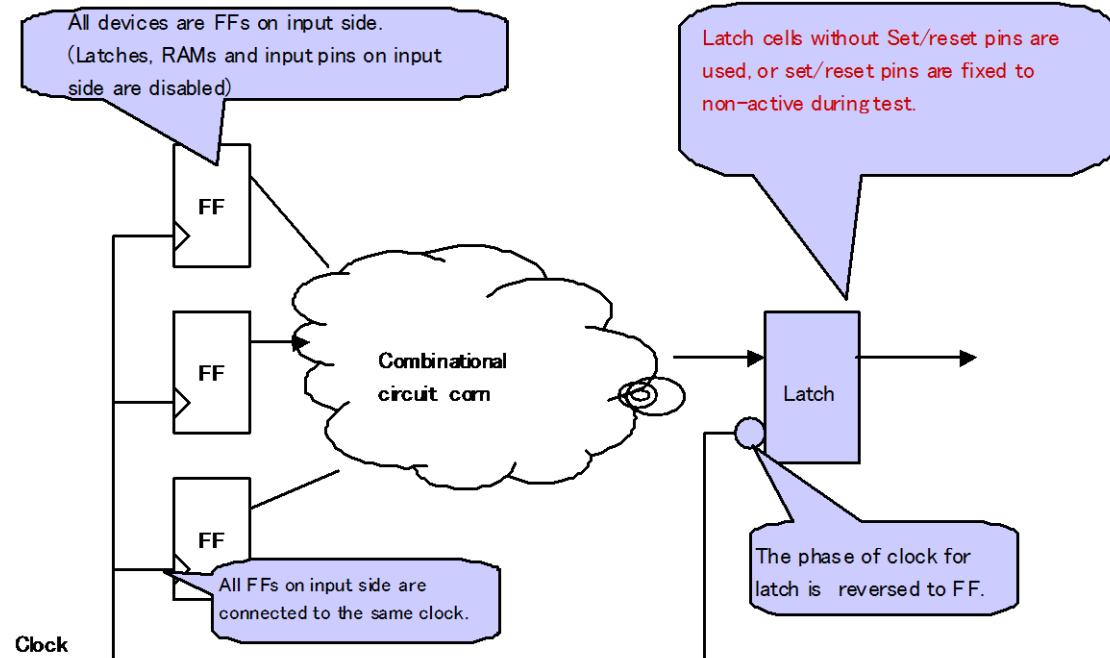
-y and -v become handled as library. This is default. Please use the following command for the change.

-NET -y and -v specified after this option are treated as net.

-LIB -y and -v specified after this option are treated as library.

3.1 Through Latch (Retiming Latch)

The latches that meet the following conditions considered to be through during test are assumed to be the through latch. The latches that are not assumed to be the through latch are handled as black boxes, whose output is considered to be an indeterminate value when checked.



OR

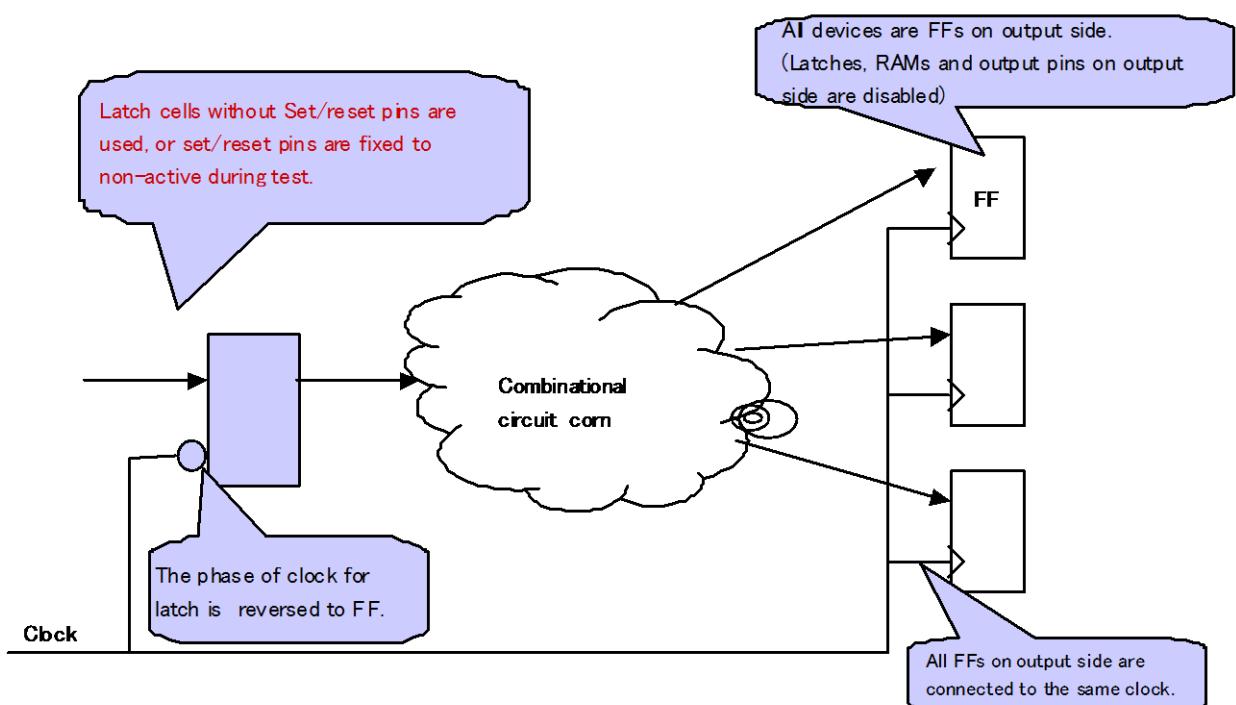
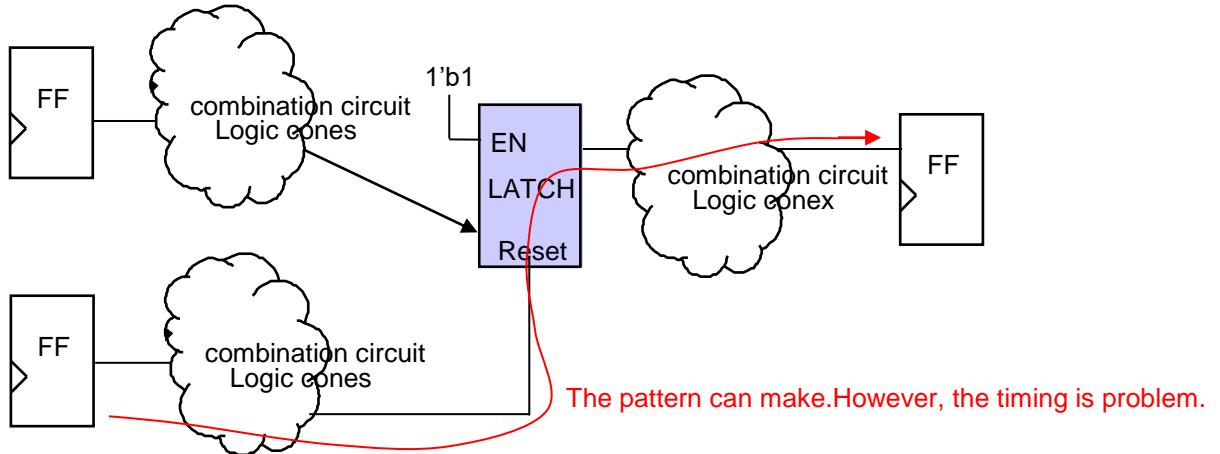


Figure 3.1 Conditions of Through Latch

Set and Reset pin of the through latch

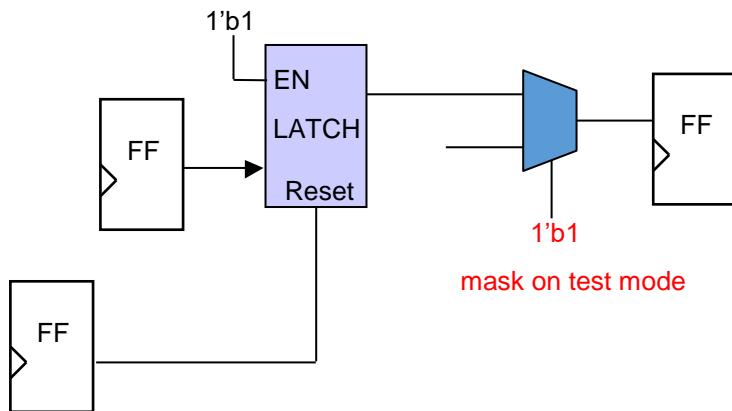
When the enable of LATCH is active, the test tool (tessent) generates a pattern via data and reset. But, when “timing_enable_preset_clear_arcs false” was specified in timing verification (Prime Time), the path via reset is excluded from an evaluation and causes a problem. Therefore, set and reset pin must be set non-active as basics. In this case, DFTcheck treats LATCH as BlackBox and outputs a message of DFT002 as a default.

If the timing does not have a problem, please specify the following. Check of set and reset is excluded.
set_strings Cancel_DFT002_01_asyc_reset yes ;

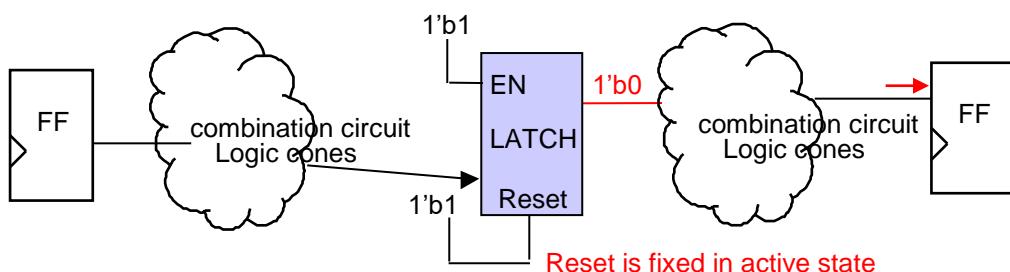


The case such as the following does not have any problem.

- LATCH is treated as BlackBox.
 - Test mode signal does not propagate to FF.
 - As there is not the combination circuit, rate of detection has little influence.
- Please check this in conjunction with DFT008 checking influence of BlackBox.



When set and reset is fixed in active as follows, rate of detection of the combination circuit reduces. Therefore, this is error in DFT002.



3.2 Execution method

(1) This is the execution command example of MuxScan limitation check.

EX)

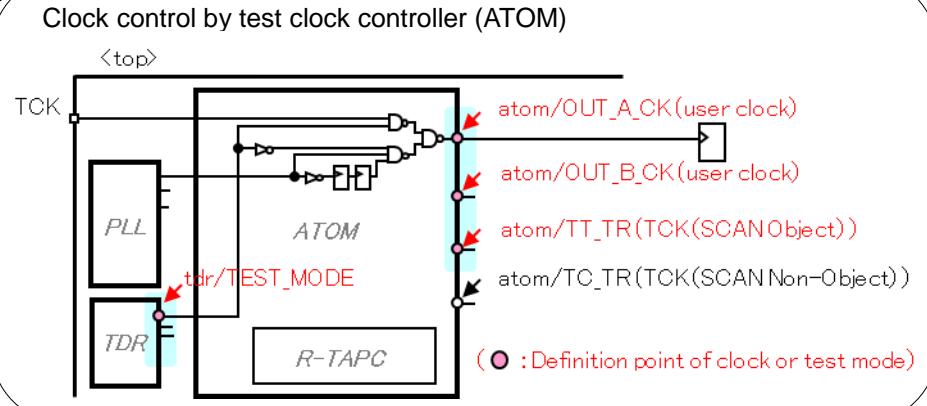
```
DFTcheck
-WORK work          ... Specify a directory for stored file to run DFTcheck.
-TOP top            ... Specify an uppermost block name.
-LANG VERILOG       ... Specify the object language. (Default : VERILOG)
-MUXSCAN           ... Specify the object rule. (Default : MUXSCAN)
-NWCELL lib.nw      ... Specify a NetWalker library.
-PTSHELL LSI.pt    ... Specify the clock or set_case_analysis or DFTcheck environment
                      command.
-TESTCOVERAGE      ... This option executes the estimate of the trouble rate of detection.
LSI.v               ... Specifies the name of the Verilog-HDL/VHDL netlist.
SUB.v
```

[<LSI.pt>](#)

```
create_clock -period 50 -name A_CK -waveform { 20 45 } atom/OUT_A_CK
create_clock -period 50 -name B_CK -waveform { 20 45 } atom/OUT_B_CK
create_clock -period 50 -name TCK -waveform { 20 45 } atom/TT_TR

set_case_analysis 1 { tdr/TEST_MODE }
set_case_analysis 0 { tdr/MBIST_MODE }
set_case_analysis 1 { tdr/TK_MODE }
set_case_analysis 0 { tdr/TK_ATSPEED }
set_case_analysis 0 { tdr/LBIST }
```

```
set_strings OUTSIDE_SCAN_IN
set_strings OUTSIDE_SCAN_IN
```



Specify the initialization state of the register in the LSI by set_case_analysis. By the initialization sequence file of the Mentor company format, the initial value can define.

Specify the block (test clock controller, test decoder, scan enable generation circuit, etc.) and F/F instance which excludes SCAN by OUTSIDE_SCAN_INS.

(2) This is the execution command example of MINORI limitation check for the netlist which MBIST circuit is not added to.

EX)

```
DFTcheck
-WORK work          ... Specify a directory for stored file to run DFTcheck.
-TOP top            ... Specify an uppermost block name.
-LANG VERILOG       ... Specify the object language. (Default : VERILOG)
-PREMINORI          ... This option executes MINORI limitation check.
                      The target netlist does not include MBIST circuit.
-NWCELL lib.nw      ... Specify a NetWalker library.
-PTSHELL LSI.pt    ... Specify the clock or set_case_analysis or DFTcheck environment
                      command.
-FILE Collared_type_out.f ... Specify the module name of collared memory.
LSI.v               ... Specifies the name of the Verilog-HDL/VHDL netlist.
SUB.v
```

<LSI.pt>

```
create_clock -period 50 -name A_CK -waveform { 20 45 } atom/OUT_A_CK
create_clock -period 50 -name B_CK -waveform { 20 45 } atom/OUT_B_CK
create_clock -period 50 -name TCK -waveform { 20 45 } atom/TT_TR

set_case_analysis 1 { tdr/TEST_MODE }
set_case_analysis 1 { tdr/MBIST_MODE } ← MBIST_MODE is ON.
set_case_analysis 1 { tdr/TK_MODE }
set_case_analysis 0 { tdr/TK_ATSPEED }
set_case_analysis 0 { tdr/LBIST_MODE }

set_strings OUTSIDE_SCAN_INS { atom };
set_strings OUTSIDE_SCAN_INS { tdr };
```

<Collared_type_out.f>

```
string CollaredMEM[] = {"b*c_cr*", "b*c_cm*", "vmc_pipeline_wrapper_*"};
```

(3) This is the execution command example of MINORI limitation check for the netlist which MBIST circuit was added to.

EX)

```
DFTcheck
-WORK work          ... Specify a directory for stored file to run DFTcheck.
-TOP top            ... Specify an uppermost block name.
-LANG VERILOG       ... Specify the object language. (Default : VERILOG)
-POSTMINORI        ... This option executes MINORI limitation check.
                     The target netlist includes MBIST circuit.
-NWCELL lib.nw      ... Specify a NetWalker library.
-PTSHELL LSI.pt    ... Specify the clock or set_case_analysis or DFTcheck environment
                     command.
-FILE Collared_type_out.f ... Specify the module name of collared memory.
LSI.v               ... Specifies the name of the Verilog-HDL/VHDL netlist.
SUB.v
```

<LSI.pt>

```
create_clock -period 50 -name A_CK -waveform { 20 45 } atom/OUT_A_CK
create_clock -period 50 -name B_CK -waveform { 20 45 } atom/OUT_B_CK
create_clock -period 50 -name TCK -waveform { 20 45 } atom/TT_TR

set_case_analysis 1 { tdr/TEST_MODE }
set_case_analysis 1 { tdr/MBIST_MODE } ← MBIST_MODE is ON.
set_case_analysis 1 { tdr/TK_MODE }
set_case_analysis 0 { tdr/TK_ATSPEED }
set_case_analysis 0 { tdr/LBIST_MODE }

set_strings OUTSIDE_SCAN_INS { atom };
set_strings OUTSIDE_SCAN_INS { tdr };
```

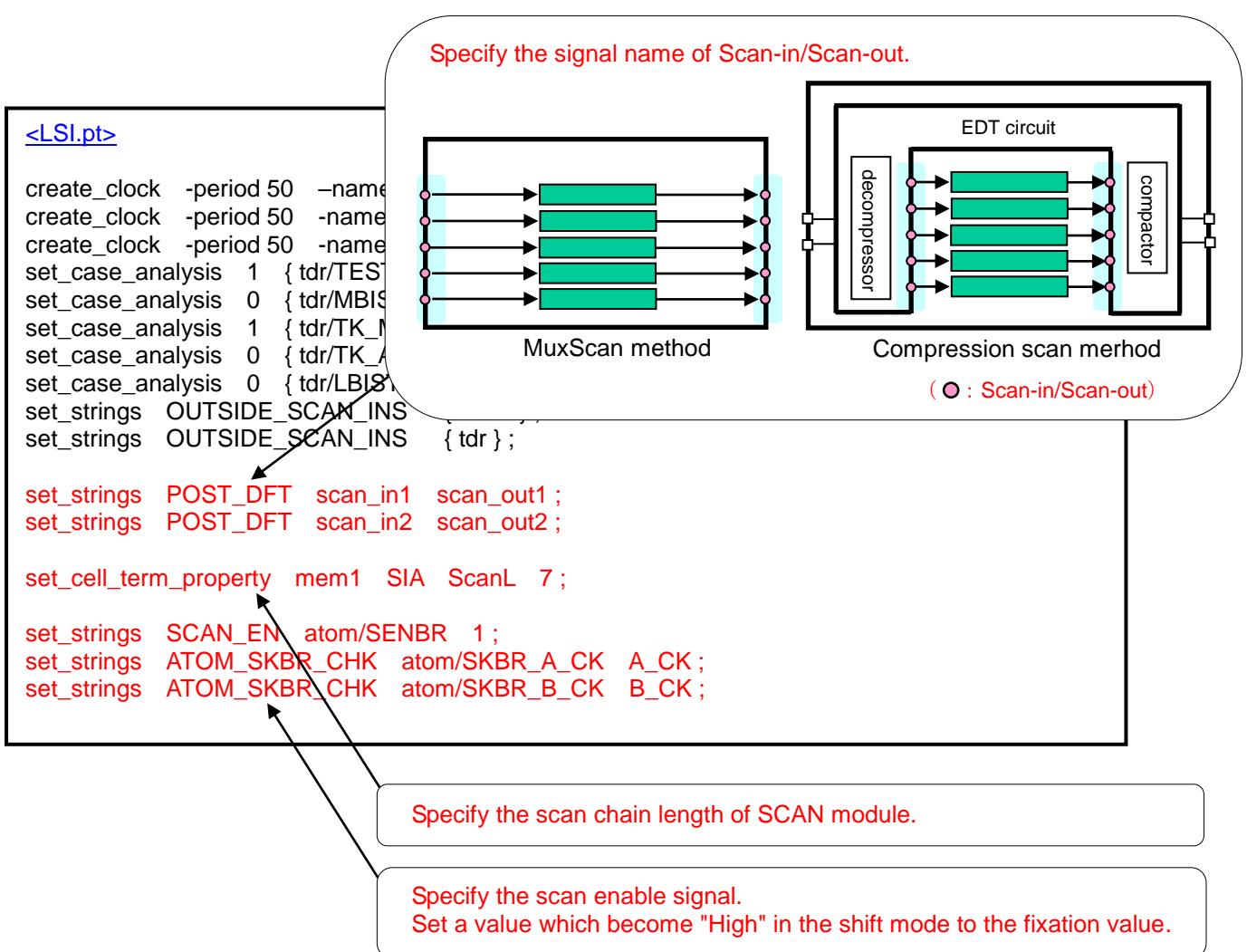
<Collared_type_out.f>

```
string CollaredMEM[] = {"b*c_cr*", "b*c_cm*", "vmc_pipeline_wrapper_*"};
```

(4) This is the execution command example of SCAN chain check after SCAN.

EX)

```
DFTcheck
  -WORK work           ... Specify a directory for stored file to run DFTcheck.
  -TOP top             ... Specify an uppermost block name.
  -LANG VERILOG        ... Specify the object language. (Default : VERILOG)
  -POST                ... This option executes SCAN chain check.
                        The target is netlist after SCAN.
  -NWCELL lib.nw       ... Specify a NetWalker library.
  -PTSHELL LSI.pt     ... Specify the clock or set_case_analysis or DFTcheck environment
                        command.
  -OUT_SCAN_DEF top.scandef ... This option creates SCANDEF file.
  LSI.v                ... Specifies the name of the Verilog-HDL/VHDL netlist.
  SUB.v
```



(5) This is the execution command example of SCAN chain check after LAYOUT/ECO.

EX)

```
DFTcheck
  -WORK work           ... Specify a directory for stored file to run DFTcheck.
  -TOP top             ... Specify an uppermost block name.
  -LANG VERILOG        ... Specify the object language. (Default : VERILOG)
  -POST                ... This option executes SCAN chain check.
                        The target is netlist after LAYOUT/ECO.
  -NWCELL lib.nw       ... Specify a NetWalker library.
  -PTSSHELL LSI.pt    ... Specify the clock or set_case_analysis or DFTcheck environment
                        command.
  -IN_SCAN_DEF top.scandef ... Specify SCANDEF file of the pre-LAYOUT/ECO. [option]
                            When you compare the scan chain before and after layout /ECO,
                            this specification is necessary.
  LSI.v                ... Specifies the name of the Verilog-HDL/VHDL netlist.
  SUB.v
```

<LSI.pt>

```
create_clock -period 50 -name A_CK -waveform { 20 45 } atom/OUT_A_CK
create_clock -period 50 -name B_CK -waveform { 20 45 } atom/OUT_B_CK
create_clock -period 50 -name TCK -waveform { 20 45 } atom/TT_TR
set_case_analysis 1 { tdr/TEST_MODE }
set_case_analysis 0 { tdr/MBIST_MODE }
set_case_analysis 1 { tdr/TK_MODE }
set_case_analysis 0 { tdr/TK_ATSPEED }
set_case_analysis 0 { tdr/LBIST_MODE }
set_strings OUTSIDE_SCAN_INS { atom };
set_strings OUTSIDE_SCAN_INS { tdr };

set_strings POST_DFT scan_in1 scan_out1;
set_strings POST_DFT scan_in2 scan_out2;

set_cell_term_property mem1 SIA ScanL 7;

set_strings SCAN_EN atom/SENBR 1;
set_strings ATOM_SKBR_CHK atom/SKBR_A_CK A_CK;
set_strings ATOM_SKBR_CHK atom/SKBR_B_CK B_CK;
```

(6) This is the execution command example of LBIST limitation check.

EX)

```
DFTcheck
  -WORK work           ... Specify a directory for stored file to run DFTcheck.
  -TOP top             ... Specify an uppermost block name.
  -LANG VERILOG        ... Specify the object language. (Default : VERILOG)
  -LBIST               ... This option executes LBIST limitation check.
  -NWCELL lib.nw       ... Specify a NetWalker library.
  -PTSHELL LSI.pt     ... Specify the clock or set_case_analysis or DFTcheck environment
                        command.
  LSI.v                ... Specifies the name of the Verilog-HDL/VHDL netlist.
  SUB.v
```

<LSI.pt>

```
create_clock -period 50 -name A_CK -waveform { 20 45 } atom/OUT_A_CK
create_clock -period 50 -name B_CK -waveform { 20 45 } atom/OUT_B_CK
create_clock -period 50 -name TCK -waveform { 20 45 } atom/TT_TR

set_case_analysis 1 { tdr/TEST_MODE }
set_case_analysis 0 { tdr/MBIST_MODE }
set_case_analysis 1 { tdr/TK_MODE }
set_case_analysis 0 { tdr/TK_ATSPEED }
set_case_analysis 1 { tdr/LBIST_MODE } ← LBIST_MODE is ON.

set_strings OUTSIDE_SCAN_INS { atom };
set_strings OUTSIDE_SCAN_INS { tdr };
```

(7) This is the execution command example of SINGEN limitation check.

EX)

```
DFTcheck
-WORK work          ... Specify a directory for stored file to run DFTcheck.
-TOP top            ... Specify an uppermost block name.
-LANG VERILOG       ... Specify the object language. (Default : VERILOG)
-SINGEN singen.txt ... This option executes SINGEN limitation check.
-NWCELL lib.nw      ... Specify a NetWalker library.
-PTSHELL LSI.pt    ... Specify the clock or set_case_analysis or DFTcheck environment
                      command.
LSI.v               ... Specifies the name of the Verilog-HDL/VHDL netlist.
```

SUB.v
DFTRAM.vs

Specify the SCAN module (DFTRAM, etc.) in VerilogHDL library (.vs).
In addition, specify the SCAN module by ALREADY_SCAN_MODULE.
(SINGEN limitation check outputs FF_Group.list for SINGEN. FF_Group.list need
the FF instance information of the SCAN module.
When the information defined in NetWalker library was input, it cannot get.
Therefore, the scan module inputs information defined in VerilogHDL library.
The information defined in NetWalker library does not input.
When both NetWalker library and VerilogHDL libraries were input, the information
from NetWalker library is given priority.)

<LSI.pt>

```
create_clock -period 50 -name A_CK -waveform { 20 45 } atom/OUT_A_CK
create_clock -period 50 -name B_CK -waveform { 20 45 } atom/OUT_B_CK
create_clock -period 50 -name TCK -waveform { 20 45 } atom/TT_TR

set_case_analysis 1 { tdr/TEST_MODE }
set_case_analysis 0 { tdr/MBIST_MODE }
set_case_analysis 1 { tdr/TK_MODE }
set_case_analysis 0 { tdr/TK_ATSPEED }
set_case_analysis 1 { tdr/LBIST_MODE } ← LBIST_MODE is ON.

set_strings OUTSIDE_SCAN_INS { atom };
set_strings OUTSIDE_SCAN_INS { tdr };

set_strings ALREADY_SCAN_MODULE { DFTRAM };
```

4. Interpreting Execution Results

4.1 Compile Results

```
Product VerilogHDL Compiler/vcomp. Version V00.02.01 5-Jul-1999 13:40:16
Copyright (C) 1998 Hitachi, Ltd. All Rights Reserved.
<< Compile File = /sv1/takaha-gr/m2100a/DEMO/demo.v >>
<< Compile File = /sv1/takaha-gr/m2100a/DEMO/udps.v >>
<< Compile Path = /sv1/takaha-gr/m2100a/DEMO/hcos893 >>

Error Information      Warning   Count : 0
                      Error     Count : 0
                      Fatal    Count : 0
                      Sever   Count : 0
memory size   :      8187kbyte
```

Display Verilog HDL net to be compiled

Compile error summary list

Memory size used for Compile

Verilog-HDL compile

4.2 Check Results

4.2.1 Execution Results (log)

```

Logic design rule check / NetWalker(V05.01.05) Mon Mar 27 23:27:37 2000
***** Summary of Linker *****
Total number of Logic Element list 176
    Used Model Count 13
        1 an02d1      32   2 an04d1      2
        3 aon22d1     16   4 dfctnq1     4
        5 dfctnqn1    16   6 dfntnq1    16
LINK cpu time:
    total cpu : 0.09s
    user cpu : 0.03s
    system cpu : 0.06s
    memory size : 888kbyte

*** input command ***
logcheck /sv1/takaha-gr/m2100a/svrf2/tools/NetWalker/DFT/rule/all.rule
[ case net is rst ]
<< DFTcheck start >>
<< DFTcheck end >>

*** Summary of Error Code *** 23:27:37
No. Error_Code:message Number          WARNING      ERROR
-----
1 "DFT000 :Undefined NetWalker Cell Library      "      0      0
2 "DFT001 :Feed Back Loop                      "      0      0
3 "DFT002 :Can Not Use Cell                   "      0      0
4 "DFT003 :Clock is controlable                "      0      37
5 "DFT004 :Set/Reset is controlable            "      0      0
6 "DFT007 :Bus Only One Drive                 "      0      0
7 "DFT008 :Black Box Check                    "      0      0
8 "DFT009 :Clock Pair/PLL Clock Check       "      0      0
9 "DFT010 :Undetect Fault                     "      0      0

*** End of Summary ***
*** input command ***
*** stop ***
CHECK cpu time:
    total cpu : 0.17s
    user cpu : 0.17s
    system cpu : 0.00s
    memory size : 1118kbyte

```

List of cells used

CPU time / max. memory used until linkage

set_case_analysis implemented

Program error summary list

CPU time / max. memory used for executing rule check

4.2.2 Check Results (log.DFTcheck)

ERROR DFT003 -1: Clock is Gated .

No.	Clock	Cell Name	Instance Name
1	clk_a	blk05.inv_clk_a_OK	(in01d1)[line 1:108]
2	clk_b	blk05.inv_clk_b_NG	(in01d1) [line 1:109]
		:	
		:	

Source name is displayed

Check Results

INFO DFT999 -1: Total Undetect Fault Count is 0

```
*****
***** Verilog SOURCE LIST *****
*****
```

No.	SOURCE NAME
1	LSI.v
2	SUB.v

[line file_umber:line_number]
The conversion table of a file number and a file name

*** Summary of Error Code *** 23:27:37

No.	Error_Cod:message Number	WARNING	ERROR
1	"DFT000 :Undefined NetWalker Cell Library "	0	0
2	"DFT001 :Feed Back Loop "	0	0
3	"DFT002 :Can Not Use Cell "	0	0
4	"DFT003 :Clock is controlable "	0	37
5	"DFT004 :Set/Reset is controlable "	0	0
6	"DFT007 :Bus Only One Drive "	0	0
7	"DFT008 :Black Box Check "	0	0
8	"DFT009 :Clock Pair/PLL Clock Check "	0	0
9	"DFT010 :Undetect Fault "	0	0

Program error summary list

*** End of Summary ***

4.2.3 Hierarchy_IO.list

Relationship file between ports and names of IO cells nonexistent in the top layer

The inside pin of IO cell must be specified as the information that needs to be specified in DFTadvisor. This file shows the relationship between the LSI ports of IO cells nonexistent in the top layer and the pin/cell names of the IO cells.

b3_b	blk01/b004/oen pt3b01c
b2_b	blk01/b003/cin pt3b01c
b2_b	blk01/b003/i pt3b01c
b2_b	blk01/b003/oen pt3b01c
b1_b	blk01/b002/cin pt3b01c
b1_b	blk01/b002/i pt3b01c
b1_b	blk01/b002/oen pt3b01c
b0_b	blk01/b001/cin pt3b01c
b0_b	blk01/b001/i pt3b01c
b0_b	blk01/b001/oen pt3b01c
obus_b	blk01/o008/i pc3o01c
obus_a	blk01/o007/i pc3o01c
cout_b	blk01/o006/i pc3o01c
o3_a	blk01/o005/i pc3o01c
o2_a	blk01/o004/i pc3o01c
o1_a	blk01/o003/i pc3o01c
o0_a	blk01/o002/i pc3o01c
cout_a	blk01/o001/i pc3o01c
te	blk01/i017/cin pc3d01
s1	blk01/i016/cin pc3d01
s0	blk01/i015/cin pc3d01
clr_b	blk01/i014/cin pc3d01
trns_b	blk01/i013/cin pc3d01
load_b	blk01/i012/cin pc3d01

4.2.4 FFGr list (FF_Group.list)

This file is output for specifying the option “-SINGEN”. This is FF list each clocked domain and output under the current directory.

```
Control(FF_Group){  
    CLOCK_ID : T0 ;  
    FF_LIST : h_enclsib.g_videob.v_videob.vx.v_moniout_reg_3_ ;  
    FF_LIST : h_enclsib.g_videob.v_videob.vx.v_moniout_reg_7_ ;  
    FF_LIST : h_enclsib.g_videob.v_videob.vx.v_moniout_reg_5_ ;  
    FF_LIST : h_enclsib.g_videob.v_videob.vx.v_moniout_reg_8_ ;  
    FF_LIST : h_enclsib.g_videob.v_videob.vx.v_moniout_reg_1_ ;  
    :  
}
```

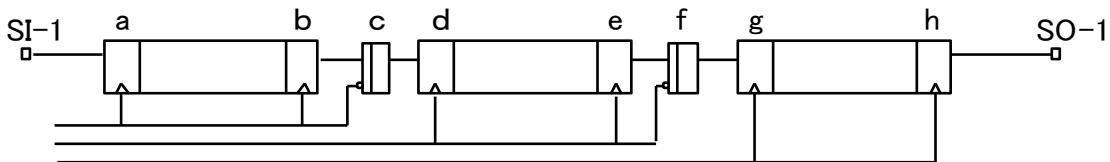
Cell list each clocked domain

4.2.5 SCAN_DEF file

This file is output for specifying the option “-POST”.

The change of file name is possible by -OUT_SCAN_DEF option.

But, if there is the error of DFT401-0, DFT401-1 or DFT401-2, the file is not made correctly.



Scan Chain : ScanIn → SI-1 / ScanOut → SO-1

Recognition Scan DEF (START and STOP is pin of F/F)

**a – c]
d – f]
g – h]** describe 3 of the left as Scan Chain

**a.SO – c.DATA
d.SO – f.DATA
g.SO – h.SIN**

Example:

```

DIVIDERCHAR "/" ;
VERSION 5.7 ;
BUSBITCHARS "[]";
DESIGN top ;

SCANCHAINS 3 ;
- chain_1_1
+ START block1/a SO
+ FLOATING
:
block1/b ( IN SIN ) ( OUT SO )
+ STOP block1/c DATA
+ PARTITION partition_clk1 MAXBITS 5 ;

- chain_1_2
+ START block1/d SO
+ FLOATING
:
+ STOP block1/f DATA
+ PARTITION partition_clk2 MAXBITS 5 ;

- chain_1_3
+ START block1/g SO
+ FLOATING
:
+ STOP block1/h SIN
+ PARTITION partition_clk3 MAXBITS 5 ;

END SCANCHAINS

END DESIGN

```

4.2.6 Debug file for scan chain

The path information is output for the scan chain which specified -PRT option of POST_DFT command in -PTSHLL. File name is "DFT401_debug.f".

Example:

```
set_strings POST_DFT scan_in1 scan_out1 -PRT ;
```

<Output Result>

The path is output in order of the input pin / output pin.

Format:

<hierarchy number> <pin name>(<cell name>) net(<net name>) [CLK(<clock name>)] [<<type>>]

```
=====
= Scan_in = scan_in1
= Scan_out = scan_out1
=====
+ 0 ud1.SIN(TH5KDFFAQXC)
+ 0 ud1.Q(TH5KDFFAQXC) net() CLK(clk1)
+ 0 ud1.SO(TH5KDFFAQXC) net(net1) CLK(clk1)
    + 1 ud2.DATA(TH5KDFFAQXCU)
    + 1 ud2.Q(TH5KDFFAQXCU) net(net2) CLK(clk1) <shift>
        + 2 ud3.DATA(TH5KDFFAQXCU)
        + 2 ud3.Q(TH5KDFFAQXCU) net(scan_out1) CLK(clk1) <shift>
        + 2 ud4.DATA(TH5KDFFAQXCU)
```

clock information

shift : Shift_register
lockup : Lockup cell
copy : Copy-Element



When there is much number of the steps, it is output without the indent by appointing the -DFT401_DEBUG_NOSPACE option.

4.2.7 RS chain list file (RS_list.f) --- β function

At the time of set_strings DFT501_MBIST_RS specification, the memory connected to the cell of the RSCHAIN type on RS chain and the instance of collared hierarchy are output. The collared memory module is searched for from instance of the memory to two hierarchies.

Example)

```
set_strings DFT501_MBIST_RS MODEREG/mbist_rs ; ← start signal of chain
```

Output example)

```
# cut.rs_select    ← cell instance of RSCHAIN type
cut.cut.uif_mem_dp2_01.ia_0_0.i0.i0 cut.cut.uif_mem_dp2_01.ia_0_0 # bdpa38p10e3b1zz0zz_dp58b112w2c_crlui
cut.cut.uif_mem_dp2_01.ib_0_1.i0.i0 cut.cut.uif_mem_dp2_01.ib_0_1 # vmc_pipeline_wrapper_mem_sp100
:
# cut.rs_select2   ← cell instance of RSCHAIN type
cut.cut.uif_mem_dp2_01.ia_0_0.i0.i0 cut.cut.uif_mem_dp2_01.ia_0_0 # vmc_pipeline_wrapper_mem_sp100
cut.cut.uif_mem_dp2_01.ib_0_1.i0.i0 cut.cut.uif_mem_dp2_01.ib_0_1 # vmc_pipeline_wrapper_mem_sp100
```

↑
Collared memory module name

4.2.8 FAV list file (FAV_list.f) --- β function

At the time of set_strings DFT501_MBIST_RS specification, the list of memory meeting the following conditions is output.

- There is it on RS chain.
- It does not have FAV pin or the logic of the FAV pin is not fixed.

The collared memory module is searched for from instance of the memory to two hierarchies.

Example)

```
set_strings DFT501_MBIST_RS MODEREG/mbist_rs ; ← start signal of chain
```

Output example)

```
cut.cut.uif_mem_dp2_01.ia_0_0.i0.i0 cut.cut.uif_mem_dp2_01.ia_0_0 # vmc_pipeline_wrapper_mem_sp100
cut.cut.uif_mem_dp2_01.ib_0_1.i0.i0 cut.cut.uif_mem_dp2_01.ib_0_1 # vmc_pipeline_wrapper_mem_sp100
```

↑
Collared memory module name

< Recognition of the collared module >

Specify the file which MEGIMI outputs by -FILE. Collared memory is thereby recognized.

This can substitute in file (Collared_type_out.f) which Collared_memory_extra command generates for DFT304-3.

In addition, please describe the individual specification as follows.

(1) Description for -FILE file

```
string CollaredMEM[] = { "b*c_cr*", "b*c_cm*", "b*c_co*", "b*c_cn*", "vmc_pipeline_wrapper_*",
                        "e*c_cr*", "e*c_cm*", "e*c_co*", "e*c_cn*",
                        "w*c_cr*", "w*c_cm*", "w*c_co*", "w*c_cn*",
                        "o*c_cr*", "o*c_cm*", "o*c_co*", "o*c_cn*",
                        "amcip*c_cr*", "amcip*c_cm*", "amcip*c_co*", "amcip*c_cn*"} ;
```

(2) Description for -PTSHELL file

```
set_strings CollaredMEM {b*c_cr*} {b*c_cm*} {b*c_co*} {b*c_cn*} {vmc_pipeline_wrapper_*} ;
set_strings CollaredMEM {e*c_cr*} {e*c_cm*} {e*c_co*} {e*c_cn*} ;
set_strings CollaredMEM {o*c_cr*} {o*c_cm*} {o*c_co*} {o*c_cn*} ;
set_strings CollaredMEM {w*c_cr*} {w*c_cm*} {w*c_co*} {w*c_cn*} ;
set_strings CollaredMEM {amcip*c_cr*} {amcip*c_cm*} {amcip*c_co*} {amcip*c_cn*} ;
```

But please specify the details not to overlap when the wild card overlaps with the user logic.

4.2.9 SENGEM insertion script file for SINGEN (SENGEN_insertion.dpf) --- β function

When set_strings ADD_SENGEN is specified in PTSHELL file, SENGEM insertion script is created automatically in DFT017.

Example)

```
set_strings SELECT_DC {tdr/select_dc} 1 {TCK};  
set_strings ADD_SENGEN b001;
```

Output Example)

```
SENGEN(1){  
    modulename: SENGEM_EOS ;           <---- cell name  
    instancename: b001.SENGEM_A_CK_1 ; <---- insertion instance name  
    TGN_clock_port: A_CK ;           <---- clock name  
    clock_net: w2 ;                  <---- net name  
    // <Mux: b001.mux1 >  
    FF_LIST: b001.ff1 ;              <---- MUX  
    // <Mux: b001.b101.b201.mux1 >  
    FF_LIST: b001.b101.b201.ff1 ;  
    // <Mux: b001.b101.b202.mux1 >  
    FF_LIST: b001.b101.b202.ff1 ;  
}  
SENGEN(2){  
    modulename: SENGEM_EOS ;  
    instancename: b001.b101.b301.SENGEM_B_CK_1 ;  
    TGN_clock_port: B_CK ;  
    clock_net: net1 ;  
    // <Mux: b001.b101.b301.mux1 >  
    FF_LIST: b001.b101.b301.ff1 ;  
}  
SENGEN(3){  
    modulename: SENGEM_EOS ;           <---- FF that is connected directly without passing MUX  
    instancename: b001.SENGEM_TCK_2 ;  
    TGN_clock_port: TCK ;  
    clock_net: w1 ;  
    FF_LIST: b001.ff2 ;  
    FF_LIST: b001.b101.b301.ff2 ;  
    FF_LIST: b001.b101.b202.ff2 ;  
    FF_LIST: b001.b101.b201.ff2 ;  
}
```

4.2.10 RSchain information file (INFO_DFT306_2.f)

At the time of set_strings INFO_DFT_306_2 specification, the memory connected to the cell of the RSCHAIN type on RS chain and the instance of collared hierarchy are output. The collared memory module is searched for from instance of the memory to two hierarchies.

Example)

```
set_strings INFO_DFT306_2 MODEREG/mbist_rs ; ← start signal of RSchain.
```

Output Example)

```
# MODEREG/mbist_rs ; ← start signal of RSchain.  
cut.cut.uif_mem_dp2_01.ia_0_0.i0.i0 cut.cut.uif_mem_dp2_01.ia_0_0 # vmc_pipeline_wrapper_mem_sp100  
cut.cut.uif_mem_dp2_01.ib_0_1.i0.i0 cut.cut.uif_mem_dp2_01.ib_0_1 # vmc_pipeline_wrapper_mem_sp100
```

↑
Collared memory module name

4.2.11 RAM memory information file without the NMA pin (INFO_DFT305_2.f)

RAM memory information without the NMA pin is output by “-CHECK_305_2” option. NMA pin is the pin having the attribute of NMA_C in NetWalker library. And RAM memory is the cell having the attribute of RAM.

Output Example)

```
cut.cut.uif_mem_dp2_01.ia_0_0.i0.i0 cut.cut.uif_mem_dp2_01.ia_0_0 # vmc_pipeline_wrapper_mem_sp100  
cut.cut.uif_mem_dp2_01.ib_0_1.i0.i0 cut.cut.uif_mem_dp2_01.ib_0_1 # vmc_pipeline_wrapper_mem_sp100
```

↑
Collared memory module name

5. Rule Implementation Results

The contents of the messages showing rule execution results are listed below.

5.1 ERROR Message List

No	Design Rule	Message	Content
0	Library check	ERROR DFT000 -1: Undefine NetWalker Cell Library Type.	Library check
	Pattern check	ERROR DFT000 -2 Initial pattern check	Comparison between simulation result by -PATTERNM and expectation specified by PATTERN_MONITOR_SIGNAL
1	Prohibit feedback loop formed by combined circuit only	ERROR DFT001 -1: Feed Back Loop.	Feedback loop formed by a combined circuit detected at <i>element name</i> (identified by FF output). The <i>Feedback-Loop</i> content is as follows: <i>element instance name. output terminal name -> input terminal name</i>
2	Only edge-trigger type F/F used	ERROR DFT002 -1: Cell Type of prohibition of use	A (cell name) is being used. There are <i>number</i> of these cells.
3	All FF clocks can be controlled directly from external source <i>(Note2)</i>	ERROR DFT003 -1: Clock is Gated.	Input clock does not reach FF clock pin due to <i>instance name (cell name)</i> .
		ERROR DFT003 -2: The clock is connected with F/F, but not a clock terminal	The clock is connected with F/F, but not a clock pin.
		ERROR DFT003 -3: The clock is connected with F/F, but it reverses with the origin	The clock is connected with F/F, but it reverses with the origin.
		WARNING DFT003 -4: The clock is connected directly with the output port	The clock is connected directly with the output port.
		ERROR DFT003 -5: The clock is not connected with the clock terminal of PLL	Clock does not reach PLL clock pin (<i>instance name. terminal name (cell name)</i>)
		ERROR DFT003 -6: The clock terminal of PLL is not connected directly with an external terminal	Clock reaching PLL clock pin cannot be controlled directly from external source. The uncontrollable element is <i>element name (cell name)</i> .
		ERROR DFT003 -7: The clock is not connected with the clock terminal of F/F	Clock net and clock pin not connected directly, or clock net not specified.
		ERROR DFT003 -8: FF Clock Term is fixed	Clock pin fixed to power supply/GND
		ERROR DFT003 -9: The Clock Signal is connected with the Crystal cell	The Crystal cell is used as test clock.
		ERROR DFT003 -10: This clock signal has already been specified by another clock definition.	The signal on clock tree that has already been specified by -PTSHLL clock definition is specified again.
4	Set/Reset of all FF can be controlled directly from external source, and do not function during Scan <i>(Note1)</i>	ERROR DFT004 -1: Set terminal of F/F not Controlable	FF set pin (<i>instance name. terminal name</i>) cannot be controlled directly from external source.
		ERROR DFT004 -2: Reset terminal of F/F not Controlable.	FF reset pin (<i>instance name. terminal name</i>) cannot be controlled directly from external source.
		ERROR DFT004 -3: Set/Reset specified with ptshell is connected with F/F, but not a Set/Reset terminal	Set/reset pin specified with -PTSHLL is connected to other than the set/reset pins of the FF.
		ERROR DFT004 -4: Set/Reset specified with ptshell is connected with F/F, but it reverses with the origin.	Set/reset pin specified with -PTSHLL is connected to other than the set/reset pins of the FF. But the phase is reversed.
		ERROR DFT004 -5: The register which has Set and Reset need to fix one side unactively.	The register which has both Set and Reset pins needs either pin fixed to inactive.
		WARNING DFT004-6 : F/F of Set is fixed no-activity.	Set pin of FF is fixed to non-active logic.
		WARNING DFT004-7 : F/F of Reset is fixed no-activity.	Reset pin of FF is fixed to non-active logic.
7	Only one bus drive becomes active during test	ERROR DFT007 -1: Bus Control (NeedOnly One Drive). <i>(Note 3) (Note 4)</i>	Possibility of conflict/floating in bus (<i>bus name</i>).
8	Black box handling	With -LBIST option WARNING DFT008 -1: Black Box Check (Output) Can not fault detected. <i>Note) Execution by -CHECK_008_1</i>	No measures for connecting FF, etc. to output (net name) of black box (<i>instance name</i>). Undetected faults are number at cell pin.
		Without -LBIST option ERROR DFT008 -3: Black Box Check (The spread of an unknown value does not permit)	The indeterminate values of black boxes must not propagate to the FF.

No	Design Rule	Message	Content
		Without -LBIST option ERROR DFT008 -4: Black Box Check (The both terminal does not permit)	Cells with bidirectional pins must not be used because they could be the sources of indeterminate values.
		WARNING DFT008 -2: Black Box Check (Input). Note) Execution by -CHECK_008_2	No measures for connecting FF, etc. to input (net name) of black box (<i>instance name</i>). Undetected faults are number at cell pin.
		ERROR DFT008 -5: RAM/ROM input terminals are not connected observation F/F.	Observation FF is not connected in RAM/ROM
9	Clock transfer	INFO DFT009 -1: Clock Pair.	Transfer from clock 1 to clock 2 implemented.
		ERROR DFT009 -2: PLL Clock Check.	More than one PLL (<i>PLL1</i> , <i>PLL2</i>) referring to a single clock.
10	Undetected fault report for supply of fixed value (test mode, etc.)	WARNING DFT010 -1: Undetect Fault for Signal tied high/low.	Cannot detect fault passing through <i>instance name.terminal name (net instance name)</i> due to input of fixed value. Undetected faults are number at cell pin.
11	Others	With -LBIST option ERROR DFT011 -1: The following cell instance's input pins are dangling.	The input pins are dangling.
		ERROR DFT011 -2 : The clock is connected with the terminal which is not the clock terminal. and there is a problem in timing.	The clock is connected with the terminal which is not the clock pin and there is a problem in timing.
		WARNING DFT011 -3: Set/Reset signal is connected with the data terminal.	The set/reset signal is connected with the data terminal.
12	-	-	-
13	Enable signal of Gated Clock cell	ERROR DFT013 -1: Clock Gated Cell Enable Check (Propagating an unknown value is not permitted)	Clock Gated Cell Enable Check (Propagating an unknown value is not permitted).
		ERROR DFT013 -2: Clock Gated Cell Enable Check (Connected external ports is not permitted).	Clock Gated Cell Enable Check (Connected external ports is not permitted).
		ERROR DFT013 -3: Clock Gated Cell Output is fixed. Can not fault detected	Clock Gated Cell Output is fixed. Can not fault detected.
		ERROR DFT013 -4: Clock Gated Cell is through mode at capture mode.	Clock is through at capture mode.
		WARNING DFT013 -5: Clock Gated Cell is clock through mode at capture mode. Note) ERROR in POST mode.	Clock is through at capture mode.
		WARNING DFT013 -6: CEN pin of Clock Gated Cell is High fixed.	Clock is through.
		ERROR DFT013 -7: SMC pin of Clock Gated Cell is not High fixed or Low fixed by SCAN_EN.	Clock is through.
		WARNING DFT013 -8: The clock_pin of Clock Gated Cell is not connected to clock signal.	Clock does not reach.
		ERROR DFT013 -9: SMC pin of Clock Gated Cell is not connected same clock control register.	The clock is different from the clock generating SCAN Enable signal.
		WARNING DFT013 -10: Clock_Gated Cell is clock through mode at capture mode. Note) The following specification is necessary. set_strings CHK_DFT013_10 yes;	SMC pin is low.
		ERROR DFT013 -11: Clocks of the observation FF are different from the clock of GCK	The enable signal of GCK cell is not connected to the observation FF at DC mode.
		WARING DFT013 -12: Clock of GCK is inverted. GCK cell can not work AC test. Note) Execution by -CHECK_013_12	Because clock of GCK is inversion, AC test cannot execute in SHINGEN.
		ERROR DFT013-13: Icsc check for GCK at AC test Note) Execution at the time of select_dc design	GCK exists behind MUX switching the clock.
14	ATPG	ERROR DFT014-1 : This module output ports don't use.	This module output ports don't use. The definition of command is necessary.
15	Fixed value check	ERROR DFT015 -1: Need to fix the terminal.	The terminal of memory or hard module needs to fix at each mode.
17	Bypass clock check	ERROR DFT017 -0: Can not find Multiplexer Gate.	Multiplexer does not exist.

No	Design Rule	Message	Content
		ERROR DFT017 -1: Clock is transferred to FlipFlop. But different.	The clock reached. But composition is different from the original clock.
		ERROR DFT017 -2: Clock is not transferred to FlipFlop.	Clock does not reach.
		ERROR DFT017 -3: Clock invert or Null at Select DC.	The clock is inverted or does not reach to multiplexer.
		INFO DFT017 -4: MUX INFOMATION	The clock information of multiplexer is output.
		ERROR DFT017 -5: Muxs are duplicated	Multiplexers are connected repeatedly on AC clock line.
		ERROR DFT017 -6: The Register is not controled by Select_dc	The register which AC clock controlled with SELECT_DC signal does not arrive at exists.
		ERROR DFT017 -7: The MUX is not defined by ADD_SENGEN	Mux which is not defined by ADD_SENGEN exists.
		ERROR DFT017-8 : Different Clocks Propagate at MUXs	User clock is connected to the multiplexer which controlled by different SELECT_DC signal.
		ERROR DFT017-9 : There are mistakes to define strings SELCECT_DC	Definition of SELECT_DC includes mistake.
		ERROR DFT017-10 : Diferrent select_dc at SCANEN and FlipFlops	SENGEN is not controlled with the clock same as scan FF.
18	Connection of ATOM SKBR pin and ScanEnable generation cell	INFO DFT018-0 : ATOM SKBR pin connection check	ATOM_SKBR_CHK is not specified.
		ERROR DFT018 -1: ATOM SKBR pin connection check	Connection is different from expectation specified by ATOM_SKBR_CHK.
		ERROR FT018 -2: SCANEN_SEM pin is not connected ATOM_SKBR pin.	SEM pin of ScanEnable cell does not have connection.
19	IOAC SCAN test	ERROR DFT019 -2: Can not find a path of IO_AC_FILE in netlist.	There is not the specified condition in netlist.
		ERROR DFT019 -3: Can not find Clock defined by IOAC_PORT	There is not the specification of IOAC_PORT. Or clock does not reach.
20	FFR test	ERROR DFT020 -1: There is a net beyond the limitation of FFR.	FFR exceeds an upper limitation.
21	Field Bist check	ERROR DFT021-0: Not defined port by CSV files.	The port which was defined with CSV file does not exist.
		ERROR DFT021-1: The unknown signal propagate.	The signal that a mask is necessary is not masked.
		ERROR DFT021-2: The specified mask signal is the wrong connection.	The mask prohibition signal is masked. (The unconnected net is checked, too.)
		ERROR DFT021-3: The specified mask signal(output) is not fixed.	The output pin is not the logic fixation value same as CSV.
		ERROR DFT021-8 : Unmatch the Name Rule.	The port defined in CSV violated the naming rule.
		ERROR DFT021-9 : Can not find the net defined by CSV files	The port defined in CSV does not exist.
22	DVFS area test	ERROR DFT022-1: There is illegal transfer at DVFS.	Transfer between DVFS is not reversed.
23	Connection of SENG恩 circuit	ERROR DFT023-1 : Wrong connection at SENG恩 cell.	SENG is not connecting to the gated clockcell. Or SEN is not connecting to the register.
999	Total undetected fault report	INFO DFT999 -1: Total Undetect Fault Count is 0	The total number of cell pins not detected for faults is number.

(Note 1)

If the set/reset pins are fixed to active, they can not be controlled.

(Note 2)

The module specified by -ALREADY_SCAN_MODULE is checked in DFT003.

The instance specified by -OUTSIDE_SCAN_INS and the control register specified by -DFT_CONTROL_REG are not checked.

But it is checked because DFT003-1 serves as the clock line check too.

The cell specified by -CHECK_EXCLUSION_MODULE is checked in DFT003-2/3.

(Note 3)

DFT 007-1 : when executing in module unit, in some cases a false error may be output if a signal supplied from an external source is used to form the bus.

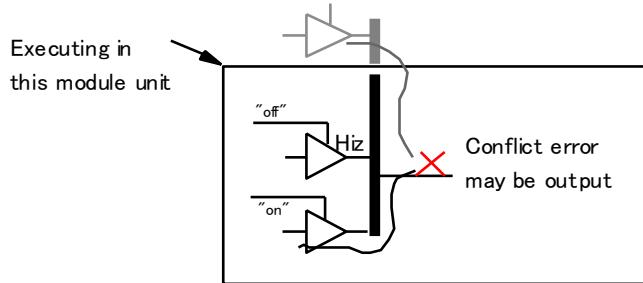


Figure 5.1 Error Example for DFT 007-1

(Note 4)

DFT007-1 needs to control the bus with the test_mode pin as shown in Figure 5.2. For the one-hot case shown in Figure 5.3, there is no need to control with the test_mode pin.

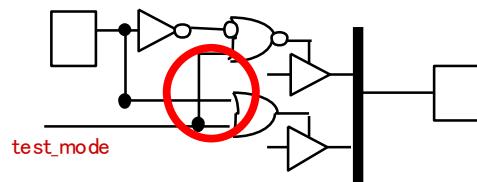


Figure 5.2 Example (1) for DFT 007-1

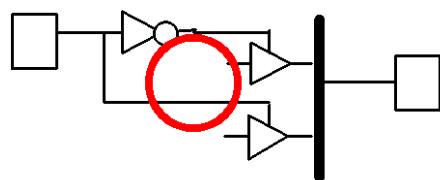


Figure 5.3 Example (2) for DFT 007-1

Check Items for - SINGEN option

No	Design Rule	Message	Content
1	Prohibited of indeterminate values propagation during BIST	ERROR DFT100-1: DFTRAM is defined in NetWalker cell library.	DFTRAM is defined at NetWalker library. (Measure) Delete DFTRAM from NetWalker library. And specify Verilog or VHDL library.
		ERROR DFT101 -1: Clock Through IO Cell.	FF clock is put through to IO cell. (Prohibited because indeterminate value (=clock) is latched when BS cell is added.) (Measure) Specify EXTEST.
		ERROR DFT108 -1: BlackBox X Value Through IO Cell.	The indeterminate value (RAM macro output, etc) is put through to IO cell. (Prohibited because indeterminate value is latched when BS cell is added.) (Measure) Specify EXTEST.
		ERROR DFT109 -1: NOBS/EXTEST input/inout Pin NOT Fixed Value or Clock.	The LSI port that no BS cells are added (NOBS) or observation type BS cells are specified to be added (EXTEST) does not have a fixed value. (The indeterminate value is latched.) (Measure) Set fixed value in ptshell.
		ERROR DFT109 -2: NOBS inout Pin Fixed Value or Clock, NOT Disable.	Although the bidirectional LSI port without BS cells has a fixed value or clock set for it, output enable is not set to input mode. (Measure) The logic change or setting of the fixed value
		WARNING DFT109 -3: input/inout Pin Fixed Value or Clock, But NOT NOBS/EXTEST.	Although the bidirectional LSI port has a fixed value or clock set for it, no BS cells are added (NOBS) or observation type BS cells are not specified to be added (EXTEST). (Fixed value has no effect.) (Measure) Specify NOBS or EXTEST in DFT profile.

Check Items for -MINORI / -PREMINORI / -POSTMINORI option

No	Design Rule	Message	Content
1	Clock connection in MINORI mode	ERROR DFT301 -1: Undefined Clock.	The clock is not reached to each clock pin of RAM and ROM.
		ERROR DFT301 -2: Clock is connected undefined terminal.	Clock is connected undefined terminal.
		ERROR DFT301 -3: Different Clock at Multi-Clock.	Different Clock at Multi-Clock.
		INFO DFT301 -4: defined Clock.	Information of Specific RAM/ROM
		INFO DFT301 -5: Number of Flip/Flop connected with the Clock.	Information of number of Flip/Flop connected with the Clock.
2	Clock connection in POSTMINORI and PREMINORI mode	ERROR DFT302 -1: Undefined Clock.	The clock is not reached to each clock pin of RAM and ROM.
2	Clock connection in POSTMINORI mode	ERROR DFT302 -2: Clocks of Porta and Portb need to same at MINORI test	The same clock does not propagate to multiple port RAM.
		ERROR DFT303 -1: The clocks of RAM/ROM and bridge circuit need to same, Moreover, at MINORI test, RAM and bridge circuit need to be connected direct.	The clock source of the first F/F and RAM is not same, in the terminal which a Bridge circuit is connected to.
3	Collared Memory check in PREMINORI mode	ERROR DFT304 -2: The memory cells are not included in Collared Memory	The memory cells are not included in Collared Memory.
		ERROR DFT304 -3: The Collared Memory module is not same, when it was RTL	The Collared Memory module is not same, when it was RTL.
4	NMA connection in POSTMINORI mode	ERROR DFT305 -1: NMA check (wrong connect).	The connection of the NAM pin is different from specification of PT shell (NMA_TEST).
5		nothing (output INFO_DFT305_2.f)	RAM without the NMA pin is reported.
6	RS connection in POSTMINORI mode	ERROR DFT306 -1: Not control RS term at USER mode.	The RS pin of CRAM is not controlled in user mode.
7		nothing (output INFO_DFT306_2.f)	The case that RS signal is connected to memory in parallel is reported.
8	Memory control signal connection in POSTMINORI	ERROR DFT307 -1: Memory control signals need to a same register.	The terminal with the following attributes is not controlled by the same register. TE1,TE2,TMA,TAE
9		ERROR DFT307 -2 : Memory test pin (TE3/TE4) connection check.	<ul style="list-style-type: none"> • The logic of TE3 pins of all SRAM is not equal. • The logic of TE4 pins of all SRAM is not equal. • The logic of TE3 and TE4 is equal.

Check Items for -POST option

DFT002/DFT003/DFT004/DFT007/DFT011/DFT013/DFT015/DFT018 and the following check item are executed.

No	Design Rule	Message	Content
1	Clock connection in POST mode	ERROR DFT401 -0: Scandef file check	The format of SCAN_DEF file is incorrect.
		ERROR DFT401 -1: Scan chain list check.	Check whether ScanChain list file is right Example: There is lock-up latch behind Scan-in.
		ERROR DFT401 -2: Scan chain check.	ScanChain list file does not have F/F included in ScanChain.
		ERROR DFT401 -3: Not connected Scan chain.	F/F in ScanChain list file is not included in ScanChain.
		ERROR DFT401 -4: Check SCAN DEF.	The SCAN_DEF file specified by -IN_SCAN_DEF and the SCAN_DEF file generated from the internal net are disagreement. (The comparison of scan chain in pre layout and post layout)
		ERROR DFT401 -5: Clock of SCAN_EN is not different from Clock of register.	There is a problem for connection of SCAN Enable signal.
		ERROR DFT401 -6: The register is connected non scan_chain_register at capture mode.	The register which the scan chain does not have is connected in capture mode.
		WARNING DFT401 -7: The transfer is different controlling cell of selector function at select_dc.	The scan chain was separated by SELECT_DC.

Check Items for –CHECK_601 option

No	Design Rule	Message	Content
1	Digital hard macro	ERROR DFT601 -1: Input port is not connected observed FF	Inout port does not arrive at ScanFF and external port.
		ERROR DFT601 -2: Output port is not connected un-control signal	The signal arriving at the output / inout port is not the output of ScanFF and external port.
		ERROR DFT601 -3: Signal of create_clock is not external_pin	The signal specified by create_clock is not external port.
		ERROR DFT601 -4: SCAN_EN of set_strings is not external_pin	The signal specified by SCAN_EN is not external port.
		ERROR DFT601 -5: SCAN_EN Cell check (differnt clock)	The clock connected to the clock pin and DATA pin of the SCANEN cell is not same.
		ERROR DFT601 -6: ATOM_SKBR_CHK of set_strings is not external_pin	The signal specified by ATOM_SKBR_CHK is not external port.
		ERROR DFT601 -7: ATOM_SKBR_CHK of set_strings ALL option is not possible. Please define Clock	The hard module cannot specify “ALL” option of ATOM_SKBR_CHK.

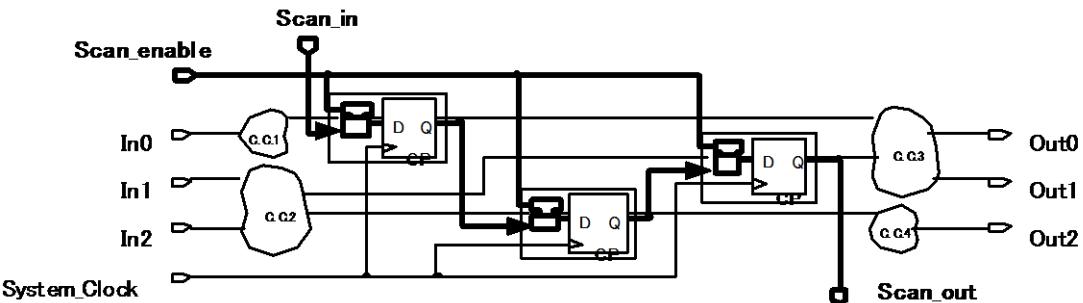
(Note)

When -CHECK_601 is specified at -MUXSCAN/-LBIST/-POST mode, this check is executed.

5.2 Check Items for MuxScan and LBIST Mode

5.2.1 MuxScan Method

In the MuxScan method, the data input part of the FF has a multiplexer attached, and the ordinary path and the path connecting FFs together (Scan_Chain) are controlled by the Scan control pin (Scan_enable). During normal operation, the multiplexer attached to the data input of the FF is fixed on the ordinary path side while in operation. To control (Scan_in) and observe (Scan_out) the internal status of the FF, switch over data input to the Scan_Chain side to let all FFs operate as shift registers (Scan_operate/Scan_Shift). Also, the memory devices handled consist only of edge-triggered FFs, and the clock (System_Clock) used during normal operation is used for Scan operation (Scan_clock). Therefore, the input pattern is scanned-in as shift register and operated on (capture_operate), and the result is compared with the scanned-out expected value.



* The devices with bold texts are added (terminal/net) and replaced (FF → FF with Mux) during scan.

Figure 5.4 Circuit in MuxScan Method

5.2.2 LogicBist Method

This is basically the same as the MuxScan method, except that the LogicBist method has a circuit incorporated in the chip that sign-compresses the results of random input pattern generation and capture operation instead of scan-in/scan-out, with comparison made between the compressed result and the expected value.

5.2.3 Differences between MuxScan and LogicBist for Constraints

Constraints are different in cases when black boxes, etc. exist and indeterminate state propagates to the flip-flop. In the MuxScan method, if an indeterminate state occurs in capture operation, the expected value is masked. The paths through which the indeterminate state propagates cannot be detected, but the low detection rates practically are not a problem. In the LogicBist method, however, an indeterminate state cannot be handled because indeterminate values cannot be sign-compressed. The -LBIST operation has enhanced restrictions on indeterminate propagation.

- (1) The indeterminate values of black boxes must not propagate to the FF.
- (2) Cells with bidirectional pins must not be used because they could be the sources of indeterminate values.

5.2.4 DFT002

Use of only edge trigger type F/F (-MUXSCAN/-LBIST)

The latch not to go through at test mode and the FF that is replaced with scan FF are errors.

< scan FF >

At -MUXSCAN (default) mode, if SMC pin of the scan FF is being fixed, scan is possible. Therefore, the scan FF is not an error. At -SINGEN mode, because DFTcheck does not support, this is an error.

(-LBIST mode supports this.)

through latch

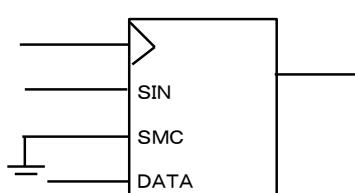
: Latch which the enable pin was fixed or latch which the reverse clock of front or back FF inputs

FF that is replaced with scan FF

: FF that cell type was defined as type=MUX_FF

scan FF

: FF that cell type was defined as type=AF_MUX_FF



scan FF that is not error

Note)

The latch and the FF to be under the scan exclusion module or the scan module are not checked.

< exclusion of scan>

Specify it by -OUTSIDE_SCAN_INS option.

< scan module >

Specify it by -ALREADY_SCAN_MODULE option. Or specify it by set_strings ALREADY_SCAN_MODULE in PTSHELL file.

Moratorium on virtual FF (-POST)

When virtual FF is used in the netlist after the scan, it is an error.

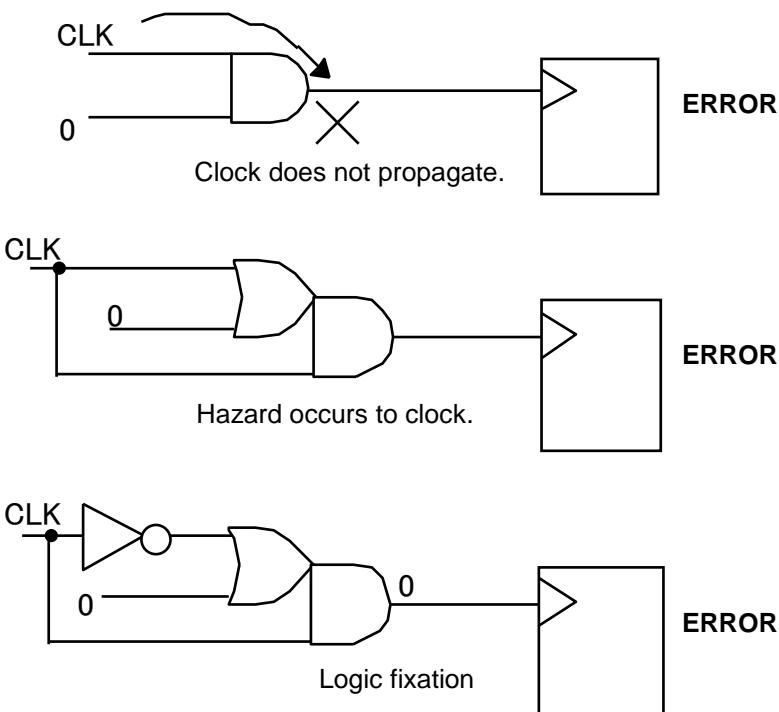
If NetWlaker library does not have the attribute of DUMMYFF, revise NetWlaker library.

Or specify follows in PTSHELL file.

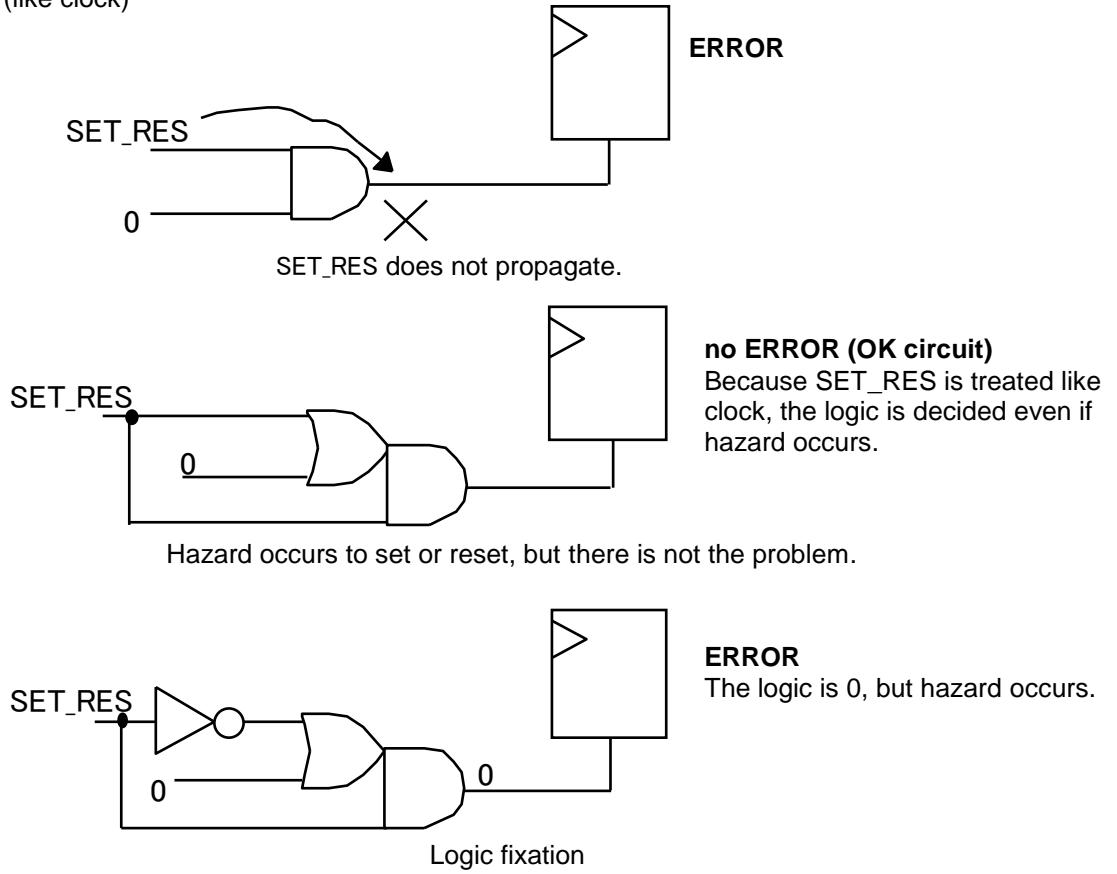
```
set_cell_type <cell name> DUMMYFF ;
```

5.2.5 DFT003-1 (Clock is gated)

(1) Clock

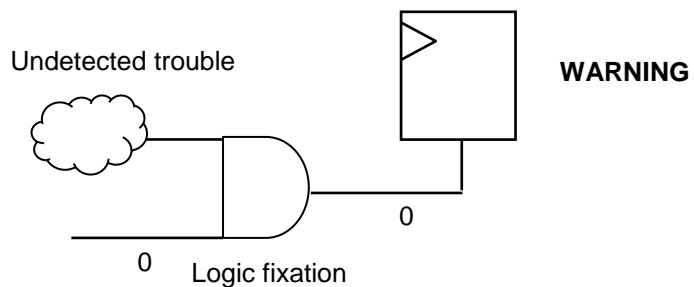
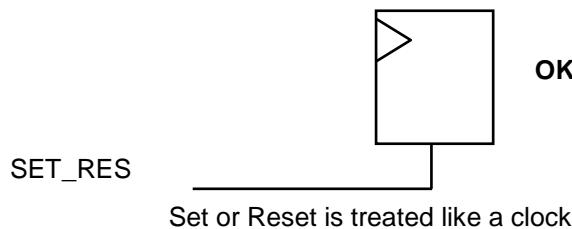


(2) Set/Reset (like clock)



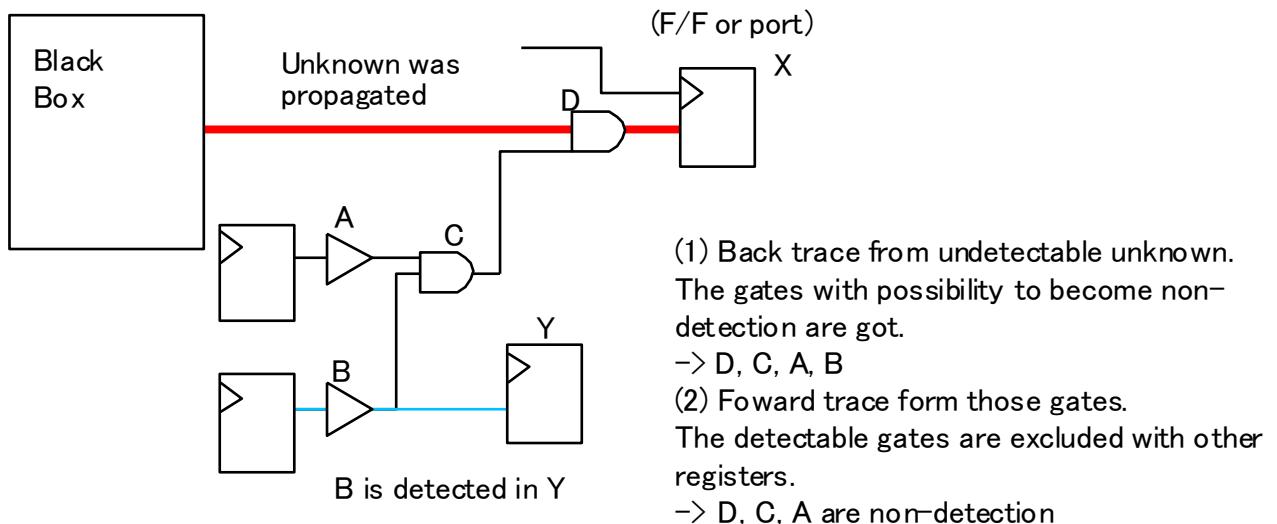
5.2.6 DFT004-6/7

When set or reset is treated like a clock, trouble about it can detect.
If set or reset is non-active, test is effective. But trouble about set or reset can not detect.
Therefore it is desirable that set or reset is treated like a clock.



5.2.7 DFT008-01

Check trouble detection fall by the unknown of output terminal of Black Box. When -CHECK_008 is specified, this check is executed. The detection conditions are shown as follows.



5.2.8 DFT008-05 (Observation check of ROM / RAM)

Observation F/F observes propagated trouble to ROM / RAM.

The input terminal of ROM / RAM that observation F/F is necessary should add observation F/F by automation tools such as MINORI or user.

The terminal needing observation F/F is mentioned in a NetWalker library.

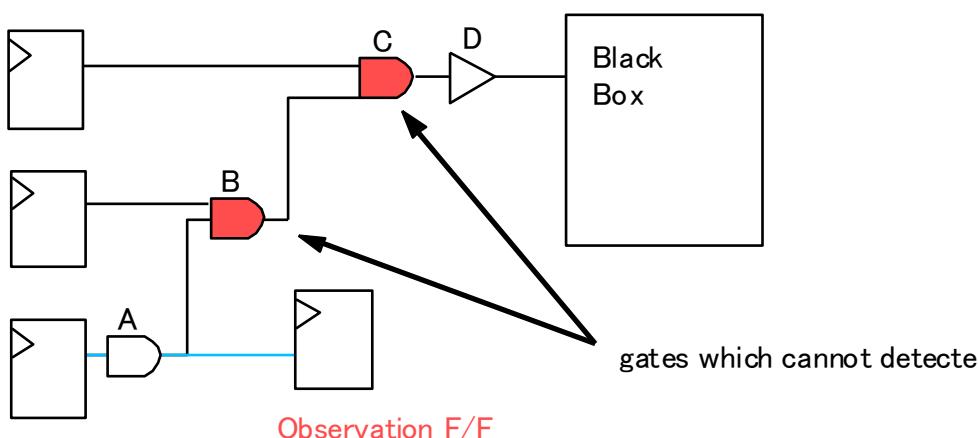
Check whether observation F/F is connected to ROM / RAM.

Other Black Box is checked with DFT008-2.

Observation F/F and RAM / ROM must not be connected with gate except Buffer or Inverter.

In the following example, cells of B and C become ERROR for non-detection.

In addition, please specify -DETAILED_008_5 to get the number of cells more than two input that were not detected.



Note1:

It is not checked whether clock is connected in POSTMINORI or PREMINOR mode. The reason is because a clock is not yet connected to the clock terminal of observation F/F.

Note2:

The gate which became same as Buffer or Inverter because the one terminal was fixed is not considered to be Buffer or Inverter. The reason is because the observation characteristics of the gate worsen, if the logic fixation signal is connected to mode signal at MINORI.

< The automatic insertion of observation F/F >

If you specify by “- DFTCLEAN_DFT008_5” option, the script of NetEdit which inserts observation F/F to the net which became the error in DFT008-5 is output. The script file name is “DFTCLEAN_DFT008_5.tcl”. Please go in the following procedure if you use this script.

Step1 <DFTcheck command>

```
%DFTcheck ¥
-RENEW ¥
test1.v ¥
-PTSSHLL ptshell.Tst ¥
-DFTCLEAN_DFT008_5 ¥
-NWCELL ..//common_lib/CELL_def ¥
-TOP LSI ¥
-WORK work
```

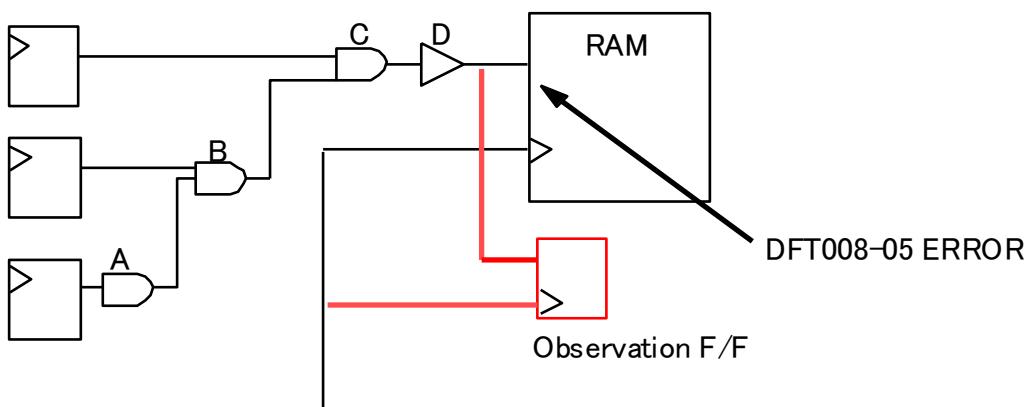
Step2 <Revision of DFTCLEAN_DFT008_5.tcl>

```
#####
# DFTCLEAN DFT008-05 observed ERROR          #
# please set cell_name data and clock term    #
#####
set ctype(@cell) $cell_name
set d_term xxxx
set ck_term xxxx
set ctype($ck_term) {ck};set ctype($d_term) {E};
create_gate_and_connect {¥DFTCLEAN_A7_RST[1]} ctype;
:
#####
# output verilog                            #
# print_verilog_sourt file_name [module_name]#
#####
print_verilog_source out.v
```

<< Specify the information of
the insertion cell>>
set ctype(@cell) dssfbtab 1
set d_term d
set ck_term cp

Please add cell name and data terminal name and clock terminal name of observation F/F to insert.
A default of the output file name is “out.v”.

The clock terminal of observation F/F is connected to clock signal of RAM which became the problem.



Step3 <NetEdit execution>

```
%NetEdit ¥  
-RENEW ¥  
test1.v ¥  
-TCL DFTCLEAN_DFT008_5.tcl ¥  
-NWCELL ..//common_lib/CELL_def ¥  
-TOP LSI ¥  
-WORK work
```

<< The explanation of the NetEdit function >>

Please refer to NetEdit user guide for the details.

Function specifications of create_gate_and_connect

Name	create_gate_and_connect
Format	create_gate_and_connect instance_name array_name
Function	[The insertion and the connection of the cell] The cell is inserted in specified instance, and it is connected according to the array. array_name : Define the information of cell to insert with the following forms. set array_name(@cell) cell_name [set array_name(term_name) net_name]* [set array_name(term_name) Fixation_value]* << keyword which defines the connection information of the terminal >> term_name : terminal name of cell net_name : net name to connect to term_name Fixation_value : 1'b0 or 1'b1
return	0 : success 1 : failure

5.2.9 DFT009-2 PLL Clock Check

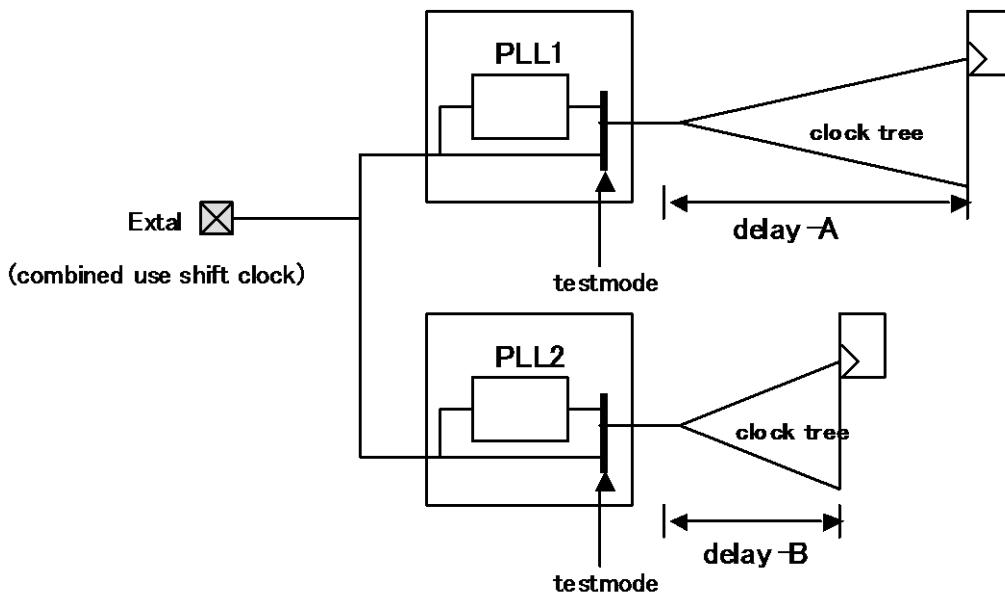
More than one PLL (PLL1 and PLL2) refers to a single clock.

When clock passes through PLL, the circuit after PLL generally makes latency equal. However, in the case of different PLL, latency of the circuit after PLL does not make equal.

Since delay-A and delay-B are different latency in chart below, latency is not equal when EXtal bypasses PLL.

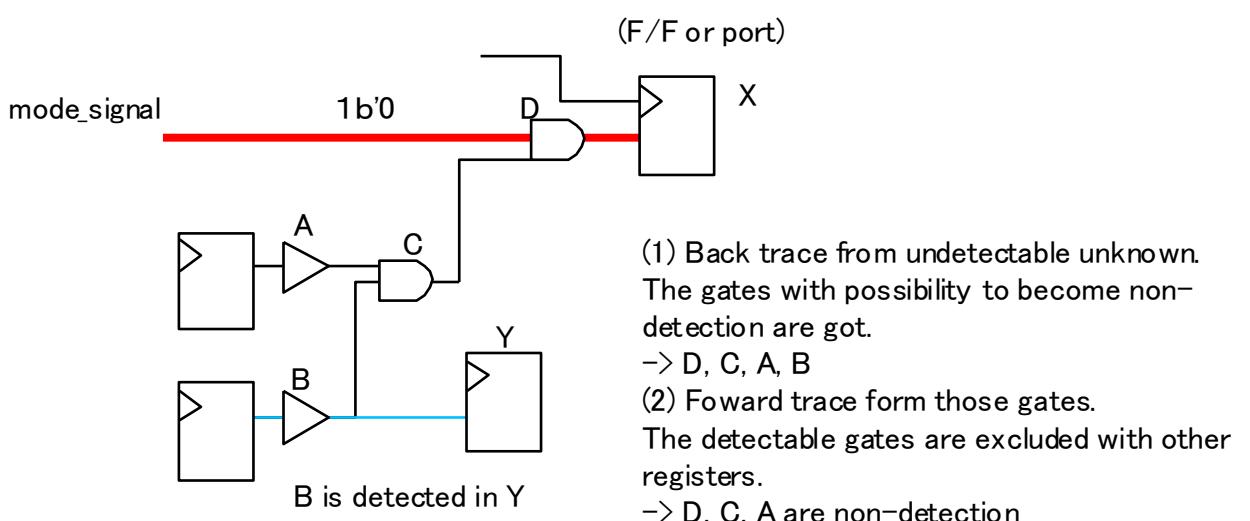
In the case of user mode, the edge will match to adjust timing in PLL.

When latency makes equal according to the recognition mentioned above, it is OK. (pseudo error)



5.2.10 DFT010-1

Check trouble detection fall by logic fixation. The detection conditions are shown as follows.

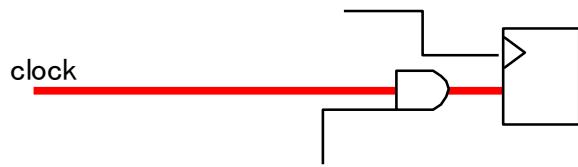


Note:

It is checked by the fixed signal in the capture mode.

5.2.11 DFT011-2 Clock is connected to terminal other than clock

If clock or the reset of clock handling at the time of test connects to terminal other than clock, there are the problems for timing.



Detection condition:

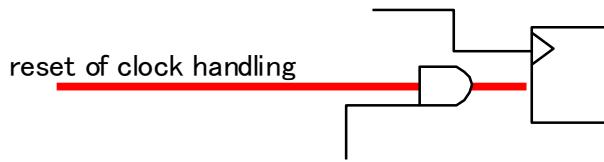
The clock or the reset of clock handling at the time of test is the following cases.

- (1) It is connected to the enable terminal of the GCK cell.
- (2) It is connected to the terminal of F/F other than the clock or the set/reset.

5.2.12 DFT011-3 Reset is connected to the data terminal

If the reset of clock handling connects to clock terminal of F/F, because clock and the reset do not change at the same time and async reset is given priority to over data change, there is not the problem of the timing. It is warning.

But the trouble detection rate decreases because async reset input into data terminal of FF is fixed to off-state value at the time of test. Because the circuitry decreases the trouble detection rate, the confirmation of the result is necessary.



5.2.13 DFT013 Check the enable terminal of gated clock cell

The CGT (SMC) terminal of a gated clock cell need to connect to a scan enable signal or a test mode signal in AC test. In addition, because the SMC terminal is fixed to high (test mode) on only DC test, connection of observation FF for the trouble detection of CEN terminal is necessary.

The case connected to the scan enable in AC test requires the following attention.

<AC test>

When CGT(SMC) terminal of gated clock cell connected a test mode signal, please fix this signal by set_case_analysis . The clock becomes the through state.

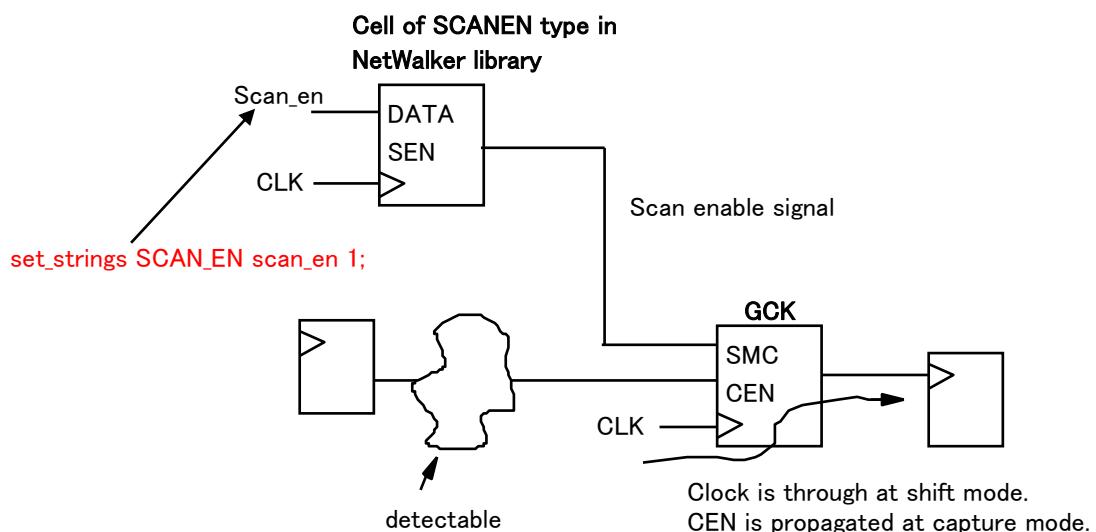
But when CGT(SMC) terminal of gated clock cell connected a scan enable signal, please fix a scan enable signal to high (shift mode) by -SCAN_EN command. Don't use set_case_analysis.

Because, at set_case_analysis, DFTcheck cannot distinguish capture mode from shift mode.

Example)

```
-SCAN_EN <signal_name> <value>
Value: "H" "L" "1" "0"
```

But if the cell for exclusive use of Scan Enable is used, it is recognized without above specification automatically.



In addition, specify GCK cell which excludes from check as follows in the PT_SHELL file.

```
set_strings DFT013_CANCEL_GCK_INS <Instance of GCK>
```

Note:

The GCK cell included in the module specified by set_strings ALREADY_SCAN_MODULE is not checked.

When a test terminal is fixed to 0 and is unconnected to a test pin in RTL, it must be connected by connect_direct function virtually.

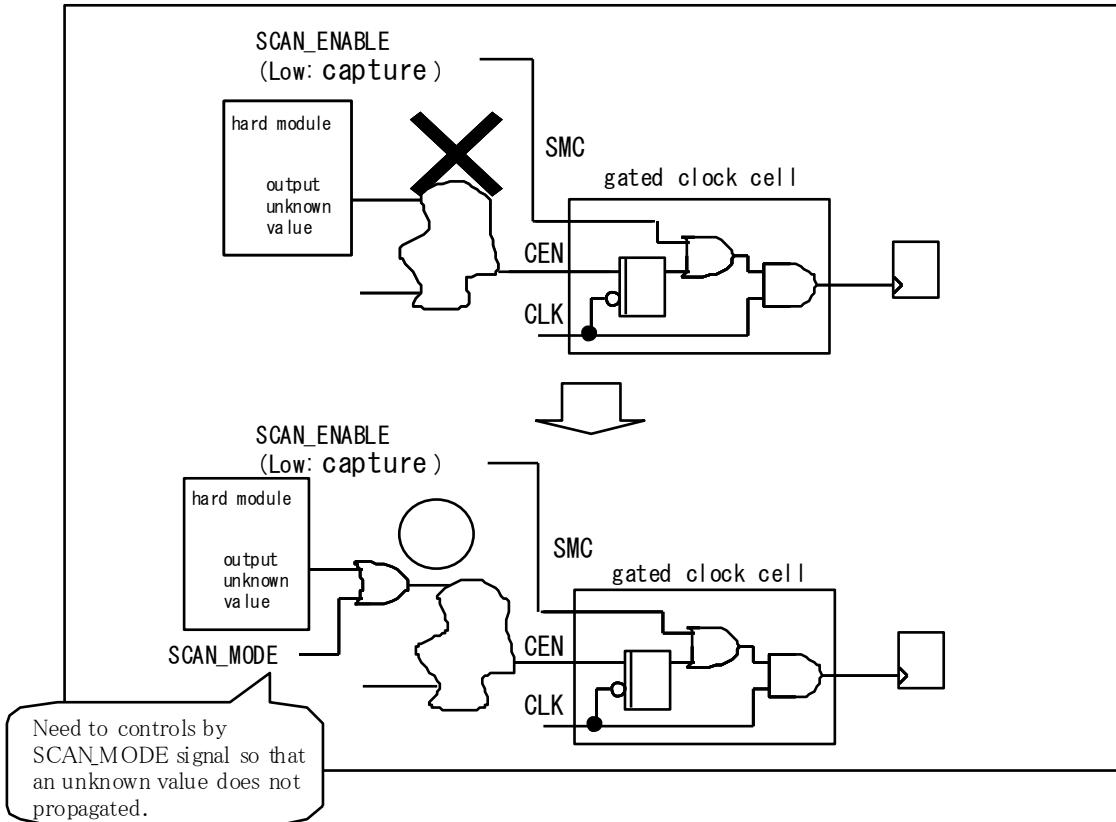
Refer to the later page (<The case which the test pin of the gated clock circuit connects to test terminal with DFT tool>).

DFT013-1 Check fault propagation to enable terminal

At shift scan mode, SCAN_ENABLE is fixed high, so, clock is always propagated to F/F.

On the other hand, capture mode, SCAN_ENABLE is fixed Low, clock is decided by the value of CEN signal. When an unknown value goes into this CEN signal, in a simulator, the output value of F/F becomes unknown. But in FastSCAN, though 0-X-0 signal goes into the clock of F/F, it performs operation equivalent to 0-1-0, and generates an expected value.

Therefore, it is necessary to make an unknown value not propagated CEN signal.



< Factor that the unknown occurs >

PRE : Hard module, LATCH which does not pass through, signal conflict, test exclusion F/F or external port
 POST : Register except the SCAN chain or external port

< Exclusion of the test control register >

The register for tests does not cause the unknown. Please exclude check as follows in the PT_SHELL file.

Example) set_strings DFT_CONTROL_REG <instance of module or register>

<Exclusion of the external port : POST>

When module unit is checked, the external port does not always cause the unknown.

There are two methods to exclude external port from the factor that the unknown occurs.

(1) If it is all exclusion, specify -CANCEL_PRIMARY option.

(2) If it is partial exclusion, exclude check as follows in the PT_SHELL file.

Example) set_strings DFT013_CANCEL_PORT <port name>

DT0130-02 Check whether enable signal has connected with an external port.

When CEN terminal has connected with an external port, the pattern for a test is added to enable signal but racing happens from a timing problem.

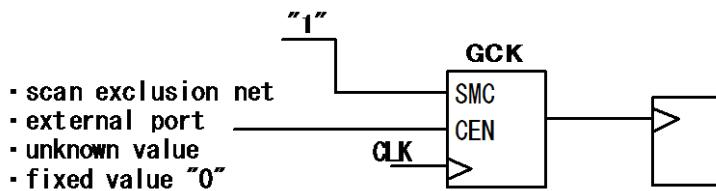
DFT0130-03 Check whether enable signal fixes Low.

When CEN terminal of a gated clock cell is fixed “Low”, F/F controlling in this gated clock does not work at capture mode.

But it is not checked when scan F/F does not connect with the output of a gated clock cell.

DFT0130-04 Check whether SMC signal fixes High. (The connection cannot change to SCAN_ENABLE)

When SMC terminal of a gated clock cell is fixed “High”, the logic to pass CEN terminal is not detected at capture mode. But SMC terminal cannot connect to SCAN_ENABLE in this case.



DFT0130-05 Check whether SMC signal fixes High. (The connection can change to SCAN_ENABLE)

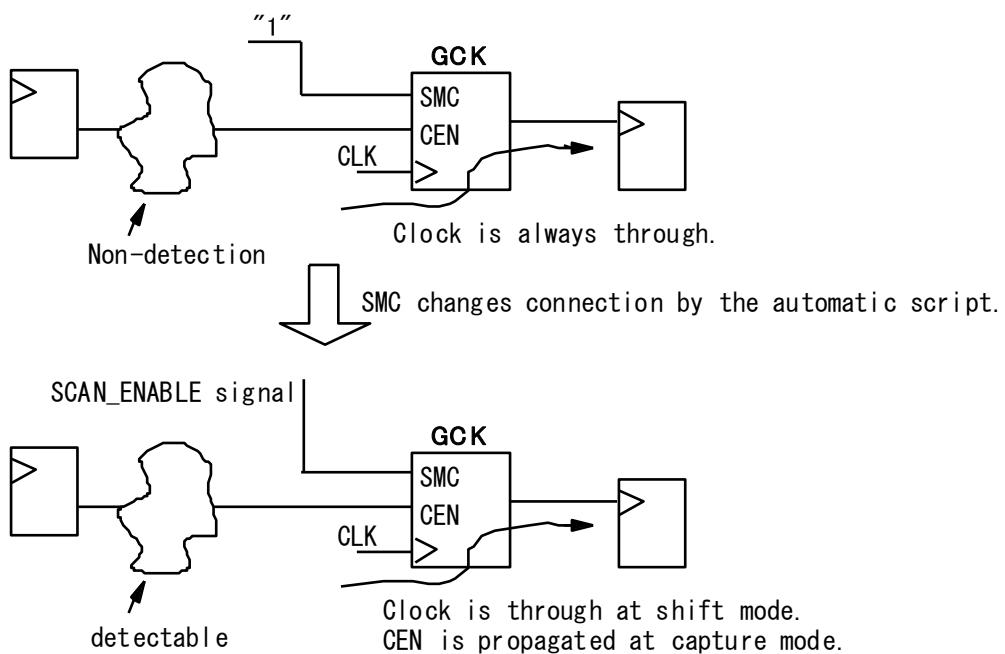
When SMC terminal of a gated clock cell is fixed “High”, the logic to pass CEN terminal is not detected at capture mode.

If SCAN_ENABLE signal was connected, clock is supplied at the shift mode (SMC=1), and it decides whether clock is output by a state of CEN terminal at the capture mode (SMC=0). Presence of trouble to propagate in CEN terminal by this is tested.

The tool generates two kinds of scripts to change connection of SMC to SCAN_ENABLE signal.

- Script for NetEdit (File name is DFT013_5_netedit.f)
- Script for SINGEN (File name is DFT013_5_SINGEN_profile.f)

Please inflect with the case leading a big rate of detection fall.



<< Revision procedure by NetEdit >>

Step1 <DFTcheck execution>

Step2 <Revision of DFT013_5_netedit.f>

Please set the scan enable signal to scanen variable about all clocks included in SCAN EN list.

```
set_delimiter . ;
set scanen_clockname xxxx ;
cut A2 SMC ; set rc [pin2pin_connect $scanen_CLK_A {A2.SMC} ]; puts "pin2pin_connect A2.SMC=$rc"
#####
SCAN EN list start #####
# scanen_CLK_A
print_verilog_source out.v ;
```



```
set_delimiter . ;
set scanen_CLKA LSITOP.scan_en ;
cut A2 SMC ; set rc [pin2pin_connect $scanen_CLK_A {A2.SMC} ]; puts "pin2pin_connect A2.SMC=$rc" ;
print_verilog_source out.v ;
```

Step3 <NetEdit execution>

```
%NetEdit ¥
-RENEW ¥
test1.v ¥
-TCL DFT013_5_netedit.tcl ¥
-NWCELL ..//common_lib/CELL_def ¥
-TOP LSI ¥
-WORK work_Err
```

<< The explanation of the NetEdit function >>

Please refer to NetEdit user guide for the details.

Function specifications of create_gate_and_connect

Name	pin2pin_connect
Format	pin2pin_connect port1 port2 [-port port3] [-cut]
Function	[Connects ports between 2 points] Connects port1 and port2. -cut:Creates a new connection by cutting the existing net, when net is already connected. By default, existing net is connected as it is.
return	0 : success 1 : failure

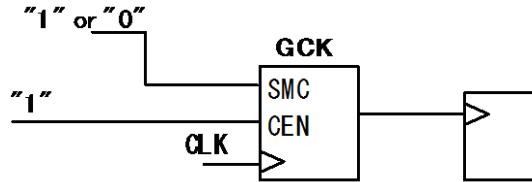
<< DFT013_5_SINGEN_profile.f >>

SINGEN script to reconnect is created.

```
Delete_Signal(cell) {
    instancename : A2 ;
    portname : SMC ;
}
Addsignal(cell) {
    instancename : A2 ;
    signame : ( SMC , %SEN_clk1G? ) ;
}
```

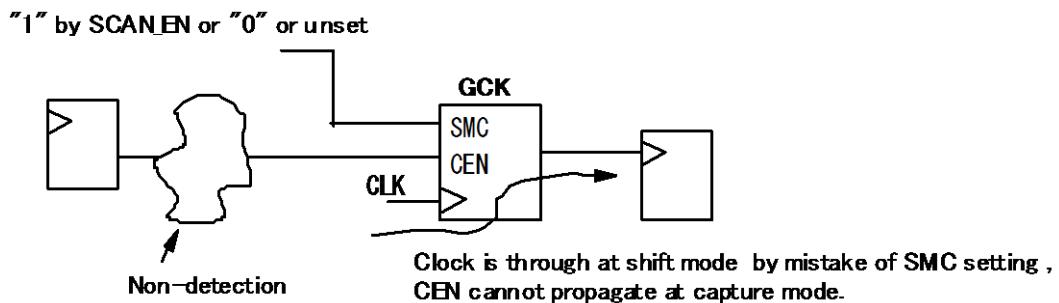
DFT013-06 Check whether enable signal fixes High.

When CEN terminal of a gated clock cell is fixed "High", clock becomes the through state regardless of SMC.



DFT013-07 Check whether SMC signal fixes High or does not fix Low by SCAN_EN.

When SMC terminal of a gated clock cell is fixed "High" or it is not fixed Low by SCAN_EN, the logic to pass CEN terminal is not detected.



DFT013-08 Check whether clock reaches the gated clock cell.

Because clock is unconnected, F/F controlling in this gated clock cell does not work.

** When clock reached the gated clock cell, the following diagram is checked. **

DFT013 (capture mode)		SMC terminal		
		Fixed to 0 by SCAN_EN	Fixed to 1	Fixed to 1 by SCAN_EN or Fixed to 0 or unset
CEN terminal	Unknown propagation	ERROR (DFT013-01)	ERROR (DFT013-04)	ERROR (DFT013-07)
	Connected to external port	ERROR (DFT013-02)		
	Fixed to 0	ERROR (DFT013-03)		
	Fixed to 1	WARNING (DFT013-06)		
	Others	-	WARNING (DFT013-05)	Note1) Fixed to 0 WARNING (DFT013-10)

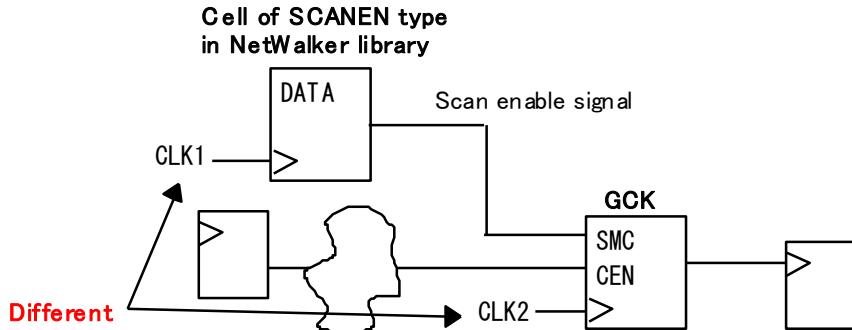
Note1) DFT013-10 check is executed by the following specification.

```
set_strings CHK_DFT013_10 yes;
```

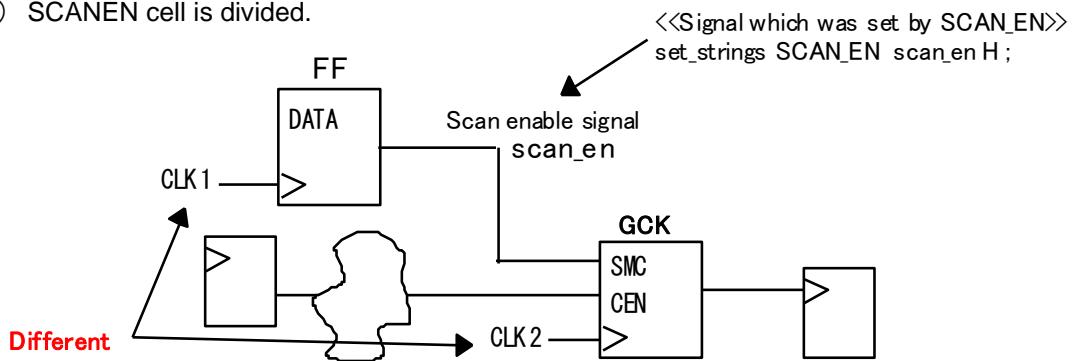
DFT013-09 Check whether clock is the same as clock generating SCAN_EN.

If clock is different, action at the time of shift and capture may be not correct.
(The GCK cell without errors in other DFT013 is checked.)

Example1)

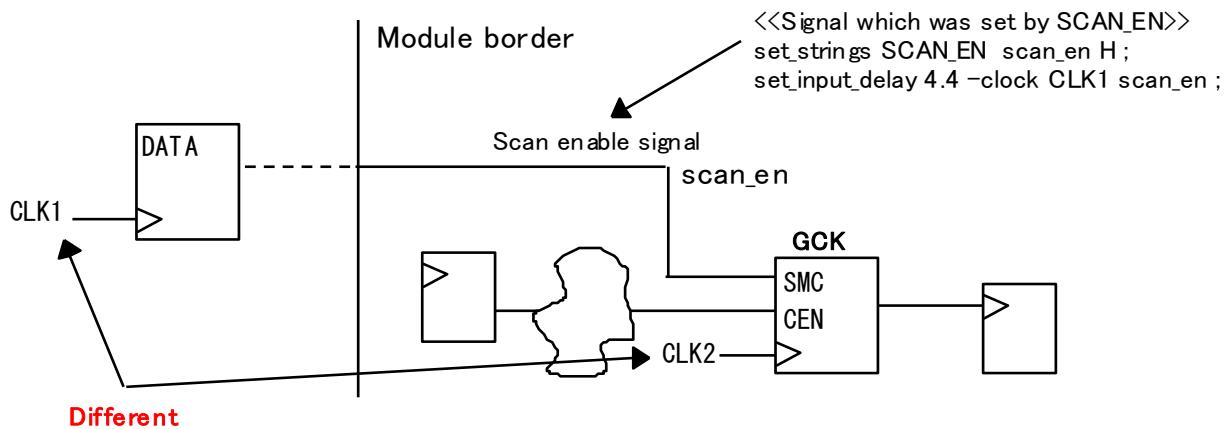


Example2) SCANEN cell is divided.



Example3) Execution of the module unit.

The clock definition of the input port by SCAN_EN and set_input_delay is necessary.



Note:

The following cases exclude the check by -CANCEL_013_09 option.

[Pre scan net] : before inserting ScanEnable generation circuit

[Post scan net] : when AC-SCAN is executed only by Broadside method

DFT013-10 Check whether SMC signal fixes Low. (The connection can change to SCAN_ENABLE)

When SMC terminal of a gated clock cell is fixed “Low”, tests are not considered because the movement is normal mode.

This case is error in DFT013-7. However, check is executed by specification of the following, the automatic connection script of the scan enable signal is created.

```
set_strings CHK_DFT013_10 yes ;
```

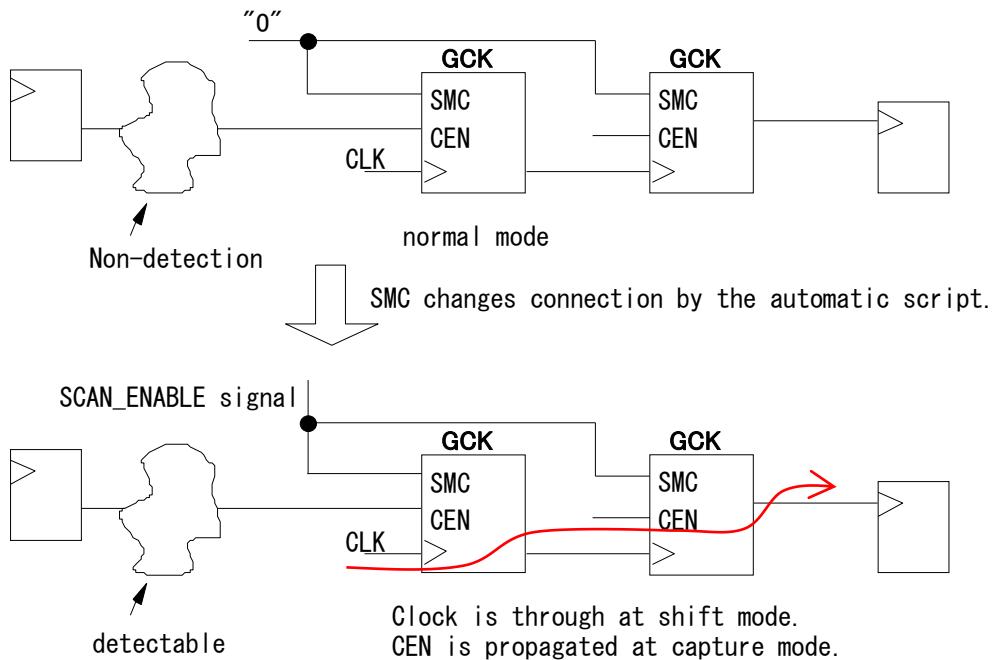
If SCAN_ENABLE signal was connected, clock is supplied at the shift mode (SMC=1), and it decides whether clock is output by a state of CEN terminal at the capture mode (SMC=0). Presence of trouble to propagate in CEN terminal by this is tested.

The tool generates two kinds of scripts to change connection of SMC to SCAN_ENABLE signal.

- Script for NetEdit (File name is DFT013_5_netedit.f)
- Script for SINGEN (File name is DFT013_5_SINGEN_profile.f)

Please inflect with the case leading a big rate of detection fall.

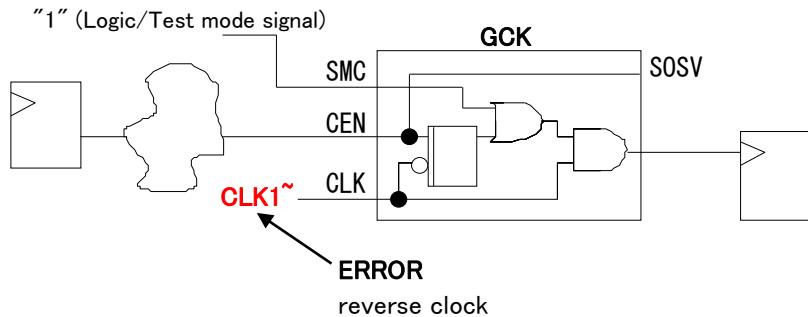
But the Low fixation with the test mode signal is not checked. And it is error of DFT013-7.
In addition, the check is excluded when the output terminal does not connect to F/F.



DFT013-12 GCK clock was reverse.

When -CHECK_013_12 is specified, this check is executed.

Because the reverse clock cannot execute AC test in SHINGEN, DC test is executed about output GCK.



DFT013-13 GCK exists behind MUX switching the clock. (At the time of LCSC use)

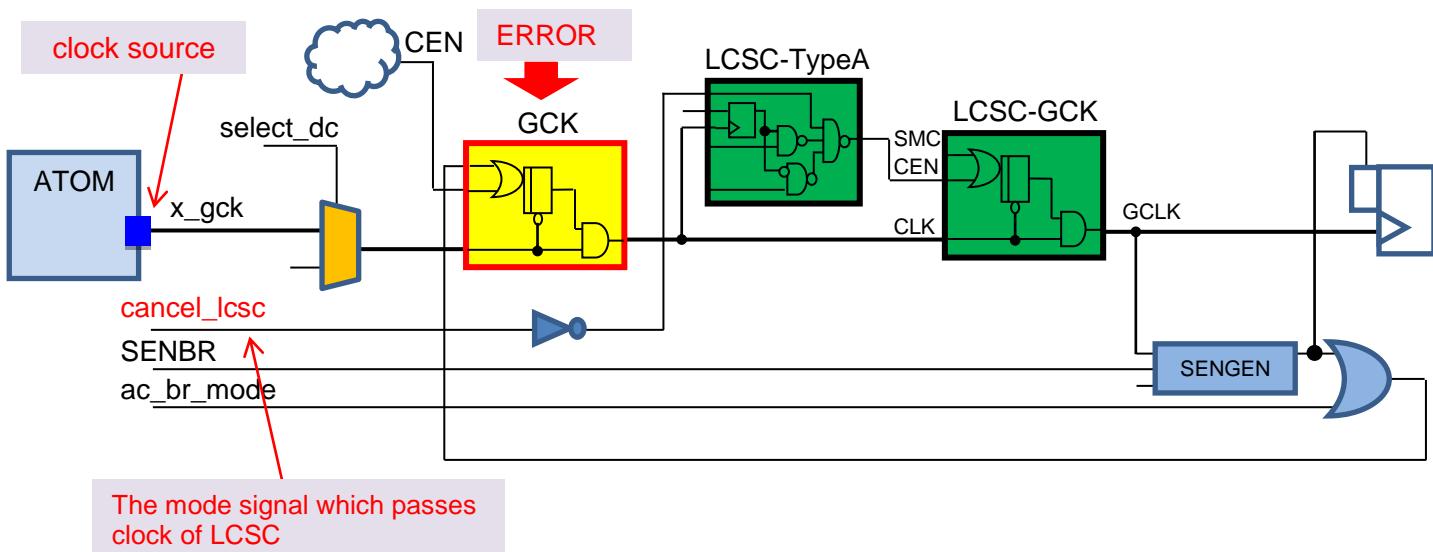
<<Check mode >>

PRE mode (specify -LBIST or -MUXSCAN or SINGEN) / POST mode (specify -POST)

When GCK cell exists behind MUX which is switched by select_dc signal on the clock line using LCSC, GCK which the mode signal does not propagate is detected as error.

The following designation is necessary.

set_strings Cancel_Icsc	cancel_icsc 1 ;
set_strings SELECT_DC	select_dc 1 tt_tr ;
set_strings SCAN_EN	SENBR 1 ;

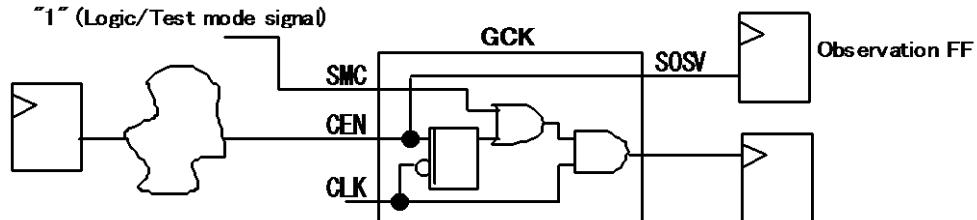


< DC test >

SMC terminal is fixed to High at test mode. For the trouble detection to CEN terminal, connection of the observation FF is necessary.

Please specify the following for DC test.

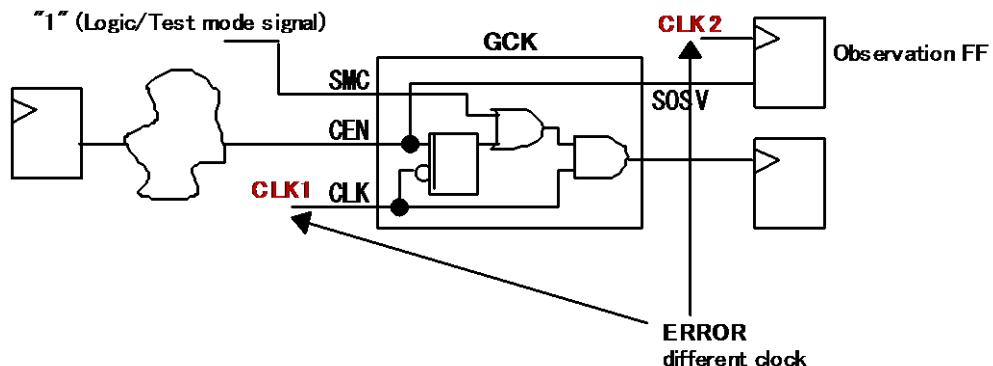
set_strings DC_TEST_MODE yes ;



DFT013 (capture mode)			SMC terminal	
CEN terminal	Unknown propagation Connected to external port Fixed to 0		Fixed to 1	Fixed to 1 by SCAN_EN or Fixed to 0 or unset
	Fixed to 1		WARNING (DFT013-06)	ERROR (DFT013-07)
	Others	No observation FF	WARNING (DFT013-05)	
		observation FF	same clock	
			-	
			different clock	ERROR (DFT013-11)

DFT013-11 Check whether clock of the observation FF is different from GCK clock.

The clock of the observation FF should be the same as the clock of GCK.



<The case which the test pin of the gated clock circuit connects to test terminal with DFT tool>

If the test pin of the gated clock circuit does not connect to test terminal at MUXSCAN, it is error. When there is the premise that the test pin of the gated clock circuit is connected to the test terminal in DFT tool, this error can exclude.

[DFTadvisor]

set scan enable <scan enable terminal name>: Connects to scan enable terminal.

setup scan insertion -ten <test mode terminal name>: Connects to test mode terminal.

setup clock gating <gated clock circuit>: -port_to_connect <pin name>

-driver <scan enable terminal name | test mode terminal name>

<gated clock circuit>: Specify cell name or instance name used in gated clock circuit, or module name of gated clock circuit.

-library <cell name> | -instance <instance name> | -module <module name>

[DFTcheck]

connect_direct -gate <instance name> | -cell <cell name> | -type <type name>

-pin <pin name> -driver <scan enable terminal name | test mode terminal name>

set_strings SCAN_EN <scan enable terminal name> <value>: Connects to scan enable terminal.

set_case_analysis [0 | 1] <test mode terminal name>: Connects to test mode terminal.

If there is not the terminal name specified by -driver, it is made automatically.

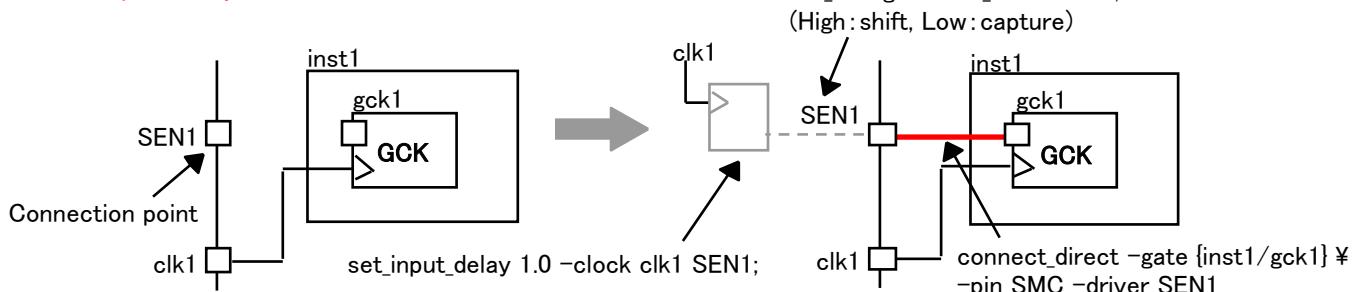
When there is not the connection of the specified terminal or it is fixed, it is connected. The connected terminal is not connected anymore. In addition, the instance of the module cannot specify.

Please refer to connect_direct for the details.

Example1) The test pin of the gated clock circuit is connected to scan enable terminal.

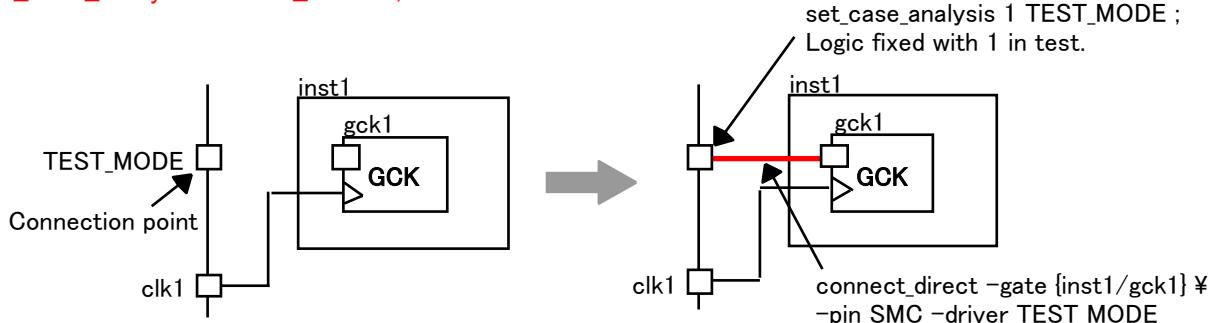
And add specification of SCAN enable for DFT013-1, and clock specification of SEN1 terminal for DFT013-9.

```
create_clock -name clk1 clk1
connect_direct -gate {inst1/gck1} -pin SMC -driver SEN1
set_strings SCAN_EN SEN1 1;
set_input_delay 1.0 -clock clk1 SEN1;
```



Example2) The test pin of the gated clock circuit is connected to the test mode terminal. And Logic is fixed.

```
create_clock -name clk1 clk1
connect_direct -gate {inst1/gck1} -pin SMC -driver TEST_MODE;
set_case_analysis 1 TEST_MODE ;
```

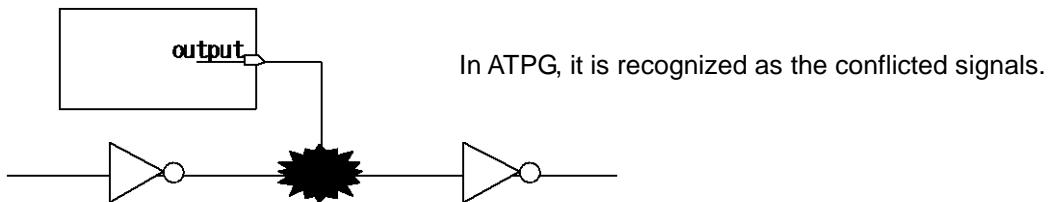


5.2.14 DFT014 Check for ATPG

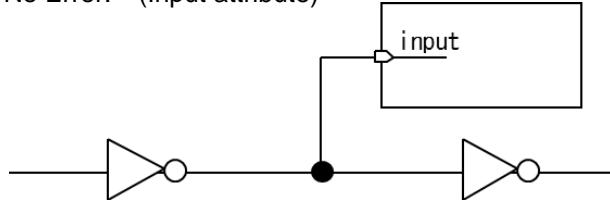
- Module output floating net check

On FastScan specification, the floating output ports of module are recognized as unknown signals, and need to specify the command at FastScan. Moreover, this circuit is easy to be created after PKS and ECO.

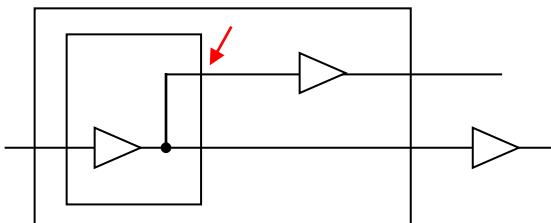
Error: (Output attribute)



No Error: (Input attribute)



Note: Like chart below, the output terminal of the module that a net diverges is pseud ERROR.



5.2.15 DFT015 Check of Fixed value

<<Check mode >>

PRE mode (default: specify -LBIST) / POST mode (specify -POST) /
PREMINORI mode (specify -PREMINORI) / POSTMINORII mode (specify -POSTMINORI)

DFT015-01 Logic fixation or port connection is necessary

For hard modules such as memory, check whether the logic of the necessary terminal of logic fixation or port connection is fixed with each mode.

The items which should be checked are mentioned in NetWalker library.

```
<NetWalker Library>
connect( term1 ( predft=L;           ← logic value at MUXSCAN or LBIST mode
            preminori=L;        ← logic value at MPREMINORI mode
            postminori=L;       ← logic value at POSTMINORI mode
            postdft=L;          ← logic value at POST mode
            );

```

In addition, when the fixed check of ROM/RAM terminal is not necessary at MUXSCAN or LBIST mode, please specify -CANCEL_015 at PRE mode. Check is excluded.

5.2.16 DFT017 Check of Bypass Clock

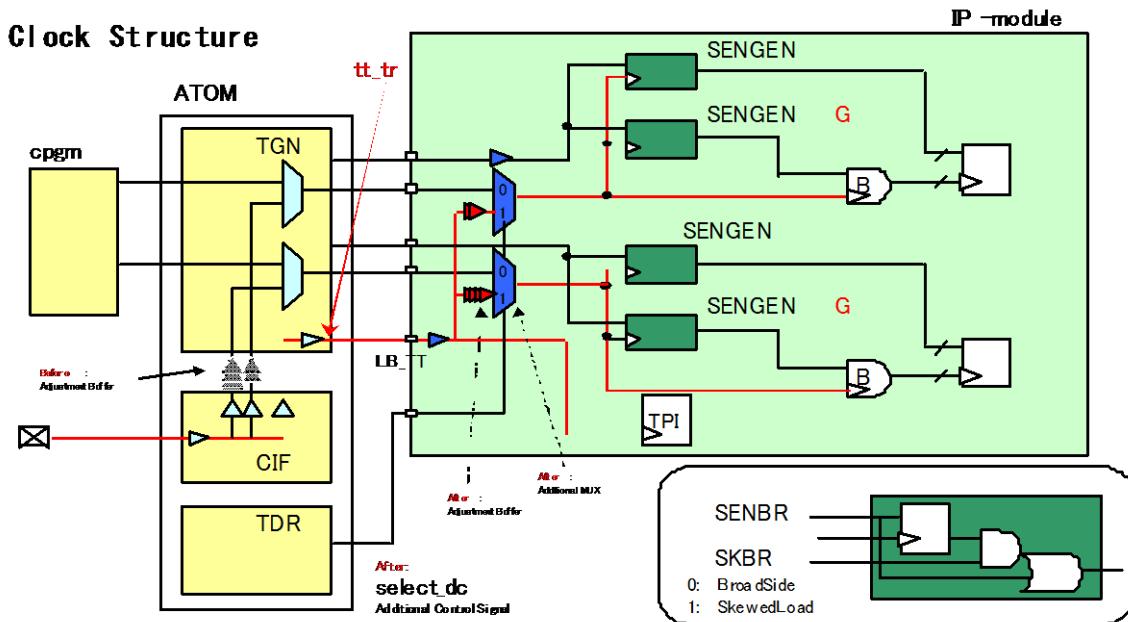
Execution mode is PRE (default/-LBIST), POST (-POST), PREMINORI (-PREMINORI), or POSTMINORI (-POSTMINORI). Specification of SELECT_DC is necessary.

Because cells for Hold measures on the test clock line are many, clock constitution such as the chart below is used. The test clock is connected directly at the time of the test. This composition is checked.

Specify the clock selection signal, the logic value to bypass and the clock which is chosen.

DFT017 is checked by specified value. The other checks are checked by the reverse value of specified value.

Example) set_strings SELECT_DC {ATOM/TDR/select_dc} 1 tt_tr ;



Note: The cell specified by set_strings DFT_CONTROL_REG is not output to SENG insertion script.

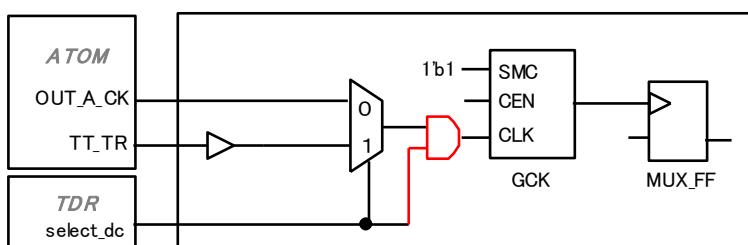
DFT017-0 Multiplexer does not exist.

The net specified by SELECT_DC does not connect with Multiplexer.

DFT017-1 Composition of clock is different from original.

Like chart below, when net (TDR/select_dc) specified by SELECT_DC is 0, original clock (OUT_A_CK) does not propagate to FF. But when TDR/select_dc is 1, test clock (TT_TR) propagates to FF. This case is error.

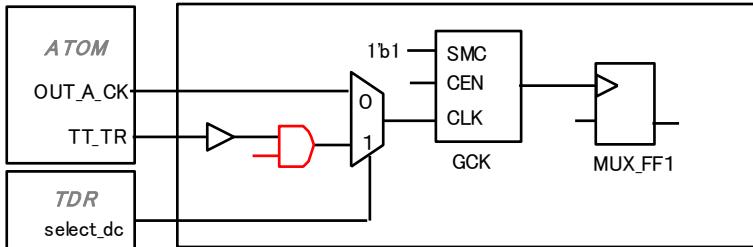
set_strings SELECT_DC {TDR/select_dc} 1 TT_TR ;



DFT017-2 Clock does not propagate.

Like chart below, when net (TDR/select_dc) specified by SELECT_DC is 0, original clock (OUT_A_CK) propagates to FF. But when TDR/select_dc is 1, test clock (TT_TR) does not propagate to FF. This case is error.

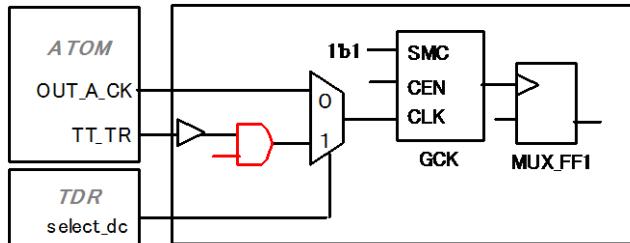
```
set_strings SELECT_DC {TDR/select_dc} 1 TT_TR ;
```



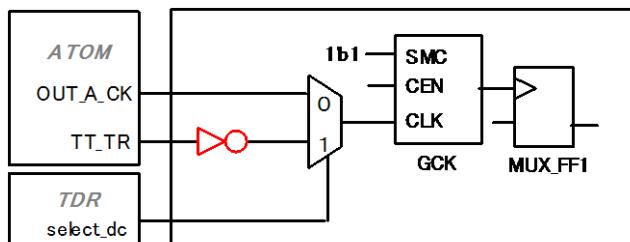
DFT017-3 Clock of the multiplexer inverts or does not propagate.

```
set_strings SELECT_DC {TDR/select_dc} 1 TT_TR ;
```

< Clock does not propagate >



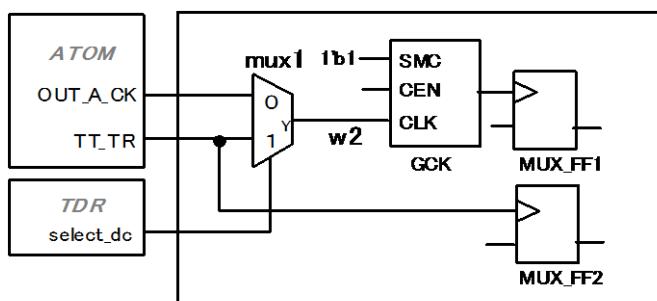
< Clock inverts >



DFT017-4 Clock information of the multiplexer

The clock information of the multiplexer without the error is output. And FF connected directly is output, too.

```
set_strings SELECT_DC {TDR/select_dc} 1 TT_TR ;
```



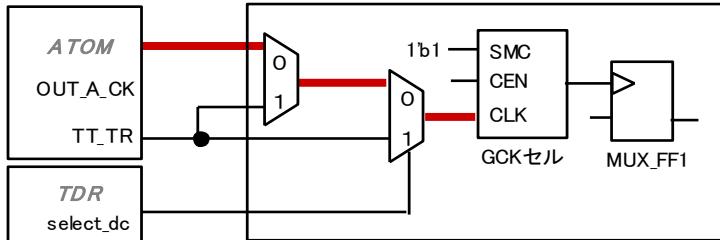
Example)

INFO DFT017 -4: MUX INFOMATION
No. Mux_InstancePin NetName Clock

1	mux1.Y	w2	OUT_A_CK
2	DIRECT_FF	TT_TR	

DFT017-5 Multiplexers are connected repeatedly on AC clock line.

```
set_strings SELECT_DC {TDR/select_dc} 1 TT_TR ;
```



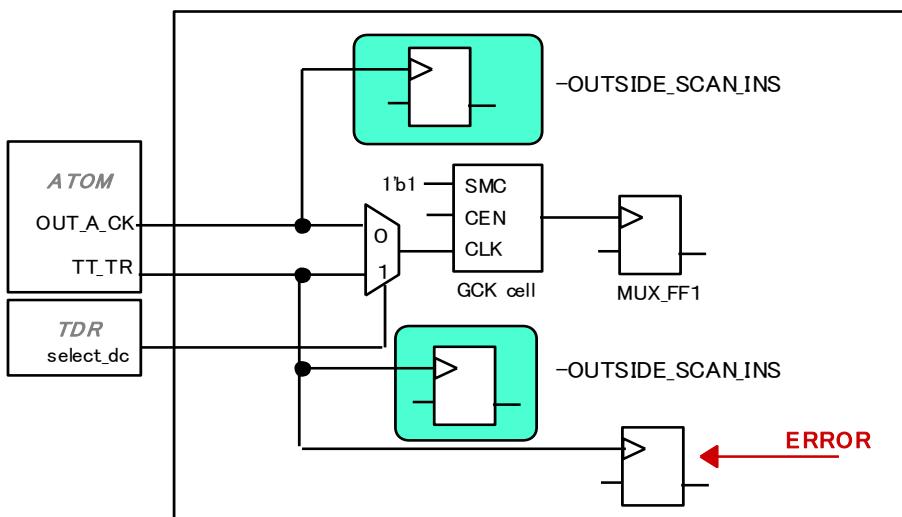
Example)

ERROR DFT017 -5: Muxs are duplicated
No. Instance Name(Cell) Instance Name(Cell)

1 mux1.Y > mux2.I0

DFT017-6 The register which AC clock controlled with SELECT_DC signal does not arrive at exists.

```
set_strings SELECT_DC {TDR/select_dc} 1 TT_TR ;
```



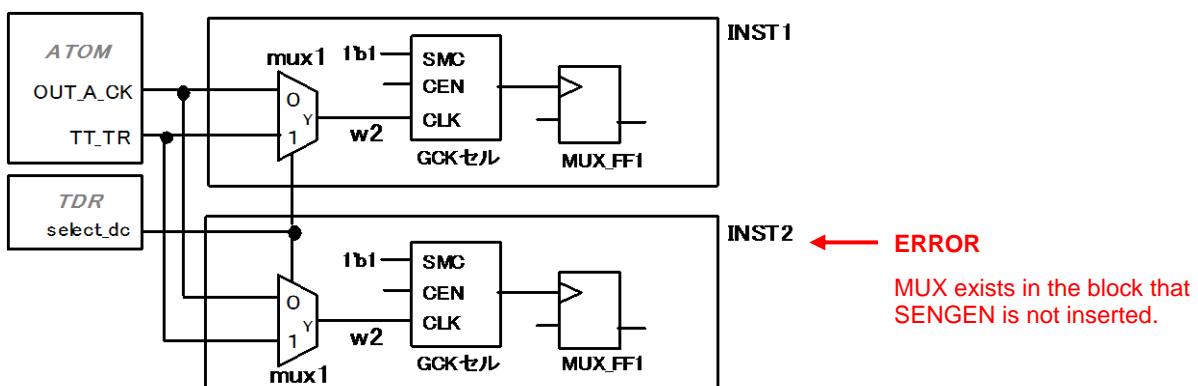
Automatic recognized TPI-FF is output to TPI-FF list and is not checked.

< Condition to recognize to be TPI-FF automatically >

- (1) MUX controlled by SELECT_DC on the DC clock line does not exist, and the output of FF that DC clock arrives is floating.
- (2) MUX controlled by SELECT_DC on the DC clock line does not exist, and the output of FF that DC clock arrives is divided by TPIEN signal.

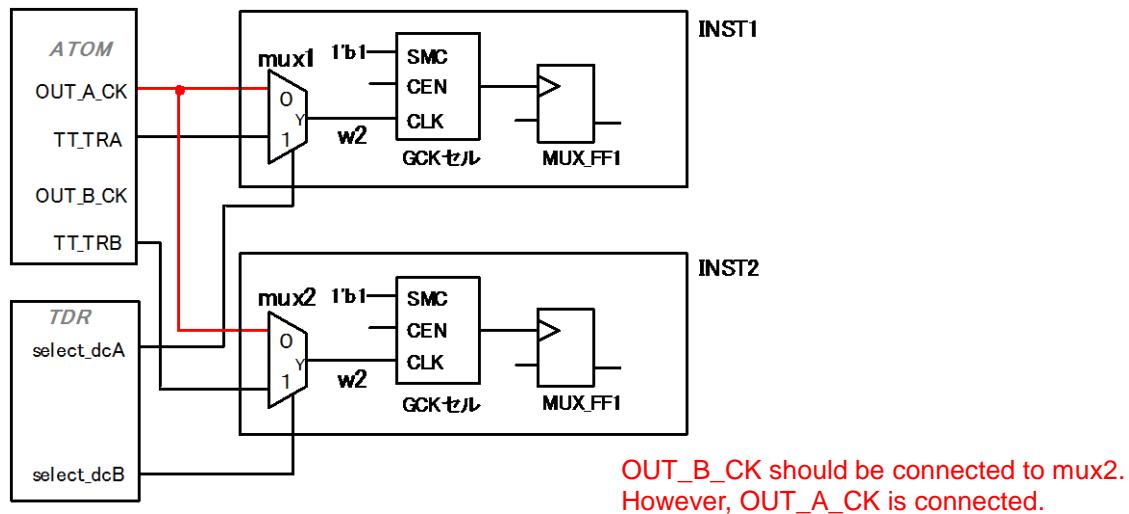
DFT017-7 Multiplexer which is not defined by ADD_SENGEN exists.

```
set_strings ADD_SENGEN INST1 ;
```



DFT017-8 User clock is connected to the multiplexer which controlled by different SELECT_DC signal.

Like the chart below, the user clock is not separated in the case that INST1 and INST2 are separated by SELECT_DC.



DFT017-9 Definition of SELECT_DC includes mistake.

When the definition has mistake as follows, error is detected.

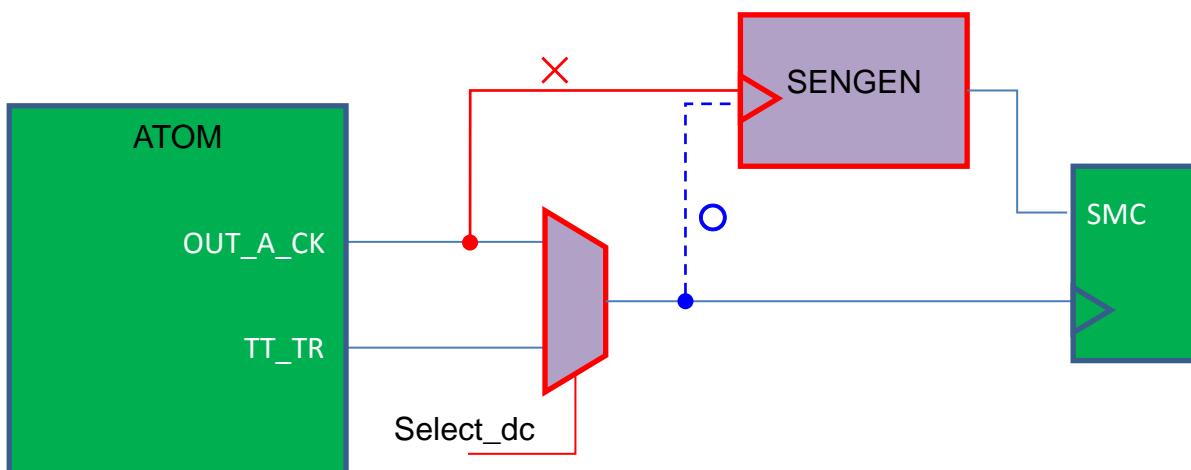
(1) The definition of same SELECT_DC signal is repeated.

```
set_strings SELECT_DC {TDR>Select_dc1} 1 TT_TR1;
set_strings SELECT_DC {TDR>Select_dc1} 1 TT_TR2;
```

(2) The definition of same test clock is repeated by different SELECT_DC signal.

```
set_strings SELECT_DC {TDR>Select_dc1} 1 TT_TR1;
set_strings SELECT_DC {TDR>Select_dc2} 1 TT_TR1;
```

DFT017-10 SENG is not controlled with the clock same as scan FF.



5.2.17 DFT018 Connection Check of ATOM SKBR pin and ScanEnable generation cell

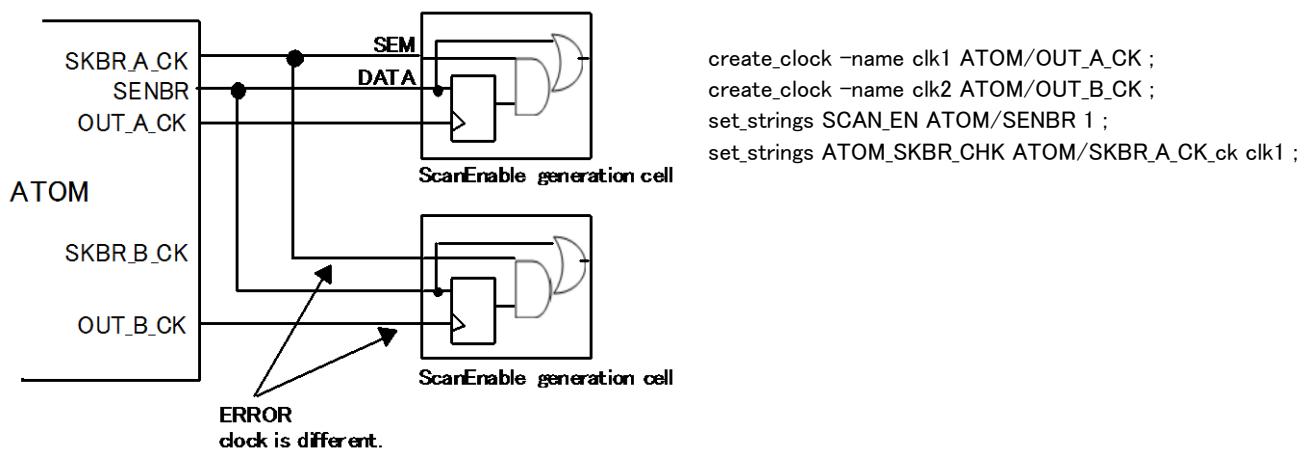
It is checked whether the connection of SKBR terminal and ScanEnable generation cell is AC test possible constitution. The SKBR terminal is a mode signal changing SkewedLoad and BroadSide on an AC test.

DFT018-1 Connection is different.

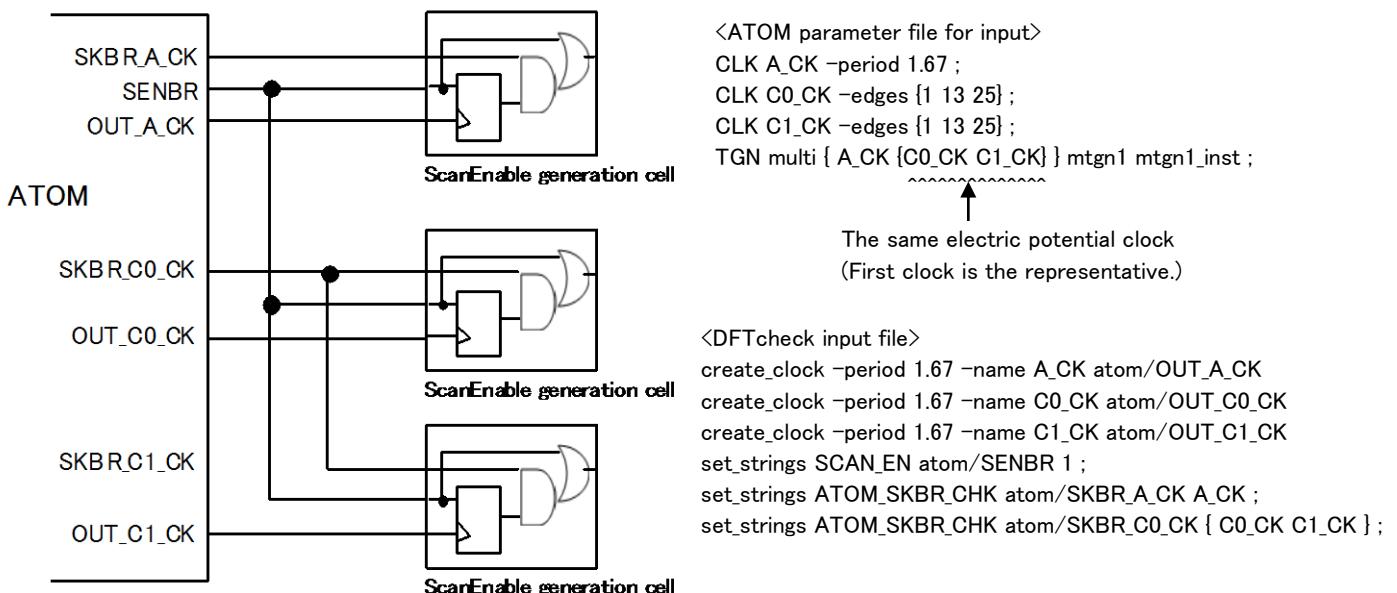
If clock controlling SKBR signal is different from ScanEnable generation cell, it is error. This check is executed by specification of the following,

```
set_strings ATOM_SKBR_CHK <signal name> <clock name list> ;
```

When there are multiple clocks, please surround those by the curly brace like {C0_CK C1_CK}.
When all clocks are target, please specify "ALL".



Example of the same electric potential clock)

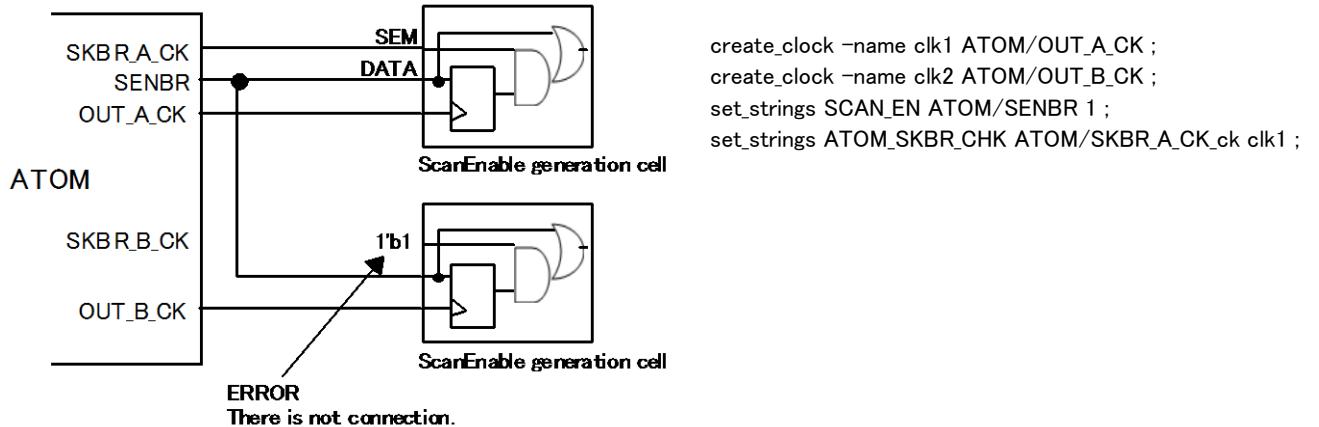


Note)

When the signal specified with set_strings ATOM_SKBR_CHK is not connected to ScanEnable cell, GCK cell, or register, it is error.

DFT018-2 SEM pin of ScanEnable cell does not have connection.

There is the ScanEnable cell which specified net and SEM terminal connect with nowhere in DFT018-1.



Note) If SENGEn cell is not used, please specify -CANCEL_018 to exclude check.
This does not execute on PREMINORI/POSTMINORI mode.

Note) If ScanEnable generation cell (SENGEn) is soft model, add the following to cell definition.

```
<Verilog-HDL of ScanEnable generation>
module sengen (data, clk, sem, q);
    input data, clk, sem ;
    output q ;
    :
endmodule
```

```
<NetWalker Library>
sengen {type=GATE,COMP,SCANEN;
    pin(clk=CK;sem=SEM;);
    posi(data->q; sem->q;};
}
```

Since the pin information is got from Verilog description, please do not exclude it.
The following specification is necessary as information.
Model type is SCANEN. Pin type is SEM.

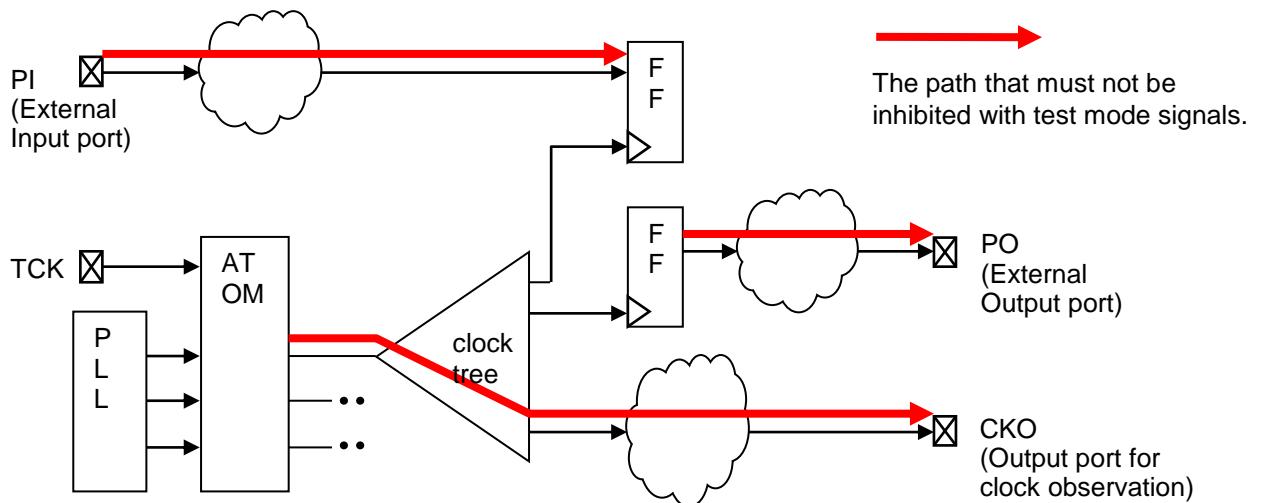
5.2.18 DFT019 IOAC SCAN Test Check

The IOAC scan test checks transition trouble between IO <-> FF by propagating transition to FF from the external input or transition to the external output from FF.

The pattern generation using the path delay trouble model generates the pattern by specifying the open path for the test.

At the time of the capture movement of the AC scan test, DFT019-2 is possible to control to validate the transfer of the open path. And it is checked the transfer of the open path is not obstructed with the test mode signal. When IN_IOAC_FILE was specified in MUXSCAN mode, this is checked.

Note: When BS is implemented by ATOM or R-TAPC deployment circuit, please set TK_INTEST signal to 0.



<< Format of IN_IOAC_FILE >>

```

PATH "<definition path name>" =
    PIN <instance name of the start point> <polarity> ;
    [PIN <instance name of the middle point> <polarity> ;]* 
    PIN <instance name of the end point> <polarity> ;
END :
  
```

<definition path name>: free name

<instance name of the start point> :

external input port name between FF from external input port, or
pin name of FF between external output port from FF

<instance name of the middle point>: (Omissible)

pin name between FF from external input port, or pin name of FF between external output port from FF

<instance name of the end point>:

pin name of FF between FF from external input port, or
external output port name between external output port from FF

<polarity>: + (posi)/ - (nega)

The sentence to begin in X is a comment line.

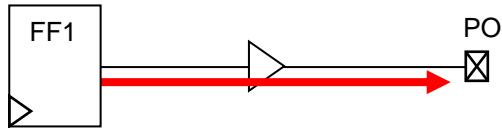
* Refer to "TsetKompress IOAC scan test guide" for the details of the IN_IOAC_FILE.

* Please prepare IN_IOAC_FILE every transfer timing.

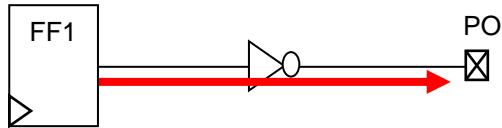
* DFTcheck ignores the middle instance name.

It is not considered whether a path going through the specified instance exists.

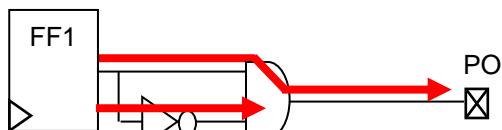
<< Example of IN_IOAC_FILE >>



```
PATH "path_1" =  
PIN /FF1/Q + ;  
PIN /PO + ;  
END ;
```

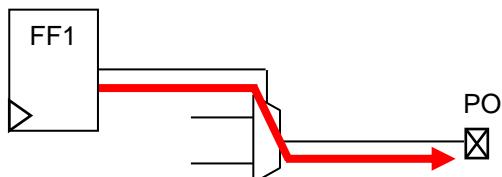


```
PATH "path_1" =  
PIN /FF1/Q + ;  
PIN /PO - ;  
END ;
```



```
PATH "path_1" =  
PIN /FF1/Q + ;  
PIN /PO + ;  
END ;  
PATH "path_1" =  
PIN /FF1/Q + ;  
PIN /PO - ;  
END ;
```

When the net diverges
and converges, define
all paths.



```
PATH "path_1" =  
PIN /FF1/Q + ;  
PIN /PO + ;  
END ;  
PATH "path_1" =  
PIN /FF1/Q + ;  
PIN /PO - ;  
END ;
```

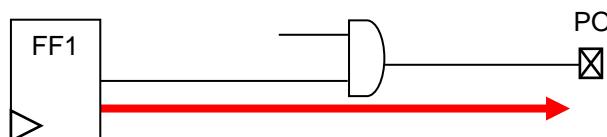
The path where the timing
arc is none supposes both
posi and nega, and define
those.

DFT019-2 Test target path does not exist.

When IN_IOAC_FILE is not specified, this is an error.

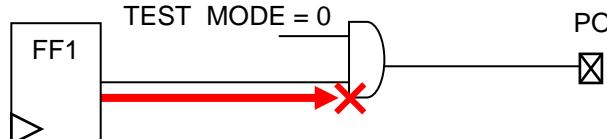
In addition, when the path specified in IN_IOAC_FILE does not exist, this is also an error.

Ex1) OK case



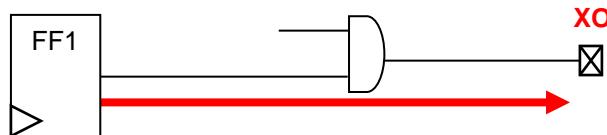
```
PATH "path_1" =
PIN /FF1/Q + ;
PIN /PO + ;
END ;
```

Ex2) ERROR case
(Cut off)



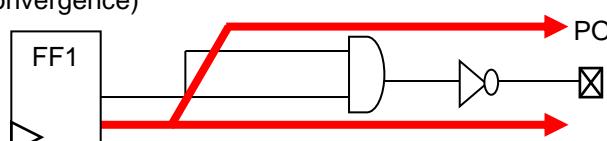
```
PATH "path_1" =
PIN /FF1/Q + ;
PIN /PO + ;
END ;
```

Ex3) ERROR case
(Non-arrival)



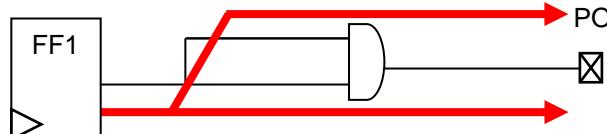
```
PATH "path_1" =
PIN /FF1/Q + ;
PIN /PO + ;
END ;
```

Ex4) OK case
(Divergence convergence)



```
PATH "path_1" =
PIN /FF1/Q + ;
PIN /PO - ;
END ;
```

Ex5) ERROR ケース
(nega path does not exist)



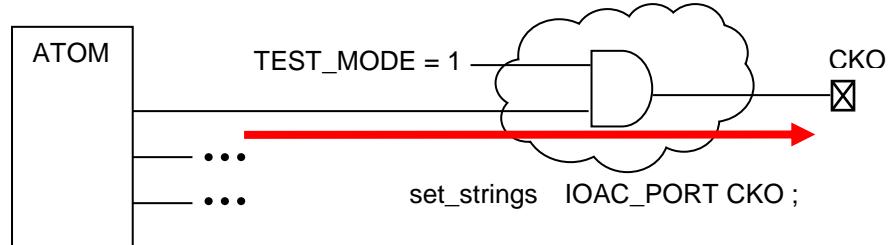
```
PATH "path_1" =
PIN /FF1/Q + ;
PIN /PO + ;
END ;
PATH "path_2" =
PIN /FF1/Q + ;
PIN /PO - ;
END ;
```

DFT019-3 Clock does not reach the output port for clock observation.

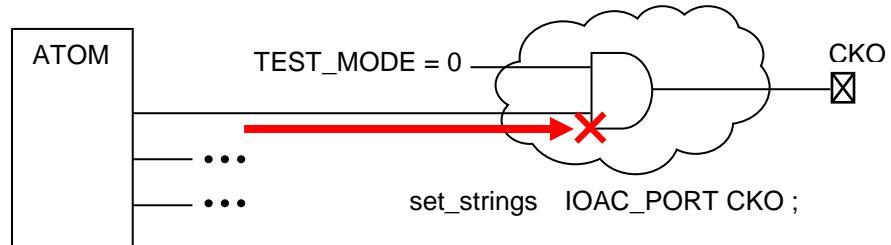
When the output port for clock observation is not specified, this is an error.

In addition, when the clock does not reach the output port for clock observation, this is also an error .
Specification of IOAC_PORT is necessary.

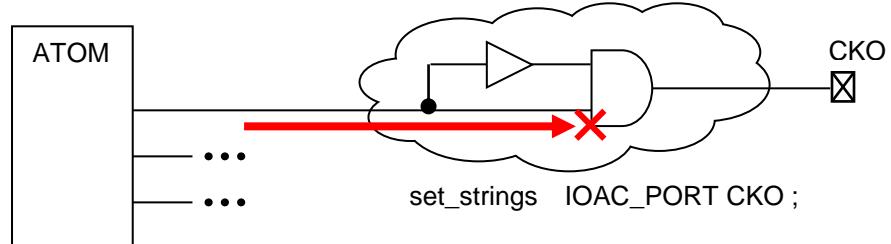
Ex1) OK case



Ex2) ERROR case
(Cut off)



Ex3) ERROR case
(Divergence convergence)



-OUT_IOAC_FILE option

This option outputs the candidate of the test target path.

When it is difficult to make IN_IOAC_FILE by hand, please use.

5.2.19 DFT020 FFR Check

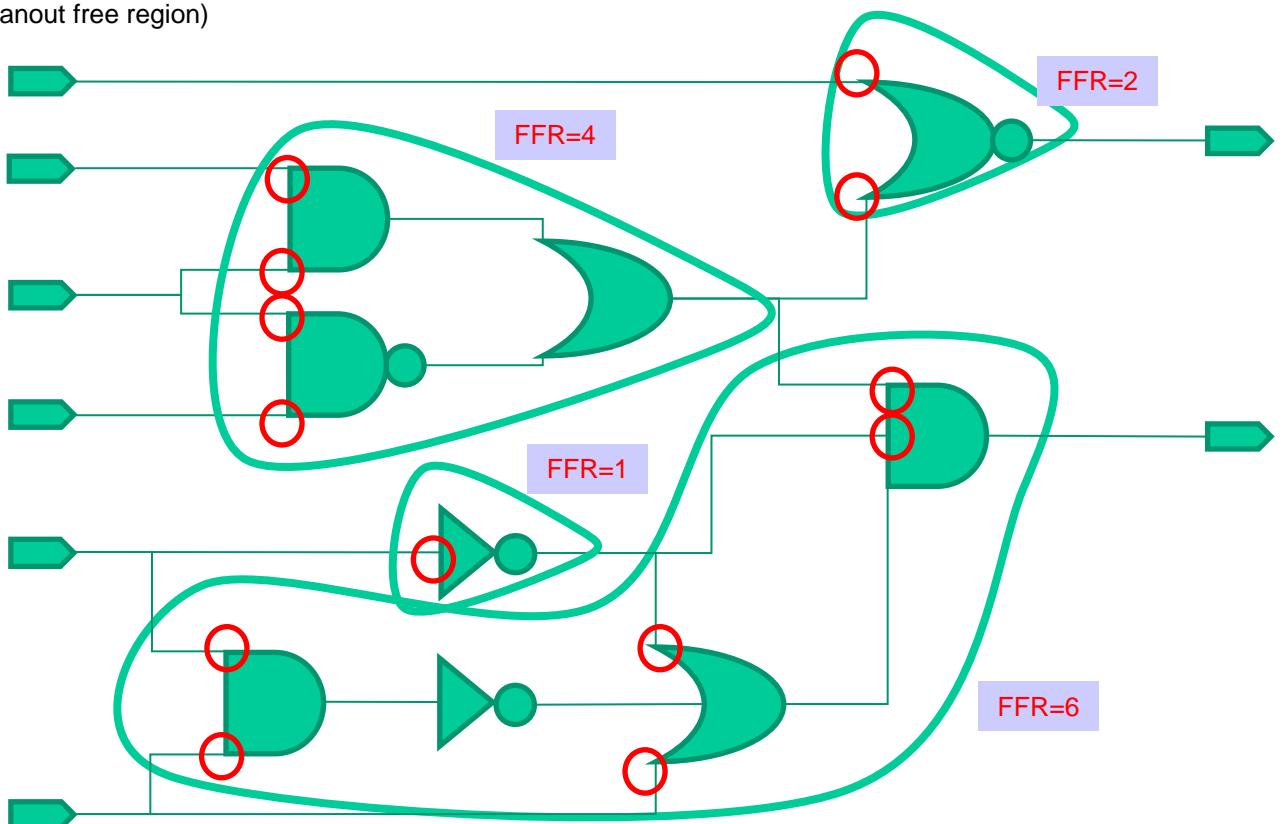
There was the product which exceeded memory capacity 64M pattern step of T6575. The number of the pattern steps of the scan pattern is about 82.3M (DC-SCAN:19.7M, AC-SCAN:62.6M).

The cause which the number of the patterns increased is the huge corn that the input pins of FFR (fanout free region) exceed 10,000. It is desirable to hold down the input pins of FFR to less than 2,000 not to increase the number of the patterns.

FFR that the input pins exceed 2000 becomes error. And the split point of FFR is output.

Note: This check is executed by -CHECK_020 option.

FFR(fanout free region)



<Method which get the split point>

If there is 5,000 FFR, for the equal division, it is calculated as follows.

$$5000 + 2000 - 1 / 2000 \rightarrow 3 \text{ splits}$$

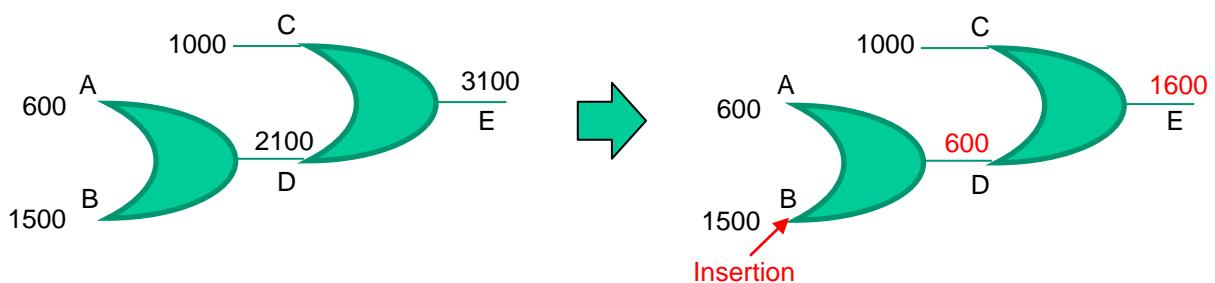
$$5000 / 3 \rightarrow 1666 \text{ (split upper limit)}$$

$$1666 * 50\% = 833 \text{ (split lower limit)}$$

The tool outputs the net which inserts observation F/F to the point that FFR exceed 1666.

Example)

Because FFR exceeds 1666 at D, A and B become the split points. However, A is excluded from the candidate because A does not exceed the split lower limit. As a result, B and E becomes the split candidate.



The limitation condition of FFR can change as follows. Default is 2000.

```
set_numerical_value limit_nFFR <value>;
```

In addition, a parameter value to decide a lower limit value can change as follows.

```
set_numerical_value Minimum_percentage <percentage(%): example 70>;
```

<Way of looking at the message>

ERROR DFT020 -1: There is a net beyond the limitation of FFR.

No. NetName InstancePin FFR_number(3) Split conditon(max:3 min:1)
Recommending_the_split_point NetName nFFR

1 h G7.Y 6

n nFFR(2) ← division candidate net and the number of FFR
o nFFR(3)

<< Result of recalculation : less than nFFR(3)>> ← <<Meaning of the message>>

2 k G5.Y 4

i nFFR(2)

<< Result of recalculation : less than nFFR(3)>>

limitation upper limit
split upper limit

split lower limit

Note: If FFR cannot split, "Can not div" appears.

<Automatic insertion method of observation F/F>

The net that observation F/F was inserted is outputted by the following specification.

```
set_strings OBSERVE_type ¥  
TH5KDFFAQXCU_fall @cell ¥ ←cell name  
DATA @data ¥ ←data pin name  
CLKB @clk ¥ ←clock pin name  
CLKP @port ¥ ←port name which is made when clock goes through module.  
clk @clk_net ¥ ←clock net name  
out.v.gz @out_file ←output file name
```

File name can change by set_strings OUTPUT_VERILOG_FILE.

But set_strings OBSERVE_type is given priority.

<naming rule>

The naming rule of the inserted gate instance is the following.

Observation F/F : <addition gate name>_ob_ff

If you change the naming rule, please specify it as follows. ob_ff changes to ob_ff1.

```
Example)set_strings PREFIX OBFF ob_ff1 ;
```

5.2.20 DFT021 Check of wrapper insertion sheet

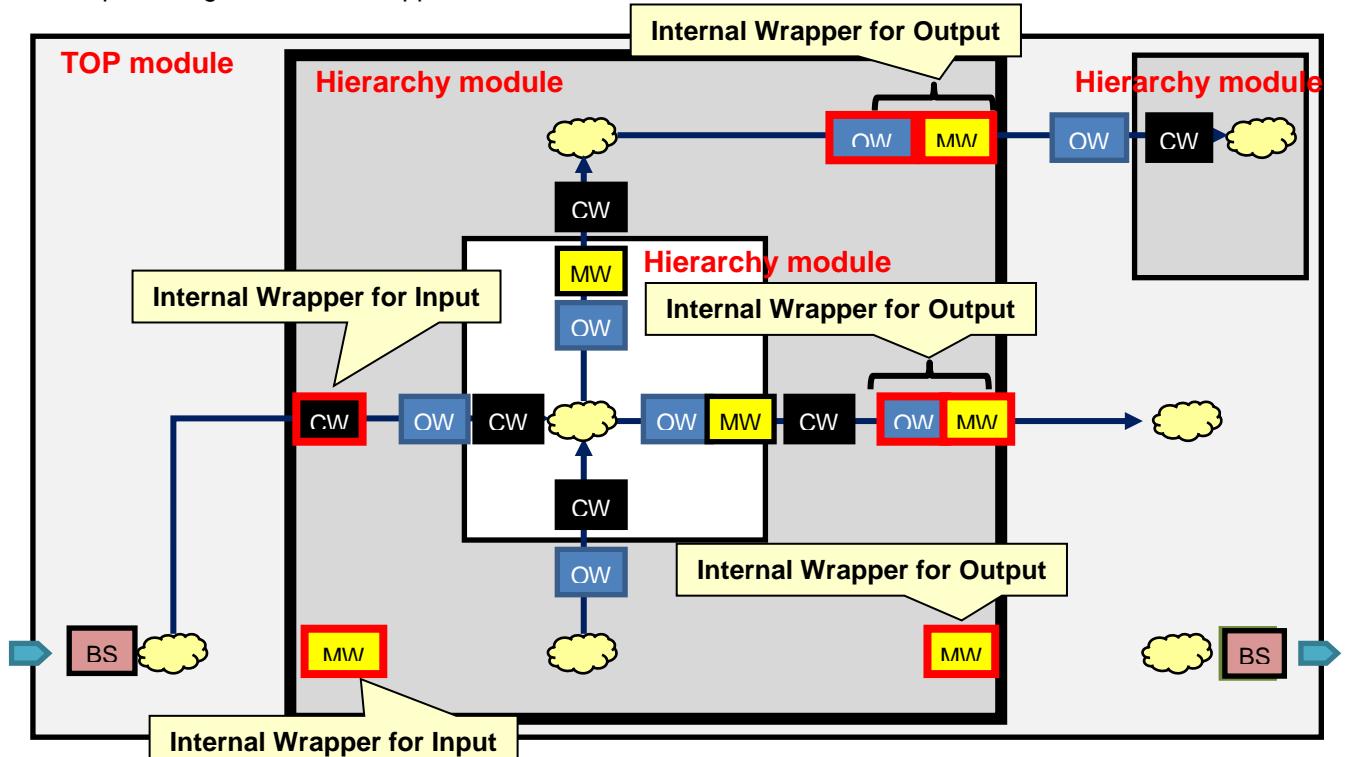
R-Car applies FieldBIST, and executes LBIST at every hierarchy module.

X must not propagate from the hierarchy module not to test. In order to prevent this, the logic (DFT wrapper) to mask the input signal of that hierarchy module is inserted.

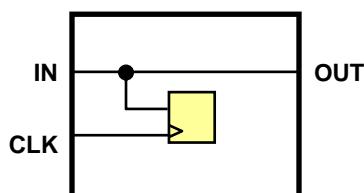
There is the case which the problem of X propagation is found by ATPG after DFT implementation. For example, it occurs for the reason such as the insertion specification omission of DFT wrapper.

DFT021 checks the defect of DFT wrapper specifications before DFT implementation. And DFT wrapper is implemented.

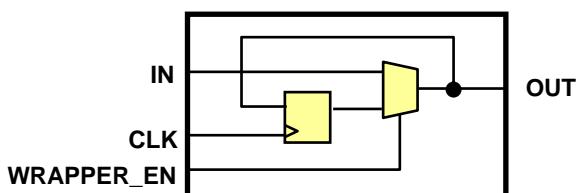
■ Conception diagram of DFT wrapper insertion



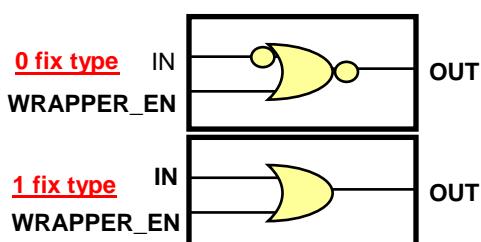
ow Observe Wrapper



cw Control Wrapper



MW Mask Wrapper



BS Boundary Scan Cell



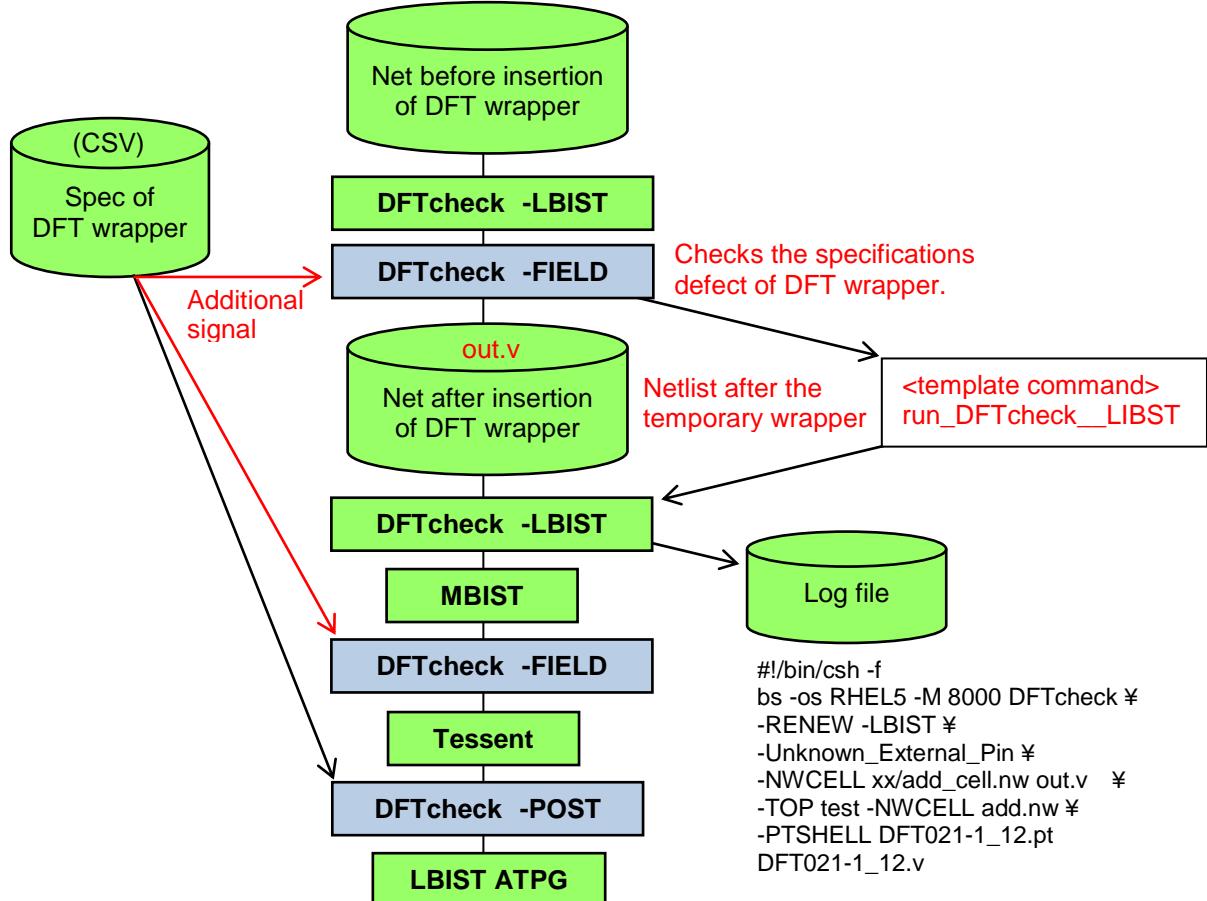
Boundary Scan Cell

■ Application flow of DFTcheck (-FIELD)

<Check Items>

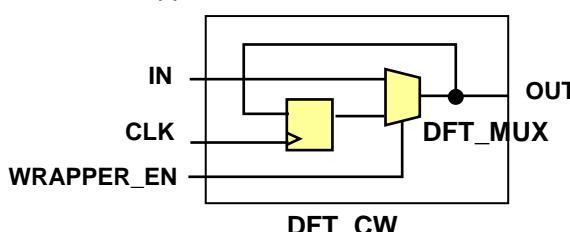
1. Checks whether the logic value of output pin is same as the value specified in CSV file.
2. Checks subject to X flowing from the port.
3. LBIST mode check on the condition that X is input from external port in a net after the wrapper insertion.

A net after the temporary wrapper insertion and the template command for the check are outputted from CSV file.

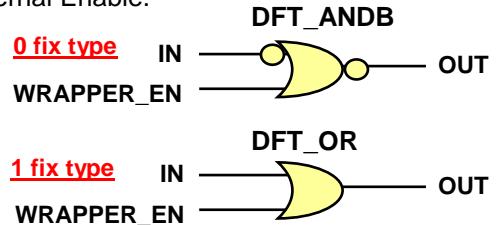


Control Wrapper: WRAPPER_EN is connected to Internal Enable. Because CLK is not specified, it is connected to TT_TR specified with create_clock.
`create_clock -name TT_TR atom/TT_TR`

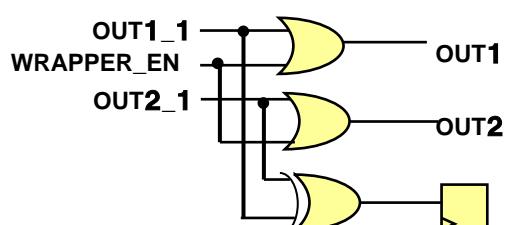
When there is the logic except inverter and buffer between the input port and register , Control Wrapper is inserted. It is not Mask Wrapper.



Mask Wrapper : DFT_ANDB/DFT_OR is distinguished with Stable Value. In addition, WRAPPER_EN is connected to Internal Enable.



Observe F/F :



■ Check Specification (-FIELD)

Mask for the module port connected to cell/module of SCAN attribute is necessary. Mask for the module port connected to clock/reset is prohibition.

Mask for the module input port connected to the unknown attribute of hardware macro is necessary. Mask for the module output port is prohibition.

The signal which was masked by set_case_analysis does not propagate.

In FIELD mode, the other rules are not checked.

<Input check >

(1-1) Mask prohibition signal (Signal which is connected with the following) DFT021-2

Exclusion circuit from scanning (Script:UTSIDE_SCAN_INS)

DFT control circuit (Script:FT_CONTROL_REG)

Power supply, reset, clock, pin of Scan-In

Analog pin (power supply name which has "I-" : Internal power supply)

Path to a port (via gates)

(1-2) Signal that a mask is necessary (Signal which is connected with the following) DFT021-1

D pin of scanning F/F (Attribute:UX_FF,AF_MUX_FF)

Scanning module (Attribute:FT,DFTMEM) (Script:LREADY_SCAN_MODULE)

ROM pin (TM,TRB[0],TRB[1],RTSEL[0],RTSEL[1],PTSEL[0],PTSEL[1])

RS pin, Unknown hardware macro (Attribute:ODULE)

The signal which is not connected to a gate and a register has mask specification.

<Output check>

(2-1) Mask prohibition signal DFT021-2

Signal which is connected to the exclusion circuit from scanning (Script:UTSIDE_SCAN_INS) on the inside
Signal which is connected to DFT control circuit (Script:FT_CONTROL_REG) on the inside

Signal which is connected to analog pin on the inside

Signal that was specified as reset/clock on the inside

Signal which is connected to Scan-Out on the inside

Signal which is connected to the unknown hardware macro (Attribute:ODULE), (except RSO)

Path to a input (via gates)

Signal which is connected to reset/clock on the outside (batch execution of the chip)

(2-2) Signal that a mask is necessary DFT021-1

Signal which is connected to RSO on the inside

Signal which is connected to cell / module of SCAN attribute on the inside

(Attribute:UX_FF,AF_MUX_FF,DFTMEM,DFT) (Script:LREADY_SCAN_MODULE)

■ Execution command (-FIELD)

```
#!/bin/csh -f
set path = (/common/appl/Renesas/OPENCAD/R2016.03/tools/netwalker/cozy/bin $path)
bs -M 64000 -os "SLES9 SLES10_0 REDHATE5_0 RHEL5"
DFTcheck ¥
-TOP IP1 ¥
-RENEW ¥
-FIELD ¥      ← option for DFT021 check
-TABLE IP1_LBIST.csv ¥
-TABLE IP1_FIELD_BIST.csv ¥    } ← CSV file to check wrapper insertion.
-NWCELL ../CELL_def ¥
-PTSHELL clock_fix.pt ¥
test.v
```

Note) -TABLE can specify two or more according to mode or module.

■ CSV file for Wrapper insertion (-TABLE)

(1) Module name key

Module name, test,

The second is a module name to check. In the case of IP, it is a top module.

(2) Port name key

The second and subsequent key can specify Direction, "Internal Wrapper", etc.

DFTcheck reads these two, and checks what number key these are. The information in the next line (signal) is got according to this order.

Example) Direction is 2nd, "Internal Wrapper" is 3rd.

```
Port name, Direction, "Internal Wrapper",A,B,
in1, input, N,N,N,
s1,  input, N,N,N,
clk1,input, N,N,N,
rs,  input, N,N,N,
```

(3) <Signal> key

These are from the next line of Port name to the end of file.

The first is a pin name. The bus specify as A[1:0].

Key corresponding to Direction is input/output/inout.

N means Wrapper prohibition. B is Mask Wrapper. Y is Control Wrapper.

■CSV file for the naming rule check (-TABLE)

The item which regular expression and Direction were equal to is checked.

Name Rule, ◇ Essential

Port name,Direction,"Internal Wrapper","Stable Value","Internal Enable" ◇ same as Wrapper insertion CSV
Regular expression of port name, inut/output, <omission>/Y/N/B, <omission>/0/1, <omission>/<signal name>,

< Regular expression >

1. The characters to use in regular expression:

. ^ \$ [] * + ? | ()

2. The kind of the meta-character

(2-1) 1 character that is good in anything: .

(2-2) The top and the last of the line: ^ \$

- As the character string from the top to the last is checked by always, this specification is unnecessary.

(2-3) The repetition of the same character: * + ?

"*" means "the repetition more than 0 characters of a character in front".

"+" means "the repetition more than 1 characters of a character in front".

"?" means "the repetition more than 1 characters of a character in front".

The repetition number "{m}" does not support.

(2-4) The continuation of characters that is good in anything: .*

(2-5) One of the designated characters: []

- If "^" was put in the top, it means "the character except the character following '^'".

(2-6) Grouping: ()

(2-7) Either character string: |

- Use it in the inside of grouping.

(2-8) The escape of the meta-character: \

- The meta-character can escape by putting backslash before the meta-character.

Example)

Name Rule,

Port name,Direction,"Internal Wrapper","Stable Value","Internal Enable",

in.*,input,B,1,s1,

o.*t.*,output,N,

s[12],input,N,

<Wrapper insertion CSV file>

Module name,test,

Instance name (full path),

Port name,Direction,"Internal Wrapper","Stable Value","Internal Enable",

in1,input,B,1,s1,

in2,input,B,0,s1,

in3,input,B,0,s1,

In4,input,B,0,s1,

s1,input,Y,0,s2,

s2,input,N,

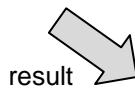
clk,input,N,

out1,output,Y,0,s1,

out2,output,Y,1,s1,

out3,output,B,1,s1,

clk_out,output,N,



ERROR DFT021-8 : Unmatch the Name Rule. (test)
No. Name_Rule Port_name different item

1 in.* input in2 stable (0 vs 1)

2 in.* input in3 stable (0 vs 1)

3 in.* input in4 stable (0 vs 1)

4 s[12] input s1 internal (Y vs N)

5 o.*t.* output out1 internal (Y vs N)

6 o.*t.* output out2 internal (Y vs N)

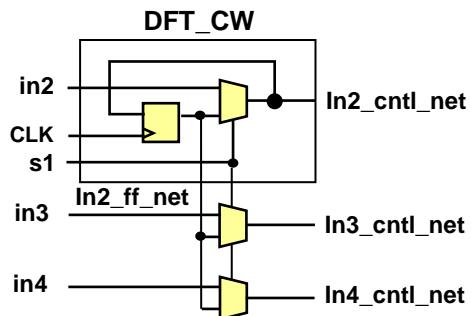
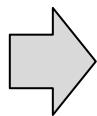
7 o.*t.* output out3 internal (B vs N)

<Example for Wrapper insertion CSV file>

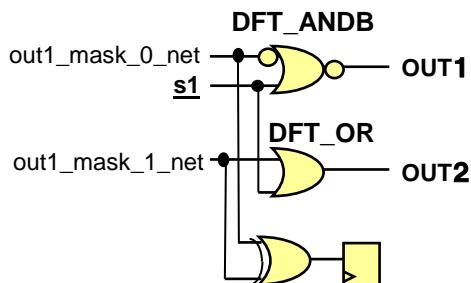
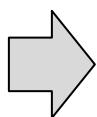
Port name,	Direction,	"Internal Wrapper",	"Stable Value",	"Internal Enable ",	Group,	Number,
in1,	input,	Y,	1,	WRAPPER_EN,	,	,
in2,	input,	Y,	0,	WRAPPER_EN,	,	,
s2,	input,	N,	,	,	,	,

Port name Port name
Direction Attribute (input/output)
Internal Wrapper Wrapper type In input (Y,:CW B:MW ,N: no Wrapper) In output (Y,:Observation F/F 付 MW B:MW ,N: no Wrapper)
Stable Value Fixed value (Only MW)
Internal Enable Enable signal name of Wrapper
Group Group name to summarize CW In input (F/F of CW is grouped.) In output (Y,:Observation F/F is grouped in eor.)

Example) input
 in2,input,Y,0,s1,G1,,
 in3,input,Y,0,s1,G1,,
 in4,input,Y,0,s1,G1,,



Example) output
 out1,output,Y,0,s1,G2,,
 out2,output,Y,1,s1,G2,,

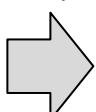


Number Specification of the processing
 Wrapper circuit is inserted for port which was specified with
 DFT021_insert. Default is for all ports.

Example) set_strings DFT021_insert a 2 3 ;

out1,output,Y,0,s1,,1,
 out2,output,Y,1,s1,,2,
 out3,output,Y,1,s1,,3,
 out4,output,Y,1,s1,,4,
 out5,output,Y,1,s1,,a,
 out6,output,Y,1,s1,,b,

Choice of the port to insert



out2,output,Y,1,s1,,2,
 out3,output,Y,1,s1,,3,
 out5,output,Y,1,s1,,a,

Output of Verilog file after the Wrapper insertion

If you output Verilog file, the definition of the Wrapper cell is necessary. The default is outputted with the temporary cell.

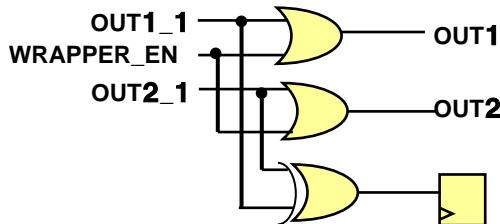
<Definition of Wrapper cell>

Specify the cell to insert as wrapper circuit in DFT021. Default is the temporary cell.

DFT_ANDB is defined with Wrapper_m0, and DFT_OR is Wrapper_m1.

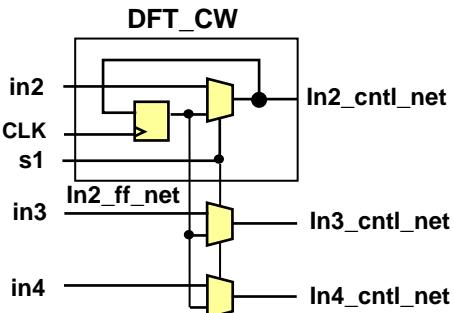


EOR that is necessary for observation F/F is defined with Wrapper_eor, and observation F/F is Wrapper_ob.



The selector in CW (control Wrapper) is defined with Wrapper_cw2.

The designated cell is used as the control Wrapper.
And DFT_CW module is produced automatically.



[Format] set_strings Wrapper_xx [<value> <key>]*

<Key>	<Meaning>
@cell	cell name
@th_in	input pin
@th_out	output pin
@en	enable pin
@ff	pin to connect to F/F of CW
@data	data pin of F/F
@clk	clock pin of F/F
@fix0	pin of 0 fixation
@fix1	pin of 1 fixation

Example)

```
set_strings Wrapper_m0 INR2D1BWP7T40P140UHVT @cell A1 @th_in B1 @en ZN @th_out
set_strings Wrapper_m1 OR2D0BWP7T40P140UHVT @cell A1 @th_in A2 @en Z @th_out
set_strings Wrapper_cw2 MUX2D0BWP7T40P140UHVT @cell I0 @th_in S @en Z @th_out I1 @ff
set_strings Wrapper_eor XOR2D1BWP7T40P140UHVT @cell A1 @th_in A2 @en Z @th_out
set_strings Wrapper_ob SDFQCK1LPD0BWP7T40P140UHVT @cell D @data CP @clk Q ¥
@th_out SI @fix0 SE @fix0
```

*The output file name can change with set_strings OUTPUT_VERILOG_FILE.

Method which change the clock connection of the Wrapper cell

The clock pin is connected by default to TT_TR specified with create_clock.
create_clock -name TT_TR atom/TT_TR

<change of Control Wrapper>

When you are connected to the signal of TCK, please add @clk_net. Other parameters are the same.

```
set_strings Wrapper_ob SDFQCK1LPD0BWP7T40P140UHVT @cell D @data CP @clk Q ¥  
@th_out SI @fix0 SE @fix0 TCK @clk_net
```

<change of observation F/F>

When you are connected to the signal of TCK, please add @clk_net.

```
set_strings Wrapper_cw DFT_CW @cell i @th_in en @en o @th_out ck @clk o2 @ff TCK @clk_net ;
```

<<Naming Rule>>

The naming rule of the inserted gate instance is the following.

Masked Wrapper (fixation 1)	:<port name>_mask_1
Masked Wrapper (fixation 0)	:<port name>_mask_0
Control Wrapper	:<port name>_ctrl
Observation F/F	:<port name>_ob_ff

If you change the naming rule, specify it as follows.

Example) set_strings PREFIX MW1 mask_1 ;

Masked Wrapper (fixation 1)	:MW1 (default is mask_1)
Masked Wrapper (fixation 0)	:MW0 (default is mask_0)
Control Wrapper	:CW (default is ctrl)
Observation F/F	:OBFF (default is ob_ff)

■ Way of looking at result (log)

```
^LLLogic design rule check /      NetWalker(V06.05.00) Wed Apr 1 13:57:51 2015
PAGE 0000
```

```
***** Summary of Linker *****
```

```
Total number of Logic Element list      51408230
```

```
Used Model Count      3357
```

```
1 assignbuf      16079      2 cdn_hs_phy_adr_slice      8
```

```
:  
3357 BRMT1BL1C0404AA0ZZ      1
```

```
LINK cpu time      total    cpu : 394.59s
                  user    cpu : 362.81s
                  system  cpu : 31.78s
                  memory size : 38980960kbyte
```

LinkageSummary

```
//RENESAS RULE CHECK -DFTcheck Version(V2.24)
```

```
<<< read before.csv >>>
```

```
Under Module u7795hrcah30hsc0->hsc
```

```
DFT_CONTROL_REG hsc_c4.mcg*
DFT_CONTROL_REG hsc_a3hsc.tcg*
DFT_CONTROL_REG hsc_a3hsc.tap*
```

Reading of CSV file
(Result of specified definition)

```
ERROR:Can not find (hsc_a3hsc.mcg*) at DFT_CONTROL_REG
```

```
Read csv end ... 14:14:10
```

```
0/2598 check masked signal(output) hsc.STP_PRDATADB[31] ...14:15:22
```

```
2597/2598 check masked signal(output) hsc.usbdm1_apresetst_cl_s3d2 ...14:15:22
```

```
*** End of DFT021 *** (14:15:22)
```

```
*** Summary of Error Code *** 14:15:22
```

```
No. Error_Code:message Number
```

```
WARNING      ERROR
```

```
-----  
1 "DFT021 :Field Bist Check
```

```
-          0      32
```

Check Summary

```
*** End of Summary ***
```

```
CHECK cpu time      total    cpu : 1047.73s
```

```
user    cpu : 1045.17s
```

```
system  cpu : 2.56s
```

```
memory size : 47111404kbyte
```

■ Way of looking at result (log.DFTcheck)

```
//RENESAS RULE CHECK -DFTcheck Version(V2.24)
//Generated at 15-03-26 11:39:56
```

Under Module u7795hrcah30hsc0->hsc

DFT_CONTROL_REG	hsc_c4.mcg*	}	← User definition
DFT_CONTROL_REG	hsc_a3hsc.tcg*		

ERROR:Can not find (hsc_a3hsc.mcg*) at DFT_CONTROL_REG ← User definition which has the problem

ERROR DFT021-1 : Propagating an unknown signal is not permitted. (u7795hrcah30hsc0)

No. Unknown-Signal	spread register: term	← Connection of the mask signal ("Y") is wrong.
--------------------	-----------------------	---

1 hsc.USB3_S0_REF_CLK_M (input)

↑ ↑

Pin name	Pin attribute
----------	---------------

-> hsc.hsc_a3hsc.us3phy0.us3phy.phy.REFPADCLKM (dwc_usb3_sspx1_hspx1_ns) [line 1:2068316] Others undefined pin

↑ ↑

Direction	Connecting Instance
-----------	---------------------

Reason (Refer error code)

ERROR DFT021-2 : Propagating an masked signal is not permitted. (u7795hrcah30hsc0)

No. Masked-Signal	spread register: term	← Connection of the mask prohibition signal ("N") is wrong.
-------------------	-----------------------	---

1 hsc.safe_grp_cond_us20_n[1] (input)

-> hsc.hsc_a3hsc.us2phy0.USB20IP.TESTCLK0 (dwc_usb20_phy_1p_ms_otg0_ns) [line 1:4087816] CLOCK

■ Error codes stack

PORT	Path to a port (via gates)
OSI	OUTSIDE_SCAN_INS is specified.
CONTROL_REG	DFT generation circuit is connecting.
SET_RES	Reset definition or set/reset pin is connecting.
CLCOK:<clock name>	Clock definition or clock pin is connecting.
analog	Analog pin (power supply name which has "I-")
SCAN-FF	Cell of Module with SCAN attribute
RS	RS pin
romtrimming	TM pin (, etc.) of ROM
SIN	Scan-in pin
SOUT	Scan-out pin
Others undefined pin	D, RS, reset, clock of unknown hardware macro Pin except romtrimming, SI, SO

<Information>

When Mask Wrapper is inserted to input, the number of the input pins of the gate becoming undetected from that effects is outputted.

When there is many it, please switch to Control Wrapper.

In addition, please consider the use of the merge function, if you are worried about the number of the registers of Control Wrapper.

<Automatic conversion from Control Wrapper to Masked Wrapper>

(CW→MW) : This means automatic conversion from Control Wrapper to Mask Wrapper

The conversion rule is the case which has only inverter and buffer in between port and registers.

Specify the following if you prohibit automatic conversion.

```
set_strings DFT021_cancel_cw2mw yes ;
```

Note: The input pin of the counted gate is not counted on the calculation of the next port.

INFO DFT021-2 : Can not detect input term number (test)

No. Masked-Signal number

1 in1 (CW->MW)	---	0
2 in2 (CW->MW)	---	1
3 in3	---	2
4 in4	---	1
5 s1 (CW->MW)	---	0

When wrapper where Mask observation F/F does not connect is inserted to output, the number of the input pins of the gate becoming undetected from that effects is reported.

<Automatic conversion from Control Wrapper to Masked Wrapper>

(CW→MW) : This means automatic conversion from Control Wrapper to Mask Wrapper

When inverters and buffers in between a port and registers are less than 8steps, the change rule is changed to MW. If you change steps to 10, set 10 in the following. And if you change it without a limit, please set 0.

```
set_numerical_value DFT021_gate_number 10 ;
```

In addition, please specify the following if you admit the gate which is not inverter or buffer.

```
set_strings DFT021_permit_gate yes ;
```

INFO DFT021-3 : Can not detect output term number (test)

No. Masked-Signal number

1 out3	---	2
--------	-----	---

■ Wrapper check (-POST)

In POST mode, the execution of module unit is necessary.

<<Check Specification>>

(1) Input port check

If CSV file was specified, DFTcheck judges as the module unit test.

The external port is the controllable signal on the chip top test. However, because X flows from the external port on the module unit test, this is checked.

Target Rule : DFT401-6

ERROR DFT401-6 : The register is connected non scan_chain_register at capture mode.

```
-----  
1 ff0.DATA (TH5KDFAAQBRBXC) [line 1:4]  
--- connected in1 [line 1:0] (Un-Control)
```

(2) Output port check

When the logic value of output is specified in CSV file, this checks whether the value is outputted.

Target Rule : DFT021-3

ERROR DFT021-3 : The specified mask signal(output) is not fixed. (test)

```
-----  
1 out2 (output) value(0) expect(1)  
2 SOUT (output) value(-1) expect(1)
```

■ Executing command(POST)

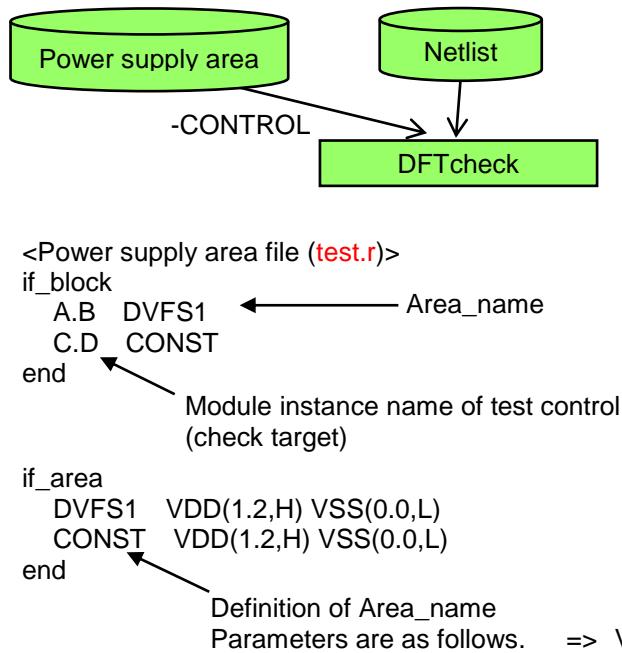
```
#!/bin/csh -f  
set path = (/common/appl/Renesas/OPENCAD/R2016.03/tools/netwalker/cozy/bin $path)  
bs -M 64000 -os "SLES9 SLES10_0 REDHATE5_0 RHEL5"  
DFTcheck -TOP IP1 ¥  
-RENEW ¥  
-POST ¥  
-TABLE IP1_LBIST.csv ¥ ← CSV file to check wrapper insertion.  
-NWCELL ..../CELL_def ¥  
-PTSHELL clock_fix.pt ¥ ← set_strings POST_DFT SIN SOUT  
-PTSHELL scan_info.pt ¥ ← set_strings SCAN_EN SMC 1  
test_post.v
```

5.2.21 DFT022 Check of Lockup latch

R-Car is adopting DFT circuit control circuit insertion and DVFS at every IP. The insertion of the lockup latch is necessary on the transfer of the DFT circuit control signal across the DVFS domain to prevent an omission of hold measures.

This checks whether the transfer using the lockup latch is correct.

The specification of the power supply area file is necessary.



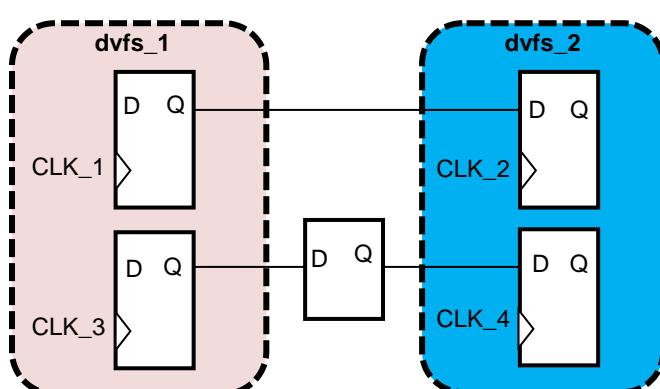
Only when **-CONTROL** option is specified in MUXSCAN/POST/LBIST mode, this check is executed.

■ Example of execution command

```

#!/bin/csh -f
DFTcheck -TOP xxxx \
-RENEW \
-POST \
-CONTROL test.r ← Specify the power supply area.
-NWCELL ./CELL_def \
-PTSHELL clock_fix.pt \
test_post.v
    
```

■ Check Specification



DFT_clock : {TT_TR , TC_TR or EDT_CLOCK}
~DFT_clock : inversed DFT_clock

CLK_1	CLK_2	OK or NG	
DFT_clock	DFT_clock	NG	
DFT_clock	~DFT_clock	OK	
~DFT_clock	DFT_clock	OK	
~DFT_clock	~DFT_clock	NG	
CLK_3	GT	CLK_4	OK or NG
DFT_clock	DFT_clock	DFT_clock	NG
DFT_clock	~DFT_clock	DFT_clock	OK
DFT_clock	DFT_clock	~DFT_clock	OK
DFT_clock	~DFT_clock	~DFT_clock	NG
~DFT_clock	DFT_clock	DFT_clock	NG
~DFT_clock	~DFT_clock	DFT_clock	OK
~DFT_clock	DFT_clock	~DFT_clock	OK
~DFT_clock	~DFT_clock	~DFT_clock	NG

■ Automatic generation of the clock

Test clock does not usually specify in DFTcheck. Because of that, DFTcheck generates from net (TT_TR) specified by create_clock TC_TR and EDT_CLOCK automatically.

```
create_clock -name TT_TR atom/TT_TR
              ↓
create_clock -name TT_TR atom/TT_TR
create_clock -name TC_TR atom/TC_TR
create_clock -name EDT_CLOCK atom/EDT_CLOCK
```

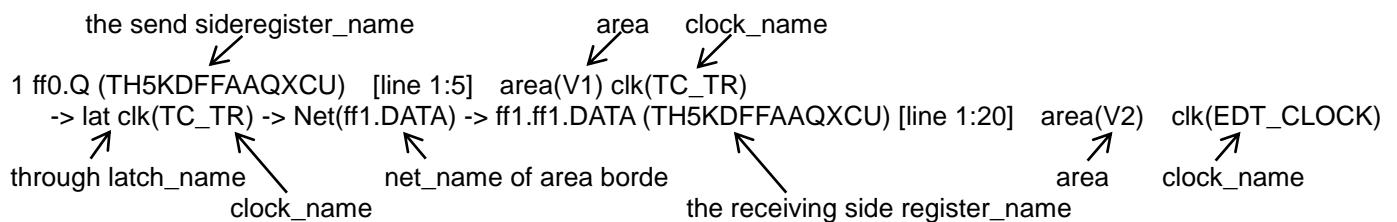
■ Transfer to the other clock

The clock from TC_TR to EDT_CLOCK~ is recognized as inversion.

< Way of looking at message >

ERROR DFT022-1 : There is illegal transfer at DVFS.

No. InstancePin (clock) --> InstancePin (clock)



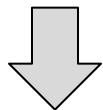
5.2.22 DFT023 Check of SENG circuit

When SEN/SENG attribute is on the output pin of the SENG circuit (SCANEN attribute), this is checked.
 SENG must connect with the gated clock cell.
 SEN must connect with the register.

When SENG circuit is described in soft macro, a cell of NetWalker is necessary.

<Soft macro>

```
module SINGSENGEN_RCARH3_ths_1_top_3 (CK, SENBR, reg_skewed_sen, ac_brmode, tm, SEN, SENG);
    input CK, SENBR, reg_skewed_sen, ac_brmode, tm;
    output SEN, SENG;
    wire SENBR_out, sensig;
    DFQEMD1BWP20P90LVT sengen(.D(SENBR_out), .CP(CK), .SEM(reg_skewed_sen), .Q(sensig));
    AN2D0BWP20P90 sengand(.A1(SENBR), .A2(tm), .Z(SENBR_out));
    OR2D0BWP20P90 sengor(.A1(sensig), .A2(ac_brmode), .Z(SENG));
    BUFFD0BWP20P90 senbuf(.I(sensig), .Z(SEN));
endmodule
```



When there is "", a regular expression is checked.
 In the case of the following example, the name after ths is OK in anything.

<SENGEN.nw>

```
"SINGSENGEN_RCARH3_ths_.*" {type=GATE,SCANEN;
    pin(CK=CK;reg_skewed_sen=SEM;SEN=SEN;SENG=SENG);
    pos(SENBR->SEN; reg_skewed_sen->SEN; tm->SEN);
    pos(SENBR->SENG; reg_skewed_sen->SENG; ac_brmode->SENG;tm->SENG);
    function(SEN=(reg_skewed_sen & Hz)|(SENBR & tm);SENG=((reg_skewed_sen & Hz)|(SENBR & tm)) | ac_brmode );
}
```

<Execution command>

```
#!/bin/csh -f
DFTcheck -TOP test \
-RENEW \
-NWCELL CELL_def \
-NWCELL SENGEN.nw \
-PTSHELL test.pt \
test.v
```

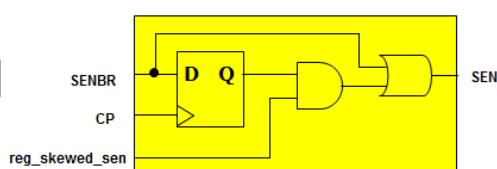
*Function is made as follows.

```
sensig = (reg_skewed_sen & Hz)|SENBR_out
SENBR_out = SENBR & tm
SENG = sensig | ac_brmode
SEN = sensing
```



```
function(
    SEN=(reg_skewed_sen & Hz) | (SENBR & tm);
    SENG= ( (reg_skewed_sen & Hz) | (SENBR & tm) ) | ac_brmode ;
);
```

Soft macro of SENG-FF



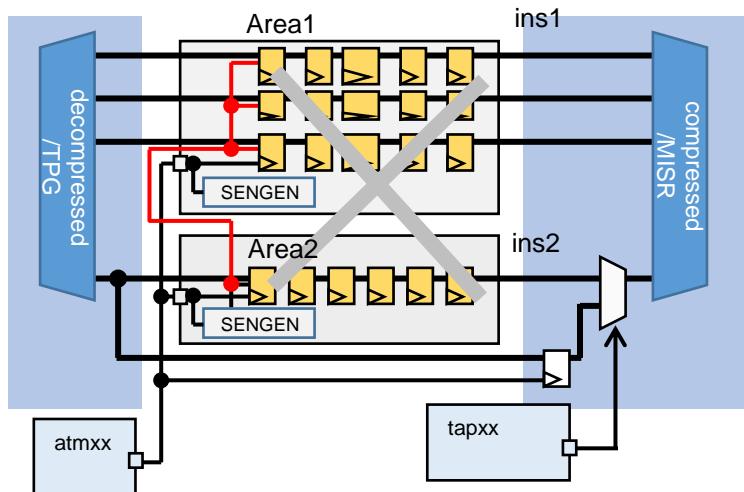
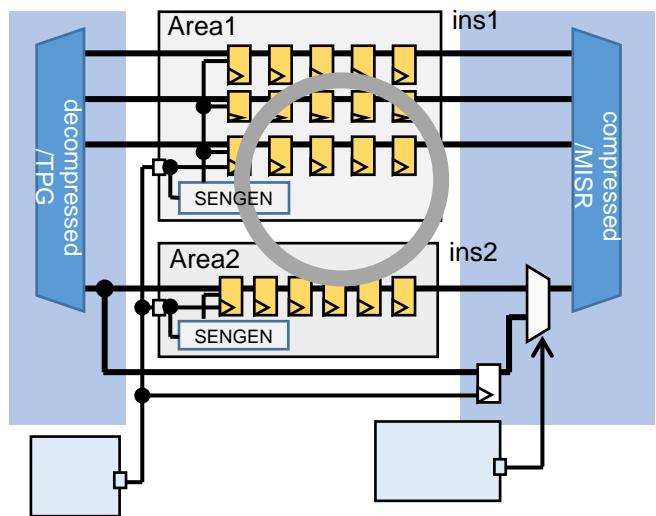
<<DFT023-02>>

This checks whether SENG circuit is an area same as register or GCK cell, about connection of SENG (has SEN/SENG attribute) which is not error in DFT023-01.

In the case that mass production LBIST is mixed with FieldBist, connection must be closed in each area.

When the area of the SENG circuit is different from register (or GCK cell), error is detected by the following designation.
When specification is omitted, this is checked as NULL.

```
set_strings DFT023_AREA ins1/* Area1
set_strings DFT023_AREA ins2/* Area2
```



SENG circuit in Area2 connects with F/F in Area1.

5.2.23 Test Coverage Estimate

Test coverage is estimated in MUXSCAN mode(default).

The rate of detection information of the module in the top hierarchy is output to log.DFTcheck. And the rate of detection of LSI is output to log.

This coverage is the rate of detection in the conditions that error is 0.

When DFT003-7 is error, if the following is not defined, test coverage is not estimated.

```
set_strings NOCLOCK_MUXFF_is_BB "yes" ;
```

<< Output example of log >>

FU (full)	172
DT (detected)	24(13.95%)
UU (unused)	52(30.23%)
TI (tied)	13(7.56%)
BL (blocked)	4(2.33%)
AU (atpg_untestable)	79(45.93%)
Test Covergae	23.30%

If the detailed report is necessary, specify as follows in the PT_SHELL file.

Output file name is "TEST_COVERAGE_DETAIL.f".

```
set_strings test_coverage_detail "yes" ;
```

<< Contents of TEST_COVERAGE_DETAIL.f >>

```
0 DT MB_HFCTS_BUF_0_hf_buf.U22.A // [line 1:138394]
1 DT MB_HFCTS_BUF_0_hf_buf.U22.A // [line 1:138394]
0 DT MB_HFCTS_BUF_0_hf_buf.U22.YB // [line 1:138394]
1 DT MB_HFCTS_BUF_0_hf_buf.U22.YB // [line 1:138394]
0 DT MB_HFCTS_BUF_0_hf_buf.U21.A // [line 1:138393]
:
```

Test coverage of the module in the top hierarchy is output in default.

If specific module is specified as follows, test coverage of that module is output to log.DFTcheck.

```
set_strings test_coverage <module instance name1>;
set_strings test_coverage <module instance name2>;
:
```

<< Output example of log.DFTcheck >>

INFO: Test Coverage .

No. Module Test_coverage

```
1 <module instance name1> 65.38% FU( 112) TI( 0) BL( 0) AU( 36) DT( 68) UU( 8)
2 <module instance name2> 25.00% FU(11224) TI( 36) BL( 16) AU( 10) DT( 10) UU(11152)
:
```

If there is the module which excludes test coverage, specify as follows.

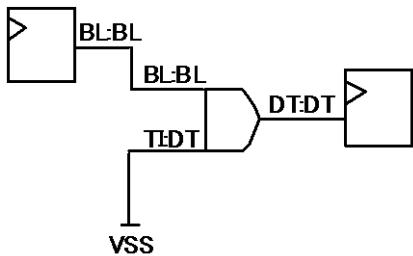
```
set_strings outside_test_coverage <module instance name3>;
```

If FF which clock does not reach assumes as Black Box, the rate of detection falls. Specify as follows.

```
set_strings NOCLOCK_MUXFF_is_BB "yes" ;
```

<< Explanation and the detection method of FU(full), DT(detected), UU(unused), TI(tied), BL(blocked), AU(atpg_untestable) >>

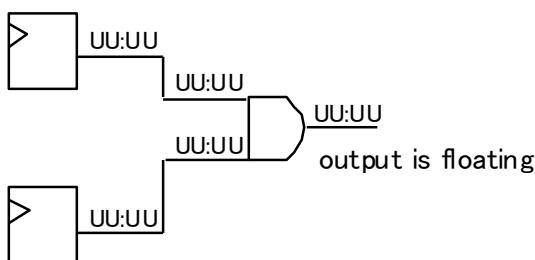
Example1) TI:The non-detection by the power supply BL:The fault supposition that was blocked



<Meaning of BL:BL>
Left is 0 fault supposition.
Right is 1 fault supposition.

BL means detection impossibility because 0/1 fault suppositions were blocked by TieL/H.

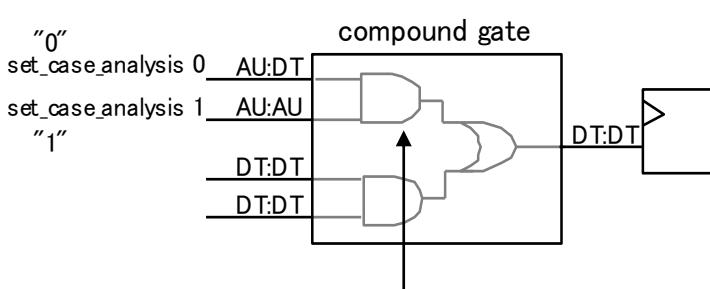
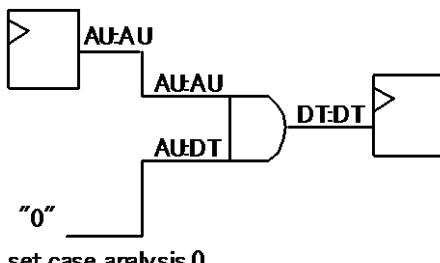
Example2) UU:The unused fault supposition



UU means that fault is not supposed because output is floating or there is not function.

Example3) AU:The untestable in ATPG

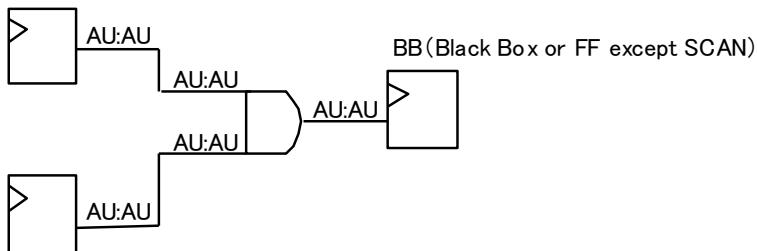
Fault cannot be detected because the logic is fixed at test mode.



The compound gate considers function.
It is estimated whether 0/1 fault suppositions are detected by 0/1 limitation.

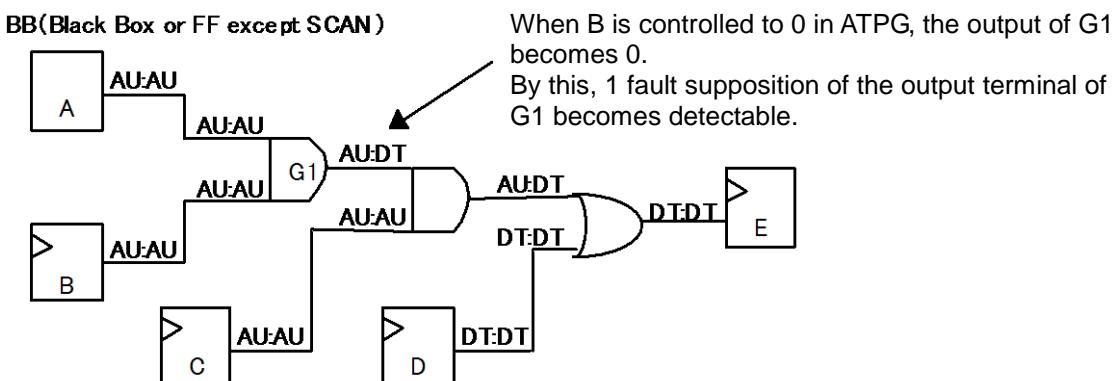
Example4) AU:The untestable in ATPG

Fault cannot be detected because output connects with BB.



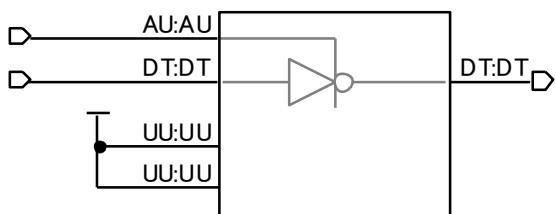
Example5) AU:The untestable in ATPG

Fault cannot be detected by unknown of BB.

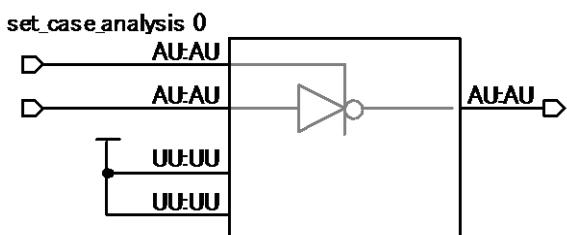


Example6) AU:The untestable in ATPG

The enable signal of I/O cell is untestable.

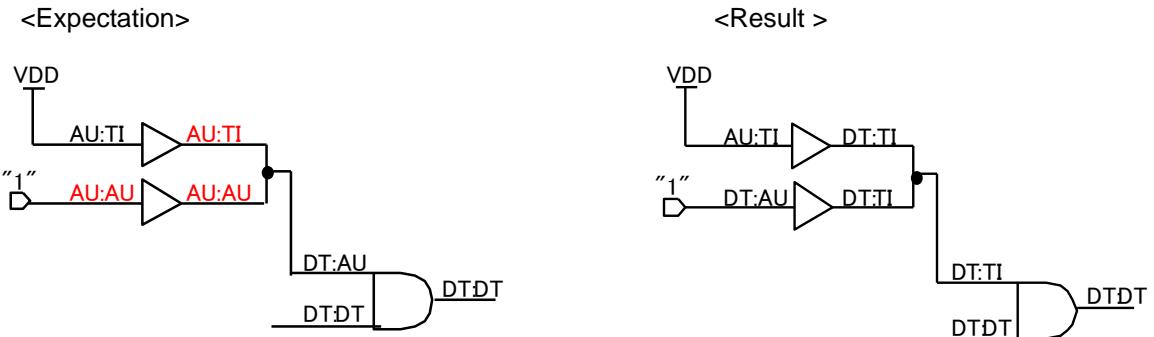


If output is Hiz, the data signal of I/O cell is untestable, too.

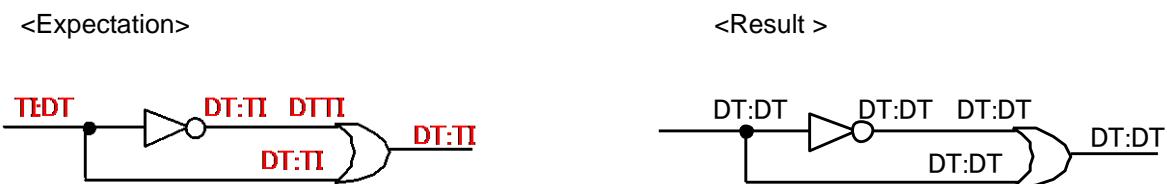


<< The case which fault cannot detect correctly. >>

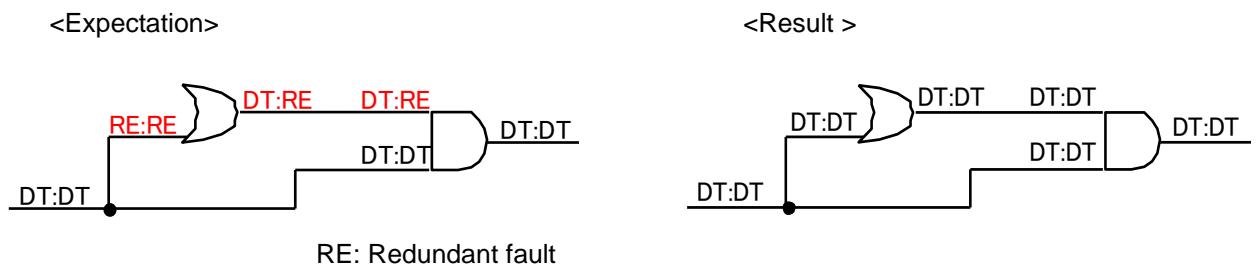
Example1) conflict



Example2) fix to 1 or 0



Example3) undetectable



5.3 Check Items for -SINGEN Option

5.3.1 DFT101

Check the indeterminate values that have occurred by being latched the clock signal to the D pin of BSFF.

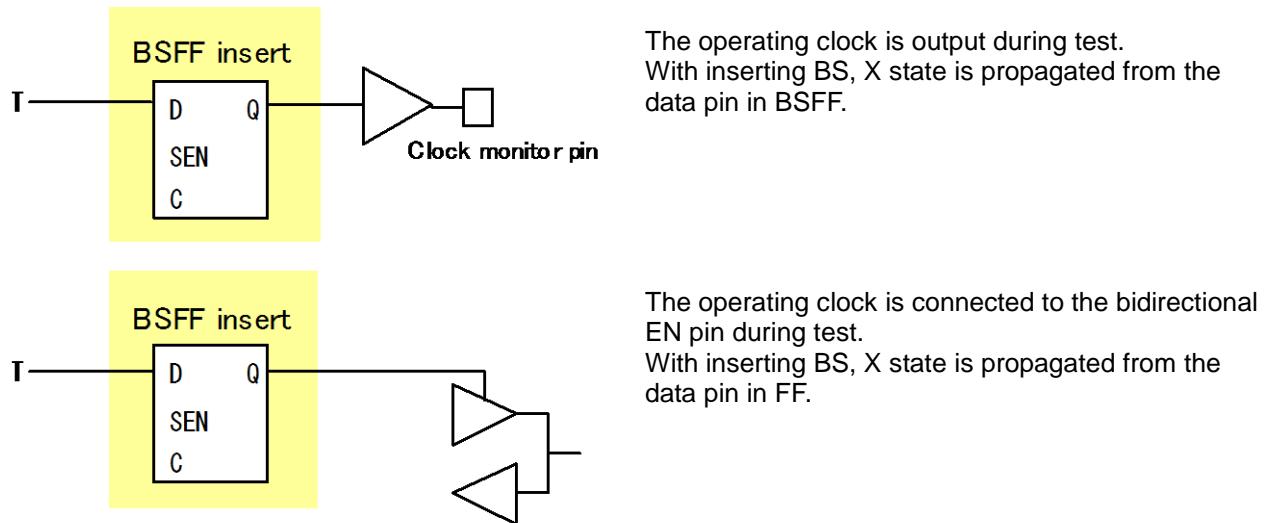
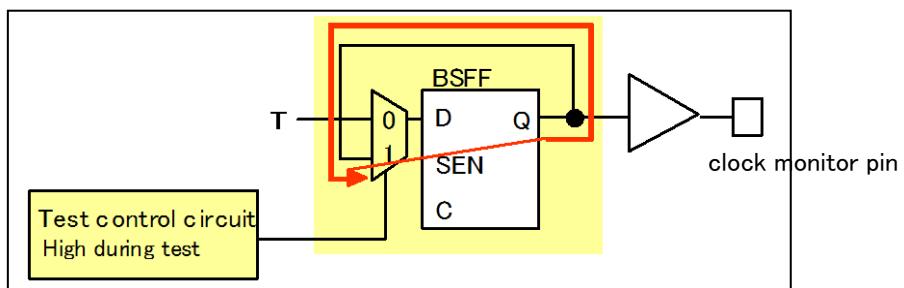


Figure 5.5 Check (1) for SINGEN Option

The following shows how to evade constraints.

Plan1: Specify EXTEST or NOBS to the LSI port which a clock is input into to the IO cell.

- <EXTEST> When logic BIST is executed, BSFF is controlled to do the self-loop by the diagnosis logic.
- <NOBS> Because BSFF cell is not added, a clock is not received.



Plan2: During test, add the logic to intercept a clock in front of IO cell.

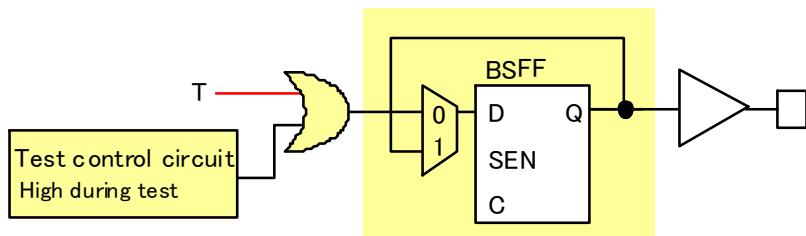


Figure 5.6 Check (2) for SINGEN Option

5.3.2 DFT108

Check the indeterminate values from the black box in BSFF.

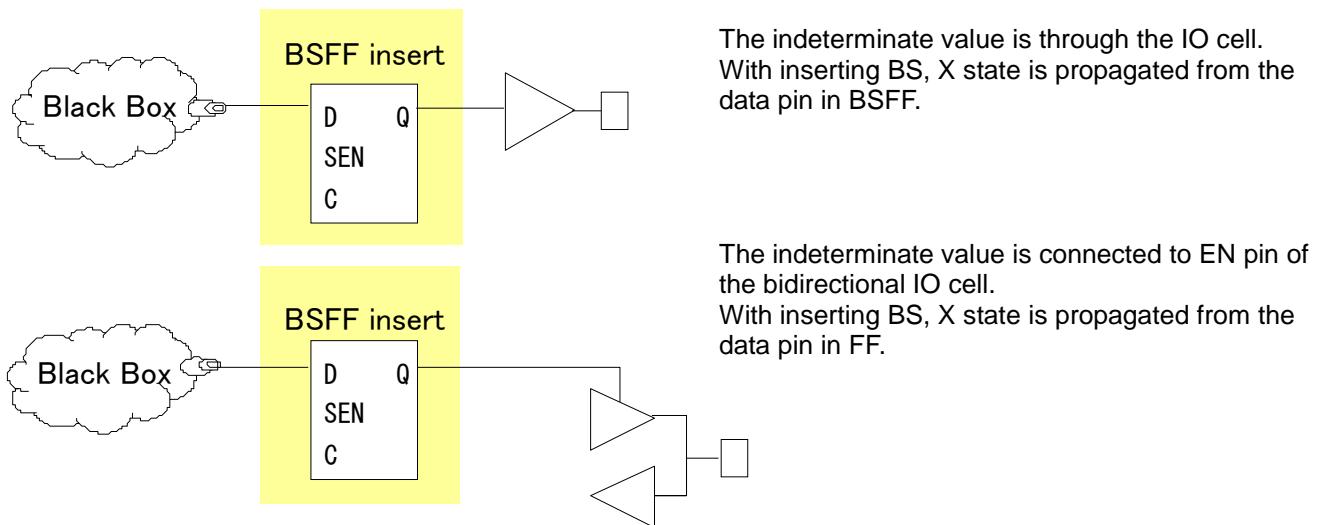
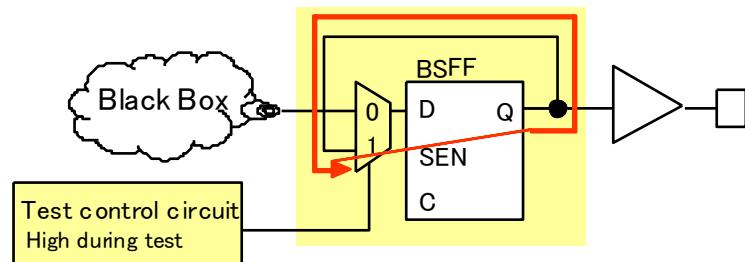


Figure 5.7 Check (3) for SINGEN Option

The following shows how to evade constraints.

Plan1: Specify EXTEST or NOBS to the LSI port which the indeterminate value is input into to the IO cell.
 <EXTEST> When logic BIST is executed, BSFF is controlled to do the self-loop by the diagnosis logic.
 <NOBS> Because BSFF cell is not added, a clock is not received.



Plan2: During test, add the logic to intercept a clock in front of IO cell.

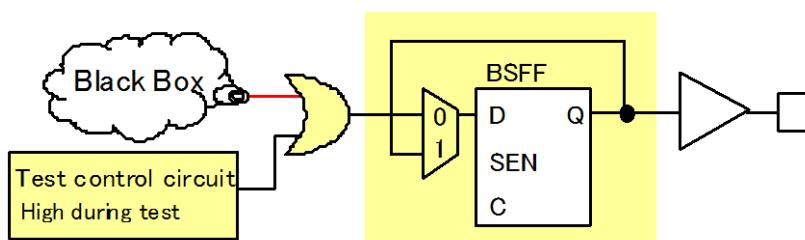
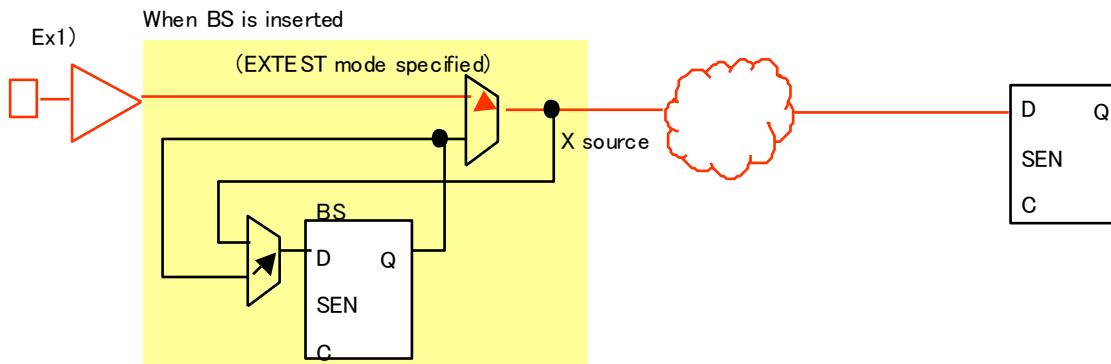


Figure 5.8 Check (4) for SINGEN Option

5.3.3 DFT109

Because fixed values are input during test, check to see if any EXTEST-specified pins have settings of their fixed values forgotten.



Ex3) In bidirectional IO which has had NOBS mode specified, fixed value & inside signal is conflicted.

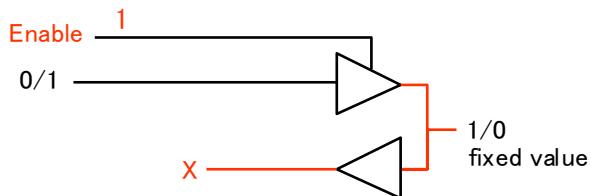


Figure 5.9 Check (5) for SINGEN Option

- If no fixed test values are specified for any pin which has had EXTEST mode specified in order to apply a value such as test mode pin from outside the LSI or reject indeterminate values from within the LSI during test, indeterminate values from the LSI pins propagate. (Ex1)
- If NOBS mode is specified when BS is not inserted because of analog pins and no fixed test values are specified for any pin during test, indeterminate values from the LSI pins propagate. (Ex2)
- In bi-directional IO which has had NOBS mode specified, if the input/output enable is active, fixed value & inside signal is conflicted, and indeterminate value is generated. (Ex3)

Function to check constraints

- In cases where a DFT profile is specified, if any input/bidirectional pin is specified for EXTEST or NOBS in the DFT profile, but no fixed values are specified for it, an error is generated to that effect.
- Also, if this pin is used for clock input during test, it is excluded.
- However, if the pin is a bidirectional pin with its output enable fixed to enable, a warning is generated. (For small pin count test)

5.4 Check Items for -MINORI / -PREMINORI / -POSTMINORI Option

5.4.1 DFT301 Check for -MINORI

Check that clock is directly connected to each clock pin of RAM and ROM in MINORI mode.

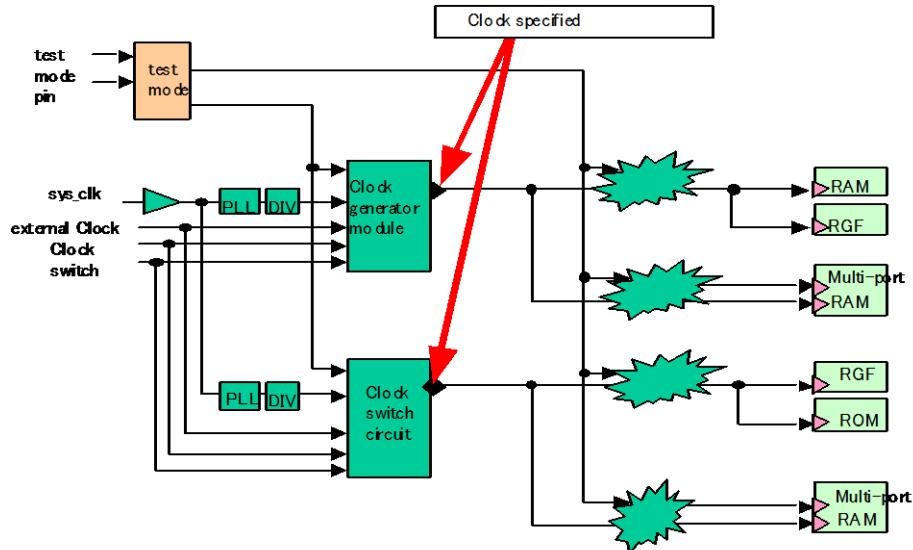


Figure 5.10 Check for MINORI Option

Input

(1) Specify clock (-PTSHELL)

Example)

```
create_clock -period 10 -name CLOCK_A -waveform {0 5} CLK_A
create_clock -period 10 -name CLOCK_B -waveform {0 5} CLK_B
set_case_analysis 1 mbist_mode
```

(2) Specify RAM/ROM module name by -MINORI option.

Check "CLK" terminal of "BSPA33P204103ZZ0ZZ" and "T0" and "T1" terminal of "C16164XU3ZGEUZZ".

Example)

```
BSPA33P204103ZZ0ZZ CLK
C16164XU3ZGEUZZ T0
C16164XU3ZGEUZZ T1
```

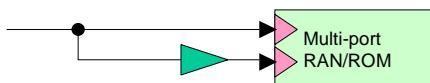
(3) Executing Procedure

Example)

```
DFTcheck -TOP TOP -WORK work -MINORI mdl1 -PTSHELL clock_source .....
```

(4) Check item

- RAM/ROM clock terminal don't connect to specified clock.
- In the case of multi-port RAM, when clocks differ and reversed clocks are checking.



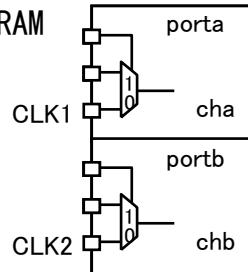
5.4.2 Check for -PREMINORI and -POSTMINOR

DFT0302-1 clock check of MINORI object RAM/ROM

<<-POSTMINORI>>

- The RAM clock terminal where clock is not transmitted directly in MINORI mode is reported.
- For multiple port RAM, check whether clock propagates to cha and chb which are defined function in NetWalker library.

Multiple port RAM



description in NetWalker library

$$\begin{aligned} \text{cha} &= (\text{SELTCLKA}? \text{TCLKA}: \text{CLKA}) \\ \text{chb} &= (\text{SELTCLKB}? \text{TCLKB}: \text{CLKB}) \end{aligned}$$

<<-PREMINORI>>

- If the clock does not arrive at "clk" and "clka" and "clkb" pins of the collared memory block, it is error.
- Specify the collared memory by -FILE or -PTSHELL option.

But if file (Collared_type_out.f) which Collared_memory_extra command generates for DFT304-3 is specified, the following additional specification is unnecessary.

(1) Description for -FILE file

```

set_strings CollaredMEM  {b*c_cr*} {b*c_cm*} {b*c_co*} {b*c_cn*} {vmc_pipeline_wrapper_*} ;
set_strings CollaredMEM  {e*c_cr*} {e*c_cm*} {e*c_co*} {e*c_cn*} ;
set_strings CollaredMEM  {w*c_cr*} {w*c_cm*} {w*c_co*} {w*c_cn*} ;
set_strings CollaredMEM  {o*c_cr*} {o*c_cm*} {o*c_co*} {o*c_cn*} ;
set_strings CollaredMEM  {amcip*c_cr*} {amcip*c_cm*} {amcip*c_co*} {amcip*c_cn*} ;
    
```

(2) Description for -PTSHELL file

```

string CollaredMEM[] = { "b*c_cr*", "b*c_cm*", "b*c_co*", "b*c_cn*", "vmc_pipeline_wrapper_**",
                        "e*c_cr*", "e*c_cm*", "e*c_co*", "e*c_cn*",
                        "w*c_cr*", "w*c_cm*", "w*c_co*", "w*c_cn*",
                        "o*c_cr*", "o*c_cm*", "o*c_co*", "o*c_cn*",
                        "amcip*c_cr*", "amcip*c_cm*", "amcip*c_co*", "amcip*c_cn*" } ;
    
```

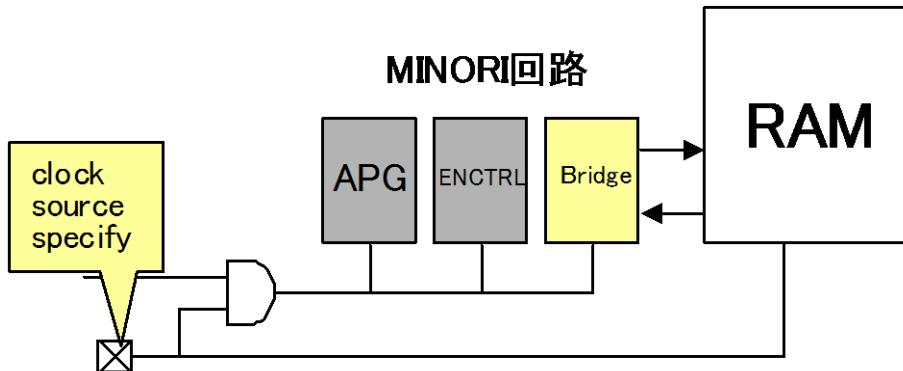
But please specify the details not to overlap when the wild card overlaps with the user logic.

DFT302-2 same clock check of the multiple port RAM

- For multiple port RAM, check whether the same clock propagates to cha and chb at POSTMINORI (MINORI test) mode.

DFT303-1 clock source same check of MINORI circuit and RAM

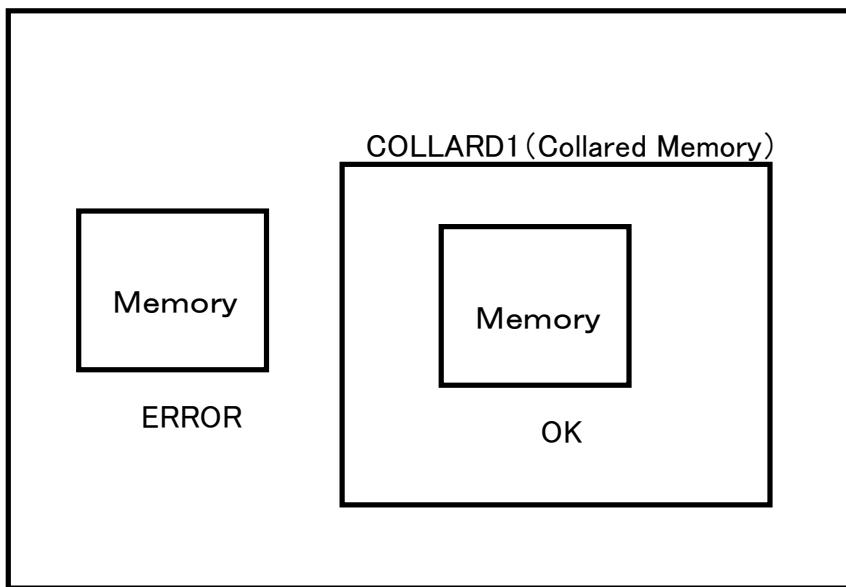
- Check whether same clock source is connected to RAM and bridge circuit at POSTMINORI test.



Note: DFT303-1 is not checked by default. Please specify -CHECK_303 to check it.

5.4.3 DFT304-2 Check of the memory which there is not in collared memory

If CollaredMEM was specified in PREMINOTI mode, it is checked. The memory cell that there is not the collared memory at the high rank hierarchy is the error.



Specify the collared memory by -FILE or -PTSHHELL option.

But if file (Collared_type_out.f) which Collared_memory_extra command generates for DFT304-3 is specified, the following additional specification is unnecessary.

(1) Description for -FILE file

```
set_strings CollaredMEM {b*c_cr*} {b*c_cm*} {b*c_co*} {b*c_cn*} {vmc_pipeline_wrapper_*} ;  
set_strings CollaredMEM {e*c_cr*} {e*c_cm*} {e*c_co*} {e*c_cn*} ;  
set_strings CollaredMEM {w*c_cr*} {w*c_cm*} {w*c_co*} {w*c_cn*} ;  
set_strings CollaredMEM {o*c_cr*} {o*c_cm*} {o*c_co*} {o*c_cn*} ;  
set_strings CollaredMEM {amcip*c_cr*} {amcip*c_cm*} {amcip*c_co*} {amcip*c_cn*} ;
```

(2) Description for -PTSHHELL file

```
string CollaredMEM[] = { "b*c_cr*", "b*c_cm*", "b*c_co*", "b*c_cn*", "vmc_pipeline_wrapper_*",  
    "e*c_cr*", "e*c_cm*", "e*c_co*", "e*c_cn*",  
    "w*c_cr*", "w*c_cm*", "w*c_co*", "w*c_cn*",  
    "o*c_cr*", "o*c_cm*", "o*c_co*", "o*c_cn*",  
    "amcip*c_cr*", "amcip*c_cm*", "amcip*c_co*", "amcip*c_cn*" } ;
```

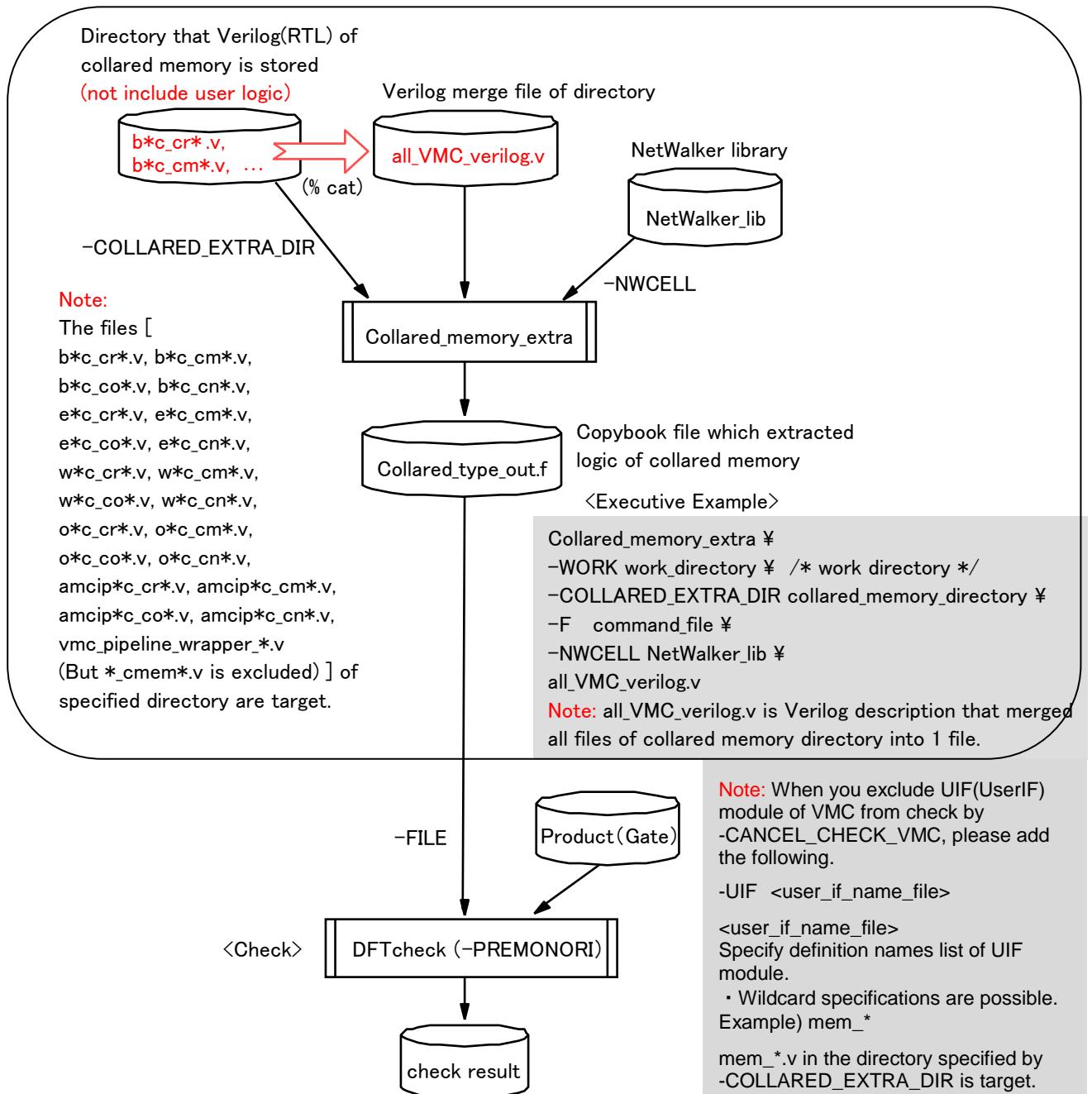
But please specify the details not to overlap when the wild card overlaps with the user logic.

5.4.4 DFT304-3 Check of the BIST Logical circuit which there is not in collared memory

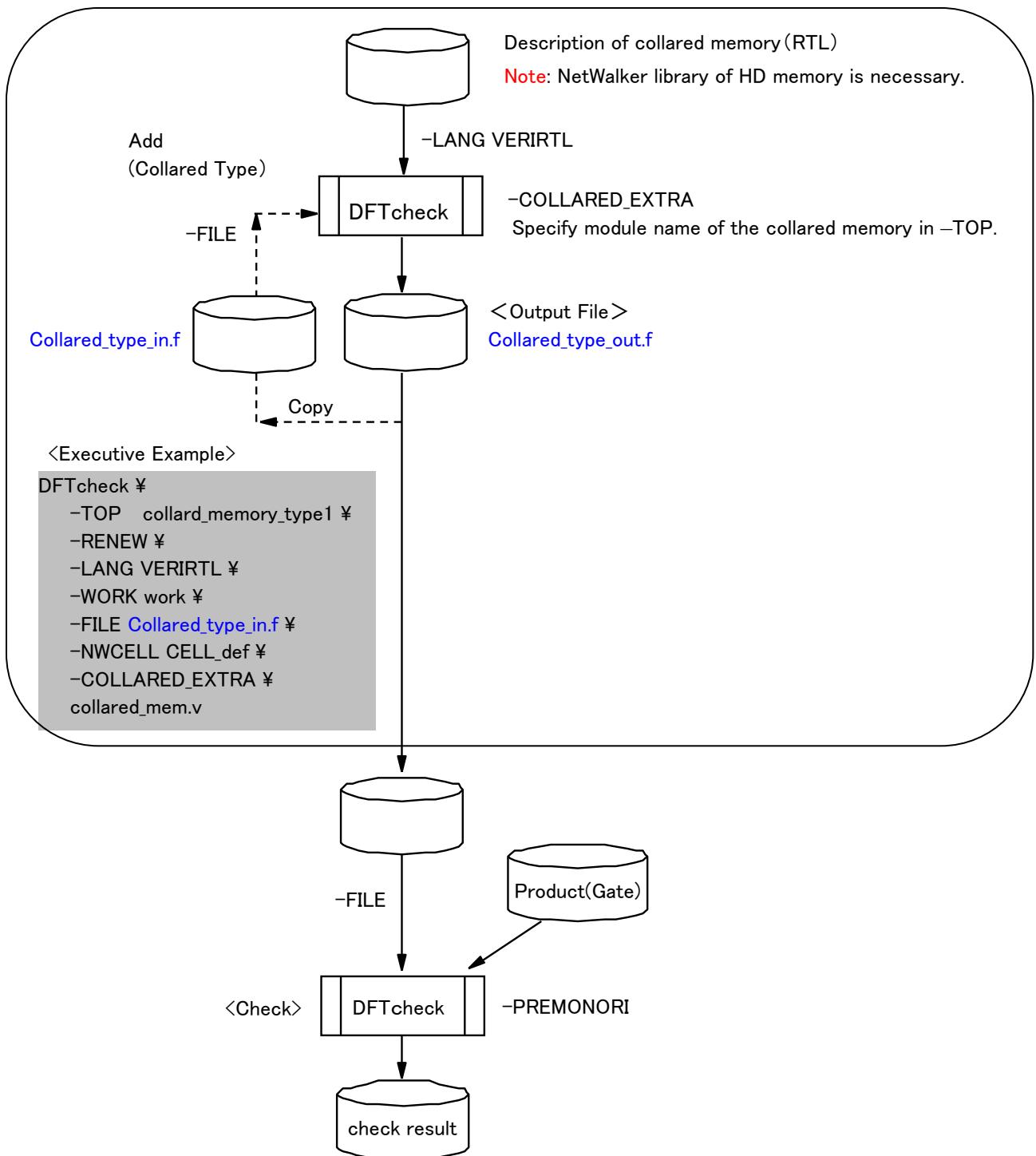
Since there is the case that the logic in CollaredMEM generated by logic composition is different from intention, it is checked whether the logic is the same as the logic before the composition.

The copybook file which extracted the logic of collared memory beforehand is made with COLLARED_EXTRA mode. When DFTcheck is executed, the logic is compared with a copybook file according to type of collared memory.

<Expectation extraction method1: Directory specification >



<Expectation extraction method2: Individual execution >

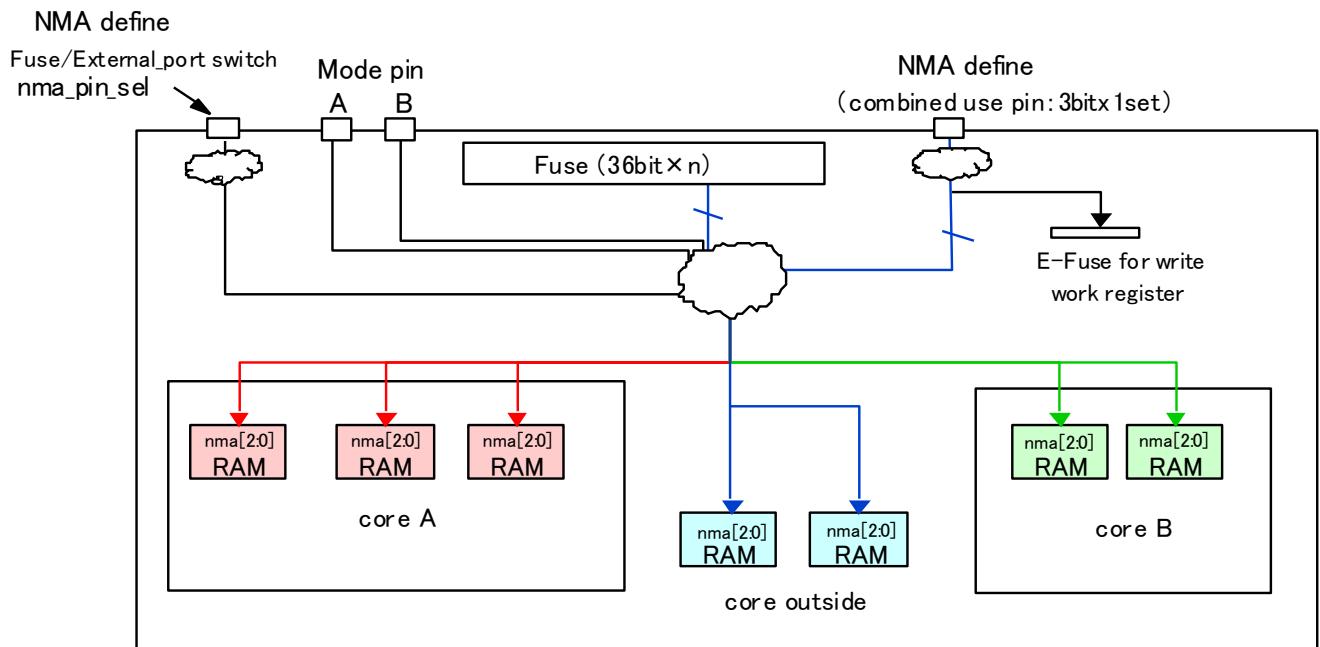


5.4.5 DFT305-1 Check of NMA connection

The connection of the RAM assist adjustment terminal (NMA) is checked.

There are two kinds of check methods.

- It is checked whether the pass from the start point (Fuse output or External port of NMA) is connected directly logically. When the gate which exists between path is like buffer by logic fixation, there is not problem.
- It is checked whether the path is not disconnected by external port definition.



Example) The path disconnection check by external port define.

Mode name	Mode	External port define	Path
A1	MBIST	nma_pin_sel = H	Fuse output port (3bit) -> NMA pin of RAM
A2	MBIST	nma_pin_sel = L	External port (3bit) -> NMA pin of RAM
B	user	nma_pin_sel = H A = L B = H	Fuse output port (3bit) -> NMA pin of RAM

Specify as follows in the PT_SHELL file for check.

When NMA_TEST is not specified, the check is not executed.

If "yes" was specified in option_dft305_permit_not_direct, the path disconnection check is executed.

The format of NMA_TEST is

"Mode_name Three start point nets External port define (signal_name and H/L) \$".

"\$" means the end.

```
set_strings option_dft305_permit_not_direct yes
set_strings NMA_TEST A1 {moni/FOUT[0]} {moni/FOUT[1]} {moni/FOUT[2]} nma_pin_sel H $
set_strings NMA_TEST A2 penc0 penc1 penc2 nma_pin_sel L $
set_strings NMA_TEST B {moni/FOUT[0]} {moni/FOUT[1]} {moni/FOUT[2]} nma_pin_sel H A L B H $
```

* The start points are 3 nets by default. If those are 6 nets, switch those by the following options.

[set_strings NMA_6BIT_MODE yes](#)

5.4.6 DFT306-1 Check of RS connection

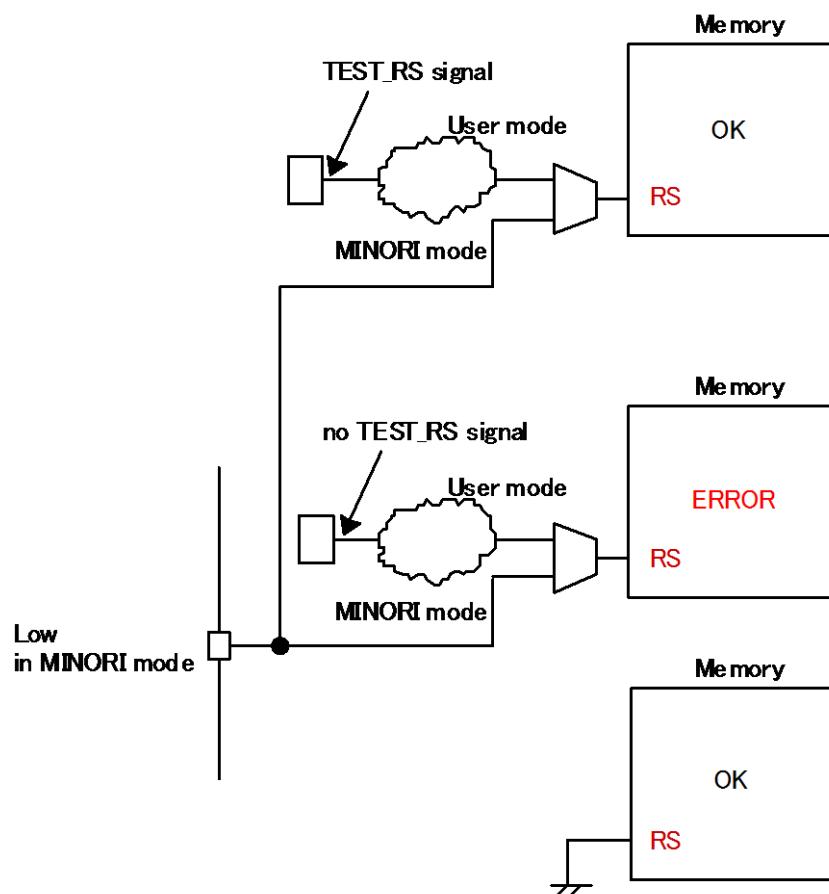
The RS (Resume Standby) pin of CRAM must be fixed to Low in POSTMINORI. This is checked in DFT015. DFT306-1 checks whether the RS pin that logic is not fixed is controlled with a user signal. Specify user signals in the PT_SHELL file as follows for check. Wildcard specifications are possible.

```
set_strings TEST_RS signal1 ;
set_strings TEST_RS signal2 ;
:
```

The RS pin which the signal specified by TEST_RS is not connected to is error.

In addition, memory connected to the specified signal is output as standard streams.

```
<<RS_TEST c2_ffddmrs_p(cpg2_pvc5.c2_ffddmrs_p) >>
->ffddm_pvc4.dram_ib_0_1.i0.i0.RS
->ffddm_pvc4.dram_ia_0_0.i0.i0.RS
->ffddm_pvc4.iram_ib_0_2.i0.i0.RS
->ffddm_pvc4.iram_ib_0_1.i0.i0.RS
->ffddm_pvc4.iram_ia_0_0.i0.i0.RS
```

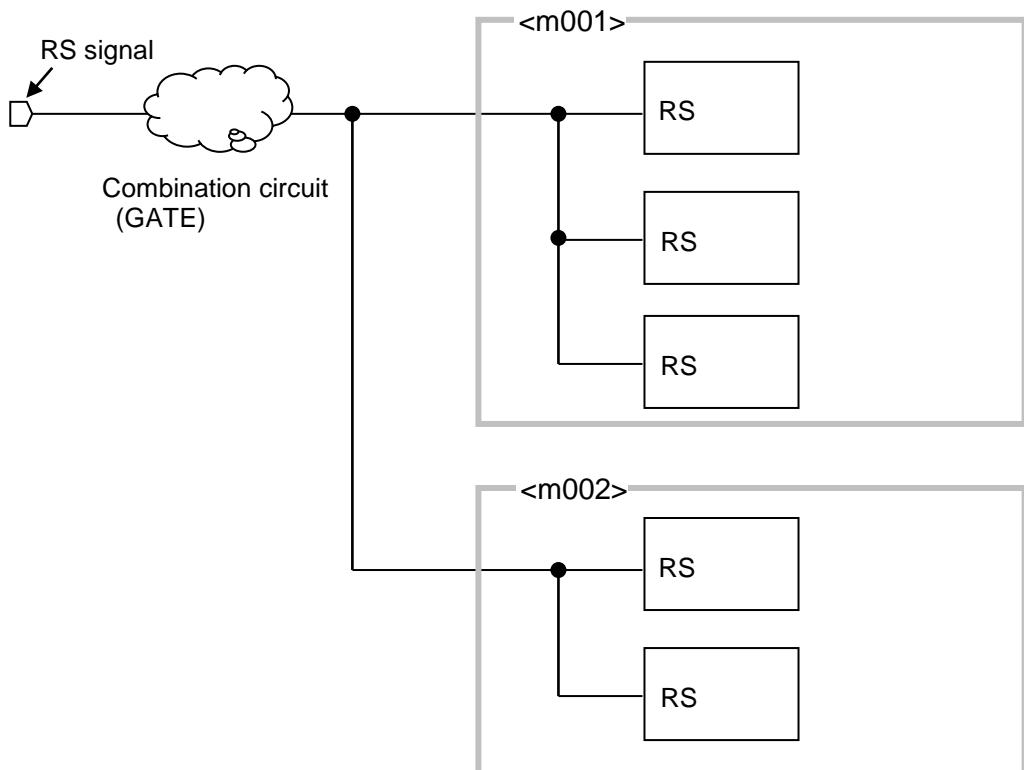


5.4.7 DFT306-2 Report of the memory where RS signal arrives at the RS terminal for -POSTMINORI

The list of memory controlled by RS signal is reported. This is in order to confirm whether memory is controlled by RS signal according to specifications that user intended.

Please confirm connection with the memory of the RS signal.

In MBIST mode, RSChain that RS signal becomes the starting point should be the constitution that is controlled with the external port directly. The case that information of the timing arc is connected directly is output.



[Format]

```
#<RS signal>
<Instance name of Memory> <Instance name of upper block>
```

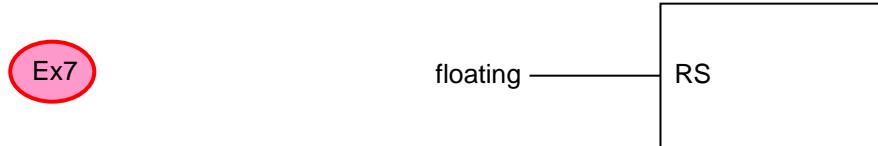
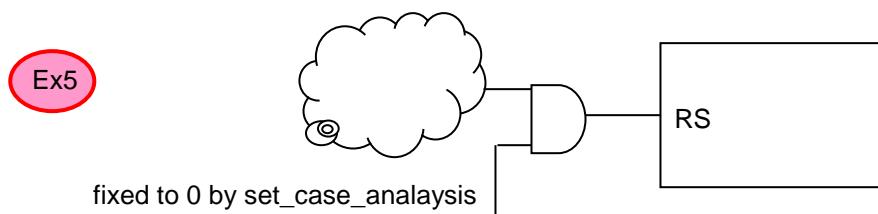
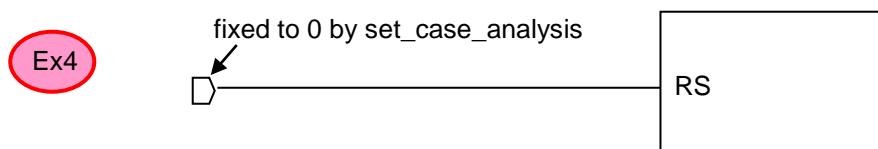
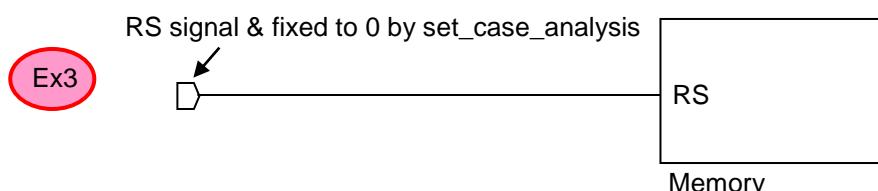
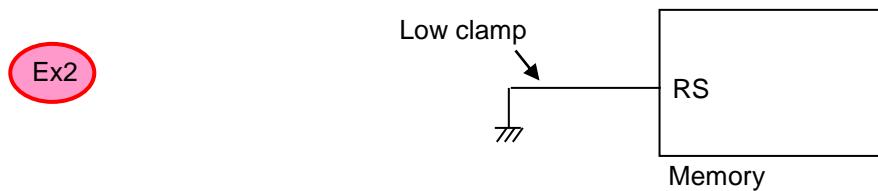
<<Output Example>>

```
# rs
m001.mem1 m001
m001.mem2 m001
m001.mem3 m001
m002.mem1 m002
m002.mem2 m002
```

- Example1) Because memory is controlled directly by RS signal specified as external port, it is output to the RS pin connection list file



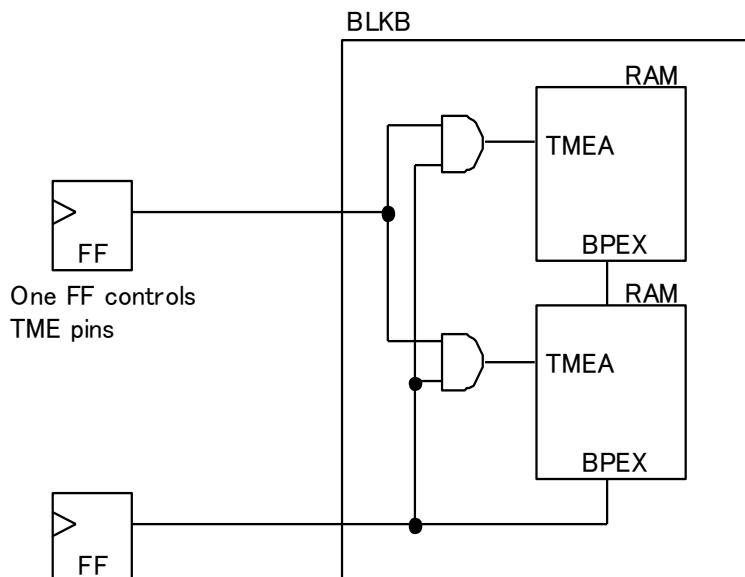
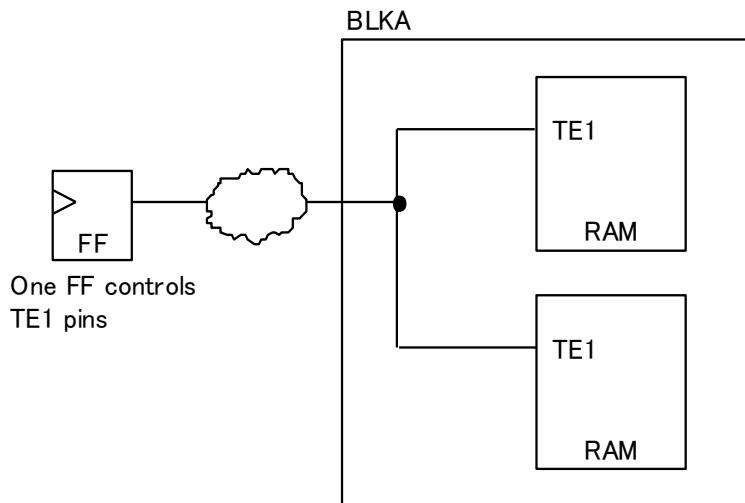
- Example2-7) Because memory is not controlled directly by RS signal specified as external port, it is not output to the RS pin connection list file. And because there is not the check function, error is not reported.



5.4.8 DFT307-1 Check of memory control signal connection for -POSTMINORI

The memory ports which has the following attributes in NetWalker library must be controlled with one same register. (The attribute is CTE1, CTE2, TME, TAE, CTPE or TE5.)

The port connected to different register is error. But the register controlling the disturb port (The attribute is BPE.) is excluded when memory has the disturb port.



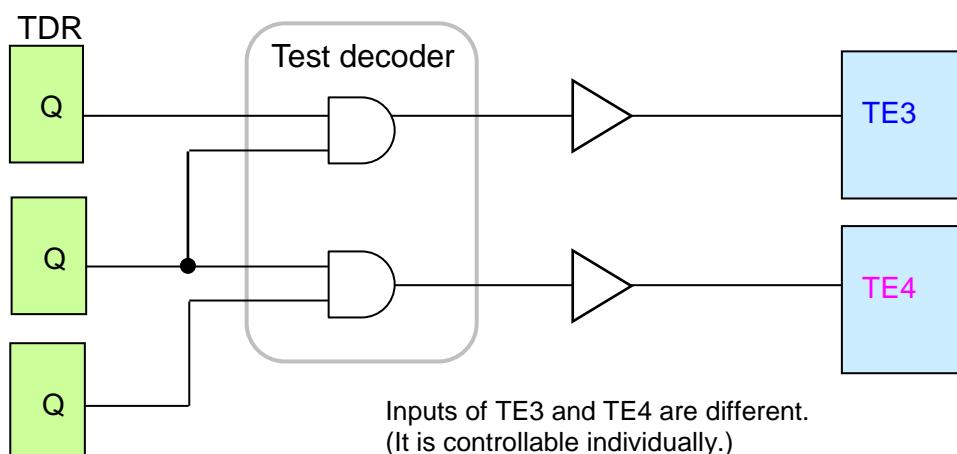
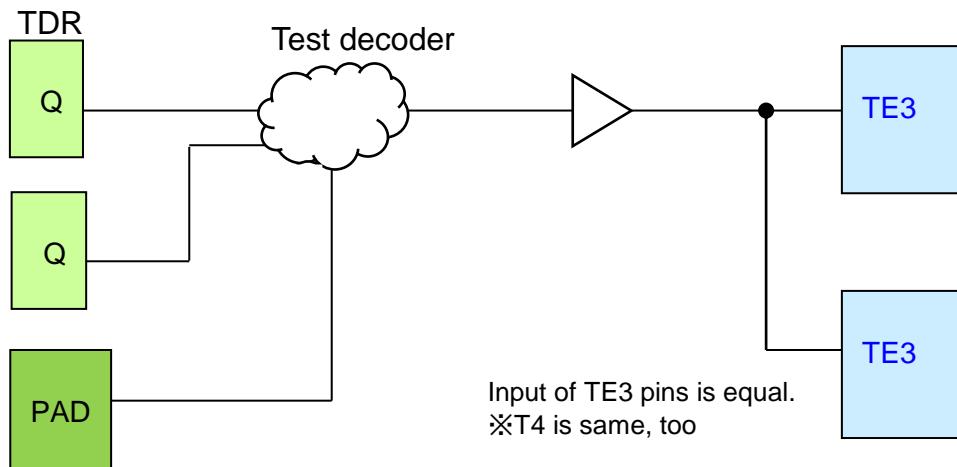
A top module is checked. If there was description in the PT_shell as follows, the specified module is checked. Specify the check module in the PT_shell file as follows.

```
set_strings DFT307_01_TYPE BLKA ;
set_strings DFT307_01_TYPE BLKB ;
```

5.4.9 DFT307-2 Check of memory test terminal connection for -POSTMINORI

Because test pins (TE3/TE4) of RV40F (ph2) SRAM are controlled by TDR(Test Data Register), these must meet the following conditions. The case which violated these conditions is error.

- The input logic of TE3 terminals of all SRAM is equal.
- The input logic of TE4 terminals of all SRAM is equal.
- The input logic of TE3 and TE4 is not equal. (Independent control is possible.)



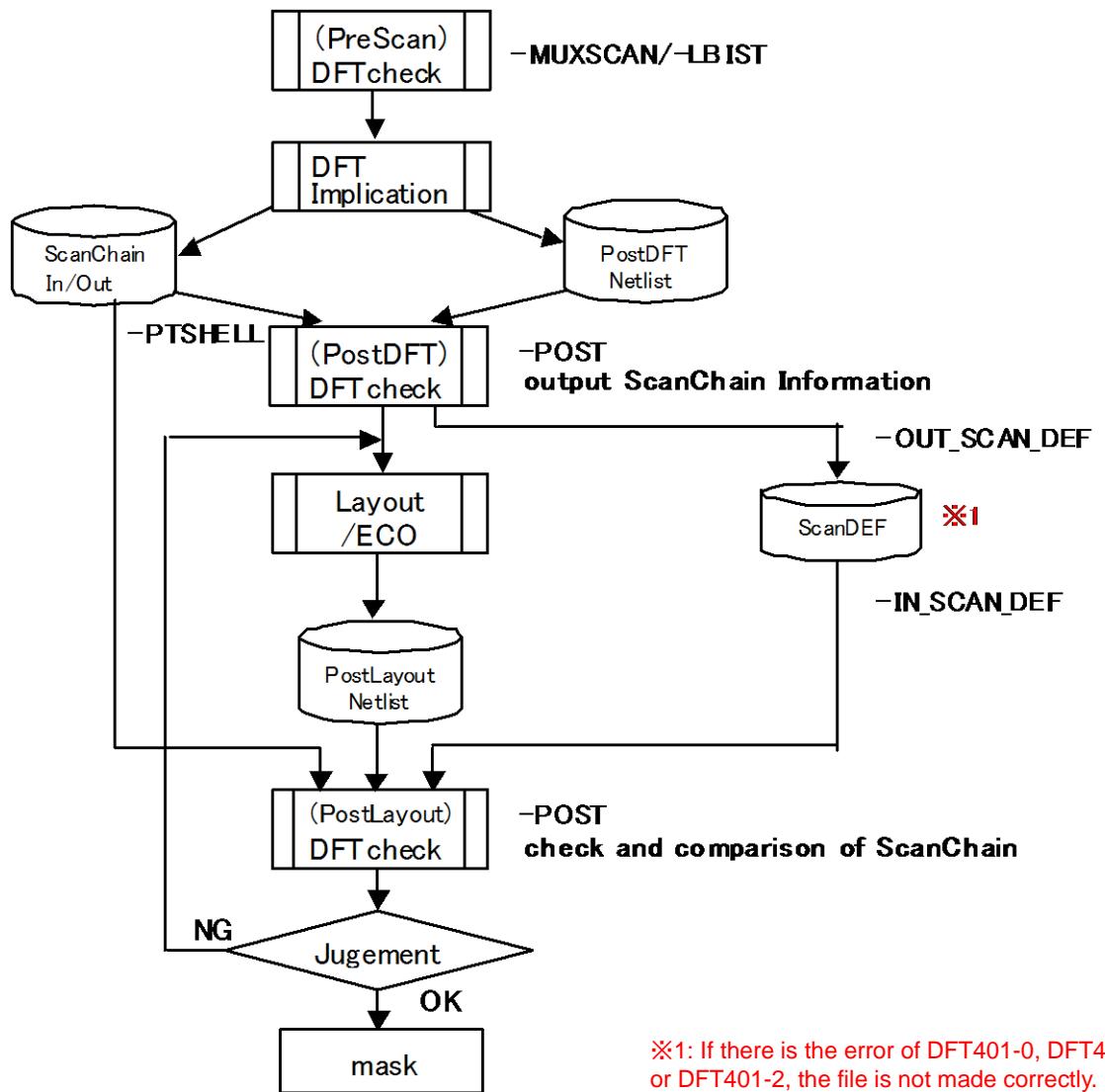
Note:

- (1)The input logic of a pin which checked first is expectation.
- (2)Only when each input logic of TE3 or TE4 was equal, the logic of T3 and TE4 is compared.

5.5 Check Items for -POST Option

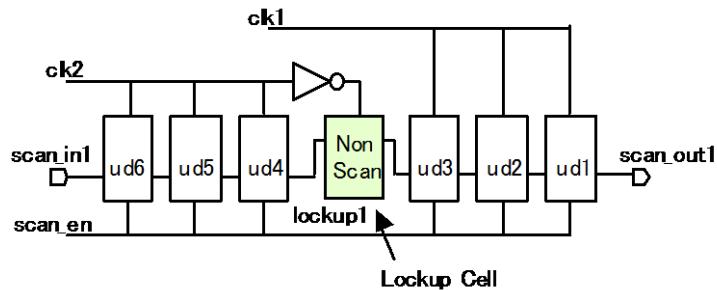
- Connection check of ScanChain.
 - Comparison of ScanChain in Layout pre and post.
- Lockup cell structure and shift register structure too are supported.

In addition, DFT003, DFT004 and 013 are checked, too.



<Lockup cell structure>

This is the structure which merged the scan chain of the different clock by Lockup cell.



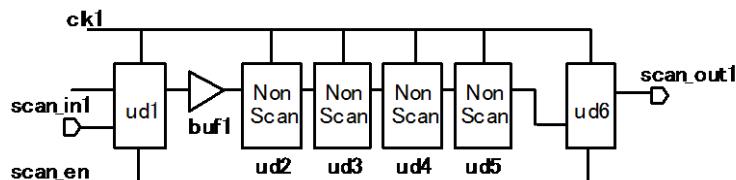
```

DIVIDERCHAR "/" ;
VERSION 5.7 ;
BUSBITCHARS "I" ;
DESIGN top ;
SCANCHAINS 2 ;
- chain_1_1
+ START ud6 SO
+ FLOATING
ud5 ( IN SIN ) ( OUT SO )
ud4 ( IN SIN ) ( OUT SO )
+ STOP lockup1 DATA
+ PARTITION partition_clk2 MAXBITS 2 ;
- chain_1_2
+ START ud3 SO
+FLOATING
ud2 ( IN SIN ) ( OUT SO )
+ STOP ud1 SIN
+ PARTITION partition_clk1 MAXBITS 1 ;
END SCANCHAINS
END DESIGN

```

<Shift_register structure>

This is the structure which the shift_register was just used for.



```

DIVIDERCHAR "/" ;
VERSION 5.7 ;
BUSBITCHARS "I" ;
DESIGN top ;
SCANCHAINS 1 ;
- chain_1_1
+ START ud1 Q
+ ORDERED
buf1 ( IN A ) ( OUT Y )
ud2 ( IN DATA ) ( OUT Q )
ud3 ( IN DATA ) ( OUT Q )
ud4 ( IN DATA ) ( OUT Q )
ud5 ( IN DATA ) ( OUT Q )
+ STOP ud6 SIN
+ PARTITION partition_clk1 MAXBITS 5 ;
END SCANCHAINS
END DESIGN

```

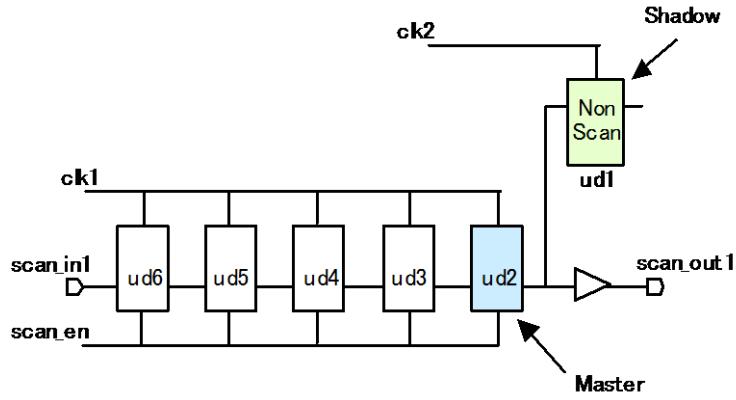
<Shadow Element>

Because there is the reason why scan is not possible, Shadow Element is the cell excluded from scan.

Default is error. If error is excluded, please specify -OUTSIDE_SCAN_INS option.

The structure of Shadow Element is not recommended.

ud2 is Master Element. ud1 is Shadow Element.



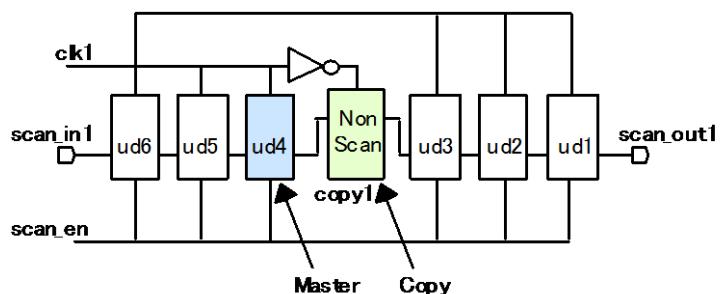
```
DIVIDERCHAR "/";
VERSION 5.7;
BUSBITCHARS "[]";
DESIGN top;
SCANCHAINS 1;
- chain_1_1
+ START ud6 SO
+ FLOATING
ud5 ( IN SIN ) ( OUT SO )
ud4 ( IN SIN ) ( OUT SO )
ud3 ( IN SIN ) ( OUT SO )
+ STOP ud2 SIN
+ PARTITION partition_clk1 MAXBITS 3 ;
END SCANCHAINS
END DESIGN
```

<Copy Element>

This is the cell which adjust the timing of scan chain.

ud4 is Master Element. The next cell of ud4 is Copy Element.

This is the structure of the Lockup latch which is used when the scan chain of the different clock is merged.



```
DIVIDERCHAR "/";
VERSION 5.7;
BUSBITCHARS "[]";
DESIGN top;
SCANCHAINS 1;
- chain_1_1
+ START ud6 SO
+ FLOATING
ud5 ( IN SIN ) ( OUT SO )
+ ORDERED
ud4 ( IN SIN ) ( OUT SO )
copy1 ( IN DATA ) ( OUT Q )
+ FLOATING
ud3 ( IN SIN ) ( OUT SO )
ud2 ( IN SIN ) ( OUT SO )
+ STOP ud1 SIN
+ PARTITION partition_clk1 MAXBITS 5 ;
END SCANCHAINS
END DESIGN
```

<Clock sequential test correspondence (DFT Shift_register structure)>

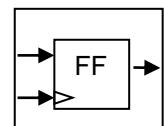
This is the constitution that used the shift register for the test.

<Clock sequential test correspondence>

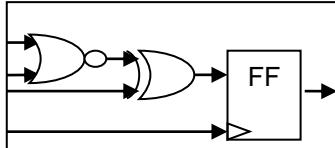
This is test to apply a clock several times at the time of capture movement to reduce LBIST execute time of FieldBIST.

A chain is built with only control TP FF, and normal FF is used.

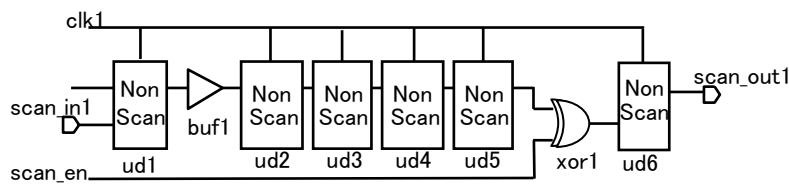
Or a chain is built with only observation TP FF, and SFF cell is replaced with the following soft macro.



Control TP FF soft macro
(normal FF)



Observation TP FF soft macro



```

VERSION 5.7 ;
DIVIDERCHAR "/";
BUSBITCHARS "I" ;
DESIGN top ;
SCANCHAINS 1 ;
- chain_1_1
+ START PIN scan_in1
+ FLOATING
ud1 ( IN DATA ) ( OUT Q )
+ ORDERED
buf1 ( IN A ) ( OUT Q )
ud2 ( IN DATA ) ( OUT Q )
+ FLOATING
ud3 ( IN DATA ) ( OUT Q )
ud4 ( IN DATA ) ( OUT Q )
ud5 ( IN DATA ) ( OUT Q )
+ ORDERED
xor1 ( IN A ) ( OUT Y )
ud6 ( IN DATA ) ( OUT Q )
+ STOP PIN scan_out1
END SCANCHAINS
END DESIGN

```

5.5.1 DFT401-0 SCAN_DEF file Check

- This is check about the description of the SCAN_DEF file.
Only the format of SCAN_DEF which DFTcheck output can be input.

<File specifications>

- (1) The delimiter is not changed by DIVIDERCHAR.
- (2) The arrangement symbol is not changed by BUSBITCHARS.
- (3) The next one character of backslash is escaped.
- (4) The top "#" of line becomes comment.
- (5) The command must be described in the top of line.
- (6) Blanks are necessary between the commands, '(', '+', or '-'.
- (7) The order of the command in the line cannot be changed.
- (8) PARTITION name and MAXBITS in PARTITION cannot be omitted.

5.5.2 DFT401-1 Scan-in/out Information Check

This is check about Scan-in/out information specified in PT shell. The double definition, or the existence of specified net is checked.

Example) The definition of scan_in1 was duplicated.

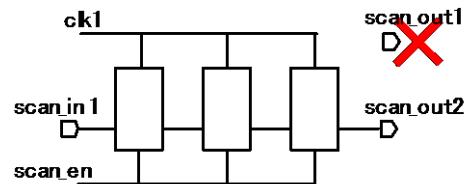
```
set_strings POST_DFT scan_in1 scan_out1 ;  
set_strings POST_DFT scan_in1 scan_out2 ;
```

5.5.3 DFT0401-2 Scan Chain Check

- F/F does not connect with SCAN-OUT.**
scan-out net is not connected instances.

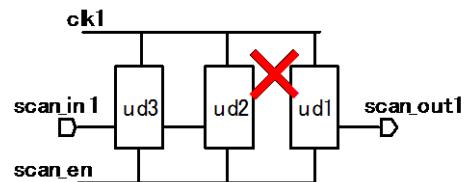
Example)

```
set_strings POST_DFT scan_in1 scan_out1 ;
-> Connection of scan_out1 is wrong.
```



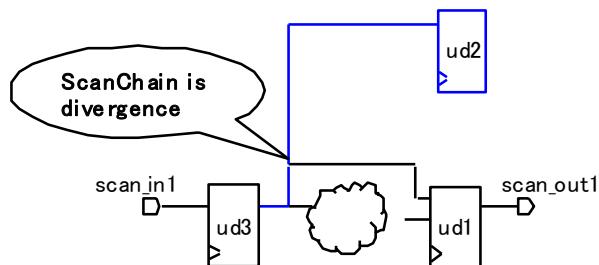
- non-arrival in SCAN-OUT. (ScanChain is divided.)**
Not reach to scan-out. The end of register is **ud2**.

The scan chain is divided.
Or it is error because the chain with the problem cannot arrive in SCAN-OUT.



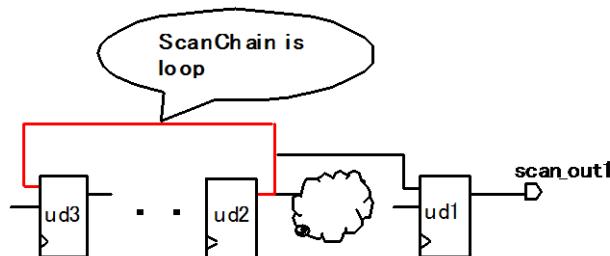
- ScanChain is diverged.**

There are 2 path of scan chain.
The register is (**ud2**).



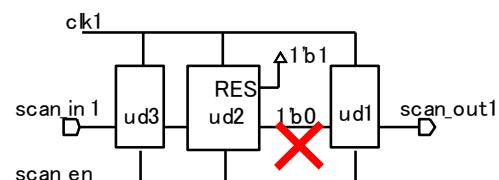
- One F/F is checked twice by junction or loop of ScanChain.**

Already exists at scan chain. The register is (**ud3**) loop.



- F/F included in ScanChain is fixed by set/reset signal.**

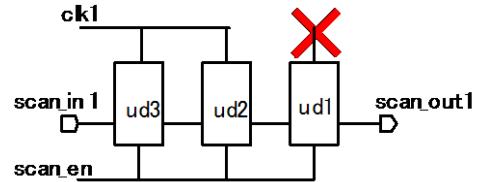
The register(**ud2**) is fixed by set/reset.



- Clock does not propagate. Or clock is different.

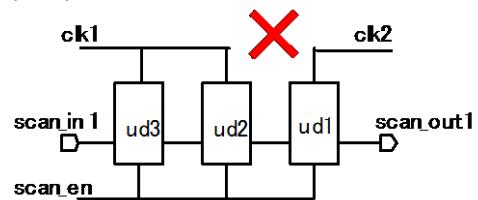
Example1) Clock does not propagate.

F/F(**ud1**) can not find clock.



Example2) Clock is different.

Clock(**clk1**) of F/F(**ud2**) is not same as clock(**clk2**) of F/F(**ud1**).

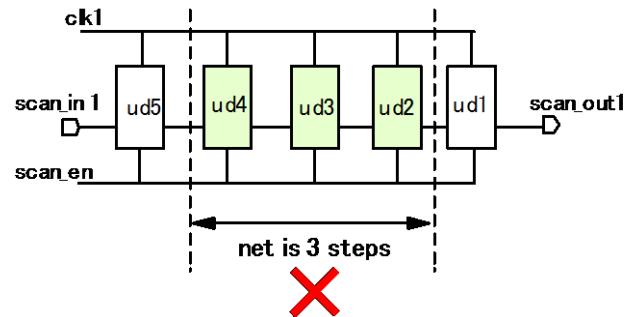


- MAX_BITS exceed the specified value.

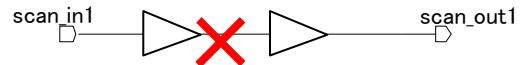
Example)

`set_numerical_value POST_DFT_MAX_BITS 2 ;
-> MAX_BITS is set to 2, but it is 3 in netlist.`

3 of **chain_1_1** is over MAX_BITS(2).

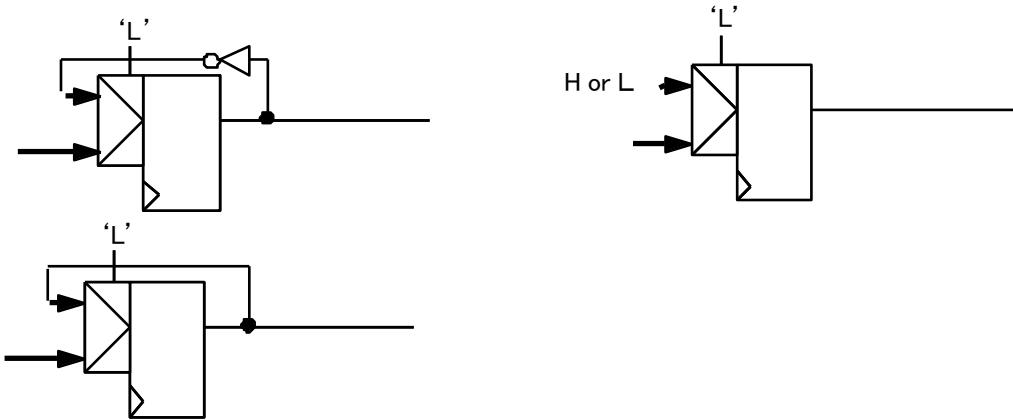


- A register does not exist between SCAN-IN and SCAN-OUT



5.5.4 DFT401-3

There is SCAN-FF which is not included in ScanChain.
But signal is fixed, and SCAN-FF using as Normal F/F is exclude.
Follows are SCAN-FF, but consider it to be Normal F/F.



5.5.5 DFT401-4

The difference of the netlist and the input SCAN_DEF file are compared.
(Comparison of ScanChain at pre and post Layout)

When there is not the error of DFT401-1 and DFT401-2, please check this.

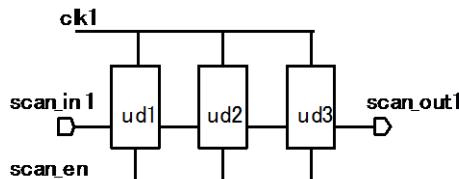
<processing summary>

- (1)SCAN_DEF make from the internal net.
- (2)The comparison of internal net SCAN_DEF and input SCAN_DEF
 - Is there information of internal net SCAN_DEF in input SCAN_DEF?
 - Is there information of input SCAN_DEF in internal net SCAN_DEF?

<The check that was based on the netlist>

- There is not the combination of START and STOP in input SCAN_DEF.

Example) Can not find START(**ud1**) and STOP(**ud3**) of netlist in SCANDEF(**chain_1_1**).

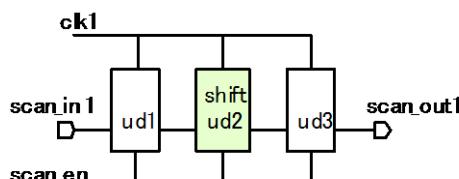


```

<SCAN_DEF>
DESIGN top :
SCANCHAINS 1 :
- chain_1_1
+ START ud1 SO
+ FLOATING
ud2 (IN SIN) ( OUT SO )
+ STOP ud3 SIN
+ PARTITION partition_clk1 MAXBITS 1 :
END SCANCHAINS
END DESIGN
  
```

- There is not the instance that was defined by ORDERED in input SCAN_DEF.
Or the order is different.

Example) Can not find ORDERED(**ud2**) of netlist in SCANDEF(**chain_1_1**).

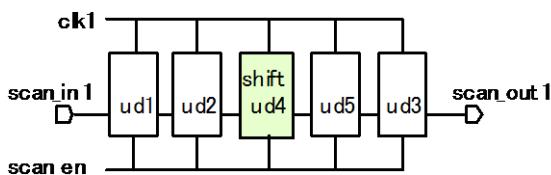


```

<SCAN_DEF>
DESIGN top :
SCANCHAINS 1 :
- chain_1_1
+ START ud1 SO
+ STOP ud3 SIN
+ PARTITION partition_clk1 MAXBITS 0 :
END SCANCHAINS
END DESIGN
  
```

- The instance that was defined by ORDERED is different from input SCAN_DEF.

Example) ORDERED(from START to **ud4**) of netlist is different in SCANDEF(**chain_1_1**). The net has **ud2**.

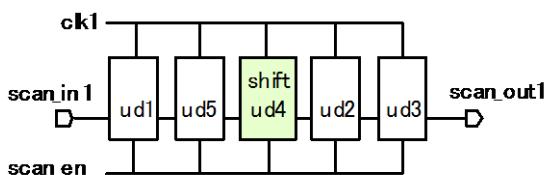


```

<SCAN_DEF>
DESIGN top ;
SCANCHAINS 1 ;
- chain_1_1
+ START ud1 Q
+ ORDERED
ud4 (IN DATA ) ( OUT Q )
+ FLOATING
ud5 (IN SIN ) ( OUT SO )
+ STOP ud3 SIN
+ PARTITION partition_ckl1 MAXBITS 2 ;
END SCANCHAINS
END DESIGN
  
```

- The instance that was defined by ORDERED is different from input SCAN_DEF.

Example) ORDERED(from **ud4** to STOP) of netlist is different in SCANDEF(**chain_1_1**). The net has **ud2**.

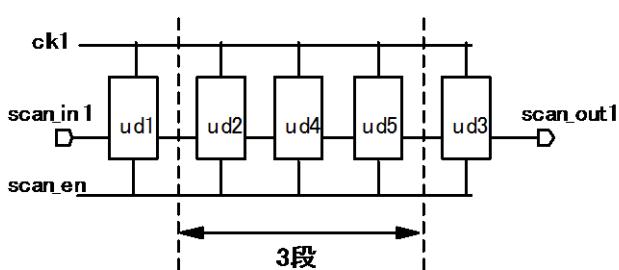


```

<SCAN_DEF>
DESIGN top ;
SCANCHAINS 1 ;
- chain_1_1
+ START ud1 SO
+ ORDERED
ud5 (IN SIN ) ( OUT Q )
ud4 (IN DATA ) ( OUT Q )
+ STOP ud3 SIN
+ PARTITION partition_ckl1 MAXBITS 2 ;
END SCANCHAINS
END DESIGN
  
```

- MAX_BITS exceed value of input SCAN_DEF.

Example) MAX_BITS(3) of netlist exceeded MAX_BITS(1) of SCAN_DEF(**chain_1_1**).

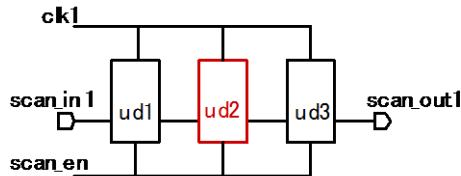


```

<SCAN_DEF>
DESIGN top ;
SCANCHAINS 1 ;
- chain_1_1
+ START ud1 Q
+ FLOATING
ud2 (IN SIN ) ( OUT SO )
+ STOP ud3 SIN
+ PARTITION partition_ckl1 MAXBITS 1 ;
END SCANCHAINS
END DESIGN
  
```

- There is not instance that was defined by FLOATING in input SCAN_DEF.

Example) Can not find FLOATING(**ud2**) of netlist in SCANDEF(chain_1_1).

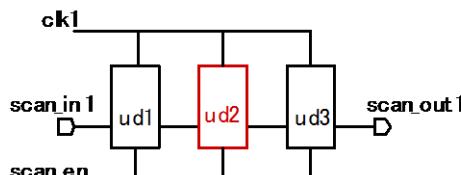


```

<SCAN_DEF>
DESIGN top ;
SCANCHAINS 1 ;
- chain_1_1
+ START ud1 SO
+ STOP ud3 SIN
+ PARTITION partition_clk1 MAXBITS 0 ;
END SCANCHAINS
END DESIGN
  
```

- There is not instance that was defined by FLOATING in same PARTITION of input SCAN_DEF.

Example) PARTITION of FLOATING(**ud2**) in netlist is **partition_clk1**.
But PARTITION in SCAN_DEF(chain_1_1) is **partition_clk2**.

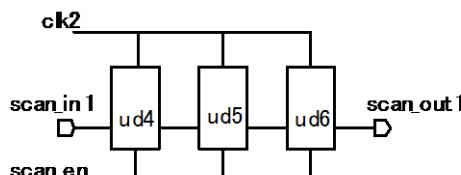


```

<SCAN_DEF>
DESIGN top ;
SCANCHAINS 2 ;
- chain_1_1
+ START ud1 SO
+ STOP ud3 SIN
+ PARTITION partition_clk1 MAXBITS 0 ;

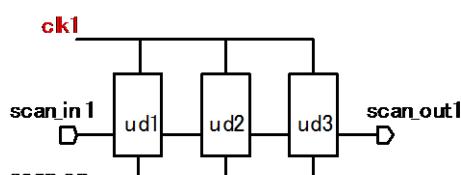
- chain_2_1
+ START ud4 SO
+ FLOATING
ud2 (IN SIN) ( OUT SO )
ud5 (IN SIN) ( OUT SO )
+ STOP ud6 SIN
+ PARTITION partition_clk2 MAXBITS 2 ;

END SCANCHAINS
END DESIGN
  
```



- The partition name of the combination at START and STOP is different from input SCAN_DEF.

Example) PARTITION at START(**ud1**) and STOP(**ud3**) is **partition_clk1** in netlist.
But PARTITION is **partition_clk2** in SCAN_DEF(chain_1_1).
The clock of the partition name is different.



```

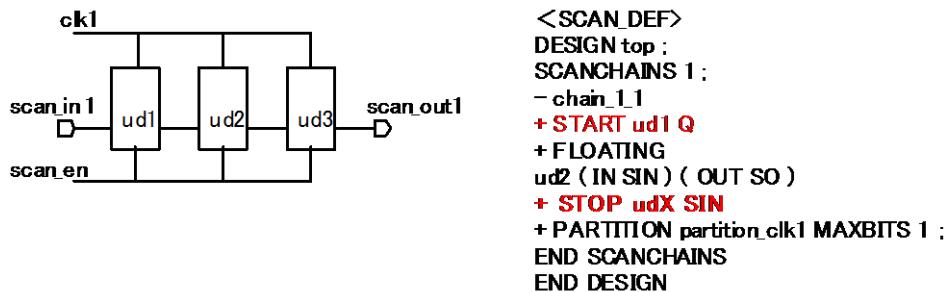
<SCAN_DEF>
DESIGN top ;
SCANCHAINS 1 ;
- chain_1_1
+ START ud1 Q
+ FLOATING
ud2 (IN SIN) ( OUT SO )
+ STOP ud3 SIN
+ PARTITION partition_clk2 MAXBITS 1 ;

END SCANCHAINS
END DESIGN
  
```

<The check that was based on input SCAN_DEF>

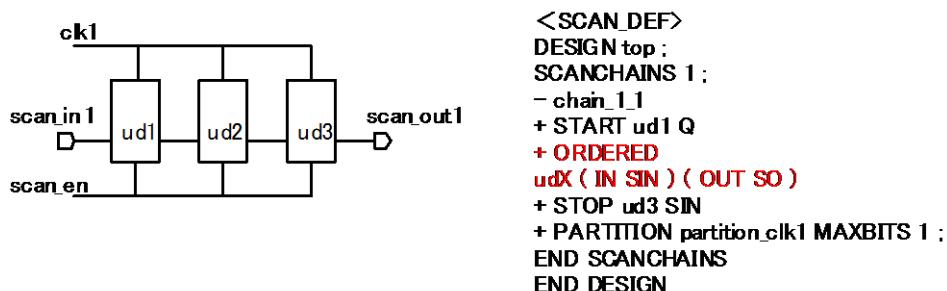
- There is not the combination of START and STOP in netlist.

Example) Can not find START(**ud1**) and STOP(**udX**) of SCANDEF(**chain_1_1**) in netlist.



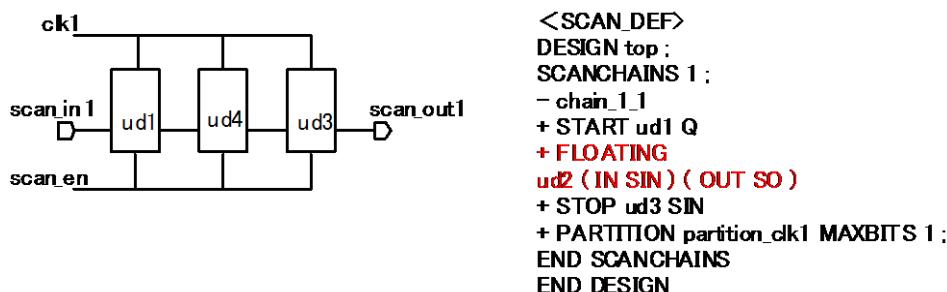
- There is not the instance that was defined by ORDERED in netlist.
Or the order is different.

Example) Can not find ORDERED(**udX**) of SCANDEF(**chain_1_1**) in netlist.



- There is not instance that was defined by FLOATING in netlist.
Or there is not it in same PARTITION.

Example) Can not find FLOATING(**ud2**) of SCAN_DEF(**chain_1_1**) in netlist.



5.5.6 DFT401-5

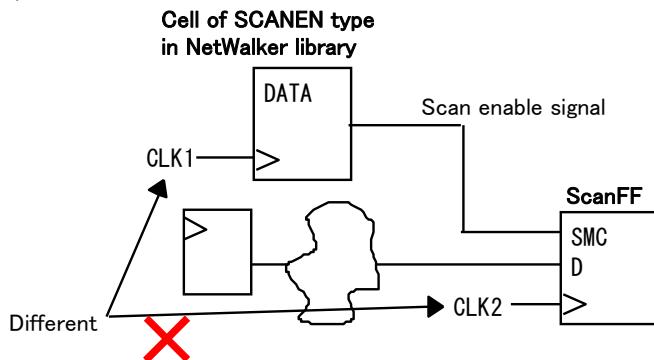
There is the problem that the clock of FF or the clock of cell for exclusive use of SanEable connects to SMC pin is different from scan FF.

Note:

In DFT013-9 and DFT401-5, the use of ScanEnable generation cell is a premise.

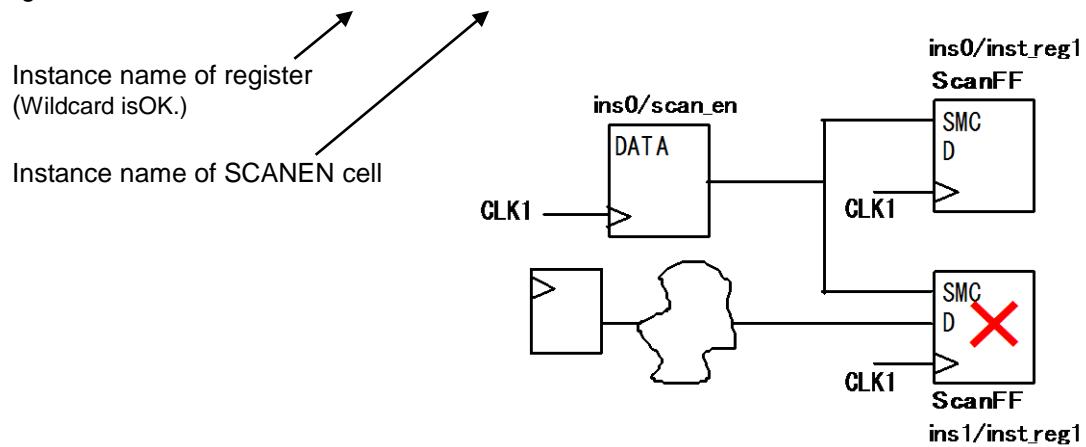
When AC-SCAN is executed only by Broadside method, please exclude check by -CANCEL_401_5.

Example1)

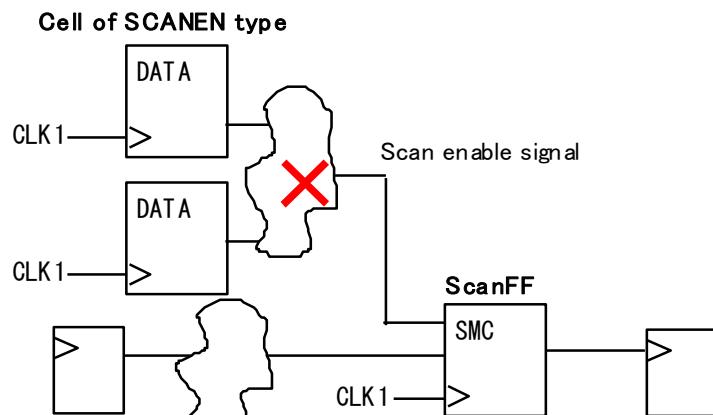


Example2) Connection is different from SCANEN_CONNECT.

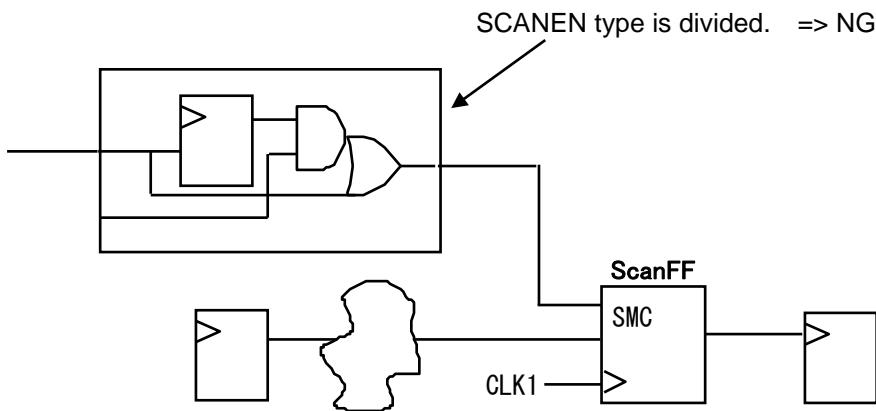
```
set_strings SCANEN_CONNECT ins0/* ins0/scan_en ;
set_strings SCANEN_CONNECT ins1/* ins1/scan_en ;
```



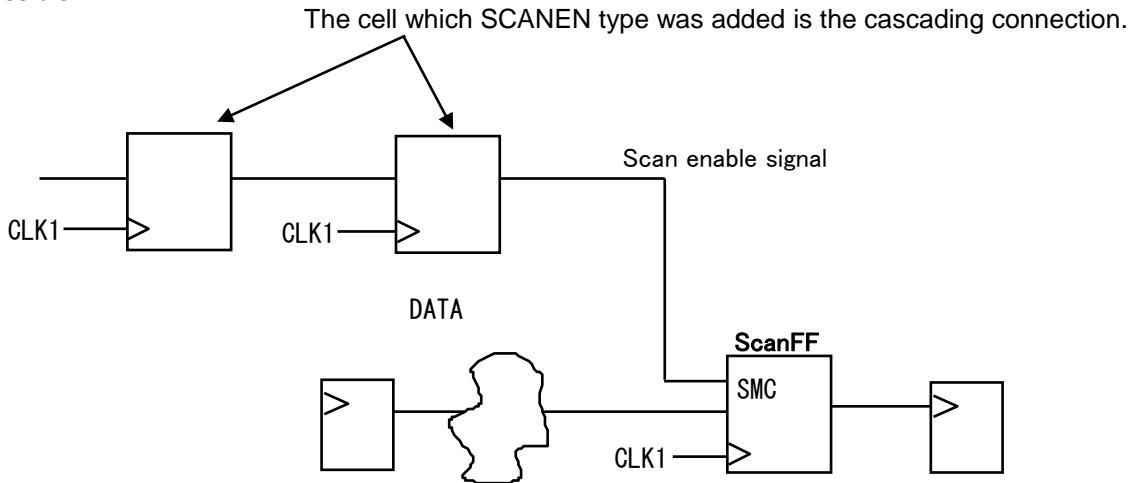
Example3) The cell of many SCANEN types is connected.



Example4) SMC terminal of scan FF is connected to the output of SCANEN type cell. Or it is connected to the other than external port.



Example5) The output of SCANEN type cell is not connected to SMC terminal of scan FF or the memory that test is possible.

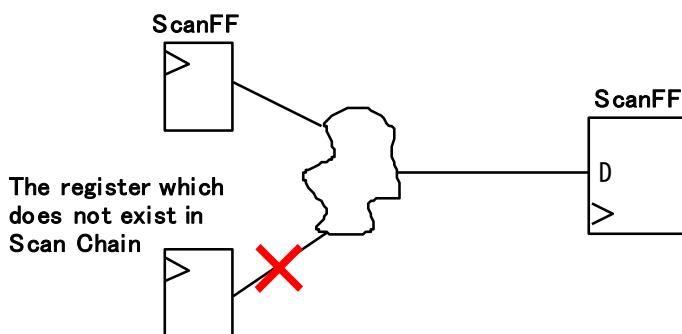


Note: Scan FF is FF existing on the scan chain.

5.5.7 DFT401-6

The register which does not exist in scan chain is connected at capture mode.

Example1)



Specify the test control register to exclude as follows in the PT_SHELL file.
`set_strings DFT_CONTROL_REG < instance of module or register > ;`

5.5.8 DFT401-7

When the FF on the scan chain is controlled with the clock which was supplied from MUX of different select_dc, the timing is not guaranteed at test mode. Therefore, it is necessary to separate the scan chain.

As substitution for “set_case_analysis 0 select_dc” which is the specification of the signal which change over TCK clock, specify the following.

```
set_strings SELECT_DC select_dc 1 TCK;
The scan chain is separated.
```

```
create_clock -name TCK tck
create_clock -name AC_CLK ac_clk
set_strings POST_DFT scan_in1 scan_out1 ;
set_strings SCAN_EN scan_en1 1;
set_input_delay 1.0 -clock clk1 scan_en1;
set_strings SELECT_DC select_dc 1 TCK;
#set_case_analysis 0 select_dc ;
```

<SCANDEF(before)>

- **chain_75_1**
- + START axistat3c/am211_reg_19 SO
- + FLOATING
- axistat3c/am211_reg_2 (IN SIN) (OUT SO)
- axistat3c/am211_reg_20 (IN SIN) (OUT SO)
- :
- axistat3c/am222_reg_9 (IN SIN) (OUT SO)
- axistat3c/arb0_axstatn_sr0_reg_0 (IN SIN) (OUT SO)**
- axistat3c/arb0_axstatn_sr0_reg_1 (IN SIN) (OUT SO)
- :
- axistat3c/arb0_axstatn_sr0_reg_27 (IN SIN) (OUT SO)
- + STOP axistat3c/arb0_axstatn_sr0_reg_28 SIN ;

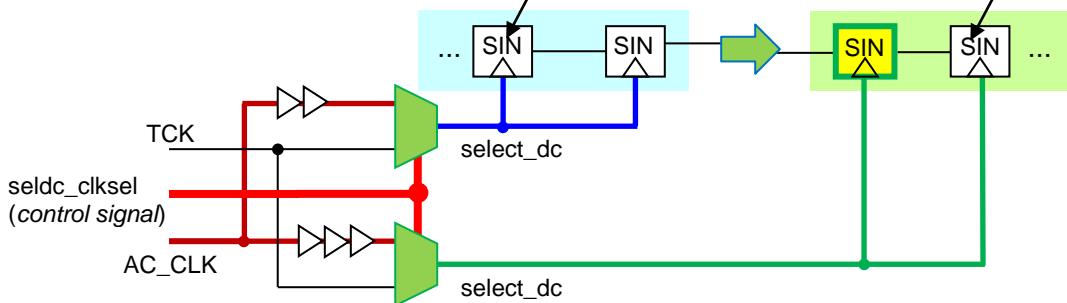
<SCANDEF(after)>

- **chain_75_1_1**

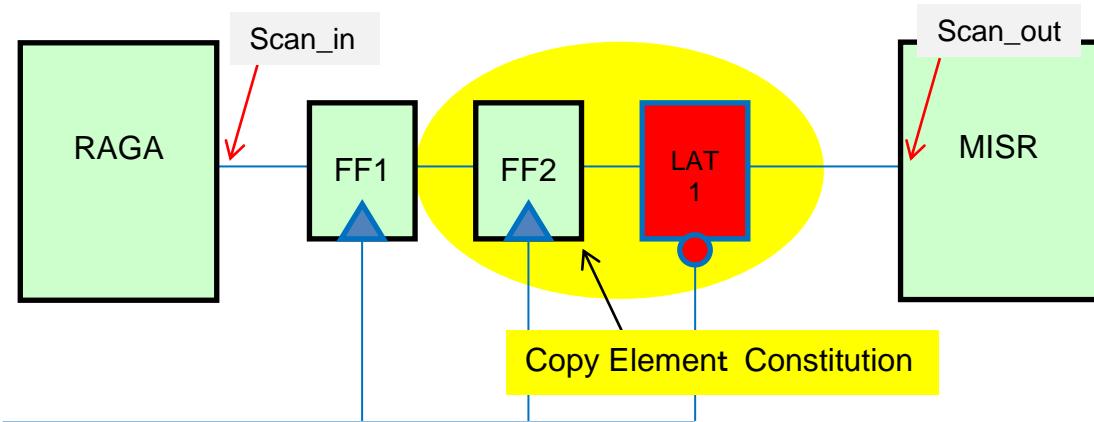
- + START axistat3c/am211_reg_19 SO
- + FLOATING
- axistat3c/am211_reg_2 (IN SIN) (OUT SO)
- axistat3c/am211_reg_20 (IN SIN) (OUT SO)
- :
- +STOP axistat3c/am222_reg_9 SIN ;**

- **chain_75_1_2**

- + START axistat3c/arb0_axstatn_sr0_reg_0 SO**
- axistat3c/arb0_axstatn_sr0_reg_1 (IN SIN) (OUT SO)
- :
- axistat3c/arb0_axstatn_sr0_reg_27 (IN SIN) (OUT SO)
- + STOP axistat3c/arb0_axstatn_sr0_reg_28 SIN ;



<<-DFT401_OLD_SCANDEF_MODE option>>



```
set_strings POST_DFT {RAGA/Y} {MISA/A} ;
```

SCANDEF of old format is output by this option. F/F connected to the specified net becomes START/END.

< Caution points of old format >

If the last is Copy Element, SCANDEF is not output correctly.

The definitions of more than two components are necessary for ORDERED.

<Scandef file (-DFT401_OLD_SCANDEF_MODE option) >
- chain_1_1
+ START FF1 SO
+ ORDERED
FF2 (IN SIN) (OUT SO) ← violation of format (one component)
+ STOP LAT1 DATA
+ PARTITION partition_clk1 MAXBITS 1 ;

< Scandef file (default) >
- chain_1_1
+ START PIN RAGA/Y ← definition value of POST_DEF
+ FLOATING
FF1 (IN SIN) (OUT SO)
+ ORDERED
FF2(IN SIN) (OUT SO)
LAT(IN DATA) (OUT Q) # COPY
+ STOP PIN MISR/A ← definition value of POST_DEF
+ PARTITION partition_clk1 MAXBITS 3 ;

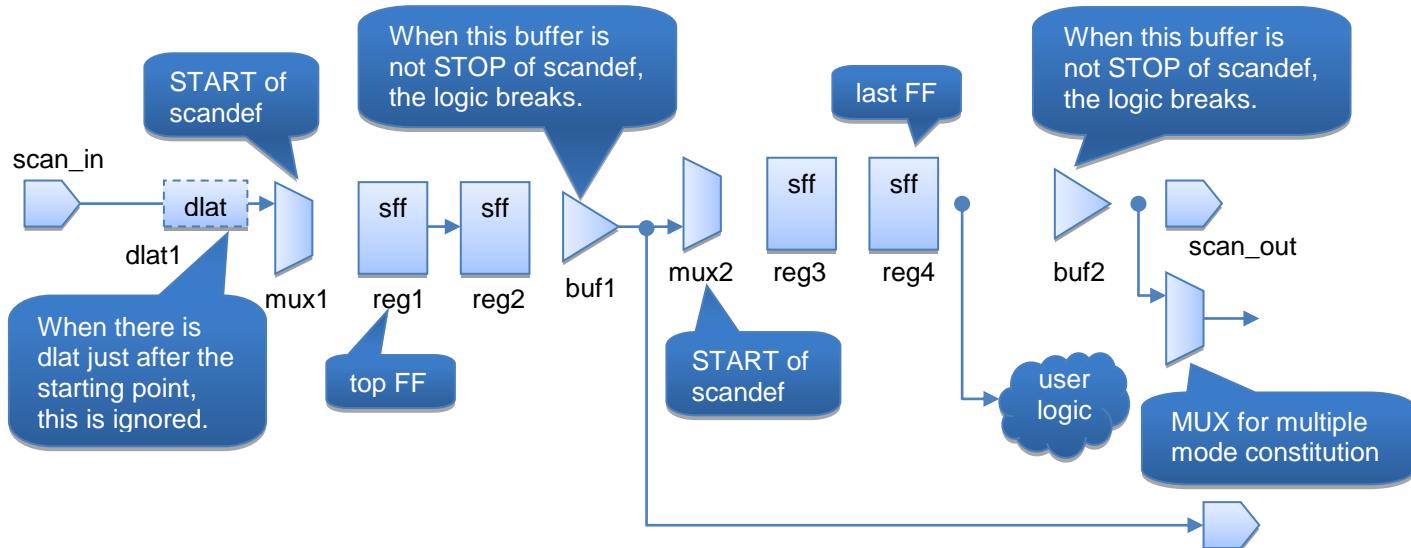
(1) Tessent new feature (hierarcal scan insertion) correspondence

Because the mounting of multiple scan modes is enabled when you execute the new feature of Tessent, this converts into the chain structure built by a new feature. If you use this function, specify the following.

```
set_strings DFT401_START_END_REDEFINE yes
set_strings DFT401_MUX_SEPA yes
```

If specify is omitted, the following problem may occur.

When the chain trace of a certain mode was executed, there is Buffer (or Mux) of other mode constitution on the chain. If scandef is not created at a unit of these Buffer (or Mux), the logic of other modes breaks.

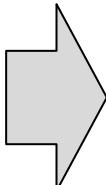


```
set_strings POST_DFT scan_in scan_out
set_strings DFT401_START_END_REDEFINE yes
set_strings DFT401_MUX_SEPA yes
```

← Move the positions of START and END to inside by new function.
← Divide by selector cell.

<Old specifications>

```
- chain_1_1
+ START PIN scan_in
+ ORDERED
dlat1 ( IN DATA ) ( OUT Q )
reg1 ( IN SIN ) ( OUT Q )
+ FLOATING
reg2 ( IN SIN ) ( OUT Q )
reg3 ( IN SIN ) ( OUT Q )
reg4 ( IN SIN ) ( OUT Q )
+ STOP PIN scan_out
+ PARTITION partition_CLK1 MAXBITS 3 ;
```



<New specifications>

```
- chain_1_1
# START scan_in
+ START PIN mux1 Y
+ FLOATING
reg1 ( IN SIN ) ( OUT Q )
reg2 ( IN SIN ) ( OUT Q )
+ STOP PIN buf_ins1 A
+ PARTITION partition_CLK1 MAXBITS 2 ;
- chain_1_2
+ START PIN mux2 Y
+ FLOATING
reg3 ( IN SIN ) ( OUT Q )
reg4 ( IN SIN ) ( OUT Q )
+ STOP PIN buf2 A
# STOP PIN scan_out
+ PARTITION partition_CLK1 MAXBITS 2 ;
```

5.6 RS Chain Check

The memory of the T28 product is using RS(Resume Standby) function, and the bits are more than 560k. In this product, time sharing movement is necessary to prevent the malfunction caused by peek electric current flowing at the return from RS (Resume Standby) mode. Please use RSChain connection tool to perform time sharing of RS chain. The use of the exclusive cell (umbtx_rschain_selector) is necessary for the selector of RS.

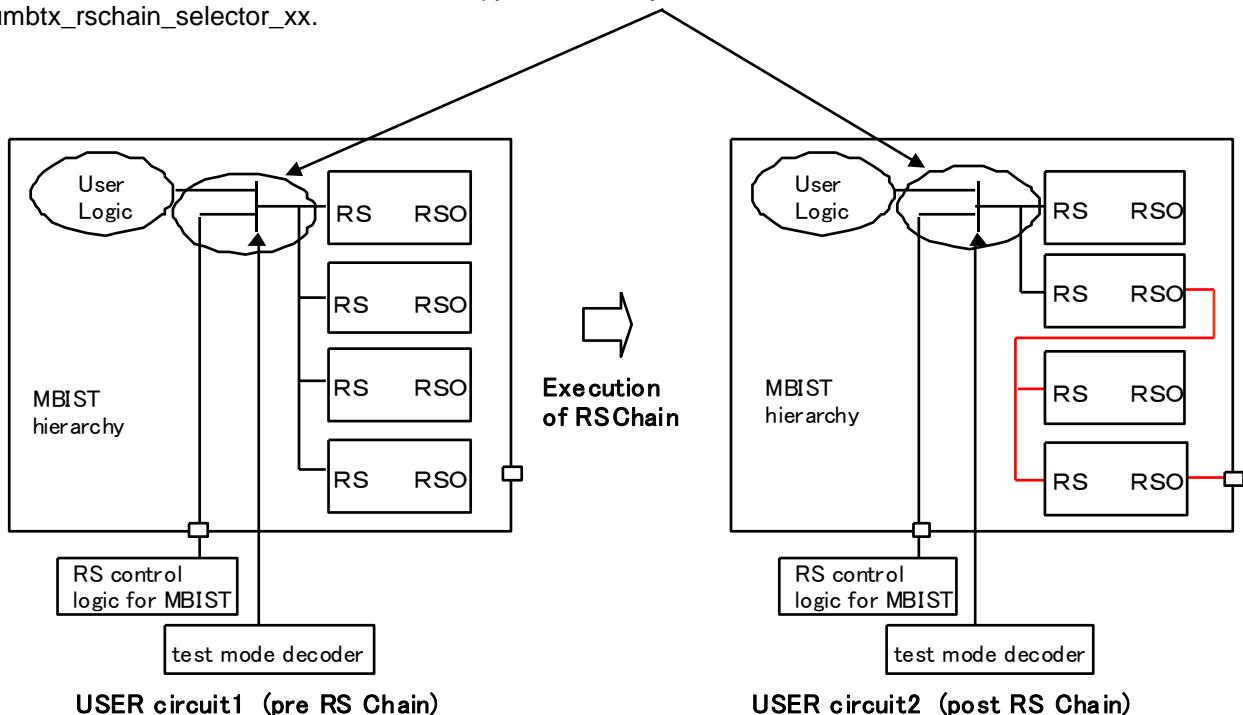
< Design flow >
DFTcheck (-PREMINORI mode)
↓
USER circuit1 design (Gate level) Uniquify of netl is necessary!
↓
Execution of RSChain connection tool (USER circuit2 generation)
Specification by PTSHELL (set_strings RSChain mbist1 rs_chain_in rs_chain_out;)
:
↓
DFTcheck :RS Chain Check (-PREMINORI mode)
↓
Timing check of RS signal
↓
Equivalence check
↓
Addition process of DFT
↓
DFTcheck :RS Chain Check (-POST mode)

RS control circuit (umbtx_rschain_selector)

```
<Verilog_lib>
module umbtx_rschain_selector ( clk_scan, rs_in,
chain_in,mbist, scan, obs_rs, rs_out );
input    clk_scan, rs_in, chain_in, mbist, scan ;
output   obs_rs, rs_out;
reg     obs_rs;
assign irs = mbist ? chain_in : rs_in;
assign rs_out = (~scan) && irs;
always @ (posedge clk_scan) begin
obs_rs <= irs;
end
endmodule
```

<Note>

umbtx_rschain_selector must maintain a hierarchy at the time of composition. Furthermore, it must estimate the selector. When RSChain is executed, uniqfy is necessary. And an umbtx_rschain_seletor module name must be umbtx_rschain_selector_xx.



(1) DFT501-1 Report of RS chain list

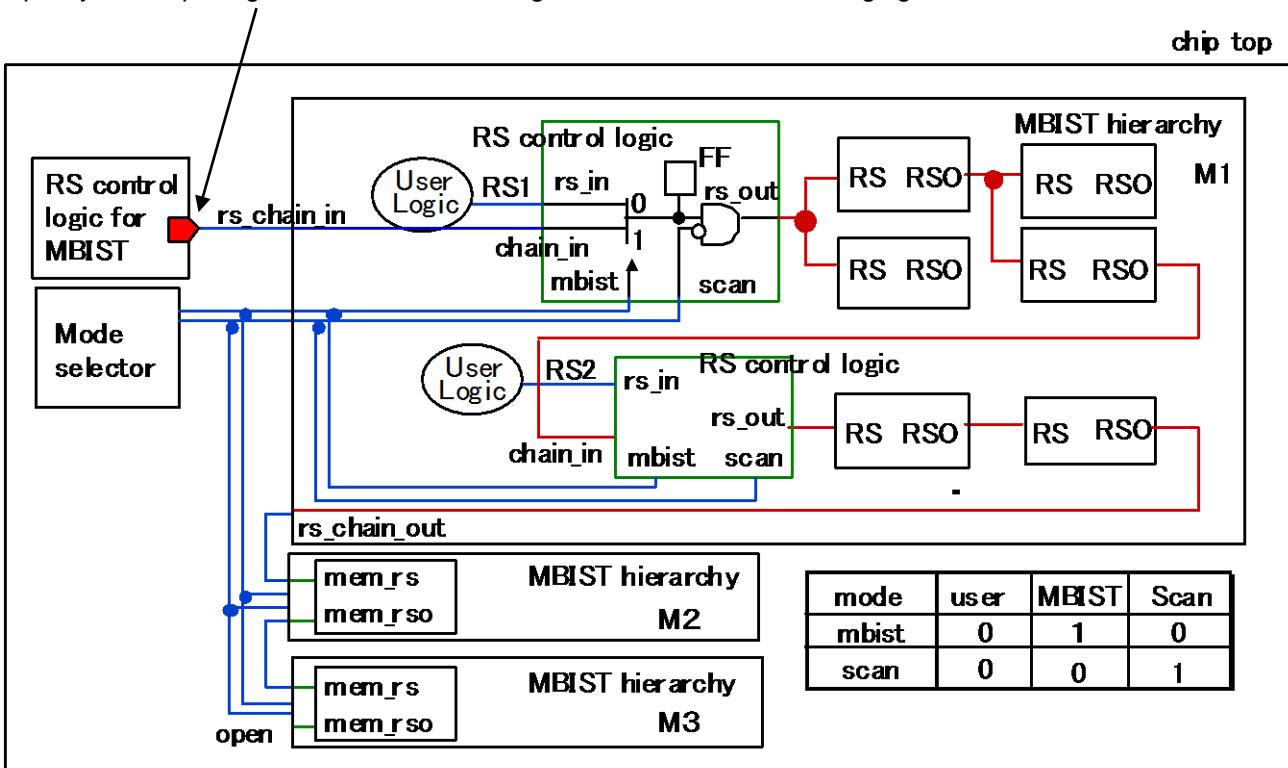
Time sharing movement in constant memory bit is necessary to prevent the malfunction caused by peek electric current flowing at the return from RS (Resume Standby) mode. The number of the steps beyond specified memory bit is displayed.

When DFT501_MBIST_RS is specified in PTSHELL file, the chain list of RS is output.

Example)

```
create_clock -period 8 -name CLKS -waveform { 2 6 } clks ;
set_numerical_value RS_MAX_BIT 150000 ;
set_strings DFT501_MBIST_RS MODEREG/mbist_rs ;
```

Specify the output signal of the RS control logic for MBIST of the following figure in DFT501_MBIST_RS.



When the chain beyond the power supply interception area was created, the unnecessary isolator cell becomes necessary and becomes the problem of power supply interception check.

Because the chain for every power supply interception area needs, please be careful.

< Way of looking at message >

INFO DFT501 -1: RS chain list

Start (rs_chain_in)	level	blockNumber	InstancePin(CellName)	Clock	Date	Addr	Bit
---------------------	-------	-------------	-----------------------	-------	------	------	-----

<<Mux:A.UMBTX(VERIFIC_MUX)>>

+ 0 A.0.i0.RS(BSPA48PM40203ZZAZZ) clk(CLKS) data(32) addr(11) bit(65536)

+ 0 0 A.i0.RS(BSPA48PL08082ZZAZZ) clk(CLKS) data(8) addr(7) bit(1024)

+ <B.UMBTX2.i3.a1(VERIFIC_MUX)>
BlockNumber=0 bit(199680)

<<Mux:B.UMBTX(VERIFIC_MUX)>>

+ 1 1 B.i0.RS(BSPA48PL10102ZZAZZ) clk(CLKS) data(16) addr(8) bit(4096)

BlockNumber=1 bit(4096)

+ 2 2 B.i0.RS(BSPA48PL10102ZZAZZ) clk(CLKS) data(16) addr(8) bit(4096)

BlockNumber=2 bit(4096)

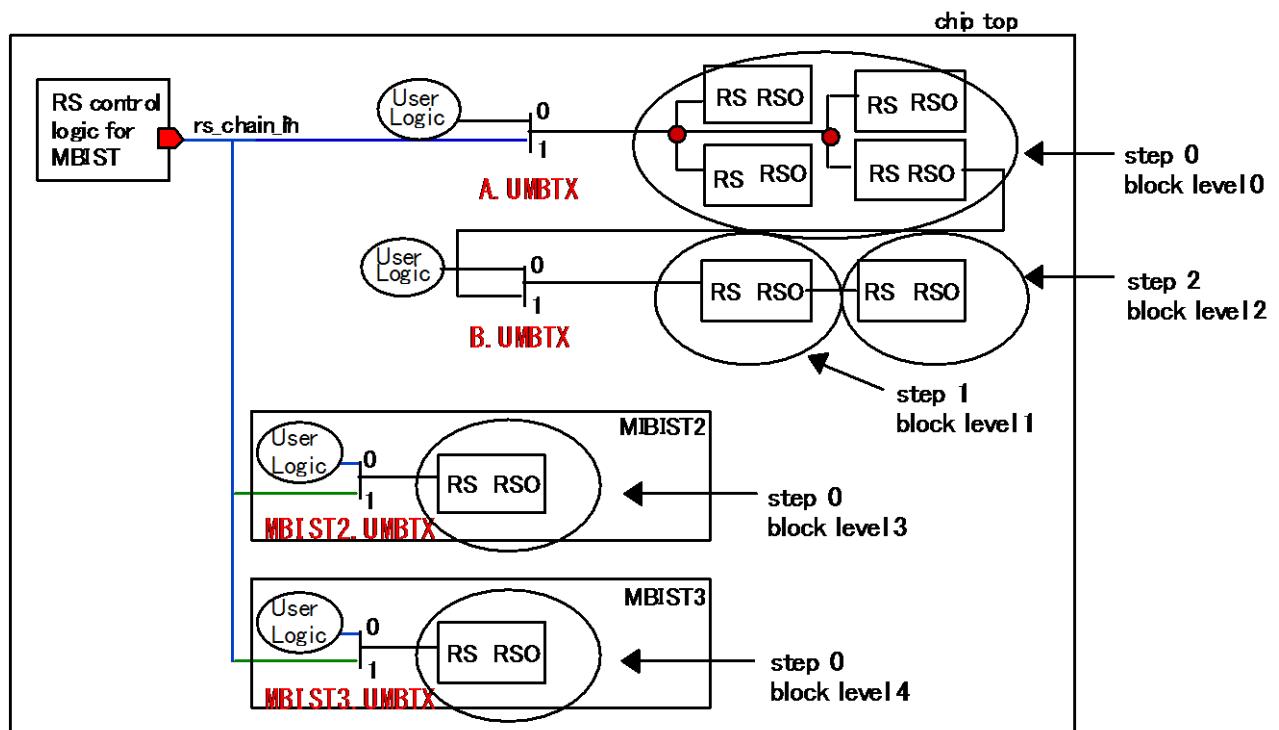
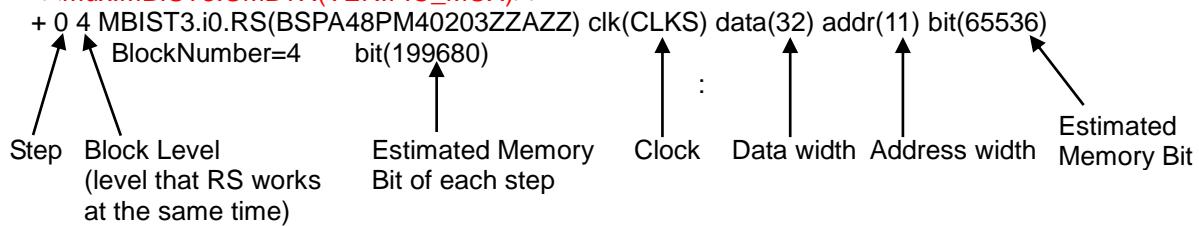
<<Mux:MBIST2.UMBTX(VERIFIC_MUX)>>

+ 0 3 MBIST2.i0.RS(BDPA48P2201A1ZZ0ZZ) clk(CLKS) data(26) addr(8) bit(6656)

BlockNumber=3 bit(199680)

<<Mux:MBIST3.UMBTX(VERIFIC_MUX)>>

+ 0 4 MBIST3.i0.RS(BSPA48PM40203ZZAZZ) clk(CLKS) data(32) addr(11) bit(65536)



(2) DFT501-2 Specified value check of memory Bit

Time sharing movement in constant memory bit is necessary to prevent the malfunction caused by peek electric current flowing at the return from RS (Resume Standby) mode. The number of the steps beyond specified memory bit is displayed.

This check needs specification of set_strings DFT501_MBIST_RS in PTSHELL file.

Example)

```
set_numerical_value RS_MAX_BIT 150000 ; ← Default is 560K.
```

ERROR DFT501 -2: RS chain check

No. error (No.) reason

1 level=0 over bit max(150000) bit(199680)

In addition, if the number of RS exceeds 10 steps, the following error is output. Because 10 steps or more are unexpected, please talk with (Memory IP Development Department).

ERROR DFT501 -2: RS chain check

No. error (No.) reason

1 over 10 step (25)

(3) DFT501-3 Check of memory excluded from RS chain list

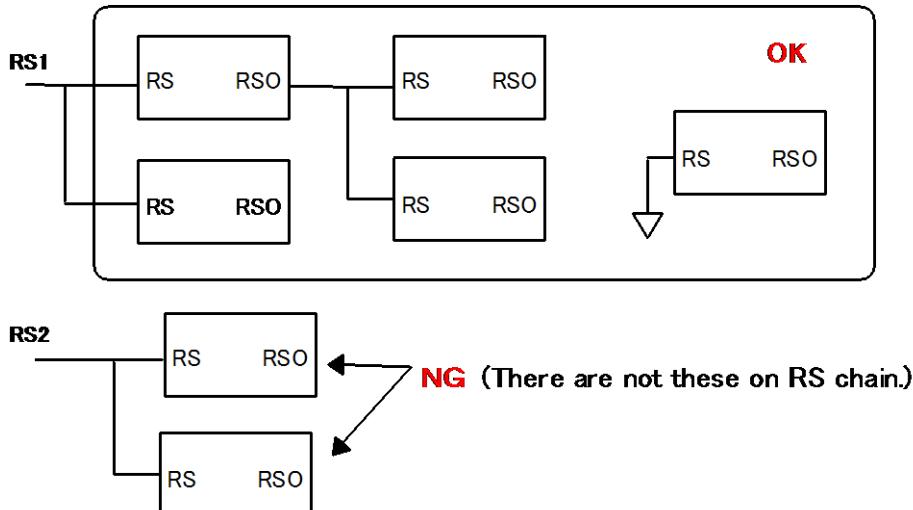
This is checked whether memory having the RS pin that satisfies one of the following conditions.

- It does not exist on RS chain and that logic is not fixed Low.
- It exists on RS chain and that logic is fixed Low.

This check needs specification of set_strings DFT501_MBIST_RS in PTSHELL file.

Example)

```
set_strings DFT501_MBIST_RS RS1 ;
```



(4) DFT501-4 Passage point check of RS chain

This is checked whether the start signal on RS chain arrives at the end signal.

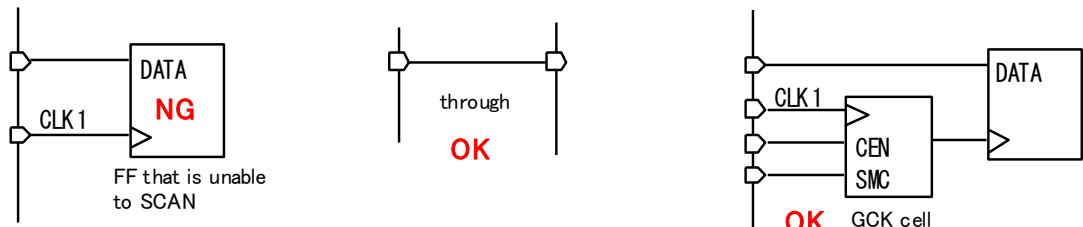
This check needs specification of set_strings DFT501_MBIST_RS_PATH in PTSHELL file.

5.7 Check Items for -CHECK_601 Option

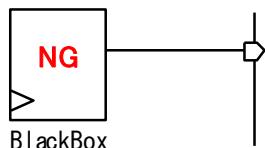
The external ports which become the digital hard macro detect trouble of the macro glue logic.
In addition, it must care so that the unknown does not propagate to the outside.
When -CHECK_601 option is specified at -MUXSCAN/-LBIST/-POST mode, this check is executed.

- (1) DFT601-1 Input port does not arrive at ScanFF and external port.

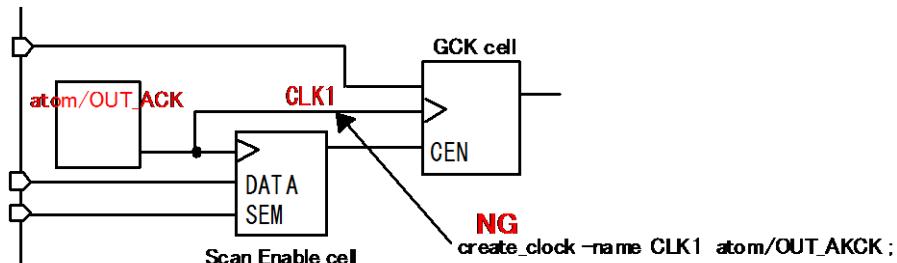
But the signal arriving at GCK or SCANEN cell is not checked.



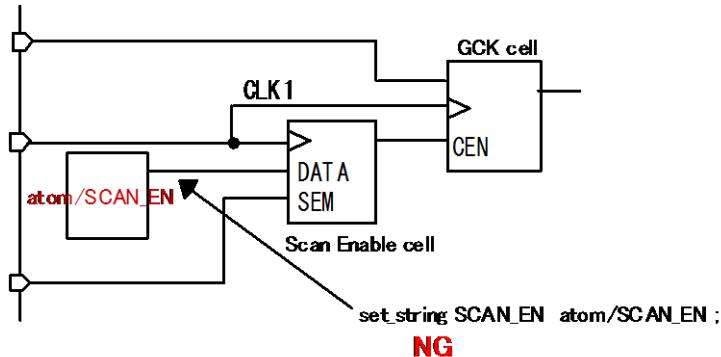
- (2) DFT601-2 The signal arriving at output port is not the output of ScanFF and external port.



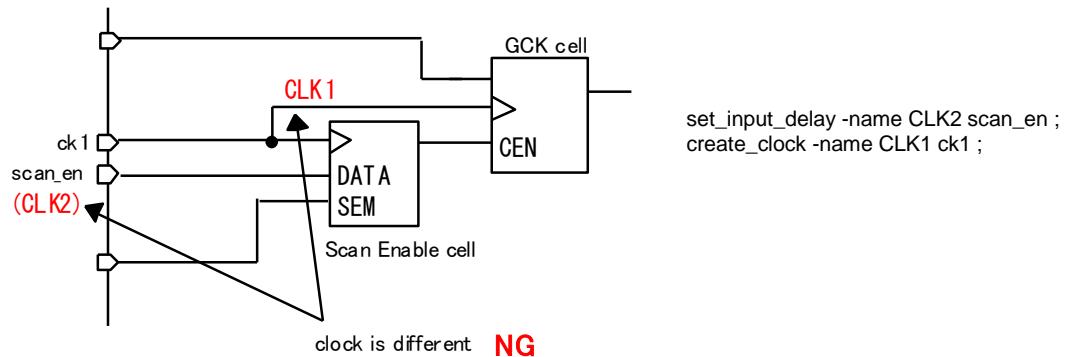
- (3) DFT601-3 The signal specified by create_clock is not external port.



- (4) DFT601-4 The signal specified by SCAN_EN is not external port.



(5) DFT601-5 The clock connected to the clock pin and DATA pin of the SCANEN cell is not same.



Note) Definition of ScanFF

- <PRE Scan> FF subject to scanning
- <POST Scan > FF existing on a scan chain

6. Error-analysis method

6.1 Debug command

The command was for analysis.

-TRACE_FROM/-TRACE_TO/-TRACE_DETAIL

If you specify the commands, DFTcheck

TCL debug commands have
the equal functions.
Please refer to Chapter 6.2.

-TRACE_LIMIT

(1) There are three kinds of traces.

<Mode 1> traces from a signal to a signal.

Trace is not traced more than a register.

Moreover, specification of -TRACE_DETAIL will output detailed information.

<Mode 2> traces from a signal.

Forward trace from a signal to a register or a port

<Mode 3> traces to a signal.

The backed race from a signal to a register or a port

In the case of mode 2 / mode 3, the number of search stages can be restricted by -TRACE_LIMIT.

The starting point, a end point: It can specify by the module port, the signal name, and a gate pin name.

A hierarchy pause is ".".

Example: b1.mul_29.U15.Y

(2) Display of gate instance (-TRACE_GATE_INFO gate_instance_name)

Two or more specification is possible.

TRACE GATE INFORMATION

** Information of instance (KKK) **

cell_name :(mi21d0)

<input> -----

i0	(D)(B)	Net(m1)	<===== (data type)(Restrictions value) Net(net name)
	from(HT_MPI_01.z Cell(an02d1))		<===== from(The element to drive)
i1	(D)(?)	Net(io1)	
	from(IO1.cin Cell(pc3d01d))		
s	(D)(1)	Net(s1)	
	from(external port s1)		

<output> -----

zn	(D)(?)	Net(m1_1)	<===== to(Fan-out element)
	to (M001.HT_MPI_02.a2 Cell(an02d1))		

6.2 TCL debug command (-TCL/-TCLD)

You can analysis, if -TCL/-TCLD is specified as a command.

“-TCL” specifies the file name which wrote debugging directions to the next.

“-TCLD” can do debugging interactively.

Since the screen of TCL rises, please input a command.

Example “-TCLD”

DFTcheck -TOP -TCLD

:

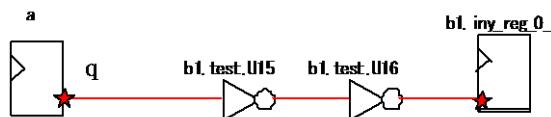
```
debug>trace -from a.q -to b1.iny_reg_0.d  
debug>exit
```

Example “-TCL”

DFTcheck -TOP -TCL test.tcl

:

```
<test.tcl>  
trace -from a.q -to b1.iny_reg_0.d
```



From : a.q
To : b1.iny_reg_0.d

```
+a.q (O) (DATA) (?)  
+b1.test.U15.A (TGAINV2XA) (I) (DATA) (?)  
+b1.test.U15.Y (TGAINV2XA) (O) (DATA) (?)  
+b1.test.U15.A (TGAINV2XA) (I) (DATA) (?)  
+b1.test.U15.Y (TGAINV2XA) (O) (DATA) (?)  
+b1.iny_reg_0.RB (TGADFF2XA) (I) (DATA) (?)
```

(1) Trace command

Name trace : Trace display
Format void trace ?-from gate_instance.pin? ?-to gate_instance.pin?
Function The path traced from the specification signal is displayed.
-from :Specify the terminal of the starting point.
-to :Specify the terminal of the end point.
-detail : The detailed information of search is outputted.
The starting point, a end point: It can specify by the module port, the signal name, and a gate pin name.
A hierarchy pause is "." Example: b1.mul_29.U15.Y

Return 0: OK 1: ERROR

Example

Trace about for two points. : trace -from xx.pin -to yy.pin
Trace from a specified signal to a register. : trace -from xx.pin
Back Trace from a specified signal to a register. : trace -to yy.pin

Note The net via register cannot trace.

Refer to Chapter 6.1 for output form.

Output form :

TRACE INFORMATION

From : Start pin

To : end pin

+instance_name.pin(cell_name)(attribute)(data type)(Restrictions value)
 +instance_name.pin(cell_name)(attribute)(data type)(Restrictions value)
 +instance_name.pin(cell_name)(attribute)(data type)(Restrictions value) [(net name)(inside moude net name)]?
 + instance_name.pin(cell_name)(attribute)(data type)(Restrictions value)
 :
 :

<attribute>

input is "I" and output is "O."

<data type>

if the clock signal has propagated. it becomes clock name,However, when the clock is reversed,~ is added to a clock name. A clock name is the name specified by the "create_clock" command.

if set/reset signal has propagated. it becomes "SET_RES". "D" is a data signal.

<Restrictions value> 1,0,?,B

1:high fixed

0:low fixed

?:don't fixed

B: The blocked state by fixed value.

The state where it was blocked cannot pass the path, when other signals are fixed at a gate. Moreover, the same result as the case where there is no timing arc at a gate

<net_name > output when only one of "From" or "To" is specified.

<inside module net name> output when it differs from Net name.

(2) gate command

Name gate : Gate information display
Format int gate gate_instance
Function The detailed information on a gate is outputted.
When “-detail” is specified by trace, the following is outputted about the gate on a path.
As for the net stepping over the hierarchy, net name (Net) in the highest hierarchy and net name (Net_org) connecting with cell directly are displayed.
Return 0: OK 1: ERROR
Example

gate a.KKK

```
<Result>
** Information of instance (a.KKK) **
cell_name :(mi21d0) Area name
<input> -----
    i0      (D)(B)    Net(m1)   Net_org(b)    <== (data type)( Restrictions value) Net(net name)
                from(HT_MPI_01.z Cell(an02d1))           <== from(drive cell)
    i1      (D)(?)    Net(io1)  Net_org(c)
                from(IO1.cin Cell(pc3d01d))
    s       (D)(1)    Net(s1)   Net_org(d)
                from(external port s1)

<output> -----
    zn      (D)(?)    Net(m1_1) Net_org(e)
                to (M001.HT_MPI_02.a2 Cell(an02d1)) <== to(fanout gate)
```

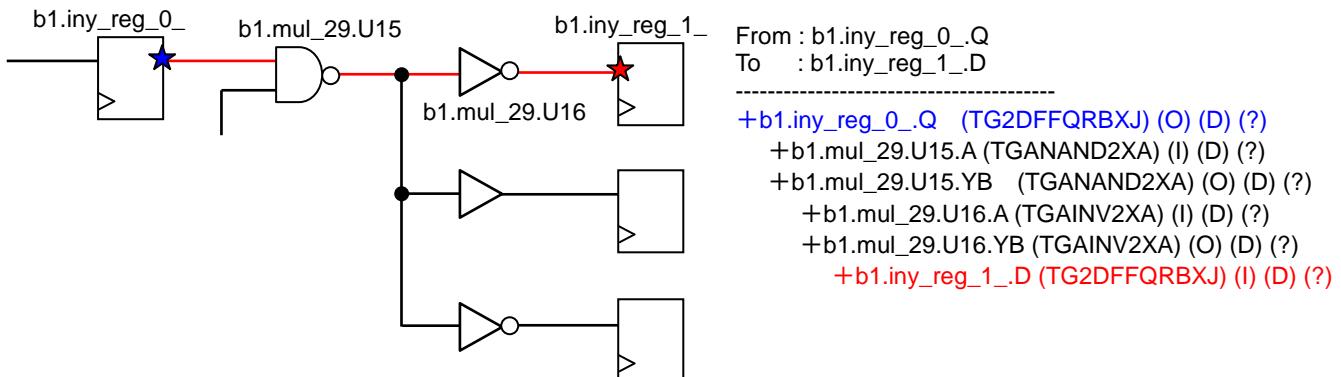
(3) net command

Name net : Net information display
Format int net net_name
Function Connection of a specification net is outputted.
Return 0: OK 1: ERROR
Example

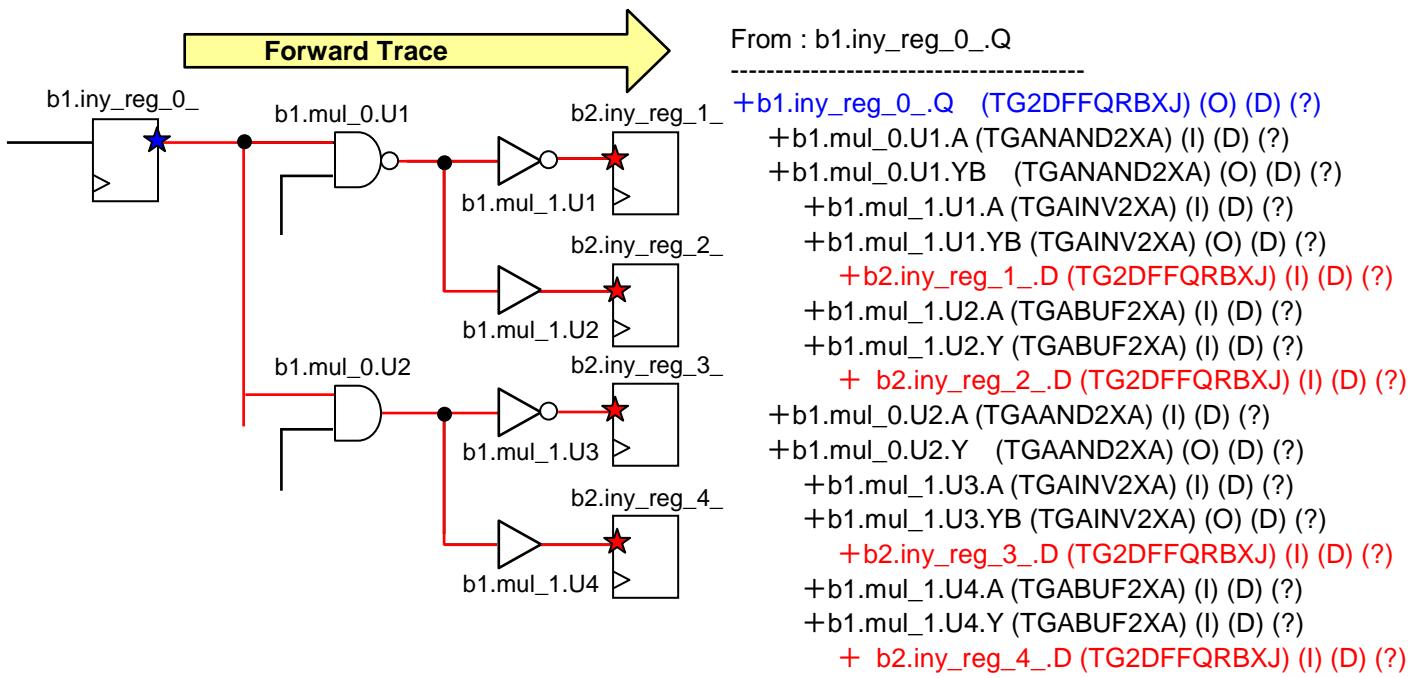
net O1

```
<Result>
** Information of net (O1) **
<< input gate >> ins_name ={tbuf03} cell_name =(TK1TBUFEXH)
```

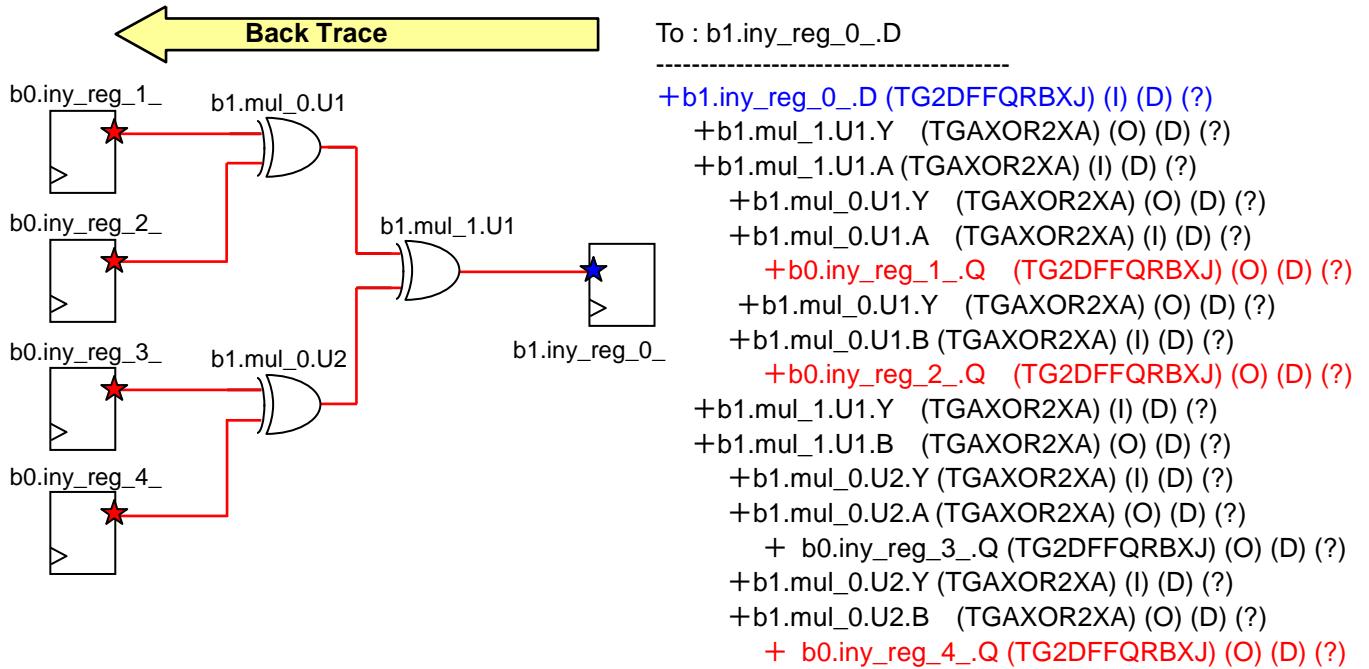
Example 1: trace -from b1.iny_reg_0_.Q -to b1.iny_reg_1_.D



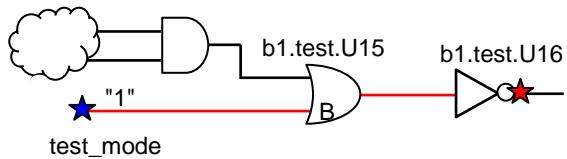
Example 2: trace -from b1.iny_reg_0_.Q



Example 3: trace -to b1.iny_reg_0_.D



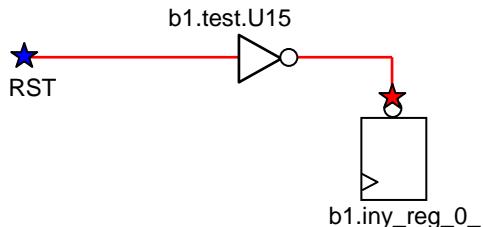
Example 4: trace -from test_mode -to b1.test.U16.Y



From : test_mode
To : b1.test.U16.Y

+test_mode (I) (D) (1)
+b1.test.U15.B (TGAOR2XA) (I) (D) (1)
+b1.test.U15.Y (TGAOR2XA) (O) (D) (1)
+b1.test.U16.A (TGAINV2XA) (I) (D) (1)
+b1.test.U16.YB (TGAINV2XA) (O) (D) (0)

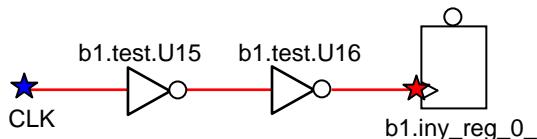
Example 5: trace -from RST -to b1.iny_reg_0_.RB



From : RST
To : b1.iny_reg_0_.RB

+RST (I) (SET_RES~) (?)
+b1.test.U15.A (TGAINV2XA) (I) (SET_RES~) (?)
+b1.test.U15.YB (TGAINV2XA) (O) (SET_RES~) (?)
+b1.iny_reg_0_.RB (TGADFF2XA) (I) (SET_RES~) (?)

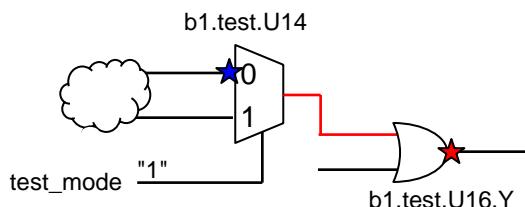
Example 6: trace -from CLK -to b1.iny_reg_0_.CLK



From : CLK
To : b1.iny_reg_0_.CLK

+CLK (I) (CLK) (?)
+b1.test.U15.A (TGAINV2XA) (I) (CLK) (?)
+b1.test.U15.YB (TGAINV2XA) (O) (CLK~) (?)
+b1.test.U16.A (TGAINV2XA) (I) (CLK~) (?)
+b1.test.U16.YB (TGAINV2XA) (O) (CLK) (?)
+b1.iny_reg_0_.CLK (TGADFF2XA) (I) (CLK) (?)

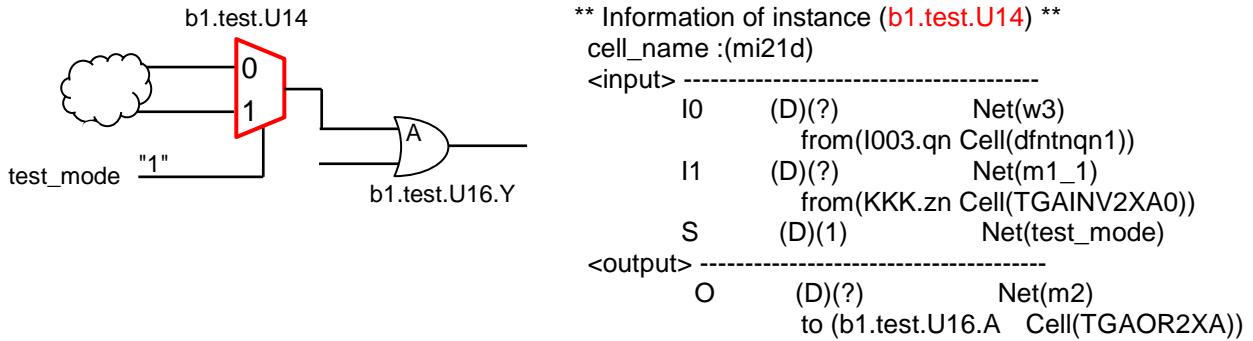
Example 7: trace -from b1.test.U14.A -to b1.test.U16.Y



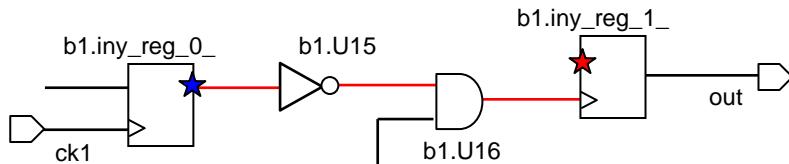
From : b1.test.U14.I0
To : b1.test.U16.Y

+b1.test.U14.I0 (TGAMUX2XA) (I) (D) (?)
+b1.test.U14.Y (TGAMUX2XA) (O) (D) (B)
+b1.test.U16.A (TGAOR2XA) (I) (D) (B)
+b1.test.U16.Y (TGAOR2XA) (O) (D) (B)

Example 8: gate b1.test.U14



Example 9: trace -from b1.iny_reg_0_.Q -to b1.iny_reg_1_.CLK -detail



From : b1.iny_reg_0_.Q
To : b1.iny_reg_1_.D

+ b1.iny_reg_0_.Q (TG2DFFQRBXJ) (O) (D) (?)
+ b1.U15.A (TGAINV2XA) (I) (D) (?)
+ b1.U15.YB (TGAINV2XAXA) (O) (D) (?)
+ b1.U16.A (TGANAND2XA) (I) (D) (?)
+ b1.U16.Y (TGANAND2XA) (O) (D) (?)
+ b1.iny_reg_1_.CLK (TG2DFFQRBXJ) (I) (D) (?)

** Information of instance {b1.iny_reg_0_} **
cell_name :(TG2DFFQRBXJ) [./hier.v:14]
:type(REG, FF, 0, rise, MUX_FF)
<input>
D (D)(?) Net{b1.net0} Net_org{net0} from({b1.U01.Y} Cell(TGABUF2XA))
CLK (VCLK)(?) Net{ck1} Net_org{ck1} from(external port ck1)
<output>
Q (D)(?) Net{b1.net1} Net_org{net1} to {b1.U15.A} Cell(TGAINV2XA))

** Information of instance {b1.U15} **
cell_name :(TGAINV2XA) [./hier.v:15]
:type(GATE, INV, NORMAL, 1)
<input>
A (D)(?) Net{b1.net1} Net_org{net1} from({b1.iny_reg_0_.Q} Cell(TG2DFFQRBXJ))
<output>
YB (D)(?) Net{b1.net2} Net_org{net2} to {b1.U16.A} Cell(TGANAND2XA))

```

** Information of instance {b1.U16} **
cell_name      :(TGANAND2XA) [./hier.v:17]
              :type(GATE, AND, NORMAL, 2, 2IN)
<input> -----
      A  (D)(?)      Net{b1.net2}  Net_org{net2}
          from({b1.U15.YB} Cell(TGAINV2XA))
      B  (D)(?)      Net{b1.net3}  Net_org{net3}
          from({b1.iny_reg_2_.Q} Cell(TG2DFFQRBXJ))
<output> -----
      Y  (D)(?)      Net{b1.net4}  Net_org{net4}
          to {b1.iny_reg_1_.CLK} Cell(TG2DFFQRBXJ)

```

```

** Information of instance {b1.iny_reg_1_} **
cell_name      :(TG2DFFQRBXJ) [./hier.v:18]
              :type(REG, FF, 0, rise, MUX_FF)
<input> -----
      D  (D)(?)      Net{in}  Net_org{in}
          from(external port in)
      CLK  (D)(?)      Net{b1.net4}  Net_org{net4}
          from({b1.U16.Y} Cell(TGANAND2XA))
<output> -----
      Q  (D)(?)      Net{out}  Net_org{out}
          to {EXT_PIN.out} Cell(wire))

```

(4) get_search command

Name	get_search: Search
Format	list get_search attribute parameter
Function	The search results that accepted the specified condition (instance name, net name, term name and block name) are displayed.
Return	list of search results
Example	

```
get_search gate {-hier *}
```

```
<Result>
tbuf03
tbuf02
tbuf01
```

<Attribute >

Attribute	Argument	Sample	Acquired information
type	cell type name	type LATCH	All cell instances of cell type "LATCH"
block	block instance name	block BUSCS	Block instance "BUSCS"
		block {-hierarchical *}	All block instances
gate	cell instance name	gate {INC.I50}	Cell instance "INC.I50"
		gate {INC.*}	All cell instances in "INC" block
		gate {-hierarchical *}	All cell instances
net	net name	net CKS	Net "CKS"
		net {-get_pins *}	All ports of the top hierarchy
		net {-hierarchical *}	All nets
celltype	cell definition name	celltype NA01	All cell instances of cell definition name "NA01"
		celltype {NA*}	All cell instances of the cell definition name beginning with "NA"
blocktype	block definition name	blocktype BLK01	All block instances of block definition name "BLK01"
		blocktype {BLK*}	All block instances of block definition name beginning with "BLK"
cellname list	cell definition name	cellnamelist{*}	All cell definition names
		cellnamelist {NA*}	All cell definition name of cell definition name beginning with "NA"
blockname list	block definition name	blocknamelist{*}	All block definition names
		blocknamelist {BLK*}	All block definition name of block definition name beginning with "BLK"
term	cell instance name	term {-get_pins INC.*}	All ports of "INC" block

< Parameter >

Parameter	Explanation	Sample	Acquired information
-hierarchical -hier	setting of search hierarchy	net {-hier *}	All nets of all hierarchies
		net {-hier *.*}	All nets of hierarchies other than the top hierarchy
		net {-hier INC.*}	All nets of the hierarchy under "INC" block
-get_pins	gain of block port	net {-get_pins *}	All ports in the top hierarchy
		net {-get_pins INC.*}	All ports of "INC" block
		net {-get_pins -hier *}	All ports of all cell/block
-get_pins_input -get_pins_output -get_pins_inout	gain of input port	net {-get_pins_input *}	All input ports in top hierarchy
	gain of output port	net {-get_pins_output INC.*}	All output ports of "INC" block
	gain of inout port	net {-get_pins_inout -hier *}	All inout ports
-tail	gain of name that omitted hierarchy	gate {-tail INC.*}	All cell instance names in "INC" block. Reports the names excluding the hierarchy names as search result.
-delcell	gain of port except cell	net {-get_pins *.*}	All ports except the top block
		net {-get_pins -delcell *.*}	All ports of all blocks except the top block
-original -org	gain of net in the specified hierarchy	net {-hier *}	All nets (substantial net name)
		net {-hier -org *}	All nets
-celldefine -celldef	gain of block inside `celldefine~`endcelldefine	block {-hier *}	All block instances
		block {-hier -celldef *}	All block instances inside `celldefine~`endcelldefine

(5) trace_limit_number command

Name trace_limit_number : Sets the number of gates to be searched
Format trace_limit_number Number of gates
Function The number of gates to be searched is changed. (default is 30)
When only one of -from/-to was specified in trace command, it is effective.
Return None
Example

```
trace_limit_number 100
```

(6) run_NetWalker_file command

Name run_NetWalker_file : Execution of NetWalker file
Format void run_NetWalker_file NetWalker_file
Function The specified NetWalker script file is executed.
Example

```
run_NetWalker_file file1
```

```
<file1>
Begin {
    long a ;
    string A ;
    printf("hello\n") ;
    a = get_search(gate("-hier *"),A) ;
}
```

(7) run_NetWalker_string command

Name run_NetWalker_string : Execution of NetWalker script
Format void run_NetWalker_string NetWalker_script
Function NetWalker script is executed.
Example

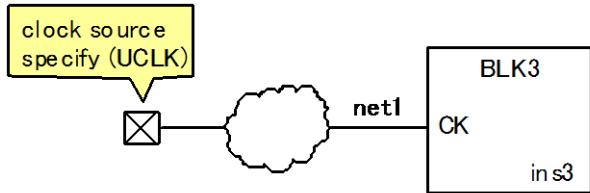
```
set nw_string "Begin { path_assigntran_mode(1); print_verilog_source ($file,$para); }"
run_NetWalker_string $nw_string
```

(8) get_block_ck_info command

Name get_block_ck_info : Clock information report which arrives at the block
Format int get_block_ck_info
Function Clock information arriving at the input terminal of all blocks is outputted.
Return 0: OK 1: ERROR
Example

```
get_block_ck_info
```

```
<Result>
** Module   Instance   Port   Net   Clock_domain **
BLKB    ins3      CK    net1    UCLK
```



(9) exit command

Name exit : The end of debugging mode
Format void exit
Function In the interactive mode, when ending, specify this command.
Example

```
exit
```

6.3 Method of analysis using Verdi GUI

The function to analyze with Verdi GUI of SpringSoft company was added.
The error message file (log.DFTcheck) which DFTcheck output is read for analysis.

Please refer to "[VerdiIF user guide](#)" for the details.

* After DFTcheck was executed, Verdi execution script (run_verdi_nw) is generated automatically in the current directory. As for this script, environmental setting is unnecessary.

7. Information Output

7.1 Clock Information for Collared Memory

All Collared memory instance and the clock pin which each clock signal defined in pt_shell arrives at are extracted. Please specify list of the module name to distinguish the Collared memory of the intermediate hierarchy.

<< Input >>

Specify the collared memory by -FILE or -PTSHLL option.

But if file (Collared_type_out.f) which Collared_memory_extra command generates for DFT304-3 is specified, the following additional specification is unnecessary.

(1) Description for -FILE file

```
set_strings CollaredMEM {b*c_cr*} {b*c_cm*} {b*c_co*} {b*c_cn*} {vmc_pipeline_wrapper_*};  
set_strings CollaredMEM {e*c_cr*} {e*c_cm*} {e*c_co*} {e*c_cn*};  
set_strings CollaredMEM {w*c_cr*} {w*c_cm*} {w*c_co*} {w*c_cn*};  
set_strings CollaredMEM {o*c_cr*} {o*c_cm*} {o*c_co*} {o*c_cn*};  
set_strings CollaredMEM {amcip*c_cr*} {amcip*c_cm*} {amcip*c_co*} {amcip*c_cn*};
```

(2) Description for -PTSHLL file

```
string CollaredMEM[] = { "b*c_cr*", "b*c_cm*", "b*c_co*", "b*c_cn*", "vmc_pipeline_wrapper_*,  
    "e*c_cr*", "e*c_cm*", "e*c_co*", "e*c_cn*",  
    "w*c_cr*", "w*c_cm*", "w*c_co*", "w*c_cn*",  
    "o*c_cr*", "o*c_cm*", "o*c_co*", "o*c_cn*",  
    "amcip*c_cr*", "amcip*c_cm*", "amcip*c_co*", "amcip*c_cn*" };
```

But please specify the details not to overlap when the wild card overlaps with the user logic.

<< Executive method >>

```
% DFTcheck -PREMINORI -FILE test.f
```

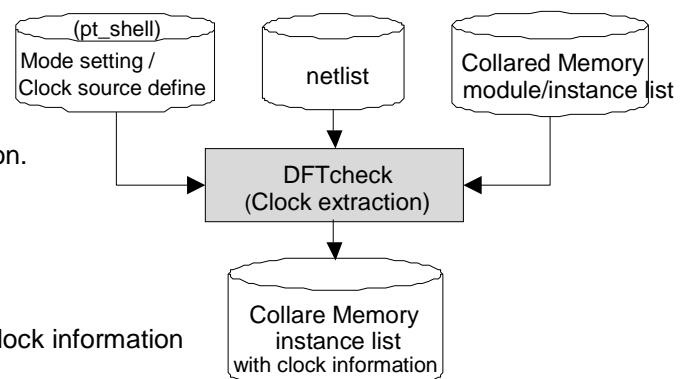
Specify the file which defined Module_list with -FILE option.

The above example is “test.f”.

If CollaredMEM was specified in PREMINORI mode,
it is executed.

<< Output >>

Instance_list of the Collared memory's clock pin with the clock information



The clock pin of the Collared memory every clock is reported.

Specification of special character as same Verilog. The characters to be included in between ¥ and space are one word.

<< Output file name>>

RAMCLK.info

Information is output to RAMCLK.info. The output format is as follows.

[format]

```
<file>== {<Collared memory instance name>, <clock pin name>, <instance name of clock source>}
```

:

Example)

```
chip_core_inst.rf.RAM2rw128d33w.CollaredRAM, clk1, bbb.clk1  
chip_core_inst.read_RAM2rw128d33w.CollaredRAM, clk2, aa.bbb.clk2  
chip_core_inst.RAM2rw128d33w.CollaredRAM, clk1, aaa.bbb.clk1  
:
```

7.2 Information of Fault detection (TEST_COVERAGE_DETAIL.f)

In PRE(default) or LBIST mode, The detailed information of the fault detection is output to the file.

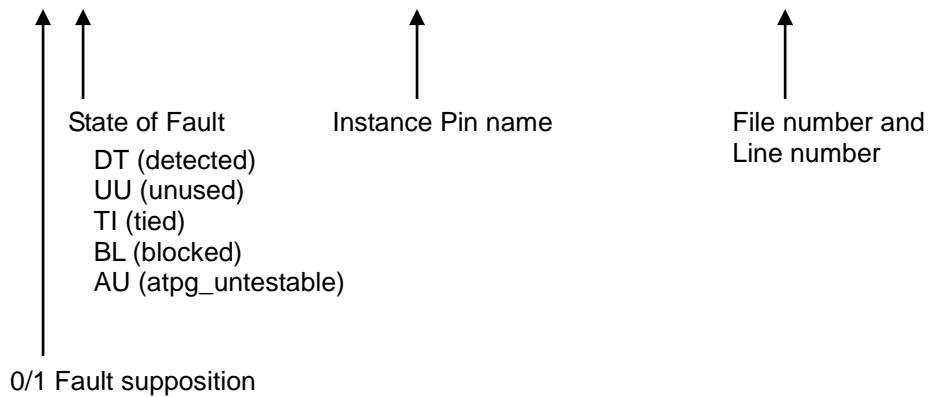
Please specify the following in -PTSHLL.

```
set_strings test_coverage_detail "yes";
```

Example)

```
1 AU MB_HFCTS_BUF_0_hf_buf.U20.A      // [line 1:138392]
0 AU MB_HFCTS_BUF_0_hf_buf.U20.YB     // [line 1:138392]
1 DT MB_HFCTS_BUF_0_hf_buf.U20.YB     // [line 1:138392]
0 AU MB_HFCTS_BUF_0_hf_buf.U19.A      // [line 1:138391]
```

:



Note)

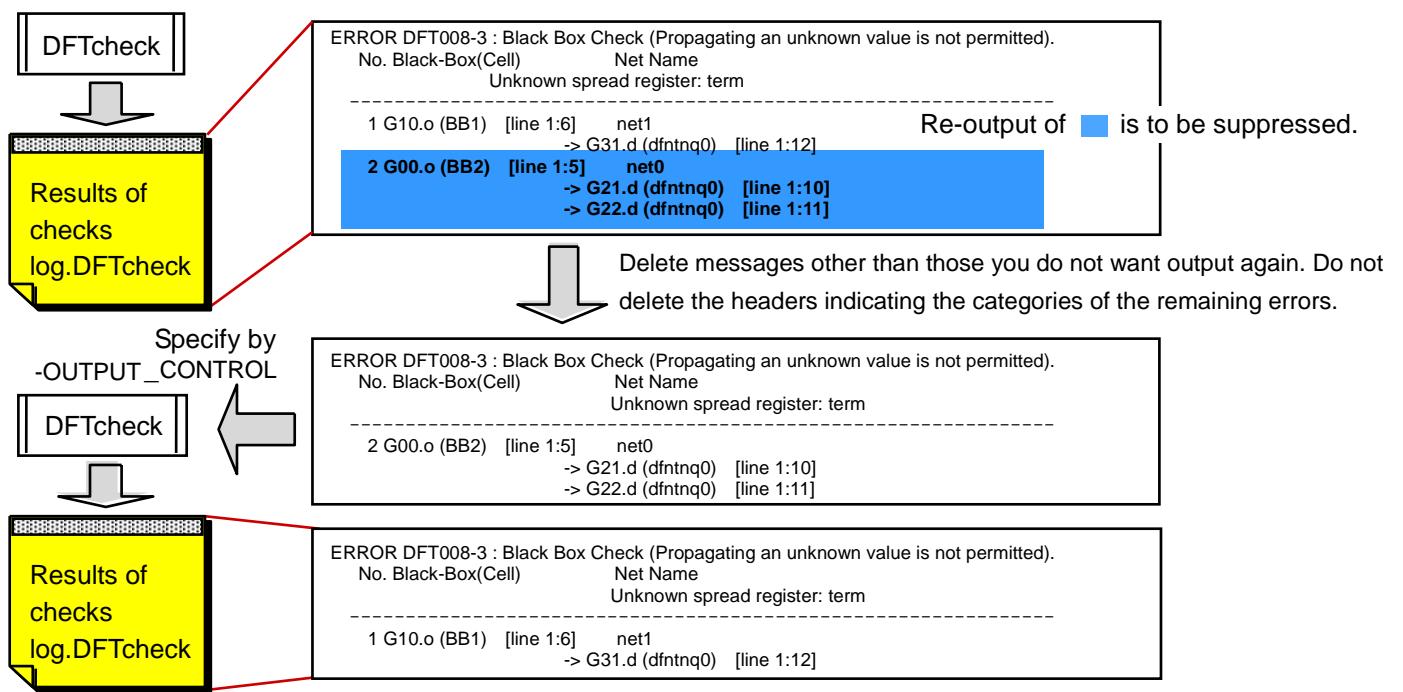
This coverage is the rate of detection in the conditions that error is 0.

When DFT003-7 is error, if the following is not defined, test coverage is not estimated.

```
set_strings NOCLOCK_MUXFF_is_BB "yes";
```

8. Suppressing the Output of Messages on Previously Checked Items

When DFTcheck is run and examination of the results has shown that some of the warning messages do not represent problems, the output of these messages can be suppressed when DFTcheck is run again. However, this does not apply to the gate-loop check.



<< Exclusion items from output suppression >>

- INFORMATION
- DFT017-0/DFT017-9/DFT018-1(partly)/DFT601-7
⇒This is the mistake of the user definition. Please review the definition.

8.1 Check-result output-control file (-OUTPUT_CONTROL)

When an output-control file has been specified, messages to be output by DFTcheck are compared with the content of this file and the output of any matching messages is suppressed. The format of the output control file is the same as that of log.DFTcheck file specified by the -CHECK_RESULT option. More than one output-control file can be specified.

Example) DFTgeck -OUTPUT_CONTROL aaa -OUTPUT_CONTROL bbb

For convenience, the following functions are supported.

(1) `define function

- Facilitates the replacement of strings.

This function may be useful when, for example, changing levels in a block hierarchy.

Example) `define XXX "aaa.bbb.ccc"

- Use get_instance_name to search for instance names to which a specific defined name (SH2DSP in the example below) is assigned. The instance names that have been hit are replaced with a given string.

However, note that this replacement function allows only one definition for a single message.

Example) `define YYY get_instance_name("SH2DSP")

(2) Partial matching

Parts of messages are compared for matches, that is, comparison is from the heads of messages to the points at which each entry in the output-control file ends.

That is, those parts of a message which are not described in the control file are regarded as matching.

Example) Compare module names and port names and ignore information on internal connections.

<output-control file>		<Suppressing message >	
No.	Module Name	No.	Port Name
	inner connect instance pin name		inner connect instance pin name
2	aaa	2	aaa
	X11.x		X11.x
			1 X11.X22.X35.i
			1 X11.X22.X34.i

(3) Multiple specification of a message under the same error category is allowed

Having more than message under the same error category does not cause problems.

Example) ERROR DFT305-1 : NMA check (wrong connect).

```
-----  
3 MOD1      SIG(nma1[0])      mem_nma1.NMA[0] (mem3)  [line 1:14] --- wrong connect  
  
ERROR (01-02) : Clock Line Check (Unused Cell)  
  
-----  
1 MOD2      SIG(nma2[1]) --- can not find it.
```

(4) When a module name is included in a conditional statement of the form shown below,

`ifdef *Module name* `endif

The message-output control with respect to that module name will not be carried out if the module name is not used.

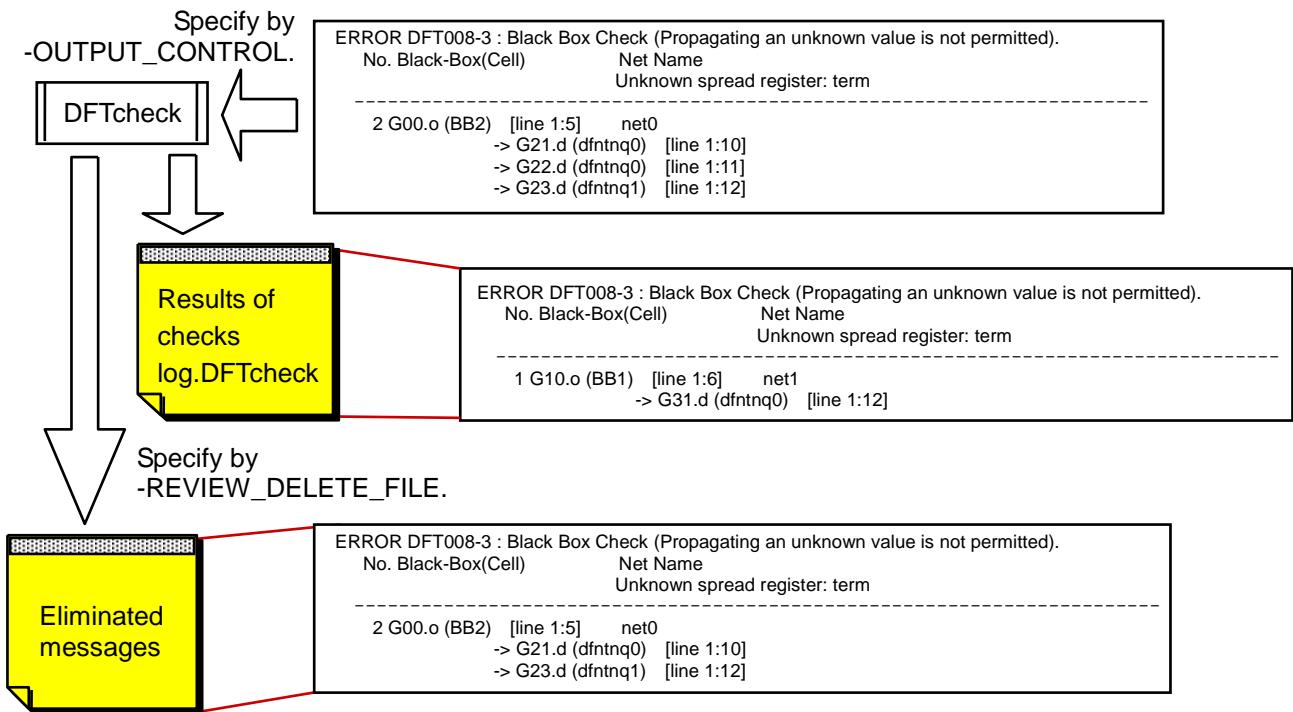
Example) Enable the output control function when the module name SH2DSP has been used.

```
-----  
'ifdef "SH2DSP"  
    ERROR DFT305-1 : NMA check (wrong connect).  
  
-----  
1 MOD2      SIG(nma2[1]) --- can not find it.  
'endif
```

(5) Lines starting with # are treated as comments.

8.2 Displaying messages eliminated by the check-result output control file (-REVIEW_DELETE_FILE)

The -REVIEW_DELETE_FILE option may be used to specify a file to receive the messages eliminated by the check-result output-control mechanism.



9. Appendix

1. DFTcheck Rule List

DEFAULT STATE:

RULE	MESSAGE	MUX SCAN	LBIST	SINGEN	POST	MINORI	PRE MINORI	POST MINORI	FIELD
DFT000	Undefined NetWalker Cell Library.	ALWAYS ON	ALWAYS ON	ALWAYS ON	ALWAYS OFF	ALWAYS OFF	ALWAYS OFF	ALWAYS OFF	ALWAYS OFF
DFT001	Feedback Loop.	ALWAYS ON	ALWAYS ON	ALWAYS ON	OFF	ALWAYS OFF	ALWAYS OFF	ALWAYS OFF	ALWAYS OFF
DFT002	Cell Type of don't use.	ALWAYS ON	ALWAYS ON	ALWAYS ON	ALWAYS ON	ALWAYS OFF	ALWAYS OFF	ALWAYS OFF	ALWAYS OFF
DFT003	Clock is controllable.	ALWAYS ON	ALWAYS ON	ALWAYS ON	ALWAYS ON	ALWAYS OFF	ALWAYS OFF	ALWAYS OFF	ALWAYS OFF
DFT004	Set/Reset is controllable.	ALWAYS ON	ALWAYS ON	ALWAYS ON	ALWAYS ON	ALWAYS OFF	ALWAYS OFF	ALWAYS OFF	ALWAYS OFF
DFT007	Bus Only One Drive.	ALWAYS ON	ALWAYS ON	ALWAYS ON	ALWAYS ON	ALWAYS OFF	ALWAYS OFF	ALWAYS OFF	ALWAYS OFF
DFT008	DFT008-1 Black Box Check(Output) Can not fault detected.	OFF	ALWAYS OFF	ALWAYS OFF	ALWAYS OFF	ALWAYS OFF	ALWAYS OFF	ALWAYS OFF	ALWAYS OFF
	DFT008-3 Black Box Check (The spread of an unknown value does not permit).	ALWAYS OFF	ALWAYS ON	ALWAYS ON					
	DFT008-4 Black Box Check (The both terminal does not permit).	ALWAYS OFF	ALWAYS ON	ALWAYS ON					
	DFT008-2 Black Box Check(Input).	OFF	OFF	OFF					
	DFT008-5 RAM/ROM input terminals are not connected observation F/F.	ON	ON	ON					
DFT009	Clock Pair/PLL Clock Check.	ALWAYS ON	ALWAYS ON	ALWAYS ON	ALWAYS OFF	ALWAYS OFF	ALWAYS OFF	ALWAYS OFF	ALWAYS OFF
DFT010	Undetect Fault.	OFF	OFF	OFF	ALWAYS OFF	ALWAYS OFF	ALWAYS OFF	ALWAYS OFF	ALWAYS OFF
DFT011	DFT011-1 The following cell instance's input pins are dangling.	ALWAYS OFF	ALWAYS ON	ALWAYS ON	ALWAYS OFF	ALWAYS OFF	ALWAYS OFF	ALWAYS OFF	ALWAYS OFF
	DFT011-2 The clock is connected with the terminal which is not the clock terminal. And there is a problem in timing.	ALWAYS ON	ALWAYS ON	ALWAYS ON	ALWAYS ON				
	DFT011-3 Set/Reset signal is connected with the data terminal.	ALWAYS ON	ALWAYS ON	ALWAYS ON	ALWAYS OFF				
DFT013	Gated Clock Enable.	ON	ON	ON	ON	ALWAYS OFF	ALWAYS OFF	ALWAYS OFF	ALWAYS OFF
DFT014	Floated output module ports.	ALWAYS ON	ALWAYS ON	ALWAYS ON	ALWAYS OFF	ALWAYS OFF	ALWAYS OFF	ALWAYS OFF	ALWAYS OFF
DFT015	Need to fix or connect.	ON	ON						
DFT017	Select DC.	OFF	OFF						
DFT018	ATOM SKBR Check.	ON	ON	ON	ON	ALWAYS OFF	ALWAYS OFF	ALWAYS OFF	ALWAYS OFF
DFT019	IOAC Scan Test Check.	OFF	OFF	OFF	ALWAYS OFF	ALWAYS OFF	ALWAYS OFF	ALWAYS OFF	ALWAYS OFF
DFT020	FFR Cone Limitation Check.	OFF	OFF	OFF	ALWAYS OFF	ALWAYS OFF	ALWAYS OFF	ALWAYS OFF	ALWAYS OFF
DFT021	Field Bist Check	ALWAYS OFF	ALWAYS OFF	ALWAYS OFF	OFF	ALWAYS OFF	ALWAYS OFF	ALWAYS OFF	OFF
DFT022	Illegal transfer at DVFS	OFF	OFF	OFF	ALWAYS OFF	ALWAYS OFF	ALWAYS OFF	ALWAYS OFF	ALWAYS OFF

DEFAULT STATE:

RULE	MESSAGE	MUX SCAN	LBIST	SINGEN	POST	MINORI	PRE MINORI	POST MINORI	FIELD
DFT023	SEN/SENG Of SENGEn	ON	ON	ON	ON	ALWAYS OFF	ALWAYS OFF	ALWAYS OFF	ALWAYS OFF
—	Test Coverage.	OFF	OFF	OFF	ALWAYS OFF	ALWAYS OFF	ALWAYS OFF	ALWAYS OFF	ALWAYS OFF
DFT999	Total undetected fault report.	OFF	OFF	OFF	ALWAYS OFF	ALWAYS OFF	ALWAYS OFF	ALWAYS OFF	ALWAYS OFF
DFT100	DFTRAM is defined in NW Library.	ALWAYS OFF	ALWAYS OFF	ALWAYS ON	ALWAYS OFF	ALWAYS OFF	ALWAYS OFF	ALWAYS OFF	ALWAYS OFF
DFT101	Clock Through IO Cell.	ALWAYS OFF	ALWAYS OFF	ALWAYS ON	ALWAYS OFF	ALWAYS OFF	ALWAYS OFF	ALWAYS OFF	ALWAYS OFF
DFT108	BlackBox X Through IO Cell.	ALWAYS OFF	ALWAYS OFF	ALWAYS ON	ALWAYS OFF	ALWAYS OFF	ALWAYS OFF	ALWAYS OFF	ALWAYS OFF
DFT109	NOBS/EXTEST Pin Fixed Value Check.	ALWAYS OFF	ALWAYS OFF	ALWAYS ON	ALWAYS OFF	ALWAYS OFF	ALWAYS OFF	ALWAYS OFF	ALWAYS OFF
DFT301	Clock is controllable.	ALWAYS OFF	ALWAYS OFF	ALWAYS OFF	ALWAYS OFF	ALWAYS ON	ALWAYS OFF	ALWAYS OFF	ALWAYS OFF
DFT302	Clock is controllable.	ALWAYS OFF	ALWAYS ON	ALWAYS ON	ALWAYS OFF				
DFT303	MINORI bridge check.	ALWAYS OFF	OFF	ALWAYS OFF					
DFT304	Collared Memory.	ALWAYS OFF	ALWAYS ON	ALWAYS OFF	ALWAYS OFF				
DFT305	NMA Check.	ALWAYS OFF	OFF	ALWAYS OFF					
DFT306	RS check.	ALWAYS OFF	OFF	ALWAYS OFF					
DFT307	Memory Terminal.	ALWAYS OFF	ALWAYS ON	ALWAYS OFF					
DFT401	Scan Chain Check.	ALWAYS OFF	ALWAYS OFF	ALWAYS OFF	ON	ALWAYS OFF	ALWAYS OFF	ALWAYS OFF	ALWAYS OFF
DFT501	RS Chain Check.	OFF	ALWAYS OFF						
DFT601	Digital Hard Macro.	OFF	OFF	ALWAYS OFF	OFF	ALWAYS OFF	ALWAYS OFF	ALWAYS OFF	ALWAYS OFF

2. DFTcheck Parameter List

RULE	MESSAGE	PARAMETER	DEFAULT VALUE	CONDITION SETTING COMMAND
DFT000	Undefined NetWalker Cell Library.			
DFT001	Feedback Loop.	-CHECK_001		
DFT002	Cell Type of don't use.			add_cell_type .. DUMMYFF set_strings Cancel_DFT002_01_async_reset_check
DFT003	Clock is controllable.	-DFTCLEAN		
DFT004	Set/Reset is controllable.	-DFTCLEAN		
DFT007	Bus Only One Drive.			
DFT008	Black Box Check.	-CHECK_008_1 -CHECK_008_2 -CANCEL_008_5 -DFTCLEAN_DFT008_5 -DETAIL_008_5		set_strings Unknown_External_Pin
DFT009	Clock Pair/PLL Clock Check.			
DFT010	Undetect Fault.	-CHECK_010 -DFT010_01_PRT_NUM	1	
DFT011	Input dangling & Problem in timing.			
DFT013	Gated Clock Enable.	-CHECK_013_12 -CANCEL_013_5 -CANCEL_013_9 -CANCEL_PRIMARY		set_strings CHK_DFT013_10 set_strings DC_TEST_MODE set_strings DFT013_CANCEL_GCK_INS set_strings DFT013_05_UNDETECT_FAULT_CHECK set_strings DFT013_CANCEL_PORT set_strings MASKED_FOR_AC
DFT014	Floated output module ports.			
DFT015	Need to fix or connect.	-CANCEL_015		
DFT017	Select DC.			set_strings SELECT_DC set_strings CANCEL_DFT017_06 set_strings TPI_EN set_strings ADD_SENGEN set_strings SENGGEN_CELL
DFT018	ATOM SKBR Check.	-CANCEL_018		set_strings ATOM_SKBR_CHK
DFT019	IOAC Scan Test Check	-IN_IOAC_FILE -OUT_IOAC_FILE		set_strings IOAC_PORT
DFT020	FFR Cone Limitation Check	-CHECK_020		set_strings OBSERVE_type set_strings OUTPUT_VERILOG_FILE set_strings PREFIX set_numerical_value limit_nFFR set_numerical_value Minimum_percentage
DFT021	Field Bist Check	-TABLE		set_strings DFT021_cancel_cw2mw set_strings DFT021_permit_gate set_strings DFT021_insert set_strings Wrapper_xx set_strings OUTPUT_VERILOG_FILE set_strings PREFIX
DFT022	Illegal transfer at DVFS	CONTROL		
DFT023	SEN/SENG of SENGGEN			set_strings DFT023_AREA
—	Test Coverage	-TESTCOVERAGE		set_strings test_coverage set_strings outside_test_coverage set_strings test_coverage_detail set_strings NOCLOCK_MUX_FF_is_BB
DFT999	Total undetected fault report.	-CHECK_010		
DFT100	DFTRAM is defined in NW Library.			

RULE	MESSAGE	PARAMETER	DEFAULT VALUE	CONDITION SETTING COMMAND
DFT101	Clock Through IO Cell.			
DFT108	BlackBox X Through IO Cell.			
DFT109	NOBS/EXTEST Pin Fixed Value Check.			
DFT301	Clock is controllable.			
DFT302	Clock is controllable.			set_strings CollaredMEM set_strings UIFMEM
DFT303	MINORI bridge check.	-CHECK_303		
DFT304	Collared Memory.	-FILE		set_strings CollaredMEM set_strings UIFMEM
DFT305	NMA Check.			set_strings option_dft305_permit_not_direct set_strings NMA_TEST
DFT306	RS check.			set_strings RS_TEST set_strings INFO_DFT306_2
DFT307	Memory Terminal.			set_strings DFT307_01_TYPE
DFT401	Scan Chain Check.	-CANCEL_401_5 -CANCEL_401_6 -IN_SCAN_DEF -OUT_SCAN_DEF -DFT401_DEBUG_NOSPACE		set_strings POST_DFT set_strings POST_DFT_ORDERED set_strings SCANDEF_PARTITION_NO_PRT set_numerical_value POST_DFT_MAX_BITS set_cell_term_property .. ScanL .. set_strings SCANEN_CONNECT set_strings MASKED_FOR_AC set_strings Cancel_wrapper set_strings DFT401_Fanout_SI
DFT501	RS Chain Check.			set_strings DFT501_MBIST_RS set_numerical_value RS_MAX_BIT set_numerical_value RS_MAX_BIT
DFT601	Digital Hard Macro.	-CHECK_601		
Common Options		-TOP -WORK -LANG -VHDL -F -RENEW -ONLYCOMP -PTSHELL -NWCELL -LOG -CHECK_RESULT -MAXERR -MUXSCAN -LBIST -SINGEN -MINORI -POST -PREMINORI -POSTMINORI -COLLARED_EXTRA -FIELD -CANCEL_WARNING -CHECK_EXCLUSION_MODULE -SCAN_EN -CANCEL_CHECK_VMC -ALREADY_SCAN_MODULE -OUTSIDE_SCAN_INS -PATTERNM -PATTERNMN -CHECK_EXPECT -f -v -y +libext+ +incdir+ -NET -LIB	./work VERILOG log log.DFTcheck 1000	create_clock set_case_analysis set_input_delay set_strings SCAN_EN set_strings DFT_CONTROL_REG set_strings CollaredMEM set_strings ALREADY_SCAN_MODULE set_strings OUTSIDE_SCAN_INS connect_direct set_strings PATTERN_MONITER_SIGNAL

RULE	PARAMETER	DEFAULT VALUE	CONDITION SETTING COMMAND
	-TRACE_FROM -TRACE_TO -TRACE_GATE_INFO -TRACE_LIMIT -TRACE_DETAIL -TCL -TCLD	30	

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