User's Manual

LLWEB-00009244

OPENCAD

Renesas Advanced Design Platform

Logic Design Rule Checker
HLDRC User's Guide V2.27

Renesas Electronics Corp.
Platform Integration Div.
Front-end Design Technology Development Dept.
Last update: 03/22/2013

[Release notes]

- v2.27 Mar 22, 2013
  (1) E-Fuse connect check (17-01) was revised.
  (2) The check objects of Clamp check (18-01) were added.
  (3) The check condition of CellCondition check (22-01) was added.
  (4) PGE terminal check (24-01) was added.
  (5) The function of shampoo2hldrc command was expanded.
  (6) The set_strings commands (PRINT_09_01/02/03/04_PATH) were added.
  (7) The set_numerical_value command (pt_flg_9_4_IGNORE_BUF_COUNT) was added.
  And the set_strings command (9_4_IGNORE_BUF_COUNT) was deleted.
  (8) -PROCESS option was added.

- v2.26 Sep 21, 2012
  (1) E-Fuse connect check (17-01) was changed for T28.
  (2) ETMcheck (23-01) was added.
  (3) The option name is changed from -CHECK_CLAMP_POST to -CHECK_CLAMP.
  (4) -CANCEL_CLAMP_TIE_CELL option was added.
  (5) The set_strings commands (Stop_propagation_at_iocell and Stop_loop_check_term) were added.
  (6) In force connection check (19-01), the setting method of external port was added.
  (7) Method of analysis using Verdi GUI was added.
  (8) The set_strings command (9_4_IGNORE_BUF_COUNT) was changed.

- v2.25 Mar 23, 2012
  (1) Cell condition check (22-01) was added.
  (2) Output information of DFILE was added. And set_strings command (DFILE) was added.
  (3) set_strings command (9_4_IGNORE_BUF_COUNT) was added.

- v2.24 Sep 20, 2011
  (1) Force connection check (19-01) was modified for inout pin.
  (2) Force connection check (19-01) was added the regular expression of pin.
  (3) Prohibit connection check (20-01) was added the regular expression of pin.
  (4) Name check (04-23/24) was added.
  (5) The specification of output float check was changed.

- v2.23 Nov 30, 2010
  (1) The function to check individually of 03-02 was added.
  (2) GROUP function of 19-01 was added.
  (3) Explanation of 20-01 was modified.
  (4) Use cell check (21-01) was added.
  (5) NetEdit+ script of 18-01 was changed.

- v2.0 March 31, 2000 - Fully revised edition following the release of HLDRC (v2.0)

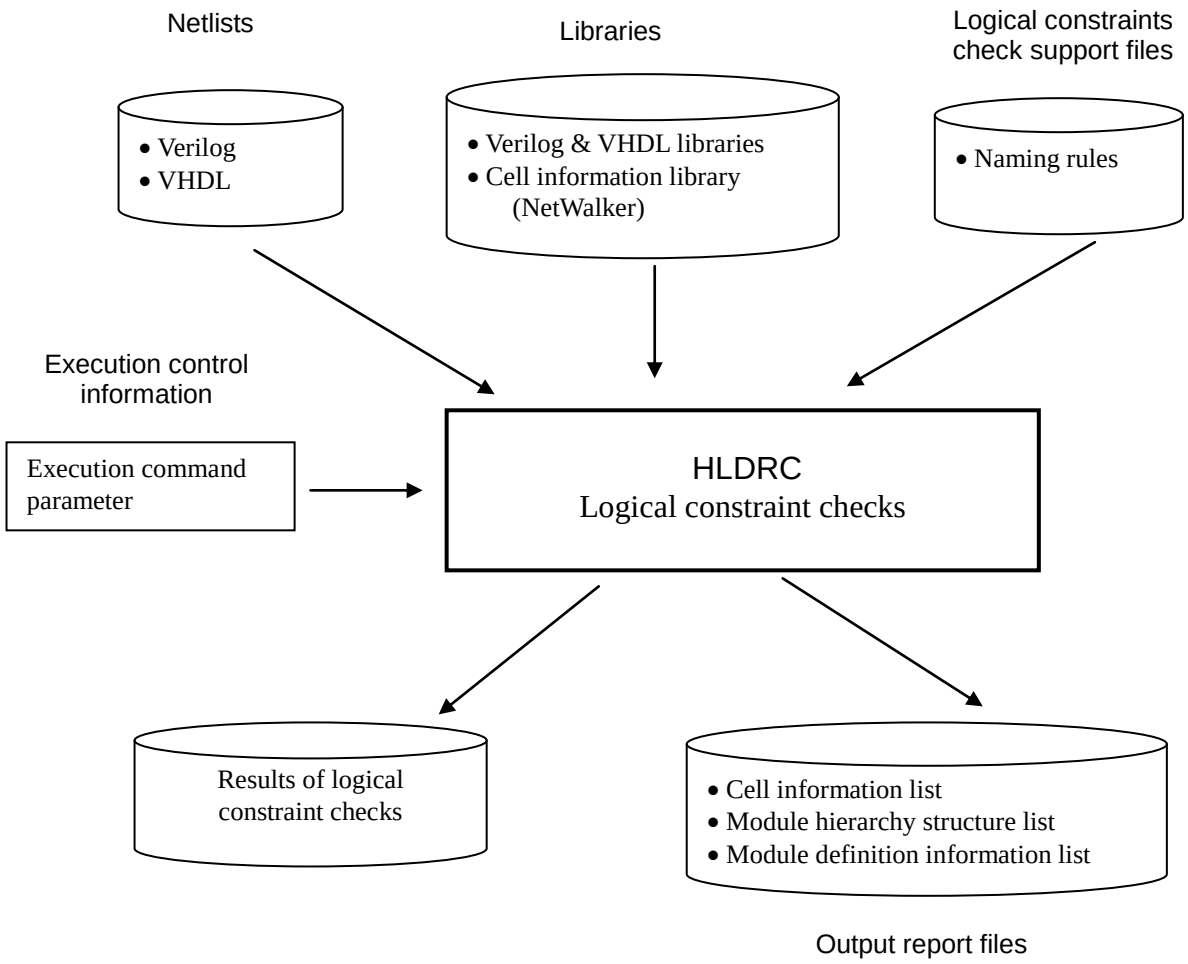
(1) Command rules have been entirely revised due to the change to NetWalker edition.

Contents

1. HLDRC overview

HLDRC (High-performance Logic Design Rule Checker) checks logic design constraints with the gate level netlists. The formats of the netlists that can be input are Verilog and VHDL. It outputs check results and netlist information to files.

2. HLDRC system structure



3. Contents of logical constraint checks

HLDRC checks the following logical constraints. Please refer to the summary of items checked for more details.

Checks to be executed can be selected using command options.
The following checks will be executed by default unless specified by –CSANCEL_XXXX option. To cancel execution of these checks, specify them by –CSANCEL_XXXX.

The numbers in parenthesis correspond to error numbers.

(1) Short circuit check of cell pins. (-CANCEL_SHORTS)
Check the power supply and GND direct connection of pins.

(2) Primary I/O check (-CANCEL_PRIMARY)
Checks the connection of I/O buffers.
Note: To execute on a module-by-module basis, specify –CANCEL_PRIMARY.

```
About (02-11) The I/O buffer of inout pad should be not connected sensibility pin
```

In a customer or testing, the change of bi-directional primary I/O generates reflection and ringing and internal logic brings an unexpected result.
However, in test pin combination, many suspected errors are outputted. In order to prevent defective product, please give me an understanding.
<Solution of errors message >
Please perform the flowing, when you don't repair the circuit. As a result, When you judged as false errors, please except using PTSHELL. For details, please refer to Chapter 6.
- Check Method by Simulator (it Avoids by Test Pattern)
In Change Step of Bi-directional Primary I/O, Please mask the output relevant to change of a sensitive terminal.
- Visual Check (Check of Evasion Circuit)
Before or after Change of Bi-directional Primary I/O, Please check whether there is any evasion circuit so that edge sensitive terminal may not change.

(3) Connection check of signals and instances (_CANCEL_DANGLING)
Checks the floating of pins and module ports.
(would lead to problems with the layout or in module diagnostic checks)
Countermeasures (for Design Compiler):
- Input/output terminals of unused blocks
  Measures such as connecting dummy cells to input/output terminals of unused blocks will be required.
  The following should be set in the synchronization from the top-level hierarchy.
  uniqfy
  remove_unconnected_ports find(-hierarchy cell,"*")
- The direct connection of power supply ground to block output pins / through nets / multi-ports
  set_fix_multiple_port_nets -feedthroughs -outputs -buffer_constants

(4) Name rule check (-CANCEL_NAME)
Checks the usable characters and the number of characters used for the net, instance, port and module names.
(if not carried out, problems can occur on the back-end tools such as layout)
Countermeasures (Design Compiler)
Use **change_names**.

(5) Gate loop check (-CANCEL_LOOP)
Checks the feedback loop connections in the circuits.
(would lead to problems with Renesas test DA tools)

(6) Fanout check (-CANCEL_FANOUT)
Checks the fanout restriction value set for each pin of a cell.
(if –FOCHECK NUMB is specified, the check is carried out for the number of pins driven)

(7) Parallel drive check (-CANCEL_PARALLEL)
Checks the parallel connection (Wired connection) of cells.

(8) Bus repeater check (-CANCEL_THREE)
Checks the connection of bus repeater cells.

(9) Clock line check (-CANCEL_CLOCK)
Checks cells that can cause problems on the clock line.
(would lead to problems with CTS (layout))

(11) Level-shifter check (-CANCEL_LEVELSHIFT)
This check is for connections between power supply lines that carry different voltages in a multi-power supply chip (this would lead to problems with layout).

(13) Module port check (-CANCEL_MODULE_PORT)
If the attributes of module ports are inconsistent, different (and incorrect) results will be obtained in STA. This check is to find out such inconsistencies.

The following checks are only executed when specified in the command.

(6) Top module fanout check (-TOP_MODULE_FANOUT_RECTRICTION *limit value (real number)*)

(11) Clamp check in multi-power supply design (-CLAMPING_CHECK *violating voltage value (real number)*)
Checks for codes that create power clamping.

(12) Top module port check (executed when –TOP_MODULE_PORT is specified)
When the signal on an output pin of a module is fed to a cell within the module, timing problems may easily occur because of the effects of capacitance outside the module.
The check is carried out on the modules immediately below the top-level module.

(14) Restricted cells check (-RESTRICTION_CELL_CHECK)
There is a possibility that cells containing pass transistors are automatically introduced during automatic layout.
This check finds such unusable cells (checks whether the cell type of the NetWalker is “DNT_USE”).

Items Checked in the Naming-Rules Check

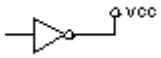
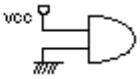
Item named		External port	Module port	Net
Number of characters	Upper limit	472	511	511
	Reasons for constraints	• TESTACT	• GDS	• spefmixer
Number of characters after expansion	Upper limit	—	1024	1024
	Reason for constraint	—	—	—
Reserved words	Not to be used	• SystemVerilog reserved words • NetWalker reserved words • Shingen (Renesas test DA tool) reserved words	• SystemVerilog reserved words • NetWalker reserved words • Shingen (Renesas test DA tool) reserved words	• SystemVerilog reserved words • NetWalker reserved words • Shingen (Renesas test DA tool) reserved words
	Reasons for constraints	• Shingen, etc	• Shingen, etc	• Shingen, etc
Usable characters	Allowed set	—	—	—
	Reasons for constraints	—	—	—
Upper/ lower case	Preferred type	Lower case in principle		
	Reason for constraint	Recommended (Default:Nocheck)		

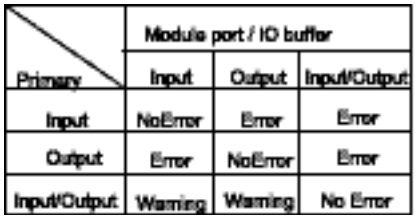
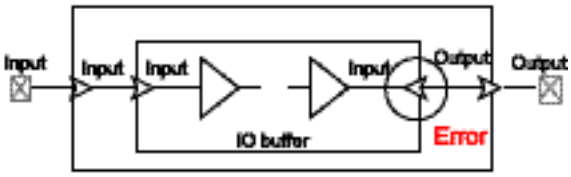
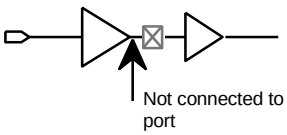
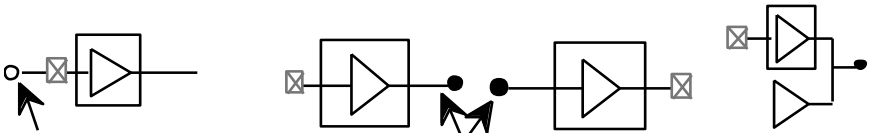
Item named		Top Module	Module	Gate/Module instance
Number of characters	Upper limit	120	233	511
	Reasons for constraints	• ZOIX	• ICC, NetWalker	• spefmixer
Number of characters after expansion	Upper limit	—	—	1024
	Reason for constraint	—	—	—
Reserved words	Not to be used	• SystemVerilog reserved words	• SystemVerilog reserved words	• SystemVerilog reserved words • NetWalker reserved words • Shingen (Renesas test DA tool) reserved words
	Reasons for constraints	—	—	—
Usable characters	Allowed set	—	—	—
	Reasons for constraints	—	—	—
Upper/ lower case	Preferred type	Lower case in principle		
	Reason for constraint	Recommended (Default:Nocheck)		

(Note)
The reserved words of Shingen are generated with Shingen. Please exclude reserved words of Shingen after Shingen execution.

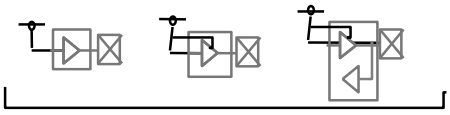
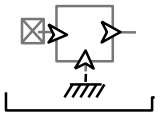
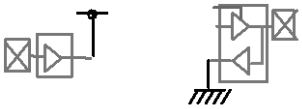
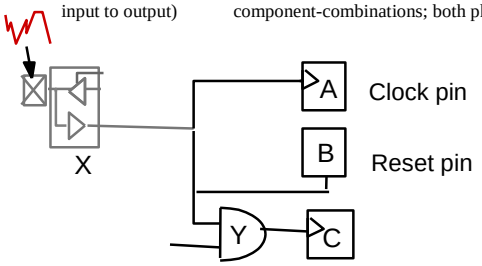
3.1 List of items checked by HLDRC

<table>
<tr><th>No</th><th>Items checked</th><th>Content of the check</th></tr>
<tr><td rowspan="2">1</td><td rowspan="2">Short circuit check
(Shorts)

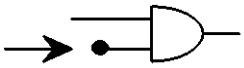
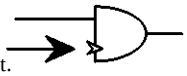
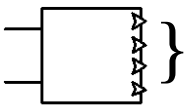
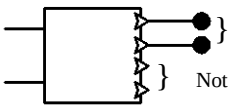
Decision on HIGH/LOW tied nets :
It checks whether nets with directly connected cell pins are HIGH/LOW. The short circuit checks of pad cells are done at the primary check.</td><td>The short circuit checks of cell output pins. An error will be output when output pins are tied either “HIGH” or “LOW”.
ERROR(01-01):The following output pins are tied high/low.
  </td></tr>
<tr><td>Short circuit checks of cell input pins. A warning will be output when not all the input pins of a cell are connected to the cell and all or some of the input pins are tied HIGH or LOW.
WARNING(01-02):The following input pins are tied high, low or X.
Net or pin not driven   </td></tr>
<tr><td>2</td><td>Primary I/O check
(primary signals)

* Checking starts at the primary ports and stops when an error is found. In the event of a warning, a message is output and the check will continue.</td><td>The connection of module I/Fs interfaces and I/O buffer cells is checked; from this check is carried out from the primary ports to the I/O buffers. The verdicts of the checks are given in the table below. Error and warning messageses are output for each attribute of primary ports.
ERROR(02-01):The following primary input port(s) should be connected to I/O buffer of pad pin.
ERROR(02-02):The following primary input port(s) should be connected to input module port.
ERROR(02-03):The following primary output port(s) should be connected to I/O buffer of pad pin.
ERROR(02-04):The following primary output port(s) should be connected to output module port.
WARNING(02-05):The following primary inout port(s) should be connected to I/O buffer of pad pin.
WARNING(02-06):The following primary inout port(s) should be connected to inout module port.
 
  </td></tr>
<tr><td></td><td></td><td>I/O buffer cells’ pad pins are checked for connection. An error message will be output when a pad pin is not connected to a primary signal.
ERROR(02-07):The following I/O buffer signal should connect to primary port.
 
(Note) When a pad pin is floating, no error will be output if the pin is tied to the high or low level.</td></tr>
<tr><td></td><td></td><td>The connection to pins of I/O buffer cells is checked. An error message will be output when a pin other than a pad pin is not connected to a cell.
ERROR(02-08):The following I/O buffer signals are dangling.
 
(Note) An error will be produced by any floating pin of an I/O buffer cell, regardless of the pin’s attributes. The error message is eliminated by connecting the floating pin to a primary pin or tying it to the high or low level, even if the pin is not connected to a cell.</td></tr>
</table>

<table>
<tr><th>No</th><th>Items checked</th><th>Content of the check</th></tr>
<tr><td rowspan="3">2</td><td rowspan="3">* Specify –CHECK_2_9 to execute this check.

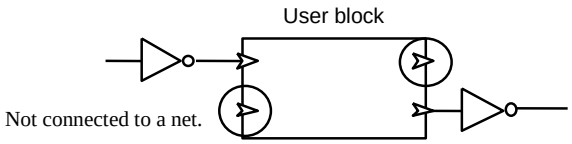
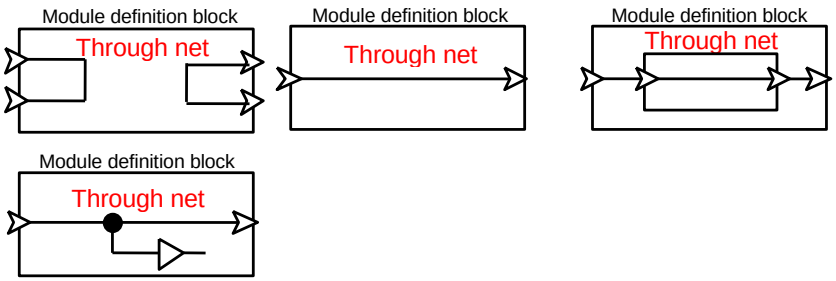
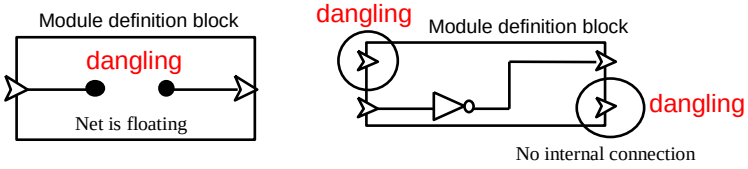
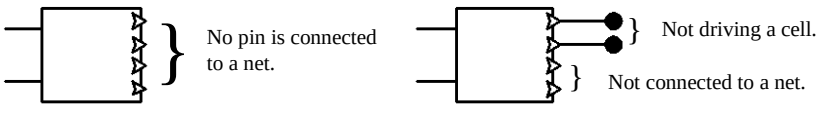
* Specify –CHECK_2_10 to execute this check.</td><td>This check is only carried out when the option given at left has been selected.
The input pins of I/O buffer cells are checked for tied-high and tied-low states. An error message is output when all of the input pins are tied high or low. An error will not be output when any of the input pins is not tied.
ERROR(02-09):The following I/O buffer all input signals are tied high/low.
 
All pins are tied.
 
Some of the pins are tied (no error).</td></tr>
<tr><td>This check is only carried out when the option given at left has been selected.
The output and input/output pins of I/O buffer cells are checked for tied-high and tied-low states. An error will be output when an internal output pin or input/output pin of an I/O buffer is tied high or low.
ERROR(02-10):The following I/O buffer output/inout signals are tied high/low.
  </td></tr>
<tr><td>This check is for the connection of bi-directional pad pins of I/O cells to sensibility pins.
ERROR(02-11):The I/O buffer of inout pad should be not connected sensibility pin.
Reflection/ringing (on changes from input to output)
Reflection is produced by incompatibility between the output impedance of an LSI circuit and the characteristic impedance of the wiring and ringing is oscillation due to the values of L, C, R component-combinations; both phenomena lead to distorted waveforms.
 

(Note) To exclude specific bi-directional cells from the scope of checking, specify the cell instance name with the -CANCEL_SENSIBILITY_PIN_CHECK option. A, B, and C will not be checked when X is specified in this way; C will not be checked when Y is specified.

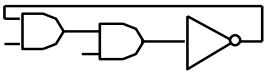
You can also avoid this check by using PTSHELL to set signal lines to fixed levels. For more details, see section 6.</td></tr>
<tr><td>3</td><td>Dangling checks
(dangling)
Checks the connections between signal lines and cell instances: Here the connections of internal cells are checked.</td><td>Connections to cell-input pins are checked. An error message is output when a net connected to the input pin of a cell instance is not being driven or when the input pin of a cell instance (other than a pad cell) is not connected to a net. (A pin is considered to be driven if it is connected to the power supply or GND net.)
ERROR(03-01):The following cell instance's input pins are dangling.
This net is not being driven.
 
This pin is not connected to a net.
  </td></tr>
<tr><td>*Specify –CHECK_3_2 or set_strings to execute this check.</td><td>This check is only carried out when the option given at left has been selected.
Cells' output pins are checked for connection. A warning will be output when none of the output pins of a cell instance is connected to a net or when the pins are not driving a cell although they are connected to a net. (No waning will be output if an output pin is connected to the power supply or GND net.
WARNING(03-02):The following cell instance's output pins are all dangling.
 
No pin is connected to a net.
 
Not driving a cell.
Not connected to a net.

(Note) On the check only for specific pins, please specify as follows. This is force connection check (19-1).

set_strings FORCE_CONNECT ¥
BASE {<cell name>} {<output pin name>} ¥
OPEN INVALID ¥
MESSAGE "" ;</td></tr>
</table>

No	Items checked	Content of the check
3	*Specify –CHECK_3_3 to execute this check.	This check is only carried out when the option given at left has been selected. Module I/Fs are checked for connection. A warning will be output when a pin defined in a user block is not connected to anything. `WARNING(03-03):The following block instance pins are dangling.` 
		Module definitions and internal descriptions are checked for several conditions. The following cases will produce errors of this type. • Through nets (shown below). • Power supply and GND nets. `ERROR(03-04):The following module port definition is/are not correct.` 
		Module definitions and internal descriptions are checked for the following two conditions; if either is detected, a warning is produced. • A signals has been defined as an interfacial signal but its internal connection has not been defined. • A net which is connected to an interfacial signal is not connected to a cell. `WARNING(03-05):The following module port definition is/are not correct.` 
	*Specify –CHECK_3_6 to execute this check.	This check is only carried out when the option given at left has been selected. Cells' inout pins are checked for connection. A warning will be output when none of the inout pins of a cell instance is connected to a net or when the pins are not driving a cell although they are connected to a net. (No waning will be output if an inout pin is connected to the power supply or GND net. `WARNING(03-06):The following cell instance's inout pins are all dangling.` 

No	Items checked	Content of the check
4	Name rule check (Name Rule) Checking the names of instances, pins, blocks and nets (normal and power supply).	Checks based on the information in name_rule_check_file when it is defined. If not defined, the default information for name_rule_check will be used. As for the default, the reserved words of SystemVerilog and Shingen are checked. <Net name> ERROR(04-01):Nets with illegal names. ERROR(04-02):Nets with long names. ERROR(04-03):Nets with reserve names. ERROR(04-04):Leaf_nets with long names. <Instance name> ERROR(04-05):Instance with illegal names. ERROR(04-06):Instance with long names. ERROR(04-07):Instance with reserve names. ERROR(04-08):Leaf_instance with long names. <Port name> ERROR(04-09):Ports with illegal names. ERROR(04-10):Ports with long names. ERROR(04-11):Ports with reserve names. ERROR(04-12):Leaf_ports with long names. <Block name> ERROR(04-13):Block with illegal names. ERROR(04-14):Block with long names. ERROR(04-15):Block with reserve names. <External port name> ERROR(04-20):Top_module_ports with illegal names. ERROR(04-16):Top_module_ports with long names. <Top block name> ERROR(04-21):Top_module with illegal name. ERROR(04-22):Top_module with long name. (Note) * Escape identifiers will not be checked. * Generic names will be checked for bus descriptions. * Escaped bus descriptions (“·A[0]”) will be checked with the names (“A[0]”) that include a bus delimiter. However, if the bus description format is defined (BUS_DELM), the check will be based on the BUS_DELM information.
	*Specify –CHECK_4_17 to execute this check.	<Duplicated name> ERROR(04-17):Only the difference between a capital letter and a small letter *It is the check in the same category. The kind of the categories is instance name or net name or block name. Example) Attr ⇔ attr is same ←ERROR
	*Specify –CHECK_4_18 to execute this check.	ERROR(04-18):Same names are used instance names and net names. *Only the name of the exact match is the error. The small and capital letter is distinguished. Example1) in01d1 inst1(.i(inst1), .zn(inst2)) ; ←ERROR Example2) in01d1 Inst1(.i(inst1), .zn(inst2)) ; ←no ERROR
	*Specify –CHECK_4_19 to execute this check.	ERROR(04-19):Same names are used instance names and net names. *The small and capital letter is not distinguished. Example) in01d1 Inst1 (.i (inst1), .zn (inst2)) ; ←ERROR
		ERROR(04-23):Same names are used net names and busbit names. *The small and capital letter is distinguished. Example1) ¥A[0] ⇔ A[0] ←ERROR Example2) ¥a[0] ⇔ A[0] ←no ERROR (Note) This is default check, but it can cancel by -CANCEL_4_23.
	*Specify –CHECK_4_24 to execute this check.	ERROR(04-24):Same names are used net names and busbit names. *The small and capital letter is not distinguished. Example1) ¥A[0] ⇔ A[0] ←ERROR Example2) ¥a[0] ⇔ A[0] ←ERROR Example3) ¥A[0] ⇔ a[0] ←ERROR Example4) ¥Abc ⇔ ABC ←ERROR（Check same as 04-17.）

<table>
<tr><th>No</th><th>Items checked</th><th>Content of the check</th></tr>
<tr><td>5</td><td>Gate loop check
(Gate Loop)</td><td>An error will be output if a signal is fed back and hence a loop is being formed.
ERROR(05-01):Each of the following groups of cells makes up a loop.
 
*Paths that go through set and reset pins, such as flip-flops, are regarded as forming a loop.
*The select signal can be excluded from check by the PTshell specification of set_case_analysis.
*The latch go through in a condition of clock ON.

Please exclude loop that go through IO cell by one of the following methods.
(1) User mode setting by set_case_analysis
(2) set_string Stop_propagation_at_iocell yes ;

When there are multiple loops, only a representative loop is output.
To check whether other loops exist, please specify the following. The path that go through a specific terminal is excluded.
set_strings Stop_loop_check_term <instance term name> ;</td></tr>
<tr><td rowspan="2">6</td><td rowspan="2">Fanout check
(Fanout Restriction)</td><td>The following error will be output when the maximum fanout defined in the NetWalker library (max_fanout) has been exceeded.
ERROR(06-02)/(06-03):Max fanout exceeded.(Fanout Restriction)

-FOCHECK capacitance (default)
* The fanout check uses a total of normalized capacitance_load to carry out checks.

-FOCHECK numb
* The fanout check simply checks the number of fanouts.

* The check will not be carried out for pins without definitions on fanout restrictions. The following warning message will be output:
WARNING(06-01):Max fanout is not defined in Library.

* The default setting selects non-application of this check to the ports of the top-level modules. However, when ‘-TOP_MODULE_FANOUT_RESTRICTION Restriction value (real number)’ is specified with the command, all ports of the top-level modules will be checked against the given restriction value.
ERROR(06-04)/(06-05):Max fanout exceeded.(Fanout Restriction) for Module Port

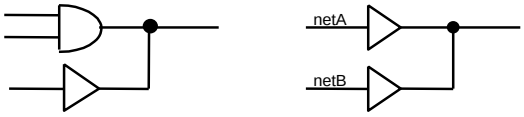
* This check is not applied to the cells of clock-trees for which clock-line checking has been specified.</td></tr>
<tr><td>The following error will be output when the maximum capacitance defined in the NetWalker library (max_capacitance) has been exceeded.
ERROR(06-07):Max capacitance exceeded.(Capacitance Restriction)

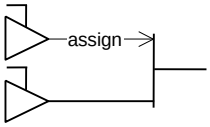
-FOCHECK pin_capacitance
* The capacitance check uses a total of capacitance of all input and bidirectional pin connecting with net to carry out checks.

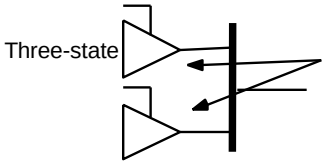
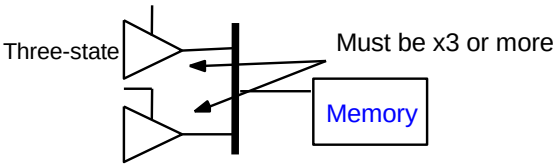
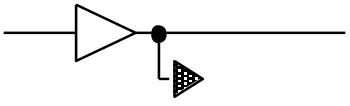
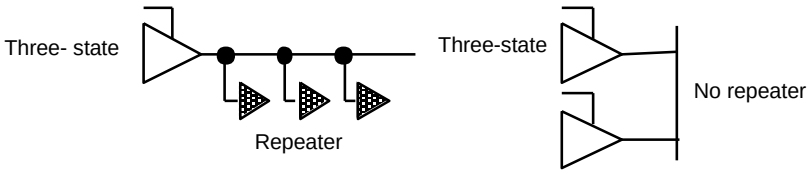
* The check will not be carried out for pins without definitions on capacitance restrictions. The following warning message will be output:
WARNING(06-06):Max capacitance is not defined in Library

* The default setting selects non-application of this check to the ports of the top-level modules. However, when ‘-TOP_MODULE_FANOUT_RESTRICTION Restriction value (real number)’ is specified with the command, all ports of the top-level modules will be checked against the given restriction value.
ERROR(06-08):Max capacitance exceeded.(Capacitance Restriction) for Module Port

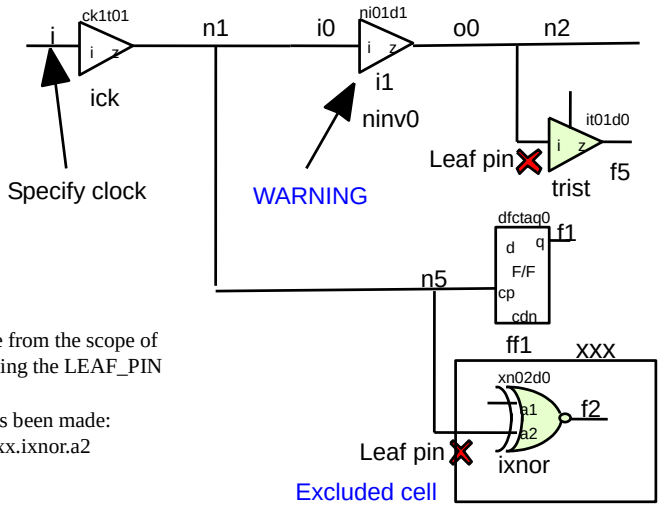
* This check is not applied to the cells of clock-trees for which clock-line checking has been specified.</td></tr>
</table>

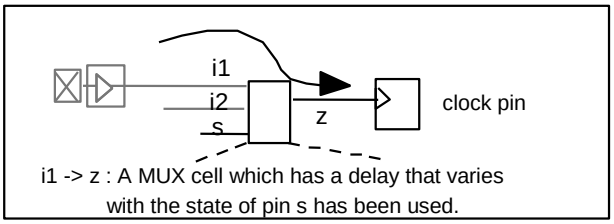
<table>
<tr><th>No</th><th>Items checked</th><th>Content of the check</th></tr>
<tr><td rowspan="3">7</td><td rowspan="3">Parallel Drive check
(Parallel Drive)</td><td>This check is for the parallel connection of cells.
ERROR(07-01):Parallel drive.
 

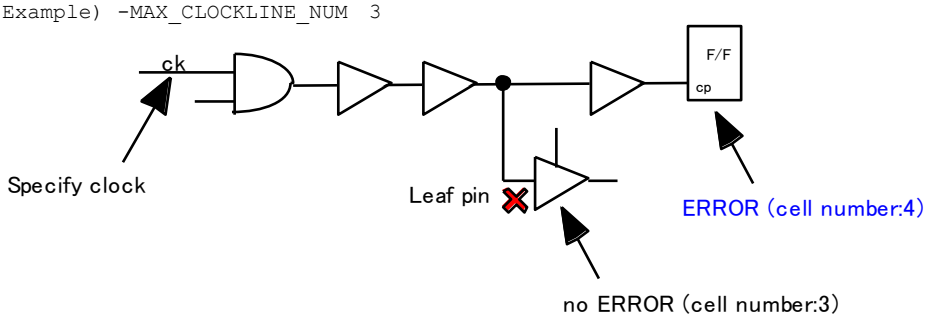
 

(Note) The change of a signal name by assign description has a case assigned to buffer cell by composition. Therefore assign description checks it as buffer cell. The left figure is recognized as a parallel drive.</td></tr>
<tr><td>*Specify –CHECK_7_2 to execute this check.</td><td>This check is only carried out when the option given at left has been selected.
Driver cells for a three-state bus must be of the same structure, which is a constraint required in TDD.
ERROR(07-02):Three state Bus needs same cell constitution.
 
</td></tr>
<tr><td>*Specify –CHECK_7_3 to execute this check.</td><td>This check is only carried out when the option given at left has been selected.
Since three-state buses (to which memory etc. is connected) will not be replaced by cells, cells with high driving capability must be used.
ERROR(07-03):Three state Bus which except three-state buffer/invert connected is necessary by x3 drived. (for TDD)
 
</td></tr>
<tr><td rowspan="2">8</td><td rowspan="2">Three-state / Bus repeater connection check
(Three-State/Bus Repeater)</td><td>Checks the connection of bus repeater cells. An error will be output when connected to a bus repeater cell.
ERROR(08-01):Out/inout signal should not be connected to a bus repeater cell.
 
</td></tr>
<tr><td>Checks the connection of bus repeater cells. A warning will be output when no repeater is connected to a Three state pin or more than one repeater are connected.
WARNING(08-02):Three-state signal not connected to bus repeater cell.
 
</td></tr>
</table>

No	Items checked	Content of the check

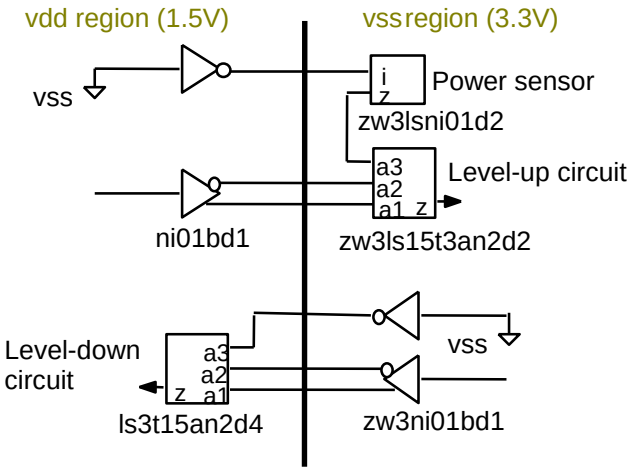
9	Clock-line check
	
	* This check is not possible unless –CLOCK_ROOT (clock signal) has been specified.
	* I/O cells are not checked. I/O cells should be checked by the primary I/O check.
	
	(Note) If permitted cell is the selector element, the connection to select pin will produce error.
	
	The NetWalker library of permitted cell has the attribute of "GATED_CLOCK".
	
	*When PRINT_09_01_PATH was specified, 09-01 displays the clock pass which is error. Following set_strings are the same, too.
	PRINT_09_02_PATH
	PRINT_09_03_PATH
	PRINT_09_04_PATH
		Cells not permitted in clock-tree synthesis (CTS) have been used on the clock line.
		`ERROR(09-01):Clock Line Check (Unused Cell)`
		
		Cells not permitted in layout have been used on the clock line.
		`WARNING(09-03):Clock Line Check (Unused Cell)`
		This warning message is output when any cell for which use as an inverter or buffer is not permitted. Inverters and buffers are automatically removed in CTS.
		
		 
		
		(Note) To exclude a specific route from the scope of checking, specify the cells' pin using the LEAF_PIN command.
		In the figure, this specification has been made:
		-LEAF_PIN trist.i -LEAF_PIN xxx.ixnor.a2

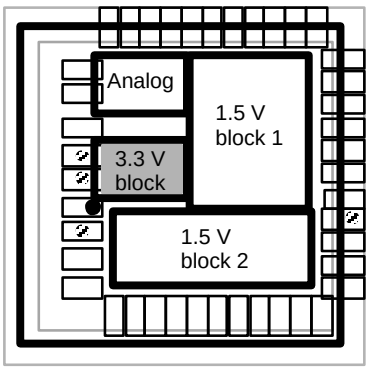
		This check is for cells that give paths state-dependent delays. `ERROR(09-02):Clock Line Check (state dependence delay Cell check)` 

	*Specify –MAX_CLOCKLINE_NUM to execute this check.	This check is only carried out when the option given at left has been selected.
		The cell number on the clock line has exceeded the specified number.
		`ERROR(09-04):Clock Line Check (gated cell number limit:3)`
		
		`Example) -MAX_CLOCKLINE_NUM 3`
		
		 

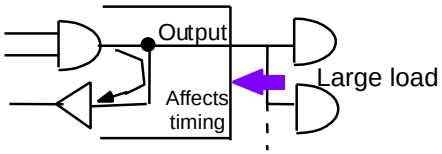
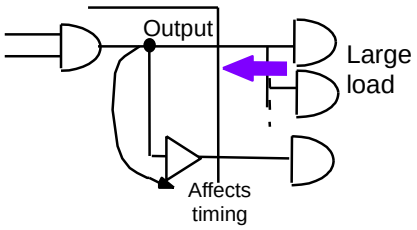
10	Assign check	An assign statement in which one side is tied to the power supply is used. `ERROR(10-01):assign Check (tied high/low) { example assign=1'b0 }` module BLK2 (); assign a= 1'b1 ; U81 BLK1(a,b,c) ; endmodule

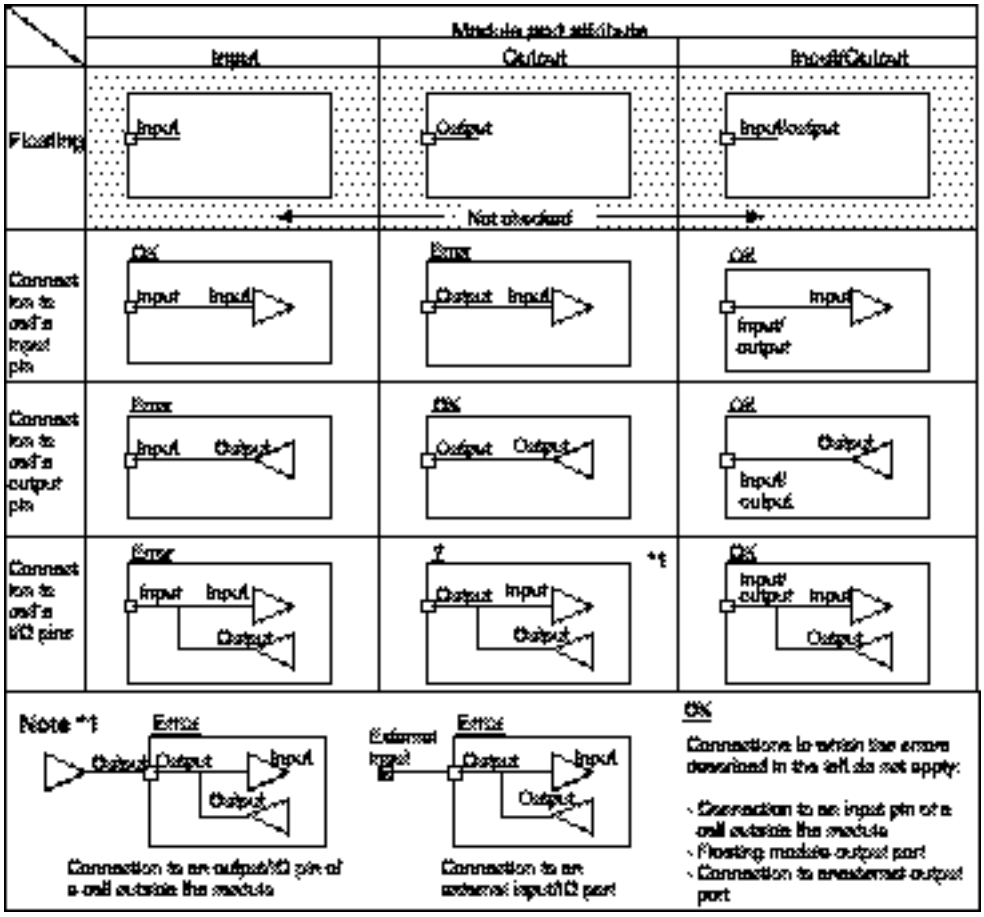
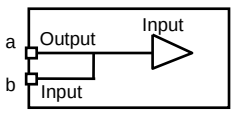
No	Items checked	Content of the check

11	Level shifter check
	(Level Shifter)
	(Check of multi-power supply design)
		This check is for connections between power supply lines that carry different voltages, i.e., it is used to ensure that circuits which carry different voltages are in the correct structures shown in the figure below.
		
		The following warning message is produced when the term “voltage” has not been defined in the library
		`WARNING(11-01):Term Voltage not defined in Library`
		
		Cell-to-cell connections of different voltages produce this error message.
		`ERROR(11-02):Voltage do not agree between Cells`
		
		Connections of level-down/up circuits’ pins are checked for errors.
		`ERROR(11-03):Connection of Level shift cells is mistaking`
		
		This error message is produced when an enable pin of a level-down circuit is not tied high by an inverter cell.
		`ERROR(11-04):Enable terminal of level-down circuit is not tied high by an inverter cell`
		
		Checks the connection of power switch sensor in the level-down circuit.
		`ERROR(11-05):Power switch sensor cell is not tied high by invert cell`
		
		Checks for prohibited combinations in the differential input section of the level-down circuit.
		`ERROR(11-08):Fixed logical value check in differential motion input circuit.`
		
		 

	* This check is only carried out when –CLAMPING_CHECK is specified.	Descriptions of local power-supply regions are checked for statements that create power clamping.
		`ERROR(11-06):This cell is clamped high by this voltage.`
		`WARNING(11-07):This cell is clamped low by this voltage.`
		
		In the case shown in the figure below, if the description of the local 3.3-V block region contains statements that create power clamping, that block might be connected to the 1.5 V power line.
		In this case, specify “–CLAMPING_CHECK 3.3” so that a check is carried out to find out if there is any “1b’ 0” or “1b’1” in the description of the 3.3-V region.
		
		 

No	Items checked	Content of the check

12	Top module port check
	(Top Module Port)
	
	* Modules immediately under top-level modules are checked.
	
	* This check is only carried out when –TOP_MODULE_PORT has been specified.
		This check is for output module ports which are connected to cells inside the module.
		Such structures tend to cause timing problems.
		`ERROR(12-01):Output module ports connected to inner cells`
		 
		
		 
		
		The following message will be output when a module has a port declared as both input and output.
		`WARNING(12-03):Mixing input and output port declaration`

13	Top module port check
	(Module Ports)
		This check is for consistency in the pin attributes of the module interface from an external pin to a cell. (Faults in the module port attribute that may cause problems with Prime Time are found out.)
		Connections between all module ports and the cells inside the module that are connected to the module ports are checked. Errors and warnings are based on the following table.
		`Error(13-01):The following module input port(s) should be connected to input pin(s).`
		`Error(13-02):The following module output port(s) should be connected to output pin(s).`
		 
		 
		
		(Note)
		In the case of multi-port connection coded as, for example, assign a=b;, if port a is connecting to a device`s input pin, HLDRC checks port a but not port b. So, this check should be executed after solving the problem of through nets (ERROR(03-04)).

<table>
<tr><th>No</th><th>Items checked</th><th>Content of the check</th></tr>
<tr><td>14</td><td>Restricted cells check
(Restriction Cells)

*Specify
–RESTRICTION_CELL_
CHECK to execute this check.</td><td>There is a possibility that cells containing pass transistors are automatically introduced during automatic layout.
This check finds such unusable cells (checks whether the cell type of the NetWalker is “DNT_USE”).
ERROR(14-01):Restriction cells

In case of adding cells to check, create elow file and specify the file with below option.

-RESTRICT_CELL_CHECK Restriction_cells_list1 ¥
-RESTRICT_CELL_CHECK Restriction_cells_list2 ¥

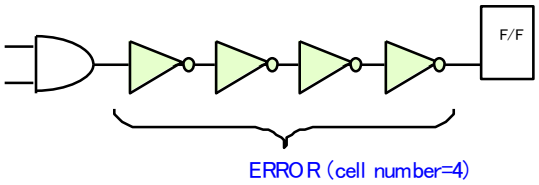
Filename : Restriction_cell_list1

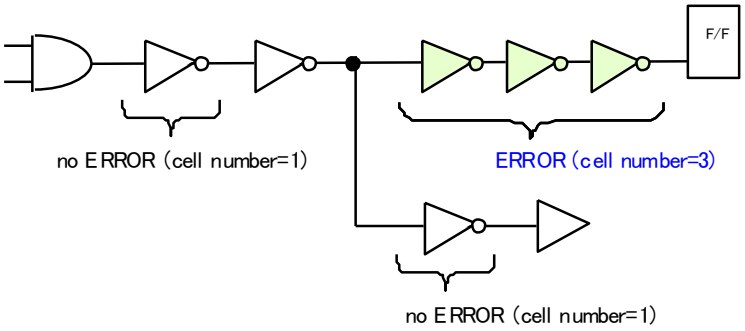
//comment
cell_name1 cell_name2 // comment
cell1_na*

// ~ [return] treats as comment line.
Only space or tab is available between specified cell name.
Wildcard is available only on ending of a word.</td></tr>
<tr><td>15</td><td>Fixed signal connect check
(Fixed signal)
*Specify
–FIXED_SIG_CHECK
to execute this check.</td><td>In TSMC, fixation of a signal by 1’b0/1’b1 is prohibited.
ERROR(15-01):Connected fixed signals.</td></tr>
<tr><td>16</td><td>Inverter Chain check

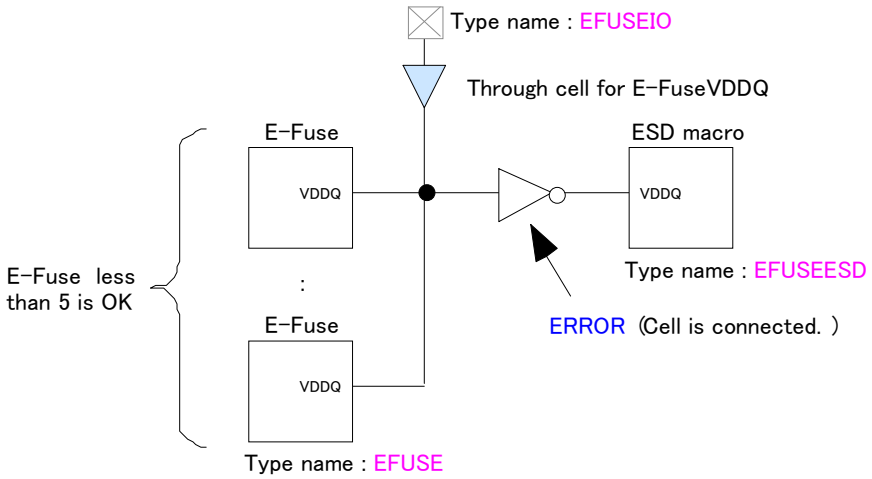
*Specify
–CHECK_16_1 to
execute this check.</td><td>The cell number which connected continually of the inverter has exceeded the specified number.
ERROR(16-01):Inverter Chain Check (inverter number limit:20)

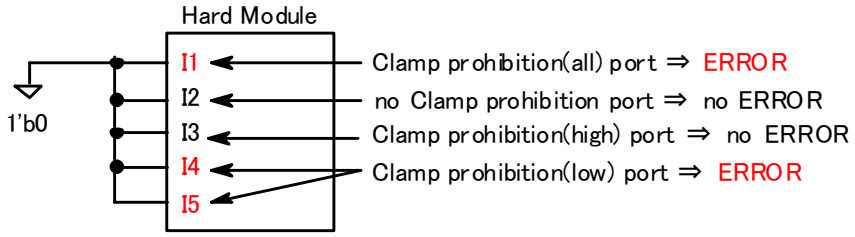
*Specify the cell number with -CHECK16_MAX_INV_NUM. (default is 20)

-CHECK16_MAX__INV_NUM 2
Example1)
 

Example2) fantou net: It is checked separately in divided front and back.
 
</td></tr>
</table>

No	Items checked	Content of the check

17	E-Fuse connectcheck
	(E-Fuse connection)
	
	*Specify –CHECK_17_1 to execute this check.
		The connection of E-Fuse is not correct.
		ERROR(17-01):E-Fuse Connection Check
		
		<Check Contents>
		(1) VDDQ attribute pin of E-Fuse connects with VDDQ attribute pin of ESD macro directly.
		(2) VDDQ attribute pin of E-Fuse connects with pad.
		Or it connects to the pad via the through cell for E-Fuse VDDQ.
		*Connection except the through cell for E-Fuse VDDQ is prohibition.
		(3) The logic cell (BUF/INV etc.) must not connect with VDDQ attribute pin of E-Fuse.
		*But the through cell for E-Fuse VDDQ is excluded
		(4) The number of E-Fuse connecting to one pad is less than 5 (default).
		The number for T28 is 8. (VDDQ attribute pin of E-Fuse is defined as input_max=8.)
		
		<NetWalker Library>
		ZWGEFVDDQSG {type=IO,0,EFUSEIO;
		EFUA15PP00000ZZ0ZZ {type=MODULE,REG,EFUSEESD;
		pin(EFUSEVDDQ =VDDQ ;);
		:
		
		EFUA15PPFF010ZZ0ZZ {type=MODULE,REG,EFUSE;
		pin(EFUSE_VDDQ =VDDQ ;);
		connect (EFUSE_VDDQ (direction=input;;input_max=8;);
		 

No	Items checked	Content of the check
18	Clamp connect check (Clamp connection) *Specify –CHECK_CLAMP to execute this check.	The ports of hard module prohibiting direct clamp(1'b0/1'b1) are fixed the logic. ERROR(18-01):The module ports are clamped directly. *The Pin setting the following clamp_fatal attribute in NetWalker library is checked. This is the pin needing the logic fixation that go through buffer because there is a problem (electrostatic breaking test (ESD)) of the device. < NetWalker Library > MOD {type=MODULE,REG; connect(I1 (voltage=1.5;direction=input;clamp_fatal=all;); ← Clamp(H/L) prohibition I2 (voltage=1.5;direction=input;); I3 (voltage=1.5;direction=input;clamp_fatal=high;); ← Clamp prohibition of H side I4 (voltage=1.5;direction=input;clamp_fatal=low;); ← Clamp prohibition of L side I5 (voltage=3.3;direction=input;clamp_fatal=low;); ← Example) -CHECK_CLAMP_POST  (Note) The case connected to the TieH/L cell is error, too. (The TieH/L cell is cell setting the attribute of PULLUP/PULLDOWN in NetWalker library.) **For the check exclusion of the TieH/L cell, please specify -CANCEL_CLAMP_TIE_CELL option.** *The hard module that the type attribute of the NetWaler library is "MODULE" is checked. Please specify the file which defined the following by -PTSHELL to check other cells. (1) Check of the specific cell add_cell_type <cell name> CHKCLAMP ; (2) Check of the specific instance add_instance_type <instance name> CHKCLAMP ;

No	Items checked	Content of the check
18		*The NetEdit+ script which inserts cell to the error port is created automatically. The script name is hldrc_clamp.tcl. Please revise the net by NetEdit+.

```
< hldrc_clamp.tcl >
#####################################################
# Direct Clamp ERROR                                #
# Plsease set cell_name(xxxxx) and cell_term(xx)    #
#####################################################
 set_delimiter .
### Cell Information of 1.5v ###
 set cell_name0       xxxxx
 set ctype0(@cell) $cell_name0
 set ctype0(xx)       @th_in
 set ctype0(xx)       @th_out
### Cell Information of 3.3v ###
 set cell_name1       xxxxx
 set ctype1(@cell) $cell_name1
 set ctype1(xx)       @th_in
 set ctype1(xx)       @th_out
                :
 insert_gate { {inst0.I1} {inst0.I4} } ctype0 {CLAMP0_0_2}
 insert_gate { {inst0.I5} } ctype1 {CLAMP0_0_3}
                :
#####################################################
# Output verilog                                    #
# print_verilog_source file_name [module_name]      #
#####################################################
 print_verilog_source out.v
```

Cell for 1.5v

Cell for 3.3v

Insertion cell information of each voltage

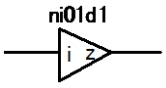
Insertion cell command of each voltage

Output netlist

■Please set the user condition to the script.

(1) xxxxx : Specify cell name to insert for each voltage.

```
set cell_name0       ni01d1
```



(2) xx : Specify pin name of cell to insert . (Set input pin and output pin in @th_in and @th_out each.)

```
set ctype(i)    @th_in
set ctype(z)    @th_out
```

■Output specification of NetEdit+ script

(1) The different cell is inserted for each voltage of the module port.

(2) One cell is inserted for each kind of clamp value in one module. The default of fanout restriction is 50. When ports more than 50 were clamped, plural cells are inserted to the net which diverged.

(3) The change of the fanout restriction is possible. Please specify the file which defined the following by -PTSHELL option.

```
set_numerical_value MAX_CLAMP <fanout number>;
```

(4) The cell is inserted to just the front of clamp port at the hierarchy same as the hard module.

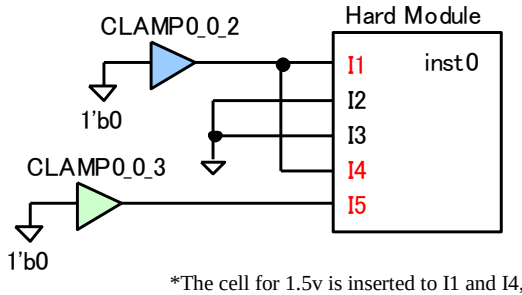
(5) The specifications of the cell insertion command are as follows.

```
[Format]     insert_gate    {<port name>}    <array name>    {<instance name>}
[Argument] <port name> : The port name list of the hard module to insert the same cell
           <array name > : The array name that defined the information of the cell to insert
           <instance name> : The instance name for the cell to insert
```

(6) The naming rule of the cell instance to insert is as follows. Because it is set to the third argument of insert_gate command, please change it if necessary.

"CLAMP<clamp value (0/1)>_< module ID number >_<port ID number >"

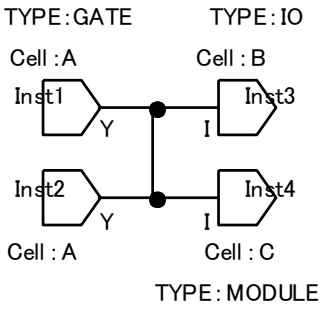
(7) The edited netlist is output to "out.v". Please change it if necessary.

No	Items checked	Content of the check
		■Execution example of NetEdit+ insert_gate { {inst0.I1} {inst0.I4} } ctype0 {CLAMP0_0_2} insert_gate { {inst0.I5} } ctype1 {CLAMP0_0_3}  *The cell for 1.5v is inserted to I1 and I4, and the cell for 3.3v is inserted to I5. (Refer to the script of the previous page.) ■Execution of NetEdit+ < Execution command of NetEdit+ > NetEdit+ ¥ -TOP top ¥ -NWCELL CELL_def ¥ -TCL hldrc_clamp.tcl ¥ ← Specify the script for net editing by –TCL option. test.v (Note) Please refer to the NetEdit+ operation manual for the details.

No	Items checked	Content of the check

19	Force connect check
	(Force connection)
		Connection relations do not obey specifications.
		`ERROR(19-01): Force connection check by the specification.`
		
		This check is carried out when the following definition was added in file to specify by -PTSHELL opion.
		set_strings FORCE_CONNECT ¥
		BASE {<cell name>} {<pin name>} ¥ <-- cell and pin name to check
		OPEN VALID ¥ <-- Float of output pin is no error.
		ANOTHER VALID ¥ <-- Connection except OBJECT is no error.
		GROUP [ALL| CELLPIN | ANY] ¥ <-- condition of connection
		OBJECT [{ cell name that is connected } | {TYPE: <type name>} {<pin name>}] * ¥
		MESSAGE <text message> ; <-- additional message
		
		*The pin of cell specified in BASE must connect with one of cell specified in OBJECT.
		
		*The default of OPEN and ANOTHER is INVAID.
		In addition, OPEN of input pin is not checked.
		
		*The cell name and the pin name can use wild card.
		These can use the regular expression, too. However specifications of –regexp and curly brace ({}) are necessary.
		Example) OBJECT { -regexp [A|B|C] } I
		Note) The meaning of % and * in the regular expression is different from GateDRC.
		
		*Type name of the NetWalker library is possible to specify as the substitution of cell name.
		Specify type name like {TYPE: <type name>}.
		If type is set for instance or cell as follows, it is added in run time.
		add_cell_type <cel name> <type name to add > ;
		add_instance_type <instance name> <type name to add > ;
		
		*The terminal name beginning in # has the following meaning.
		#IN : all input pin of cell
		#OUT : all output pin of cell
		#BIDIR : all inout pin of cell
		#3ST : all 3state output pin of cell
		
		*In connection check, the pin attribute (input and output) is not considered.
		
		* The specifications of GROUP are as follows.
		ALL : BASE must connect to all instance in OBJECT.
		CELLPIN : BASE must connect to all kinds of cell of OBJECT. <This is equal with ALL of GateDRC.>
		ANY : BASE must connect with one of OBJECT. <This is equal with ANY of GateDRC.>
		
		If GROUP is ALL and the pin name is "*", the following error is output in log.
		`ERROR NOT support FORCE_CONNECT %s %s -> %s %s at GROUP ALL`
		
		If GROUP is ALL and OPEN is VALID, the following error is output in log.
		In addition, it is similar when GROUP is CELLPIN and OPEN is VALID.
		`ERROR NOT support FORCE_CONNECT 'OPEN VALID' at 'GROUP ALL'/'GROUP CELLPIN'`
		
		(Note) The definition order of the item has the following restrictions.
		First : BASE
		End : MESSAGE
		
		*As for OBJECT, plural definitions are possible.

No	Items checked	Content of the check
		Example1)




```
set_strings FORCE_CONNECT ¥
BASE A Y ¥
GROUP ALL ¥
OBJECT A Y   B I   C I ¥
MESSAGE "xxx" ;
```

○

```
set_strings FORCE_CONNECT ¥
BASE A Y ¥
GROUP ALL ¥
OBJECT B I   C I ¥
MESSAGE "xxx" ;
```

×

There is no definition of Inst2.

Note) Specifications are different from GateDRC.

```
set_strings FORCE_CONNECT ¥
BASE A Y ¥
GROUP ANY ¥
OBJECT B I   D I   E I ¥
MESSAGE "xxx" ;
```

×

There is the connection with OBJECT. However, because there is not the definition of ANOTHER, connection of Inst2 is NG.

```
set_strings FORCE_CONNECT ¥
BASE A Y ¥
ANOTHER   VALID   ¥
GROUP ANY ¥
OBJECT B I   D *   E * ¥
MESSAGE "xxx" ;
```

○

```
set_strings FORCE_CONNECT ¥
BASE A Y ¥
ANOTHER   VALID   ¥
GROUP ANY ¥
OBJECT D *   E I   ¥
MESSAGE "xxx" ;
```

×

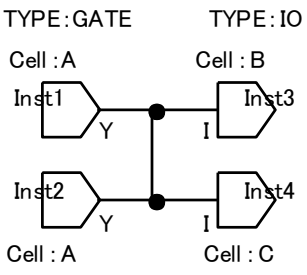
There is not connection with OBJECT.

```
set_strings FORCE_CONNECT ¥
BASE TYPE:IO * ¥
ANOTHER   VALID   ¥
GROUP ANY ¥
OBJECT TYPE:MODULE * ¥
MESSAGE "xxx" ;
```

○

Inst3 connects with Inst4.

Example2)




```
set_strings FORCE_CONNECT ¥
BASE A Y ¥
GROUP ALL ¥
OBJECT A Y   B I   C I ¥
MESSAGE "xxx" ;
```

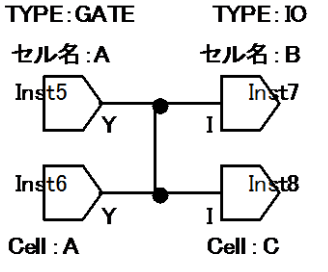
×

Inst1 connects with Inst2, but Inst1 does not connect with Inst5 and Inst6.

In addition, it connects with Inst3, but does not connect with Inst7.

It connects with Inst4, but does not connect with Inst8.

Inst2, Inst5, Inst6 are similar, too.



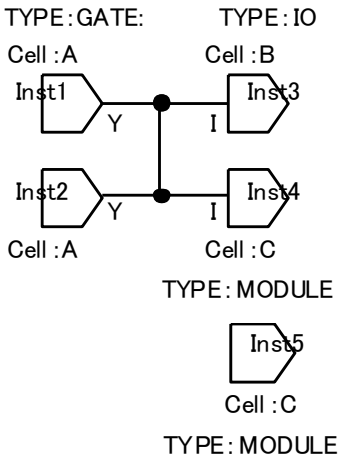

```
set_strings FORCE_CONNECT ¥
BASE A Y ¥
GROUP CELLPIN ¥
OBJECT A Y   B I   C I ¥
MESSAGE "xxx" ;
```

○

```
set_strings FORCE_CONNECT ¥
BASE A Y ¥
GROUP ANY ¥
OBJECT A Y   B I   C I   D I ¥
MESSAGE "xxx" ;
```

○

No	Items checked	Content of the check
19		Example) The difference of ALL and CELLPIN



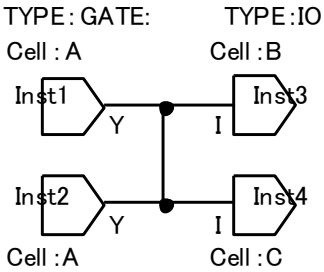

```
set_strings FORCE_CONNECT ¥
BASE A Y ¥
GROUP CELL ¥
OBJECT A Y   B I   C I ¥
MESSAGE "xxx" ;
```

All instance needs not to be connected.

```
set_strings FORCE_CONNECT ¥
BASE A Y ¥
GROUP ALL ¥
OBJECT A Y   B I   C I ¥
MESSAGE "xxx" ;
```

All instance should be connected.
Inst5 is not connected.

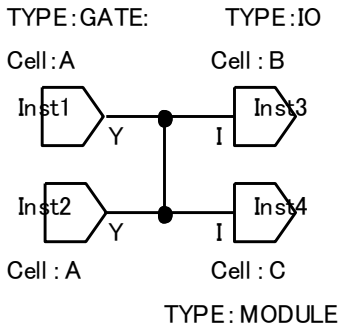
Example of the regular expression specification)




```
set_strings FORCE_CONNECT ¥
BASE A Y ¥
GROUP ALL ¥
OBJECT A Y   { -regexp [B|C] } I ¥
MESSAGE "xxx" ;
```

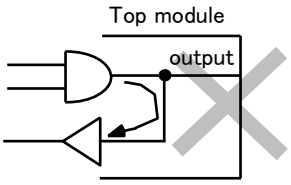
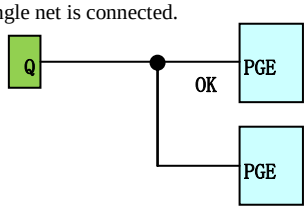
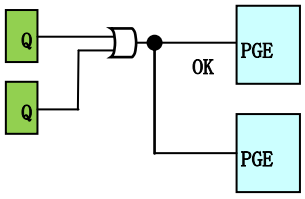
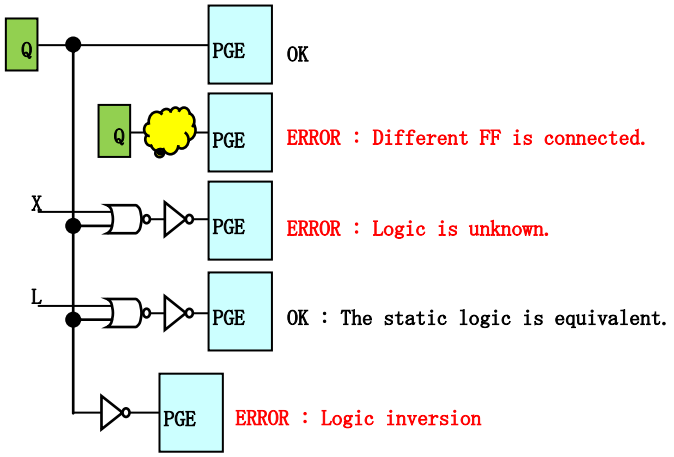
< Regular expression >
1. The characters to use in regular expression:
   . ^ $ [ ] * + ? | ( )
2. The kind of the meta-character
   (1) 1 character that is good in anything: .
   (2) The top and the last of the line: ^ $
   (3) The repetition of the same character: * + ?
   "*" means "the repetition more than 0 characters of a character in front".
   "+" means "the repetition more than 1 characters of a character in front".
   "?" means "the repetition more than 1 characters of a character in front".
   The repetition number "¥{m¥}" does not support.
   (4) The continuation of characters that is good in anything: .*
   (5) One of the designated characters: [ ]
   - If "^" was put in the top, it means "the character except the character following "^"".
   (6) Grouping: ( )
   (7) Either character string: |
   - Use it in the inside of grouping.
   (8) The escape of the meta-character: ¥
   - The meta-character can escape by putting backslash before the meta-character.

* In the case of external port, please specify EXT_PIN as cell name.
Example) BASE EXTPIN IN1

No	Items checked	Content of the check
20	Prohibit connect check (Prohibit connection)	There are connection relations of the prohibition obeying specifications. `ERROR(20-01): Prohibit connection check by the specification.` This check is carried out when the following definition was added in file to specify by -PTSHELL option. set_strings PROHIBIT_CONNECT ¥ BASE {<cell name>} {<pin name> } ¥ <-- cell and pin name to check OBJECT [{ cell name that is connected } | {TYPE: <type name> } {<pin name>}] * ¥ MESSAGE <text message> ; <-- additional message * The pin of cell specified in BASE must not connect with cell specified in OBJECT. *The cell name and the pin name can use wild card. These can use the regular expression, too. However specifications of –regexp is necessary. *Type name of the NetWalker library is possible to specify as the substitution of cell name. Specify type name like {TYPE: <type name>}. If type is set for instance or cell as follows, it is added in run time. add_cell_type <cel name> <type name to add > ; add_instance_type <instance name> <type name to add > ; *The terminal name beginning in # has the following meaning. #IN : all input pin of cell #OUT : all output pin of cell #BIDIR : all inout pin of cell #3ST : all 3state output pin of cell *In connection check, the pin attribute (input and output) is not considered. *As for OBJECT, plural definitions are possible. Example)  set_strings PROHIBIT_CONNECT ¥ BASE A Y ¥ OBJECT TYPE:RAM * ¥ MESSAGE "xxxx" ; set_strings PROHIBIT_CONNECT ¥ BASE A Y ¥ OBJECT C * ¥ MESSAGE "xxx" ; Inst1 connects with Inst4. (Note) For details, please refer to Chapter 6.12. Please refer to the appendix about the conversion from shampoo file.

No	Items checked	Content of the check
21	Use cell check (MustUse)	Terms of use do not obey specifications. ERROR(21-01):There is not it in terms of use in specifications. This check is carried out when the following definition was added in file to specify by -PTSHELL option. <more than minimum, and less than maximum > set_strings MUST_USE <min> <max> [<cell name>]* {} ; <use more than 1> set_strings MUST_USE 1 INF [<cell name>]* ; <use of less than 2 > set_strings MUST_USE 1 2 [<cell name>]* {} ; <use prohibition > set_strings MUST_USE 0 0 [<cell name>]* {}; *Please specify the minimum and the maximum that the use of cell is permitted. Finally please describe {} by all means. The omission is not possible When only one cell name was described, the number of the use of that cell is evaluated. When plural cell names was described, the total value of the number of the use of that plural cells is evaluated. Example1) The total number of cells should be less than max in min or more. Other than it is error. set_strings MUST_USE {min} {max} {cell name1} {cell name2} {cell name3} … { }; Example2) The total number of cells should be less than 5 in 1 or more. Other than it is error. set_strings MUST_USE {1} {5} {cell name1} {cell name2} {cell name3} { } ; →If the number of cells are (0,0,1) or (1,1,1) or (4,0,1), this case is not ERROR. If the number of cells are (0,0,0) or (2,2,2), this case is ERROR. Example3) The number of cells must be more than 1. The maximum does not have the limitation. set_strings MUST_USE {1} {INF} {cell name1} {cell name2} {cell name3} … { }; Example4) The number of cells should be less than 2 in 1 or more. set_strings MUST_USE {1} {2} {cell name1} {cell name2} {cell name3} … { }; Example5) use prohibition of cell set_strings MUST_USE {0} {0} {cell name1} {cell name2} {cell name3} … { };

22	Cell condition check
	(CellCondition)
		The error condition of the cell is not followed.
		ERROR(22-01):Cell Condition Check.
		
		When inputs (a1 and a2) of the differential circuit are 1 or 0 at the same time, shoot-through current flows.
		Therefore, this is prohibition condition.
		When library description has the following setting, check is executed according to condition.
		
		CellName {type=GATE,CHKCOND;
		area(1.666670);
		posi(a1->z; a2->z;);
		connect(a1 (direction=input;);
		a2 (direction=input;);
		z (direction=output;);
		function(z=a1&!a2;error_condition=(a1&a2)|(!a1&!a2););
		}
		
		⇒When the operation result of the logic set in error_conditon became 1, it is error because the error condition was met.
		
		*Set the error condition to error_condition.
		*Set the condition which is not error to need_condition. When the condition of need_conditon is not met, it is error.
		
		*When library description does not have the setting, please specify the file which defined the following by -PTSHELL option.
		add_cell_type CellName { CHKCOND } ;
		set_cell_function CellName { error_condition=(a1&a2)|(!a1&!a2); } ;

No	Items checked	Content of the check
23	ETM condition check (ETM) *Specify ETM_module in PTSHELL file to execute this check.	The output port is used as input in the inside of module. ERROR(23-01) : The output port(s) should be not connected to gates at ETM.  The execution of check needs the following definition. set_strings ETM_module yes ;
24	PGE terminal check (PGE)	The connection of PGE terminal is not correct. ERROR(24-01) : PGE term connection check PGE terminal of all memory should be the same logic from one same net or OR logic of same two net. RV40F SRAM has PGE terminal. PGE is the acceleration mode in Burn-in, and it is High at the time of acceleration. When it is High, reliability is in the extremely low condition. The cell that the type attribute is "PGE" is checked. <NetWalker Library> MEM1 { type=MODULE,REG,PGE; connect(PGE(direction=input;); } ■The single net is connected.  ■Two nets are connected.  Example) 

4. Command options

Command options used in HLDRC

hldrc_nw

[-64]	····· Specifies to execute on 64bit OS.
-TOP <top_module_name>	····· Specifies the top-level block.
[-RENEW]	····· Specifies to recompile.
[-WORK <work_directry>]	····· Specifies HLDRC's work directory (./work if omitted).
[-FOCHECK capacitance | numb | <fanout number > | pin_capacitance]	····· Specifies the fanout check mode (capacitance if omitted).
[-CLOCK_ROOT <clock_signal>]*	····· Specifies the clock root pin (if omitted, the clock line check cannot be performed).
[-LEAF_PIN <leaf_instance_pin>]*	····· Specifies to exclude a specific route from the scope of checking.
[-DIVIDER < / | . >]	····· Specifies the hierarchy delimiter (if omitted, ".").
[-NAMERULE <name_rule_file>]	····· Specifies the naming-rules file (if omitted, a default file is used).
[-PTSHELL <ptshell script file>]*	····· Specifies the ptshell file.
[-F <hldrc command file>]*	····· Specifies the command file for HLDRC commands. (See the next page for details.)
[-MAXNAMEERR <number>]	····· Specifies the max. number of naming rule errors (100 if omitted).
[-MAXERR <number>]	····· Specifies the max. number of the error detection number. (1000 if omitted) All errors are output by appointing 0.
[-CHECK16_MAX_INV_NUM <number>]	·····Specifies the max. number of the inverter chain. (20 if omitted)
[-PROCESS <number>]	·····Specify the numbers of the process (machine), if you execute by multi-processing. (Default is 1. Maximum is 5.) [Note] When the numbers of the process (machine) are not specified by -n option of bs command, execution may dump core because of memory lack.

<<Library Command>>

[-NWCELL <NetWalker_Lib>]*

<<Message output cancel command>>

[-CANCEL_SHORTS]	····· Specifies the cancellation of individual checks.
[-CANCEL_DANGLING]	
[-CANCEL_PRIMARY]	
[-CANCEL_FANOUT]	
[-CANCEL_THREE]	
[-CANCEL_NAME]	
[-CANCEL_PARALLEL]	
[-CANCEL_LOOP]	
[-CANCEL_CLOCK]	
[-CANCEL_LEVELSHIFT]	
[-CANCEL_SENSIBILITY_PIN_CHECK <Bi-Direction_IO_Cell>]	
[-CANCEL_MODULE_PORT]	
[-CANCEL_1_2]	····· Specifies the partial cancellation of individual checks.
[-CANCEL_2_8]	
[-CANCEL_2_11]	
[-CENCAL_3_4]	
[-CANCEL_3_5]	
[-CANCEL_4_23]	
[-CANCEL_CLAMP_TIE_CELL]	····· The TieH/L cell is not error in clamp check.

<< Name rule>>

[-CANCEL_NAMERULE_SYSTEMVERILOG] ····· Specifies the cancellation of SINGEN netlist check.
[-CANCEL_NAMERULE_SINGEN] ····· Specifies the cancellation of TESTACT netlist check.
[-CANCEL_NAMERULE_TESTACT]

<<Check execution command>>

[-TOP_MODULE_FANOUT_RESTRICTION *limit value (real number)*]
·····Selects checking of the degrees of fanout from ports.
[-TOP_MODULE_PORT] ·····Selects the module-port check.
[-CLAMPING_CHECK *violation voltage value (real number)*]*
·····Selects checking for clamped states.
(in multi-power supply design)
[-RESTRICTION_CELL_CHECK [cell_file]]* ·····Selects checking for cells that cannot be used.
[-FIXED_SIG_CHECK] ·····Selects checking for TSMC. (signal fixation check)
[SET_CELL_ATTR [fanout_file]] ……Specifies the file to modify fanout constraint.

[-CHECK_2_9] ····· Specifies checking of individuals.
[-CHECK_2_10]
[-CHECK_3_2]
[-CHECK_3_3]
[-CHECK_3_6]
[-CHECK_4_17]
[-CHECK_4_18]
[-CHECK_4_19]
[-CHECK_4_24]
[-CHECK_7_2]
[-CHECK_7_3]
[-CHECK_16_1]
[-CHECK_17_1]
[-CHECK_CLAMP]
[-MAX_CLOCKLINE_NUM <number>] ····· Specifies the cell number limit on the clock line.

<<Output control command>>

[-LOG <output_file>] ·····Specifies the file to hold the results of execution (default: log).
[-HLDRCFILE <result_output_file>] ·····Specifies the file to hold the results of checks (default: hldrc.log).
[-OUTPUT_CONTROL <output control file>]*·····Specifies the file used to prevent the re-output of check-result messages (default: file not output).
[-REVIEW_DELETE_FILE <review delete_file>] ·····Should be specified when removed error messages are to be output to a separate file (default: file not output).
[-DFILE <cell_defince_output_file>] ·····Specifies the cell-definition information file (default: file not output).
[-BLKDFILE <block_defince_output_file>] ·····Specifies the block-definition information file (default: not output).
[-BLKHFILE <block_hierachical_output_file>] ·····Specifies the block-hierarchy information file (default: not output).
[-BLKHFILE_TOP <module_instance_name>] ·····Block-hierarchy information: Module at start of output (default: top-level module)
[-BLKHFILE_HIER_NUM <hierachy_number>] ·····Block-hierarchy information: The number of levels in the hierarchy to be output (default: all levels).
[-GATE_ADJUST <Gate adjustment coefficient>] ·····Specifies the number of the conversion gates adjustment coefficient. (Multiplication)

<<Command option for Verilog version>> *See the next page for details.*

[-f <command_file_name>]*
[-v <source_file_name>]*
[-y <library_path_name>]*
[+libext+<.ext>]*
[+define+<define>[=value]>]*
[Verilog_source_file ...]+

[ ]: Omission is possible.
[ ]*: Zero or more can specify.
[ ]+: One or more can specify.

<<-F command option>>

■ [-F <hldrc command_file_name>]*

Specifies the command file name. HLDRC command options can be described in this file.
Comments can be inserted using '#' or '//' (they can be inserted in the middle of a line as well as at the head of a line).

Example: hldrc_nw -F cmmand_file

Content of command_file

```
-FOCHECK numb
-LEAF_PIN     k1_cell_2/a1
-LEAF_PIN     k1_cell_0_3/i
-CANCEL_SENSIBILITY_PIN_CHECK    k1_cell_10
-HLDRCFILE /work10/m2100a/hldrc.log
-DFILE        /work10/m2100a/hldrc_d.log
-BLKDFILE /work10/m2100a/hldrc_blkdf.log
-BLKHFILE    /work10/m2100a/hldrc_blkh.log
-WORK ./work_h
-TOP counter
-NWCELL CELL_def
counter.v
```

<<Verilog version command option>>

■ [-f <command_file_name>]*

Specifies a command file name. Only command options for Verilog/VHDL can be described in this file. Comments can be inserted using # or // (they can be inserted in the middle of a line as well as at the head of a line).
This option is only applicable to Verilog/VHDL commands.

■ [-v <source_file_name>]*

Specifies a Verilog model description file such as a Verilog net file and compiled RAM to be input. Can be specified more than once.

■ [-y <library_path_name>]*

Specifies the directory of model libraries for Verilog. It is used for Verilog source file analysis. Can be specified more than once.

■ [+libext+<.ext>]*

Defines the extension of a Verilog model library file name. Can be specified more than once.
Example: when libext+.ismvmd is specified, xxxxx.ismvmd will be the model file name.

■ [+define+<define>[=value]>]*

Verilog's 'define' specification. Can be specified more than once.
Example: +define+BUS_WIDTH=8

■ [Verilog source file…]+

Specifies Verilog net files to be input. More than one file can be specified. This is equivalent to the specification using the –v option.

Note: The input of the compressed file by gzip is possible.

5. Naming-rules file

This file is setting the limitation value of the name rule check.
The default value is listed in the next page. When you check by individual limitation, please change the limitation value.

- MAX_HIER_NAME_LENGTH

Defines the max number of characters for the absolute path name of an instance, net, port or block.

- MAX_LEAF_INSTANCE_NAME_LENGTH

Defines the max number of characters for an instance name.

- MAX_LEAF_NET_NAME_LENGTH

Defines the max number of characters for a net name.

- MAX_LEAF_PORT_NAME_LENGTH

Defines the max number of characters for a port name.

- MAX_BLOCK_NAME-LENGTH

Defines the max number of characters for a block name.

- MAX_TOP_MODULE_NAME_LENGTH

Defines the max number of characters for the top block name.

- MAX_TOP_MODULE_PORT_NAME_LENGTH

Defines the max number of characters for the external port name.

- INSTANCE_NR

Defines the valid expression of the name rule for instance names.

- NET_NR

Defines the valid expression of the name rule for net names.

- PORT-NR

Defines the valid expression of the name rule for port names.

- BLOCK_NR

Defines the valid expression of the name rule for block names.

- TOP_MODULE_NR

Defines the valid expression of the name rule for the top block name.

- TOP_MODULE_PORT_NR

Defines the valid expression of the name rule for the external port names.

- MAX_ERR_OF_NAME_RULE

Defines the max number of errors output in the name rule check.

- reserved_words_ins[]

It is checked whether the words which defined in the array as instance names overlap. Plural names can specify.

- reserved_words_net[]

It is checked whether the words which defined in the array as names of nets or ports overlap. Plural names can specify.

- reserved_words_ins_block[]

It is checked whether the words which defined in the array as block names overlap. Plural names can specify.

Example of naming-rules file description

```
`define MAX_LEAF_INSTANCE_NAME_LENGTH 255
`define INSTANCE_NR      "[a-zA-Z][a-zA-Z0-9_]*"
`define NET_NR           "[a-zA-Z][a-zA-Z0-9_¥[¥]]*"
```

Default description

```
// Maximum length of full pathname of insts/nets/ports
  `define MAX_HIER_NAME_LENGTH          1024
// Maximum name length of leaf insts/nets/ports and module
  `define MAX_LEAF_INSTANCE_NAME_LENGTH    511
  `define MAX_LEAF_NET_NAME_LENGTH       511
  `define MAX_LEAF_PORT_NAME_LENGTH      511
  `define MAX_BLOCK_NAME_LENGTH          233
  `define MAX_TOP_MODULE_NAME_LENGTH     120
  `define MAX_TOP_MODULE_PORT_NAME_LENGTH   472
// Rules for valid instance/net/port/module names
  `define INSTANCE_NR              "[a-zA-Z][a-zA-Z0-9_]*"
  `define NET_NR                   "[a-zA-Z][a-zA-Z0-9_¥[¥]]*"
  `define PORT_NR                  "[a-zA-Z][a-zA-Z0-9_¥[¥]]*"
  `define BLOCK_NR                 "[a-zA-Z][a-zA-Z0-9_]*"
  `define TOP_MODULE_NR            "[a-zA-Z][a-zA-Z0-9_]*"
  `define TOP_MODULE_PORT_NR       "[a-zA-Z][a-zA-Z0-9_]*"
  `define MAX_ERR_OF_NAME_RULE      100

string SystemVerilog[] = {
"always","and","assign","attribute","begin","buf","bufif0","bufif1","case","casex","casez",
"cmos","deassign","default","defparam","disable","edge","else","end","endattribute","endcase",
"endfunction","endmodule","endprimitive","endspecify","endtable","endtask","event","for",
"force","forever","fork","function","highz0","highz1","if","ifnone","initial","inout","input",
"integer","join","large","macromodule","medium","module","nand","negedge","nmos","nor","not",
"notif0","notif1","or","output","package","parameter","pmos","posedge","primitive","pull0",
"pull1","pulldown","pullup","rcmos","real","realtime","reg","release","repeat","rnmos","rpmos",
"rtran","rtranif0","rtranif1","scalared","signed","small","specify","specparam","strength",
"strong0","strong1","supply0","supply1","table","task","time","tran","tranif0","tranif1","tri",
"tri0","tri1","triand","trior","trireg","unsigned","use","vectored","wait","wand","weak0",
"weak1","while","wire","wor","xnor","xor" } ;

string singen[] = {"HT_TPI_FF_Cell_*","HT_TPI_INV_Cell_*",
                   "HT_TPI_FF_Net_*","HT_TPI_INV_Net_*",
                   "HT_MPI_AND_Cell_*","HT_MPI_AND_Net_*" } ;

string TESTACT[] = {"TESTACT_*"} ;

string netwalker[] = {"assignbuf"} ;

// Reserved words - this net names is only permitted the Power supply names
   string reserved_words_vdd[], reserved_words_vss[] ;

// Reserved words
   long nrins=0, nrnet=0, nrblk=0 ;
   string reserved_words_ins[], reserved_words_net[], reserved_words_block[] ;

`ifdef Cancel_NameRule_SystemVerilog
`else
// SystemVerilog
   for (i=0;SystemVerilog[i]!=0;i++) {
     reserved_words_ins[nrins++]   = SystemVerilog[i] ;
     reserved_words_net[nrnet++]   = SystemVerilog[i] ;
     reserved_words_block[nrblk++] = SystemVerilog[i] ;
   }
`endif

`ifdef Cancel_NameRule_SINGEN
`else
// singen
   for (i=0;singen[i]!=0;i++) {
     reserved_words_ins[nrins++]   = singen[i] ;
     reserved_words_net[nrnet++]   = singen[i] ;
   }
`endif
```

(Note) After SINGENexecution, Shingen limitation net is generated Please specify –CANCEL_NAMERULE_SINGEN option at command.

```
`ifdef Cancel_NameRule_TESTACT
`else
// TESTACT
   for (i=0;TESTACT[i]!=0;i++) {
     reserved_words_ins[nrins++]   = TESTACT[i] ;
     reserved_words_net[nrnet++]   = TESTACT[i] ;
   }
```

(Note)After TESTACT execution, TESTACT net is generated Please specify –CANCEL_NAMERULE_TESTACT option at command.

6. INPUT File

6.1 PTSHELL File

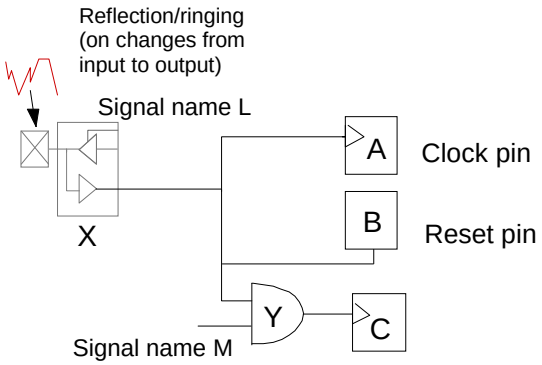
6.1.1 set_case_analysis

The PTSHELL file is used to specify the fixityof signals.
This file can be used instead of the -CANCEL_SENSIBILITY_PIN_CHECK command option to cancel checking for the connection of sensibility pins with bi-directional pad pins, which is otherwise carried out as part of the primary input/output check.

set_case_analysis [1/0] Signal name

Example) Primary input/output check (Primary Signals)

A bi-directional pad pin of an I/O cell should not be connected to a sensibility pin.



(1) Canceling the checking of element X and all the elements downstream of X (signal direction is fixed by assigning a fixed value to the I/O cell's output-enable signal).
set_case_analysis 1 L

(2) Canceling the checking of element C (the output of AND gate Y is tied low by assigning 0 to the signal M).
set_case_analysis 0 M

6.1.2 set_strings

The PTSHELL file is used to specify the check condition of HLDRC.

set_strings <key> <parameter_list> [-hsc <delimiter>]

The delimiter of key is able to define by -hsc individually.
When different delimiter is defined in same key, the last designation is effective.

Example) Generally delimiter is "/". But delimiter of DFILE is ".".
```
set_delimter {/} ;
set_strings DFILE B.D -hsc {.} ;
```

(1) FORCE_CONNECT
This is necessary for the forced connection check (19-01).

```
set_strings FORCE_CONNECT ¥
    BASE {<cell name>} {<pin name>} ¥      <-- cell and pin name to check (The omission is impossible.)
    OPEN VALID ¥                           <-- Float of output pin is no error. (The omission is possible.)
    ANOTHER VALID ¥                        <-- Connection except OBJECT is no error. (The omission is possible.)
    GROUP [ALL| CELLPIN | ANY] ¥           <-- condition of connection (The omission is possible.)
    OBJECT [ { cell name that is connected } | {TYPE: <type name>} {<pin name>} ] * ¥
                                           <-- plural definitions are possible. (The omission is possible.)
    MESSAGE <text message> ;               <-- additional message (The omission is impossible.)
```

- The default of OPEN and ANOTHER is INVAID.
- In addition, OPEN of input pin is not checked.

- The cell name and the pin name can use wild card.
- These can use the regular expression, too. However specifications of –regexp is necessary.

- The specification order of each keyword is arbitrary. But please specify MESSAGE last.
- MESSAGE is impossible of omission. When the output of the message is unnecessary, please specify "MESSAGE {};".

Example1) Wild card
```
set_strings FORCE_CONNECT ¥
    BASE {QNSA3N064K0V1} {VCPHV} ¥
    OBJECT {QNSB3N*K0V1} {VCPHV} {QNSC3NCP0V1} {VCPHV} ¥
    MESSAGE "in violation in the conditions of connection specification." ;
```

Example2) Regular expression
```
set_strings FORCE_CONNECT ¥
    BASE {-regexp Q[BIO].*} {DOUT} ¥
    OBJECT {TBCL*} {*} {Q*} {*5V} {Q*} {*3V} {Q*} {*HV} ¥
    MESSAGE "violation in the conditions of connection specification." ;
```
(Note) {-regexp Q[BIO].*} is equivalent to QBABC,QIXYZ,QOO,etc. If anything is good, it is ".*".

(2) PROHIBIT_CONNECT
This is necessary for the prohibited connection check (20-01).

```
set_strings PROHIBIT_CONNECT    ¥
      BASE    {<cell name>} {<pin name> }    ¥      <-- cell and pin name to check (The omission is impossible.)
      OBJECT    [ { cell name that is connected } | {TYPE: <type name> } {<pin name>} ] *    ¥
                                                    <-- plural definitions are possible. (The omission is possible.)
      MESSAGE    <text message> ;                   <-- additional message (The omission is impossible.)
```

- The cell name and the pin name can use wild card.
- These can use the regular expression, too. However specifications of –regexp is necessary.

- The specification order of each keyword is arbitrary. But please specify MESSAGE last.
- MESSAGE is impossible of omission. When the output of the message is unnecessary, please specify "MESSAGE {};".

Example1) Wild card

```
set_strings PROHIBIT_CONNECT ¥
      BASE {QNSA3N064K0V1} {VCPHV} ¥
      OBJECT    {QNSB3N*K0V1} {VCPHV} {QNSC3NCP0V1} {VCPHV} ¥
      MESSAGE "violation in the conditions" ;
```

Example2) Regular expression

```
set_strings PROHIBIT_CONNECT ¥
      BASE {-regexp Q[BIO].*} {DOUT} ¥
      OBJECT    {TBCL*} {*} {Q*} {*5V} {Q*} {*3V} {Q*} {*HV} ¥
      MESSAGE "violation in the conditions." ;
```

(3) DFILE
Specify module instance which output as additional information in information report file on use cell.

```
set_strings DFILE <module instance name> ;
```

- The module instance name can use wild card.

Example) Outputs all the module instance which exists on low rank hierarchy of the TOP.

```
set_strings DFILE {*} ;
        or
foreach i [ get_search block * ] {
   set_strings DFILE $i ;
}
```

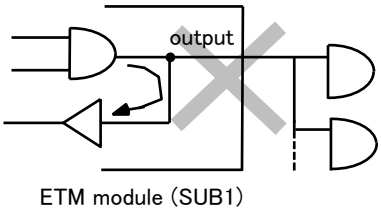
~~(4) 9_4_IGNORE_BUF_COUNT~~
~~This does not count buffer and inverter in clock line check (09-04).~~

~~set_strings 9_4_IGNORE_BUF_COUNT yes ;~~

(Note) This was changed to set_numerical_value. (Please refer to Chaper 6.1.3)

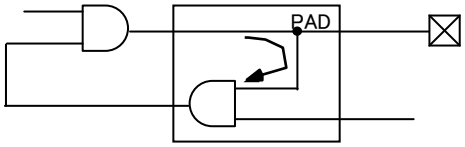
(5) ETM_module
Specify a module definition name to check in ETM condition check (23-01).

Example) set_strings ETM_module SUB1 ;



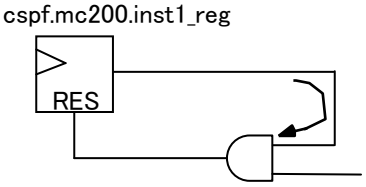
(6) Stop_propagation_at_iocell
The loop that go through the PAD terminal of I/O cell is excluded in the gate loop check (05-01).
Because a external port becomes the input and output combined use for test, a loop occurs.
If the logic is fixed to the user mode, the loop disappears. This is one of the exclusion methods of the loop.

Example) set_strings Stop_propagation_at_iocell yes ;



(7) Stop_loop_check_term
The loop that go through a specified terminal is excluded in the gate loop check (05-01).

Example) set_strings Stop_loop_check_term -hsc "." cspf.mc200.inst1_reg.RES ;
←The loop that go through "cspf.mc200.inst1_reg.RES" is excluded.



(8) PRINT_09_01/02/03/04_PATH
The search path is reported to error message in the clock line check (09-01/02/03/04).
Example) set_strings PRINT_09_04_PATH yes ;

```
ERROR(09-04) : Clock Line Check ( gated cell number limit:4)
   No. From net -> Instance_InPin=>OPin
 ------------------------------------------------------------------------------
   1 CLK g0.a1 (an02d1) [line 1:4]      ->   inst01.en (lacfnq0) [line 1:10]   number(5)
                  + EXT_PIN.CLK
                  + g0.a1 (an02d1)
                  + g0.z
                  + g1.i (in01d0)
                  + g1.zn
                  + g2.i (in01d0)          } The path is displayed.
                  + g2.zn
                  + g3.a1 (an02d1)
                  + g3.z
                  + g4.i (in01d0)
                  + g4.zn
```

6.1.3. set_numerical_value

(1) pt_flg_9_4_IGNORE_BUF_COUNT
If "1" was designed, Buffer / inverter is not counted in the clock line check (09-04).

set_numerical_value pt_flg_9_4_IGNORE_BUF_COUNT 1 ;

<Regular expression>
1. The characters to use in regular expression: . ^ $ [ ] * + ? | ( )
2. The kind of the meta-character
(1) 1 character that is good in anything: .
(2) The top and the last of the line: ^ $
(3) The repetition of the same character: * + ?
"*" means "the repetition more than 0 characters of a character in front".
"+" means "the repetition more than 1 characters of a character in front".
"?" means "the repetition more than 1 characters of a character in front".
The repetition number "¥{m¥}" does not support.
(4) The continuation of characters that is good in anything: .*
(5) One of the designated characters: [ ]
- If "^" was put in the top, it means "the character except the character following "^"".
(6) Grouping: ( )
(7) Either character string: |
- Use it in the inside of grouping.
(8) The escape of the meta-character: ¥
- The meta-character can escape by putting backslash before the meta-character.

6.2 SET_CELL_ATTR File

(1) When you change fanout restrictions, please create the following file and specify by -SET_CELL_ATTR.

<<Format>>
set_attribute library name / cell name / terminal name max_fanout value
(A numerical value can be defined as a variable like MAX_FANOUT_6x = 50.)

Example)

```
MAX_FANOUT_6x = 50
MAX_FANOUT_8x = 50
MAX_FANOUT_12x = 50
MAX_FANOUT_16x = 50
MAX_FANOUT_24x = 50

/* 0.5x */
set_attribute DPLIB_DP76CH12/zstsltcd1/q max_fanout MAX_FANOUT_05x
set_attribute hcos2083av/it02d0/zn max_fanout MAX_FANOUT_05x
set_attribute RC03ATBA_max/TBAADDFXA/COUT max_fanout MAX_FANOUT_05x
set_attribute RC03ATBA_max/TBAADDFXA/SUM max_fanout MAX_FANOUT_05x
set_attribute RC03ATBA_max/TBAADDHXA/COUT max_fanout MAX_FANOUT_05x
set_attribute RC03ATBA_max/TBAADDHXA/SUM max_fanout MAX_FANOUT_05x
                                    :
```

(2) When you change capacitanc restrictions, please create the following file and specify by -SET_CELL_ATTR.

<<Format>>
set_attribute library name / cell name / terminal name max_capacitance value
(A numerical value can be defined as a variable like MAX_CAPACITANCE_1 = 0.034.)

Example)

```
MAX_CAPACITANCE_1 = 0.034
MAX_CAPACITANCE_2 = 0.065

set_attribute DPLIB_DP76CH12/zstsltcd1/q max_capacitance MAX_CAPACITANCE_1
set_attribute hcos2083av/it02d0/zn max_capacitance MAX_CAPACITANCE_1
set_attribute RC03ATBA_max/TBAADDFXA/COUT max_capacitance 0.041
set_attribute RC03ATBA_max/TBAADDFXA/SUM max_capacitance 0.041
                                    :
```

7. Execution result output files

7.1 Error check result report file (-HLDCFILE)

Header info output — Command conditions are output.

```
//High-performance Logic Design Rule Checker -hldrc Version(V2.0)
//Ganerated at 00-03-25 13:24:22

Name Rule File:
        /sv1/takaha-gr/m2100a/svrf2/tools/NetWalker/HLDRC/FILE/namerules.vlog

Design Name:
        counter

Hierarchical Divider:
        /

Max Error of NameRule:
        10

Fanout Check Item:
        capacitance

Output Design Complexity Summary:
        /work10/m2100a/hldrc_d.log

Output Block Hierarchy List:
        /work10/m2100a/hldrc_blkh.log

Output Block Definition List:
        /work10/m2100a/hldrc_blkdf.log
```

ERROR/WARNIGN output ... Errors and warnings output by the hldrc checks.

Short-circuit message

```
shorts   check start ...(13:24:22)

ERROR : The following outpin pins are tied high/low:

   No. Cell Name  Pin Name  Instance Name
  ------------------------------------------------------------------------
  1 in01d1         zn        FIX_H
  2 in01d1         zn        FIX_L

WARNING : The following input pins are tied high/low:

   No. Cell Name  Pin Name  Instance Name
  ------------------------------------------------------------------------
  1 ni01d1         i         hierblk_i/DMY2
  2 in01d1         i         k1_block_1/err02_g05
  3 in01d1         i         k1_block_1/err02_g04
  4 in01d1         i         FIX_L
  5 in01d1         i         FIX_H
```

The output and power supply are short-circuited.

Primary message

```
primary  check start ...(13:24:22)

ERROR : The following primary input ports(s) should be connected to I/O buffer of pad
pin.

    Primary port  connected Port
  ------------------------------------------------------------------------
  1 data_in[5]
              E144/i (pt3o02a)
  2 data_in[7]
              E146/i (in01d0)
  3 k1_8
              k1_7 (INPUT)
              gk1_2/pad (pt3d01)
  4 k1_5
              k1_6 (INOUT)
  5 k1_1       (dangling)

ERROR : The following primary input ports(s) should be connected to input module port.

    Primary port  connected Port
  ------------------------------------------------------------------------
  1 k2_2       k1_block_1/in2 (INOUT)
  2 k2_1       k1_block_1/in1 (OUTPUT)

ERROR : The following I/O buffer siganls are dangling.

         Cell Name      I/O buffer . port
  ------------------------------------------------------------------------
  1          pt3d01    UNUSE_I/pad
  2         pt3o02a    UNUSE_O/i
  3         pt3b02a    UNUSE_B/i
```

Not connected to an IO cell's PAD pin.

More than one are connected. Not connected to an IO cell.

Not connected to a pin.

```
ERROR : The following primary output ports(s) should be connected to I/O buffer of pad
pin.

    Primary port     connected Port
  ------------------------------------------------------------------------
  1 unconnectnet       (dangling)

ERROR : The following primary output ports(s) should be connected to output module port.

    Primary port     connected Port
  ------------------------------------------------------------------------
  1 k2_3       k1_block_1/in3 (INPUT)

ERROR : The following primary inout ports(s) should be connected to I/O buffer inout
port.

    Primary port     connected Port
  ------------------------------------------------------------------------
  1 vdd
              NetName2/zn (in01d0)
              k1_block_1/vcc/pad (pt3b02a)
  2 k1_9        (dangling)

ERROR : The following primary inout ports(s) should be connected to module inout port.

    Primary port     connected Port
  ------------------------------------------------------------------------
  1 k1_19       (dangling)

ERROR : The following I/O buffer siganl should connect to primary port.

    I/O Instance Name (Cell Name)   Connect Instance.Ports(Cell)
  ------------------------------------------------------------------------
  1 E144(pt3o02a)
                                    U98/a1(aon222d1)

ERROR : The following I/O buffer all input siganls are tied high/low.

    I/O buffer  (Cell Name)
  ------------------------------------------------------------------------
  1  k1_cell_2(pt3b02a)

ERROR : The following I/O buffer output/inout siganls are tied high/low.

    Cell Name    I/O buffer       Pin Name
  ------------------------------------------------------------------------
  1 pt3b02a        cin              fix_io_i/FIX_B_PART
  2 pt3b02a        pad              fix_io_i/FIX_B_ALL

ERROR : The I/O buffer of inout pad should be not connected sensibility pin.

    I/O buffer (Cell Name )   Instance Pin (Cell Name)
  ------------------------------------------------------------------------
  1  kkk (pt3b01)  kk1_cell_3/cp (dfntnq0)
  2  kkk (pt3b01)  k1_cell_5/cp (dfntnq0)
  3  kkk (pt3b01)  k1_cell_7/cp (dfntnq0)
```

Dangling message

```
dangling check start ...(13:24:23)

ERROR : The following cell instance's input pins are dangling
    Cell Name     Pin Name      Instance Name
  ------------------------------------------------------------------------
  1 ni01d1            i          hierblk_i/DMY2
  2 an02d1            a2         UnuseGate

WARNING : The following cell instance's output pins are all dangling
    Cell Name     Pin Name      Instance Name
  ------------------------------------------------------------------------
  1 pt3b02a         cin           UNUSE_B
  2 pt3o02a         pad           UNUSE_O
  3 pt3d01          cin           UNUSE_I

WARNING : The following block instance pins are dangling
    Block Name     Pin Name      Instance Name
  ------------------------------------------------------------------------
  1 fanout_check_test1   o1       fanout_check1
  2 subloop              O1       UnuseHier

ERROR : The following module port definition is/are not connect
    Module_Name     Port   ---- Factor
  ------------------------------------------------------------------------
    1 ¥aaa_k1!        out, out2 --- Through net
    2 ¥aaa_k1!        VCC2 --- tied high/low
    3 fn04d0          thruin, thruout --- Through net

ERROR : The following module port definition is/are not connect
    Module_Name     Port  ---- Factor
  ------------------------------------------------------------------------
    1 fix_ext         B2  --- dangling net
```

Details are output to the Factor column.

Pins listed in the same line are module pins connecting a net.

The net name is output when a dangling net (the net is connecting to nothing) exists.

Naming rule message

```
name      check start ...(13:24:24)

ERROR : Nets with illegal names.(NET_NR=[a-zA-Z][a-zA-Z0-9_]*)
   No.    Net Name            Block Name
  ------------------------------------------------------
    1    \RemainSC.          counter
    2    \RemainSC$          counter
  ***** Max Name Rule(2) Error exceeded

ERROR: Nets with long names.(MAX_HIER_NAME_LENGTH=255)
   No.    Net Name * Block Name
  ------------------------------------------------------
    1
k1_block_1/aaaaaaaaaaaaaaaaaaaaaaaaaa/aaaaaaaaaaaaaaaaaaaaaaaaaaaaaa/aaaaaaaaaaaaaaa
aaaaaaaaaaaaaaa/aaaaaaaaaaaaaaaaaaaaaaaaaaaaaa/aaaaaaaaaaaaaaaaaaaaaaaaaaaaaa/aaaaaa
aaaaaaaaaaaaaaaaaaaaaaaaa/aaaaaaaaaaaaaaaaaaaaaaaaaaaaaa/aaaaaaaaaaaaaaaaaaaaaaaaaa
aaa/w * aaa_k8

ERROR : Nets with reserve names.
   No. Net Name              Block Name
  ------------------------------------------------------
    1 pdc             counter
    2 ndc             counter

ERROR : Leaf_nets with long names.(MAX_LEAF_NET_NAME_LENGTH=32)
   No.    Net Name            Block Name
  ------------------------------------------------------
    1
N23456789a123456789b123456789c123456789d123456789e123456789f123456789g123456789h123456789
i123456789j123456789k123456789l123456789m123456789n123456789o123456789p123456789q12345678
9r123456789s * counter

ERROR : Instance with illegal names.(INSTANCE_NR=[a-zA-Z][a-zA-Z0-9_]*)
   No.    Instance Name              Block Name
  ------------------------------------------------------
    1    \ErrNet;gate         counter
    2    \ErrNet,gate         counter

ERROR: Instance with long names.(MAX_HIER_NAME_LENGTH=255)
   No.    Instance Name * Block Name
  ------------------------------------------------------
    1
k1_block_1/aaaaaaaaaaaaaaaaaaaaaaaaaa/aaaaaaaaaaaaaaaaaaaaaaaaaaaaaa/aaaaaaaaaaaaaaa
aaaaaaaaaaaaaaa/aaaaaaaaaaaaaaaaaaaaaaaaaaaaaa/aaaaaaaaaaaaaaaaaaaaaaaaaaaaaa/aaaaaa
aaaaaaaaaaaaaaaaaaaaaaaaa/aaaaaaaaaaaaaaaaaaaaaaaaaaaaaa/aaaaaaaaaaaaaaaaaaaaaaaaaa
aaa/w * aaa_k8

ERROR : Instance with reserve names.
   No.    Instance Name              Block Name
  ------------------------------------------------------
    1    k1_block_1/vcc             k1_block1
```

The name rule defined is shown in the brackets.

When the max number of name rule errors are output, a message indicating this fact is output and ends the check. The number in the brackets is the max value defined. The checks are ended for each rule.

```
ERROR : Leaf_instance with long names.(MAX_LEAF_INSTANCE_NAME_LENGTH=32)
   No.    Instance Name * Block Name
  ------------------------------------------------------------
    1   i23456789012345678901234567890123 * counter
    2   blk_name_length_over_33abcdefghijk * counter

ERROR : Ports with illegal names.(PORT_NR=[a-zA-Z][a-zA-Z0-9_]*)
   No. Ports Name            Block Name
  ------------------------------------------------------------
    1   \k2_5!                 counter

ERROR: Ports with long names.(MAX_HIER_NAME_LENGTH=255)
   No. Ports Name            Block Name
  ------------------------------------------------------------
    1
k1_block_1/aaaaaaaaaaaaaaaaaaaaaaaaaaa/aaaaaaaaaaaaaaaaaaaaaaaaaaaaaaa/aaaaaaaaaaaaaaa
aaaaaaaaaaaaaaaa/aaaaaaaaaaaaaaaaaaaaaaaaaaaaaaaa/aaaaaaaaaaaaaaaaaaaaaaaaaaaaaaa/aaaaaa
aaaaaaaaaaaaaaaaaaaaaaaaa/aaaaaaaaaaaaaaaaaaaaaaaaaaaaaaa/aaaaaaaaaaaaaaaaaaaaaaaaaaa
aaa/in                aaa_k8

ERROR : Ports with reserve names.
   No.    Ports Name          Block Name
  ------------------------------------------------------------
    1   vdd           counter
    2   k1_block_1/aaaaaaaaaaaaaaaaaaaaaaaaaa/in               aaa_k1!

ERROR : Leaf_ports with long names.(MAX_LEAF_PORT_NAME_LENGTH=32)
   No.    Ports Name * Block Name
  ------------------------------------------------------------
    1   blk_name_length_over_33abcdefghijk/bp_345678901234567890123456789012345678 *
blk_name_length_over_33abcdefghijk

ERROR : Block with illegal names.(BLOCK_NR=[a-zA-Z][a-zA-Z0-9_]*)
   No.    Block Name
  ------------------------------------------------------------
    1   aaa_k1!

ERROR : Block with long names.(MAX_BLOCK_NAME_LENGTH=32)
   No.    Block Name
  ------------------------------------------------------------
    1   blk_name_length_over_33abcdefghijk

ERROR : Block with reserve names.
   No.    Block Name
  ------------------------------------------------------------
    1   vcc
```

Gate loop message

```
loop      check start ...(13:24:24)

ERROR : Each of the following groups of cells makes up a loop:
   No.   Instance Name
      net : Loop Instance(Cell) InputTerm -> OutputTerm
  ------------------------------------------------------------
    1 GL1_1
        xx : GL1_1 (an02d1) a1->z
    2 GL2_1
        xx : GL2_2(an02d1) a2->z
        yy :GL2_1(an03d1) a1->z
```

Fanout message

```
fanout   check start ...(13:24:24)

WARNING : Max fanout is not defined in Library

  No. Cell Name               Pin Name
  ------------------------------------------------------------------------

ERROR : Max fanout exceeded(Fanout Restriction)
```

Number of actual fanout
(max = Max value of fanout)

```
  No. Cell Name        Pin Name      Fanout(MaxFanout)     Instance Name
  ------------------------------------------------------------------------
    1 an02d1      z          76.676(    12.062)      GateLatch2
    2 in01d0      zn         64.507(    12.062)      E135_25
    3 in01d0      zn         33.420(    31.179)      U135
    4 in01d0      zn         12.818(    12.062)      U133
```

The max fanout value references the valid max_fanout in the Synopsys library and compares the total value of fanout_load of the input pins connected to this net. “FOCHECK NUMB” should be input in the input parameter when comparing max_fanout and the number of input pins connected to this net.

Parallel drive message

```
ERROR : Parallel drive

   No. Cell Name   Pin Name   Instance Name (Cell Name)
  ------------------------------------------------------------------------
    1 ER24net is driven by:
                    ER24_1/co (ad01d0)
                    ER24_1/s (ad01d0)
    2 wired is driven by:
```

The number of parallel drive is output.

Three state / bus repeater message

```
three_state/repeater check start ...(13:24:25)

ERROR : Out/inout signal should not be connected to a bus repeater cell.

   No. Net Name
          Instance Name (Cell Name) Pin Name
  ------------------------------------------------------------------------
    1 tri2state is connected by
        Repeat2state (rp01d1) z
        OneTriG (in01d1) zn

WARNING : Three-state should only be connected to one bus repeater cell.

   No. Net Name
  ------------------------------------------------------------------------
    1 gl9_3 (No Pereater)
    2 Two3stM is connected by:
       Two3stMr3 (rp01d1)
       Two3stMr4 (rp01d1)
       Two3stMr5 (rp01d1)
```

Clock line check message

```
Clock Line check start ...(13:24:25)

ERROR : Clock Line Check (Unused Cell)

   No.     Cell Name  InPin->OPin Instance Name
  ------------------------------------------------------------------------
    1        nd02d0    a1->zn        k1_cell_2
    2        mx21d0    i0->z         k1_cell_4
    3        mx21d0    i1->z         k1_cell_6
    4        mi21d0    i1->zn        k1_cell_8

WARNING : Clock Line Check (Unused Cell)

   No.     Cell Name  InPin->OPin Instance Name
  ------------------------------------------------------------------------
    1        in01d0    i1->zn        k1_cell_s

ERROR : Clock Line Check (state dependence delay Cell check)

   No.    Cell Name  InPin->OPin  Instance Name
  ------------------------------------------------------------------------
    1        mx21d0    i0->z         k1_cell_4
    2        mx21d0    i1->z         k1_cell_6
```

Assign check message

```
Assign check start ...(13:24:25)

ERROR : assign Check (tied high/low) { example assign=1'b0 }

   No. Assign Exist Block_Name
  ------------------------------------------------------------------------
    1 aaa_k1!
```

Module Ports check message

```
Module port         check start ...(17:48:27)

ERROR : Output module ports connected to inner cells

  No. Module Name     Port Name
                            No.  inner connect instance pin name
  ------------------------------------------------------------------------
    1 aaa             X11.b
                            1 X11.X22.X33.i
    2 bbb             X11.X22.b
                            1 X11.X22.X33.i

WARNING : Mixing input and output port declaration

  No. Module Name     Port Name
  ------------------------------------------------------------------------
    1 aaa             X11.c
    2 bbb             X11.X22.c
```

Level shift check message

```
ERROR : Voltage do not agree between Cells

  No. From Instance & Pin Name (Cell Name) To Instance & Pin name (Cell Name)
  ------------------------------------------------------------------------------
    1 a2 z 3.3 (zw3ls15t3an2d2) -> e1 i 1.5 (ni01d1)

ERROR : Connection of Level shift cells is mistaking

  No. From Instance & Pin Name (Cell Name) To Instance & Pin name (Cell Name)
  ------------------------------------------------------------------------------
    1 e7 z (zw3ni01bd1) dangling
    2 e6 z (ni01bd1) dangling
    3 e6 zn (ni01bd1) dangling
    4 e2 z (ni01bd1)    -> e3 a2 (zw3ls15t3an2d2)
    5 e2 zn (ni01bd1)   -> e3 a1 (zw3ls15t3an2d2)
    6 Low       -> e5 a1 (zw3ls15t3an2d2)
    7 e4 z (ni01d1)     -> e5 a2 (zw3ls15t3an2d2)

ERROR :  Enable terminal of level down circuit cells is not tied high by invert cell
  No. Instance & Pin Name (Cell Name)
  ------------------------------------------------------------------------------
    1 e8 a3 (zw3ls15t3an2d2) <- e9 (zw3an02d1) (Not connect invert cell)

ERROR :  Power switch sensor cell is not tied high by invert cell
  No. Instance & Pin Name (Cell Name)
  ------------------------------------------------------------------------------
    1 e12 i (zw3ls15t3an2d2)  (Not high)
    2 e10 i (zw3ls15t3an2d2) <- e11 (ni01d1) (Not connect invert cell)
```

Error/Warning count output

```
********** SUMMARY OF DESIGN ERRORS AND WARNINGS *********
```

The number of errors/warnings for each check are displayed.

```
MESSAGE_LEVEL MESSAGE_TYPE              # ERRORS   # WARNINGS
-------------------------------------------------------------------
   1          Shorts                         16         18
   2          Dangling                       80        322
   3          Primary Signals               289          4
   4          Through Net                     0         20
   5          Parallel Drive                 29          3
   6          Three-State/Bus Repeater        0          9
   7          Fanout Restriction             18         13
   8          Name Rule                      48          0
                                        exceeded          <----
   9          Gate Loop                       1          0
  10          Fanout Restriction by User      5          0
  11          Level Shift                     0          0
-------------------------------------------------------------------
  TOTALS:                                   486        404
```

This is displayed when the number of errors in each name rule check exceed MX_ERR_OF_NAMERU

7.2 Information report file on cells used (-DFILE)

Information on cells used will be output (specify by option)

```
//------------------------------------------------------------------------------
//High-performance Logic Design Rule Checker -hldrc Version(V2.0)
//Generated at 00-03-25 15:25:36
//------------------------------------------------------------------------------

*******************************
    HLDRC Summary                          The attributes and the number of pad cells used are output.

Number of Input Pads         19
Number of Output Pads        0
Number of Bidirectional Pads  9
Number of Unknown Pads       0

*******************************

I. DESIGN STATISTICS ============          Information regarding nets is output.

 Number of Nets              :  344
 Average Number of Pins per Net :  2.99
 Maximum Number of Pins per Net :   72

II. DESIGN COMPLEXITY SUMMARY ============          Information regarding cells is output.

   Series Name    Cell Name   Number of Cell   Gate/Cell  Total Gate Count   Total  Leak Power
 ------------------------------------------------------------------------------------------------
 hcos1083av       ad01d0             8        5.67          45.34             1.4e-3
 hcos1083av       in01d0           113        1.00         113.00             1.5e-3
 hcos1083av       in01d1            52        1.33          69.32             1.3e-3
 hcos1083av       mi21d0             1        2.33           2.33             1.4e-3
 hcos1083av       mx21d0             2        2.67           5.33             1.4e-3
 hcos1083av       mx21d3             1        3.67           3.67             1.2e-3
 hcos1083av       ni01d1            47        1.33          62.65             1.4e-3
                     .
                     .
 hcos1083av       nd02d0             2        1.00           2.00             1.4e-3
 hcos1083av       nd02d1             2        1.67           3.33             1.2e-3
 hcos1083av       nr02d0             1        1.33           1.33             1.7e-3
 hcos1083av       rp01d1            12        1.67          20.00             1.8e-3
 ------------------------------------------------------------------------------------------------
 Total                             393        1.56         305.99             1.4e-2
```

*1) The number of the conversion gate can adjust by coefficient of GATE_ADJUST.

*2) If information of the module instance is necessary, specify the following in PTSHELL file.

```
set_strings DFILE <module instance name> ;
```

Example) Outputs all the module instance which exists on low rank hierarchy of the TOP.

```
set_strings DFILE {*} ;
        or
foreach i [ get_search block * ] {
   set_strings DFILE $i ;
}
```

7.3 Cell step number report file (-MAX_CLOCKLINE_NUM)

Outputs the cell step number on the clock line. (specify by option) File name is “check_9_4.f”.

```
<<<clk01>>>                          <<<Clock name>>>
   5 inst01.en(lacfnq0)                 cell number  Leaf pin name(Cell name)
   5 inst04.e(zrddf01n1)
   4 inst03.e(zrddf01n1)
   3 inst02.e(zrddf01n1)
```

7.4 Module definition information report file (-BLKDFILE)

Outputs information on the definition of blocks used (specify by option)

```
//-----------------------------------------------------
//High-performance Logic Design Rule Checker -Version V2.0
//Ganerated at 00-03-25 15:25:36
//-------------------------------------------------------------


*************************************************************
 Block definition list  (Product Name:          NoName  ) *
*************************************************************
+----+------------------+---+-----------+---------------+-----------------------------+
|    |  Block Name      |Use| Interface | Before Expand |         Expanded            |
| No.|                  |   |  I,  O,  B| Cell, Blk, Net|    Gate,  Cell,   Net,  Leak|
+====+==================+===+===========+===============+=============================+
|   1|top               |  1|  6,  7,  4|    5,   8,  30|   133.5,    65,   126,   1e-3|
|   2|MODULE_A          |  1|  4,  4,  1|    7,   0,  17|    80.1,     7,    17,   1e-2|
|   3|test_mod          |  2|  2,  2,  2|   14,   0,  13|    14.3,    14,    68,   1e-3|
|   4|test_module1      |  2|  4,  2,  0|    9,   0,  15|     5.7,     9,    15, 1.4e-3|
|   5|MODULE_B          |  2|  4,  3,  0|    3,   0,  10|     5.3,     3,    10,   1e-5|
|   6|test              |  1|  1,  1,  0|   15,   4,   3|    17.0,    15,    68, 1.3e-3|
+----+------------------+---+-----------+---------------+-----------------------------+
```

*1) A conversion gate number can be adjusted by the coefficient specified by -GATE_ADJUST.
*2) In order to confirm whether the NetWalker library used by hldrc lacks the information on Leak, please check the Leak information for every cell in a use cell information report file (-DFILE).

7.5 Module hierarchy information report file (-BLKHFILE)

Outputs information on block hierarchy (specify by option)

Output conditions can be changed by the following options.
- BLKHFILE_HIER_NUM *Number of hierarchical levels*
  :The number of hierarchical levels to be output can be specified.
- BLKHFILE_TOP *Module instance name*: Output start module can be designated.

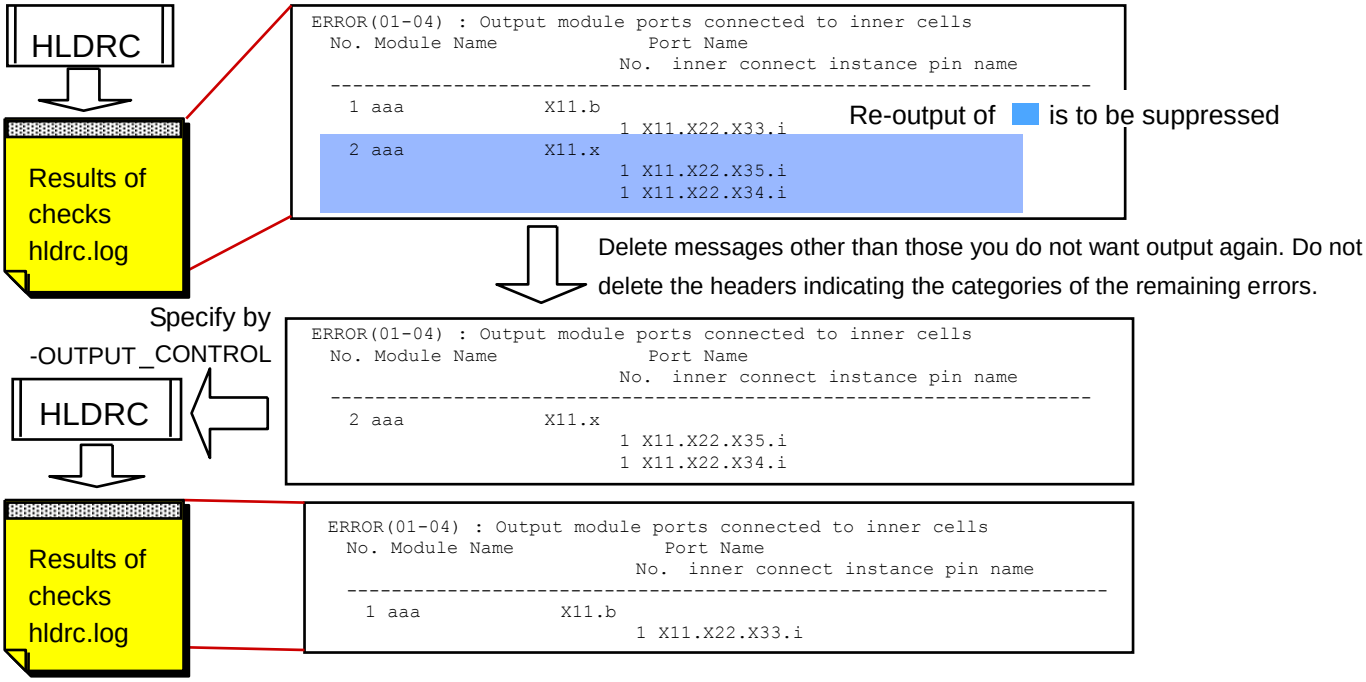
```
//-------------------------------------------------------
//High-performance Logic Design Rule Checker -hldrc Version(V2.0)
//Ganerated at 00-03-25 15:25:36
//-------------------------------------------------------------

************************************************************
 Block Hierarchy list    (Product Name:        NoName  ) *
************************************************************
Hierarcy level --->
0----1----2----3----4----5----6----7-----8-----9
top
   +-test_module1(TM1)
       +-test_mod(T_Mod)
       +-test_mod(test)
   +-test(test_mod)
       +-test_module1(TM2)
   +-MODULE_B(MB1)
   +-MODULE_A(M_A)
   +-MODULE_B(MB2)
```


Integrated when moving down the hierarchy.

8. Suppressing the Output of Messages on Previously Checked Items

When HLDRC is run and examination of the results has shown that some of the warning messages do not represent problems, the output of these messages can be suppressed when HLDRC is run again. However, this does not apply to the gate-loop check.



8.1 Check-result output-control file (-OUTPUT_CONTROL)

When an output-control file has been specified, messages to be output by HLDRC are compared with the content of this file and the output of any matching messages is suppressed. The format of the output control file is the same as that of the hldrc.log file specified by the –HLDRCFILE option. More than one output-control file can be specified.
Example: hldrc_nw -OUTPUT_CONTROL aaa -OUTPUT_CONTROL bbb ……

For convenience, the following functions are supported.

(1) `define function

- Facilitates the replacement of strings. This function may be useful when, for example, changing levels in a block hierarchy.
  Example: `define XXX "aaa.bbb.ccc"
- Use get_instance_name to search for instance names to which a specific defined name (SH2DSP in the example below) is assigned. The instance names that have been hit are replaced with a given string. However, note that this replacement function allows only one definition for a single message.
  Example: `define YYY get_instance_name("SH2DSP")

(2) Partial matching

Parts of messages are compared for matches, that is, comparison is from the heads of messages to the points at which each entry in the output-control file ends.
That is, those parts of a message which are not described in the control file are regarded as matching.
Example: Compare module names and port names and ignore information on internal connections.

```
No. Module Name     Port Name
               No.  inner connect instance pin name
-------------------------------------------------
  2 aaa            X11.x
                        1 X11.X22.X35.i
                        1 X11.X22.X34.i
```

```
No. Module Name     Port Name
               No.  inner connect instance pin name
-------------------------------------------------
  2 aaa            X11.x
```

(3) Multiple specification of a message under the same error category is allowed

Having more than message under the same error category does not cause problems.

Example:

```
ERROR (01-02) : Clock Line Check (Unused Cell)
------------------------------------------------------------
         3        mx21d0 i1->z YYY.a1
ERROR (01-02) : Clock Line Check (Unused Cell)
------------------------------------------------------------
         1         xxxxx
```

(4) When a module name is included in a conditional statement of the form shown below,

`ifdef *Module name* `endif

the message-output control with respect to that module name will not be carried out if the module name is not used.

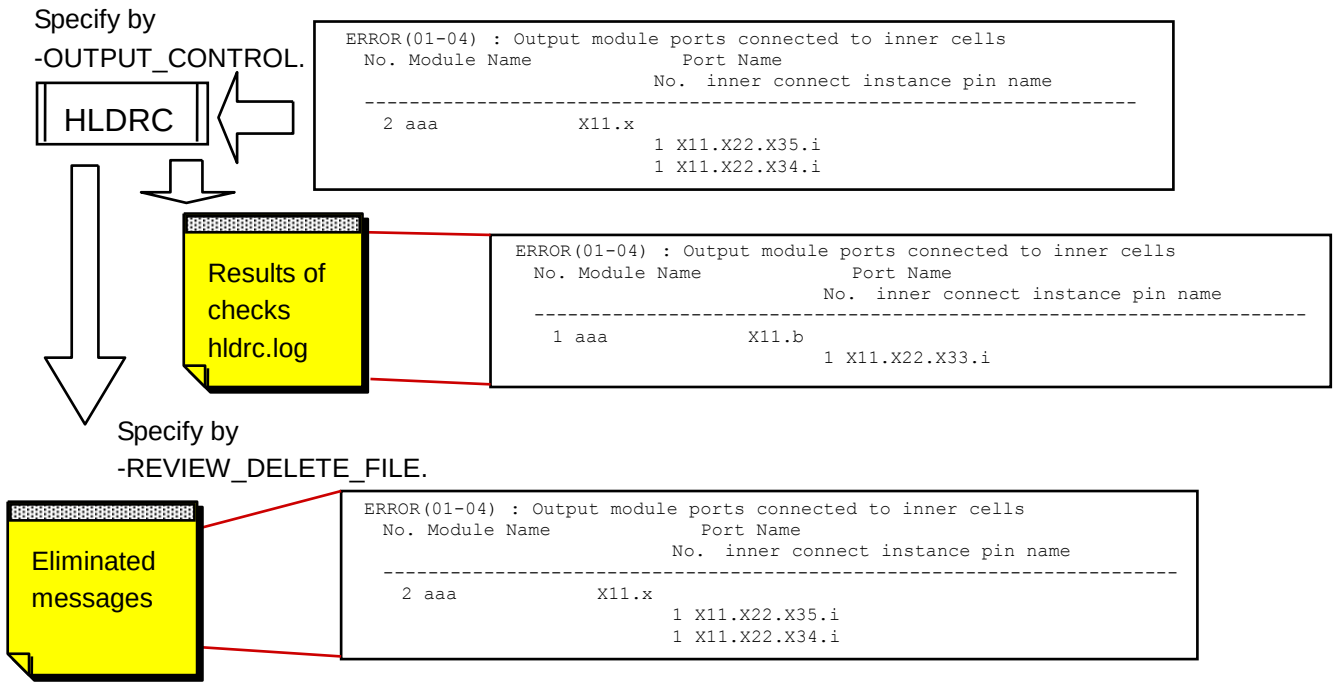
Example: Enable the output control function when the module name SH2DSP has been used.

```
`ifdef  "SH2DSP"
 ERROR (01-02) : Clock Line Check (Unused Cell)
------------------------------------------------------------
     1            xxxxx
`endif
```

(5) Lines staring with # are treated as comments.

8.2 Displaying messages eliminated by the check-result output control file (-REVIEW_DELETE_FILE)

The -REVIEW_DELETE_FILE option may be used to specify a file to receive the messages eliminated by the check-result output-control mechanism.



9. Error method of analysis

9.1 Method of analysis using Verdi GUI

The function to analyze with Verdi GUI of SpringSoft company was added. The error message file (hldrc.log) which HLDRC output is read for analysis.

Please refer to "VerdiIF user guide" for the details.

* After HLDRC was executed, Verdi execution script (run_verdi_nw) is generated automatically in the current directory.
  As for this script, environmental setting is unnecessary.

Appendix: Method to create FORCE_CONNECT/PROHIBIT_CONNECT from shampoo file

Method to create FORCE_CONNECT/PROHIBIT_CONNECT description from shampoo file which exists in the certain directory is as follows. shampoo2hldrc.pt is create.

<< Execution shell >>　　← Execute with the directory that the shampoo file exists.

```
#!/bin/csh -f
echo "" > shampoo2hldrc.pt
foreach name ( * )
   if ( -f $name ) then
      if ( "$name" =~ *.sha ) then
         echo "<< $name    >>"
         awk -f /common/appl/Renesas/REAP/R201X.XX/tools/netwalker/cozy/NetWalker/HLDRC/shampoo2hldrc.awk $name >>shampoo2hldrc.pt
      endif
   endif
end
```

<< Conversion specifications of shampoo2hldrc.awk >>

(1) PROHIBIT_BASE
   The specification of !FUNC sets FUNC for NetWalker type and checks it. (set_cell_type)

(2) FORCE_OBJECT
   FORCE_GROUP ALL adds those because own cell and pin are not described in shampoo.

(3) Regular expression
   The regular expression using in shampoo is different from HLDRC.
   "Q[BIO]*" needs conversion to "-regexp Q[BIO].*".
   When there is "]", "*" is converted to "-regexp .*"
   Because other than this is not supported , please revise the script if necessary.
   In addition, only a cell name supports regular expression. When there is not "[ ]", "*" is recognized as the wild card.

(4) #ALL
   This is replaced with *.

(5) The OPEN error of the output pin outputs the following FORCE_CONNECT.
   The OPEN of the input pin is default check of HLDRC.

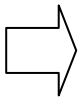
(6) When FORCE_CONNECT description has multiple FORCE_GROUP, error message is output.

(7) Multiline comment can write. (/*…*/)

<< shampoo file>>

```
ELEMENT    TM7INVCLX10 ;
      :
   PIN     YB ;
           PIN_TYPE    OUT ;
           PIN_NICKNAME      YB ;
           PIN_ATTRIBUTE     DATA ;
           CLAMP    FATAL ALL ;
           OPEN       FATAL ;
           EQUAL      OFF ;
           FANOUT     0.639247 ;
```

Conversion



```
set_strings FORCE_CONNECT ¥
    BASE       {TM7INVCLX10} {YB} ¥
    OPEN       INVALID ¥
    MESSAGE "" ;
```