

Arty S7

Xilinx

Digilent Inc.

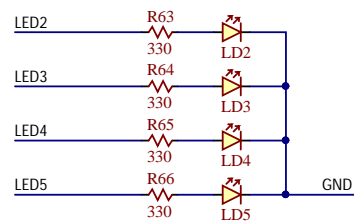
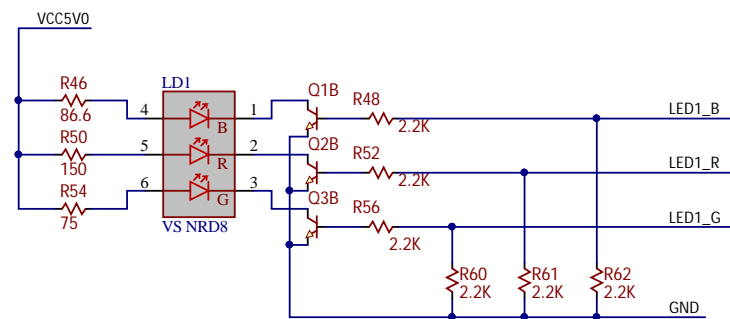
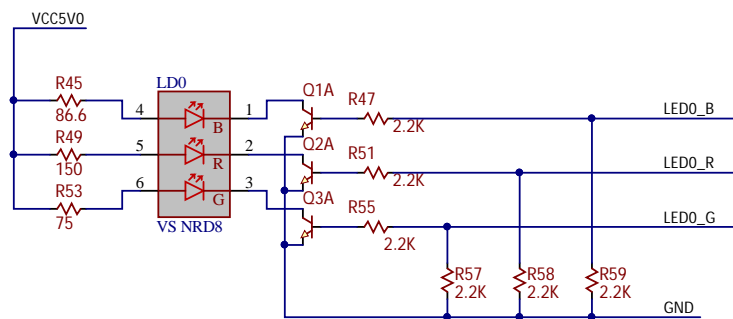
CE

ROHS

Chinese ROHS

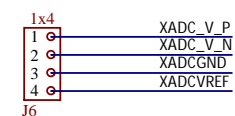
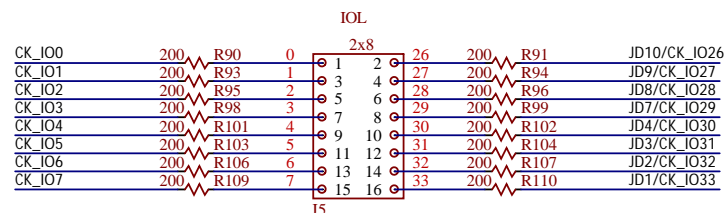
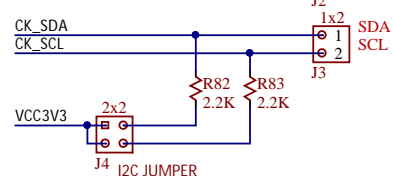
Foot  
F1  
Foot  
F2  
Foot  
F3  
Foot  
F4

|                            |             |   |
|----------------------------|-------------|---|
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| Circuit<br>Pmod, BTN, SWTs |             |  <b>DIGILENT</b> ® |
| Doc#                       | 500-352     |   |
| Engineer                   | MTA         |   |
| Author                     | GMA         |   |
| Date                       | 4/7/2017    |   |
| Sheet#                     | 1 out of 11 |   |

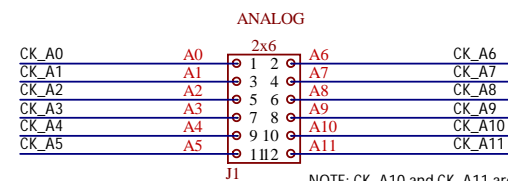
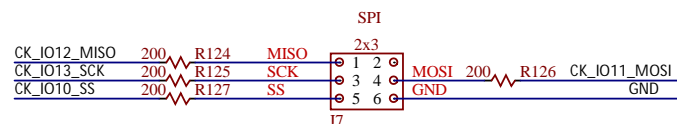
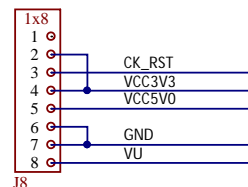


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|--------------|-------------|----------------|
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| Arty S7      |             | B.0            |
| Circuit LEDs |             | Copyright 2017 |
| Doc#         | 500-352     |                |
| Engineer     | MTA         |                |
| Author       | GMA         |                |
| Date         | 4/7/2017    |                |
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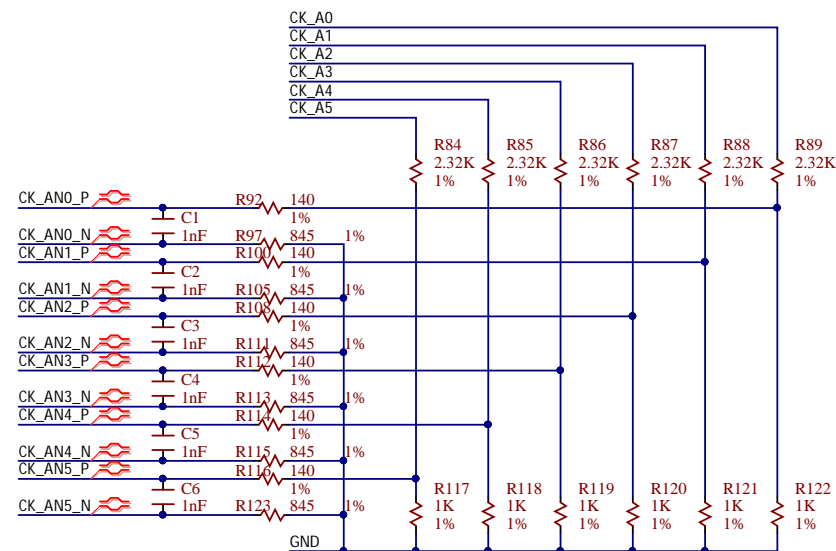




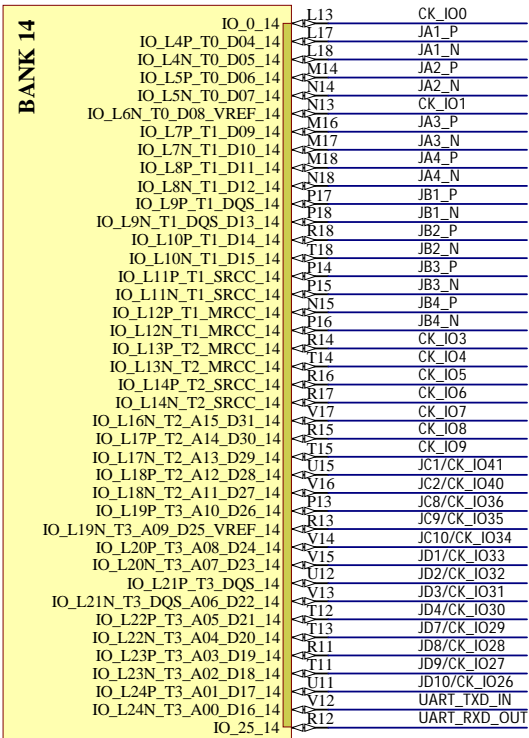
## POWER



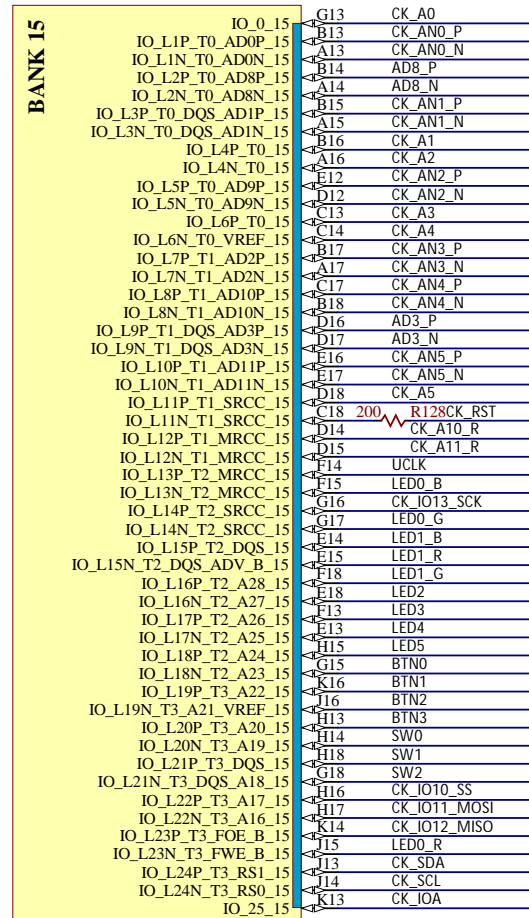
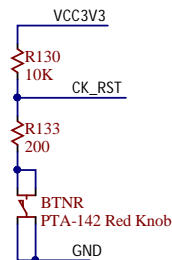
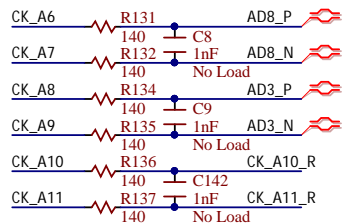
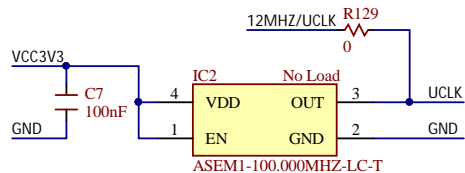
NOTE: CK\_A10 and CK\_A11 are Digital I/O only!



Note: Terminate N signals next to Analog Header



IC1B



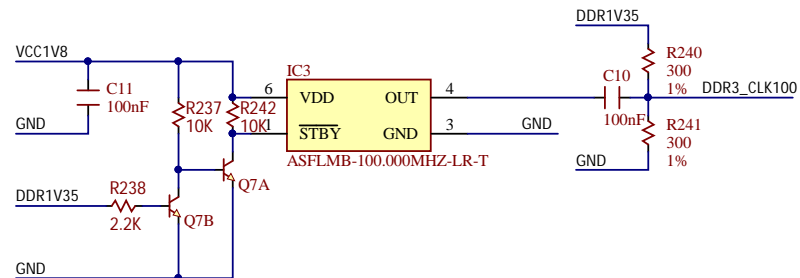
IC1C

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| Circuit  | FPGA Banks  |  |
| Doc#     | 500-352     |   |
| Engineer | MTA         |   |
| Author   | GMA         |   |
| Date     | 4/7/2017    |   |
| Sheet#   | 4 out of 11 |   |

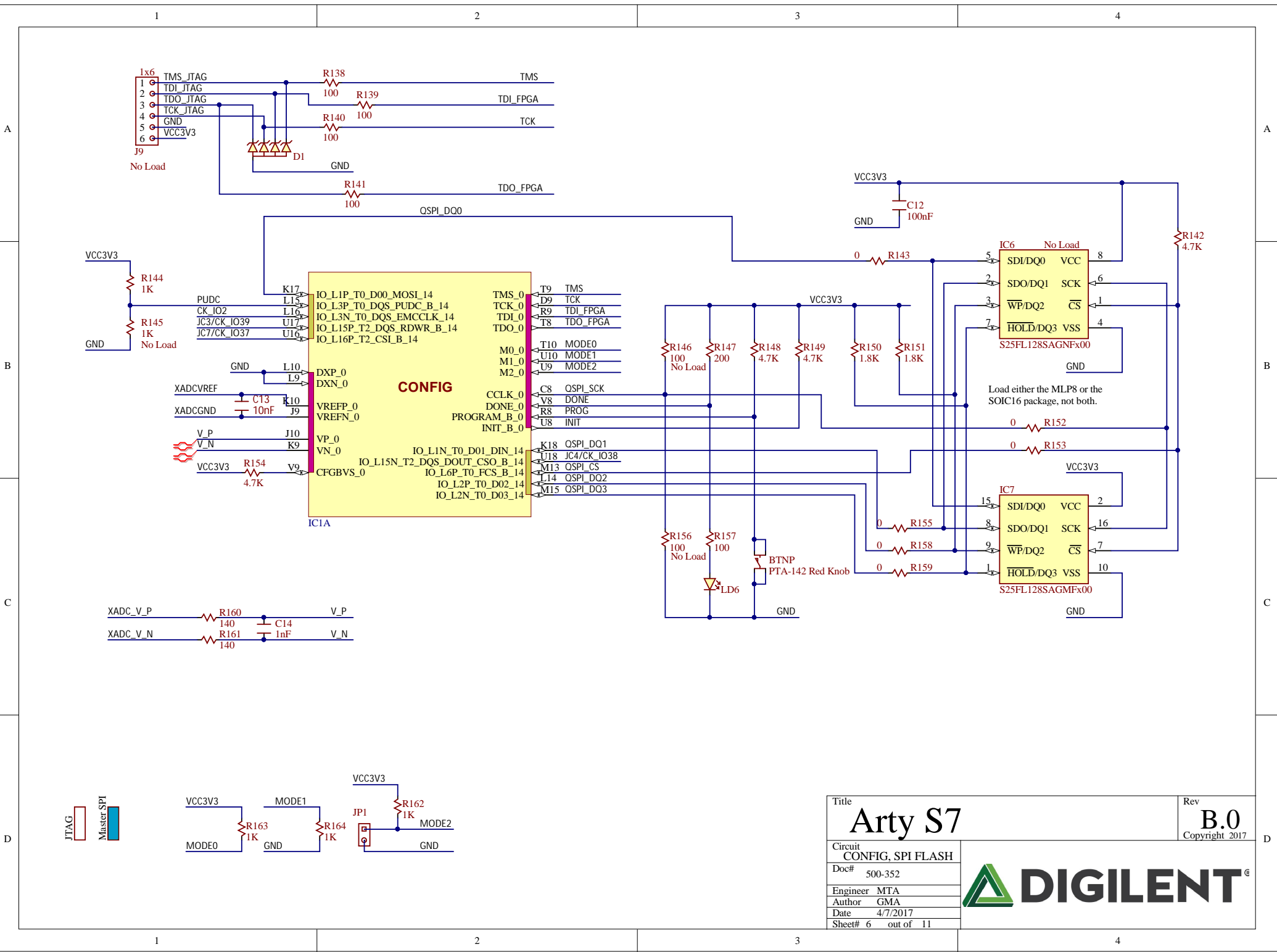
# **BANK 34**

|                    |    |             |
|--------------------|----|-------------|
| IO_0_34            | J6 | DDR3_RESET  |
| IO_L1P_T0_34       | K4 | DDR3_DM0    |
| IO_L1N_T0_34       | L4 | DDR3_DQ2    |
| IO_L2P_T0_34       | K3 | DDR3_DQ1    |
| IO_L2N_T0_34       | K2 | DDR3_DQ0    |
| IO_L3P_T0_DQS_34   | K1 | DDR3_DQS0_P |
| IO_L3N_T0_DQS_34   | L1 | DDR3_DQS0_N |
| IO_L4P_T0_34       | K6 | DDR3_DQ4    |
| IO_L4N_T0_34       | L6 | DDR3_DQ7    |
| IO_L5P_T0_34       | L5 | DDR3_DQ6    |
| IO_L5N_T0_34       | M4 | DDR3_DQ5    |
| IO_L6P_T0_34       | M6 | DDR3_DQ3    |
| IO_L6N_T0_VREF_34  | M5 | SW3         |
| IO_L7P_T1_34       | M3 | DDR3_DM1    |
| IO_L7N_T1_34       | M2 | DDR3_DQ12   |
| IO_L8P_T1_34       | M1 | DDR3_DQ14   |
| IO_L8N_T1_34       | N1 | DDR3_DQ10   |
| IO_L9P_T1_DQS_34   | N3 | DDR3_DQS1_P |
| IO_L9N_T1_DQS_34   | N2 | DDR3_DQS1_N |
| IO_L10P_T1_34      | N5 | DDR3_DQ11   |
| IO_L10N_T1_34      | N4 | DDR3_DQ8    |
| IO_L11P_T1_SRCC_34 | P2 | DDR3_DQ15   |
| IO_L11N_T1_SRCC_34 | P1 | DDR3_DQ13   |
| IO_L12P_T1_MRCC_34 | R2 | DDR3_CLK100 |
| IO_L12N_T1_MRCC_34 | R1 | DDR3_DQ9    |
| IO_L13P_T2_MRCC_34 | R3 | DDR3_CS     |
| IO_L13N_T2_MRCC_34 | T2 | DDR3_CKE0   |
| IO_L14P_T2_SRCC_34 | T1 | DDR3_BA1    |
| IO_L14N_T2_SRCC_34 | U1 | DDR3_RAS    |
| IO_L15P_T2_DQS_34  | U3 | DDR3_BA2    |
| IO_L15N_T2_DQS_34  | U2 | DDR3_A0     |
| IO_L16P_T2_34      | V3 | DDR3_CAS    |
| IO_L16N_T2_34      | V2 | DDR3_A2     |
| IO_L17P_T2_34      | V5 | DDR3_BA0    |
| IO_L17N_T2_34      | V4 | DDR3_A3     |
| IO_L18P_T2_34      | R4 | DDR3_A1     |
| IO_L18N_T2_34      | T3 | DDR3_A4     |
| IO_L19P_T3_34      | P6 | DDR3_A10    |
| IO_L19N_T3_VREF_34 | P5 | DDR3_ODT    |
| IO_L20P_T3_34      | V7 | DDR3_A9     |
| IO_L20N_T3_34      | V6 | DDR3_A6     |
| IO_L21P_T3_DQS_34  | R5 | DDR3_CLK0_P |
| IO_L21N_T3_DQS_34  | T4 | DDR3_CLK0_N |
| IO_L22P_T3_34      | T6 | DDR3_A7     |
| IO_L22N_T3_34      | T5 | DDR3_A11    |
| IO_L23P_T3_34      | R7 | DDR3_A5     |
| IO_L23N_T3_34      | R6 | DDR3_A12    |
| IO_L24P_T3_34      | U7 | DDR3_A8     |
| IO_L24N_T3_34      | U6 | DDR3_A13    |
| IO_25_34           | P7 | DDR3_WE     |

IC1E



|                         |   |                                     |
|-------------------------|---|-------------------------------------|
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| Circuit<br>FPGA Banks   |  |                                     |
| Doc# 500-352            |   |                                     |
| Engineer MTA            |   |                                     |
| Author GMA              |   |                                     |
| Date 4/7/2017           |   |                                     |
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| Engineer |  | MTA            |
| Author   |  | GMA            |
| Date     |  | 4/7/2017       |
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| Engineer |  | MTA            |
| Author   |  | GMA            |
| Date     |  | 4/7/2017       |
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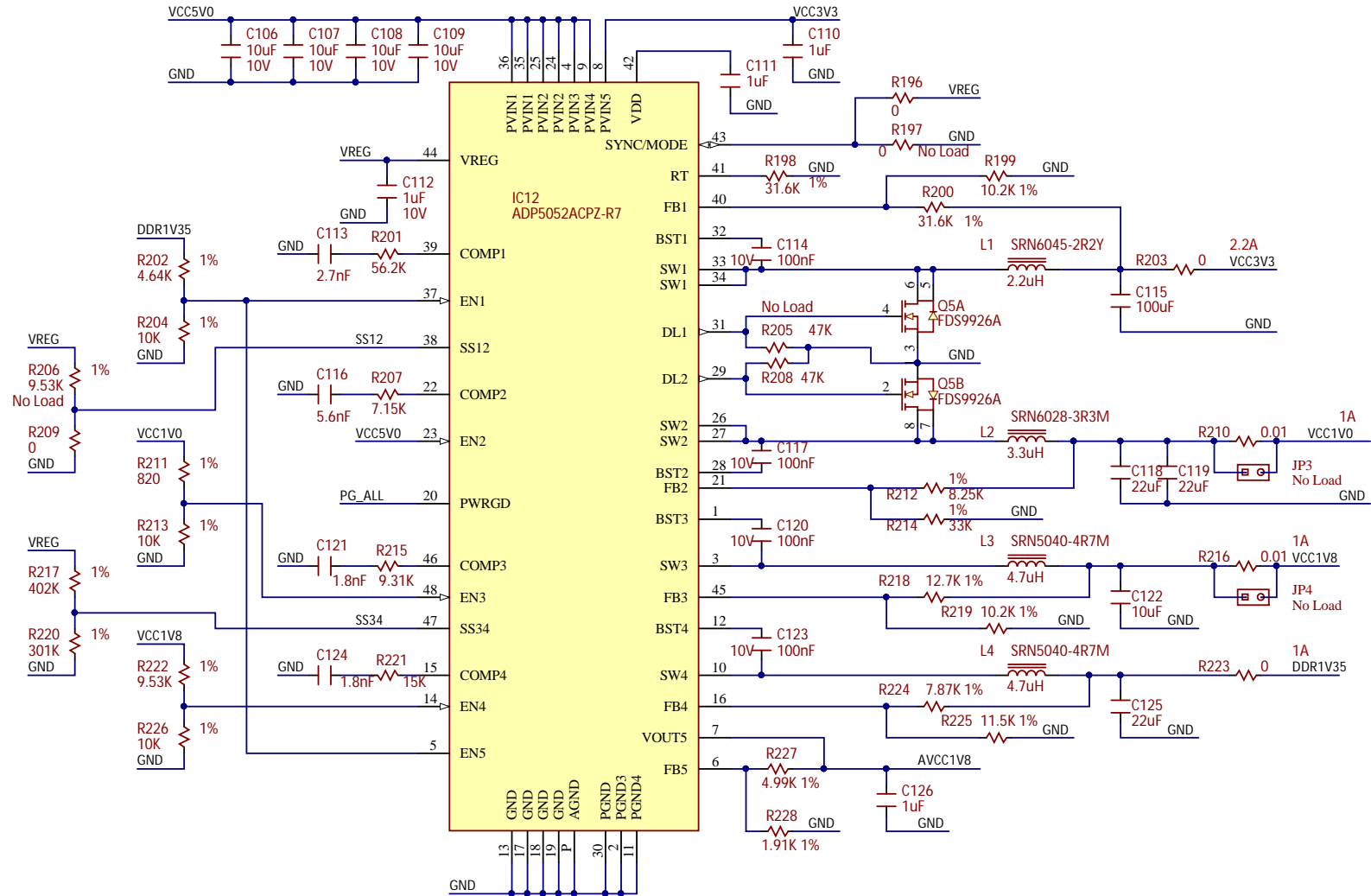
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Author GMA  
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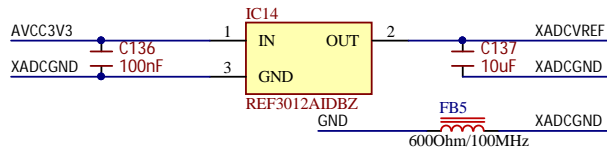
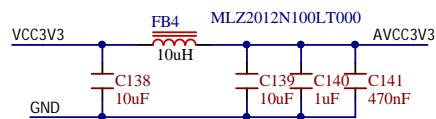
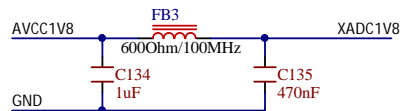
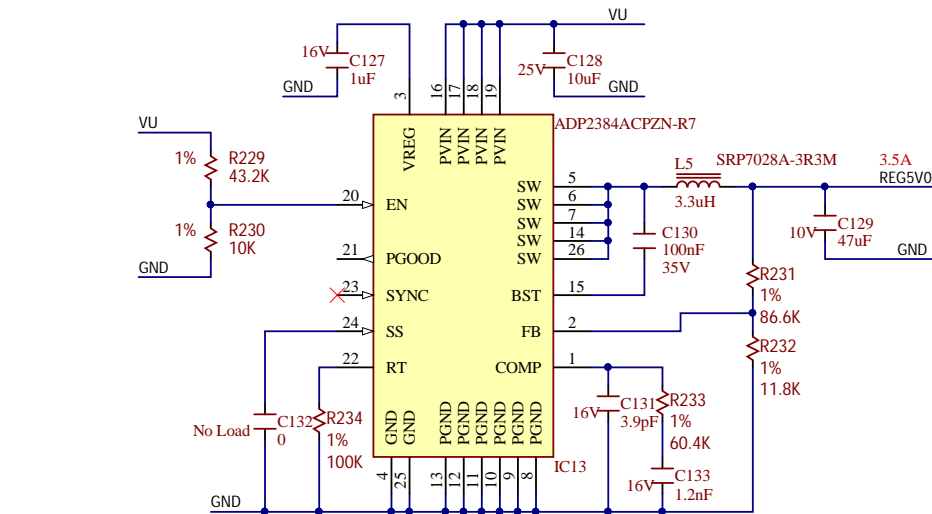


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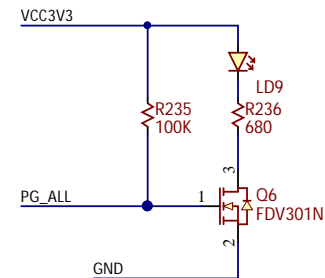
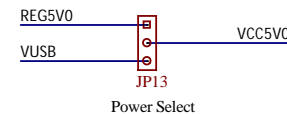
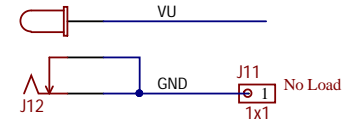
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Note: Input Voltage 7-15V.



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