

DIGITAL SIGNAL PROCESSING IN IF/RF DATA CONVERTERS

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Abstract

To meet the ever increasing data demands of smartphone functionality, the infrastructure architecture of modern digital mobile communication systems must constantly evolve to accommodate wider bandwidths and faster data conversion. Functional processing blocks that are now being utilized in data conversion architectures to achieve faster data rates are digital IF processing, DDC (digital downconverter), and DUC (digital upconverter). These digital functions can be realized in DSPs and FPGAs and some big companies also build their own digital IF processing ASICs. ADI is integrating more and more of these digital IF processing blocks into high speed converter ICs, which significantly relieves design work and provides cost and power savings in the system. This article explores the integrated DDC and DUC channels in ADI's IF and RF converters and explains how they work in real-world applications.

High speed converters are one of the key functions in a modern wireless base station system. More and more such converters are integrated with complex digital signal processing blocks to simplify the FPGA's work in the system design. Digital signal processing blocks in converters provide valuable benefits to system designs, but these benefits are still not widely understood by many engineers. This article will hopefully give a clear view of DDC and DUC functionality in data converters and enable system designers to fully utilize the benefits that ADI converters can provide to the transceiver architecture. Note that this article will focus on digital processing blocks in ADCs and DACs, so the transmitter and receiver blocks are combined in some descriptions. Please omit the signal flow direction if it causes confusion.

In modern digital mobile communication systems, the transmission and receive paths (including observation receive path in the following description) can be divided into three major stages based on the signal's properties: the RF stage, the analog IF stage, and the digital IF stage.

Figure 1 shows the block diagram of typical transmitter and receiver.

The RF stage deals with the RF signal, which generally includes the signal frequency range of 700 MHz to 3.8 GHz in the current LTE standard.

After the mixer, modulator, or demodulator—which are all frequency shifting stages—the RF signal will be shifted to a lower frequency around dc to less than 300 MHz. From the data converter to the mixer, the process module includes converters (ADCs or DACs), analog filters, and IF amplifiers. We call this stage the analog IF stage.

After the converters, in fact, after the quantizer portion of the converters, the signal becomes digital, and together with the subsequent FPGA or ASIC, we called this the digital IF stage. The common term for individual digital signal processing blocks in this stage is the DUC (digital upconverter) for T_x path and the DDC (digital downconverter) for R_x path.

An exception is in a direct RF architecture where data converters sample RF signals directly, so the analog IF stage will be omitted and the signal chain will consist of the RF stage and digital IF stage only.

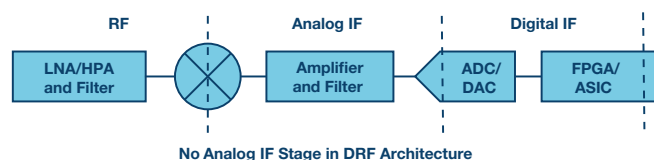


Figure 1. Typical block diagram of transmitter or receiver.

A typical DDC module includes the carrier selection, frequency downconverter, filter, and decimator. These function blocks work in sequence or can be bypassed respectively and finally generate a complex signal at dc or a real signal based on the requirements of the following FPGA or ASIC with lower sampling rates.

A typical DUC module includes interpolation, a filter, a frequency upconverter, and a carrier combiner. A DUC will generate a complex signal at dc, IF-based, or RF directly depending on the system architecture design. The DUC processing is almost converse with that of the DDC.

Multiple stages of DDCs and DUCs are often cascaded respectively for flexibility. Independent DDCs and DUCs requires dealing with multiple carriers in parallel and combining them together before outputting the transmission signal or separating them in the received signal.

DDC

In the R_x chain, higher sampling rates are necessary to avoid signal aliasing, easy analog filter design, and to provide wider signal band. But on the other hand, lower data rates on interface are preferred to save power, cost, and high speed logics in FPGAs/ASICs. The converter's integrated DDC will address the previous requirements.

Figure 2 shows the block diagram of a typical DDC.

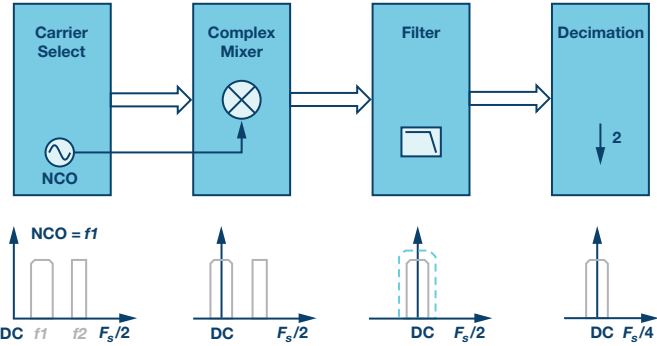


Figure 2. DDC block diagram.

NCO and Mixer

To choose the desired carriers from interferences (blockers and other carriers), the output frequency of an NCO is mixed with input IF signal to shift the desired carriers to dc. This will ease the complexity of the followed filter and decimator stage.

Filter and Decimation

Following the NCO and Mixer stages, a low-pass filter is used to pick up the desired carriers and suppress other unwanted signals. Following the filter, a decimator will reduce the data rate by a factor of two to lower the data rate. To save resources and provide flexibility to the customer, a half-band FIR filter plus decimator by two functions are combined in one block; the block is copied and pasted to cascade three to four levels. System designers can choose to use some or all of them based on the application. Decimation by other numbers more than two are also used for additional flexibility, especially in RF ADCs.

DUC

In the T_x chain, there are the same requirements as in R_x chain: high sampling rates are desired to ease filter design, place the signal on high IF or RF directly, and push the image far away, but lower data rates are preferred for the interface. The converter's integrated DUC will address these requirements.

Figure 3 shows the block diagram of a typical DUC.

Interpolation and Filtering

The simplest digital interpolation algorithm is called zero padding, which means inserting zero into every other sample. The sampling rate is doubled but an image is also generated at $F_s - F_i$ in the resulting spectrum. Therefore, following the interpolator with a filter stage is necessary to remove the image or the original carrier based on the application. If the original carrier is removed, the result is an interpolation and coarse modulation with $F_s/2$.

As in the DDC, the interpolation by two and the filter are combined as a block. This functional block is then copied, pasted, and cascaded three to four levels for flexibility. Other interpolation factors more than two are also used for additional flexibility, especially in RF DACs.

NCO and Mixer

Very similar to this block in the DDC, but converse in function, the following NCO and Mixer stage in the DUC are used to shift the carrier to the desired IF or RF frequency depending on the requirements of the system architecture. In a ZIF architecture, this block can be bypassed to keep the carrier at dc.

Gain, Phase, I/Q Offset, and Inverse Sinc

The gain, phase adjust, I/Q offset, and inverse sinc blocks are accessories in many IF/RF DACs.

Gain and phase adjust, I/Q offset often work together to tune the output signal I/Q channel independently, compensate different kinds of I/Q mismatch (caused by the DAC, analog filter, and modulator), and finally get a perfect complex signal from the analog modulator with low LO leakage and image.

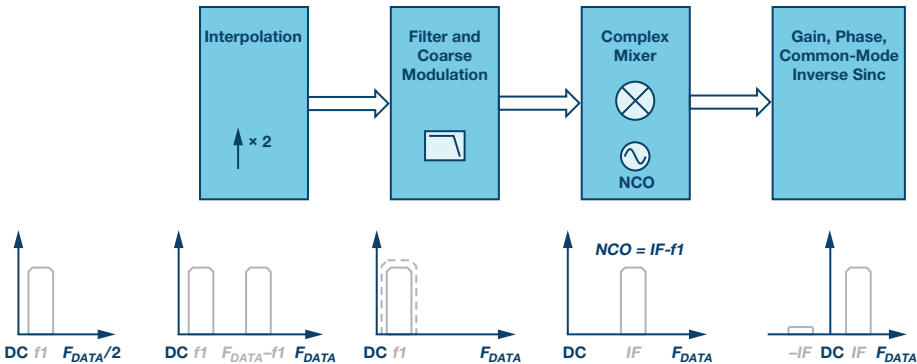


Figure 3. DUC block diagram.

Inverse sinc filter compensates the sinc roll-off caused by the DAC, which affects the flatness and signal's amplitude, especially in wideband applications on high IF or in DRF architecture.

Summary

In this article, we have a brief description of typical DDC and DUC integrated in current IF/RF converters, what they are, why, and how they work in signal chain. Proper understanding of these and correctly making use of them will relieve resources and code works in FPGAs/ASICs, as well as save power and cost in system. Additional details and descriptions can be found in the following references.

References

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About the Author

Alex Zou graduated from the University of Electronic Science and Technology of China in 1999 with a Master of Radio Physics. He previously worked as a hardware design engineer at China Telecom and as an applications engineer at NXP Semiconductors before joining Analog Devices in 2007 as a senior field applications engineer supporting wireless infrastructure applications.

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