Fixed-Latency, Multi-Gigabit Serial Links With Xilinx FPGAs

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***Abstract*—Most of the off-the-shelf high-speed Serializer-Deserializer (SerDes) chips do not keep the same latency through the data-path after a reset, a loss of lock or a power cycle. This implementation choice is often made because fixed-latency operations require dedicated circuitry and they are usually not needed for most telecom and data-com applications. However timing synchronization applications and triggers systems of the high energy physics experiments would benefit from fixed-latency links.**

In this paper, we present a link architecture based on the high-speed SerDeses embedded in Xilinx Virtex 5 and Spartan 6 Field Programmable Gate Arrays (FPGAs). We discuss the latency performance of our architecture and we show how we made it constant and predictable. We also present test results showing the fixed latency of the link and we finally offer some guidelines to exploit our solution with other SerDes devices.

***Index Terms*—Data acquisition, fixed latency, FPGA, serial link.**

I. Introduction

DISTRIBUTED systems for data acquisition and control applications are increasingly being based on networks of multi-Gigabit serial links both on copper and optical fibers. Most of the deployed high-speed Serializers/Deserializer (SerDes) chips do not keep the same latency neither in terms of Unit Intervals (UIs, 1 UI is the duration of a serial symbol) nor in terms of parallel clock cycles after a reset, a loss of lock or a power cycle. For instance, the Texas TLK2711A [1] exhibits latency variations up to 4 UIs on the transmitter data-path and 31 UIs on the receiver side. Also, the National SCAN25100 exhibits latency variations between power-cycles, as specified in [2]. Such an implementation choice is often made because the fixed-latency operation requires dedicated circuitry and it is usually not needed for most telecom and data-com applications. However, timing synchronization and clock distribution applications would benefit from high-speed fixed-latency SerDeses.

The IEEE 1588 [3] standard defines the Precision Time Protocol (PTP), which is designed for the synchronization of the clocks of a distributed system (slave clocks) to a high precision clock (the grandmaster clock). The PTP allows a system to achieve microsecond and sub-microsecond time synchronization between the clocks depending on their intrinsic precision and on the timing performance of the underlying network. A higher precision is achieved with PTP when the latency of the up-link and down-link are constant and equal.

Fixed-latency links also find application in data-acquisition systems for High Energy Physics experiments, specifically in the trigger sub-systems, where it is crucial to preserve the timing information associated with the transferred signals. Trigger sub-systems of experiments at the Large Hadron Collider rely on the Timing Trigger and Control [4] system developed at CERN, which distributes all the signals with predictable latency and phase. The GigaBit Transceiver (GBT) project [5], under development at CERN, is aiming at developing a unique link for data transfer, trigger and clock distribution in future Super LHC experiments. The GBT must feature deterministic latency and phase matched clock recovery.

Fixed-latency serial links would also be needed for the Trigger and Data Acquisition system (TDAQ) of the SuperB [6] experiment where the links used to transport data also carry a global clock and timing information.

In this paper, we present a link architecture based on high-speed transceivers embedded in latest generation Field Programmable Gate Arrays (FPGAs) working with fixed data transfer latency. Some projects about the topic of clock synchronization are described in [7]–[9] and an interesting approach to the problem is proposed by the White Rabbit project [10]. Some fixed latency links with FPGA-embedded transceivers have been implemented [11], [12], but up to now implementations required to fan in the same reference clock both to the transmitter and to the receiver. In the implementation here described this requirement is relaxed, while keeping the latency of the data and phase of the clock recovered by the serial stream constant during the transfer, after a loss of lock or a power cycle.

II. The GTP Transceiver

The architecture we present in this paper is based on the GTP transceiver [13] of the Xilinx Virtex 5 FPGA family. Our concept is also compatible with the GTX transceivers available in the same family and with the GTPs embedded in Spartan-6 devices. Inside the FPGA, GTPs are available as configurable hard-macros (or "tiles"). Each tile includes a pair of transceivers, which share some basic components, like a Phase Locked Loop (PLL) and the reset logic. Fig. 1 shows the architecture of the transmitter (Tx) and the receiver (Rx) included in each transceiver.

The device consists of a Physical Medium Attachment (PMA) sublayer, actually serializing and de-serializing the data, and a Physical Coding Sublayer (PCS), processing the data before serialization and after de-serialization. The shared PLL locks to a reference clock (CLKIN) and generates the high-speed serial

Manuscript received September 13, 2010; revised November 10, 2010 and December 02, 2010; accepted December 12, 2010. Date of publication January 28, 2011; date of current version February 09, 2011.

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Digital Object Identifier 10.1109/TNS.2010.2101083

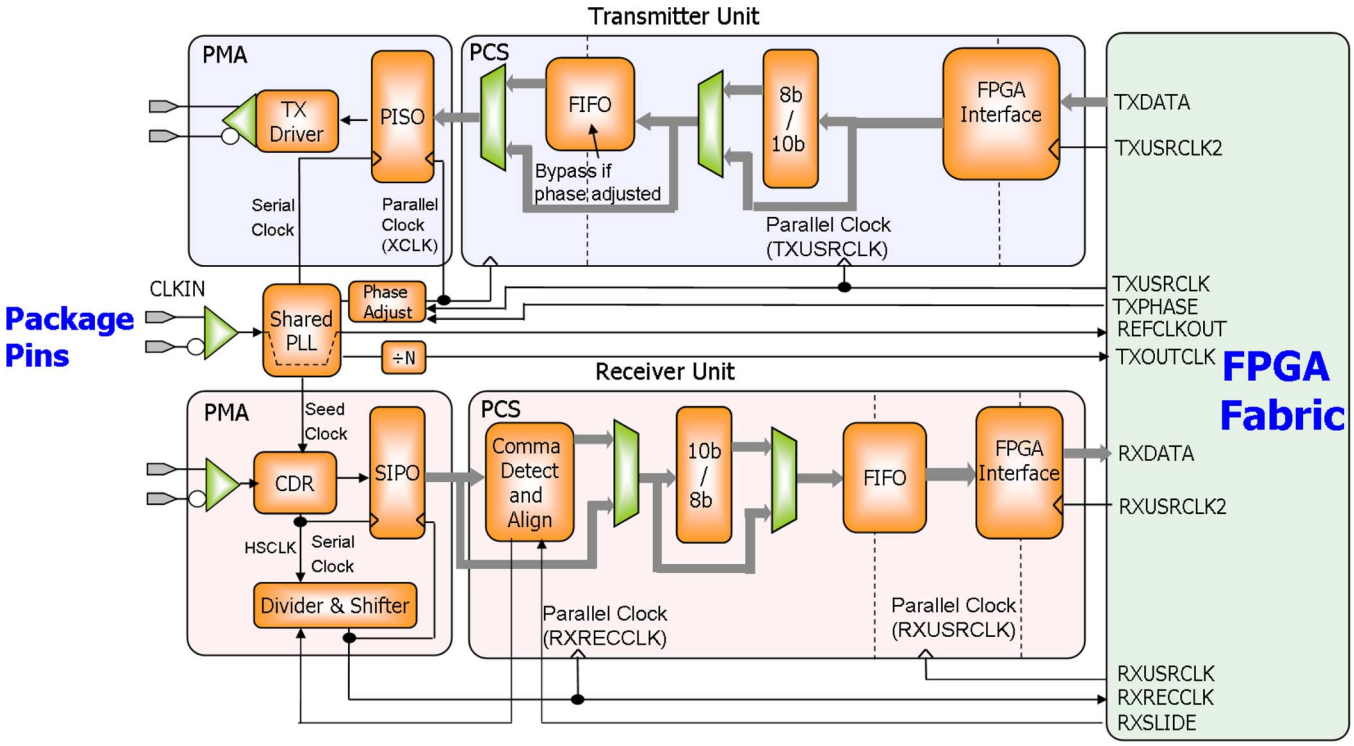

Fig. 1. Simplified block diagram of the GTP transceiver. Half a tile is shown.

clock for the transmitter, a seed clock for the Clock and Data Recovery (CDR) circuit and the parallel clock XCLK for the Parallel Input to Serial Output (PISO).

The transmitter requires two input clocks TXUSRCLK and TXUSRCLK2, which, as far as it concerns the architecture we propose in this paper, are always driven with the same signal.

Data is 8b to 10b encoded, if needed, and it is transferred to a First In First Out (FIFO) buffer (also called elastic buffer), which allows safe data transfers between the TXUSRCLK domain and the XCLK domain. In some configurations XCLK and TXUSRCLK have the same frequency and a constant phase offset. The FIFO can be bypassed if the offset is sufficiently small and in fact the device offers a phase alignment circuit in order to minimize it. In the PMA, data in the XCLK domain is serialized by the PISO block, whose output is synchronous with the high-speed serial clock from the internal PLL. In addition to the already listed signals, the PLL also provides a parallel clock output (TXOUTCLK), which can be used to drive TXUSRCLK. It is worth mentioning that, due to limitations of the GTP, TXOUTCLK cannot be used for this purpose when by-passing the FIFO buffer on the transmitter. In our implementation we drive the TXUSRCLK input with a clock synthesized in the fabric from the external reference clock.

Analogously to the transmitter, the receiver requires two input clocks RXUSRCLK and RXUSRCLK2, which in this work are always driven with the same signal. On the GTP receiver unit, the serial stream from dedicated FPGA pins is received by the CDR, which extracts a clock (HSCLK) and uses it to sample the data. The extracted clock is divided to generate a parallel recovered clock (RXRECCLK) for the Serial In to Parallel Output (SIPO) and for the PCS. The recovered clock is also routed to the FPGA fabric to be used by the receiving logic. The Comma Detect and Align block following the SIPO can be programmed to search in the serial stream for a specific symbol (e.g., an 8b10b comma) and automatically use it to define a word boundary. Data is then 10b to 8b decoded, if needed, and transferred to a FIFO (also called elastic buffer) in order to enter the RXUSRCLK domain.

The GTP does not work with fixed latency in configurations based on its internal resources. We show that implementing in the FPGA the adequate logic and suitably configuring the GTP permits to achieve fixed latency.

III. Latency Variations in Serial Links

This paragraph briefly presents sources of latency variations in a general SerDes architecture. It is not specifically related to the GTP, yet it is useful to better understand the discussion coming in the next two sections.

Latency variations may come from both the serial and parallel sections of a SerDes device. We now focus on the serial section. Let us suppose to multiply the frequency of a clock signal c_i by a factor N and let c_N be the resulting signal (Fig. 2). Let us now divide the frequency of c_N back by N, in order to obtain the same frequency of c_i. There are N possible phases for c_d, each associated with an edge of c_N (we are supposing all the clock signals to be edge-aligned). If there is data traveling from the clock domain of c_i to the one of c_d, the phase variation of c_d leads also to a variation in latency of the data. If fixed-latency operation is required, a mechanism is needed to choose always the same phase for the divided signal and therefore also the same latency for the data.

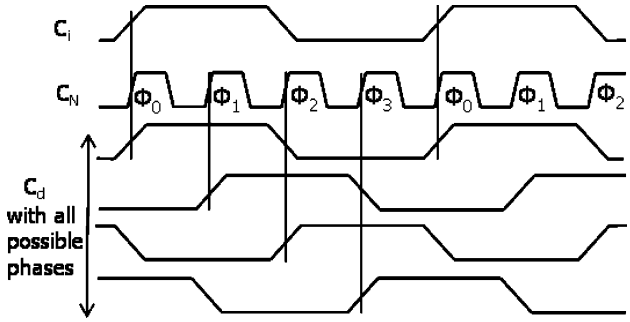

Fig. 2. Clock multiplication and subsequent division (case $N = 4$).

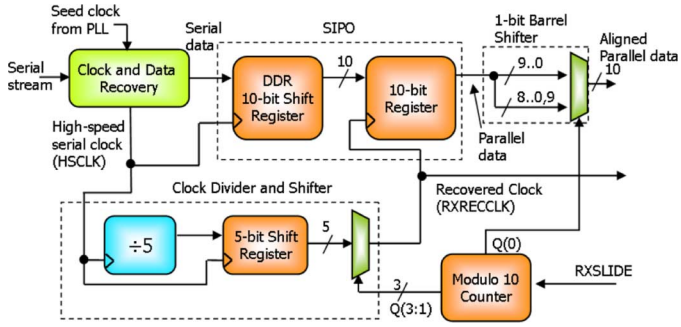

Fig. 3. Conceptual block diagram of the shift architecture used in PMA mode.

In a serial link the frequency multiplication happens in the serializer and the division in the deserializer. In a serializer, the parallel transmit clock (i.e., c_i) is multiplied to provide the high-speed clock to the serial side of the PISO. In the deserializer, the high-speed recovered clock from the CDR is divided to provide the low-speed recovered clock (i.e., c_d) to the parallel side of the SIPO. We thus have a potential phase variation of the parallel recovered clock with respect to the transmit clock in terms of integer numbers of UIs. A phase variation of the recovered clock implies a latency variation of the data transferred on the link. It is important to keep in mind that this effect happens each time the frequency of a clock is multiplied and then divided, not only in SerDeses but also in PLLs, for instance.

As far as it concerns the parallel section, latency variations may be induced by the presence of elastic buffers, which are usually implemented by means of FIFOs. Assuming an equal write and read rate from the buffer, after each reset the latency trough the buffer is determined by the difference of the write and read pointers. This difference may vary depending on the behavior of the logic accessing the buffer and causes variations in terms of integer numbers of periods of the clocks for buffer read/write. So, a dedicated mechanism is needed to ensure that always the same number of words has been written in the buffer before they start being read (the receiver elastic buffer of the GTP implements this feature).

Due to the discussed effects, the total latency ΔL variation between two subsequent resets of a SerDes can then be written:

$$\Delta L = nUI + mT \tag{1}$$

where T is the parallel clock period, UI is the time duration of one serial symbol, n and m are integers and their ranges are dependent on the implementation of the SerDes and how it is operated in the field.

IV. Word Alignment Mechanisms of the GTP Transceiver

In order to support custom alignment algorithms, the GTP also allows the alignment to be driven by the logic in the FPGA fabric. A dedicated signal (RXSLIDE), when asserted, causes the parallel word to be shifted by one more bit. There are two modes for the bit sliding to be achieved: the first one is realized in the PCS by shifting the parallel data (PCS mode) and the second one in the PMA with a shifting of the recovered clock phase combined with the logical shifting of the data (PMA mode).

In PCS mode, the alignment is performed logically, e.g., with a barrel shifter, and there is no way to change the phase of the recovered clock. As we stated in Section III, in order to avoid latency variations, there is the need for a mechanism capable of choosing always the same phase of the recovered clock. It follows that the PMA mode is the best candidate for fixed latency implementations.

Xilinx does not disclose any information about the internal architecture of the PMA, however we propose a model of how the phase shift could be performed (Fig. 3). We experimentally tested that the model correctly predicts the behavior of the device under the operating conditions of interest for this work.

The CDR recovers a high-speed clock (HSCLK) running at half the bit-rate ($T_{\mathrm{HSCLK}} = 2$ UIs) and uses both edges to sample the incoming stream. A Double Data Rate (DDR) shift-register in the SIPO receives the serial data and clock from the CDR and a register re-captures the output from the shift-register on the parallel recovered clock (RXRECCLK) edge. Inside the "Clock Divider and Shifter", HSCLK is divided down by 5 and then fed in a 5-bit shift-register. The outputs of the shift-register are all separated by 1 high-speed clock cycle each (2 UIs). A modulo-10 counter, receives the RXSLIDE signal and selects which output from the shift register to use as a recovered clock. Each time a different phase from the multiplexer is selected, the recovered clock phase offset with respect to HSCLK changes. Inside the SIPO, this phase-offset determines which bit in the shift register is latched into the least significant bit (lsb) of the parallel register. Therefore, by selecting a different input in the multiplexer, the alignment of the parallel data with respect to the serial data is changed.

With this model of the Clock Divider and Shifter, it is possible to shift the recovered clock phase only with steps of 2 UIs with respect to the stream. The transceiver must perform a correct logical shift for any required number of bit slips. For this reason, a 1-bit barrel-shifter receives the parallel data from the SIPO and shifts the data by 1 bit, if needed. The select signal of the multiplexer inside the barrel-shifter is driven by the LSB of the modulo-10 counter (Q(0)). On the odd RXSLIDE assertions Q(0) equals '1' and the barrel-shifter shifts the data, while on the even assertions the barrel shifter is deactivated and the data is shifted only by the shift of the recovered clock phase (Fig. 4). This way the data is always correctly shifted but for each possible recovered clock phase there are two different alignments

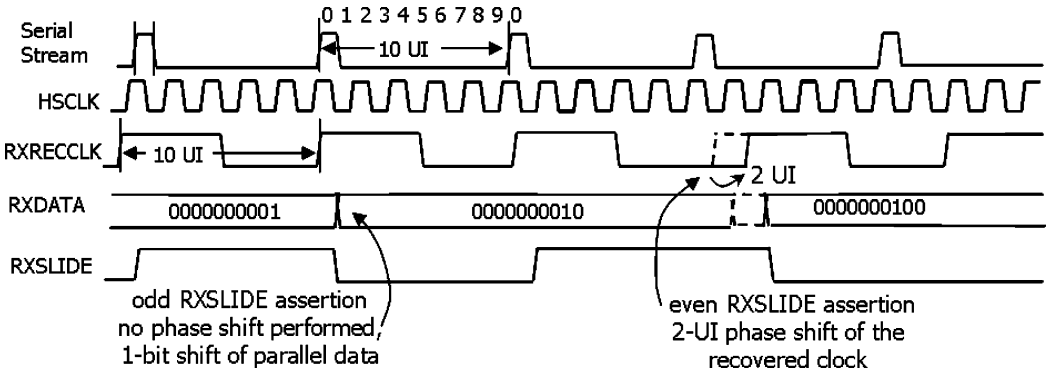

Fig. 4. Recovered clock phase adjustment by means of bit slips.

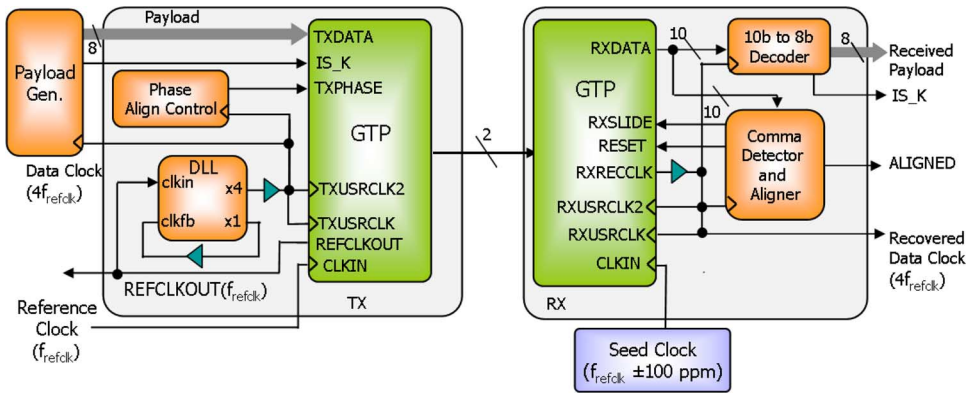

Fig. 5. Implementation of a serial link with fixed latency and fixed clock phase, based on a GTP transceiver.

of the parallel data, corresponding respectively to an odd and an even number of bit shifts. There is 1 UI of latency difference between the two alignments.

The alignment performed by shifting the recovered clock (PMA mode) can be driven only by logic external to the GTP, by means of the RXSLIDE signal. On the contrary, when using the internal comma aligner and detector the alignment is achieved only by shifting the data (PCS mode). This is due to limitations of the device. By itself, no one of the supported alignment modes (PCS or PMA) guarantees the fixed latency operation of the SerDes.

V. Fixed-Latency Data Transfers With the GTP

We will now present an implementation of a fixed-latency 8b10b-encoded serial link, running at 2.5 Gbps, based on the GTP SerDes (Fig. 5).

We have chosen a 8b10b coding because it is the most widespread coding for serial data (e.g., Gb-Ethernet, FibreChannel). Similarly, we chose the 2.5 Gbps data-rate because it is widely used in standards for optical transmissions (e.g., OC-48/STM-16x/2.5 G SONET).

On the transmitter side, we exploit the internal 8b10b encoder and thus the GTP expects 8-bit input data words. The data generator can be programmed with a custom pattern of data and control symbols. If the IS_K input of the GTP is asserted, the incoming data is considered a control character and encoded accordingly. In this design we periodically send a K28.5 control character on the link for the receiver to find the correct byte-boundary.

The CLKIN input of the PLL of the GTP receives a 62.5-MHz reference clock. In order to provide the transmit clocks, a Delay Locked Loop (DLL) external to the GTP takes the reference clock (REFCLKOUT) from the GTP and multiplies its frequency by 4, thus providing TXUSRCLK. The DLL is there to ensure the same phase offset between TXUSRCLK and REFCLKOUT at each power-up. The reason for using the REFCLKOUT output of the GTP instead of the CLKIN signal directly is that CLKIN is connected to dedicated pins of the SerDes and it is not available to the fabric.

Since the parallel clock for the PISO (XCLK) is generated from the reference clock by multiplication and subsequent division, at each power-up its phase can be different. To work this issue around, we use the phase alignment circuit, which aligns the phase of XCLK to the one of TXUSRCLK. Since TXUSRCLK is generated with a deterministic phase from the reference clock, this leads to have XCLK, TXUSRCLK and the reference clock running with a deterministic fixed phase. In order to achieve this behavior, at each power up or after a loss of lock, a controller in the fabric activates the phase align circuit by means of the TXPHASE signal. The procedure we follow for activating the alignment circuit is the one suggested in the GTP user's guide. Under this operating condition the transmit FIFO is unnecessary and therefore we bypassed it.

On the receiver side, the CLKIN input of the GTP is driven by a clock generator with a frequency offset smaller than 100 ppm with respect to the reference clock of the transmitter. The PLL uses this signal to generate a seed clock for the CDR to lock on the stream and correctly recover the high-speed clock. The recovered clock (RXRECCLK) drives the receive clocks (RXUSRCLK and RXUSRCLK2). Due to the reasons explained in Section III, at each CDR lock-up, the recovered clock edge can be aligned with any bit inside the 10-bit symbol. In order to recover the clock always with the same phase with respect to the transmit clock, we had to deactivate the 8b10b comma detector and aligner internal to the GTP. We designed an external "Comma Detector and Aligner" in the fabric, which controls the bit sliding feature of the GTP in PMA mode. The comma detection in the fabric can be performed on the raw data (still encoded) from the transceiver. It is worth mentioning that the GTP gives access to a signal called RXBYTEISALIGNED which can be used to detect if a comma has been received on the current byte boundary, without accessing the raw data. However, this approach requires to pulse the RXSLIDE signal in a "trial-and-error" fashion until the correct alignment has been achieved. On the contrary, with an external comma detector, we exploit the property of comma symbols in such a way to find the correct alignment at the first received comma character. Also, being the decoder external to the GTP, our approach can be customized to work with any serial encoding. In fact, we have been able to implement fixed-latency transfers between the GTP and some off-the-shelf devices, such as the Agilent G-Link chip-set [14] (supporting the conditional inversion master transition protocol) and the National Semiconductors DS92LV18 chip [15] (supporting a proprietary encoding).

In order to establish a bi-unique relationship between the bit shifts performed and the corresponding recovered clock phase, it is necessary either to reject the CDR-locks leading to odd bit-shifts or to reject those leading to even bit-shifts.

Our comma detector looks for commas (e.g., the one included in the K28.5 symbol) and when it finds one it determines how many bit shifts, let it be n, are required in order to align the parallel data to the correct byte boundary. Once the comma is found, the aligner behaves according to the following algorithm:

1) If n is odd the logic resets the GTP and it waits for the CDR to re-lock.
2) If n is even the logic drives the RXSLIDE signal in such a way to perform an n-UI shift of the clock phase and thus a n-bit logical shift of the data. The logic then asserts the ALIGNED output, flagging the correct alignment of the receiver.

Data from the GTP is decoded by means of a dedicated logic and payload bits are provided as outputs on the FPGA board for test purposes. The 10b to 8b decoder also provides a flag indicating if the received word is a control character (IS_K). Its architecture is similar to the one presented in [16] and in the expired patent [17].

The latencies of the transmitter and the receiver, estimated by means of the user guide, are given in Table I.

The concept proven with our design can be used to achieve fixed latency on duplex-links. In the case of independent forward and return channels, one just simply needs to use two instances of the architecture we proposed. In the case of a synchronous re-transmission on the return channel, some care is needed. The clock recovered by the receiver can not be directly used as a reference clock for the re-transmission. In fact, the internal PLL is shared among the transmitters and receivers in the same tile and at the receiver tile it is already locked to the seed clock. Moreover, the recovered clock might also require to be filtered in order to match the jitter specifications for the GTP reference clock. An example of such a work can be found in [18].

We notice that the value of the latency of our serializer and deserializer architecture is known (it is measured in Section VI) and fixed. In some applications it might be necessary to measure in the field the latency of the link including the cables, this could be performed in a duplex link based on our architecture. Also, the proposed method is in open-loop, i.e., there is no feedback to continuously track for sub-UI latency changes and compensate

TABLE I
LATENCY OF THE INTERNAL BLOCKS OF THE TRANSMITTER AND OF THE RECEIVER

	# of RXUSRCLK cycles	Block latency (ns)
Transmitter		
FPGA Interface	1	4
8b10b Encoder	1	4
FIFO (bypassed)	1	4
Serial Section	2	8
Total Transmitter Latency	5	20
Receiver		
Serial Section	1.5	6
Comma Detector (bypassed)	3	12
FIFO	5	20
FPGA Interface	2	8
10b8b Decoder	1	4
Total Receiver Latency	12.5	50
Total Link Latency	17.5	70

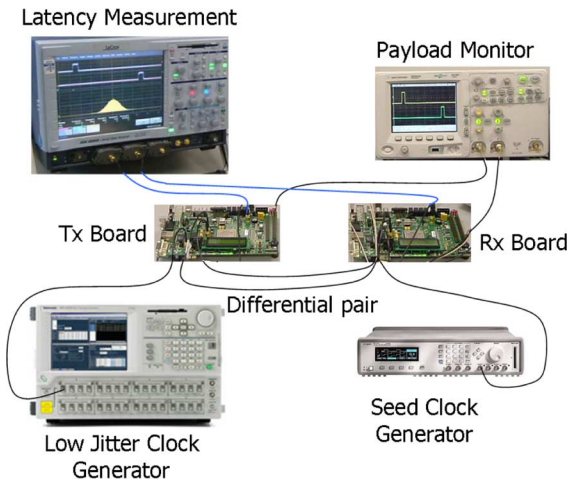

Fig. 6. Experimental setup for latency tests.

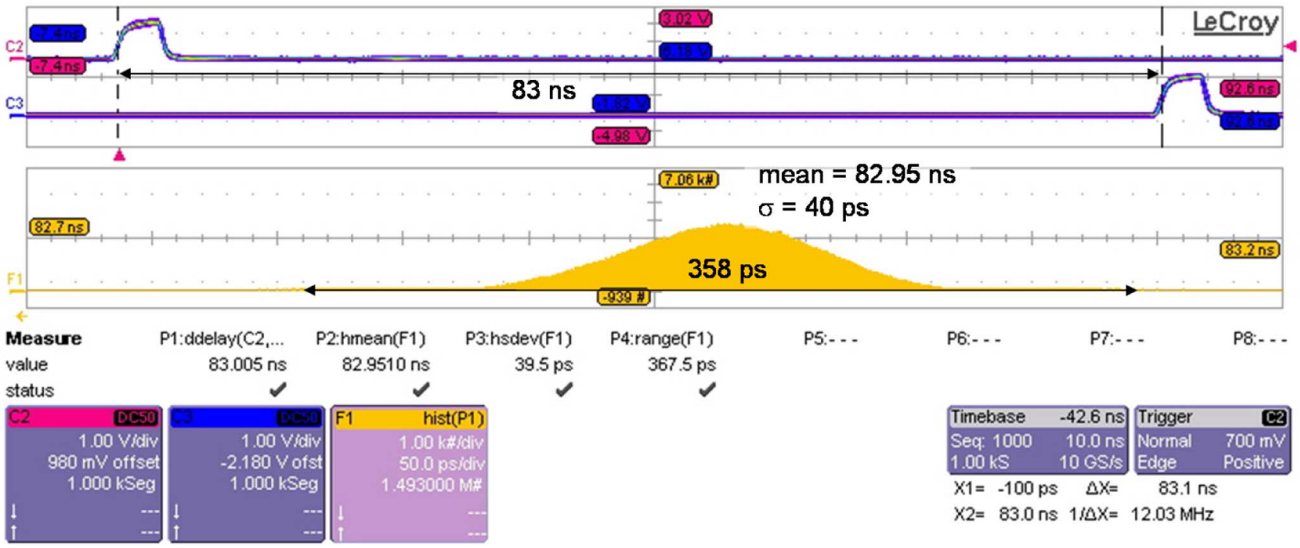

Fig. 7. Histogram of the latency of the link. Topmost trace: transmitted payload bit. Second trace: corresponding received bit. Down: histogram of the latency.

for unavoidable deviations due to temperature, voltage and other parameters variations.

The discussed scheme applies to the GTP transceiver of Xilinx Virtex 5 family of devices, but it has been proven successfully also with the GTX transceiver. The GTP transceivers included in the Xilinx Spartan-6 family are also compatible with this scheme.

VI. Test Results

In order to test our architecture, we deployed two off-the-shelf boards (Xilinx ML-505 [19]). The boards route the serial I/O pins of one of the GTPs on the FPGA to Sub-Miniature version A (SMA) connectors. We connected the Tx and Rx GTPs with a pair of 5 ns, 50 Ω impedance coaxial cables. Transmitted and received payloads were available on SMA test-points and were monitored by means of an oscilloscope (Fig. 6). We checked that the transmission latency and the phase of the recovered clock remained always the same during transfers and between subsequent power-ups of the system. We performed a 24-hour test, resetting the transmitter and the receiver every 3 seconds (i.e., simulating a power-cycle) and holding all the acquired waveforms on the oscilloscope screen, in order to record latency variations. The histogram in Fig. 7 shows the distribution of the link latency during subsequent resets. The standard deviation of the latency is ~ 40 ps and it includes the contributions from all the subsequent power-ups of the system. The precision of the synchronization between the transmitted and recovered clocks is ~ 400 ps (range of the histogram). We note that the latency in terms of integer number of parallel clock cycles and UIs is fixed at each power up. The distribution we observe is only due to the jitter of the received data edge with respect to the transmitted one. In other words, considering (1), we built a system such that m and n are fixed and therefore the latency L is fixed.

We measured the latency of the transmitter and of the receiver (Fig. 8) with respect to the serial stream. In order to easily find the serial bit corresponding to a pulse on the parallel word, we sent a word sequence containing 1023 zero words and one marker word ($(0001)_{16}$), having all bits set to zero but the least significant.

We measured the latency of the transmitter (receiver) by probing the bit #0 of the payload on a test point and the serial output (input) of the transceiver.

In our setup, the transmitter latency was $L_{\mathrm{tx}} = 18$ ns. However, this measurement underestimates the latency by the propagation delay of the FPGA Input/Output Block (IOB) and internal routing. This delay is estimated to be at most 7 ns by the Xilinx timing analysis tool. This explains the difference between the measured and the estimated latency of Table I.

In our setup, the oscilloscope receives the stream at the same time of the GTP receiver but it receives the parallel payload bit with a delay equal to the sum of the propagation through the FPGA IOB (≤ 7 ns) and the connection cable (5 ns). The measured latency after the subtraction of the cable delay is $L_{\mathrm{rx}} = 55$ ns, but it still overestimates the actual latency by a quantity equal to the IOB delay.

The rms jitter on the recovered clock has been measured to be of the order of 20 ps. We measured the jitter with respect to the reference clock at the transmitter, therefore the measured quantity can be taken as an estimate of the precision of the synchronization between the reference and recovered clock. For more information about the jitter performance of our architecture see [20].

VII. Key Features for Fixed Latency

We provide useful hints for the application of our results to other SerDeses.

On the transmitter, the parallel clock driving the PISO must have a predictable phase relationship with respect to the external parallel data clock. In many transmitters this might be supported by using features for serial channel bonding. In fact, channel bonding is used for multi-lane serial buses such as PCI Express, RapidIO and Infiniband, which require the same latency through each bonded data-path.

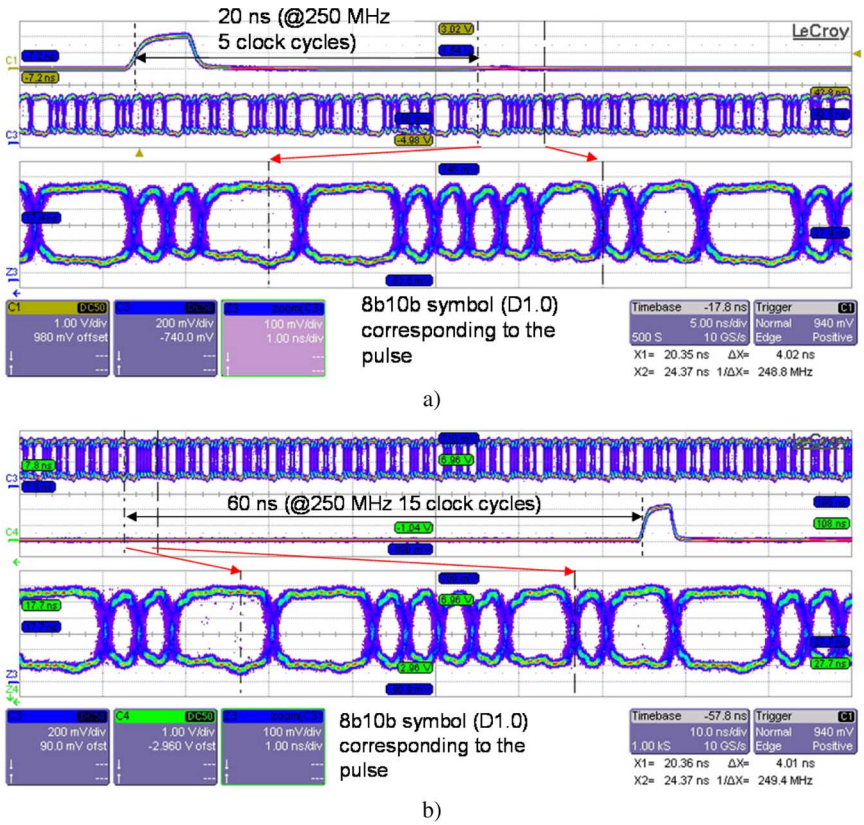

Fig. 8. Oscilloscope screen-shots showing the latencies of the transmitter and of the receiver. (a) Upper trace: transmitted payload bit. Middle trace: 8b10b encoded serial stream. Lower trace: zoom on serial stream (b) Upper trace: 8b10b encoded serial stream. Middle trace: received payload bit. Lower Trace: zoom on serial stream.

On the receiver, the recovered clock must have a predictable phase relationship with respect to the byte boundary in the incoming serial stream. The receiver should offer a direct method to determine this phase offset or some feature to be exploited in order to determine it indirectly. The phase offset determination can be done externally if the device is able to output un-decoded and un-aligned parallel words. Since, at each power-up of the receiver, the phase offset changes, the designer might add an external logic, which only checks the offset (by finding the data alignment) and resets the receiver if it is not the desired one (*roulette* approach). When the desired phase offset occurs, the logic does not reset the device and the lock is achieved with the same latency as all the other successful locks. The *roulette* approach does not strictly require to perform any alignment of the data, since the receiver can simply reject the locks requiring to shift the parallel data and accept only the locks leading to have data already correctly aligned. The receive logic is then simpler, since it does not require a comma detector or a word aligner, but only a decoder to check that the received data is valid. An obvious drawback of such an approach is the increase in the average lock time, which is proportional to the number of bits in the parallel symbol. Therefore, there is here a trade-off between the average lock time and the simplicity of the receive logic.

If the device can not output raw data, but automatically decodes and aligns the data to the byte boundary, it might store the phase-offset between the stream and the recovered clock in a register. This is equivalent to finding the phase-offset externally.

VIII. Conclusion

High-speed SerDes chips are typically designed for variable-latency transfers. In fact, the fixed-latency operation needs special design care and it is often not needed in most of telecom and data-com applications. However, protocols for timing synchronization and clock distribution applications, which sometime are present in HEP experiments, would benefit from fixed-latency serial links. By suitably configuring two GTP transceivers embedded in Xilinx FPGAs and adding to them a control logic in the FPGA fabric, we implemented fixed-latency operation. Our link transfers data with fixed latency and recovers the clock from the serial stream with a predictable phase, even after a reset or a power-cycle of the system. As an example of implementation, we designed a 2.5 Gbps serial link based on 8b10b encoding. Our architecture is independent of the data encoding and can be customized to support any. We highlighted the features of the GTP architecture which are crucial for the fixed latency operation and we provided some guidelines to allow the reader to use our results also with other off-the-shelf high-speed SerDeses.

Acknowledgment

The authors are grateful to G. Guasti and F. Contu from Xilinx Italy for their help in configuring the GTP transceiver. The authors would also like to thank the SuperB-TDR project of the Istituto Nazionale di Fisica Nucleare (INFN, Italy) for

supporting the research, whose results have been presented in this paper.

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