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Latest developments in the Sinara open hardware ecosystem

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***Abstract*—The complexity of quantum experimentation setups generates demand for a hardware platform that ensures means of standardization of the equipment used as well as setup**

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repeatability.

Sinara Hardware is an open-source answer to those challenges. It offers a modular architecture and well over 50 different modules. While originating from ion trapping experiments, it provides an ecosystem that can meet a wide range of quantum experimentation needs. Accompanied by researchers and engineers from different universities and private companies, Sinara Hardware is not only a hardware platform but also a vibrant community.

Sinara Hardware is developed along with an open-source control system - ARTIQ. ARTIQ provides a high-level programming interface along with experiment management tools. It offers nanosecond timing accuracy, sub-microsecond latency and means of timing distribution across several controller modules.

This poster covers the developments from the last 2 years in the Sinara Hardware project. The most interesting novelties are: CERN Distributed IO Tier (DIOT) integration that will introduce backplane for communication and will enable use of DIOT Zynq UltraScale+ based controller; Artix-7 based FMC (FPGA Mezzanine Card) carrier along with two Sinara-dedicated FMCs: Shuttler - 125 MSPS 16 ch. 16-bit DAC (Digital to Analog Converter), with separate analog front end for application versatility and Waver - 1.5 GSPS 4 ch. 16-bit DAC; Unified Arbitrary Waveform Generator Framework as a common firmware platform for Sinara DAC applications as well as Xilinx RFSoC-based high bandwidth signal generator. Additionally, an overview of what is to be expected in future developments is shown.

***Index Terms*—ion trap, FPGA, ARTIQ, Sinara, quantum instrumentation, DAC, FMC, RFSoC**

I. Introduction

Sinara is an open source hardware ecosystem aimed at supplying signals controlling quantum experiments. It features over 50 modules that are in production or in active prototyping stage. All Sinara modules are licensed under CERN Open Hardware License, which allows sharing, modifying and production of provided designs.

Sinara Hardware is designed to work with ARTIQ (Advanced Real-Time Infrastructure for Quantum physics) [1] control system. It provides precise control with 1 ns timing resolution and an extensive set of tools facilitating experiment scheduling and versioning, results storage and hardware management.

II. New modules in production

In the last 2 years many module designs were finalized and entered stable production.

A. Kasli v2.0

Kasli is a controller module with a Field Programmable Gate Array (FPGA) that can run as an ARTIQ core device [2]. Kasli is used to control other modules in the Sinara Hardware family. Kasli v2.0 is an upgrade to the original design with the following main differences:

- 12 EEM (Eurocard Extension Module) connectors (up from 8 on board),
- oscillators for White Rabbit (WR) synchronization scheme,
- 4 SFP connectors (up from 3),
- bug fixes and other improvements.

B. Kasli SoC

Kasli SoC [3] is a Zynq based controller, featuring much faster ARTIQ kernel execution [4] and additional RJ45 port for Ethernet. Otherwise the board is functionally the same as Kasli v2.0

C. Phaser

Phaser is a 2 channel 1 GS/s RF AWG (Arbitrary Waveform Generator) [5]. It can generate complex multitone pulses [6]. It features dual IQ upconverter and a 300 MHz to 4.8 GHz VCO.

D. Mirny and Almazny

Mirny is a 4 channel microwave frequency synthesizer [7]. It can be used for laser spectrum shifting. It can generate frequencies between 50 MHz and 4 GHz.

Almazny is an Analog Front End (AFE) board for Mirny [8]. It extends Mirny's output to 12 GHz bandwidth enabling full use of ADF5356 chip used in Mirny.

E. Fastino

Fastino is a 32 channel 16 bit 3 MS/s DAC (Digital to Analog Converter) module [9]. Its outputs have 500 kHz bandwidth and ±10 V range. It can be used for ion shuttling. The board features a HD68 connector, however BNC/SMA adapters are available.

F. Stabilizer

Stabilizer is a STM32-based PID (Proportional-Integral-Derivative) controller [10]. It has 2 channels of 2 MS/s 16 bit ADC (Analog to Digital Converter) and 2 channels of 3 MS/s 16 bit DAC. It can be used for magnetic field stabilization with mains feed-forward. Stabilizer can be extended with mezzanine boards, one of which can be used for PDH (Pound–Drever–Hall) lock generation.

III. Current development

A. DIOT integration

Distributed IO Tier (DIOT) is an open scientific hardware unification project at CERN [11]. To gain synergy and to enable usage of Sinara modules in different scientific areas it was decided to make it compatible with DIOT. Sinara in DIOT will feature:

- Zynq Ultrascale+ Controller [12],
- a common 3U crate with 8 peripheral slots,
- dedicated backplane with gigabit link, 16x LVDS, I^2C and clock line to every peripheral module,
- Kintex Ultrascale FMC HPC (FPGA Mezzanine Card, High Pin Count) Carrier [13],

Existing Sinara modules will be available to use with a common adapter.

Current and planned development includes:

- porting ARTIQ to Zynq Ultrascale+ controller,
- STM32 based controller for slow-controlled applications [14],
- SILPA – Simple Low Distortion Power Amplifier [15].

B. FMC subsystem

Further expansion of Sinara capabilities will be achieved by using FMC modules.

1) EEM FMC Carrier: EEM FMC Carrier is a FMC HPC carrier module [16]. The board is designed to be compatible with both DIOT and EEM standards, with 2 form factors available. Xilinx Artix-7 100T FPGA is present on the module. EEM FMC Carrier is currently in development with first prototypes in testing.

2) Shuttler: Shuttler is a 16 channel 125 MS/s 14 bit DAC module in FMC form factor [17]. It has ±5 V output with external AFE for application specific adjustments. This project is currently at the prototype testing stage.

3) Waver: Waver is a 4 channel 1.5 GS/s 16 bit AWG [18]. It has ±10 V output with 800 MHz analog bandwidth. This project is at prototype production stage.

C. Fast Servo

Fast Servo is a board designed to offer wider regulation bandwidth than Stabilizer module [19]. It features a Zynq XC7Z015 SoC (System on a Chip) on a module by Trenz. It allows the user to swap the Zynq module for a different one. Fast Servo has 2 channel 125 MHz 16 bit ADC and 2 channel 125 MHz 14 bit DAC. It is compatible with the same mezzanines as Stabilizer. This module is currently in the prototype testing stage. Linien software [20] support is planned.

D. RFSoC AMC

RFSoC AMC is a MicroTCA form factor module featuring a Xilinx XCZU27DR SoC [21]. It is an attempt to open Sinara ecosystem to quantum experiments which require high bandwidth low-latency instrumentation. The module features 8 channels of 12 bit 4 GS/s ADC and 8 channels of 14 bit 6 GS/s DAC. Analog front end is implemented as a separate mezzanine module enabling application-specific adjustments. Platform is equipped with 4 GB DDR4 RAM for the PS (Processing System) and 8 GB DDR4 RAM for the PL (Programmable Logic). To allow system-wide integration with ARTIQ an additional timing FPGA was used. It is also capable of providing White-Rabbit time synchronization.

E. Universal Arbitrary Waveform Generator

For the purpose of Shuttler and Waver a Universal AWG Framework is under active development. It focuses on providing a platform for AWG firmware implementation abstracting out memory access and various triggering schemas.

F. Cryogenic DAC ASIC

Scaling an ion based quantum systems to a large number of qubits requires a massive DAC channel count [22]. To address thermal challenges of such systems, a dedicated DAC ASIC (Application-Specific Integrated Circuit) featuring a large number of channels and dedicated control logic is being developed. This ASIC will be designed to minimize the number of connections to 4 K trap zone. Currently, tests of 130 nm process are being conducted in cryogenic chambers.

IV. Conclusion

In the last 2 years many new and updated hardware designs were developed in the Sinara hardware family. Presented modules enable ARTIQ and Sinara users to extend capabilities of their experimental setup and to integrate more functionalities into a single control system. Ongoing efforts aim to provide an even more unified and robust hardware platform as well as address upcoming challenges of quantum computing.

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