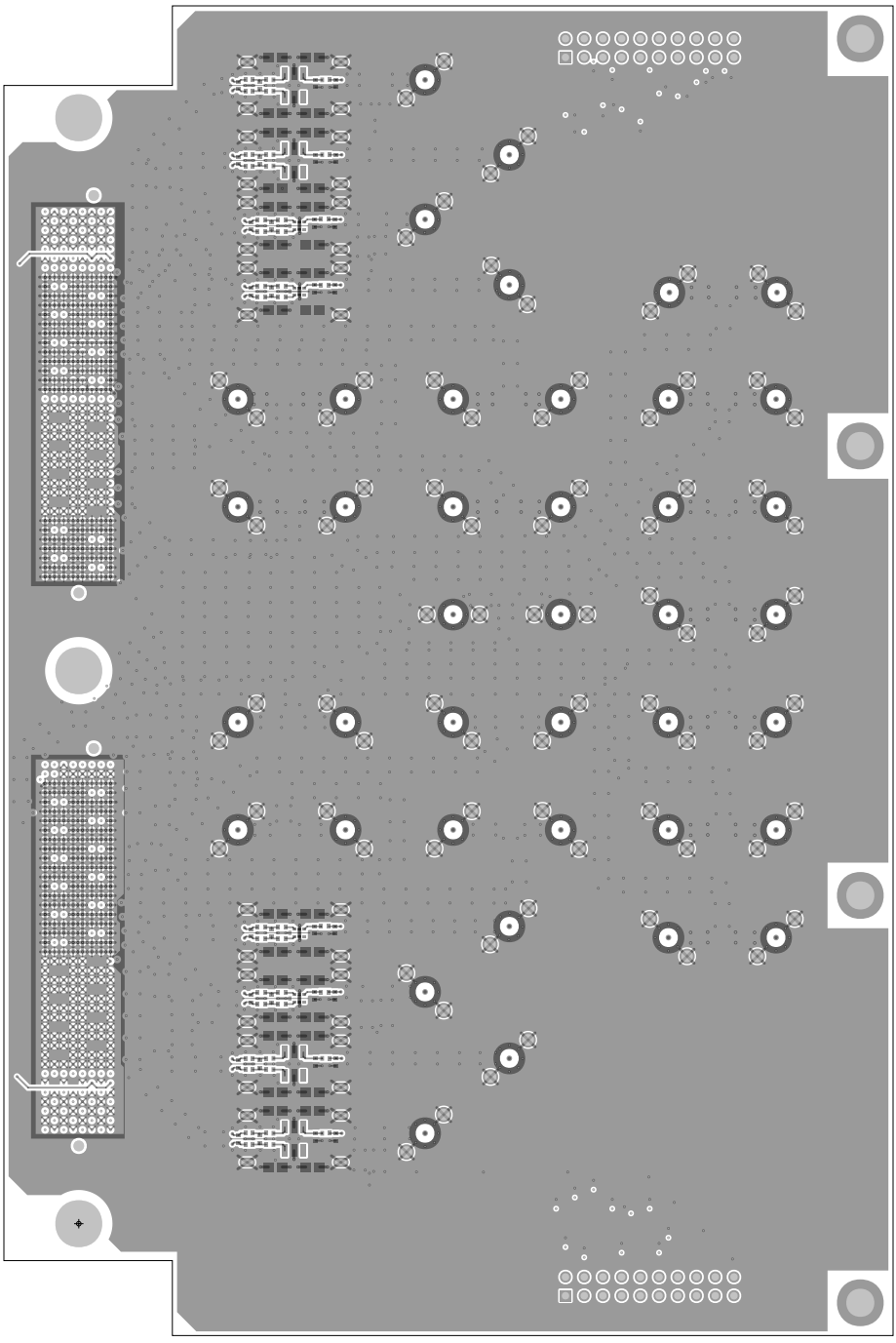
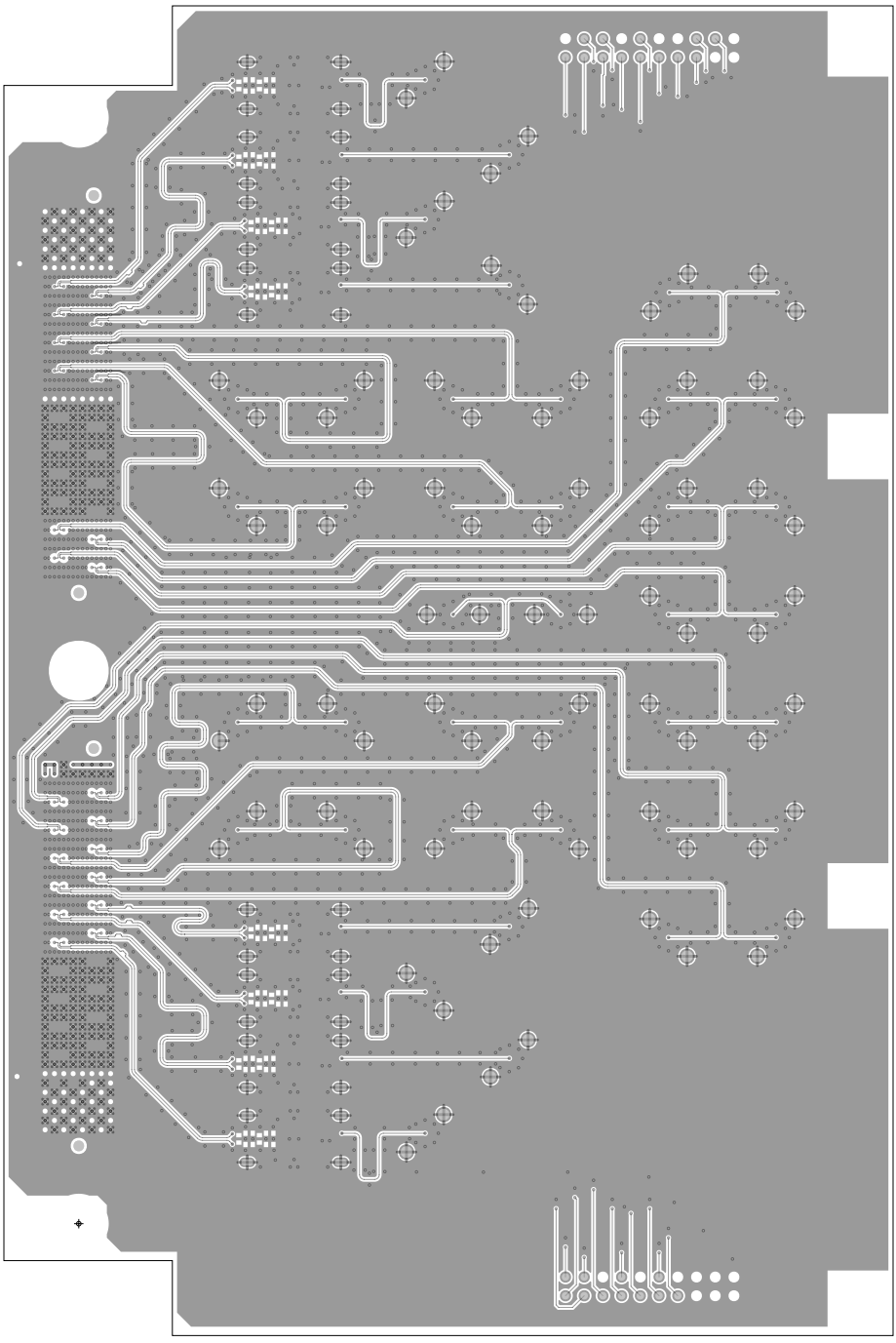
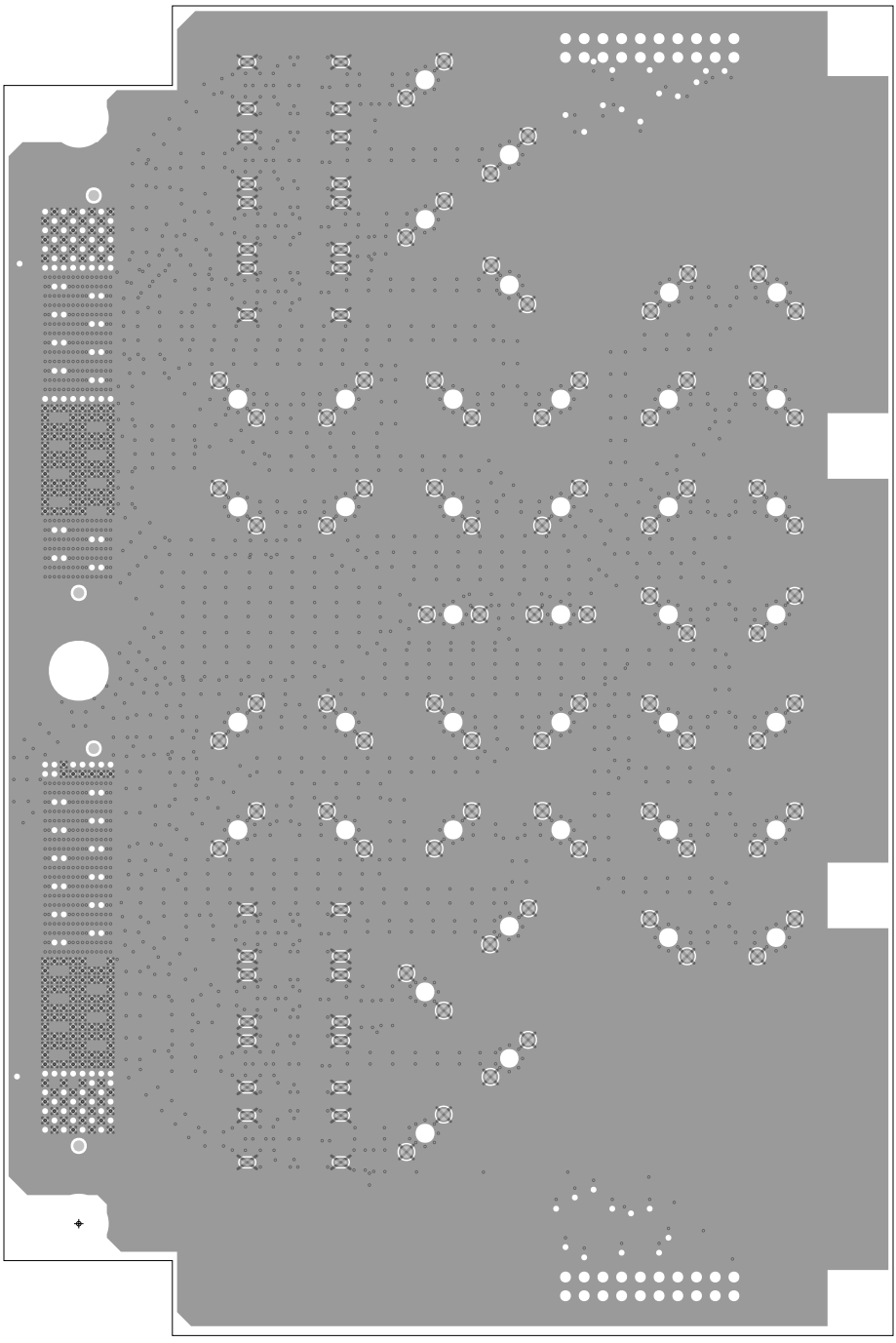


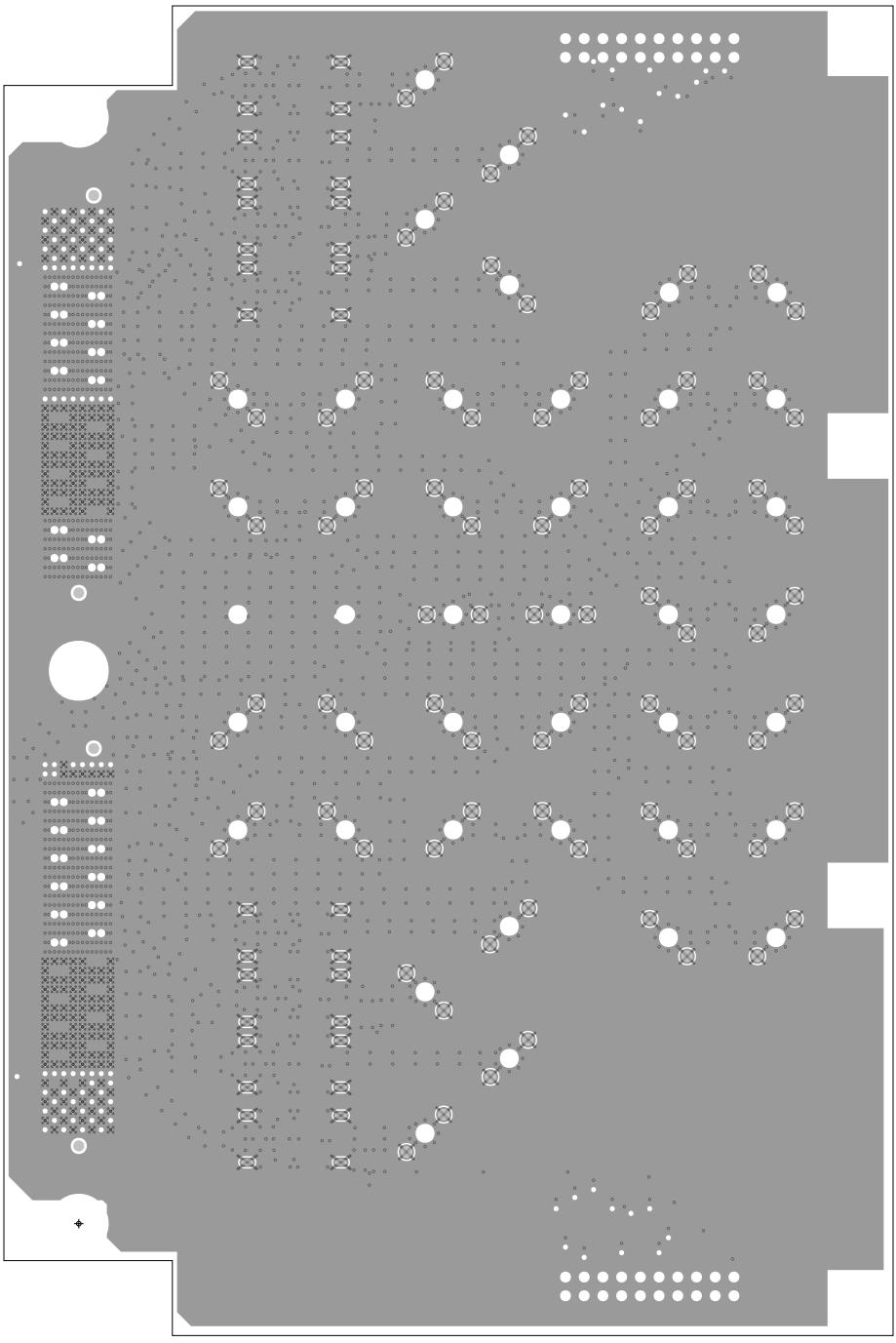
ARTWORK, ROHS COMPLIANT, HW-FMC-XM500	
PCB # 1281021	LAYER: L01_TOP
Designed by Xilinx	DATE: 06/14/2018
BOARD designer: GREG I.	PHONE: 408-879-6870
SHEET 01 OF 12	XILINX DOC USE ONLY REVISION: 1.0



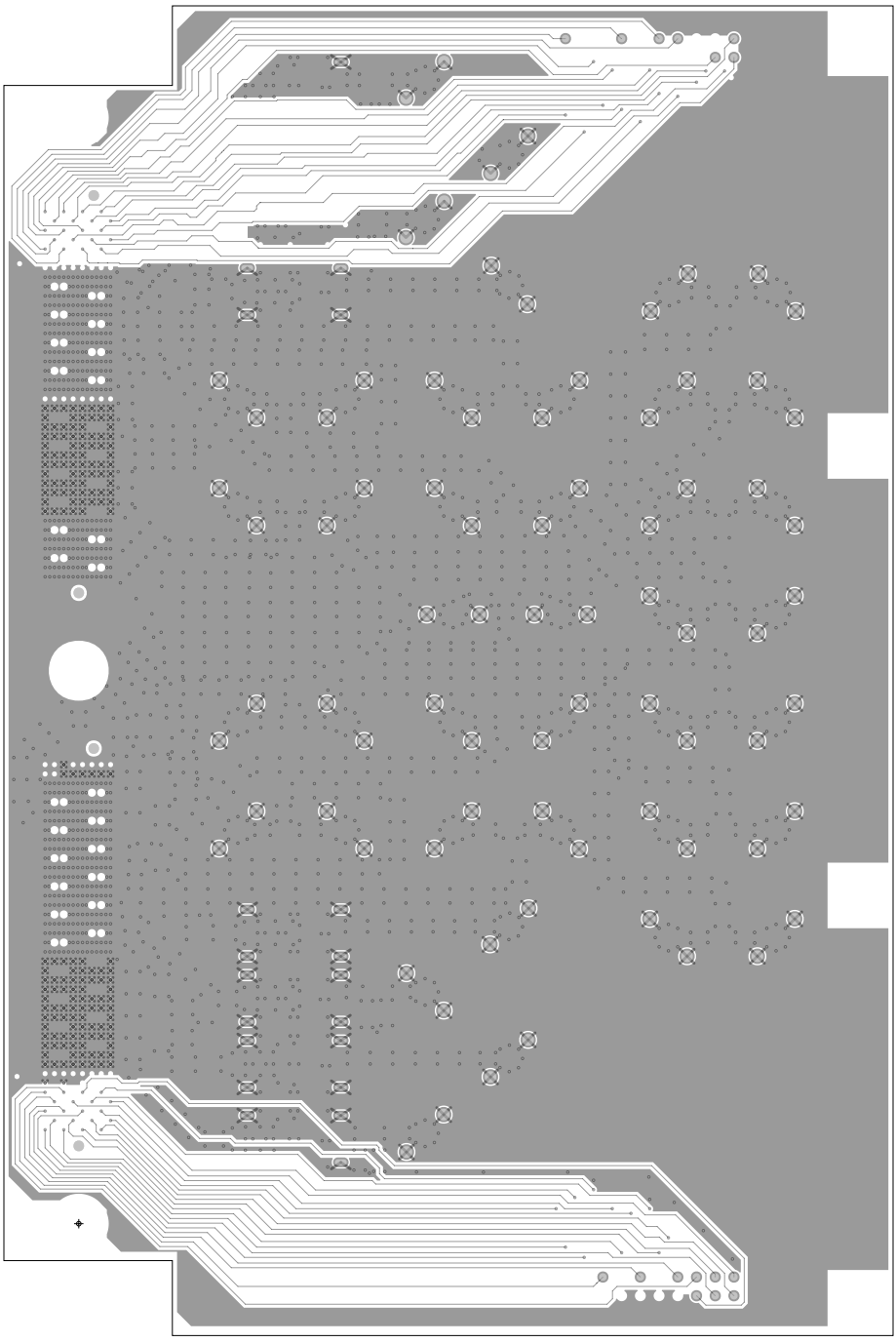
ARTWORK, ROHS COMPLIANT, HW-FMC-XM500	
PCB # 1281021	LAYER: L02_SIGNAL
Designed by Xilinx	DATE: 06/14/2018
BOARD designer: GREG I.	PHONE: 408-879-6870
SHEET 02 OF 12	XILINX DOC USE ONLY REVISION: 1.0



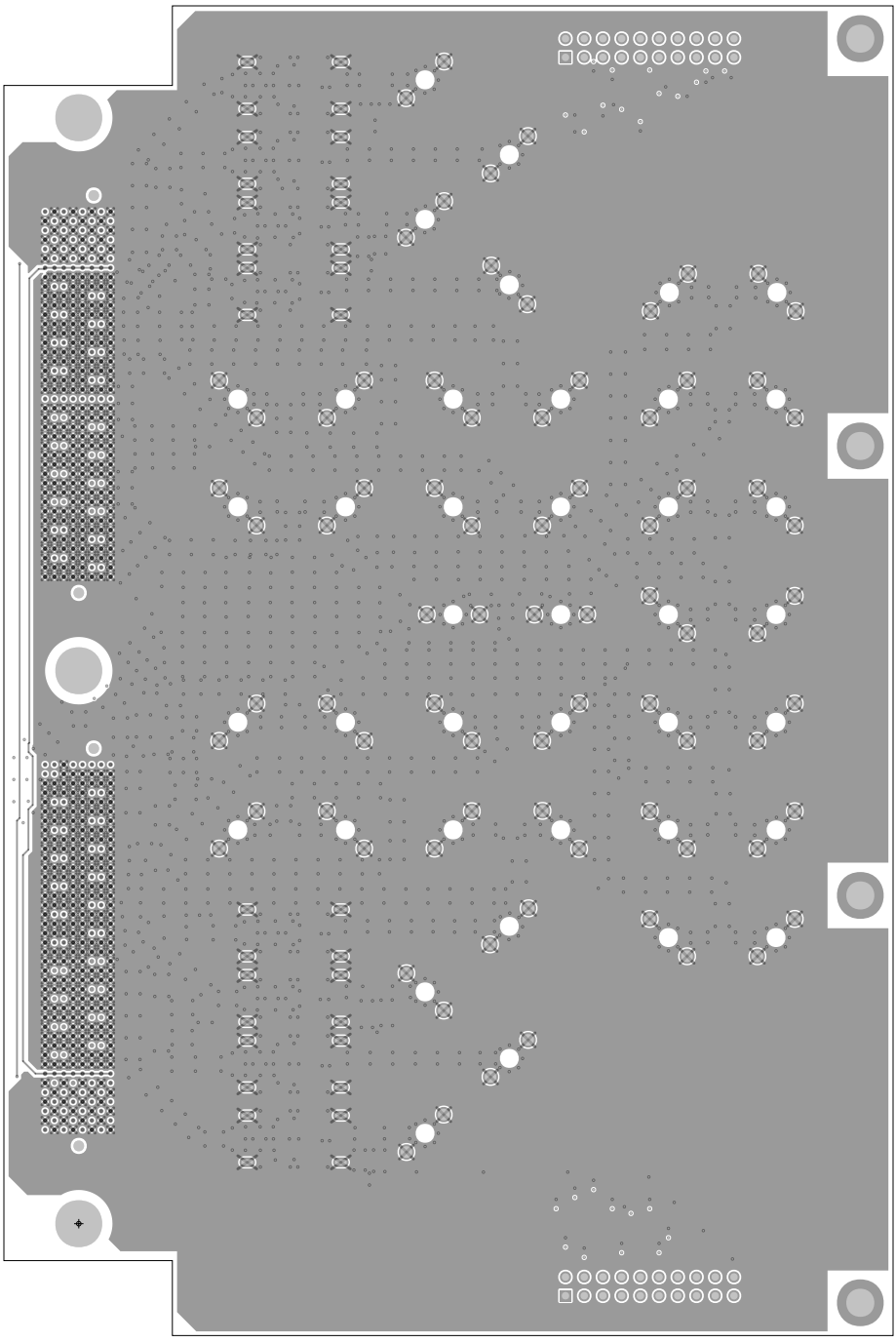
ARTWORK, ROHS COMPLIANT, HW-FMC-XM500	
PCB # 1281021	LAYER: L03+GND
Designed by Xilinx	DATE: 06/14/2018
BOARD designer: GREG I.	PHONE: 408-879-6870
SHEET 03 OF 12	XILINX DOC USE ONLY REVISION: 1.0



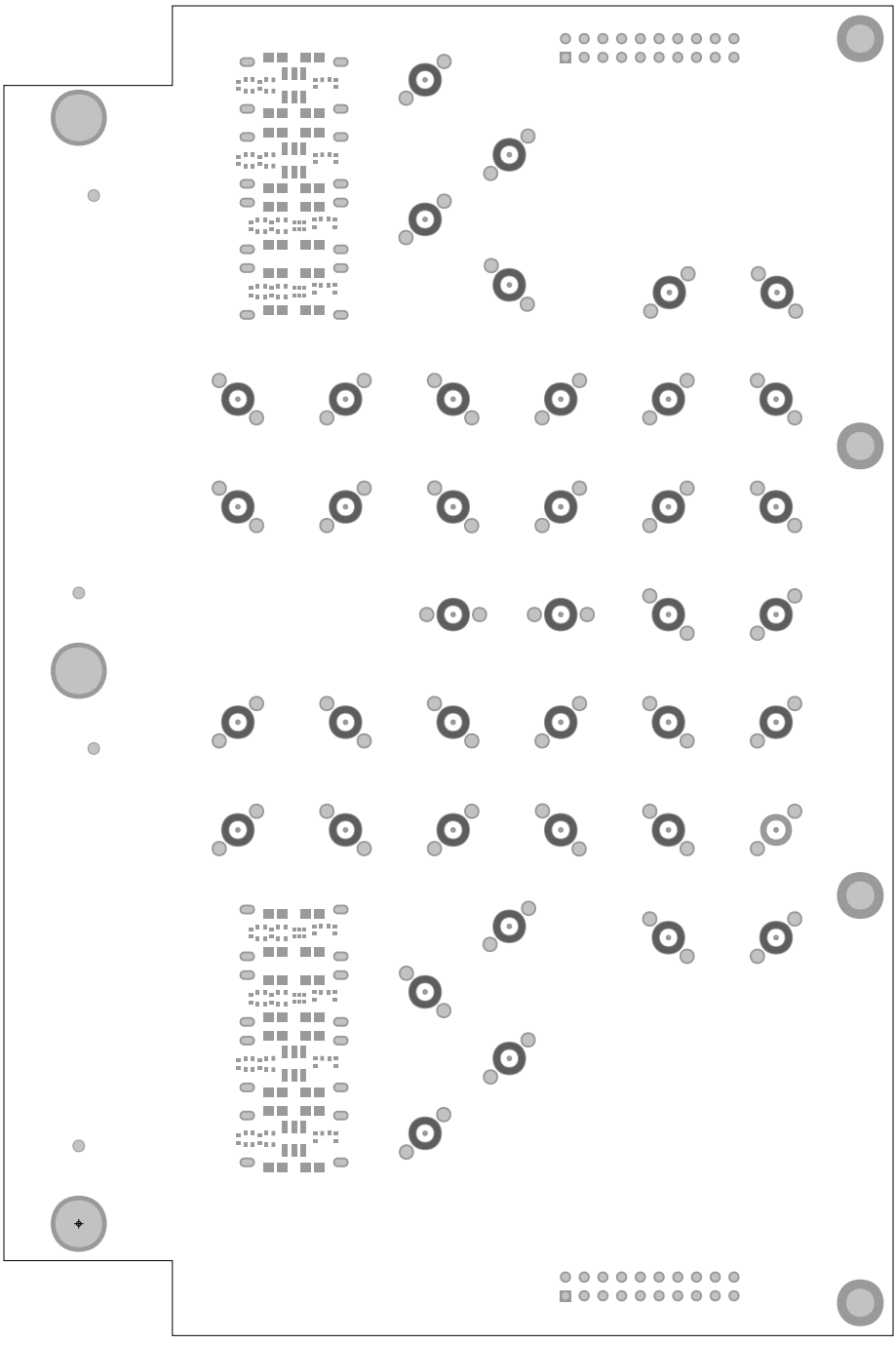
ARTWORK, ROHS COMPLIANT, HW-FMC-XM500	
PCB # 1281021	LAYER: L04_GND
Designed by Xilinx	DATE: 06/14/2018
BOARD designer: GREG I.	PHONE: 408-879-6870
SHEET 04 OF 12	XILINX DOC USE ONLY REVISION: 1.0



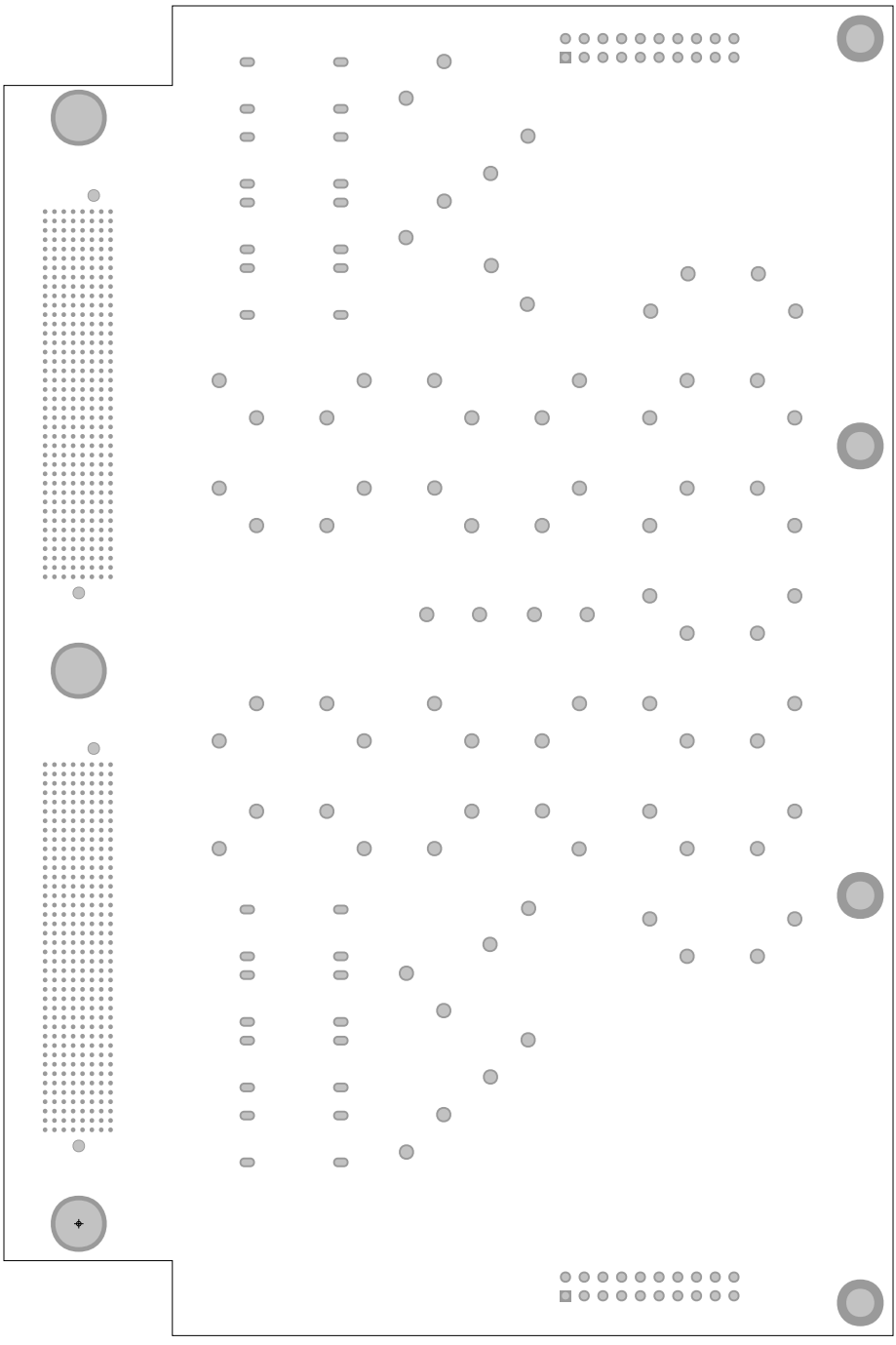
ARTWORK, ROHS COMPLIANT, HW-FMC-XM500	
PCB # 1281021	LAYER: L05_SIGNAL
Designed by Xilinx	DATE: 06/14/2018
BOARD designer: GREG I.	PHONE: 408-879-6870
SHEET 05 OF 12	XILINX DOC USE ONLY REVISION: 1.0



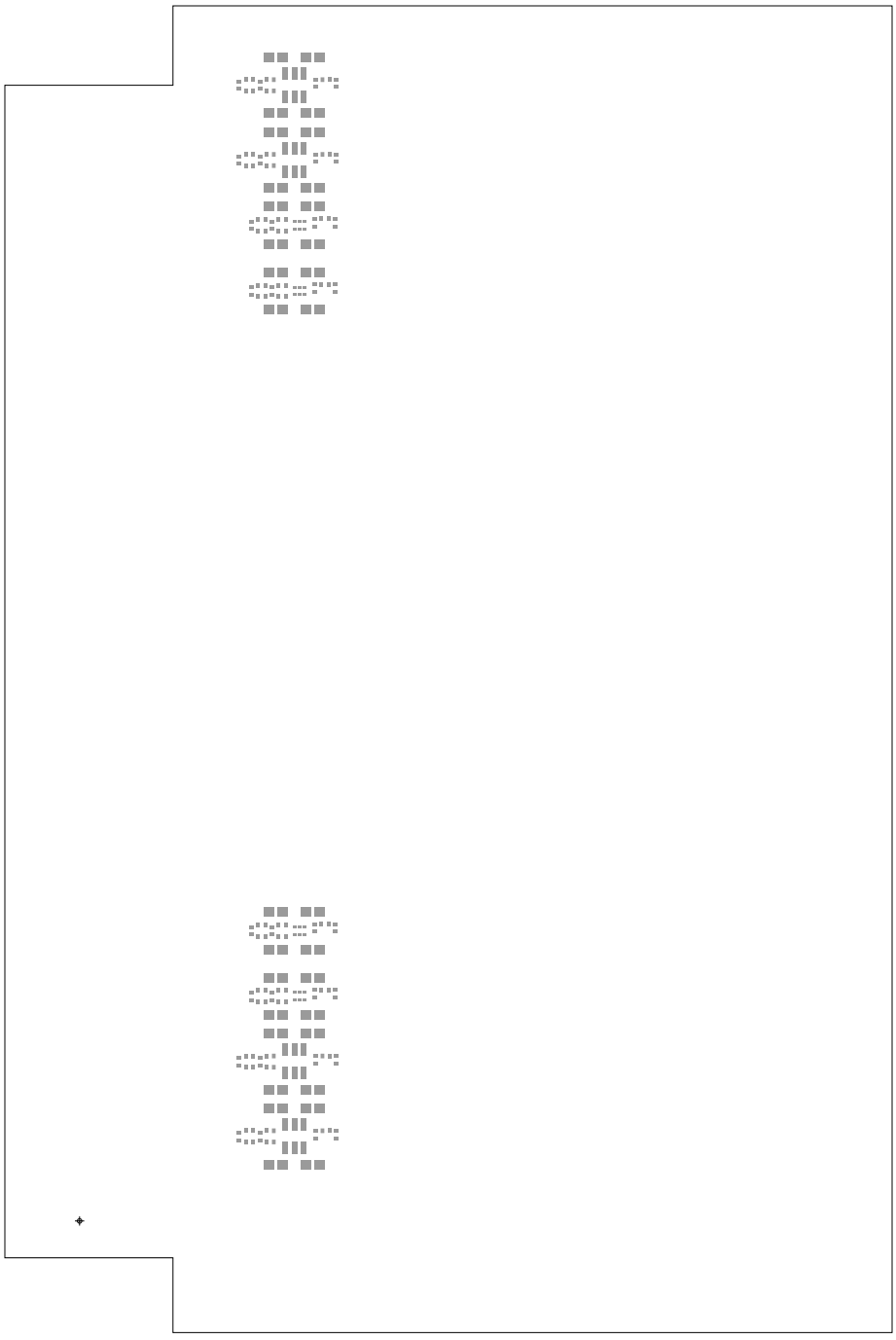
ARTWORK, ROHS COMPLIANT, HW-FMC-XM500	
PCB # 1281021	LAYER: L06_BOTTOM
Designed by Xilinx	DATE: 06/14/2018
BOARD designer: GREG I.	PHONE: 408-879-6870
SHEET 06 OF 12	XILINX DOC USE ONLY REVISION: 1.0



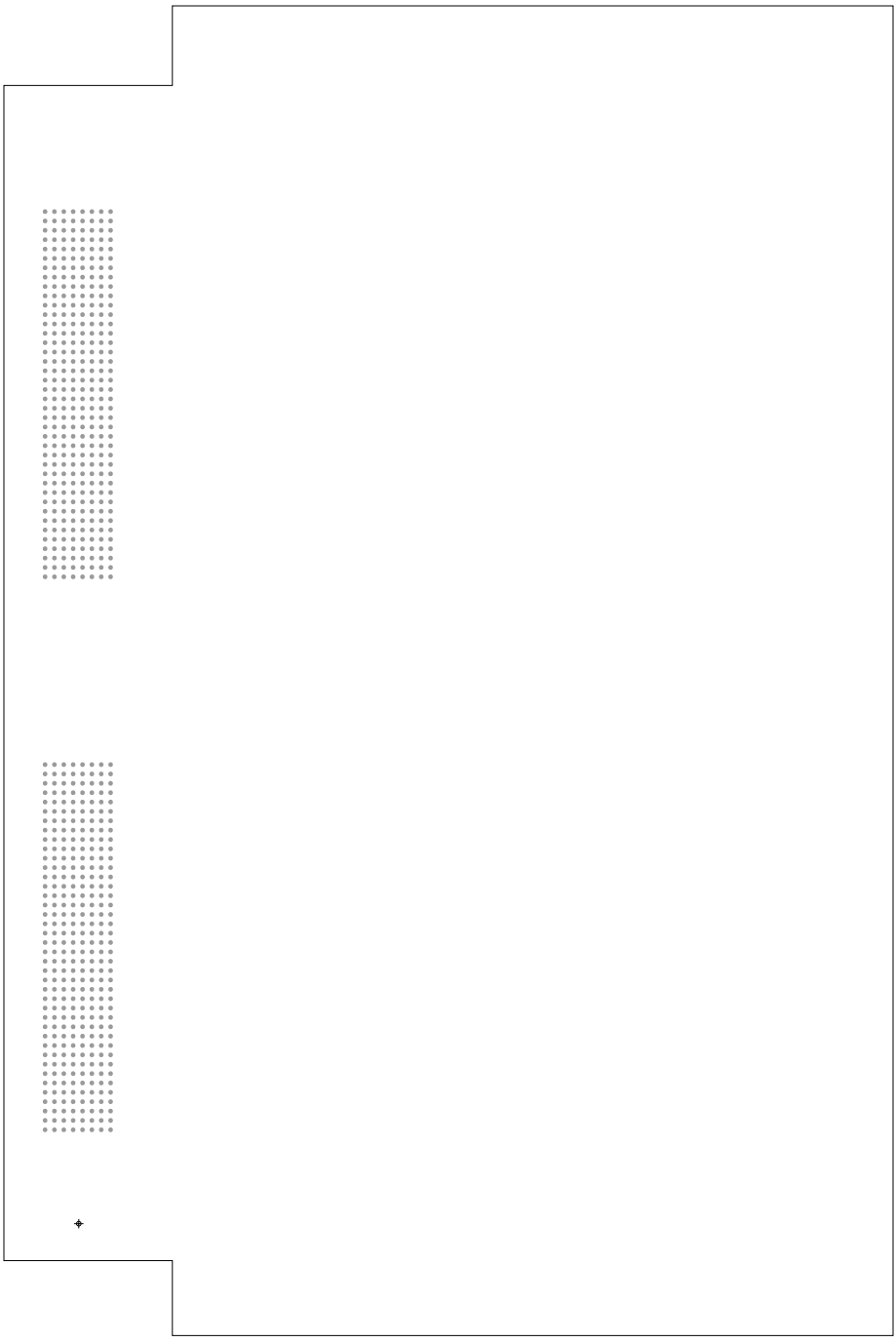
ARTWORK, ROHS COMPLIANT, HW-FMC-XM500	
PCB # 1281021	LAYER: L09_TOP_MASK
Designed by Xilinx	DATE: 06/14/2018
BOARD designer: GREG I.	PHONE: 408-879-6870
SHEET 09 OF 12	XILINX DOC USE ONLY REVISION: 1.0



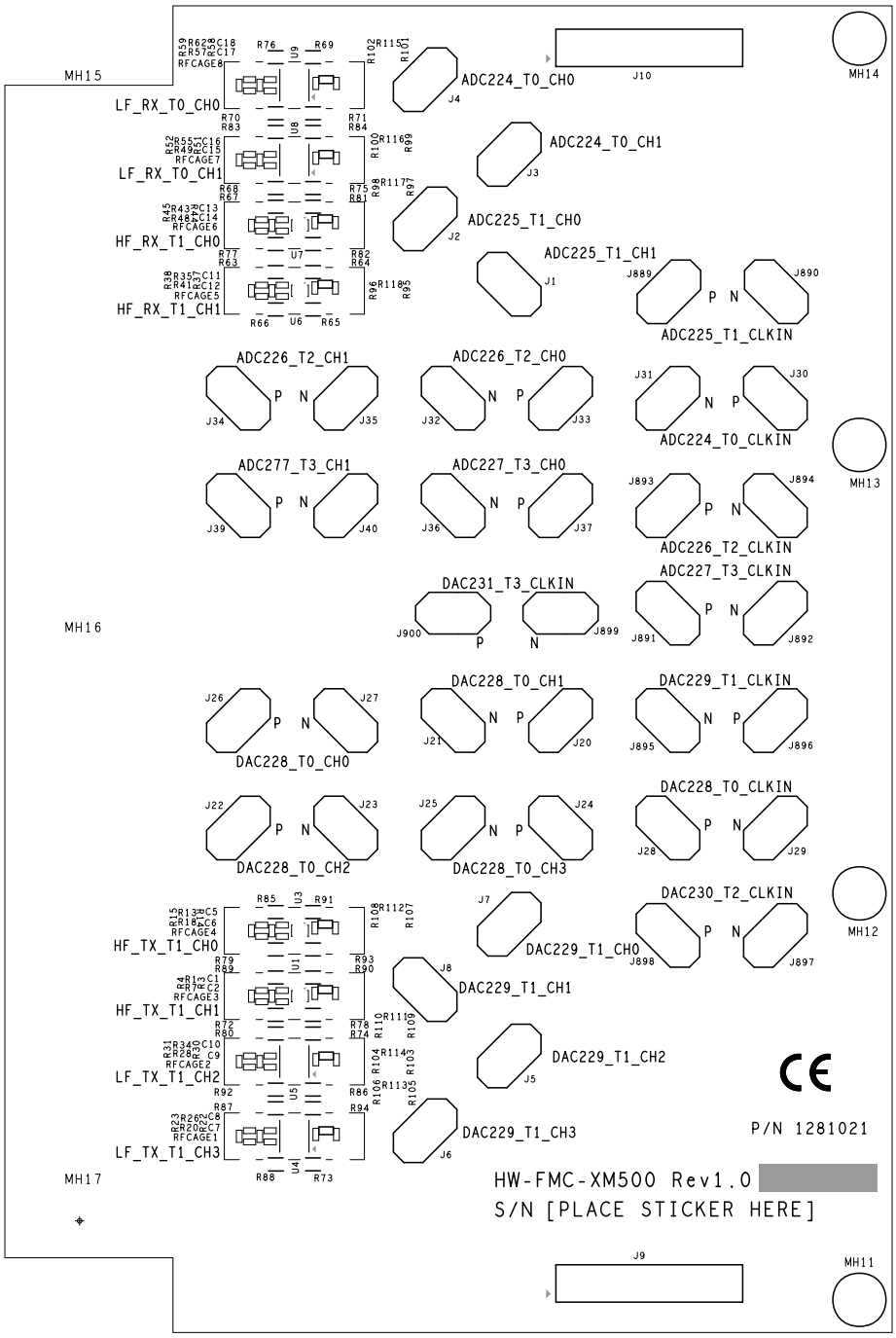
ARTWORK, ROHS COMPLIANT, HW-FMC-XM500	
PCB # 1281021	LAYER: L10_BOT_MASK
Designed by Xilinx	DATE: 06/14/2018
BOARD designer: GREG I.	PHONE: 408-879-6870
SHEET 10 OF 12	XILINX DOC USE ONLY REVISION: 1.0



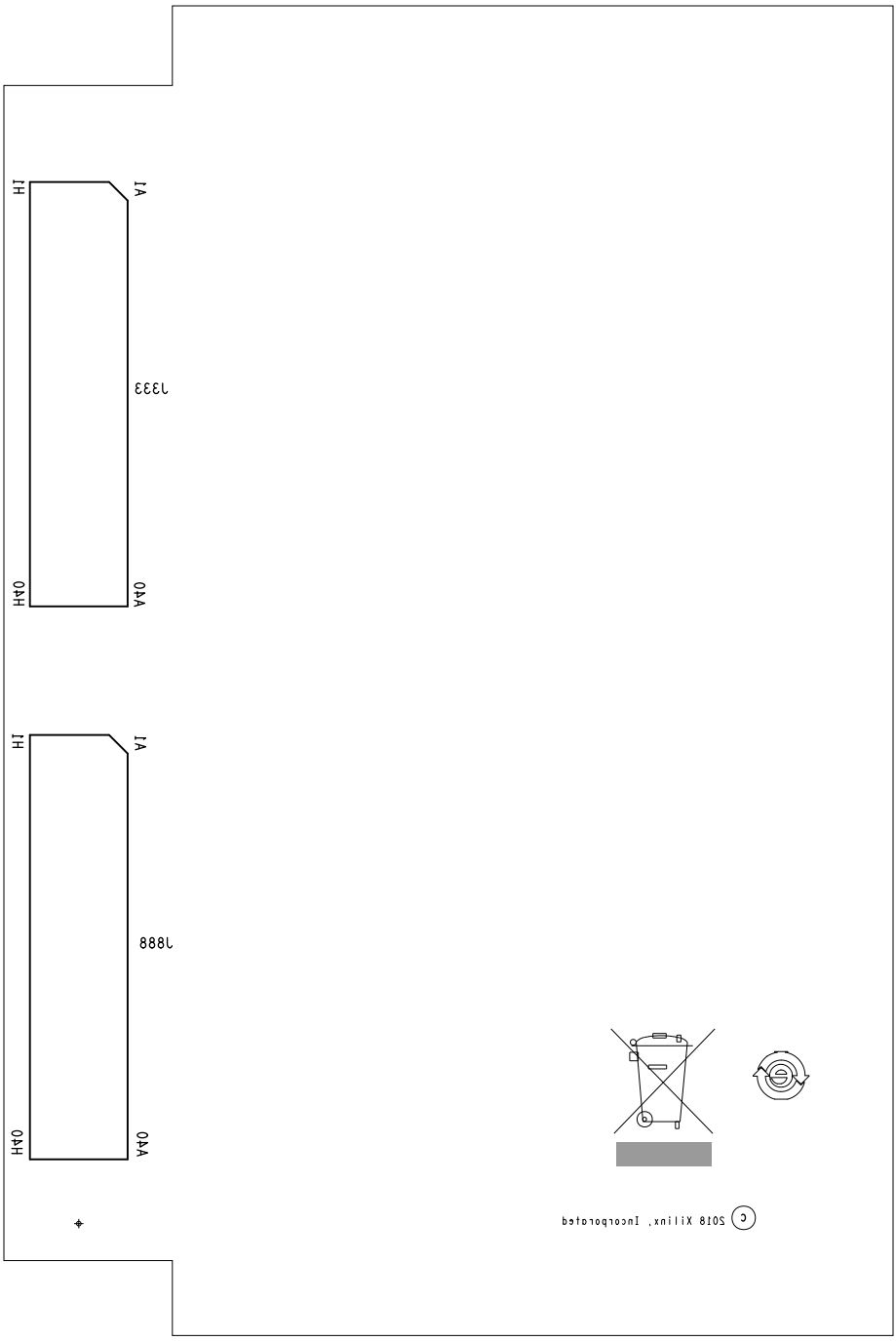
ARTWORK, ROHS COMPLIANT, HW-FMC-XM500	
PCB # 1281021	LAYER: L11_TOP_PASTE
Designed by Xilinx	DATE: 06/14/2018
BOARD designer: GREG I.	PHONE: 408-879-6870
SHEET 11 OF 12	XILINX DOC USE ONLY REVISION: 1.0



ARTWORK, ROHS COMPLIANT, HW-FMC-XM500	
PCB # 1281021	LAYER: L12_BOT_PASTE
Designed by Xilinx	DATE: 06/14/2018
BOARD designer: GREG I.	PHONE: 408-879-6870
SHEET 12 OF 12	XILINX DOC USE ONLY REVISION: 1.0



ARTWORK, ROHS COMPLIANT, HW-FMC-XM500	
PCB # 1281021	LAYER: L07_TOP_SILK
Designed by Xilinx	DATE: 06/14/2018
BOARD designer: GREG I.	PHONE: 408-879-6870
SHEET 07 OF 12	XILINX DOC USE ONLY REVISION: 1.0



ARTWORK, ROHS COMPLIANT, HW-FMC-XM500	
PCB # 1281021	LAYER: L08_BOT_SILK
Designed by Xilinx	DATE: 06/14/2018
BOARD designer: GREG I.	PHONE: 408-879-6870
SHEET 08 OF 12	XILINX DOC USE ONLY REVISION: 1.0