30.1: *Invited Paper:* 24-Inch Wide UXGA TFT-LCD for HDTV Application

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Abstract

A 24-inch wide screen format TFT-LCD with a resolution of 1920×1200 has been developed for high end monitor and HDTV application. This high-resolution display integrated with a novel wide viewing angle technology demonstrates itself as an ideal display for HDTV and multi-task monitor supported by its larger screen size and panel characteristics. In this paper, we present the system configuration, fabrication and characteristics of the panel. Also we propose new application areas for this high performance, high information content LCD monitor.

Introduction

As technology level for TFT-LCD advances, larger screen size and high resolution LCD monitors have been introduced for engineering workstations and financial market applications. 17 inch and 18.1 inch SXGA LCD monitors with wide viewing angle capability are introduced in the market since 1998. However, very high information contents application area such as displays for complex financial market analysis and CAD works. In addition, HDTV-TV requires large amount of pixel count and even larger screen size over 24 inch.

LCD for digital TV application also provides a great opportunity for TFT-LCD. However, there exists remaining technical and cost issues in order to be practically applied to large screen size TV over 20". LCD-TV is considered as a new important business territory for future growth of TFT-LCD industry.

There were many panel driving approaches to overcome the insufficient panel charging problem such as complicated driving techniques, timing manipulations to obtain enough charging time [1][2] or dual scan driving method using frame memory. Sufficient and uniform pixel charging is primarily relates to panel's picture quality and performance. However, designing simplified and standard structure is also an important system design criteria for the cost effective production of display systems.

In this work, we propose a series of practical criteria for designing and driving large size panel for wide format 24 inch. In addition, we describe a novel wide viewing technology that was applied to the fabrication of the panel showing a high level of electro-optical performance.

Panel Design

As panel size and resolution of display increases, the design consideration for pixel charging becomes more critical. The major difficulty is signal delay and distortion coming from high resistance and parasitic capacitance of long row and column lines. Therefore, minimizing line loading is the primary concern in designing the active matrix.

Fig. 1 shows the dimension of 24-inch panel, it comprised of 20.39 inch long 1200 gate lines and 12.74 inch long 5760 data lines (Fig.1). The allocated gate line charging time for WUXGA panel is less than 10 μsec. Because of its longer gate line dimension, reducing gate line delay is a primary important factor to achieve a uniform screen quality without cross-talk and flicker effect that can be caused by the insufficient pixel charging across the large display area.

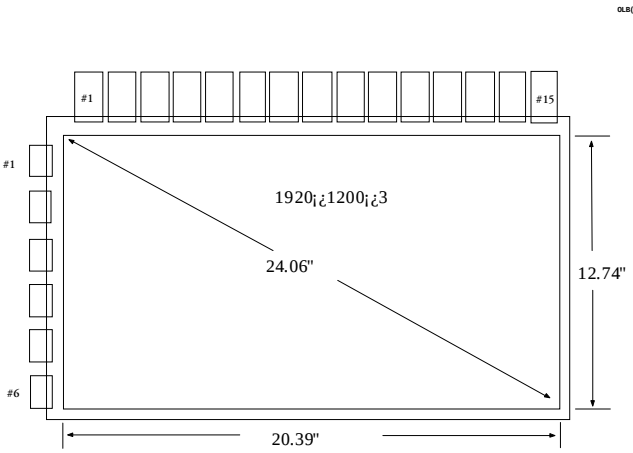

Fig. 1 24-inch TFT-LCD panel dimensions

Therefore, it is critical to have a minimum gate line loading by using low resistance aluminum gate line and TFT design for minimized parasitic capacitance in order to use the single scan, single-sided driving method.

To review the pixel charging conditions and calculate minimum requirements for single scan, single-sided gate and

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data driving for 24-inch panel, Hspice simulation tool was applied to pixels and driving signals. Fig. 2 and 3 show simulated waveform of gate and data line signals, respectively. Fig. 4 and 5 show the measured signal delay for gate and data line, respectively. By comparing the simulated and measured data of RC delay, we were able to obtain relatively accurate design parameters of pixel and panel structure.

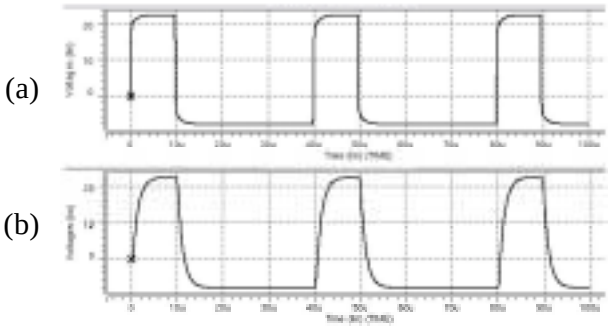

Fig. 2 Simulated waveforms of gate signal at left and right positions.

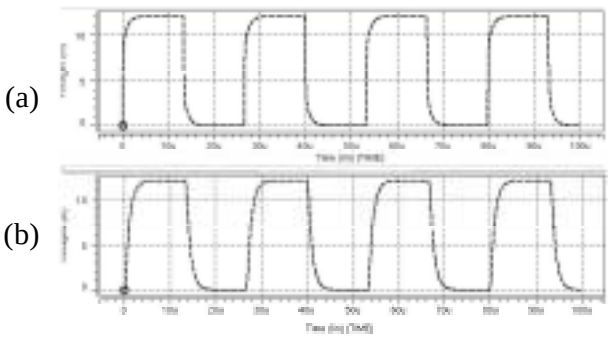

Fig. 3 Simulation results of the data signal at (a) top and (b) bottom position (b)

According to the simulation results, it was noted that gate line delay causes insufficient charging to pixels that relates to flickering of the screen, while data line delay causes insufficient pixel charging that relates to vertical cross-talk. For minimum data line delay, we used Cr/Al alloy/Cr claded structure. By using Al alloy gate and data line structure with minimized parasitic capacitance design, sufficient pixel charging within 9.8 μsec was feasible with single scan, single sided driving method.

Driving Method

With reduced line resistance, single scan for row drive could be possible, and single sided column driver was also possible. Single scan configuration of column drive causes a high

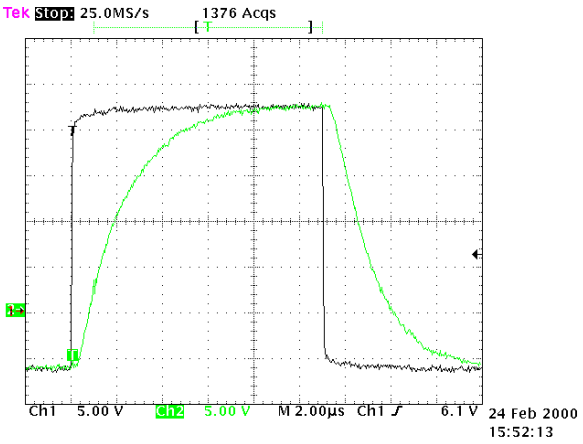

Fig. 4 Waveform of the gate signal at (a) left and (b) right position

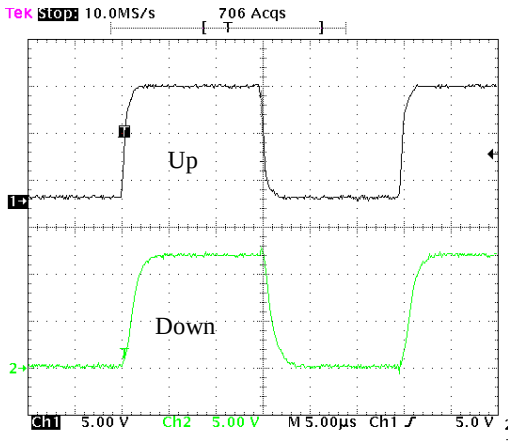

Fig. 5 Waveforms of data signal at top and bottom positions.

frequency condition compared to both sided column drive case. However, with the split of data bus lines, we were able to reduce clock and data rate enough to use slow peripheral devices under 30Mhz. Using 8bits per sub-pixel, the bandwidth of display data is 3.3 Gb/sec. To reduce the data clock frequency of driving circuits, the display area is divided into 4 blocks, i.e. 4 different data bus are required to carry each block data. And each bus consists of 2 pixel data at one clock edge. Thus total pixel data rate per one clock edge would be 8 pixels/clk, because column drivers have 2 port input for data as usual. Normally, currently available column driver ICs have dual port input.

For the simplicity of system interface, system input interface can not be divided into 2 pixel/clock, i.e. the timing controller (T-CON) receives dual digital data (even/odd) per clock.

Timing controller input receive data come from interface IC like TMDS or LVDS. With VESA standard blanking at 60Hz frame rate, equivalent clock rate is 190MHz estimated, therefore, 97.5MHz clock signal is used for data transmission between graphic system to panel with 2 pixel/clock rate. LVDS type (DS90C388, Receiver) interface is used because this interface can support over 120MHz per channel at 2pixel/clock rate. If maximum reduced blanking suggested by DVI-DDWG is allowed, TMDS (SiI161) may be a solution for this interface. To handle 4 different parallel data bus at the same time two T-CON must be used, because there are too many signal lines to fan out from a single chip package. Each T-CON can control 4 digital data bus, and 2 data bus send 2 pixel/clock data to the one of each blocks simultaneously as shown in Fig. 6.

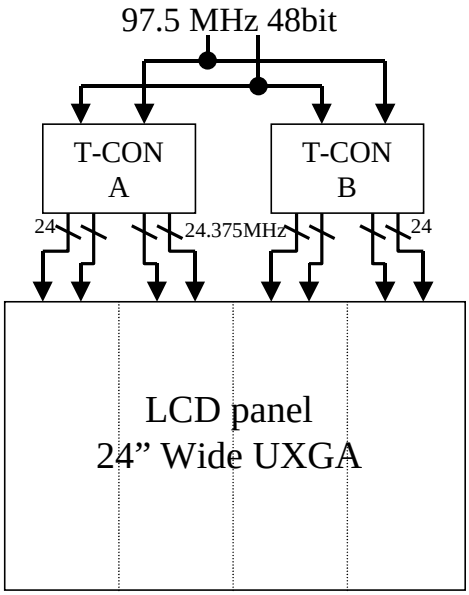

Fig. 6 Driving schematics of 24-inchWide UXGA panel

System Configuration

Total system used for 24-inch WUXGA display consists of 3 parts; computer with graphic card, interface board with scaler IC, and 24 inch TFT-LCD module. IBM-PC compatible computer that can support high performance graphic card is required. This graphic card usually has DVI output or standard analog RGB output for graphic signal. With DVI suggestion, DVI output of graphic card might be connected to directly to panel, if we consider reduced blanking time. For analog case, input part of interface board will be exchanged with suitable A/D converters. Fig. 7 shows 24-inch WUXGA display system that can support DVI interface with multi-sync scaling function. This interface board has on-screen-display function, control software that support sync timing variation and image scaling logic circuits supporting various resolutions.

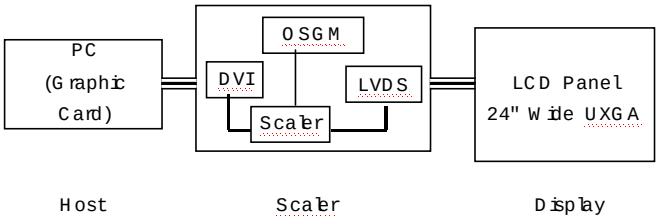

Fig. 7 System design of 24-inch WUXGA

Panel Process with Wide Viewing Angle Technology

For the enhancement of panel viewing angle, we have developed a novel VA mode (vertical alignment). We named the mode as PVA (patterned vertical alignment), that utilizes the fringe field effect of VA mode by pattering the ITO electrode. Through the combination of computer simulation and experiments, we optimized the cell parameters and process conditions. The electro-optical properties of the fringe field effect can be optimized by cell parameters, multi-domain structure and film compensation. As a result, this 24-inch wide UXGA TFT-LCD monitor showed a contrast ratio over 500:1, panel transmittance near 4.8 %, response time near 27 ms, and viewing angle higher than 80 degree in all directions (see Table 1). Details of PVA angle technology is described in [3,4].

Table 1. Electro-optical properties of 24-inch WUXGA PVA TFT-LCDs

Panel size	24” diagonal (16:10)
Resolution	WUXGA (1920×1200)
Luminance	420 cd/m^2
Panel transmittance	4.8 %
Contrast ratio	> 500 : 1
Response time	27 ms
Viewing angle (U/D/L/R) Diagonal direction	> 80 ° > 80 °
Gray scale inversion	> 80 °
Flicker	< 2
Cross-talk	0.73 %
Color reproduction	54 %
Driving voltage	6 V

Fig. 8 and 9 illustrate actual 1920 x 1200 display image of 24-inch WUXGA in a module and completed monitor, respectively.

Fig. 8 Actual display image of 24” WUXGA module

This figure is reproduced in color on page 1311.

Fig. 9 Actual display image of 24” Wide TV

This figure is reproduced in color on page 1311.

Application Areas for 24” Wide Monitor

The 24-inch screen is large enough to accommodate two A4 size or two letter size and still leaves extra space for icon bars. This size provides an ideal full size screen for high productive professional applications such as CAD/CAE, desktop publishing, web master or wide spreadsheet in a finance market. For HDTV application, where the requirements for display is more stringent in the area of brightness, contrast ratio, screen size, wide viewing capability and fast liquid crystal response time, this 24-inch wide display nearly satisfies the requirements.

Conclusions

We have developed a 24-inch multi-function monitor, that can be applied to HDTV and high information content multi-task information display. This is the first TFT-LCD developed that can receive true HDTV signal either in 1920x1080 interlaced or 1280x720 progressive format.

A noble wide viewing angle technology, PVA, was proven to be a feasible solution for manufacturing larger size TFT-LCD with high performance panel characteristics. We also proposed a multi-sync interface solution that links between computer and this 1920x1200 format LCD.

References

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