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AMOLED pixel driver circuits based on poly-Si TFTs: A comparison

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Abstract

In this paper, four different driver circuits for an active matrix organic light-emitting diode (AMOLED) pixel based on thin film transistor (TFT) technology are analyzed and compared. In particular, the comparison analyzed accuracy, driving speed, power consumption and area occupied. Moreover, in order to allow array simulations, the RC equivalent models of the pixel were also derived. The results were achieved considering a QVGA display (320×240), a line frequency of 60 Hz, and were verified by simulations with AIM-SPICE.

Keywords: TFT; Driver; AMOLED; Digital circuit; Mixed design

1. Introduction

Organic light-emitting diode (OLED) displays are power efficient, vivid and ideal for portable applications. Indeed, they have a lower material cost and fewer processing steps than LCDs. For these reasons OLED displays appear to be the best candidate for a variety of mobile applications.

The OLED is a current-driven device where the luminance level is determined by the level of current flowing through it. This current can be provided by a passive matrix OLED (PMOLED) or active matrix OLED (AMOLED) backplane architecture. In the latter case, a thin film transistor (TFT) circuit composes the matrix. This solution is preferred over the passive matrix approach, especially when the size of the display is increased. This is because passive matrix schemes require high-current level peaks through the pixel to obtain high luminance peaks. Higher power consumption has adverse effects on OLED reliability in the passive matrix [1].

Several OLED driver circuits, which differ in their driving speed, power consumption, area occupied and the accuracy needed to set the current level (i.e., the OLED brightness), have been presented in the literature [2,5–7]. In this paper, we review four AMOLED driver circuits having two or three input lines (data and select) and a simple signal management, and we carry out in-depth analysis and critical comparisons. Although there are other driver circuits which allow to compensate threshold voltage shift, such as [8,9], they need more control lines and complicated signal management. In particular, in Section 2 the four circuits are presented and classified into voltage-programming driver circuits and current-programming driver circuits. In Section 3, we introduce the metrics adopted to develop the comparisons. In Section 4, we give the design rules and process parameters of poly-TFTs considered and then compare the solutions. In Section 5 simulation results are reported and compared with analytical results. Finally, in Section 6 conclusions are given. The manuscript also contains an Appendix A, which presents an evaluation of the time required to charge the driver's TFT capacitance.

2. OLED driver circuits

The OLED driver circuits can be divided into two main classes: voltage-programming driver circuits and current-programming driver circuits depending on the kind of data. For both it is preferable for the OLED to be connected to the drain terminal of the driving TFT. Indeed, connecting the OLED to the source of the driving TFT results in the

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driving TFT gate–source voltage dependence on the drop across the OLED, which may change over time [7].

2.1. Voltage-programming driver circuits

The simplest OLED driver circuit is realized by using a TFT in common-source configuration. Here the current level, which is that of the TFT drain, is set by the voltage signal applied to the TFT gate terminal, as clearly shown by the well-known transistor relationship

$$I_{DS1} = \mu_0 C_{ox} \frac{W_1}{L_1} \frac{(V_{GS1} - V_t)^2}{2}, \quad (1)$$

where the parameters have the usual meanings, and we neglected second-order effects.

Following this approach, the simplest driver circuit, named 2-TFT and shown in Fig. 1, is made up of two TFTs (T_1 and T_2). In particular, transistors T_1 and T_2 are the driving transistor and selection transistor, respectively. The presence of both parasitic (C_{gs} and C_{gd} due to the overlap between gate and source/drain) and intrinsic (C_g due to gate oxide layer) capacitances is highlighted in Fig. 1. When the Select line is high, transistor T_2 is switched on and the data passes from Dataline to the gate of T_1 charging its gate capacitance. When Select goes down, transistor T_2 is switched off and the data is stored at the gate of T_1 where, neglecting current leakage, it is held constant (i.e., the OLED current is constant) thanks to the capacitances at the TFT gate until the next refresh which sets a new data value.

The limit of the above topology is due to the heavy drain current dependence on the TFT's threshold voltage shift and mobility variation, which can reach 50% and 10%, respectively.

To overcome this drawback of the simplest topology a self-compensated circuit must be introduced, but more components are needed. In particular, the self-compensated topology shown in Fig. 2 was proposed in [2]. This topology, that in the following will be called 4-TFT driver circuit, exploits the matching of transistor T_1 and T_3. Indeed, assuming that the gate of T_1 is previously precharged to an high value through TFT T_4, when the data is applied to the Dataline T_4 and T_3 turns off and on, respectively. Thus the gate voltage of T_1 reaches the value $V_{Dataline} + V_{t,T_3}$. If T_1 and T_3 have the same threshold

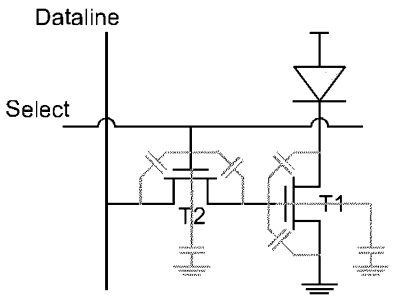

Fig. 1. 2-TFT OLED driver circuit.

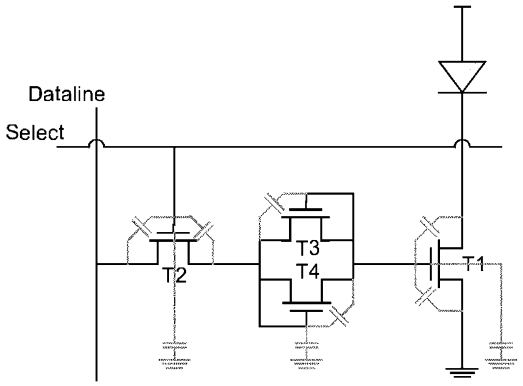

Fig. 2. 4-TFT OLED driver circuit.

voltage (this is a reasonable assumption if they are in physical proximity to each other on the wafer), the current level results as

$$\begin{aligned} I_{DS1} &= \mu_0 C_{ox} \frac{W_1}{L_1} \frac{(V_{GS,T_1} - V_{t,T_1})^2}{2} \\ &= \mu_0 C_{ox} \frac{W_1}{L_1} \frac{(V_{Dataline} + V_{t,T_3} - V_{t,T_1})^2}{2} \\ &= \mu_0 C_{ox} \frac{W_1}{L_1} \frac{V_{Dataline}^2}{2}. \end{aligned} \quad (2)$$

Then, the driver is reset by applying to the Dataline a negative voltage, which discharges the gate of T_1 through TFT T_3.

It is apparent that even if the threshold voltage shifts are solved, the current level is still heavily dependent on the variation in mobility. Nevertheless, since mobility variation is generally lower than 10%, it can be ignored.

2.2. Current-programming driver circuits

To accurately set the current on the OLED, we can adopt a current-programming mode approach. Specifically, topologies whose circuit core is based on a TFT current mirror have been proposed. If the two transistors that constitute the current mirror are matched (i.e. close and with the same electrical characteristics) and neglecting the channel length modulation, the current at the output node (i.e., provided to the OLED) is equal to

$$I_{load} = \frac{W_1/L_1}{W_2/L_2} I_{data}, \quad (3)$$

where I_{data} is set at the input of the current mirror and $(W_1/L_1)/(W_2/L_2)$ is the mirror aspect ratio. Its independence from mobility and threshold voltage variations is apparent in Eq. (3).

The current-programming topology shown in Fig. 3 is equivalent to that presented in [3]. Except for a small change in the topology that does not affect fundamental behavior, it is based on the same principle as switched current (SI) circuits based on a current mirror that implements a current track-and-hold [4]. Indeed, when

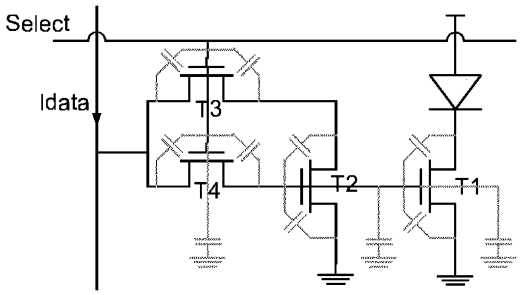

Fig. 3. Current mirror driver circuit.

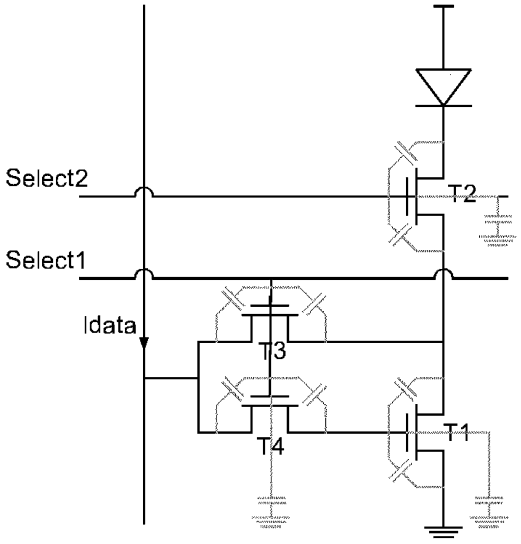

Fig. 4. One-transistor current memory driver circuit.

the TFT T_3 and T_4 are switched on, TFT T_1 and T_2 act as a current mirror. Instead, when T_3 and T_4 are switched off, TFT T_1 holds the last value of current level (before the switches are opened), thanks to its gate capacitance, which maintains the voltage constant.

Another current-driver circuit was proposed in [5,6] and is shown in Fig. 4. This circuit is again based on the SI approach, but uses the one-transistor current memory topology [4]. In particular, when the signal Select1 allows the TFT T_3 and T_4 to switch on, the TFT is diode connected and current I_{data} flows through it. Moreover, once the TFT T_2 opens thanks to the Select2 signal, T_1 is disconnected from the OLED. When transistors T_3 and T_4 are opened and T_2 is closed, T_1 gate capacitance holds a voltage that sets the T_1 drain current equal to I_{data}.

3. Driver circuit metrics

To compare the four driver circuits introduced in the previous section, we assumed that all the circuits had to set an equal amount of current. This choice allowed them to be compared independently of the load. Hence, the specific topology was analyzed only in terms of driving speed, power consumption, and area occupied.

3.1. Driving speed

The frame rate (FR) of a pixel matrix is an important feature for a display and is related to the driving speed. In particular, the FR is defined

$$FR = \frac{1}{n(t_{line} + t_{settle} + t_{discharge})} \approx \frac{1}{n(t_{line} + t_{settle})}, \quad (4)$$

where n is the number of matrix rows, t_{line} is the time required to charge all the capacitances in a row, t_{settle} is the time needed to charge the driver TFT capacitance, and $t_{discharge}$ is the time slot to switch off and discharge an entire row. Since the major contribution comes from t_{line} and t_{settle} the approximation holds [3].

Assuming a line frequency equal to 60 Hz, it must be $FR > 60$ Hz. Hence, t_{line} and t_{settle} limit the number of columns and consequently, the size of the entire display. In contrast, considering n a constant, FR can be considered as an index of speed performance.

As shown in [10], we can evaluate t_{line} of a matrix with m columns

$$t_{line} = 2.2 C_{eq} R_{eq} \frac{m(m+1)}{2}, \quad (5)$$

where R_{eq} and C_{eq} are the resistance of the select line and the sum of the select line capacitance, $C_{data\text{-}select}$, with the gate capacitance of the switching TFTs, respectively.

It is worth noting that the relationship of C_{eq} is different for voltage- and current-programming driver circuits, since the circuitry to connect and disconnect the driving transistor from the line providing data is different. In particular, for voltage-programming driver circuits, which need of the only TFT T_2 used as switch, it is equal to

$$C_{eq} = C_{data\text{-}select} + C_{gT_2} + C_{gsT_2} + C_{gdT_2} \quad (6a)$$

and for current-programming driver circuits, which contain both the switching TFT T_3 and T_4 whose gates are connected to Select line, it is equal to

$$C_{eq} = C_{data\text{-}select} + C_{gT_3} + C_{gT_4} + C_{gsT_3} + C_{gdT_3} + C_{gsT_4} + C_{gdT_4}. \quad (6b)$$

It is worth noting that in (6a) and (6b) we include the effect of parasitic capacitances too. Indeed, we are assuming that when the Select goes up the drain and source voltages of the switching TFTs remain constant; thus the entire capacitive load on the Select is provided by the intrinsic capacitance ($C_{data\text{-}select}$), the gate capacitance of the switching transistors (C_g), and their parasitic capacitances (C_{gs} and C_{gd}).

By inspection of Eq. (5), it is apparent the square law dependence of t_{line} from m in practical cases makes the contribution of time t_{settle} (evaluated in the Appendix A) negligible with respect to t_{line}. This is true of course for high and medium gray levels. Indeed, as highlighted by (A.1), t_{settle} must be taken into account when low gray levels (i.e., low values of I_{data}) are of concern.

In conclusion, to compare the topologies we have to evaluate the capacitive load on the select line and on the gate of the driving TFT, and assume m and n are constant. In the following, keeping in mind the features of QVGA, we will assume $m = 320$ and $n = 240$.

3.2. Power consumption

Power consumption in a circuit depends on a variety of factors including OLED current requirements, the supply voltage, TFT sizing, and current rise times. In general, we have both static and dynamic power consumption contributions. However, to compare the topology, under the assumption of an equal output current, we need only to consider the dynamic contribution

$$P_{\mathrm{dyn}} = C_{\mathrm{Deq}} V_{\mathrm{swing}}^2 f, \tag{7}$$

where C_{Deq} is the charging and discharging equivalent capacitance at the gate of the driving TFT, V_{swing} is the voltage swing on the node and f is the signal frequency set to 60 Hz.

3.3. Area

In this specific application, silicon area represents an important feature, especially for an AMOLED display bottom emitting [3]. Indeed, here the OLED is placed near the circuitry, thus placing a limit on the aperture ratio, since the effective area through which the light passes is less than the total pixel area. Of course circuits with lower and smaller components (i.e. a higher aperture ratio) allow a higher level of brightness.

4. Comparisons

To compare the four driving circuits, we consider the TFT shown in Fig. 5 whose main design rules, device parameters and related parasitics are summarized in Table 1. We assume the driving TFTs to be equal, and report their transistor aspect ratios together with those of the other transistors in the driver in Table 2. The gate to source, gate to drain, and gate capacitances are also given in Table 2. Capacitance values of C_{eq} and C_{Deq} are those reported in Table 3.

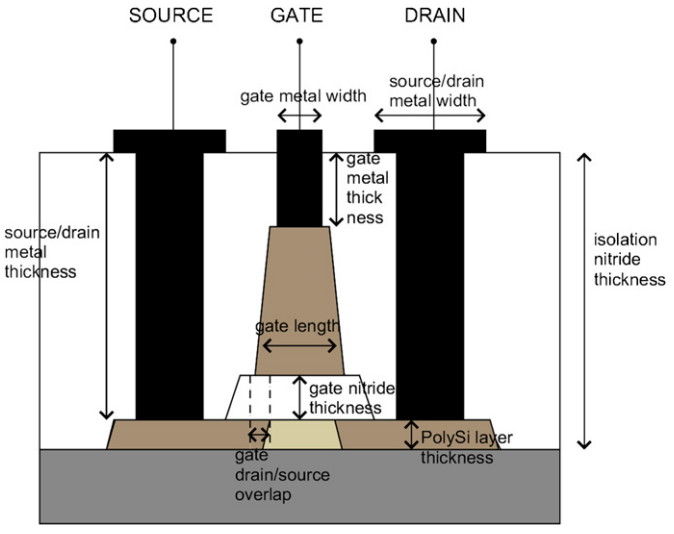

Fig. 5. TFT cross-section (the quantities indicated are evaluated in Table 1).

Table 1
Design rules, device parameters and parasitics

Parameter	Value
Gate length	12 μm
Gate metal width	10 μm
Source/drain metal width	15 μm
Contact size	10 μm × 10 μm
Gate/drain–source overlap	1 μm
Gate metal sheet-resistance	0.058 Ω/□
Source/drain metal sheet-resistance	0.9 Ω/□
Gate-nitride thickness	100 nm
Poly Si layer thickness	50 nm
Gate metal thickness	75 nm
Source/drain metal thickness	200 nm
Isolation-nitride thickness	1 μm
$C_{\mathrm{data\text{-}select}}$	0.46 fF
R_{select}	12 Ω
R_{data}	0.84 Ω

Table 2
Driver characteristics

	2-TFT	4-TFT	Current mirror	Current memory
T_1	1 μm/1 μm	1 μm/1 μm	1 μm/1 μm	1 μm/1 μm
T_2	1 μm/1 μm	1 μm/1 μm	1 μm/1 μm	1 μm/1 μm
T_3	–	1 μm/1 μm	1 μm/1 μm	1 μm/1 μm
T_4	–	1 μm/1 μm	1 μm/1 μm	1 μm/1 μm
$C_{\mathrm{gs,gd}}$ (T_1) (fF)	0.4	0.4	0.4	0.4
$C_{\mathrm{gs,gd}}$ (T_2) (fF)	0.4	0.4	0.4	0.4
$C_{\mathrm{gs,gd}}$ (T_3) (fF)	–	0.4	0.4	0.4
$C_{\mathrm{gs,gd}}$ (T_4) (fF)	–	0.4	0.4	0.4
C_{g} (T_1) (fF)	0.3	0.3	0.3	0.3
C_{g} (T_2) (fF)	0.3	0.3	0.3	0.3
C_{g} (T_3) (fF)	–	0.3	0.3	0.3
C_{g} (T_4) (fF)	–	0.3	0.3	0.3

Table 3
Values of C_{eq} and C_{Deq}

	2-TFT	4-TFT	Current mirror	Current memory
C_{eq} (fF)	1.56	1.56	2.66	2.66
C_{Deq} (fF)	207.6	208.2	304.2	303.5

Considering a current of 40 μA to be delivered to the OLED (which represents a typical value to have high luminance level for an AMOLED display [7]), we are in a position to evaluate FR (or its inverse named T_{matrix}) from

Table 4
Comparison results

	2-TFT	4-TFT	Current mirror	Current memory
T_{matrix} (ns)	505.0 (1)	505.0 (1)	6802.7 (13.5)	6711.4 (13.3)
FR (MHz)	2.0	2.0	0.1	0.1
Dynamic power (nW)	0.2 (1)	0.2 (1)	0.3 (1.5)	0.3 (1.5)
Area (μm^2)	4 (1)	8 (2)	8 (2)	8 (2)

Eqs. (4)–(6), the dynamic power consumption from Eq. (7), and the area. The results obtained, that allow comparisons with a QVGA display ($m = 320$, $n = 240$), are presented in Table 4, where the normalized results with respect to the best values are reported in round brackets.

As expected, the circuit that shows the best performance in terms of speed, power consumption and area is the 2-TFT. However, as we discussed in Section 2, it is the most sensitive to mobility and threshold voltage variations, because it is not a compensated driver circuit. Therefore, among the compensated solutions, the 4-TFT topology seems the most attractive thanks to its better speed and power consumption performance (paid for in term of silicon area) compared with the current-driver circuits. Of course, unlike for the current mode topologies, this topology is still affected by uncompensated variation in mobility. Nevertheless, this variation is much lower than the one on the threshold voltage.

Finally, observing the last two columns of Table 4, it is worth noting the worst performances of the current-programming driver circuits in terms of T_{matrix} and, consequently, *FR* even in the case of high gray level (i.e., high value of current provided to the OLED). Indeed, considering low gray values, the time to settle pixel luminance significantly increases [11], further confirming the trend outlined in the table.

5. Simulation results

To validate the analysis developed above, simulations on driver circuits were performed by using AIM-SPICE 3.2 and the transistor model PSIA2 poly-Si TFT (LEVEL = 16), with a threshold voltage and surface mobility equal to 1.5 V and 100 $cm^2/V s$, respectively.

To verify whether the compensated topologies behaved correctly, the drain current variation of driving TFT with a threshold voltage shift, ΔV_t, equal to ± 0.5 V (a percentage shift of $\pm 33.3\%$) were analyzed. The results obtained are reported in Figs. 6–9 for 2-TFT, 4-TFT, current mirror and current memory driver circuits, respectively, and the corresponding error percentages are summarized in Table 5. It is apparent that 2-TFT suffers from drain current variation, while the compensated topologies have a negligible percentage variation, which is two orders of magnitude lower than that for 2-TFT circuits. It is worth noting the efficient compensation of the 4-TFT topology under the assumption of the same electrical properties of T_1 and T_3. Indeed, simulation results show that a voltage

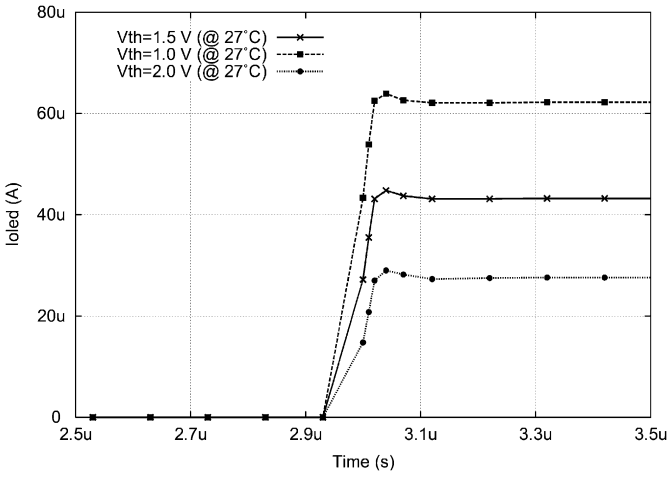

Fig. 6. Drain current shifts for the 2-TFT driver circuit at 27 °C.

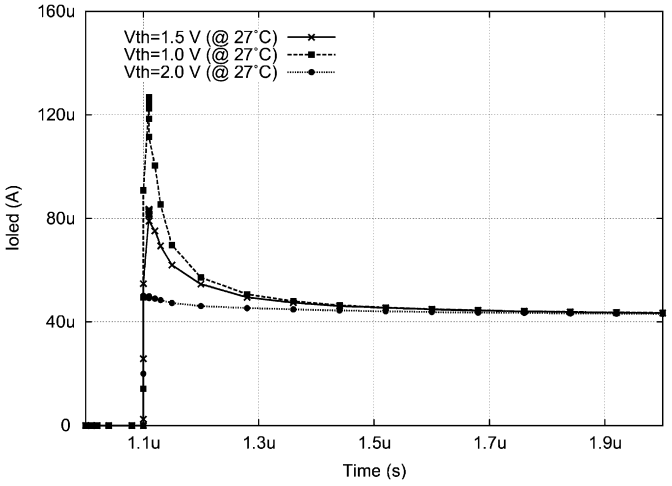

Fig. 7. Drain current shifts for the 4-TFT driver circuit at 27 °C.

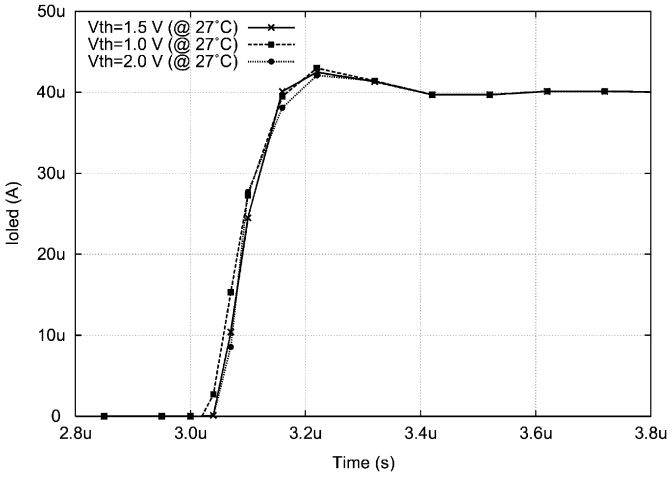

Fig. 8. Drain current shifts for the current mirror driver circuit at 27 °C.

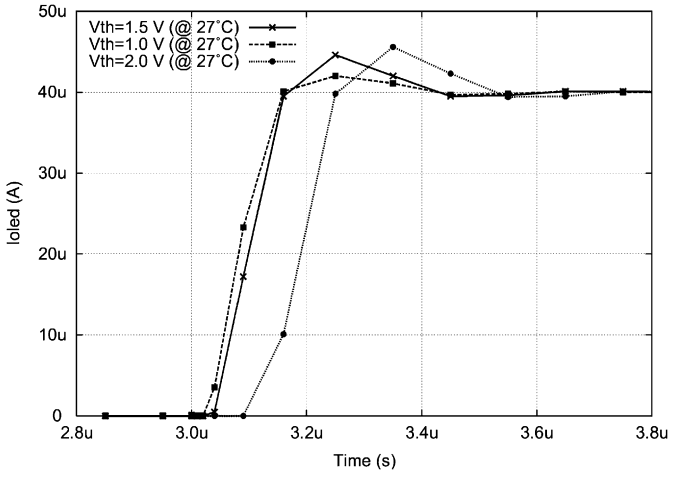

Fig. 9. Drain current shifts for current memory driver circuit at 27 °C.

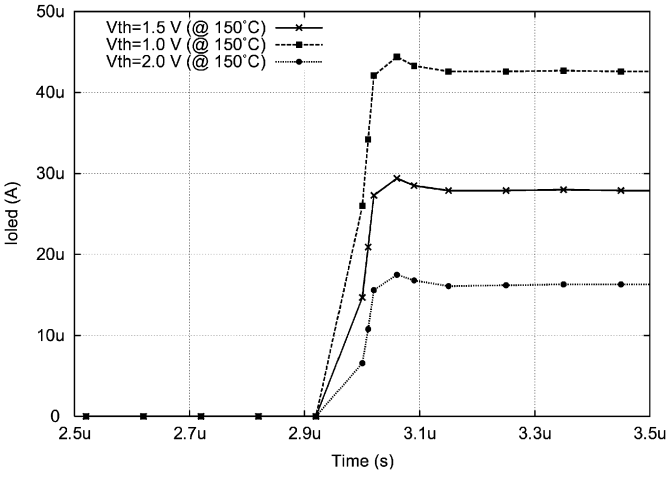

Fig. 10. Drain current shifts for the 2-TFT driver circuit at 150 °C.

Table 5
Percentage errors on drain current for a 33.3% V_t shift

	2-TFT	4-TFT	Current mirror	Current memory
$\Delta V_t = -33.3\%$	+44.1%	+0.7%	+0.3%	+0.01%
$\Delta V_t = +33.3\%$	−36.1%	−0.5%	−0.01%	−0.3%

Table 6
Comparisons between expected and simulated results of $t_{\text{line-pixel}}$

	2-TFT	4-TFT	Current mirror	Current memory
Expected (fs)	46.1 (1)	46.1 (1)	70.2 (1.5)	70.2 (1.5)
Simulated (fs)	50.2 (1)	53.5 (1.1)	82.0 (1.6)	78.4 (1.6)
Percentage error (%)	8.9	16.1	16.8	11.7

Table 7
Comparisons between expected and simulated results of $P_{\text{dyn-pixel}}$

	2-TFT	4-TFT	Current mirror	Current memory
Expected (pW)	199.9 (1)	201.9 (1.0)	296.1 (1.5)	293.4 (1.5)
Simulated (pW)	215.6 (1)	224.3 (1.0)	341.5 (1.6)	328.4 (1.5)
Percentage error (%)	7.9	10.0	15.3	11.9

shift of 33.3% between the two TFTs implies a proportional drain current shift.

Simulation results in regard to speed and dynamic power consumption for a single pixel were also gathered and are summarized in Tables 6 and 7, respectively. It is apparent that expected results agree with simulations, confirming the comparisons carried out in Section 4. An equivalent accuracy was found for the negligible t_{settle}.

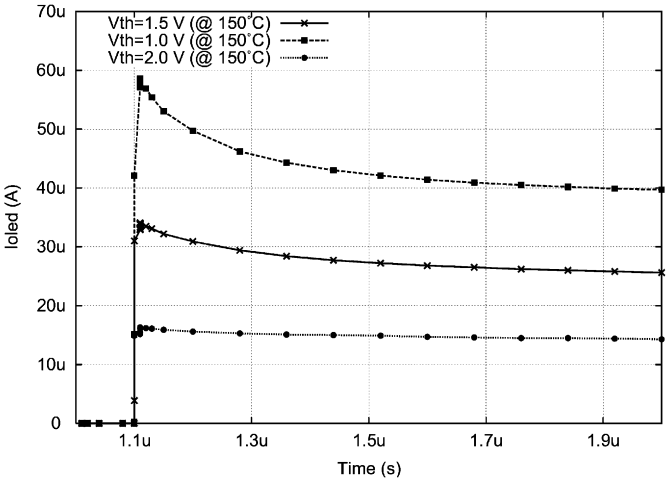

Fig. 11. Drain current shifts for the 4-TFT driver circuit at 150 °C.

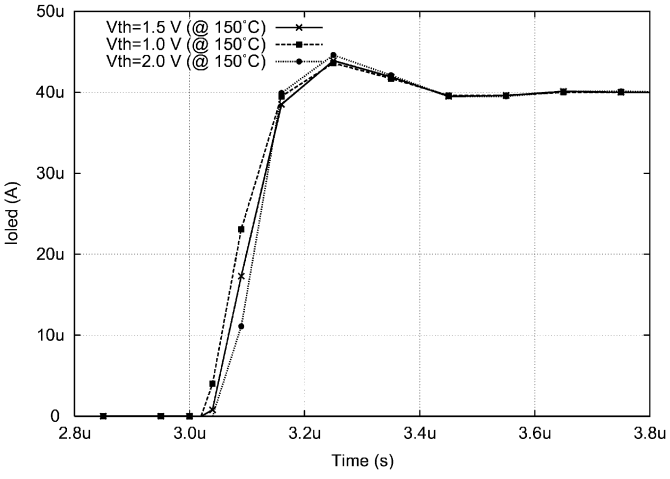

Fig. 12. Drain current shifts for the current mirror driver circuit at 150 °C.

It is worth noting that simulation data reported in Figs. 6–9 were obtained by setting the simulation temperature to 27 °C. Of course, threshold voltage shift

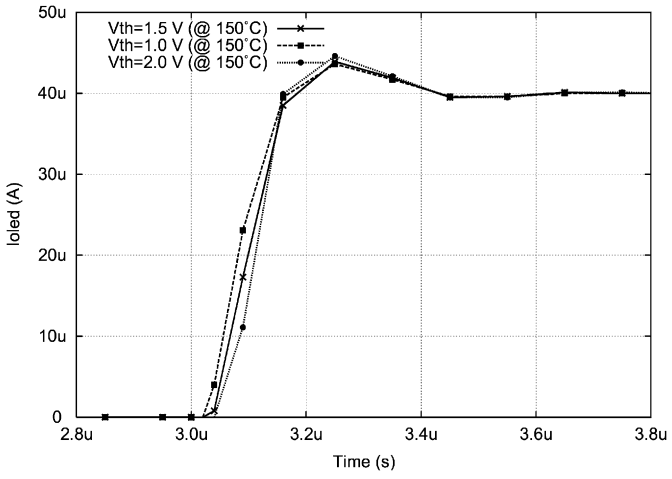

Fig. 13. Drain current shifts for the current memory driver circuit at 150 °C.

depends on device thermal conditions, which are ones of the main causes of TFT performance degradation [12]. Indeed, due to the high drain current levels delivered, the circuit is thermally stressed, and it was demonstrated that device temperature can grow up to 200 °C, with an increasing TFT threshold voltage. In order to evaluate how the compensating driver circuits respond to these thermal stresses, we also performed simulations at temperatures higher than 27 °C. The results are shown in Figs. 10–13, where transient waveforms are plotted for a simulation temperature equal to 150 °C. In this case, the uncompensated driver circuit (see Fig. 10) suffers not only from the random threshold voltage variation, but also from the positive voltage threshold shift, causing a percentage error in the current delivered to the OLED equal to 25% (a current equal to 30 μA is provided instead of the desired level of 40 μA). The case of the 4-TFT driver circuit is particularly interesting (see Fig. 11). Indeed, in this case the compensation scheme fails, since TFT T_1 and T_3, which would have the same threshold voltage, conduct different amount of currents (i.e., have different thermal stress), and thus suffer from unequal threshold voltage shifts. As a results, to the percentage error in the current delivered to the OLED equal to 25%, as in the previous case, a further current shift occurs whose error is about 40%. Finally, as shown by Figs. 12 and 13, the threshold voltage shift has no effect on the current delivered to the OLED by the current-programming driver circuits for the intrinsic nature of these topologies.

As a result of the analysis and comparisons developed through the paper, we can state that among the compensated topologies the best is the voltage driver 4-TFT whose speed performance is about 10 times higher than the current-driven topologies with a higher than 30% saving on power consumption. However, it has been shown that this compensation scheme suffers from performance degradation due to temperature variations (even if techniques can be exploited to reduce the increasing of device temperature when high drain current levels are of concern [12]). Moreover, the 4-TFT topology is uncompensated for mobility variation. Thus, if a 10% variation on the current delivered to the OLED is not acceptable, the topologies which promise the highest accuracy are the current-driver circuits.

6. Conclusions

In this paper, we have presented a review of AMOLED driver circuits, which can be divided into two groups, voltage- and current-programming driver circuits. Except for the 2-TFT topology (the simplest one), the others are able to compensate the threshold voltage variations. The comparison involved speed, power consumption and area, and was detailed for a QVGA display.

Among the compensated topologies the best is the voltage driver 4-TFT whose speed performance is about 10 times higher than the current-driven topologies with a higher than 30% saving on power consumption. However, if the 10% variation on the current drain due to the mobility variation is not acceptable, the topology to be used is the current-driver.

The analytical results for a single pixel were also evaluated in simulations through transistor-like simulator AIM-SPICE and found high agreement with the overall analytical results.

Appendix A

Time t_{settle} must be evaluated differently for voltage- and current-programming driver circuits [6]. In particular, for 2-TFT and 4-TFT driver circuits, it is given by $t_{settle} = 2.2 C_{Deq} R_{Deq}$, where R_{Deq} and C_{Deq} are the equivalent resistance of the data line and the charging and discharging equivalent capacitance at the gate of the driving TFT, respectively.

For current mirror and current memory driver circuits t_{settle} results as

$$t_{settle} = 0.8 \frac{C_{Deq} V_{data}}{I_{data}}, \tag{A.1}$$

where V_{data} and I_{data} are the voltage at the gate of the driving TFT and the current delivered to the OLED, respectively.

C_{Deq} can be evaluated by assuming the voltage on the select line is stationary when the data is being written on the pixel. Hence, the equivalent capacitance of the pixel in its OFF state is the sum of the gate–source overlap capacitance, C_{gs}, of the switching TFTs and the capacitance between the select line and the data line, $C_{data\text{-}select}$. Otherwise, when the pixel is ON, the total capacitance is the sum of the previously introduced contributions plus the gate–drain capacitance, C_{gd}, of the switching TFTs, the gate capacitance, C_g, and the gate–source capacitance, C_{gs} of the driving TFTs. Therefore, the relationships to evaluate C_{Deq} for 2-TFT, 4-TFT, current mirror and

current memory topologies are

$$C_{\mathrm{Deq}} = n(C_{\mathrm{data-select}} + C_{\mathrm{gs}T_2}) + C_{\mathrm{gd}T_2} + C_{\mathrm{gd}T_1} + C_{\mathrm{gs}T_1}, \tag{A.2}$$

$$C_{\mathrm{Deq}} = n(C_{\mathrm{data-select}} + C_{\mathrm{gs}T_2}) + C_{\mathrm{gd}T_2} + C_{\mathrm{gs}T_3} + C_{\mathrm{g}T_3} + C_{\mathrm{g}T_1} + C_{\mathrm{gs}T_1}, \tag{A.3}$$

$$C_{\mathrm{Deq}} = n(C_{\mathrm{data-select}} + C_{\mathrm{gs}T_3} + C_{\mathrm{gs}T_4}) + C_{\mathrm{gd}T_4} + C_{\mathrm{gs}T_2} + C_{\mathrm{g}T_2} + C_{\mathrm{g}T_1} + C_{\mathrm{gs}T_1}, \tag{A.4}$$

$$C_{\mathrm{Deq}} = n(C_{\mathrm{data-select}} + C_{\mathrm{gs}T_3} + C_{\mathrm{gs}T_4}) + C_{\mathrm{gd}T_4} + C_{\mathrm{g}T_1} + C_{\mathrm{gs}T_1}, \tag{A.5}$$

respectively.

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