

Logic Design Lab Report: Week 7

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1. Introduction

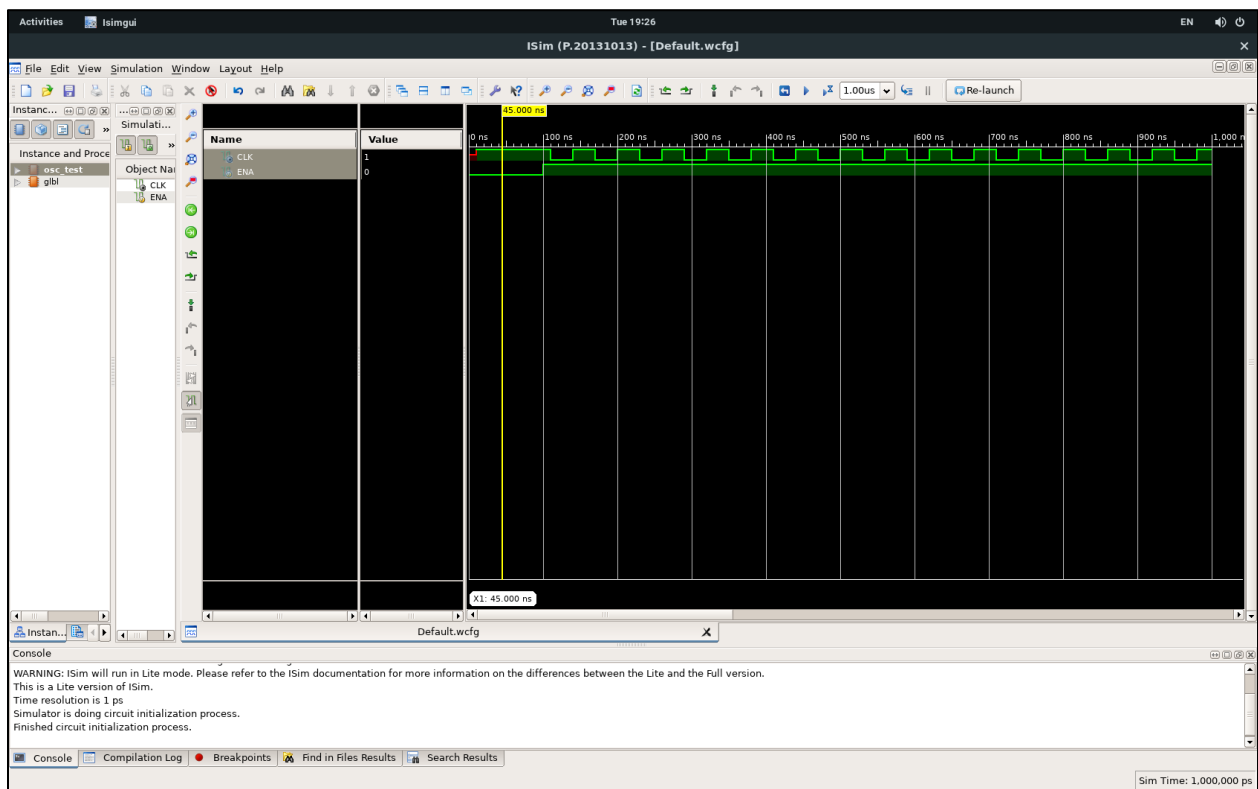
이번 lab 에서는 oscillator, RS latch, gated RS latch, master-slave latches 를 verilog 로 implement 한 다음 그것들의 behavior 를 simulate 했다. 또한 JK flip-flop 과 D lip-flop 을 verilog 로 implement 한 다음 그것들의 behavior 를 simulate 했다.

2. Implementation

verilog 를 통하여 구현한다.

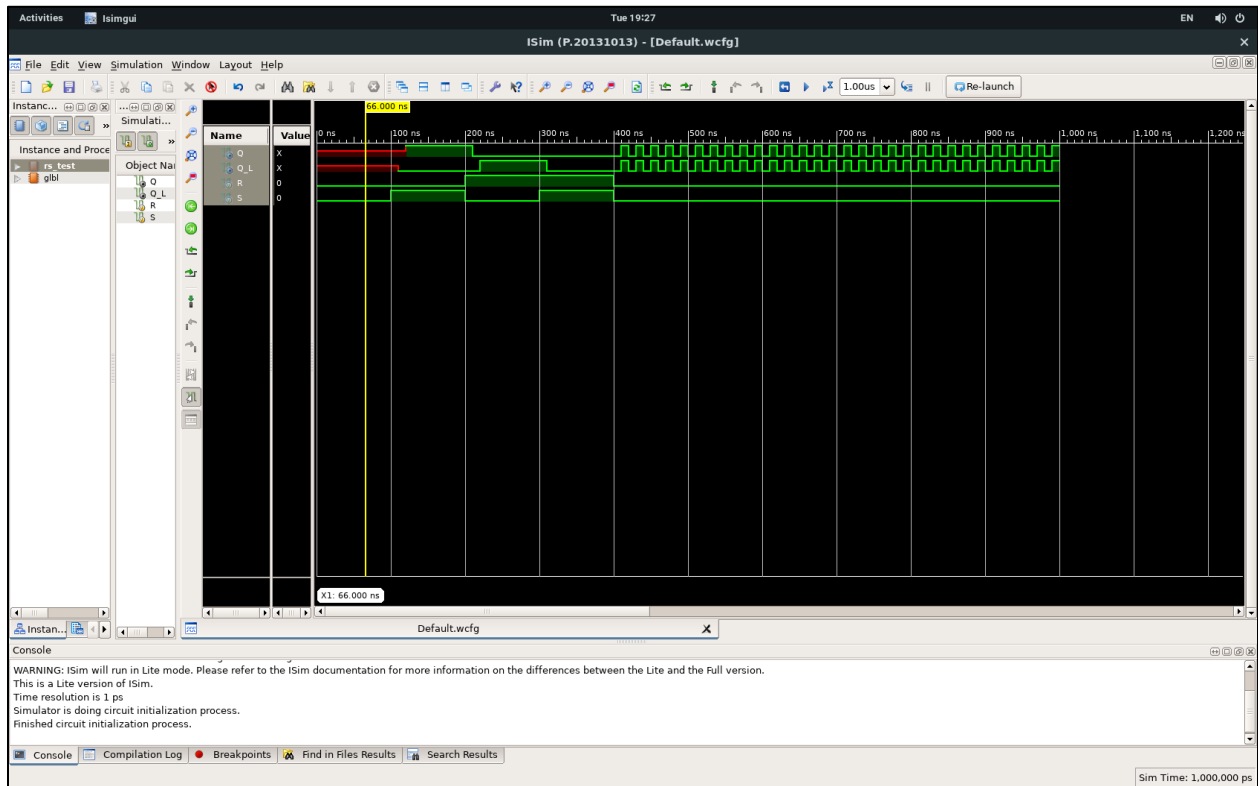
3. Result

-Oscillator



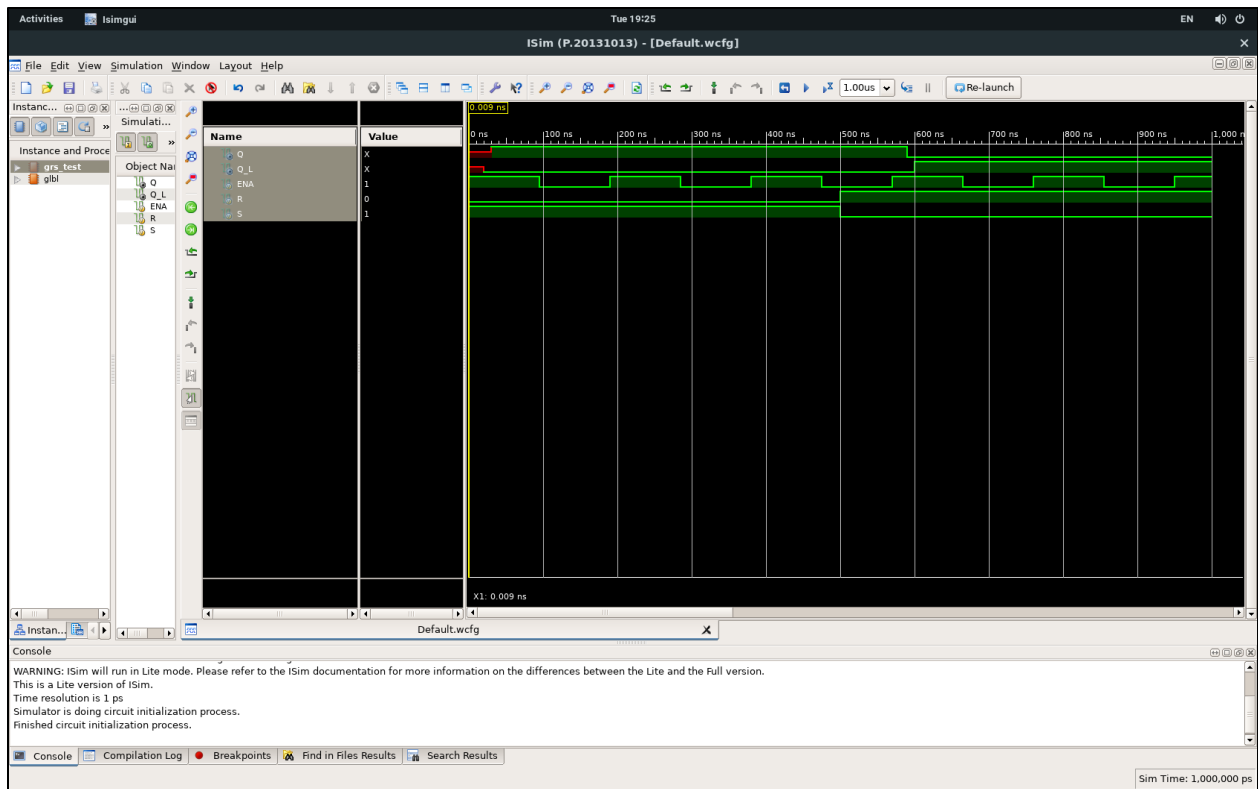
Clock(CLK)를 통해 gate delay 를 주어 일정 시간의 주기를 갖도록 구현했다.

-RS latch



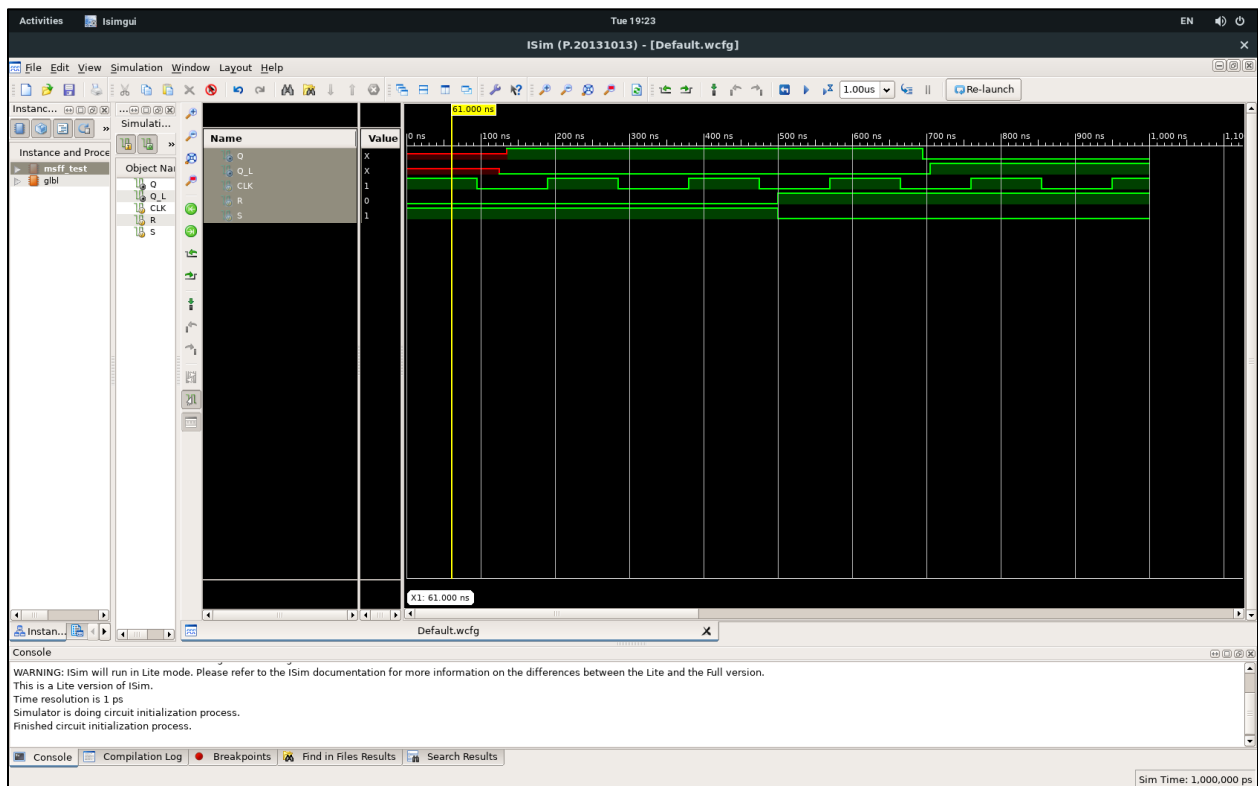
S, R 의 값에 따라 Q 가 변화하도록 구현했다. (왜 처음 밸류 빨간색인지 물어보기)

-Gated RS latch



R-S latch 가 불안정한 것을 보완하기 위해 gate 를 추가하였다.

-Master-slave latches

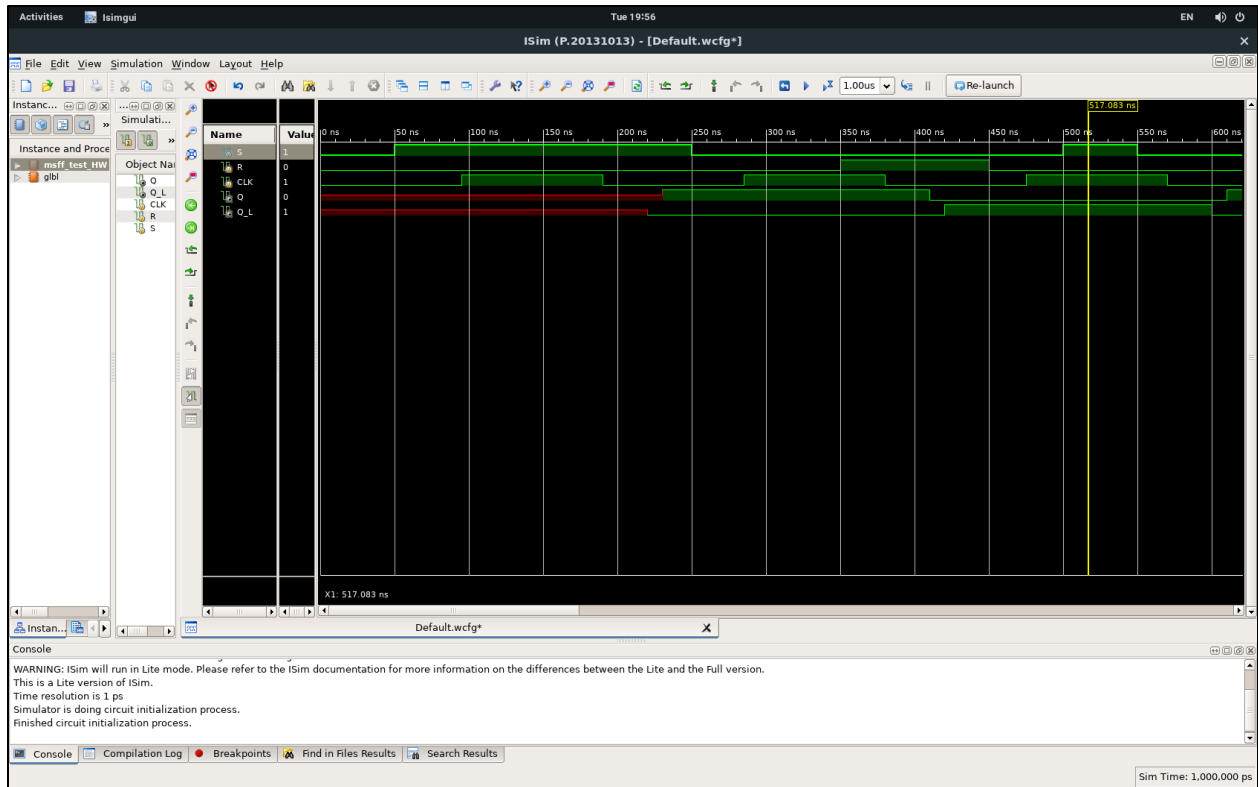


master stage 와 slave stage 로 나뉘어 있는 latches 를 구현하였다. 의도치 않은 노이즈 신호가 그대로 전달되는 현상인 race 현상을 해결할 수 있다.

-Master-slave latches 1s catching problem

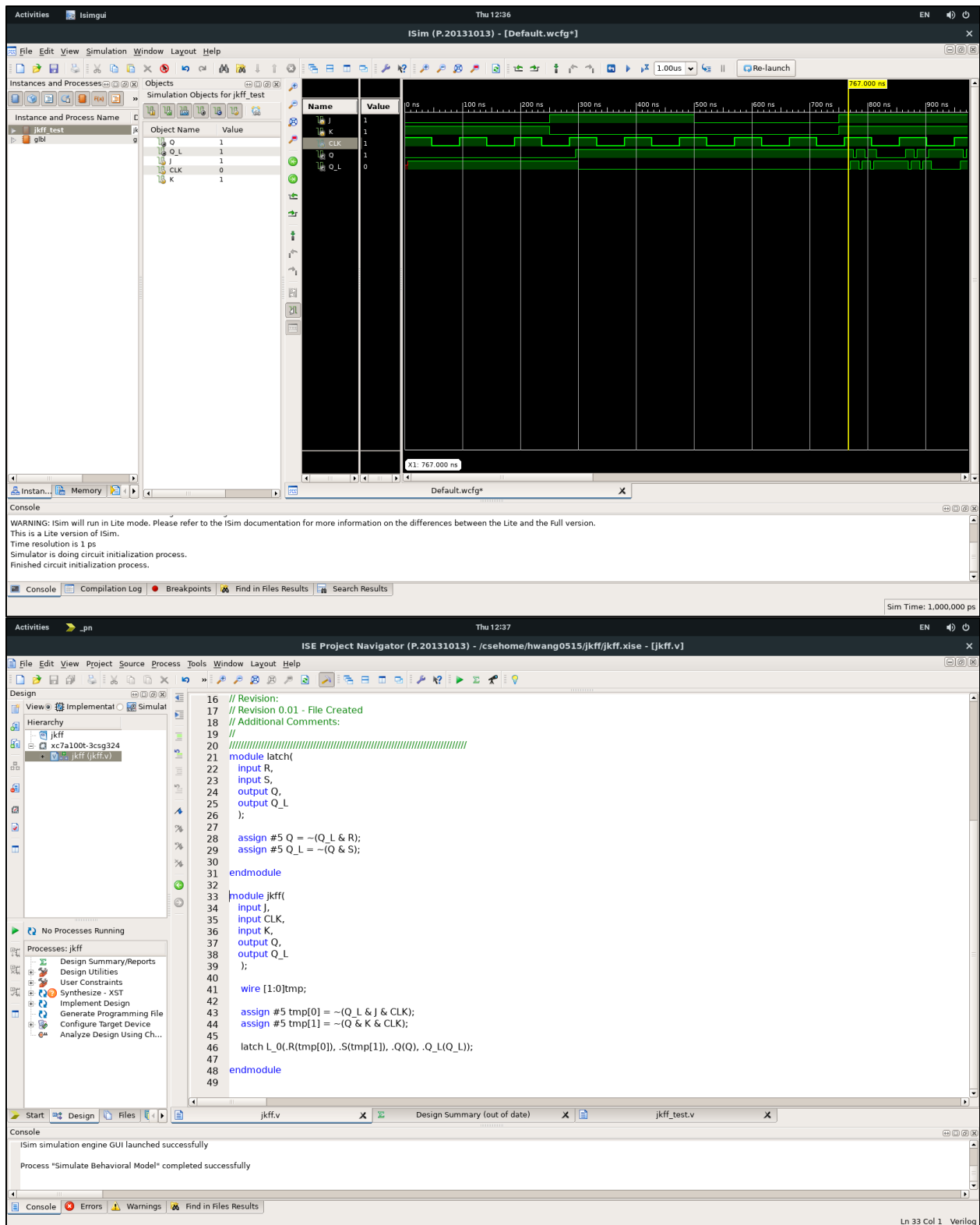
The screenshot displays the ISim (P.20131013) - [Default.wcfg] simulation window. The main area shows a timing diagram with signals S, R, CLK, O, and O_L. A yellow vertical line marks a point at 82.000 ns. The console at the bottom shows a warning: "WARNING: ISim will run in Lite mode. Please refer to the ISim documentation for more information on the differences between the Lite and the Full version. This is a Lite version of ISim. Time resolution is 1 ps. Simulator is doing circuit initialization process. Finished circuit initialization process." The simulation time is 1,000,000 ps.

On the right, a presentation slide titled "Master-Slave structure & The 1s catching Problem" is shown. The slide includes a circuit diagram of a master-slave latch structure. The master stage has inputs R, S, and CLK, and outputs P and Q. The slave stage has inputs R, S, and CLK, and outputs P and Q. The slide also shows a timing diagram for the 1s catching problem, with signals S, R, CLK, P, Q, and Q. The timing diagram shows a race condition where the master output P and Q change before the slave output P and Q, leading to a 1s catching problem.



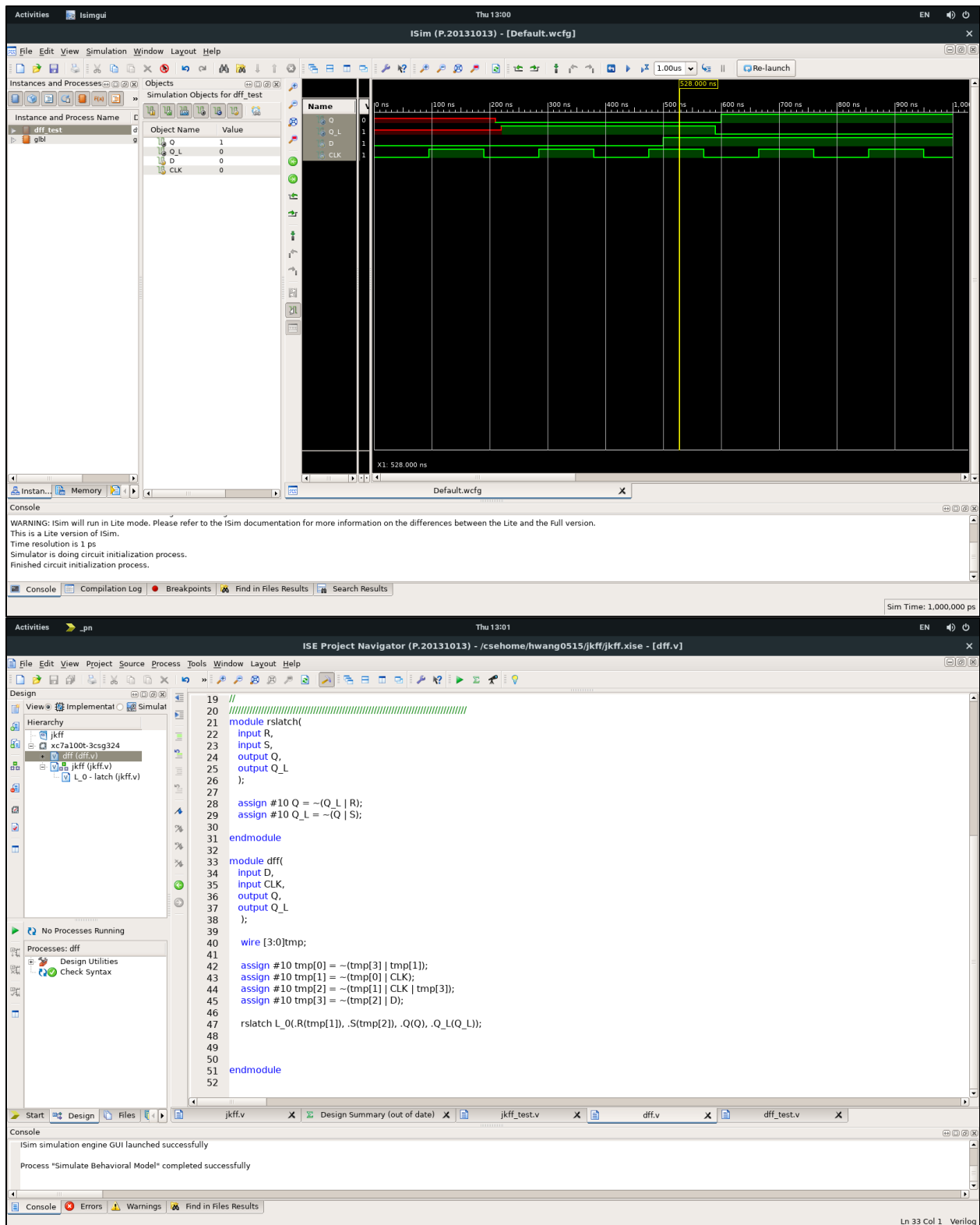
Hold 기능 때문에 생기는 문제다. $R = S = 0$ 이었다가 순간적으로 S 가 1 로 glitch 를 일으켰다.

-JK flip-flop



Master-Slave f/f 에서 master stage 와 slave stage 에 각각 gated 한 JK f/f 를 구현했다.

-D flip-flop(negative edge-triggered)



RS f/f 에서 R 대신 D', S 대신 D 가 입력으로 주어진다.

4. Conclusion / Discussion

Sequential logic element 들을 직접 verilog 로 구현하여 이해하였다.