Logic Design Lab Report: Week 4

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1. Introduction

이번 시간에는 verilog를 이용해 직접 논리 회로를 설계하는 방법에 대해 배웠다. 직접 코딩한 4-to-1 Multiplexer를 가지고 16-to-1 Multiplexer를 설계해 보았다.

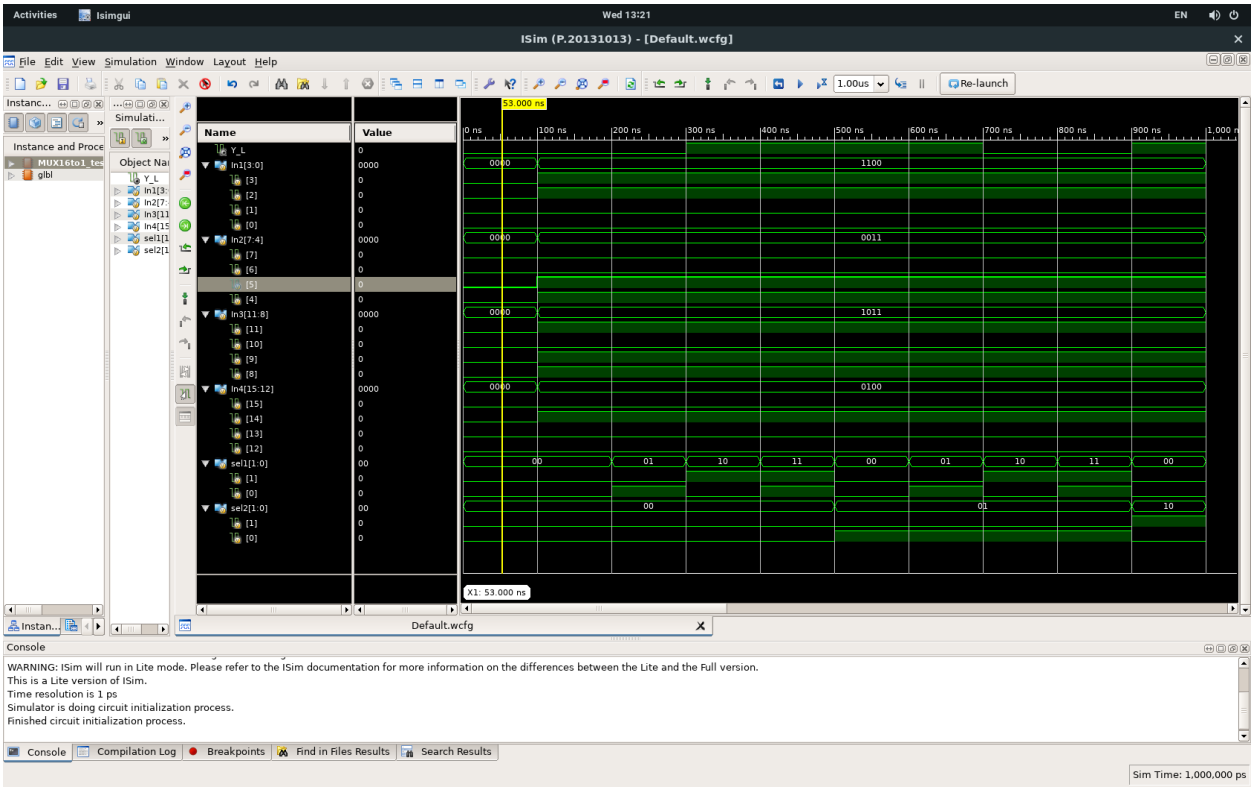
2. Implementation

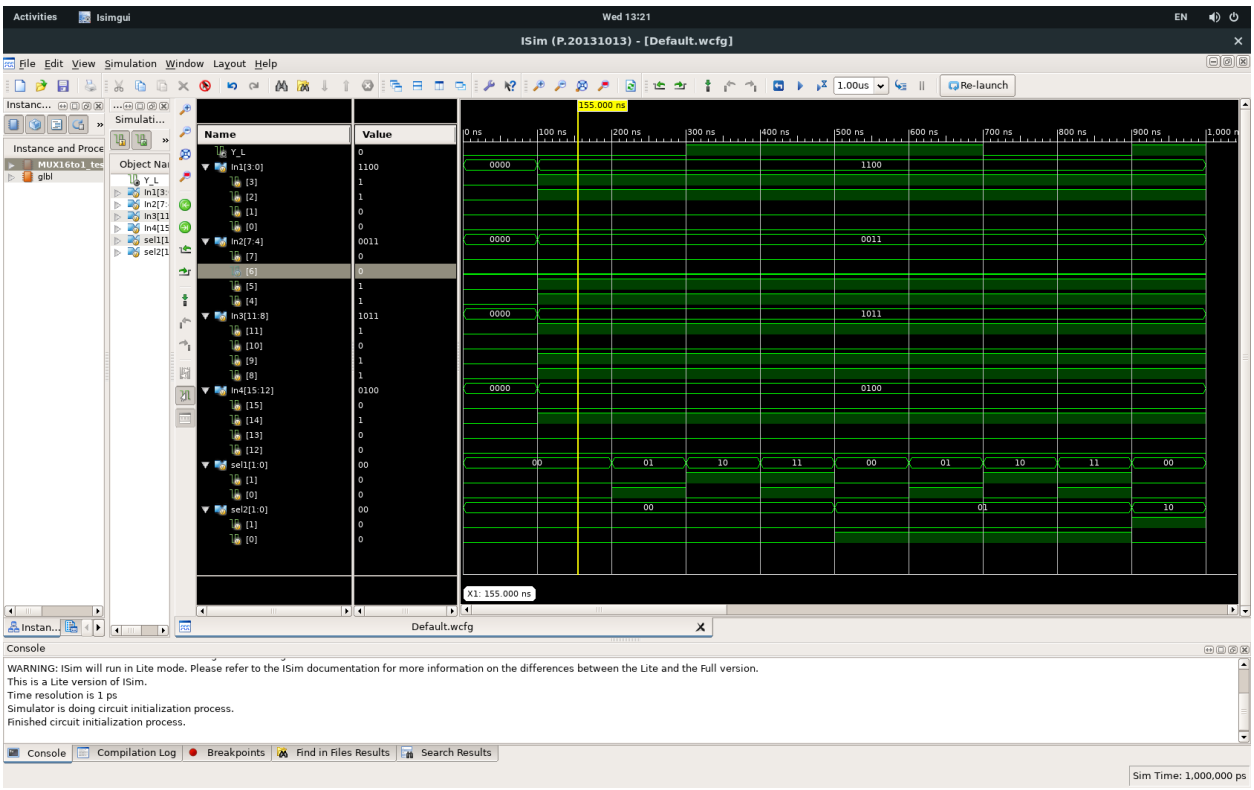
Verilog의 문법에 따라 4-to-1 Multiplexer 코드, 16-to-1 Multiplexer 코드, 16-to-1 Multiplexer testbench 코드를 작성했다. 코드를 실행한 후 나오는 결과에서 selection line의 값에 해당하는 input line의 값이 output과 같은 지 비교하였다.

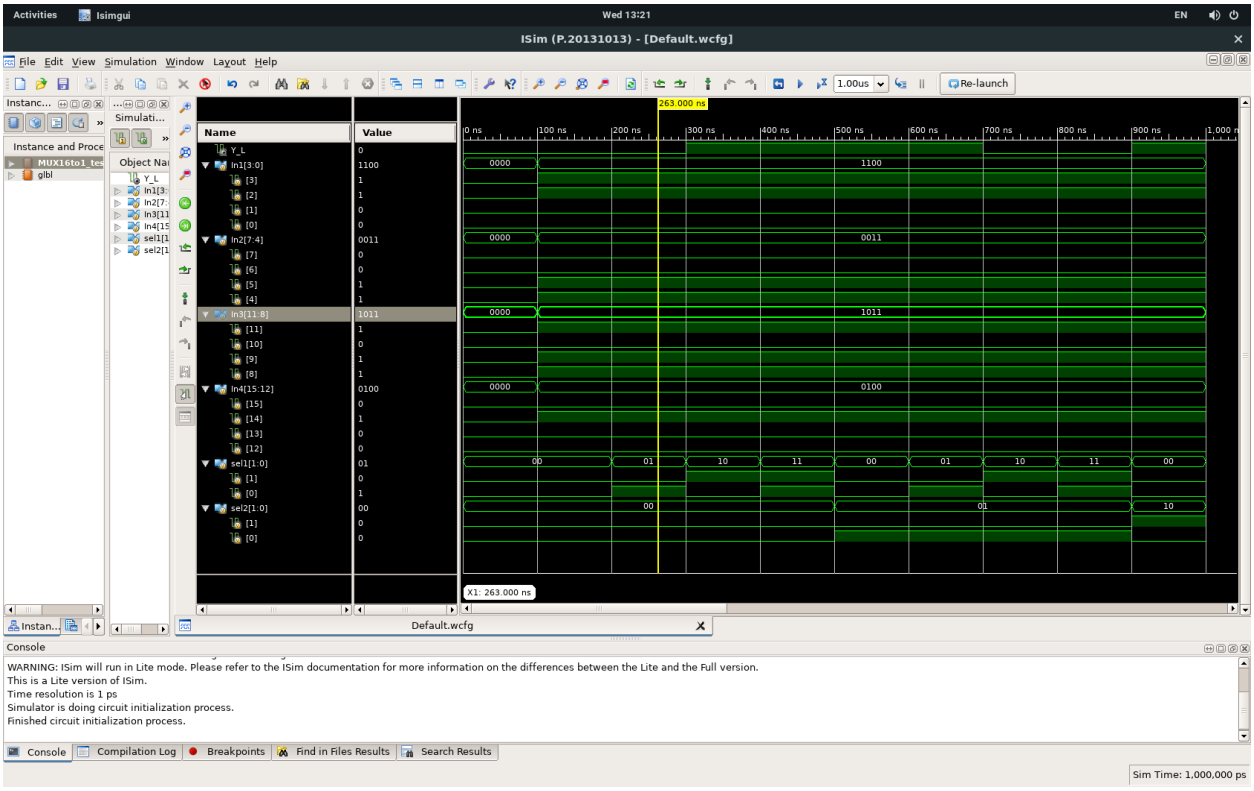
3. Result

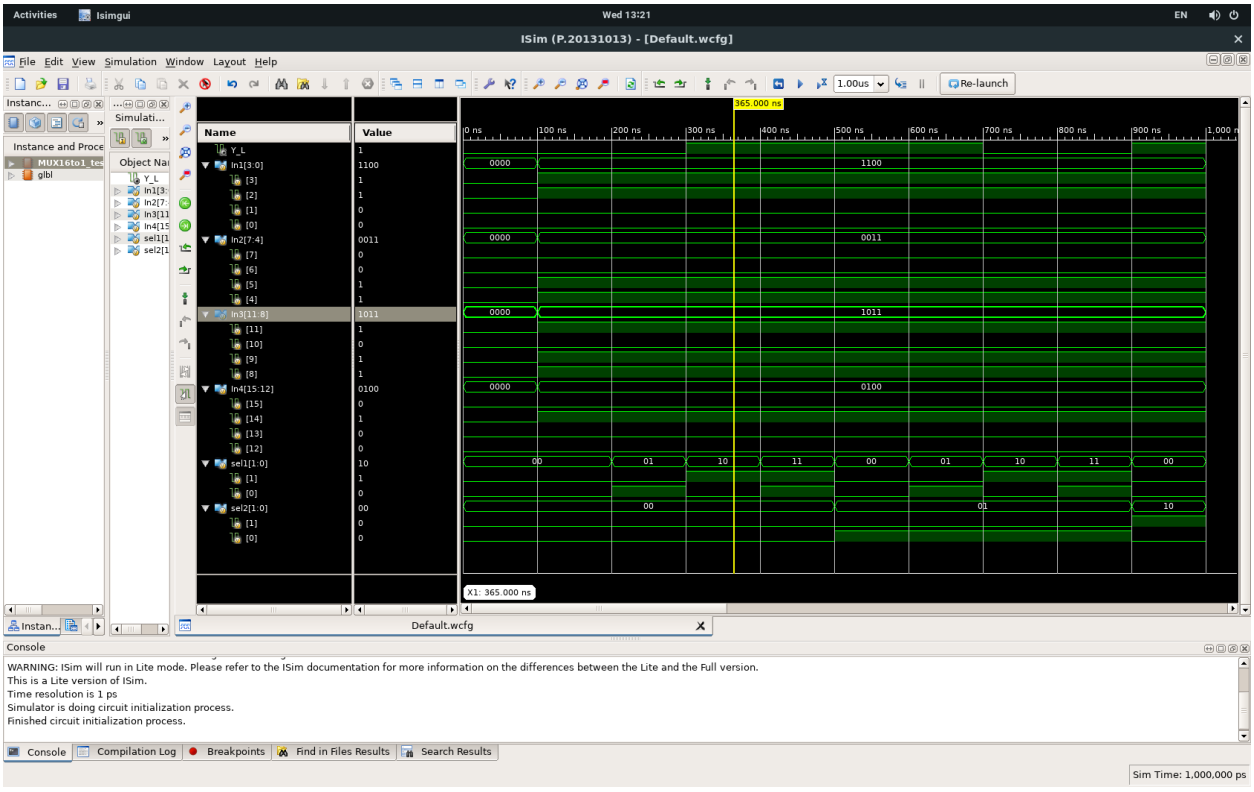
4-to-1 Multiplexer 코드 파일, 16-to-1 Multiplexer 코드 파일, 16-to-1 Multiplexer testbench 코드 파일은 압축하여 리포트와 함께 제출하였다.

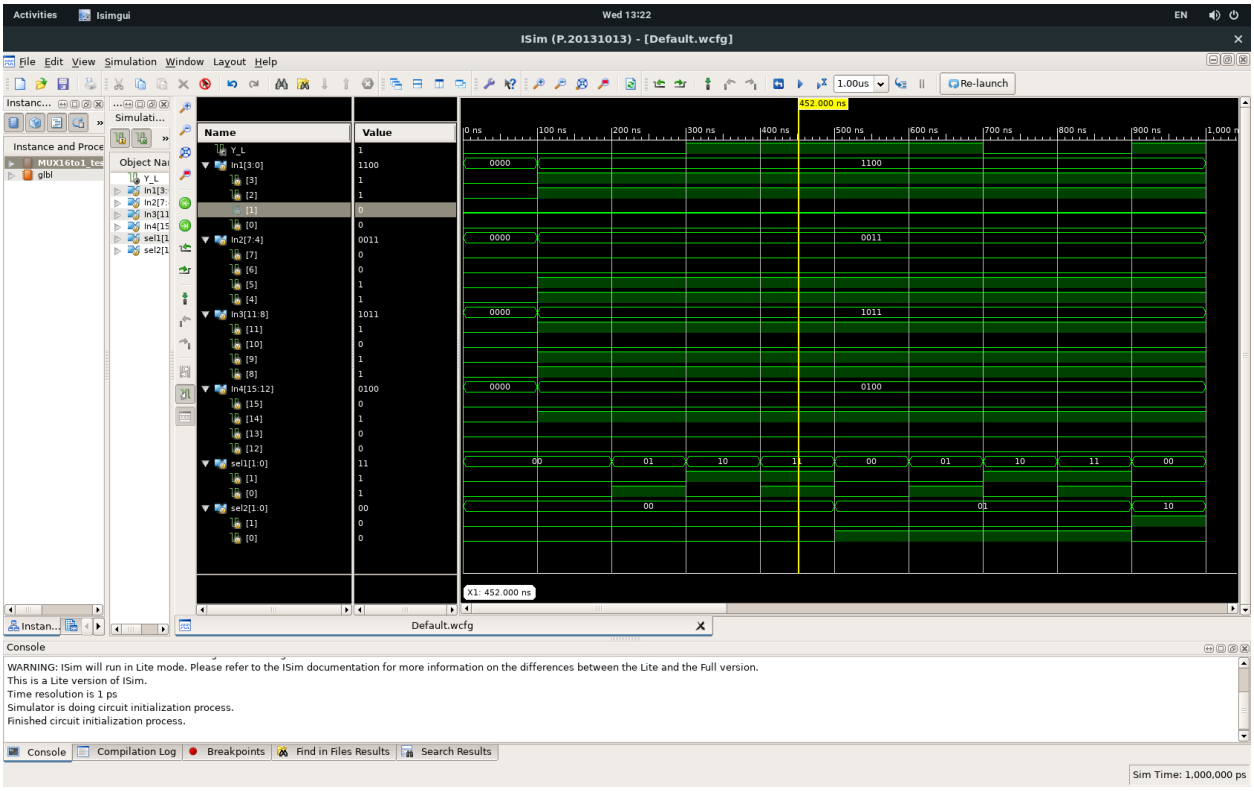
//1st case fixed input 16'b1100001110110100

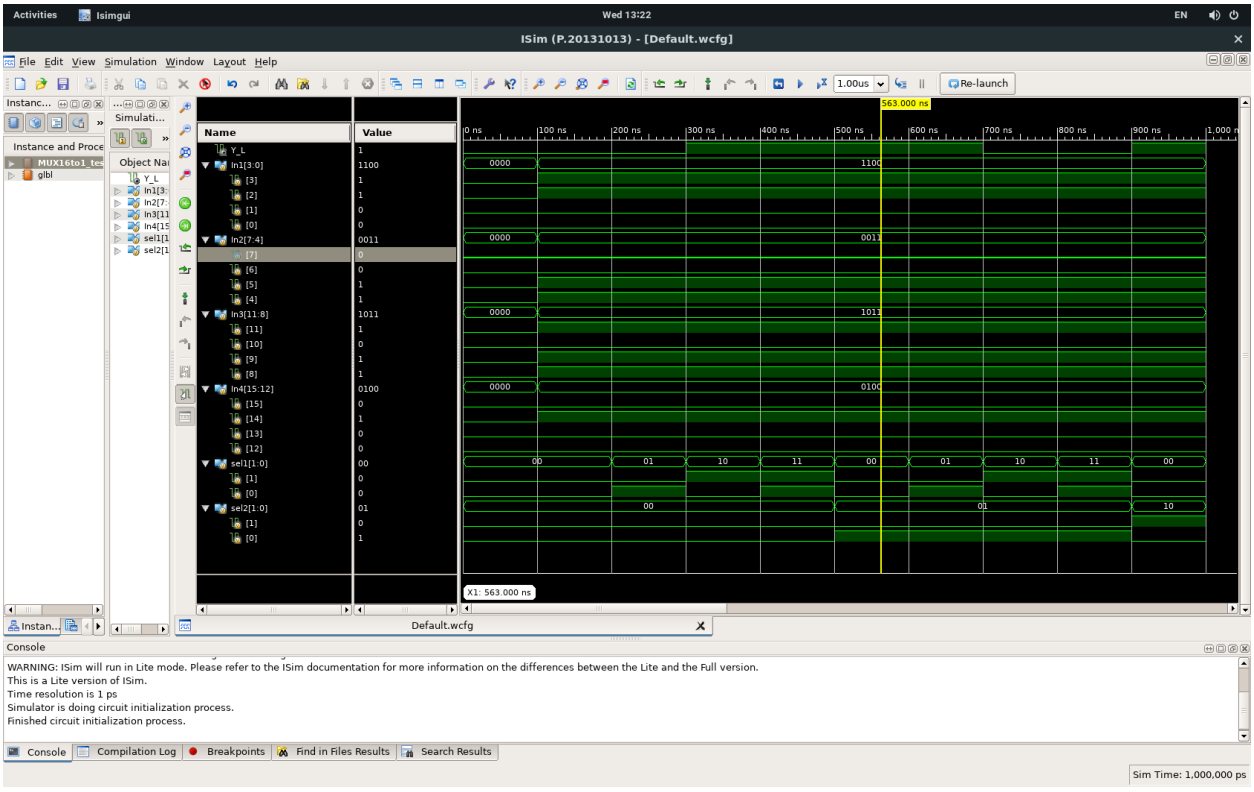


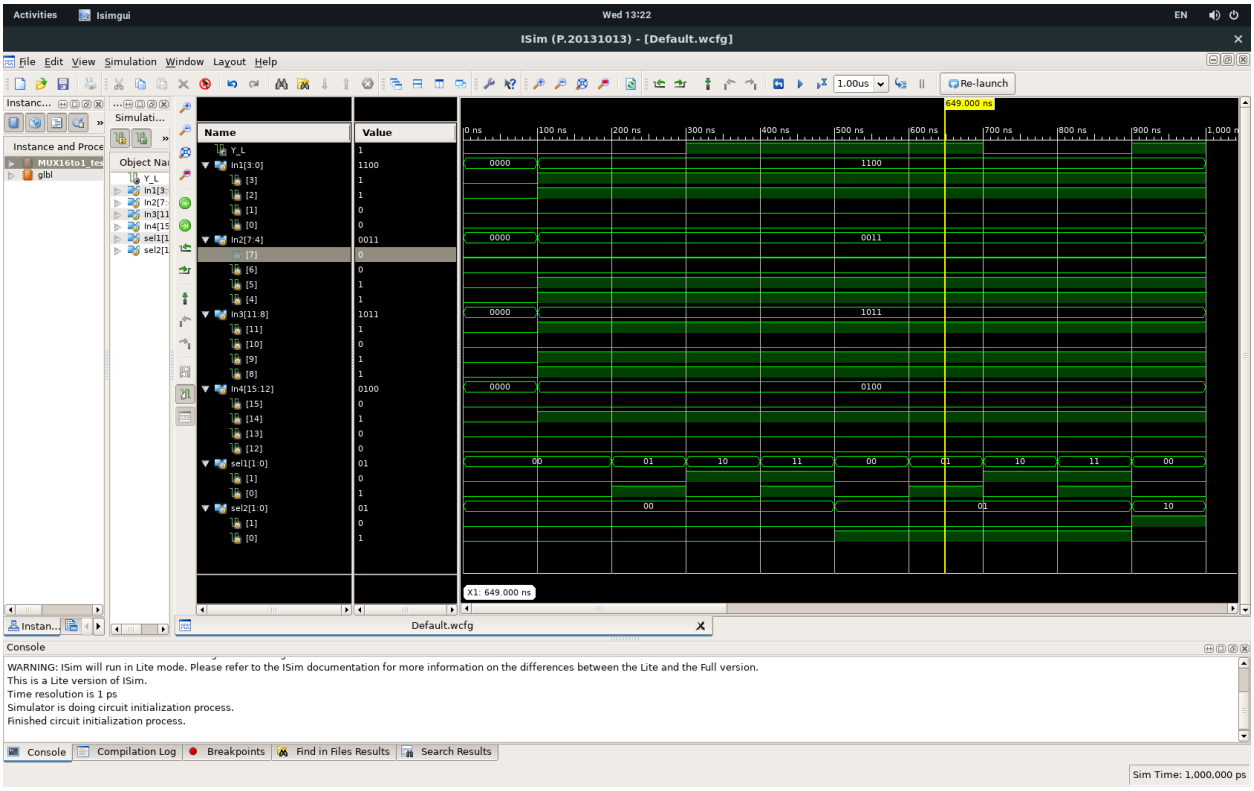


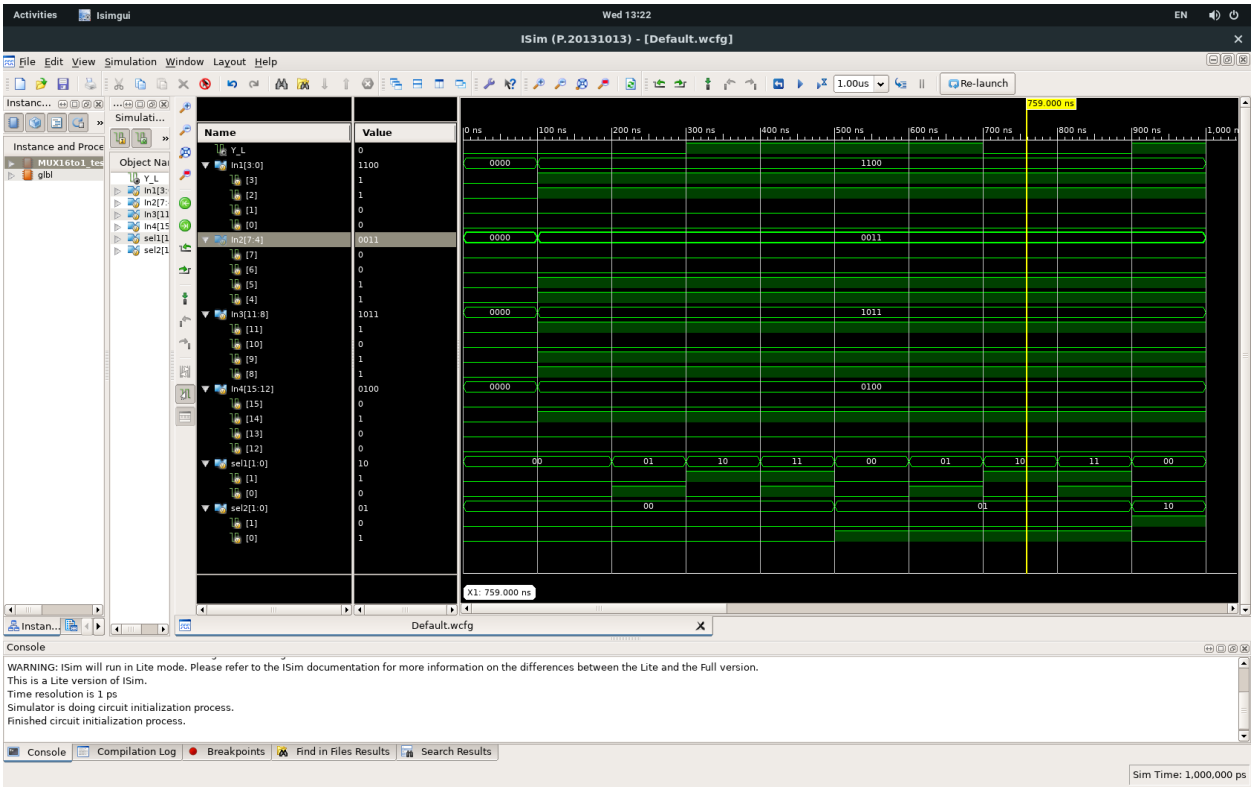

Activities
Isimgui
Wed 13:21
EN
ISim (P.20131013) - [Default.wcfg]
File Edit View Simulation Window Layout Help
Re-launch
Name
Value
263.000 ns
X1: 263.000 ns
Default.wcfg
Console
WARNING: ISim will run in Lite mode. Please refer to the ISim documentation for more information on the differences between the Lite and the Full version.
This is a Lite version of ISim.
Time resolution is 1 ps
Simulator is doing circuit initialization process.
Finished circuit initialization process.
Console
Compilation Log
Breakpoints
Find in Files Results
Search Results
Sim Time: 1,000,000 ps

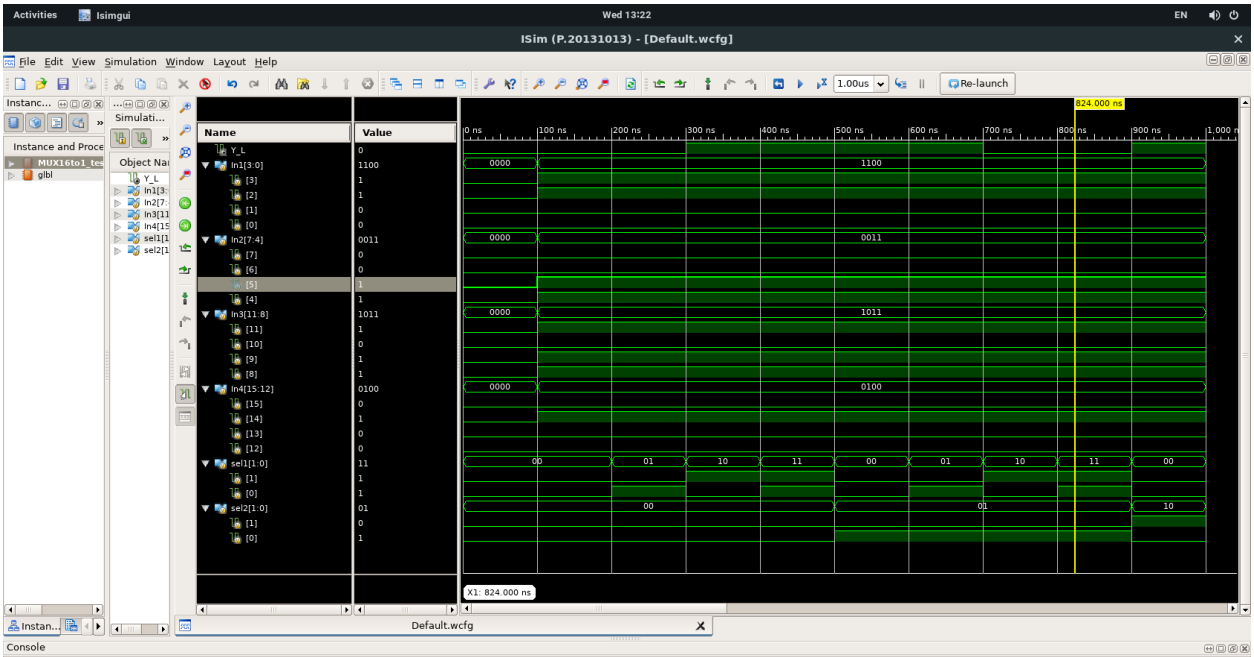

Activities
Isimgui
Wed 13:21
EN
ISim (P.20131013) - [Default.wcfg]
File Edit View Simulation Window Layout Help
Re-launch
Name
Value
365.000 ns
X1: 365.000 ns
Default.wcfg
Console
WARNING: ISim will run in Lite mode. Please refer to the ISim documentation for more information on the differences between the Lite and the Full version.
This is a Lite version of ISim.
Time resolution is 1 ps
Simulator is doing circuit initialization process.
Finished circuit initialization process.
Console
Compilation Log
Breakpoints
Find in Files Results
Search Results
Sim Time: 1,000,000 ps

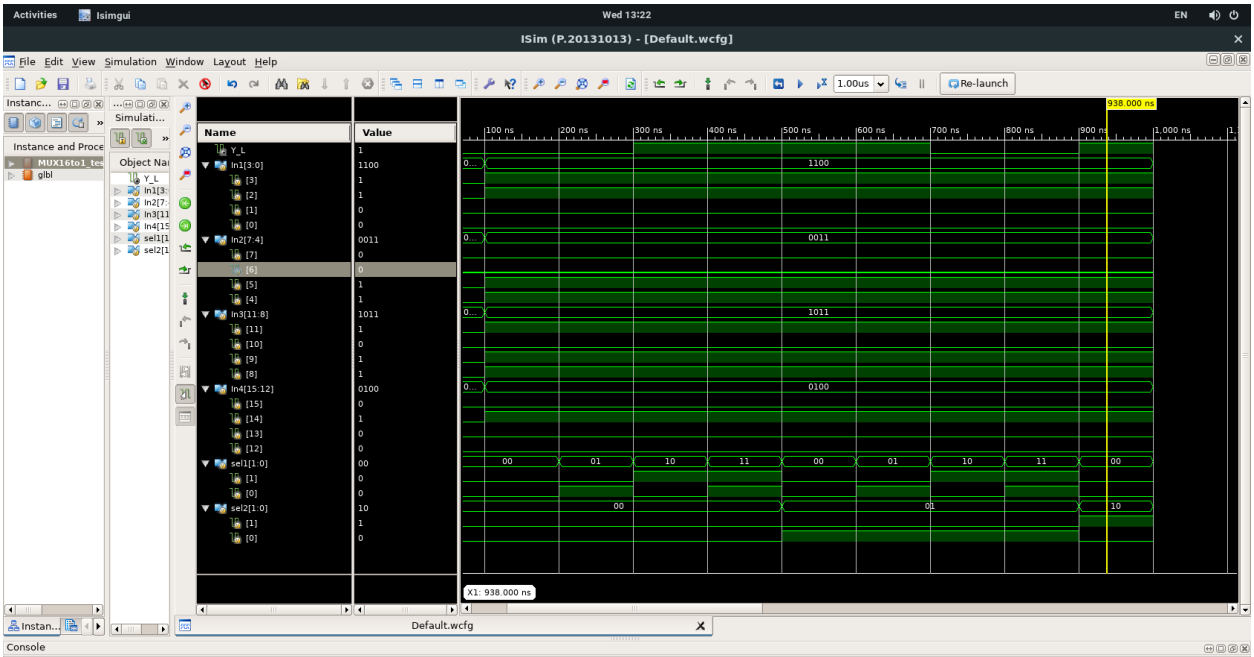

Activities
Isimgui
Wed 13:22
EN
ISim (P.20131013) - [Default.wcfg]
File Edit View Simulation Window Layout Help
Re-launch
1.00us
452.000 ns
Name
Value
Y_L
In1[3:0]
In2[7:4]
In3[11:8]
In4[15:12]
sel1[1:0]
sel2[1:0]
X1: 452.000 ns
Default.wcfg
Console
WARNING: ISim will run in Lite mode. Please refer to the ISim documentation for more information on the differences between the Lite and the Full version.
This is a Lite version of ISim.
Time resolution is 1 ps
Simulator is doing circuit initialization process.
Finished circuit initialization process.
Console
Compilation Log
Breakpoints
Find in Files Results
Search Results
Sim Time: 1,000,000 ps


Activities
Isimgui
Wed 13:22
EN
ISim (P.20131013) - [Default.wcfg]
File Edit View Simulation Window Layout Help
Re-launch
1.00us
563.000 ns
Name
Value
Y_L
In1[3:0]
In2[7:4]
In3[11:8]
In4[15:12]
sel1[1:0]
sel2[1:0]
X1: 563.000 ns
Default.wcfg
Console
WARNING: ISim will run in Lite mode. Please refer to the ISim documentation for more information on the differences between the Lite and the Full version.
This is a Lite version of ISim.
Time resolution is 1 ps
Simulator is doing circuit initialization process.
Finished circuit initialization process.
Console
Compilation Log
Breakpoints
Find in Files Results
Search Results
Sim Time: 1,000,000 ps

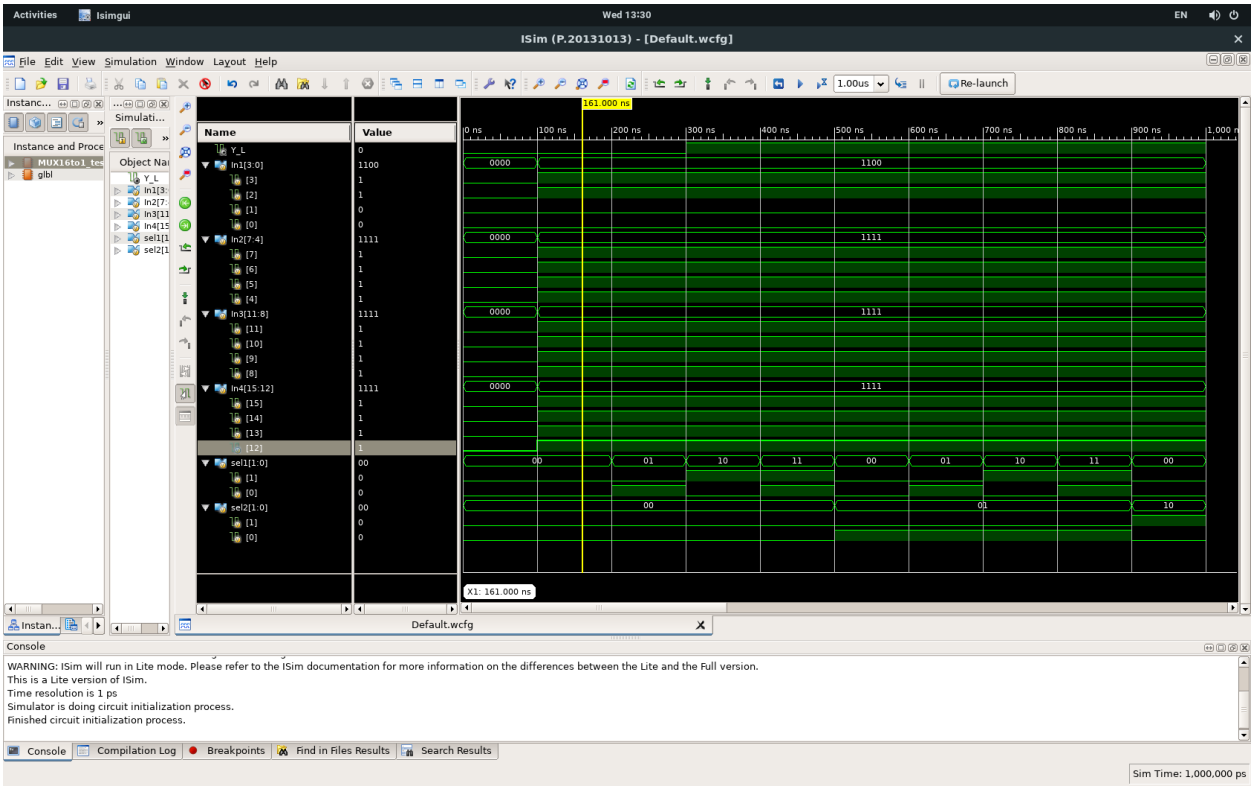

Activities
Isimgui
Wed 13:22
EN
ISim (P.20131013) - [Default.wcfg]
File Edit View Simulation Window Layout Help
1.00us
Re-launch
649.000 ns
Name
Value
Y_L 1
In1[3:0] 1100
[3] 1
[2] 1
[1] 0
[0] 0
In2[7:4] 0011
[7] 0
[6] 0
[5] 1
[4] 1
In3[11:8] 1011
[11] 1
[10] 0
[9] 1
[8] 1
In4[15:12] 0100
[15] 0
[14] 1
[13] 0
[12] 0
sel1[1:0] 01
[1] 0
[0] 1
sel2[1:0] 01
[1] 0
[0] 1
0 ns
100 ns
200 ns
300 ns
400 ns
500 ns
600 ns
700 ns
800 ns
900 ns
0000
1100
0011
1011
0100
00
01
10
11
X1: 649.000 ns
Default.wcfg
Console
WARNING: ISim will run in Lite mode. Please refer to the ISim documentation for more information on the differences between the Lite and the Full version.
This is a Lite version of ISim.
Time resolution is 1 ps
Simulator is doing circuit initialization process.
Finished circuit initialization process.
Console
Compilation Log
Breakpoints
Find in Files Results
Search Results
Sim Time: 1,000,000 ps

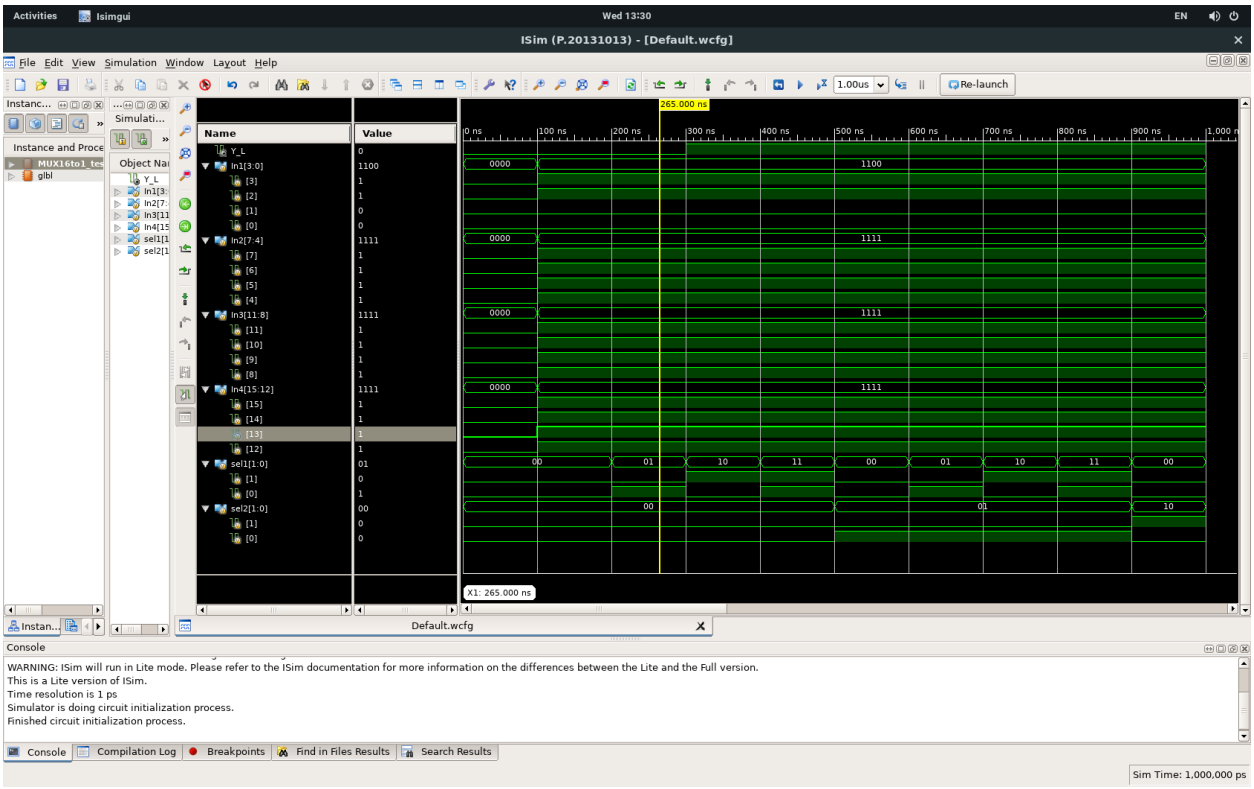

Activities
Isimgui
Wed 13:22
EN
ISim (P.20131013) - [Default.wcfg]
File Edit View Simulation Window Layout Help
1.00us
Re-launch
759.000 ns
Name
Value
Y_L 0
In1[3:0] 1100
[3] 1
[2] 1
[1] 0
[0] 0
In2[7:4] 0011
[7] 0
[6] 0
[5] 1
[4] 1
In3[11:8] 1011
[11] 1
[10] 0
[9] 1
[8] 1
In4[15:12] 0100
[15] 0
[14] 1
[13] 0
[12] 0
sel1[1:0] 10
[1] 1
[0] 0
sel2[1:0] 01
[1] 0
[0] 1
0 ns
100 ns
200 ns
300 ns
400 ns
500 ns
600 ns
700 ns
800 ns
900 ns
0000
1100
0011
1011
0100
00
01
10
11
X1: 759.000 ns
Default.wcfg
Console
WARNING: ISim will run in Lite mode. Please refer to the ISim documentation for more information on the differences between the Lite and the Full version.
This is a Lite version of ISim.
Time resolution is 1 ps
Simulator is doing circuit initialization process.
Finished circuit initialization process.
Console
Compilation Log
Breakpoints
Find in Files Results
Search Results
Sim Time: 1,000,000 ps

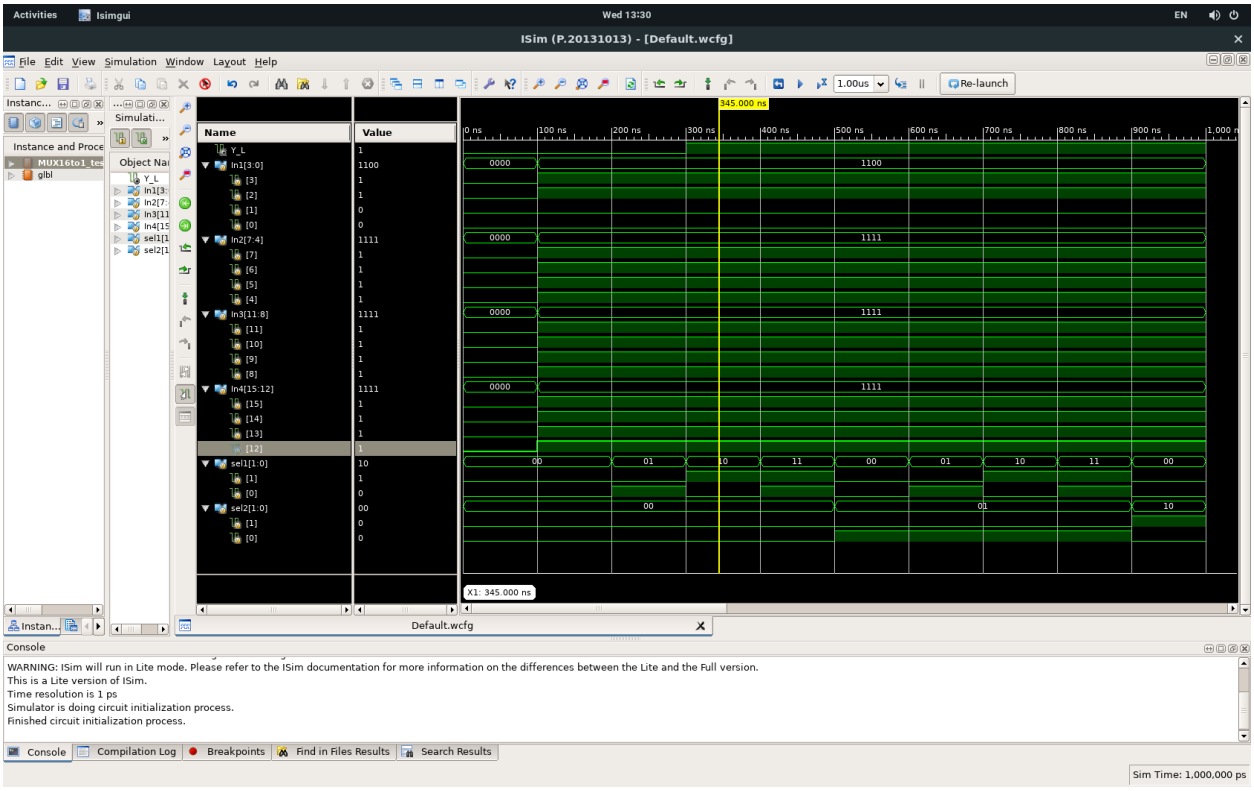

Activities
Isimgui
Wed 13:22
EN
ISim (P.20131013) - [Default.wcfg]
File Edit View Simulation Window Layout Help
Re-launch
Name
Value
Y_L
In1[3:0]
In2[7:4]
In3[11:8]
In4[15:12]
sel1[1:0]
sel2[1:0]
824.000 ns
X1: 824.000 ns
Default.wcfg
Console
WARNING: ISim will run in Lite mode. Please refer to the ISim documentation for more information on the differences between the Lite and the Full version.
This is a Lite version of ISim.
Time resolution is 1 ps
Simulator is doing circuit initialization process.
Finished circuit initialization process.
Console
Compilation Log
Breakpoints
Find in Files Results
Search Results
Sim Time: 1,000,000 ps

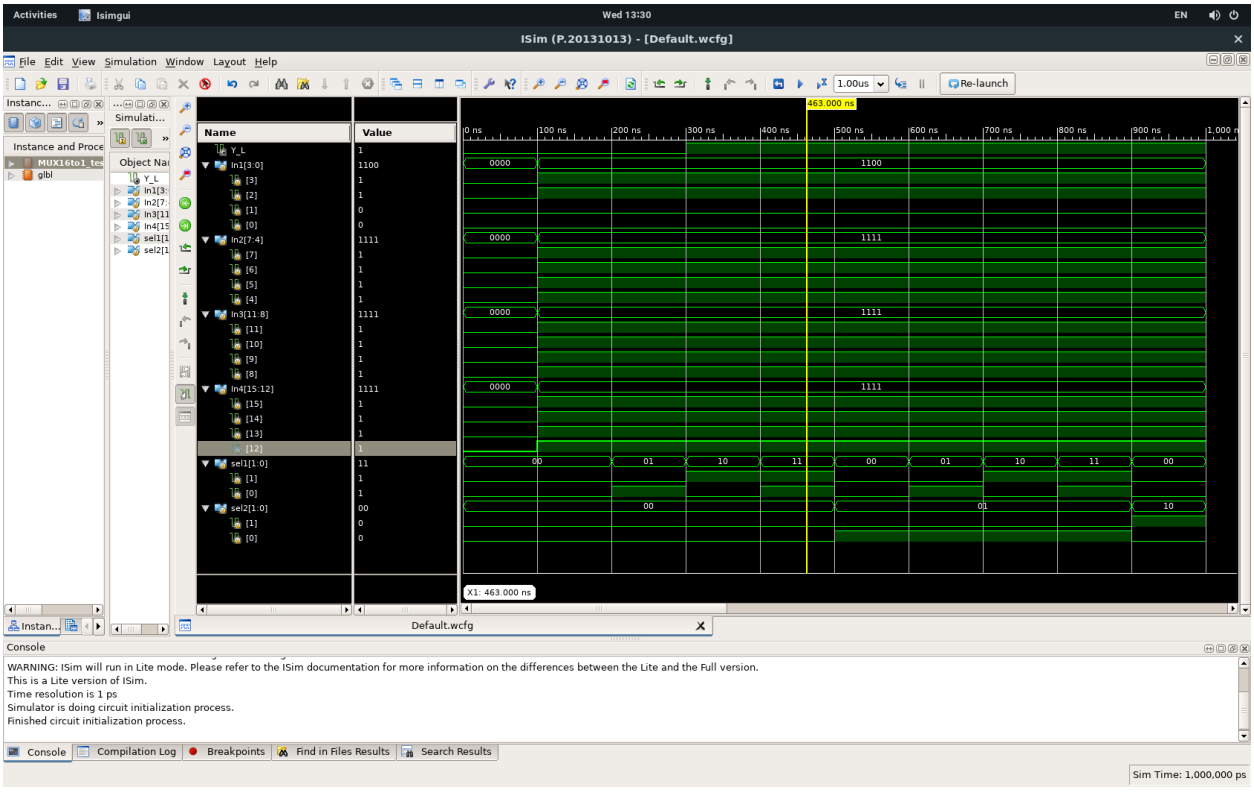

Activities
Isimgui
Wed 13:22
EN
ISim (P.20131013) - [Default.wcfg]
File Edit View Simulation Window Layout Help
Re-launch
Name
Value
Y_L
In1[3:0]
In2[7:4]
In3[11:8]
In4[15:12]
sel1[1:0]
sel2[1:0]
938.000 ns
X1: 938.000 ns
Default.wcfg
Console
WARNING: ISim will run in Lite mode. Please refer to the ISim documentation for more information on the differences between the Lite and the Full version.
This is a Lite version of ISim.
Time resolution is 1 ps
Simulator is doing circuit initialization process.
Finished circuit initialization process.
Console
Compilation Log
Breakpoints
Find in Files Results
Search Results
Sim Time: 1,000,000 ps

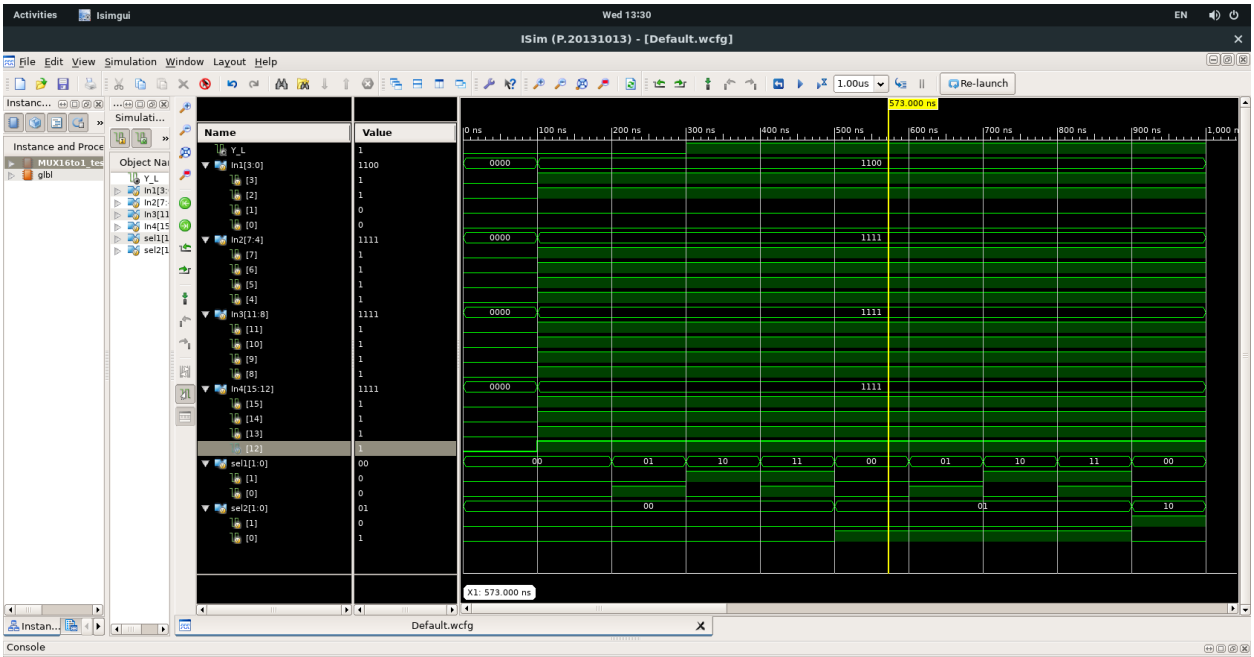
//2nd case fixed input 16'b1100111111111111

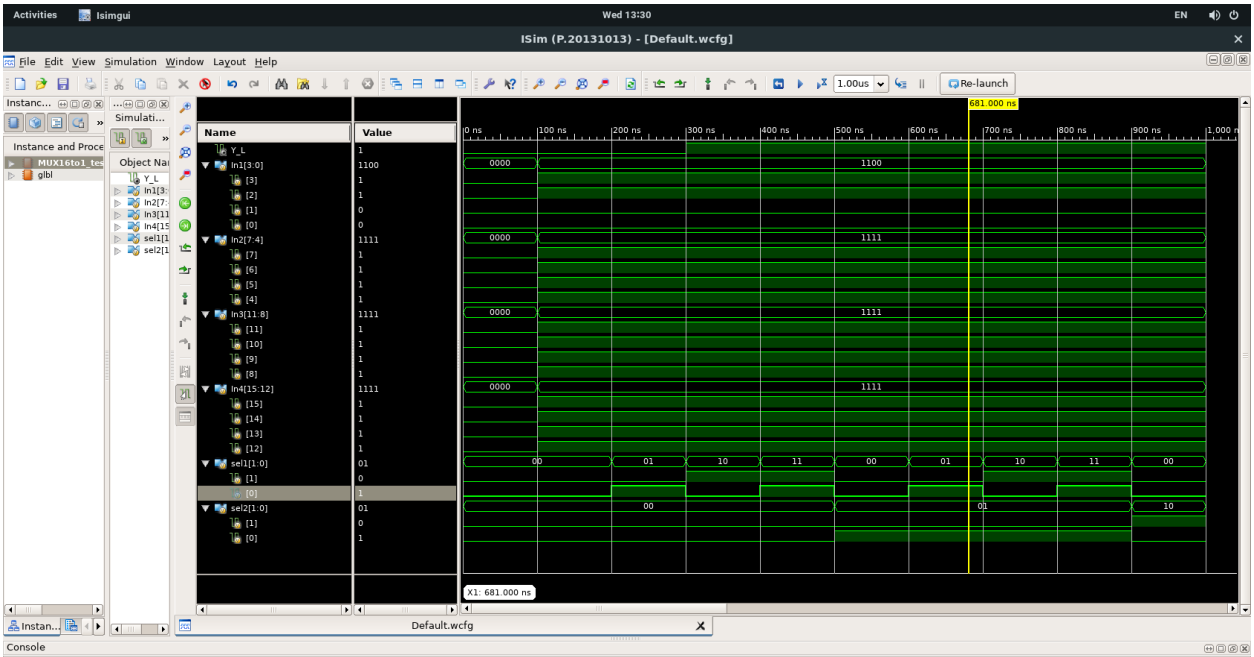


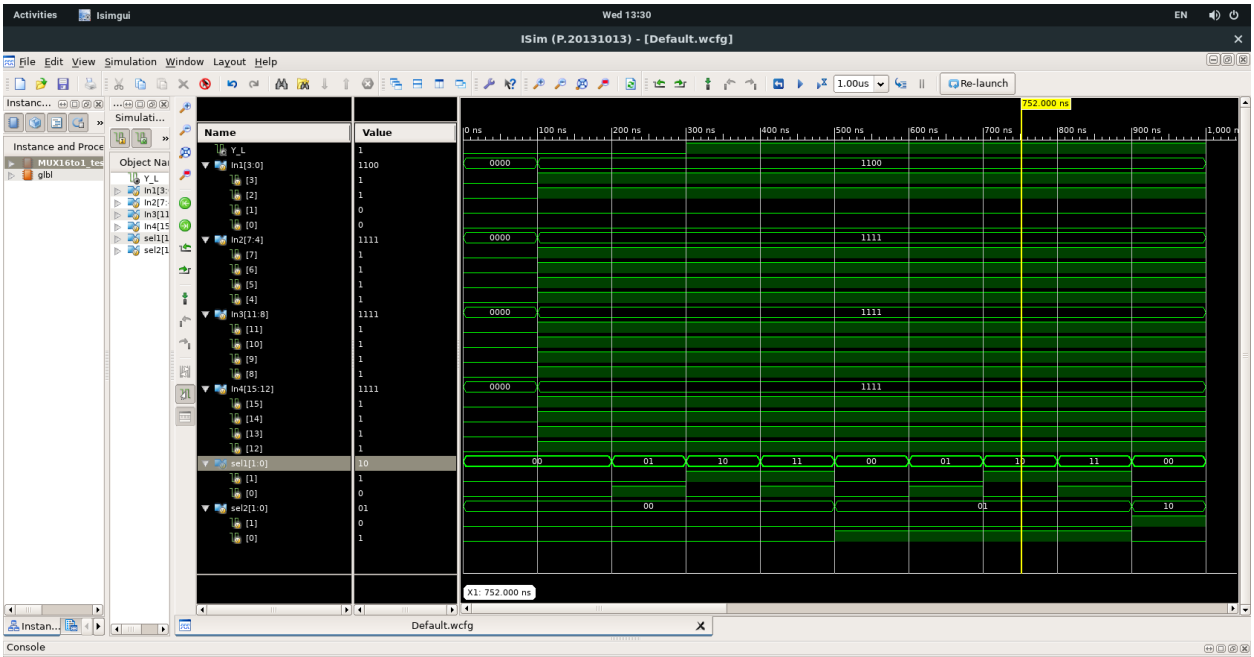


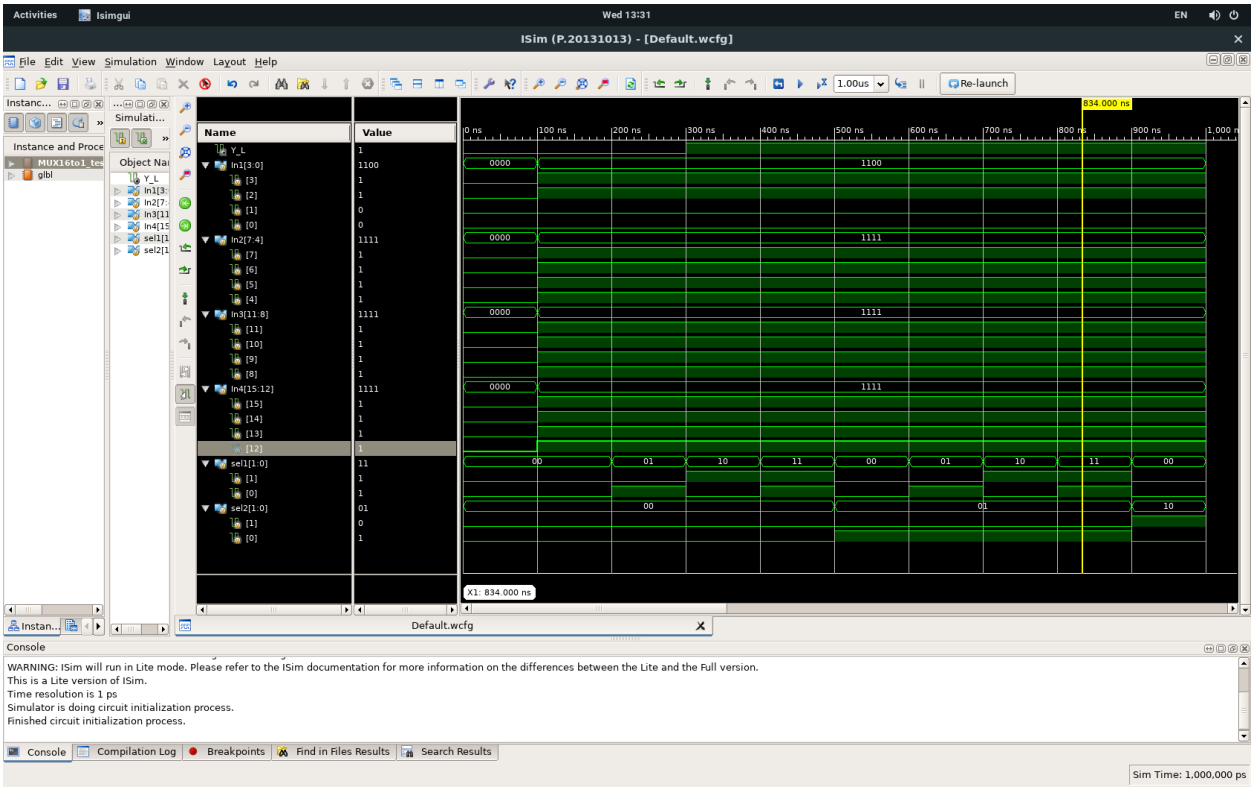

Activities
Isimgui
Wed 13:30
EN
ISim (P.20131013) - [Default.wcfg]
File Edit View Simulation Window Layout Help
Re-launch
Name
Value
345.000 ns
X1: 345.000 ns
Default.wcfg
Console
WARNING: ISim will run in Lite mode. Please refer to the ISim documentation for more information on the differences between the Lite and the Full version.
This is a Lite version of ISim.
Time resolution is 1 ps
Simulator is doing circuit initialization process.
Finished circuit initialization process.
Console
Compilation Log
Breakpoints
Find in Files Results
Search Results
Sim Time: 1,000,000 ps

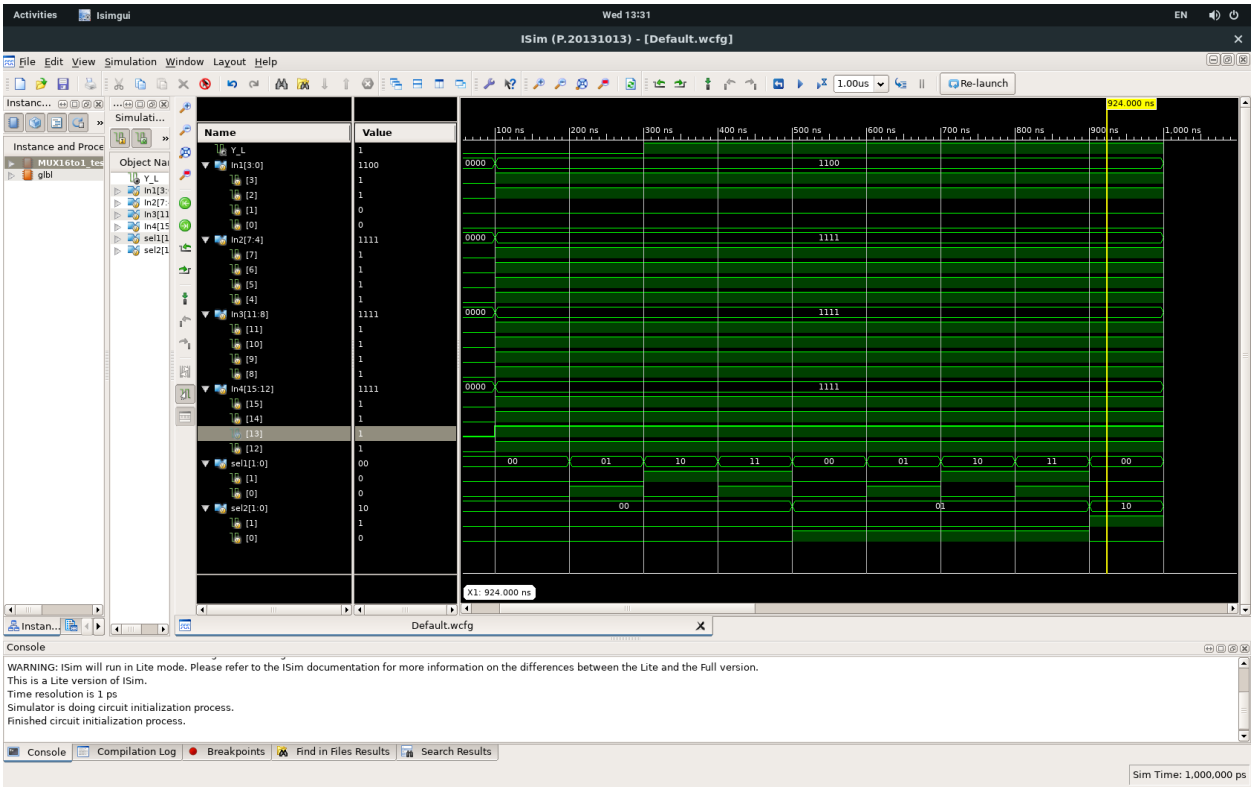

Activities
Isimgui
Wed 13:30
EN
ISim (P.20131013) - [Default.wcfg]
File Edit View Simulation Window Layout Help
Re-launch
Name
Value
463.000 ns
X1: 463.000 ns
Default.wcfg
Console
WARNING: ISim will run in Lite mode. Please refer to the ISim documentation for more information on the differences between the Lite and the Full version.
This is a Lite version of ISim.
Time resolution is 1 ps
Simulator is doing circuit initialization process.
Finished circuit initialization process.
Console
Compilation Log
Breakpoints
Find in Files Results
Search Results
Sim Time: 1,000,000 ps


Activities
Isimgui
Wed 13:30
EN
ISim (P.20131013) - [Default.wcfg]
File Edit View Simulation Window Layout Help
Re-launch
1.00us
573.000 ns
Name
Value
Y_L
in1[3:0]
in2[7:4]
in3[11:8]
in4[15:12]
sel1[1:0]
sel2[1:0]
X1: 573.000 ns
Default.wcfg
Console
WARNING: ISim will run in Lite mode. Please refer to the ISim documentation for more information on the differences between the Lite and the Full version.
This is a Lite version of ISim.
Time resolution is 1 ps
Simulator is doing circuit initialization process.
Finished circuit initialization process.
Console
Compilation Log
Breakpoints
Find in Files Results
Search Results
Sim Time: 1,000,000 ps

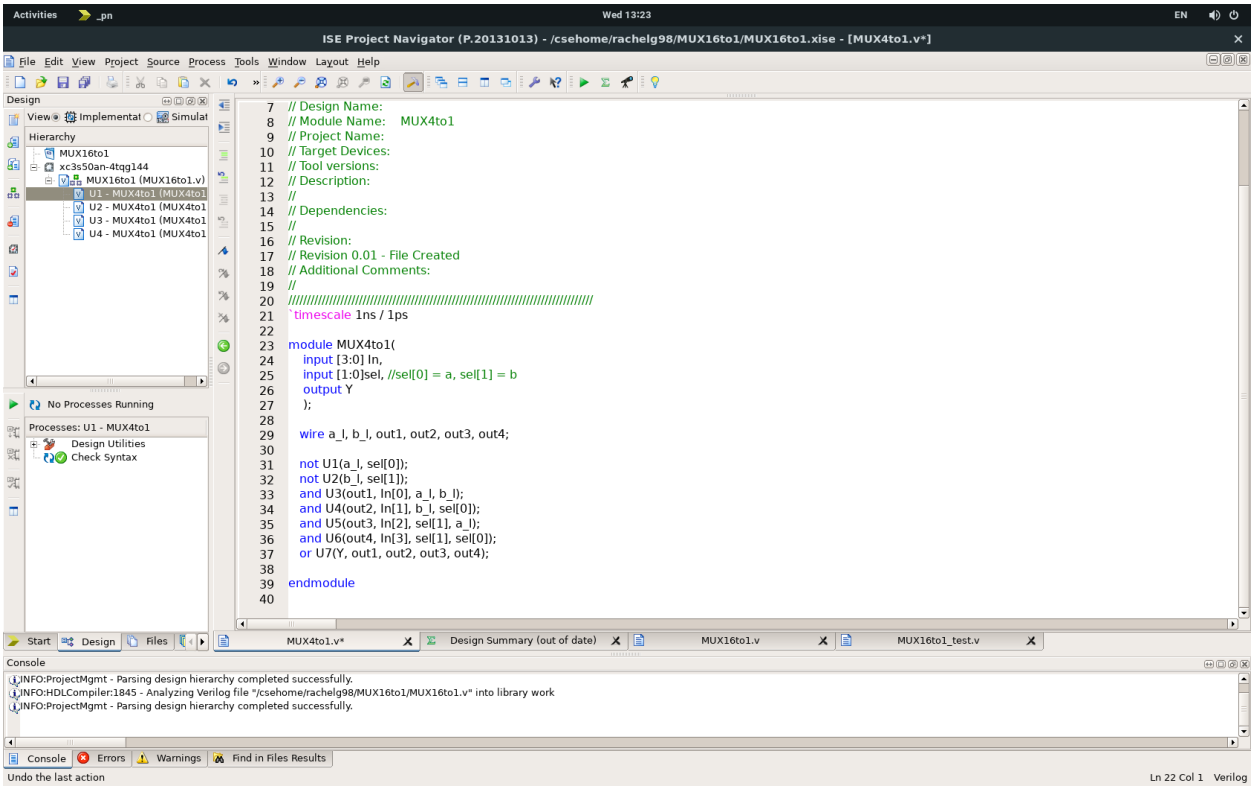

Activities
Isimgui
Wed 13:30
EN
ISim (P.20131013) - [Default.wcfg]
File Edit View Simulation Window Layout Help
Re-launch
1.00us
681.000 ns
Name
Value
Y_L
in1[3:0]
in2[7:4]
in3[11:8]
in4[15:12]
sel1[1:0]
sel2[1:0]
X1: 681.000 ns
Default.wcfg
Console
WARNING: ISim will run in Lite mode. Please refer to the ISim documentation for more information on the differences between the Lite and the Full version.
This is a Lite version of ISim.
Time resolution is 1 ps
Simulator is doing circuit initialization process.
Finished circuit initialization process.
Console
Compilation Log
Breakpoints
Find in Files Results
Search Results
Sim Time: 1,000,000 ps


Activities
Isimgui
Wed 13:30
EN
ISim (P.20131013) - [Default.wcfg]
File Edit View Simulation Window Layout Help
Re-launch
Name
Value
752.000 ns
X1: 752.000 ns
Default.wcfg
Console
WARNING: ISim will run in Lite mode. Please refer to the ISim documentation for more information on the differences between the Lite and the Full version.
This is a Lite version of ISim.
Time resolution is 1 ps
Simulator is doing circuit initialization process.
Finished circuit initialization process.
Console
Compilation Log
Breakpoints
Find in Files Results
Search Results
Sim Time: 1,000,000 ps

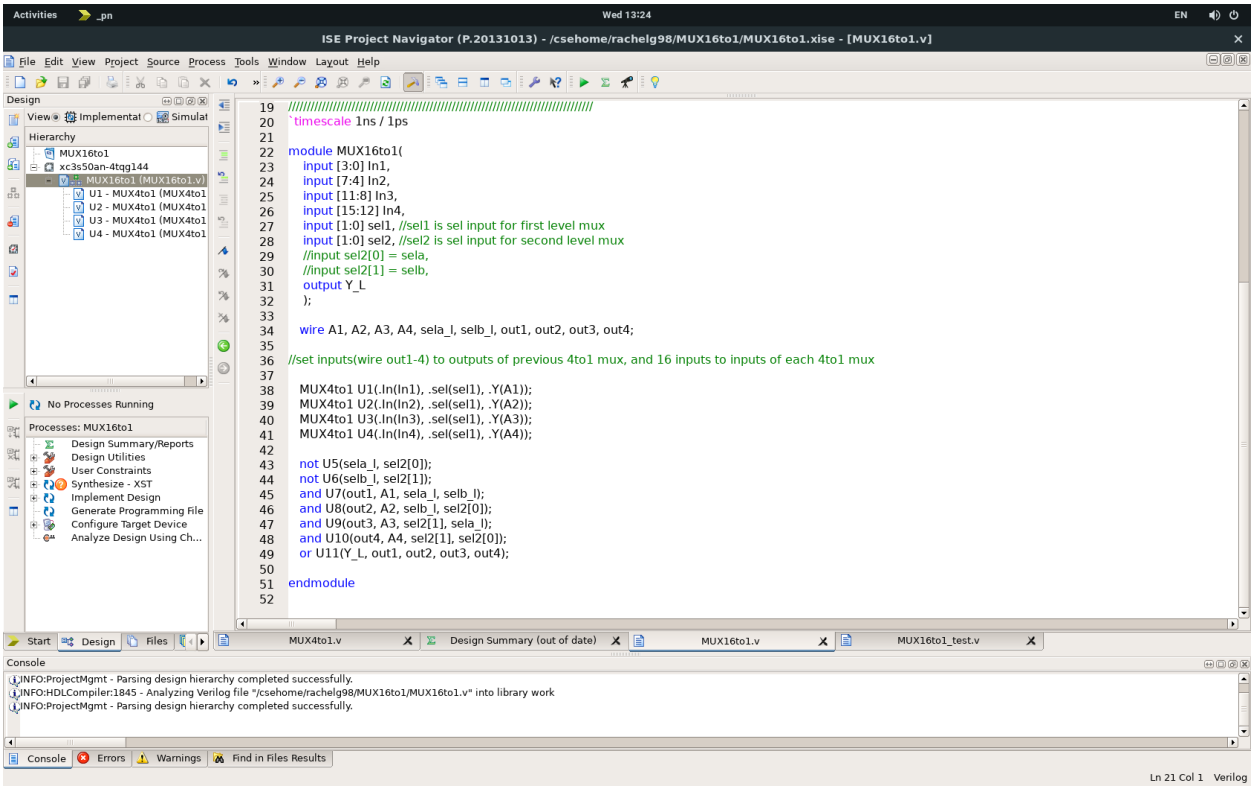

Activities
Isimgui
Wed 13:31
EN
ISim (P.20131013) - [Default.wcfg]
File Edit View Simulation Window Layout Help
Re-launch
Name
Value
834.000 ns
X1: 834.000 ns
Default.wcfg
Console
WARNING: ISim will run in Lite mode. Please refer to the ISim documentation for more information on the differences between the Lite and the Full version.
This is a Lite version of ISim.
Time resolution is 1 ps
Simulator is doing circuit initialization process.
Finished circuit initialization process.
Console
Compilation Log
Breakpoints
Find in Files Results
Search Results
Sim Time: 1,000,000 ps



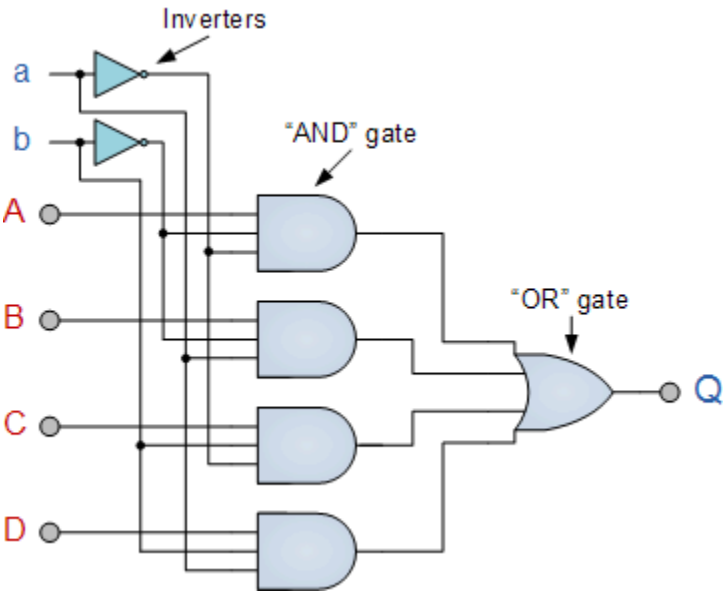
Code 4 to 1 MUX (Structural):



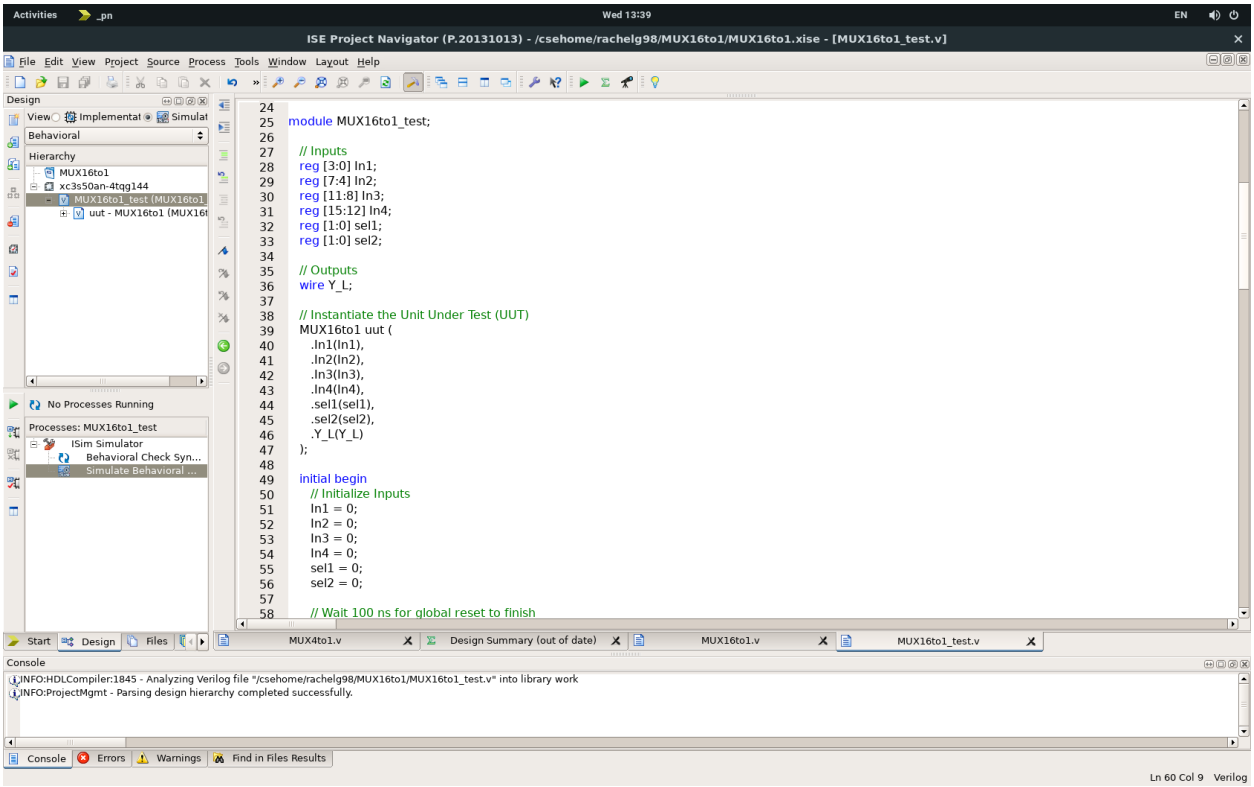
Code 16 to 1 (Hierarchy):



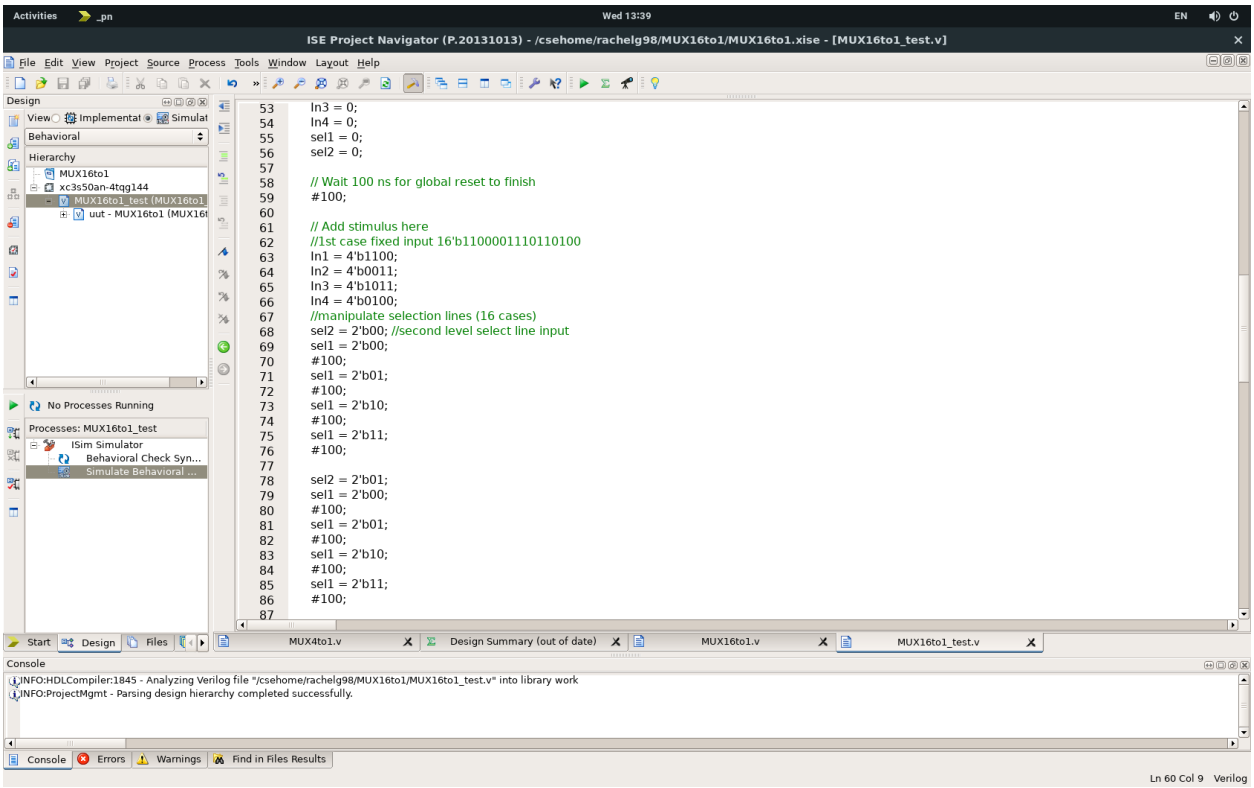
Logic Diagram:



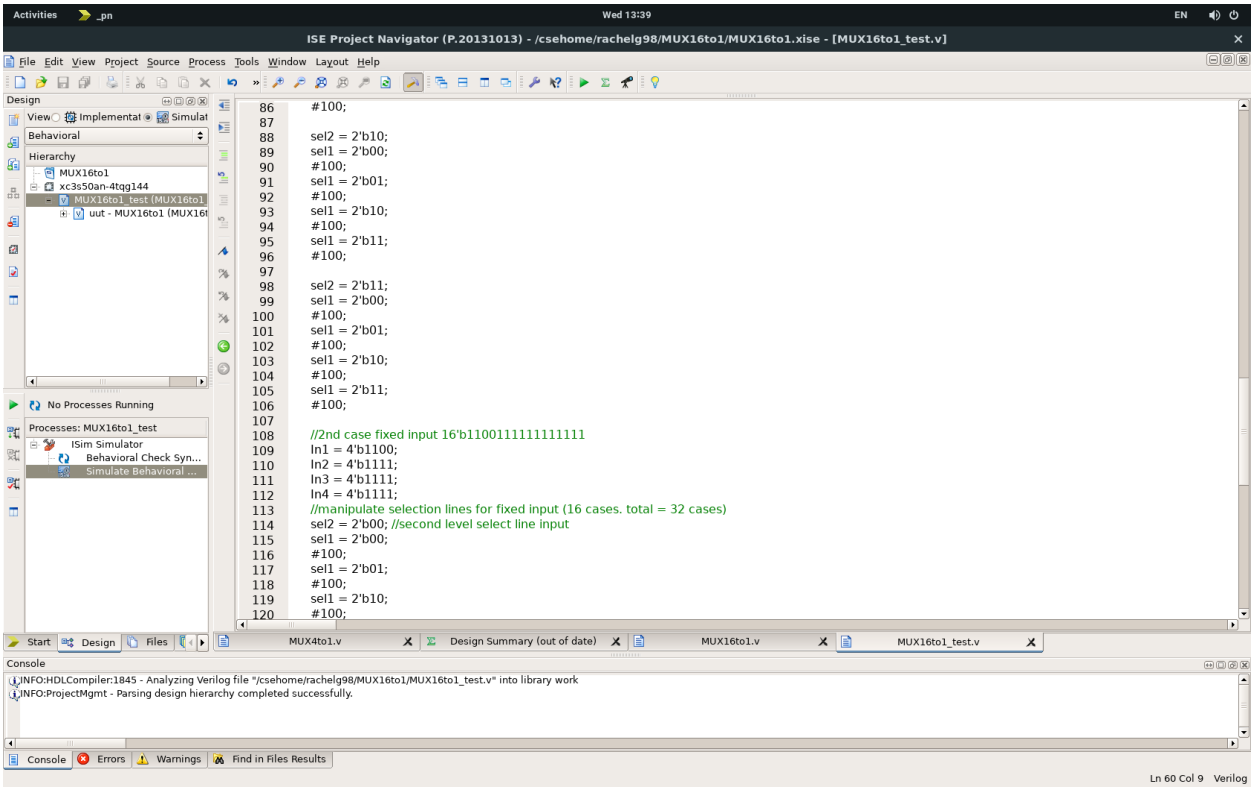
Test Bench:




```
24
25  module MUX16to1_test;
26
27    // Inputs
28    reg [3:0] In1;
29    reg [7:4] In2;
30    reg [11:8] In3;
31    reg [15:12] In4;
32    reg [1:0] sel1;
33    reg [1:0] sel2;
34
35    // Outputs
36    wire Y_L;
37
38    // Instantiate the Unit Under Test (UUT)
39    MUX16to1 uut (
40      .In1(In1),
41      .In2(In2),
42      .In3(In3),
43      .In4(In4),
44      .sel1(sel1),
45      .sel2(sel2),
46      .Y_L(Y_L)
47    );
48
49    initial begin
50      // Initialize Inputs
51      In1 = 0;
52      In2 = 0;
53      In3 = 0;
54      In4 = 0;
55      sel1 = 0;
56      sel2 = 0;
57
58      // Wait 100 ns for global reset to finish
```




```
53      In3 = 0;
54      In4 = 0;
55      sel1 = 0;
56      sel2 = 0;
57
58      // Wait 100 ns for global reset to finish
59      #100;
60
61      // Add stimulus here
62      //1st case fixed input 16'b1100001110110100
63      In1 = 4'b1100;
64      In2 = 4'b0011;
65      In3 = 4'b1011;
66      In4 = 4'b0100;
67      //manipulate selection lines (16 cases)
68      sel2 = 2'b00; //second level select line input
69      sel1 = 2'b00;
70      #100;
71      sel1 = 2'b01;
72      #100;
73      sel1 = 2'b10;
74      #100;
75      sel1 = 2'b11;
76      #100;
77
78      sel2 = 2'b01;
79      sel1 = 2'b00;
80      #100;
81      sel1 = 2'b01;
82      #100;
83      sel1 = 2'b10;
84      #100;
85      sel1 = 2'b11;
86      #100;
87
```


Activities
_pn
Wed 13:39
EN
ISE Project Navigator (P.20131013) - /csehome/rachelg98/MUX16to1/MUX16to1.xise - [MUX16to1_test.v]
File Edit View Project Source Process Tools Window Layout Help
Design
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Behavioral Check Syn...
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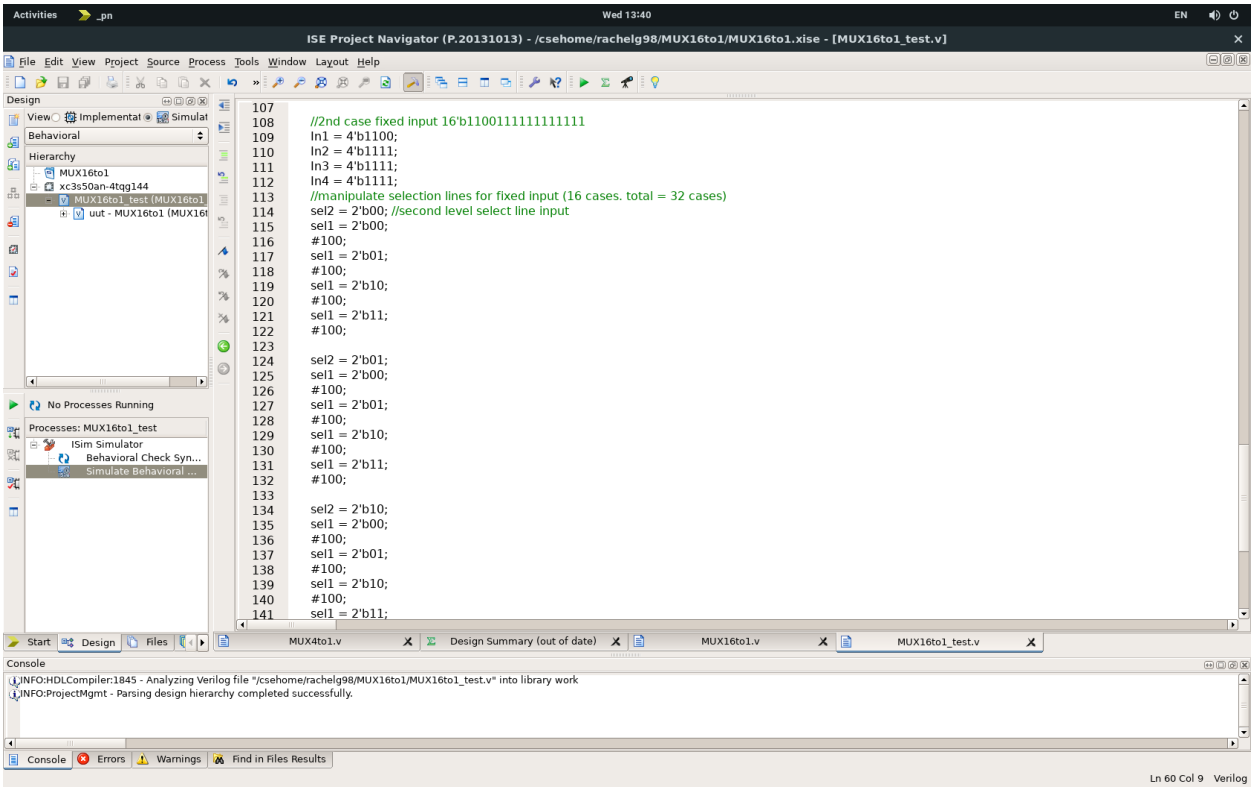
Design Summary (out of date)
MUX16to1.v
MUX16to1_test.v
Console
INFO:HDLCompiler:1845 - Analyzing Verilog file "/csehome/rachelg98/MUX16to1/MUX16to1_test.v" into library work
INFO:ProjectMgmt - Parsing design hierarchy completed successfully.
Console Errors Warnings Find in Files Results
Ln 60 Col 9 Verilog


Activities
_pn
Wed 13:40
EN
ISE Project Navigator (P.20131013) - /csehome/rachelg98/MUX16to1/MUX16to1.xise - [MUX16to1_test.v]
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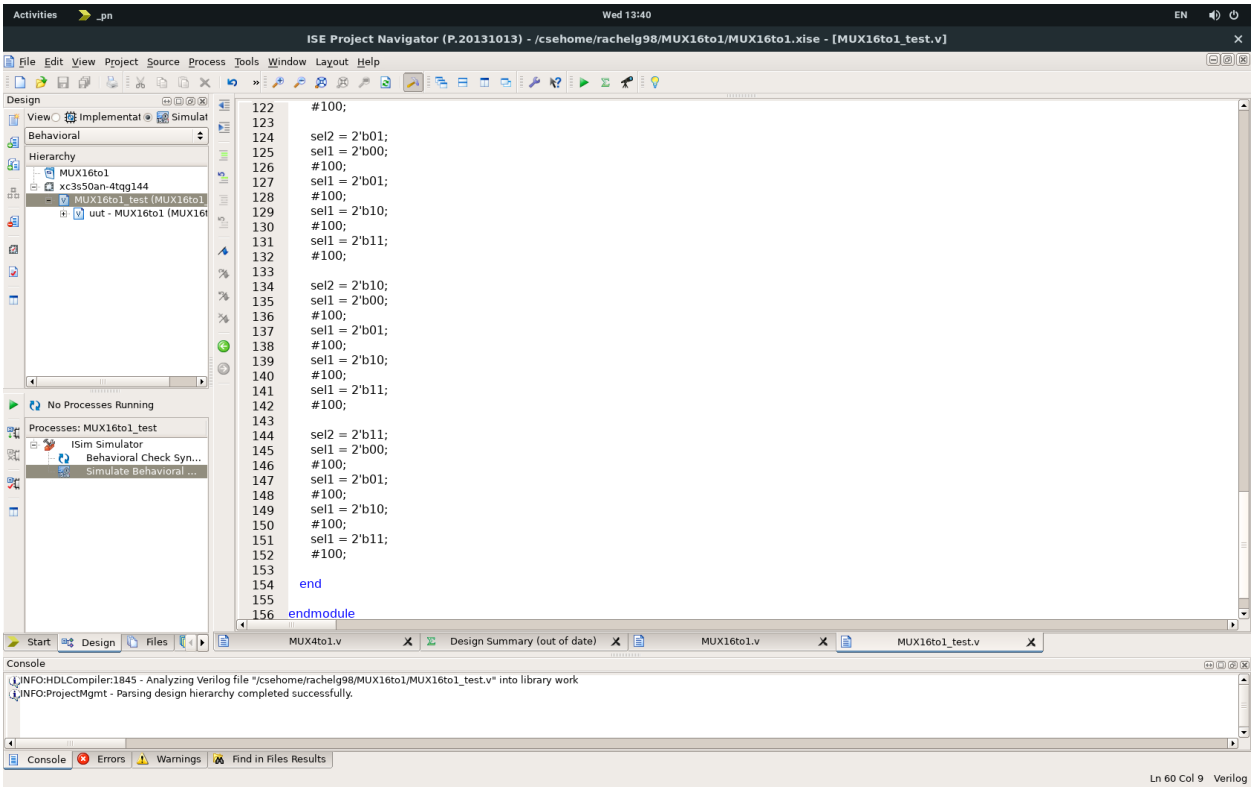
No Processes Running
Processes: MUX16to1_test
ISim Simulator
Behavioral Check Syn...
Simulate Behavioral ...
Start Design Files
MUX4to1.v
Design Summary (out of date)
MUX16to1.v
MUX16to1_test.v
Console
INFO:HDLCompiler:1845 - Analyzing Verilog file "/csehome/rachelg98/MUX16to1/MUX16to1_test.v" into library work
INFO:ProjectMgmt - Parsing design hierarchy completed successfully.
Console Errors Warnings Find in Files Results
Ln 60 Col 9 Verilog



4. Conclusion/Discussion

Verilog를 이용해 직접 논리 회로를 코딩하면서 verilog의 문법을 익혔다. Multiplexer의 기능도 이해했고 4-to-1 Multiplexer이 5개 있으면 16-to-1 Multiplexer를 설계할 수 있다는 사실을 알게 되었다.