

Logic Design Lab Report: Week 9

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1. Introduction

이번 lab 에서는 8-bit universal shift register 를 verilog 를 이용하여 implement 하고 simulate 했다.

2. Implementation

verilog 를 통하여 구현한다.

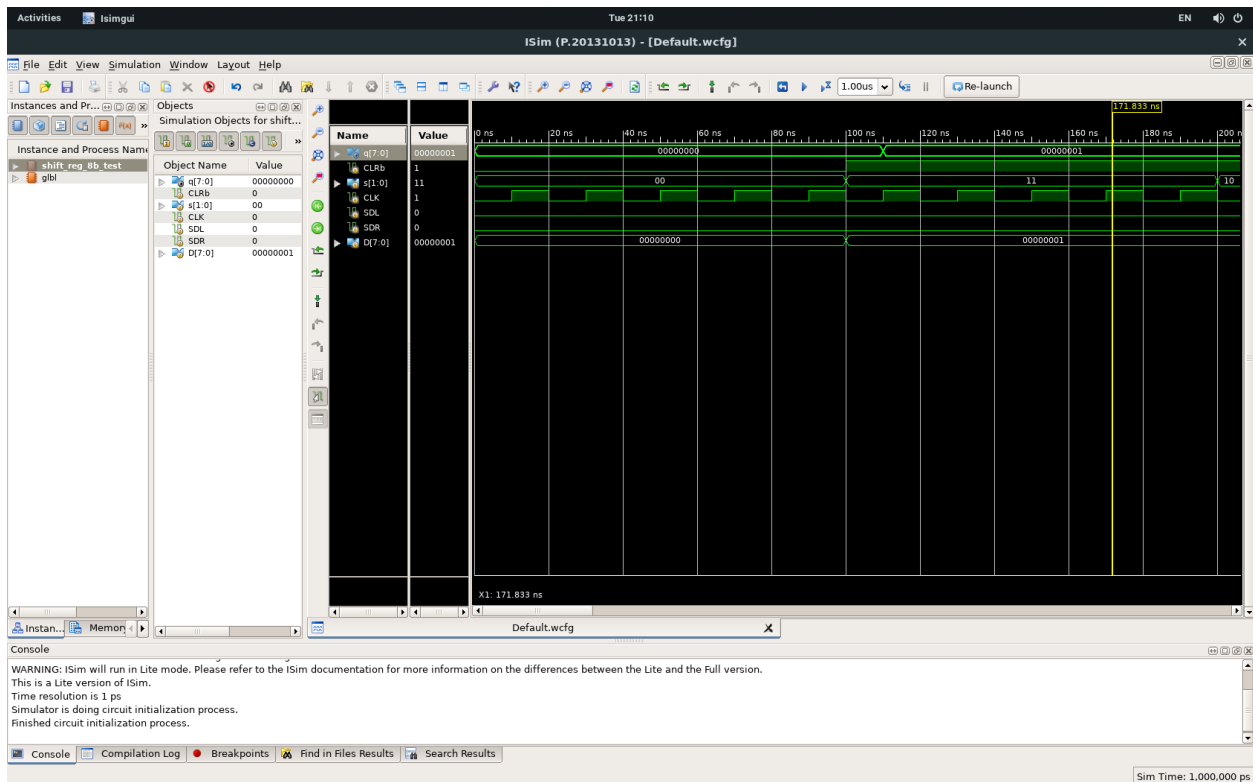
3. Result

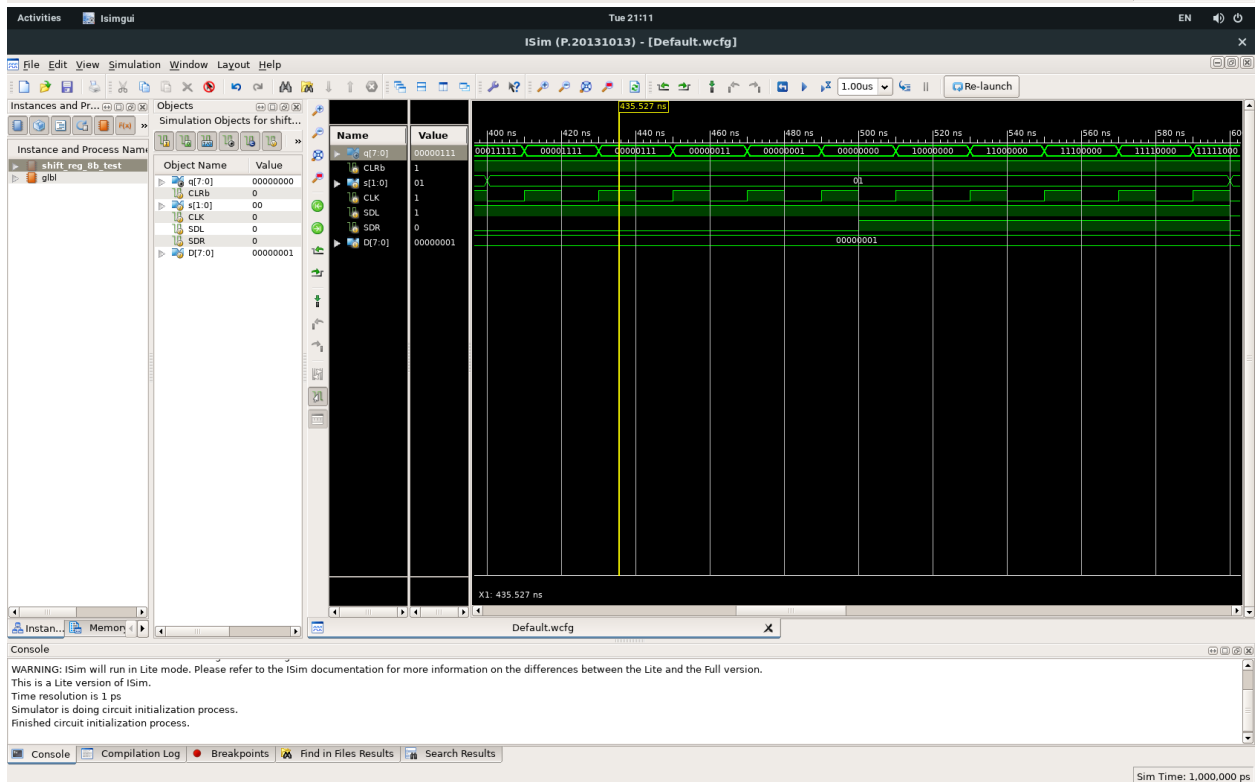
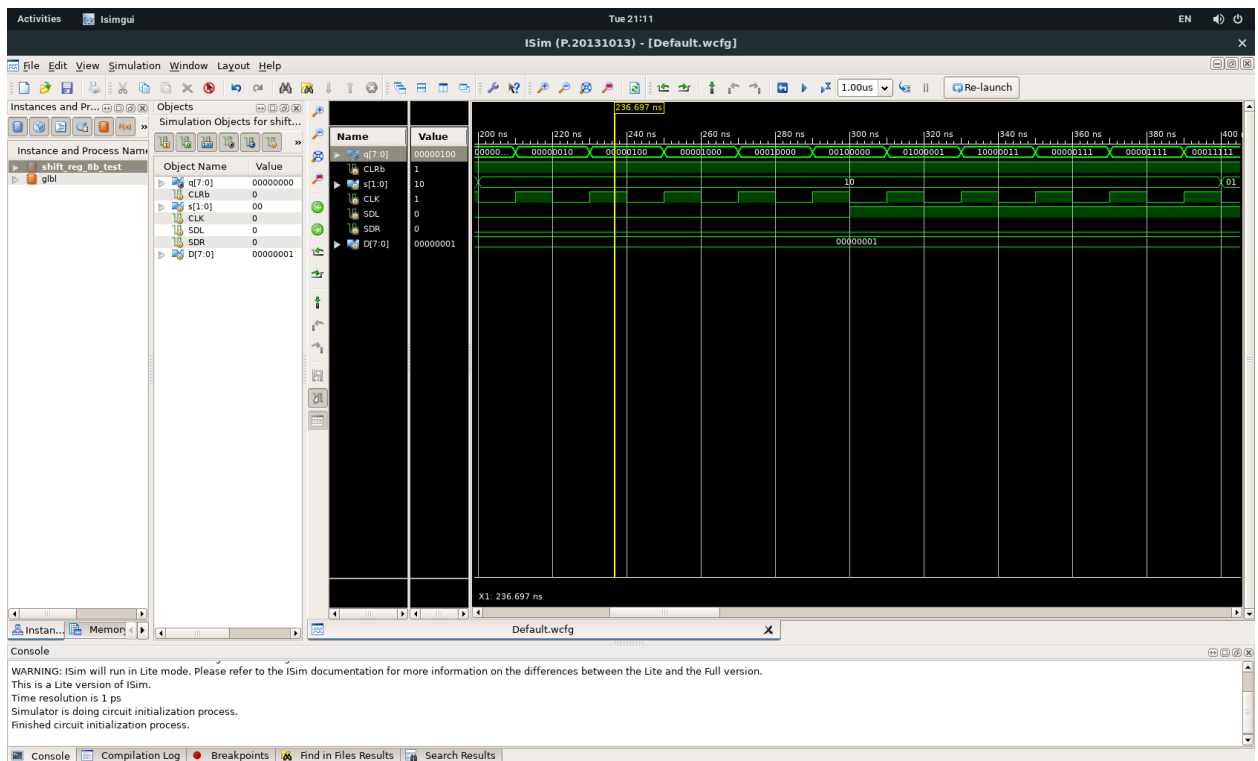
아래의 표를 참고하여 code 를 작성하였다.

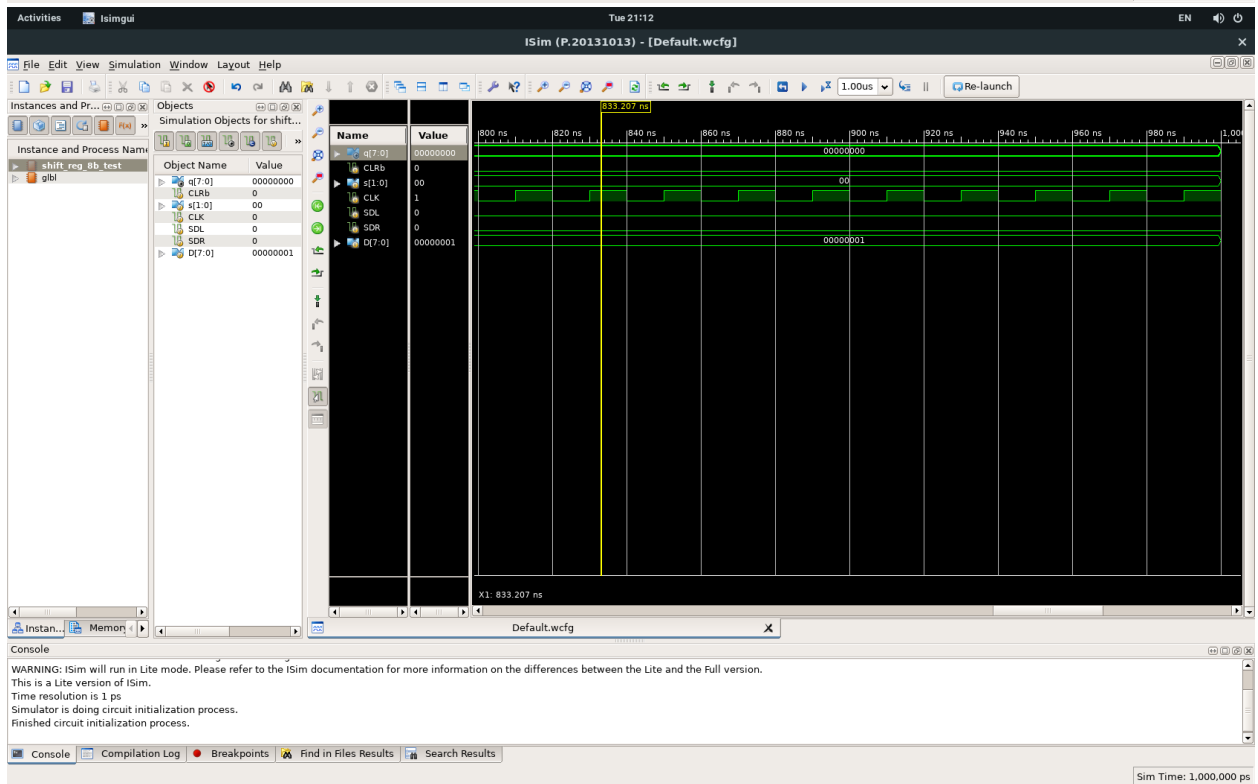
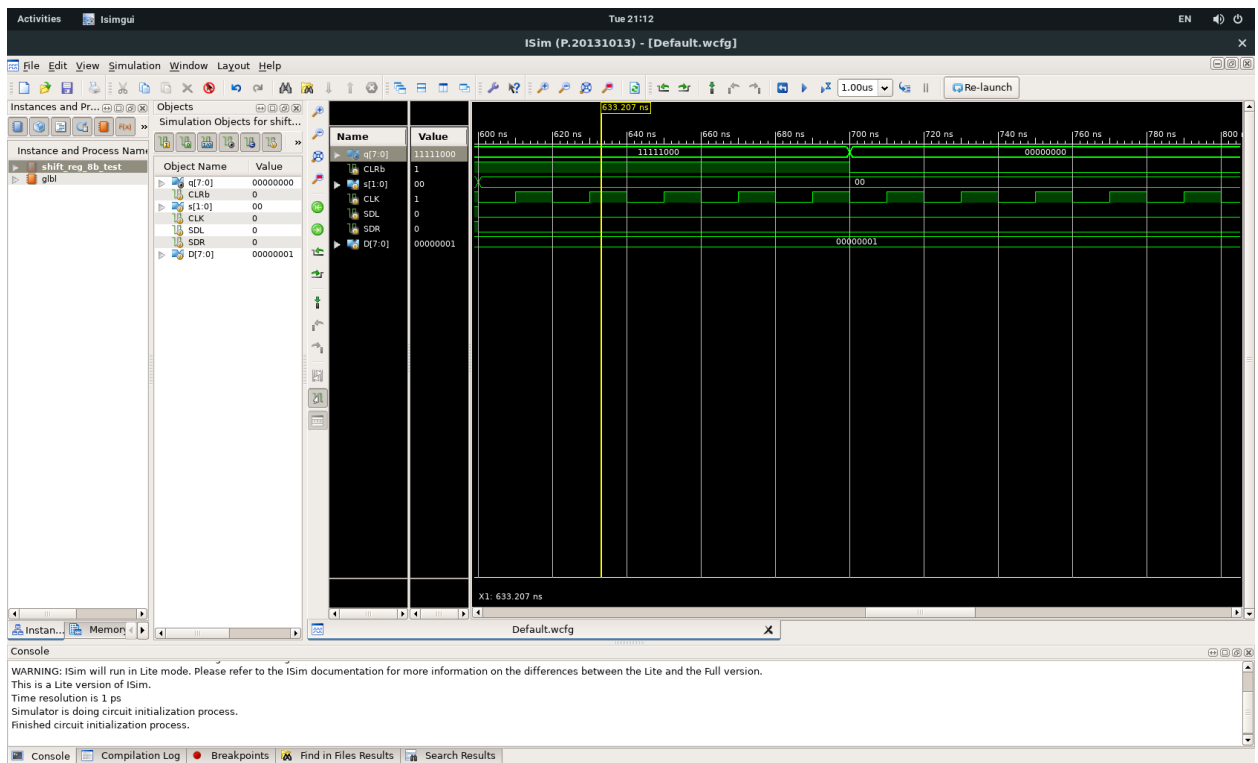
Asynchronous CLRb

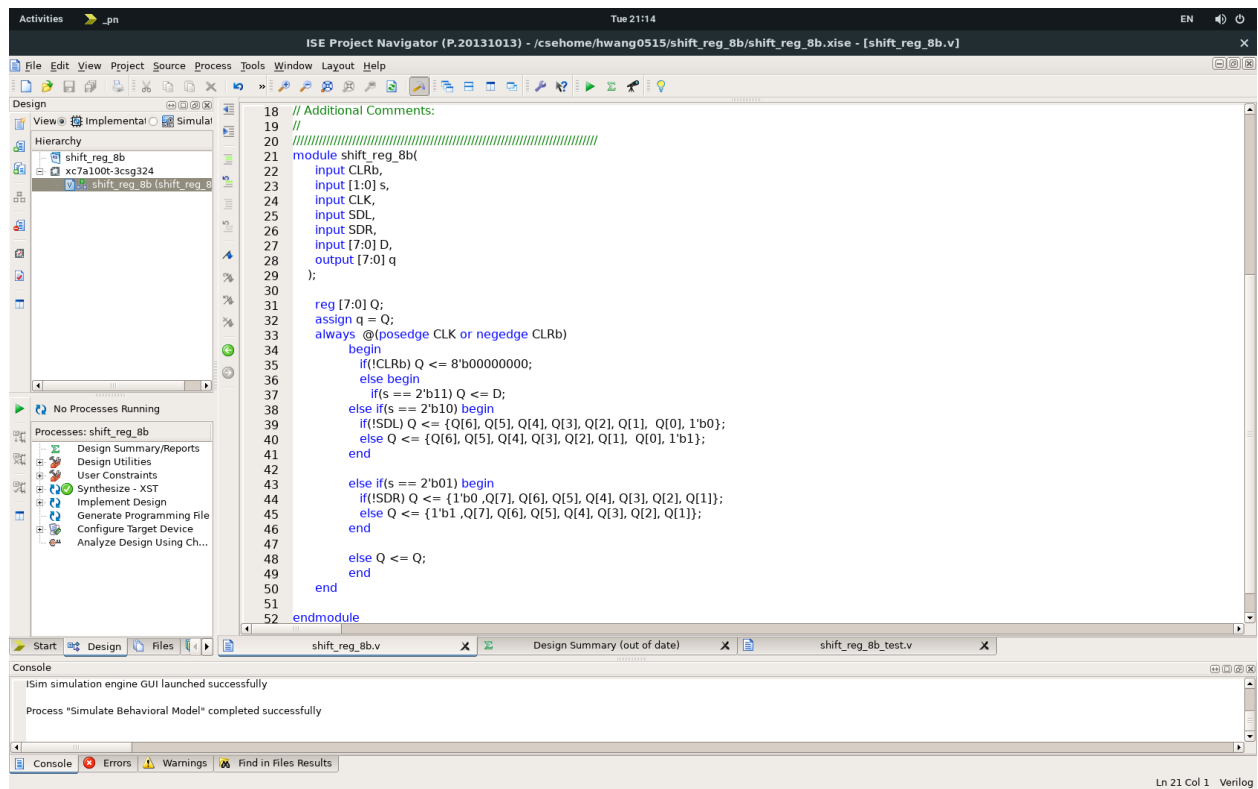
CLRb	MODE		CLK	SERIAL		PARALLEL								PARALLEL							
	S1	S0		SDL	SDR	D7	D6	D5	D4	D3	D2	D1	D0	Q7(t+1)	Q6(t+1)	Q5(t+1)	Q4(t+1)	Q3(t+1)	Q2(t+1)	Q1(t+1)	Q0(t+1)
0	X	X	X	X	X	X	X	X	X	X	X	X	X	0	0	0	0	0	0	0	0
1	X	X	-	X	X	X	X	X	X	X	X	X	X	Q7(t)	Q6(t)	Q5(t)	Q4(t)	Q3(t)	Q2(t)	Q1(t)	Q0(t)
1	1	1	↑	X	X	d7	d6	d5	d4	d3	d2	d1	d0	d7	d6	d5	d4	d3	d2	d1	d0
1	1	0	↑	0	X	X	X	X	X	X	X	X	X	Q6(t)	Q5(t)	Q4(t)	Q3(t)	Q2(t)	Q1(t)	Q0(t)	0
1	1	0	↑	1	X	X	X	X	X	X	X	X	X	Q6(t)	Q5(t)	Q4(t)	Q3(t)	Q2(t)	Q1(t)	Q0(t)	1
1	0	1	↑	X	0	X	X	X	X	X	X	X	X	0	Q7(t)	Q6(t)	Q5(t)	Q4(t)	Q3(t)	Q2(t)	Q1(t)
1	0	1	↑	X	1	X	X	X	X	X	X	X	X	1	Q7(t)	Q6(t)	Q5(t)	Q4(t)	Q3(t)	Q2(t)	Q1(t)
1	0	0	↑	X	X	X	X	X	X	X	X	X	X	Q7(t)	Q6(t)	Q5(t)	Q4(t)	Q3(t)	Q2(t)	Q1(t)	Q0(t)

CLEAR
NO CHANGE
PARALLEL LOAD
SHIFT LEFT
SHIFT RIGHT
HOLD









4. Conclusion / Discussion

Verilog 를 이용하여 CLK 가 비동기화된 8-bit universal shift register 를 구현할 수 있었다.