

RTL DESIGN AND SIMULATION OF ELECTRONIC VOTING MACHINE ARCHITECTURE USING VERILOG

A Major Project Report Submitted in partial fulfillment of the requirements for the degree of Bachelor of

Technology

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DECLARATION

We hereby declare that the project work entitled “ **RTL Design & Simulation of Electronic Voting Machine Architecture using Verilog**”, is an authenticated work carried out by us under the guidance of **Dr. Agile Mathew** sir for the requirements of **Major Project-II**, as part of the *8th* Semester curriculum of Bachelor of Technology in Electronics and Communication Engineering and this work, has not been submitted for similar purpose anywhere else except to the Department of Electronics and Communication Engineering, Central Institute of Technology, Kokrajhar.

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BONAFIDE CERTIFICATE

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ABSTRACT

In this project, an attempt has been made to show the Architectural Design (RTL Design) and Functional Verification and Simulation of Electronic Voting Machine's Protocol. Primarily we have come to this project approach by looking at the design of an existing microprocessor and microcontroller based Electronic Voting Machine.

When we compare the architectural differences of our design with reference to the existing microprocessor based EVM system, we get to see the following points –

- They used 8086 Microprocessor to execute various instructions; but in our project, we used specific digital circuit to perform all the instruction which are needed without the use of 8086 Microprocessor.
- They used Two EEPROMs as odd bank and even bank memory to store 16-bit data. These EEPROMs store the main operating system, acts like RAM during instruction execution and also store voting information. But in our project, we used single EEPROM which perform the same operation.

Basically, in the existing design they had created a general purpose architecture. But, in this project we are mainly doing application specific architectural design which is purely for a particular application. Also we have realized the need for a framework that can offer some of the best technology for designing an Electronic Voting Machine. Since we all understand that it is laborious to manage control signals, here we have tried to structure the RTL design of Electronic Voting Machines in Verilog HDL.

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Contents

DECLARATION	2
CERTIFICATE	3
ABSTRACT	4
ACKNOWLEDGMENT	5
List of Figures	10
1 INTRODUCTION	11
1.1 Background of Study	11
1.2 Electronic Voting Machine Overview	11
1.3 Problem Statement	12
1.4 Project Outline	12
2 LITERATURE REVIEW	14
3 METHODOLOGY & SYSTEM DESIGN	22
3.1 Methodology	22
3.1.1 Research Purpose	22
3.1.2 Research Approach	22
3.2 Requirements Analysis & Specification	23
3.2.1 Main Units of EVM	23
3.2.2 DESIGN DESCRIPTION	27
3.2.3 Design Specification	29
3.2.4 RTL Design	29

3.3	Hardware Description Block Diagram	29
3.4	DATAPATH DESIGN	30
3.4.1	During Reset Mode	30
3.4.2	During Voting Mode	32
3.4.3	During Individual Counting Mode	32
3.4.4	During Total Counting Mode	32
3.5	Algorithmic State Machine (ASM Chart)	32
3.6	Finite State Machines (FSM chart)	32
3.7	State Table	39
4	SUB-SYSTEM DESCRIPTION	41
4.1	Encoder	41
4.2	Parallel In Parallel Out (PIPO) Shift Registers	42
4.3	Multiplexer	43
4.4	Random Access Memory (RAM)	45
4.5	Adder	45
4.6	Counter	45
4.7	Monostable Multivibrator	46
5	SYSTEM VERIFICATION & SIMULATION	47
5.1	16:4 Encoder	47
5.2	Parallel In Parallel Out (PIPO) Shift Registers	47
5.3	2:1 Multiplexer	47
5.4	Random Access Memory (RAM)	47
5.5	Adder	50
5.6	Counter	50
5.7	Monostable Multivibrator	50
5.8	Final Simulation Result of EVM	52

List of Figures

2.1	Block diagram of Electronic Voting Machine	15
2.2	Flow Chart	17
2.3	Circuit Diagram of SEVM for the position of two Candidates	18
2.4	Flowchart of the Biometrically Secured EVM	20
2.5	Proposed system blocks of voting station	21
3.1	Ballot Unit	24
3.2	Control Unit	25
3.3	Design Flow Diagram	28
3.4	Block diagram of EVM	30
3.5	Block diagram of Datapath Design	31
3.6	Datapath Design of Reset Mode	33
3.7	Datapath Design of Voting Mode	34
3.8	Datapath Design of Individual Counting Mode	35
3.9	Datapath Design of Total Counting Mode	36
3.10	ASM Chart	37
3.11	FSM Chart	38
3.12	State Table	40
4.1	A General Encoder's Block Diagram	41
4.2	Truth Table of 16:4 Encoder	42
4.3	4-bit PIPO Shift Register	43

4.4	Block Diagram of 2:1 Multiplexer	44
4.5	Truth Table of 2:1 Multiplexer	44
4.6	Block Diagram of RAM	45
5.1	Simulation Result of 16:4 Encode	48
5.2	Simulation Result of PIPO Shift Registers	48
5.3	Simulation Result of 2:1 Multiplexer	49
5.4	Simulation Result of RAM	49
5.5	Simulation Result of Adder	50
5.6	Simulation Result of Counter	51
5.7	Simulation Result of Monostable Multivibrator	51
5.8	Simulation Waveforms showing Clear Mode and Vote Casted by Candidate . .	52
5.9	Simulation Waveforms showing Individual and Total Counting of Vote	53

Chapter 1

INTRODUCTION

1.1 Background of Study

In every democratic setting with persons of differing and inconsistent opinions, decisions must be made between several options. This happens in business environment, educational environment, social organisations, and mostly in governance. One of the ways of making such a decision is through voting. Voting is a formal process of expressing individual opinions for or against some motion. In the governance sector of many organisation this process is always used as a means of selecting or electing a leader. One of the key areas where voting is applied is in election. Election is the formal process of selecting a person for public office or of accepting or rejecting a political proposition by voting.

1.2 Electronic Voting Machine Overview

Elections in India are conducted almost exclusively by using electronic voting machines developed over the past two decades by a pair of government - owned companies. These devices, known in India as EVMs, have been praised for their simple design, ease of use, and reliability. The Electronic Voting Machine (EVM) consists of two interconnected units, the Ballot Unit where the voter casts his vote by pressing a button alongside the name of the candidate and symbol of the party for whom the person chooses to vote for and the Control Unit by which the polling official enables the Ballot Unit for the voter to cast his vote and where all related data like number of votes polled for each candidate, total number of votes cast etc. resides . EVMs reduce the time in both casting a vote and declaring the results compared

to the old ballot paper system. The control unit can store the result in its memory for more than 10 years. Invalid votes can be greatly reduced by use of EVMs. Blank votes can be counted. Despite the many advantages of EVMs, there are certain issues in terms of software and hardware.

1.3 Problem Statement

In the existing voting machines, the number of candidates supported is limited to around 16 only, if the number of candidates exceeds 16 we are supposed to use 2 voting machines. At present, EVMs are used only in LOK SABHA and ASSEMBLY elections (it accepts only 1 vote from each voter), but in elections such as GRAMA PANCHAYATH and COOPERATIVE SOCIETIES where each voter cast their votes to more than one candidate; available voting machines can not be used.

Also this present voting system applicable in the Nigerian electoral system has proved inefficient as the voters' registration process is slow, the manual collation of results takes time and gives room for result manipulation, also the inaccessible nature of election venues which includes the long distances to be covered by voters' to their registered location increases voters' apathy towards the election processes, and finally the issues of ballot box snatching and damage and other election violence and issues associated with the traditional ballot paper voting all defiles the purpose of voting in election process as a formal process of expressing individual opinions for or against some motion.

1.4 Project Outline

This project work on ‘RTL Design and Simulation of Electronic Voting Machine Architecture’ is made up of six chapters: **Introduction, Literature Review, Methodology & System Design** (in terms of Block Diagram, Algorithmic State Machine (ASM chart), Finite State Machines (FSM chart) & State Table), **Sub-System Description, System Verification & Simulation**, and **Conclusion**.

In the chapter one of this project, the introduction which briefly explains voting and elections in general, is seen. It goes further to explain the background of an electronic voting machine or system, the aim and objectives of the e-voting machine, its significance, scope, and constraints. It summaries by giving the project outline.

In the chapter two, a review of previous literature and technologies used for electronic voting machine

was treated. We also see the different approaches to electronic voting machine, their implementation, criticism with their literature reviews and noted the various gaps in the existing literature's.

In chapter three, we see the block diagram of the project work, different methodologies used in development stages, the different phases of the project work which include its research, RTL design, Verilog programming, Testing and Simulation. We extensively cover the requirements of the project, such as the mathematical models used, algorithms, designs and software incorporated in the work.

In chapter four, we talk about the steps taken and techniques used for the actual Verification and Simulation of the project. We see tests carried out to ensure that the project is efficient and also display the result gotten and their significance. We also see the problems encountered and the techniques and solutions taken to overcome them or not.

And finally, in chapter five, we conclude the work and give notable recommendations for optimal operation of the product. Also we provide suggestions for improvement, enhancement and optimization of our existing work. We also outline the major contribution to the body of knowledge in which our work has achieved.

Chapter 2

LITERATURE REVIEW

[1] **Muhammad Raisul Alam etc. al.**, had presented a study named “Design and Implementation of Microprocessor Based Electronic Voting System”. In this study they described the design and hardware implementation of an electronic voting machine. The main aim of their project is not to design a power efficient perfect device but is to design a mother device that can be adoptable to any recent technologies. The design of the machine and its usage is as simple as an illiterate common people can easily use it. A vote casting procedure is also proposed to use the machine where they prescribed a new procedure called DEMO vote casting which is a testing mechanism to test the device before vote casting and also at the run time. The vote casting system is almost similar to traditional system, only ballot box will be replaced by the device. The machine uses Voter ID to identify a valid voter and restrict multiple vote casting.

In their design, they used 8086 microprocessor to execute instructions. Several latches are used to latch address generated from microprocessor. Data buffers are used to control directions of data. Two EEPROMs are used as odd bank and even bank memory to store 16 bit data. These EEPROMs store the main operating system, acts like RAM during instruction execution and also store voting information. The EEPROMs are removable. An address decoder is used to enable display latch, control panel buffer and symbol panel buffer. The block diagram of their device is shown in the below Figure. Also, In their control panel and symbol panel key pad, encoders are used to encode key stroke. As they are using mechanical switch, the circuit generates incorrect encoded value because of contact bouncing. A Mono stable Multi vibrator IC is used to prevent contact bounce. A Counter is used to indicate new data has arrived.

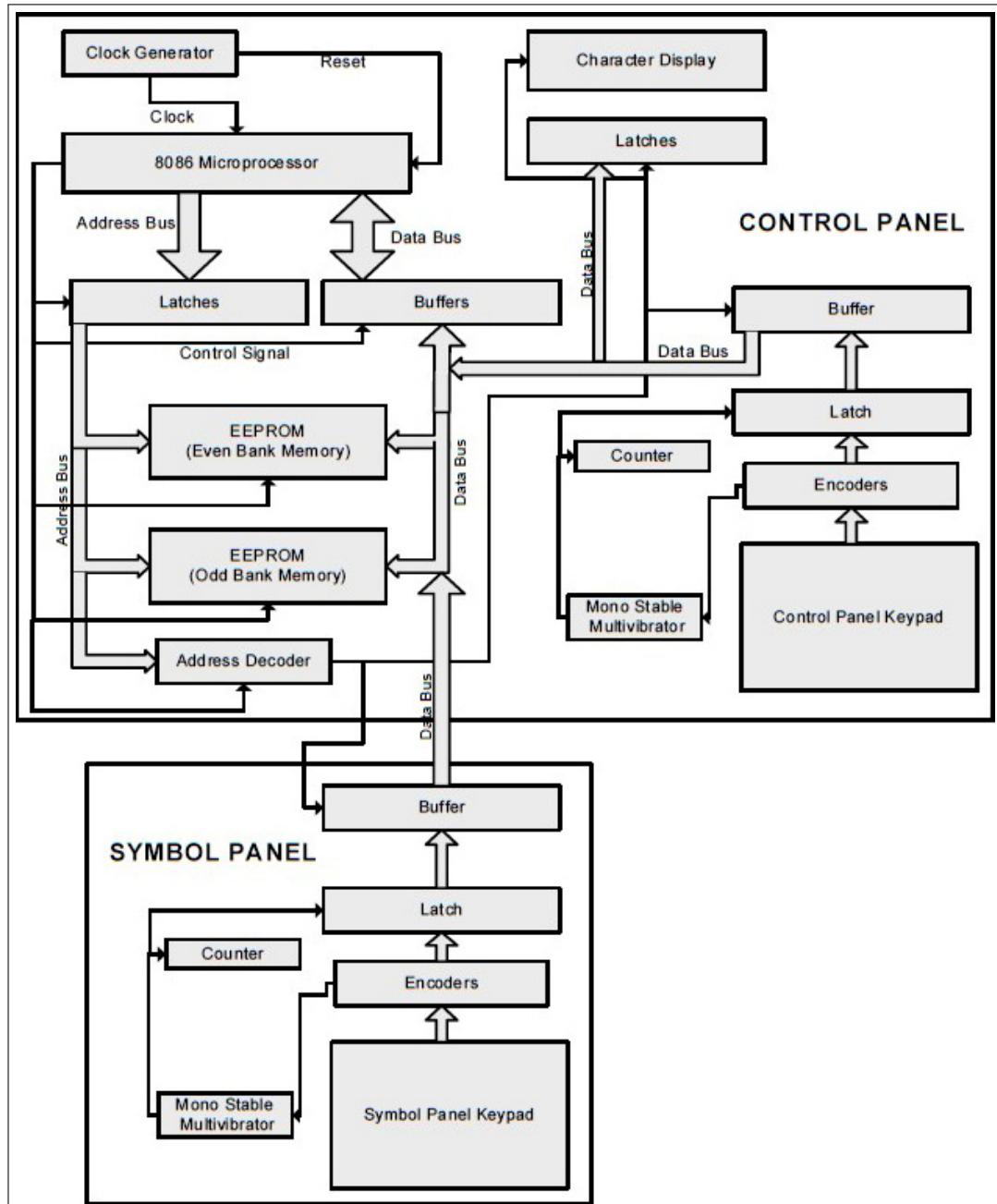


Figure 2.1: Block diagram of Electronic Voting Machine

[2] **Jordi Cucurull etc. al.**, had presented a study named “QR Steganography: A Threat to New Generation Electronic Voting Systems”. In this study Quick Response (QR) codes used to store machine readable information, have become very common nowadays and have found many applications in different scenarios. One of such applications is electronic voting systems. Indeed, some electronic voting systems are starting to take advantage of these codes, e.g. to hold the ballots used to vote, or even as a proof of the voting process. Nevertheless, QR codes are susceptible to steganographic techniques to hide information. This steganographic capability enables a covert channel that in electronic voting systems can suppose an important threat. A misbehaving equipment (e.g. infected with malware) can introduce hidden information in the QR code with the aim of breaking voters’ privacy or enabling coercion and vote-selling. Their paper shows a method for hiding data inside QR codes and an implementation of a QR writer/reader application with steganographic capabilities. The paper analyses different possible attacks to electronic voting systems that leverage the steganographic properties of the QR codes. Finally, they propose some solutions to detect the mentioned attacks.

Basically, their method proposed to insert hidden information in a QR code exploits the error correction capability so that it is not detected by a regular QR reader. Their design consists on replacing a certain number of code words of data in the QR code with the information to hide. When the QR is read, the replaced code words are considered as errors and are corrected by the error correction mechanism when read. In order to take full advantage from the error correction mechanism and maximise the capacity for hidden information, the modification has to be performed without altering the error correction code words.

[3] **Sahibzada Muhammad Ali etc. al.**, had presented a study named “Micro-Controller Based Smart Electronic Voting Machine System”. In their study an electronic voting machine EVM is introduced which is faster, efficient and reliable and error free as compared to manual voting system which is slower, poses full day fatigue on people and chances of error are greater. Its main feature is its ease to operate. Voter polls a vote very easily and final results are displayed in no time by just pressing a result button, after the elections have been conducted.

The main and important part of their EVM is control unit, in which the control unit keeps track of the input switches. When a vote is polled, the control unit increments the contents of the memory locations/registers reserved for the candidate polled for. It then turns ON the Busy-Lamp, indicating that

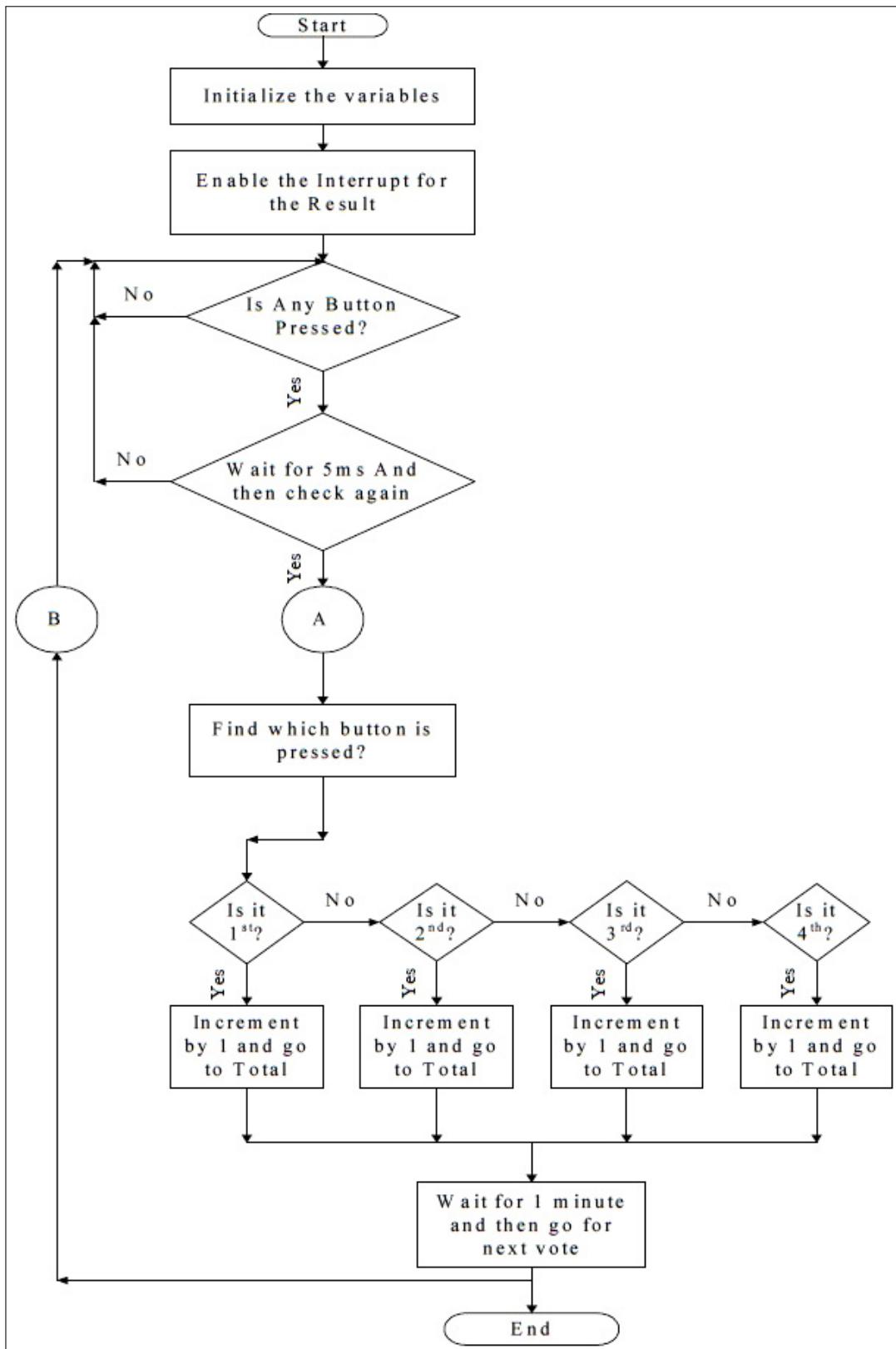


Figure 2.2: Flow Chart

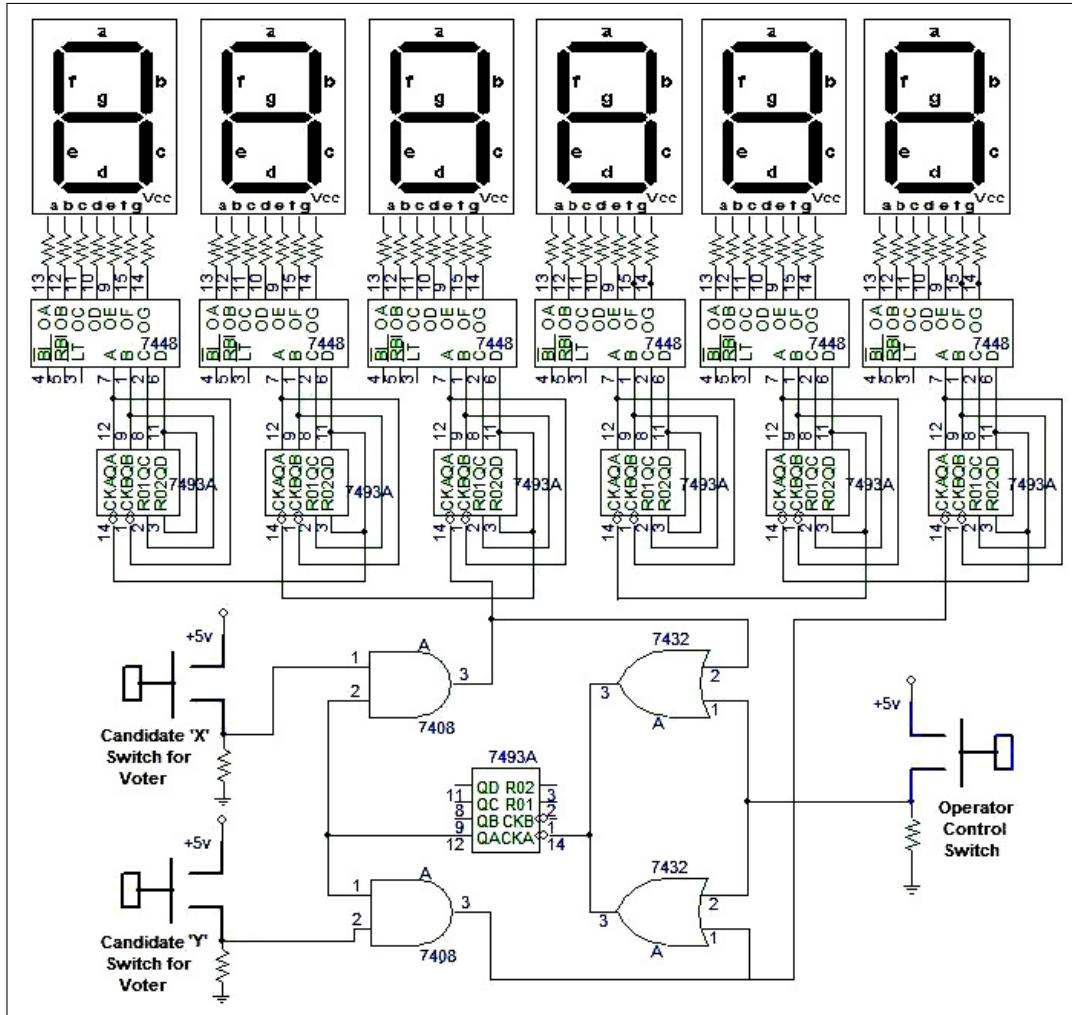


Figure 2.3: Circuit Diagram of SEVM for the position of two Candidates

all the input switches are disabled for a calculated amount of time. After the voting is over the results of voting can be seen in LCD using a button, “RESULT”, on control unit. The whole design of their system is shown with the help of below flow chart.

[4] Murshadul Hoque, had presented a paper named “A Simplified Electronic Voting Machine System”. In this paper, an Electronic Voting Machine (EVM) system is proposed which is in operation as transparent as the digital system. The Simplified Electronic Voting Machine (SEVM) responds on some flow of pulses coming from the switch operated by voter and produces the output of the counting values i.e. total casting votes of individual nominee and displays it. Their machine is controlled both automatically and manually to operate the system for successive voters and to ensure that a voter can give only one vote to his/her chosen candidate of the same position. Their manual controlling mode must be operated by presiding officer who have the authorization to check and to declare a voter valid after checking

some unique information e.g. NID number where as the automatic controlling happens whenever a voter pushes a switch to vote. Designing and implementing of their simplified electronic voting machine system is very plain and convenient due to having discrete digital circuitry.

In their specified system design, they use ‘pulses’ as the effect of a vote and count those to make the result. Some very elementary logic gates, counter and innocent switches are also used to design the simple system in its constructional and operational as well where no programmable memory element is used. The pulse, that is generated by a voter by pressing a switch which is marked with the name of a candidate in the booth, goes to drive the corresponding counter and display units. The operator-control unit controls to allow the voter to vote, to transmit the pulse to automatic control unit and to enable the counting and display units. The whole overview of their proposed design is depicted by the following Figure

[5] Rahil Rezwan etc. al., had presented a study named “Biometrically Secured Electronic Voting Machine”. In this study of project, they have developed a system which will be suitable for elections in countries like Bangladesh. The usual system for voting in Bangladesh is ballot paper-based voting system, where voting is sometimes unfair. In this proposed system they have used Arduino and Finger Print Scanner that can identify each voter, count votes and can prevent fake votes. The proposed system is more digital, technology-based and secured system.

In this design, the system is able to identify each voter by getting their fingerprint. Whenever the system will receive a fingerprint, it will match the fingerprint from the database. According to the information given by the database, the system will decide if the person is registered or not. System is also able to distinguish second vote. If a particular voter is not registered voter or tries to cast more than one vote, system will identify him and will restrict from voting. However, if neither case is applicable for a voter, it will allow the voter to cast the vote. The system is designed in such a way, if vote is given to a candidate mistakenly, the voter has the ability to change their decision but only once. Furthermore, just like any other electronic voting machines, the device will count votes for each candidate. It is also able to show the result, after a certain period of time when the voting is over. The controller unit of their whole design is Arduino UNO R3 which is an open source micro controller. Also, the Fingerprint scanner module used for their project is GT 511C3 from ADH-Tech. This module is able to capture fingerprint, save it, manipulate it, match fingerprint with the database. The whole overview of their proposed design

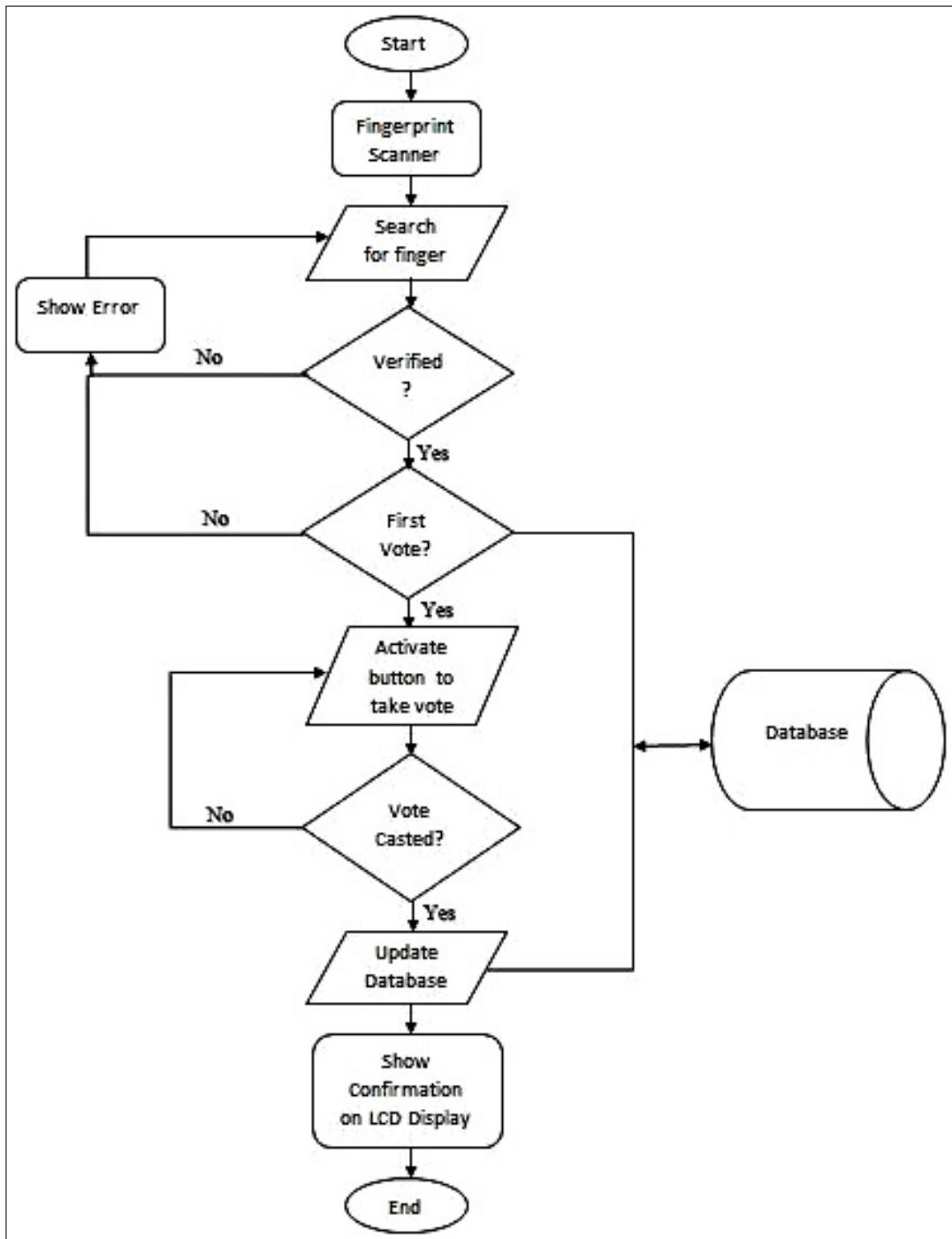


Figure 2.4: Flowchart of the Biometrically Secured EVM

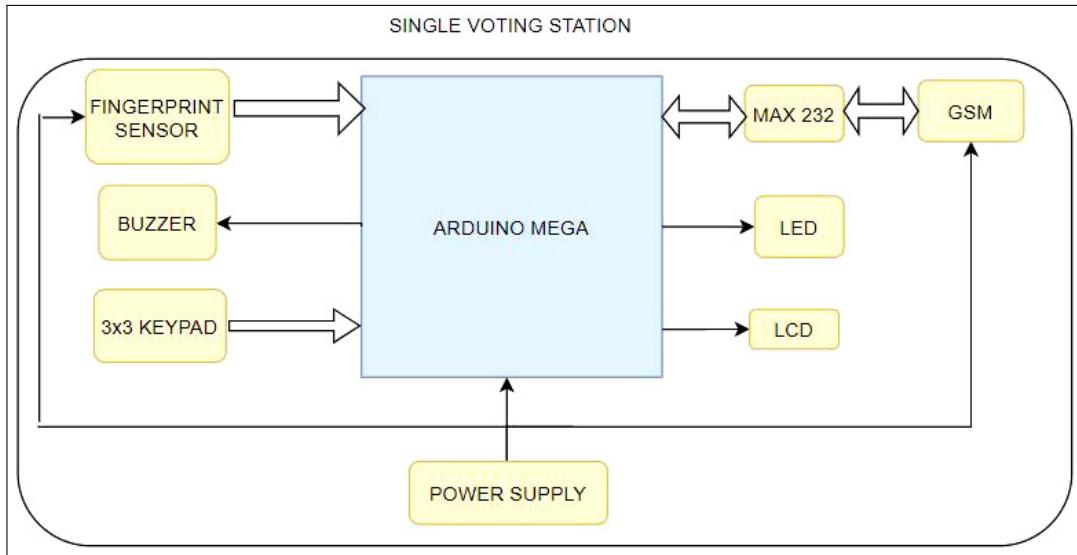


Figure 2.5: Proposed system blocks of voting station

is depicted by the following Flowchart

[6] Ravindra P. Rajput etc. al., had presented a study named “Design and implementation of convenient and compulsory voting system using finger print sensor and GSM technologies”. In their study the existing voting system, doesn’t have person identification, so that there are chances to misuse the others rights. Fingerprint based authentication for voting is proposed in this paper, which eliminates the misuse in voting. GSM module is incorporated with finger print sensor to collect the data before election. Their proposed model is implemented in Arduino for effective authentication and quick process with more flexibility.

In their proposed designed, the voters are informed to place their fingers on the fingerprint reader. The finger print reader senses the ID and sends this information to the arduino. After receiving the ID the arduino checks for authorization, if its fingerprint is valid then this person is allowed to vote. Keypad or switches is used for selecting the voting preferences. After selecting voting preference, the LED will be turned on for the particular key or switch pressed. After the voting done for the day, the controller calculates the total votes for that day. The whole overview of their proposed design is depicted by the above Figure

Chapter 3

METHODOLOGY & SYSTEM DESIGN

3.1 Methodology

Methodology is the systematic, theoretical analysis of the methods applied to a field of study. The aim of this chapter is to give an introduction about the general research methodology and waterfall methodology for development used in this project.

3.1.1 Research Purpose

In the information age, it seems that the application of digital electronic is an in-dispensable tendency for the evolution of organizations in 21st century, regardless of public or private organizations. The application of digital technology into public affairs briefly includes the electronic democracy, which is governance-oriented, and e-government, which is service-oriented. Electronic Voting being a vital part of the services being offered by e-Government would lead the application of digitization to improve the efficiency of public sector obviously and the participation of the citizen through the electronic forum.

The purpose of this research is to

3.1.2 Research Approach

There are two main research approaches used in scientific work, quantitative and qualitative. The main difference between these two is that the aim of quantitative research is to find explanation to a phenomenon or a situation that can be generalized to other people and places while in qualitative research

the aim is to gain deeper understanding of a phenomena or a situation.

3.2 Requirements Analysis & Specification

The first phase involves understanding what needs to design and what is its function, purpose, etc. Here, the specifications of the input and output or the final product are studied and marked.

3.2.1 Main Units of EVM

EVM consists of mainly two interconnected units- (A) Control Unit (CU) and (B) Ballot Unit (BU) with a cable for connecting it with the Control Unit. Here, the Ballot Unit caters up to 16 candidates.

BALLOT UNIT

- The Ballot Unit is that unit of the machine which the voter operates to exercise his vote.
- It consists of a rectangular box. The box, which is as shown in **Fig. 3.1** has -
 1. **Interconnecting Cable**:- The interconnecting cable is used to connect Ballot unit and Control Unit; one end of which is permanently attached to the Ballot Unit, but its other end is attached to the Data Buffer from where it is further used for connecting it to the Control Unit.
 2. **Ready Lamp**:- The ‘Ready Lamp’ is on the top side of the Ballot Unit. This lamp glows GREEN when the ‘Ballot’ button on the Control Unit is pressed by the Presiding Officer to enable the voter to cast his/her vote. It goes off when the voter has cast his/her vote.
 3. **16 Candidates’ Buttons**:- The voter records his/her vote by pressing the candidate’s button against the name and symbol of the candidate of his/her choice.
 4. **16 Candidates’ Lamps**:- When the button is pressed, the candidate’s lamp on the left side of that button glows RED, to notify the voter that his/her vote was successfully recorded.

CONTROL UNIT

- The Control Unit controls the polling process. It is operated by the Presiding Officer or the first Polling Officer.

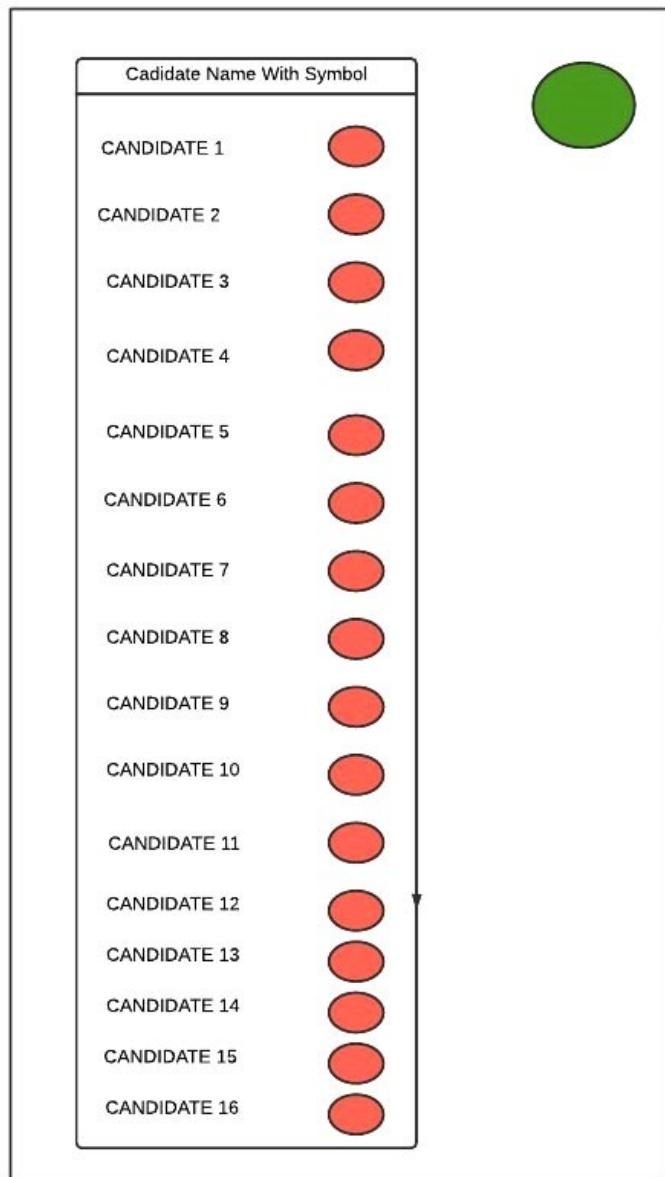


Figure 3.1: Ballot Unit

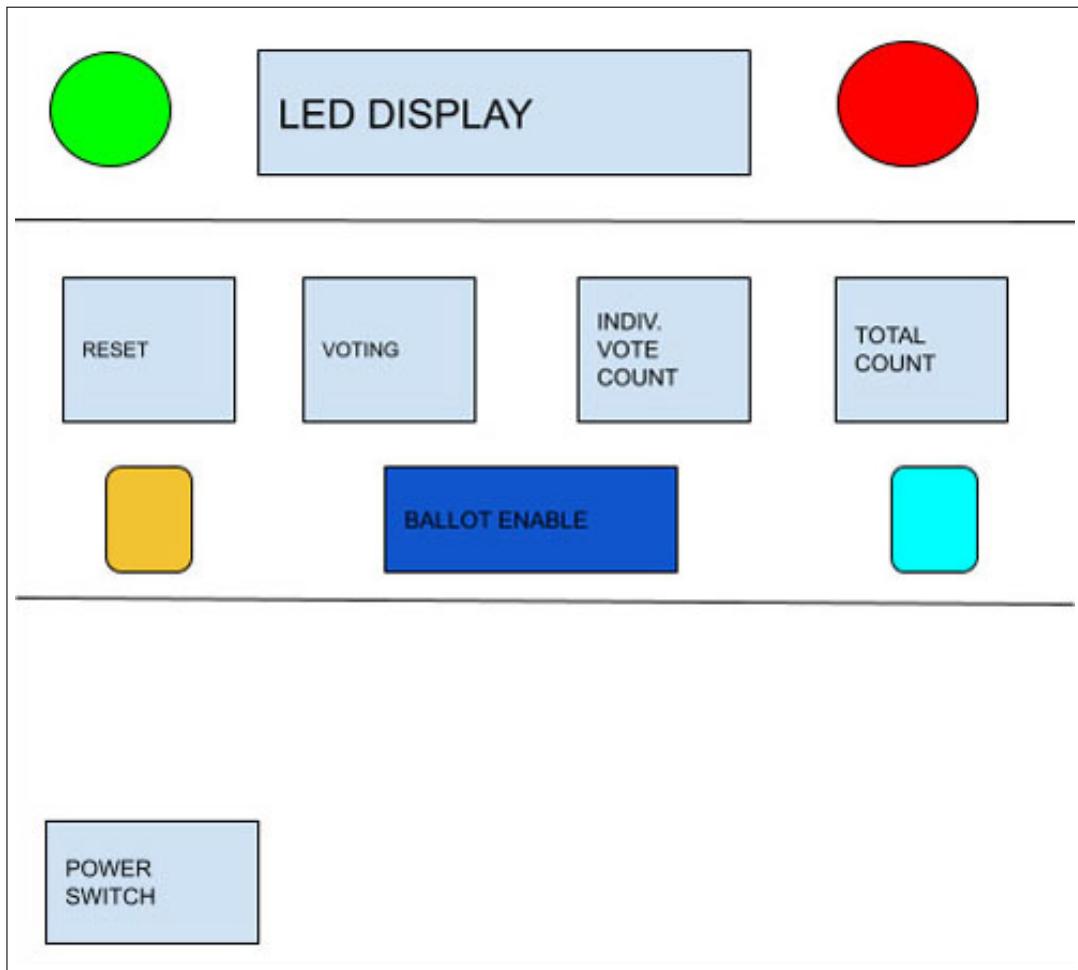


Figure 3.2: Control Unit

- Here, the Control Unit consists of -

1. **Display Section:**- Display section consists of two lamps ‘On’ and ‘Busy’ and a display panel, which are as shown in Fig. 3.2 -

- (a) The ‘ON’ lamp is located at the top left corner of the display section. When the power switch is pushed upwards to the ‘ON’ position, the Lamp glows ‘GREEN’ to indicate that the EVM is ready for use.
- (b) The red ‘Busy’ Lamp is located at the top right corner of the display section. It glows RED when the ‘Ballot’ button is pressed by the polling official to enable the ballot unit for the voter to cast his/her vote. It goes off when the voter has cast his/her vote, which is used to indicate to the presiding officer that the voter has cast his/her vote.
- (c) The display panel is used for displaying the RESULT.

2. **Mode Selection Section:**- There are four different modes in our EVM, for which the presiding officer has to select a particular mode to be operated. The modes are given below

-
- (a) Voting mode.
- (b) Reset mode.
- (c) Individual candidate vote counting mode.
- (d) Total vote counting mode.

3. **Reset Button:**- While in Reset mode, the ‘Reset’ button is required to be pressed before the start of a POLL for clearing the memory and showing that no votes are already recorded in favors of any candidate.

4. **Ballot Enable Button:**- This Ballot Enable Button is operational in two modes (Voting Mode & Individual candidate vote counting mode).

- (a) While in Voting Mode, the ‘Ballot Enable’ button has to be pressed, for enabling a voter to record his/her vote. When this button is pressed, the ‘Busy’ lamp in the Control Unit and the ‘Ready’ lamp in the Ballot Unit will start glowing and will continue to glow until the voter records his/her vote. This button will again become operational for the next voter only when the earlier voter has recorded his/her vote.

- (b) While in Individual Candidate Vote Counting Mode, the ‘Ballot Enable’ button has to be pressed, for enabling the presiding officer to select the candidate for he/she wishes to see the result. When this button is pressed, the ‘Busy’ lamp in the Control Unit and the ‘Ready’ lamp in the Ballot Unit will again start glowing and will continue to glow until the officer records his/her choice of candidate. This button will again become operational for officers only when the earlier candidate results are displayed in the display panel.
5. **Total Count Button**:- The ‘Total’ button, when pressed will show the total number of votes recorded till then. This button may be pressed at any time after a voter has recorded his/her vote or before the ‘Ballot’ button is pressed to enable him/her to record his/her vote, but not when the ‘Busy’ lamp is ON.
6. **Power Switch**:- To switch ON the EVM, the ‘Power’ switch is to be pushed upwards to the position marked ‘ON’.

3.2.2 DESIGN DESCRIPTION

This section[7] should provide the reader with all the information necessary to repeat the work. Our voting machine works as same as electronic voting device. But there is a little bit change we made on our voting machine. .We use four different steps for our design and these are -

Firstly we have to prepare our proposed system or design specification. From our design specification we write RTL Description with the help of Algorithmic state machine (ASM Chart), Finite State Machine (FSM Design) & State Table. From RTL Description we go to Verilog code of our design. Finally we verify and simulate our design using verilog code.

If we fail to fulfil one step, next step does not work. Though they are four different steps and work individually, they fully depend on each other. Without any of these we cannot complete our design as we want. Design flow diagram is given below -

Our Electronic Voting Machine (EVM) works in two major units- Control Unit and Ballot Unit. Here, The control unit counts the individual party results as well as the total vote counts. Whereas the ballot unit makes a beep sound and gives a green signal when a cast vote is accepted.

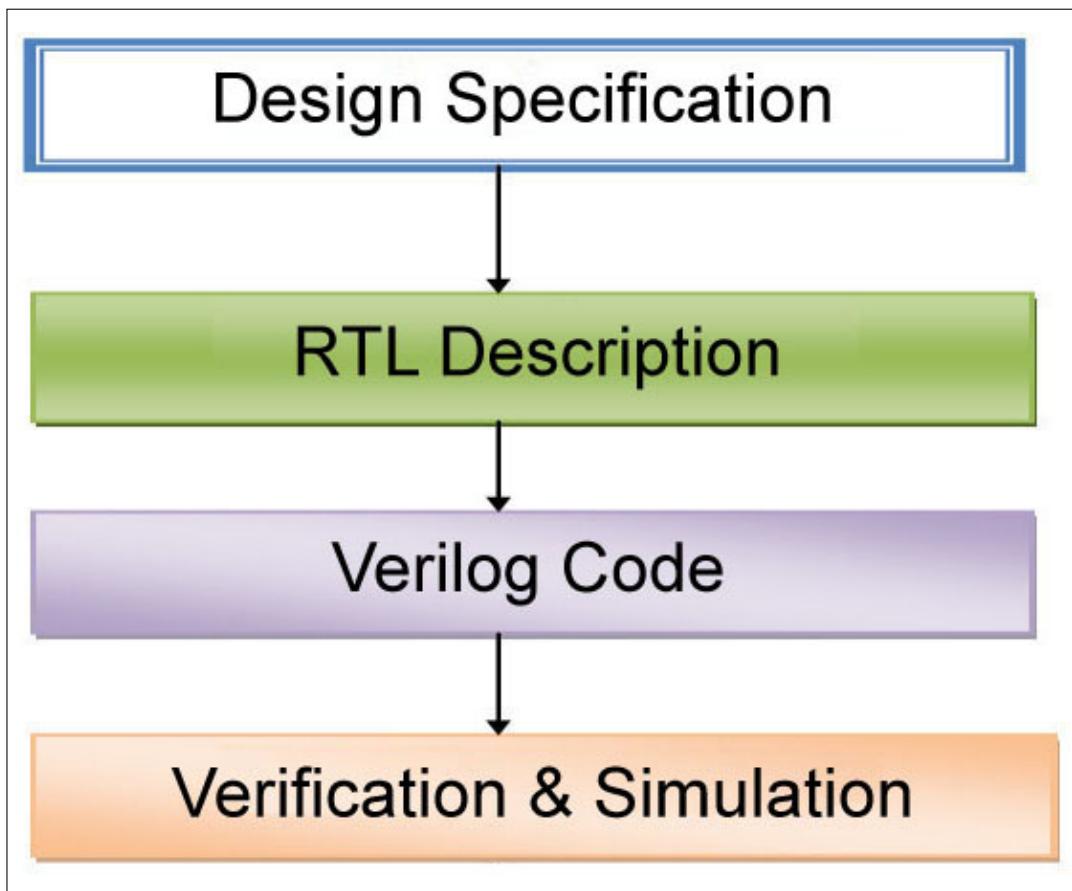


Figure 3.3: Design Flow Diagram

3.2.3 Design Specification

The design specification consists of three stages; in the first stage we decide the total number of voters and the total number of contestants taking part in the election process. We have assigned Voting enable which is active high input signal for the voter in order to cast his vote by using voter switch input signal for making this election process more secure and safe. In stage two, voting process begins when the voter casts his vote to a particular party or contestants the polled vote is registered in the individual contestant registry. In stage three after completion of voting process the votes are validated by comparing the votes polled to the contestants with their registries after which the election process ends. The above proposed method can be verify and simulate using verilog as it has the advantage that it can be reprogrammed over and over for different tasks, making them very cost efficient by avoiding recurring expenses.

3.2.4 RTL Design

In digital circuit design, Register Transfer Level (RTL) is a design abstraction which models a synchronous digital circuit in terms of the flow of digital signals (data) between hardware registers, and the logical operations performed on that signals. Register-transfer-level abstraction is used in hardware description languages (HDLs) like Verilog and VHDL to create high-level representations of a circuit, from which lower-level representations and ultimately actual wiring can be derived.

Also, In RTL Design the basic building blocks are registers, Multiplexers & Adders. Here, it allows us to synthesize complex circuits with a large number of States with much more ease as compared to Sequential Logic Design.

3.3 Hardware Description Block Diagram

A block diagram is a graphical representation of a system which provides a functional view of a system. Block diagrams give us a better understanding of a system's functions and help create interconnections within it. Block diagrams derive their name from the rectangular elements found in this type of diagram. They are used to develop and describe hardware or software systems as well as represent their workflows and processes. Block diagrams are described and defined according to their function and structure as well as their relationship with other blocks. Here, block diagrams are used for visualization of informa-

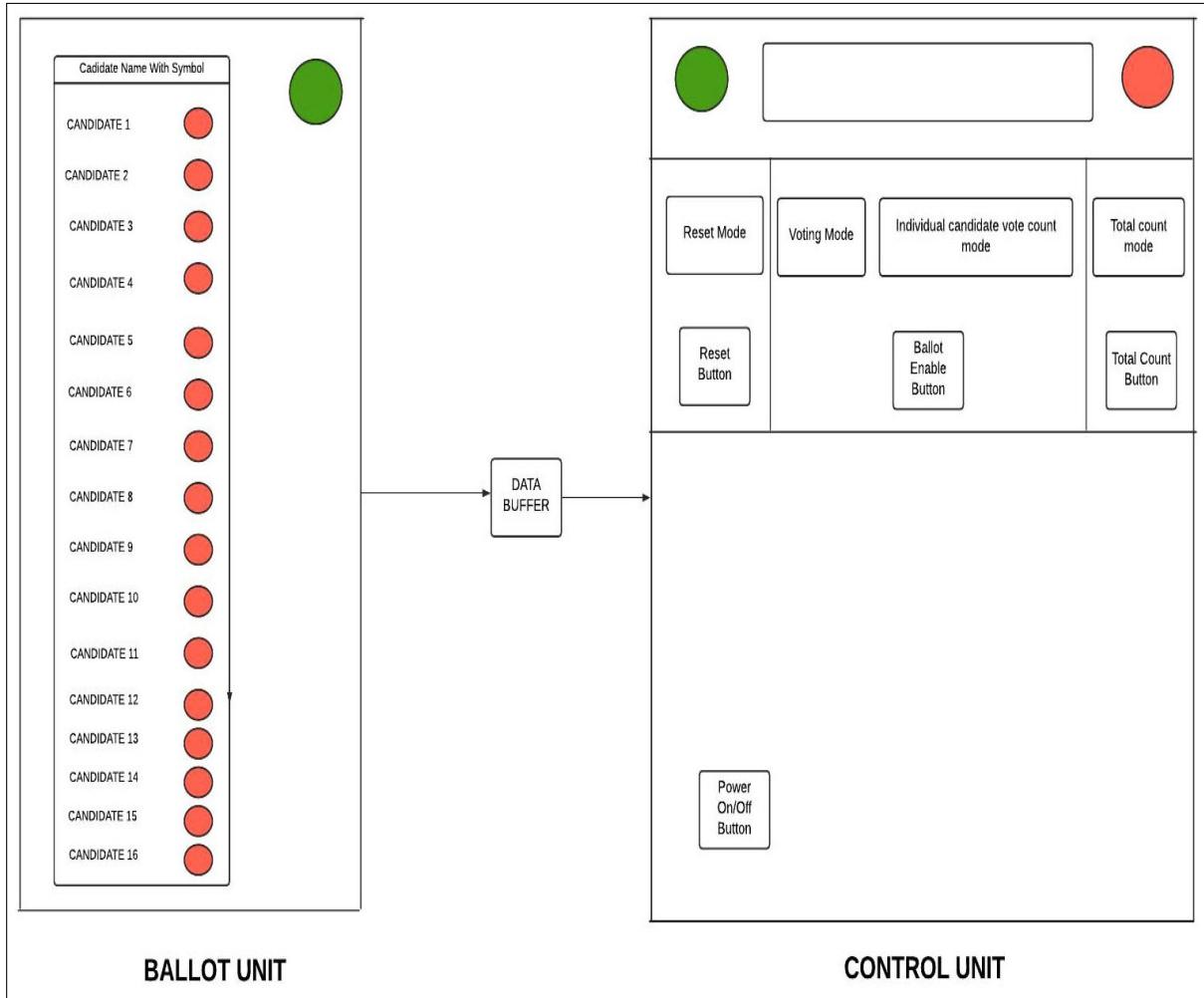


Figure 3.4: Block diagram of EVM

tion or control flows, and In this way we can represent complex algorithms or flows of information or communication among individual components within a large system as with.

3.4 DATAPATH DESIGN

A datapath is a collection of functional units such as arithmetic logic units or multipliers that perform data processing operations, registers, and buses. Datapath for each step is set up by control signals that again set up dataflow directions on communication buses and select ALU and memory functions. Control signals are generated by a control unit consisting of one or more finite-state machines.

3.4.1 During Reset Mode

In VLSI design, reset function is normally included in order to bring the logic into a predefined known

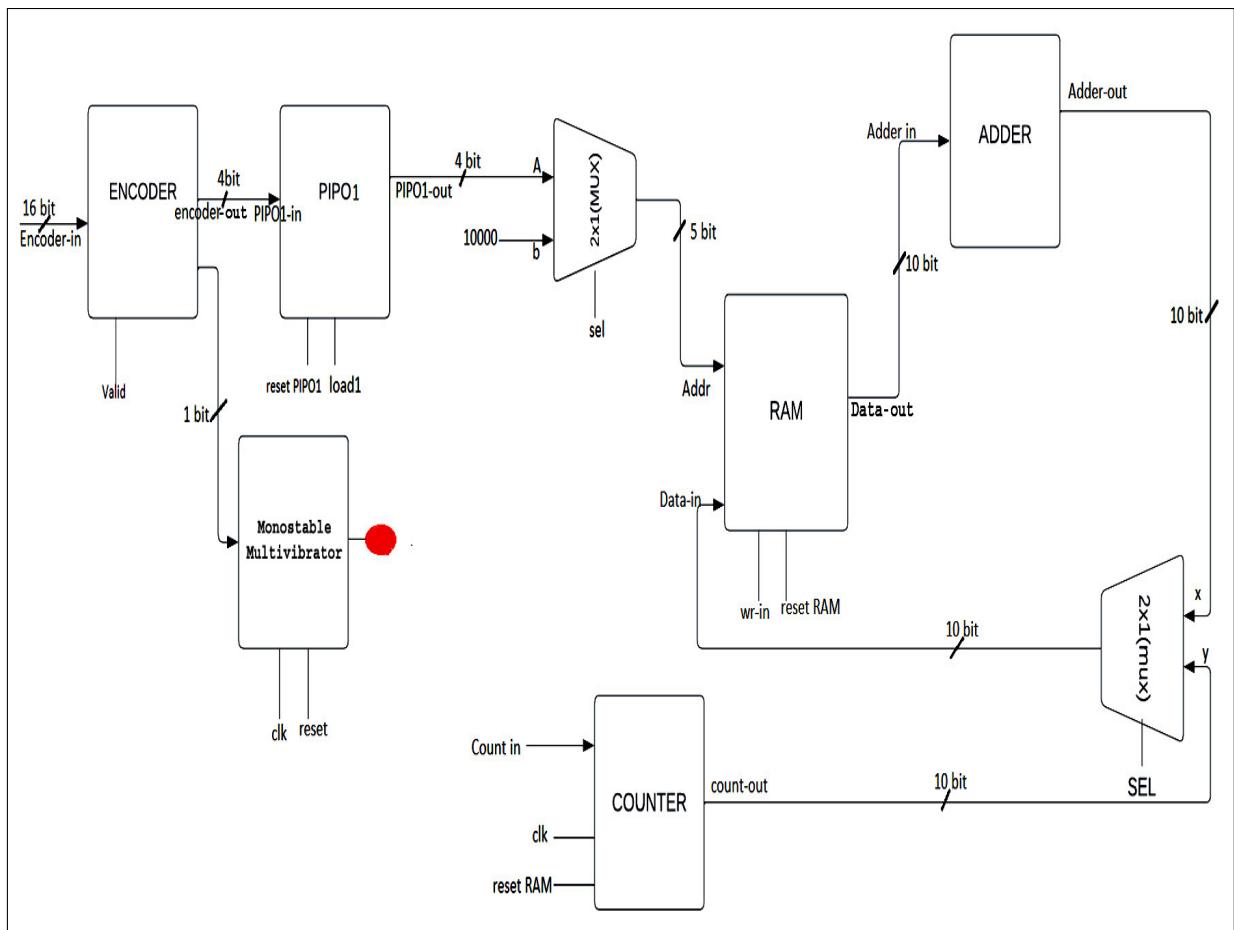


Figure 3.5: Block diagram of Datapath Design

state after power-up. Reset is mostly required for the control logic and may be eliminated from the data path logic, reducing logic area. Reset may be either synchronous or asynchronous relative to the clock signal.

3.4.2 During Voting Mode

3.4.3 During Individual Counting Mode

3.4.4 During Total Counting Mode

3.5 Algorithmic State Machine (ASM Chart)

ASM Chart is a special type of flow chart that is used to describe the sequential operations of a digital circuit. It determines the sequence of events, timing relationship between the states of sequential controller and the events that happen while going from one state to another. An ASM chart consists of an interconnection of four types of basic elements: state name, state box, condition checks, and conditional outputs. Basically, it can be divided into three blocks namely the state box, the decision box, and the conditional output box.

3.6 Finite State Machines (FSM chart)

Finite state machine (FSM) is a term used by programmers, mathematicians, engineers and other professionals to describe a mathematical model for any system that has a limited number of conditional states of being. Mainly, a system where particular inputs cause particular changes in state can be represented using finite state machines. A finite state machine has a set of states and two functions called the next-state and output function.

- The set of states correspond to all the possible combinations of the internal storage. If there are n bits of storage, there are 2^n possible states.
- The next state function is a combinational logic function that, given the inputs and the current state, determines the next state of the system.

Also, there are four components which exists in a finite state machine & this are given below -

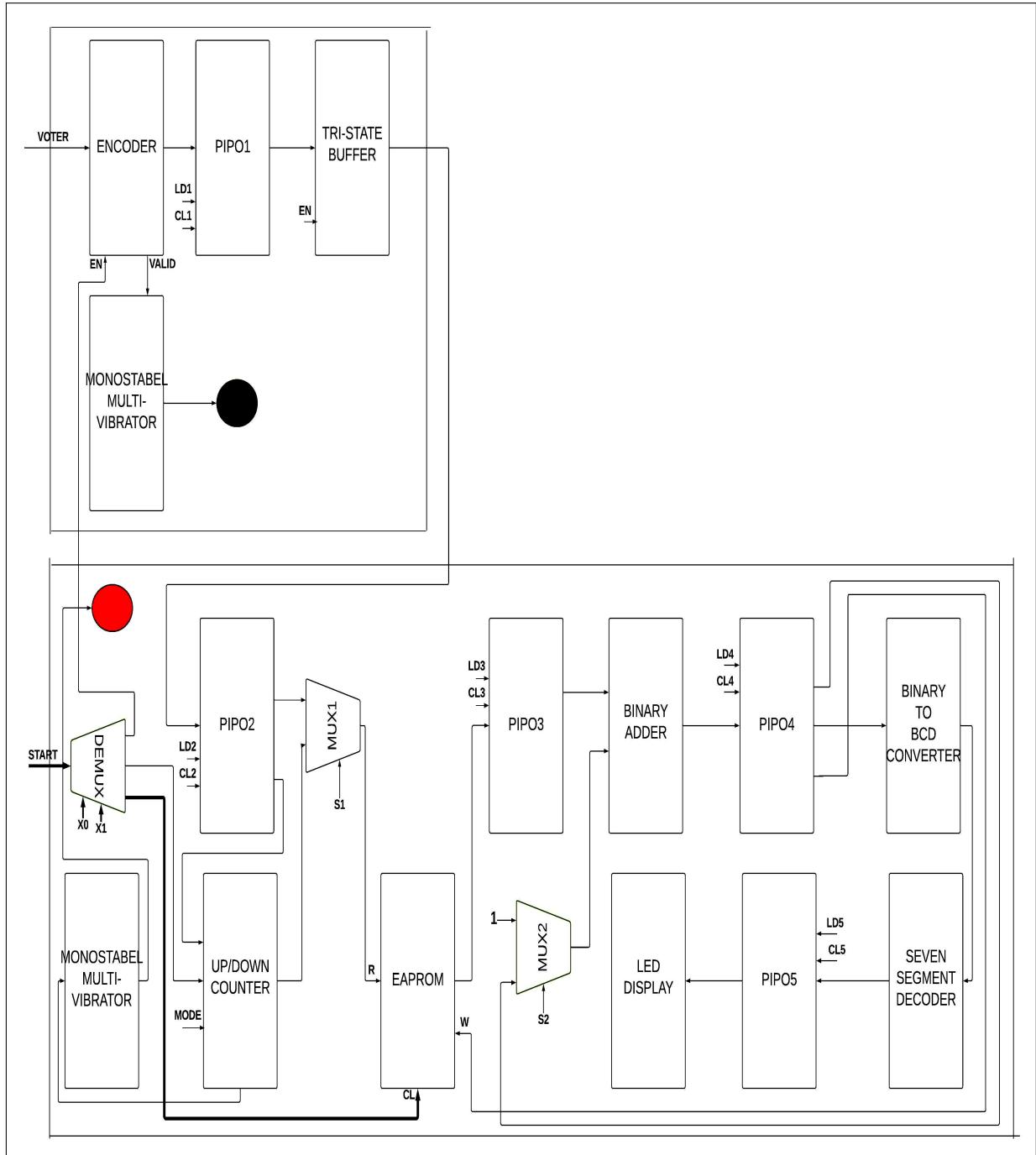


Figure 3.6: Datapath Design of Reset Mode

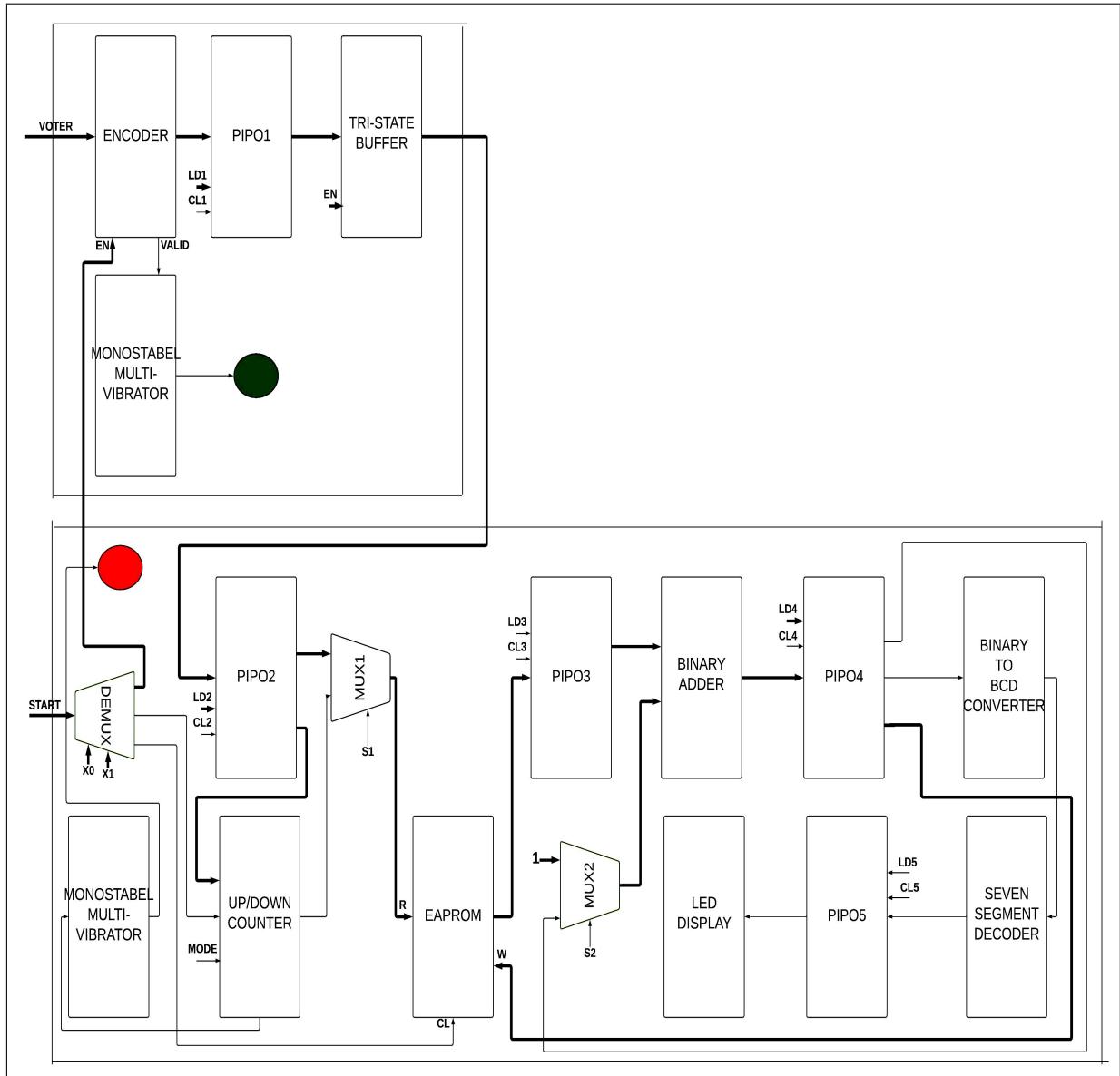


Figure 3.7: Datapath Design of Voting Mode

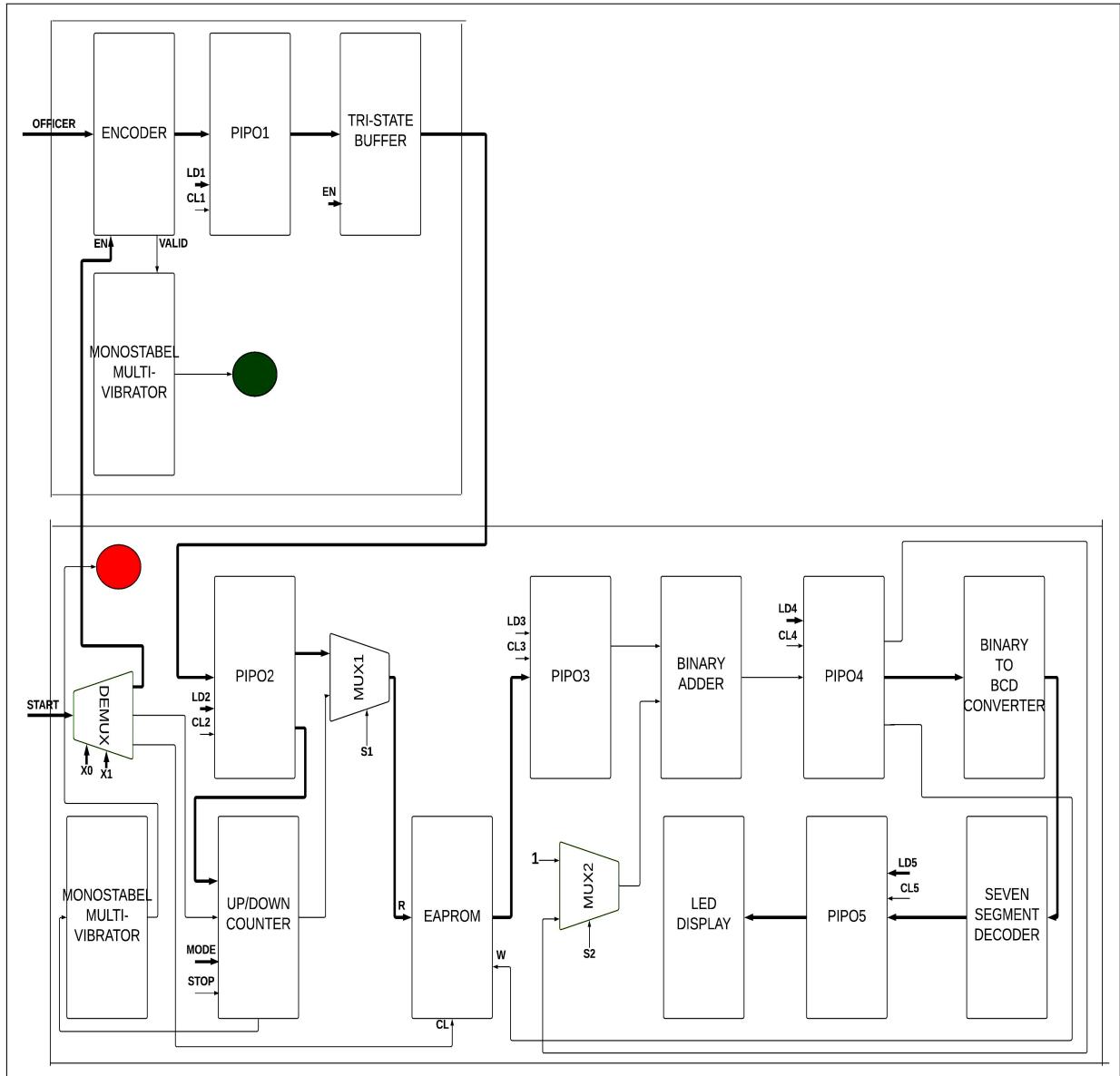


Figure 3.8: Datapath Design of Individual Counting Mode

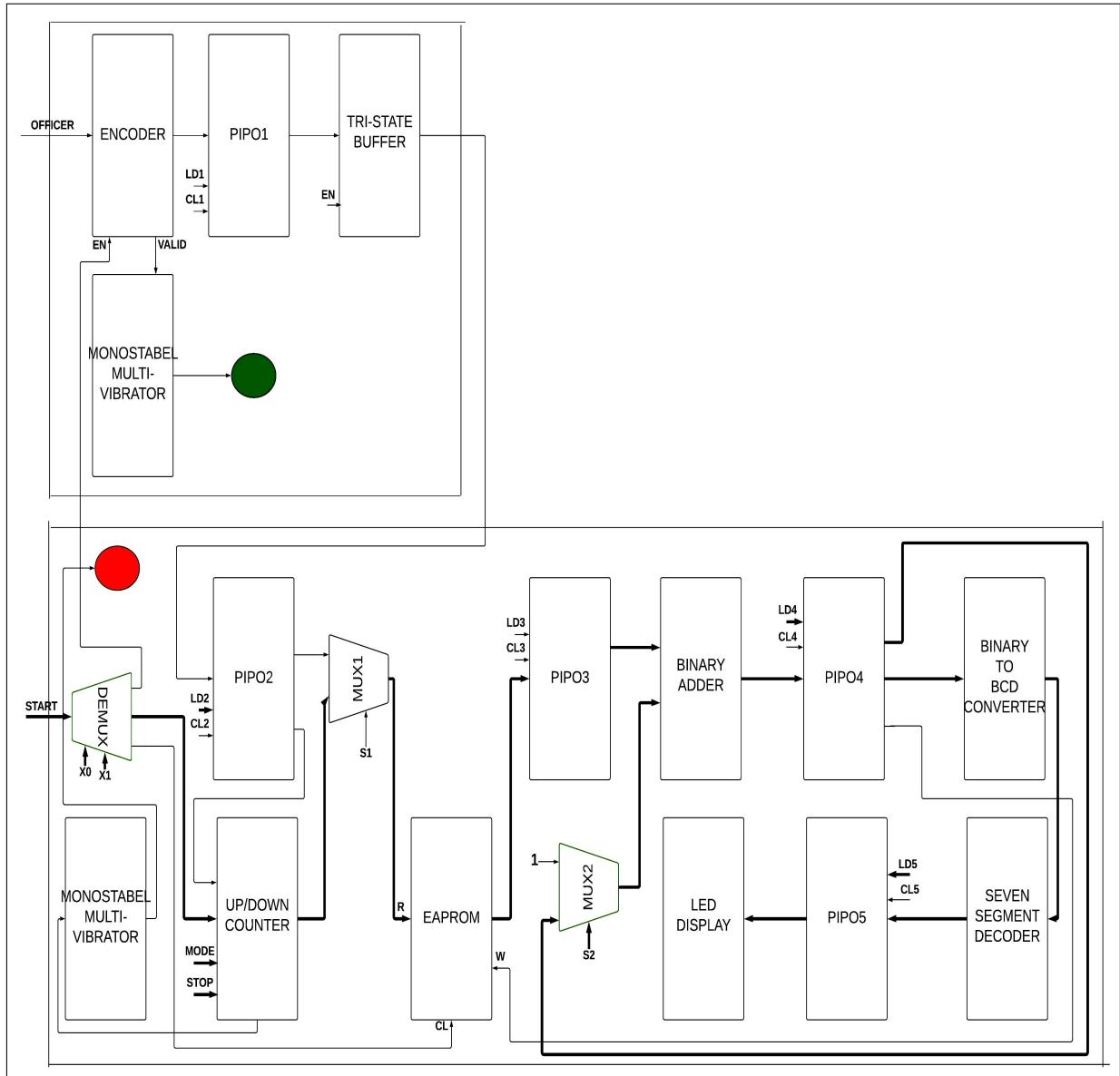


Figure 3.9: Datapath Design of Total Counting Mode

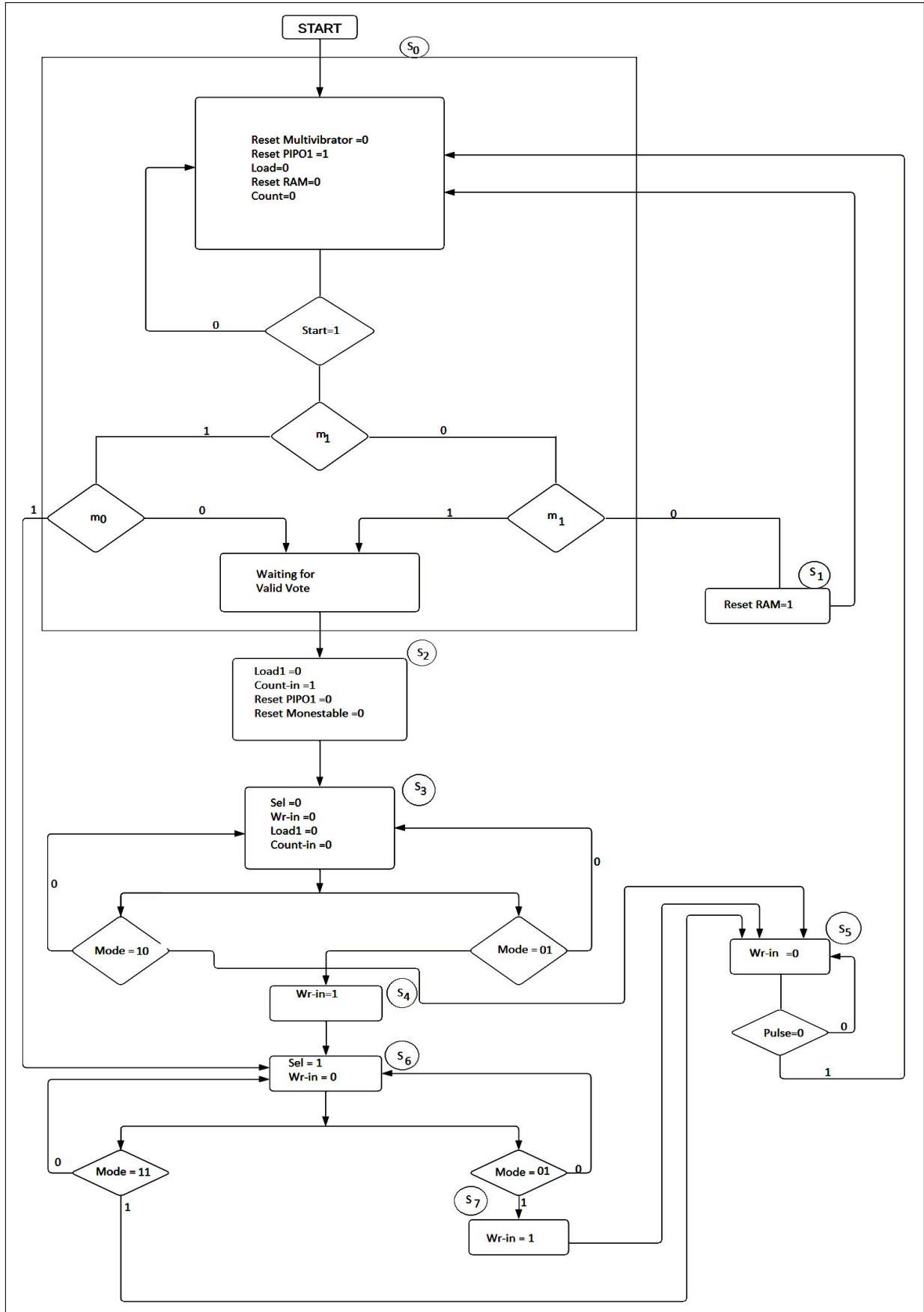


Figure 3.10: ASM Chart

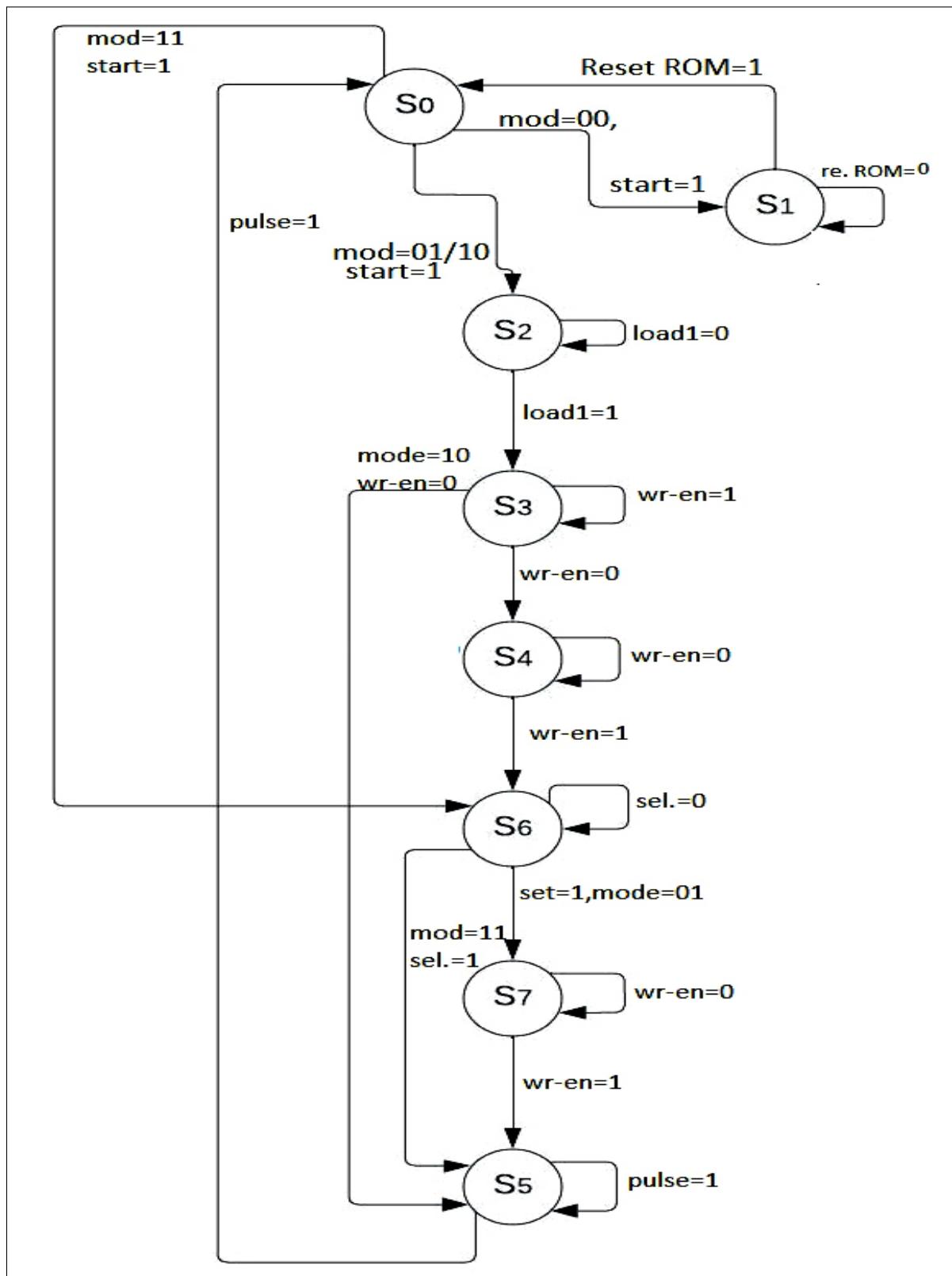


Figure 3.11: FSM Chart

State - The states are usually drawn with circles and only one state can be active at a time.

Initial State - It is the starting point of our system. Initial states are usually drawn with an arrow pointed to state.

Final state - It is a subset of known states that indicates whether the input we processed is valid or not. Accepting states are usually drawn as a double circle.

Transitions - The machine moves from one state to another and is indicated as transition. These are drawn as two states connected with a line.

3.7 State Table

The state table is a table that describes how the sequential circuits behave for the input variables and state variables. The information contained in the state diagram is transformed into the state table. Although in order to implement it in the circuit, it has to be transformed into the tabular form.

Cur re. Sta te	Q A	Q B	Q C	Mo de	St art	Enab Lin	Pul se	Q A+	Q B+	Q C+	Res et	Mu lt.	Res et PIP O1	Res et RA M	Res et d1	Loa d1	S el	WR En	Coun t.In	Ne xt Sta te
S0	0	0	0	00	0	X	X	0	0	0	1	1	0	0	0	0	0	0	S0	
S0	0	0	0	00	1	X	X	0	0	1	1	1	0	0	0	0	0	0	S1	
S0	0	0	0	01	0	X	X	0	0	0	1	1	0	0	0	0	0	0	S0	
S0	0	0	0	01	1	0	X	0	0	0	1	1	0	0	0	0	0	0	S0	
S0	0	0	0	01	1	1	X	0	1	0	1	1	0	0	0	0	0	0	S2	
S0	0	0	0	10	0	X	X	0	0	0	1	1	0	0	0	0	0	0	S0	
S0	0	0	0	10	1	0	X	0	0	0	1	1	0	0	0	0	0	0	S0	
S0	0	0	0	10	1	1	X	0	1	0	1	1	0	0	0	0	0	0	S2	
S0	0	0	0	11	0	X	X	0	0	0	1	1	0	0	0	0	0	0	S0	
S0	0	0	0	XX	1	X	X	1	1	0	1	1	0	0	0	0	0	0	S6	
S1	0	0	1	XX	X	X	X	0	0	0	0	0	1	0	0	0	0	0	S0	
S2	0	1	0	01	X	X	X	0	1	1	0	0	0	0	1	0	0	1	S3	
S3	0	1	1	01	X	X	X	1	0	0	0	0	0	0	0	0	0	0	S4	
S3	0	1	1	10	X	X	X	1	0	1	0	0	0	0	0	0	0	0	S5	
S4	1	0	0	XX	X	X	X	1	1	0	0	0	0	0	0	0	1	0	S6	
S5	1	0	1	XX	X	X	X	0	0	0	0	0	0	0	0	0	0	0	S0	
S6	1	1	0	XX	X	X	X	1	1	1	0	0	0	0	0	1	0	0	S7	
S7	1	1	1	XX	X	X	X	1	0	1	0	0	0	0	0	0	0	1	S5	

Figure 3.12: State Table

Chapter 4

SUB-SYSTEM DESCRIPTION

4.1 Encoder

An encoder in digital electronics is an electronic device used to convert an analogue signal to a digital signal such as a BCD code. It has a number of input lines, but only one of the inputs is activated at a given time and produces an N-bit output code that depends on the activated input.

Here, a 16:4 encoder is used which provides binary equivalent (10101010101010) of any of the asserted input signal (0110010001000001). i.e.

16 inputs : Y0, Y1, Y2,.....,Y15 and

4 outputs : A0, A1, A2, A3, A4

Here, the input, Y15 has the highest priority, whereas the input, Y0 has the lowest priority. In

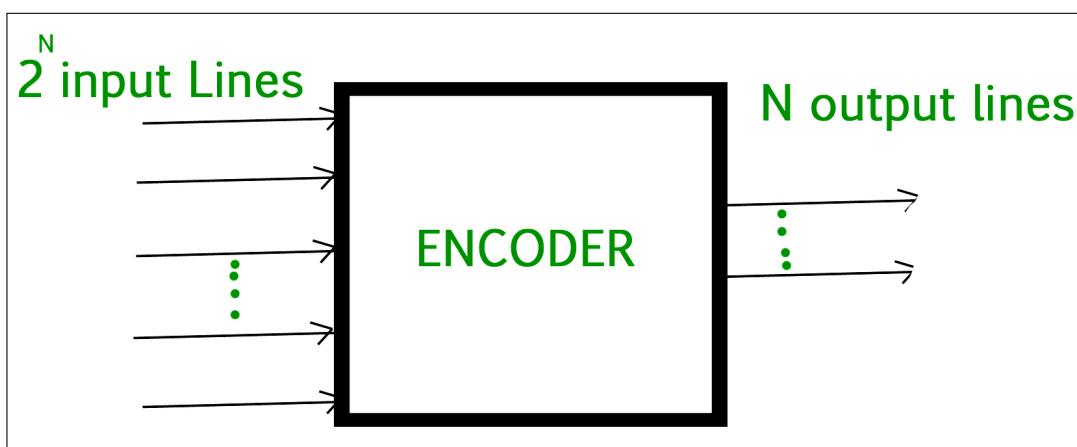


Figure 4.1: A General Encoder's Block Diagram

Y 15	Y 14	Y 13	Y 12	Y 11	Y 10	Y 9	Y 8	Y 7	Y 6	Y 5	Y 4	Y 3	Y 2	Y 1	Y 0	A3	A 2	A1	A 0	E=V
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	X	X	X	X	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	1
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	X	0	0	0	1
0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	X	X	0	0	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	X	X	0	0	1	1
0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	X	X	X	0	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	X	X	X	0	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	X	X	X	0	1	1
0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	X	X	X	0	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	X	X	X	0	1	1
0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	X	X	X	0	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	X	X	X	0	1	1
0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	X	X	X	0	1	1
0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	X	X	X	0	1	1
0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	X	X	X	0	1	1
0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	X	X	X	0	1	1
0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	X	X	X	0	1	1
1	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	1	1	1	1

Figure 4.2: Truth Table of 16:4 Encoder

this case, even if more than one input is ‘1’ at the same time, the output will be the (binary) code corresponding to the input, which is having higher priority. A general block diagram of encoder’s and the truth table of 16:4 encoder is shown above.

4.2 Parallel In Parallel Out (PIPO) Shift Registers

The shift register, which allows parallel input (data is given separately to each flip flop and in a simultaneous manner) and also produces a parallel output is known as PIPO shift register. Basically, Parallel In Parallel Out (PIPO) shift registers are the type of storage devices in which both data loading as well as

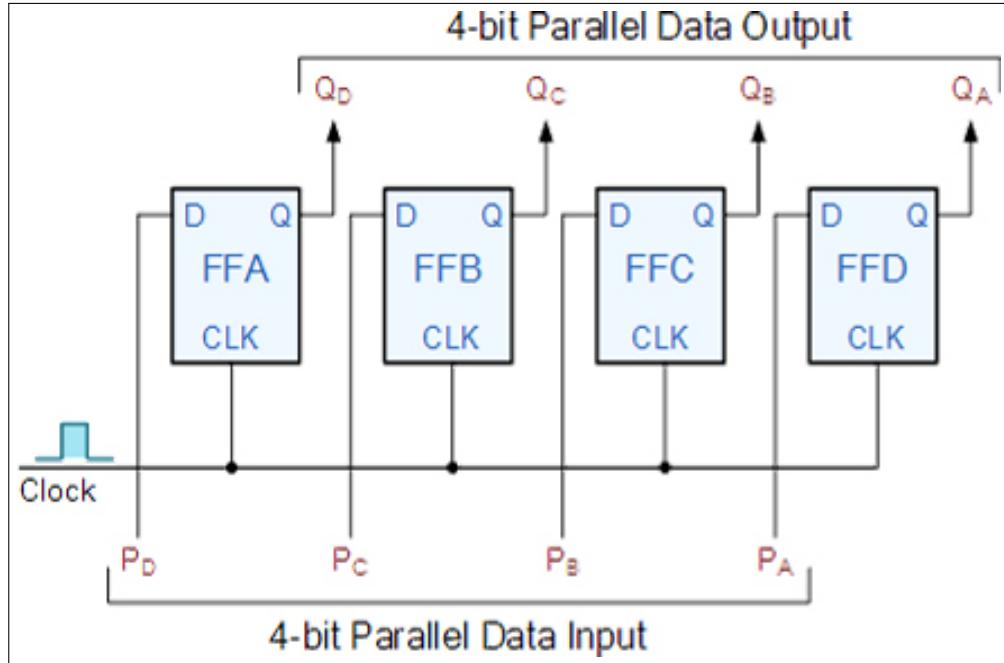


Figure 4.3: 4-bit PIPO Shift Register

data retrieval processes occur in parallel mode.

The logic circuit given above shows a parallel-in-parallel-out shift register. The circuit consists of four D flip-flops which are connected. The clear signal (Clr) and clock signals (Clk) are connected to all the 4 flip flops. In this type of register, there are no interconnections between the individual flip-flops since no serial shifting of the data is required. Data is given as input separately for each flip flop and in the same way, output is also collected individually from each flip flop.

4.3 Multiplexer

The multiplexer or MUX is a digital switch, also called as data selector. It is a Combinational Logic Circuit with more than one input line, one output line and more than one select line. It accepts the binary information from several input lines or sources and depending on the set of select lines, a particular input line is routed onto a single output line.

In our project, the 2:1 multiplexer is used which consists of two inputs D0 and D1, one select input S and one output Y. Depending on the select signal, the output is connected to either of the inputs. Since there are two input signals, only two ways are possible to connect the inputs to the outputs, so one select is needed to do these operations.

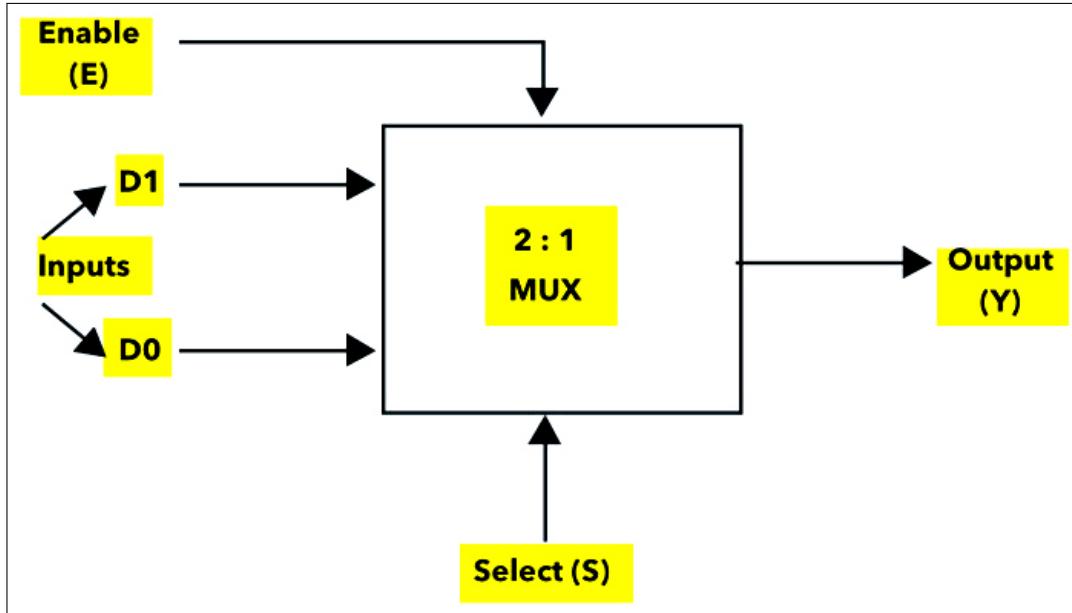


Figure 4.4: Block Diagram of 2:1 Multiplexer

Here, if the select line is low, then the output will be switched to D0 input, whereas if select line is high, then the output will be switched to D1 input. The above figure shows the block diagram of a 2:1 MUX which connects two 1-bit inputs to a common destination.

Also, the truth table of the 2:1 MUX is shown below. Depending on the value of the select input, the inputs i.e., D0, D1 are produced at outputs. The output is D0 when Select value is S = 0 and the output is D1 when Select value is S = 1, where 'X' in the below truth table denotes a don't care condition.

S	D0	D1	Y
0	0	X	0
0	1	X	1
1	X	0	0
1	X	1	1

Figure 4.5: Truth Table of 2:1 Multiplexer

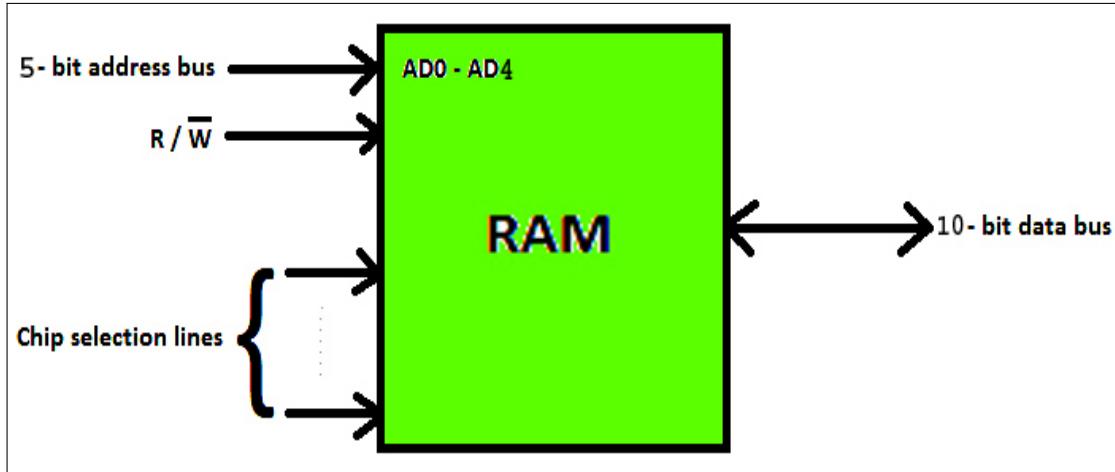


Figure 4.6: Block Diagram of RAM

4.4 Random Access Memory (RAM)

A digital processing system required the facility of storing digital information. This information is basically in the form of binary codes and data, the data or information is stored in memory. Random Access Memory is a form of semiconductor memory technology that is applied for reading and writing data in any order. It is used for such purposes as the computer or processor memory where variables and others are stored and are needed on a random basis.

Here, data can be stored and read many times to and from this type of memory. In RAM the memory location is arranged in such a way that any memory location requires equal time for reading and writing. Basically, RAM is used to Read and Write data into it which is accessed by CPU randomly. The block diagram of RAM which is used in our project is given above.

4.5 Adder

An adder is a digital circuit that performs addition of numbers, i.e. it will add together two bits and give the result as the output. In our project, we will use a specific adder which will add '1' to the input value.

4.6 Counter

Counters are specially designed synchronous sequential circuits, in which the state of the counter is equal to the count held in the circuit by the flip flops. Counters calculate or note down the number that how

many times an event occurred. These are the crucial hard ware components and are defined as ‘The digital circuit which is used to count the number of pulses’. Counters are well known to us as ‘Timers’. Counters are designed by grouping of flip flops and applying a single clock signal (Clk) to them. In simple words, the counters are those, which have the group of storage elements like flip flops to hold the count.

In our project, the counter which has a clock input signal (Clk) and a group of output signals that represent an integer ‘counts’ value. Depending upon each qualified clock edge, the circuit will increment the counts. When the counts have reached the end of the counting sequence (maximum counts when incriminating), the next clock will cause the counts to overflow and the counting sequence will start over. Internally, counters use flip-flops to represent the current counts and to retain the counts between clocks. Depending on the type of counter, the output may be a direct representation of the counts (a binary number) or it may be encoded.

4.7 Monostable Multivibrator

Generally multivibrators have two different electrical states, an output “HIGH” state and an output “LOW” state giving them either a stable or quasi-stable state depending upon the type of multivibrator. One such type of a two state pulse generator configuration are called Monostable Multivibrators. Monostable Multivibrators have only ONE stable state (hence their name “Mono”), and produce a single output pulse when it is triggered externally. Monostable Multivibrators only return back to their first original and stable state after a period of time determined by the time constant of the RC coupled circuit.

So, in oure project Monostable multivibrators can be considered as triggered pulse generators and it used to produce a time delay within a circuit as the frequency of the output signal is the same as that for the trigger pulse input the only difference being the pulse width.

Chapter 5

SYSTEM VERIFICATION & SIMULATION

5.1 16:4 Encoder

The result of the simulation observed in the GTK waveform after verifying the 16:4 Encoder by verilog code is shown in the following Figure 5.1-

5.2 Parallel In Parallel Out (PIPO) Shift Registers

The result of the simulation observed in the GTK waveform after verifying the Parallel In Parallel Out (PIPO) Shift Registers by verilog code is shown in the following Figure 5.2-

5.3 2:1 Multiplexer

The result of the simulation observed in the GTK waveform after verifying the 2:1 Multiplexer by verilog code is shown in the following Figure 5.3-

5.4 Random Access Memory (RAM)

The result of the simulation observed in the GTK waveform after verifying the RAM by verilog code is shown in the following Figure 5.4-

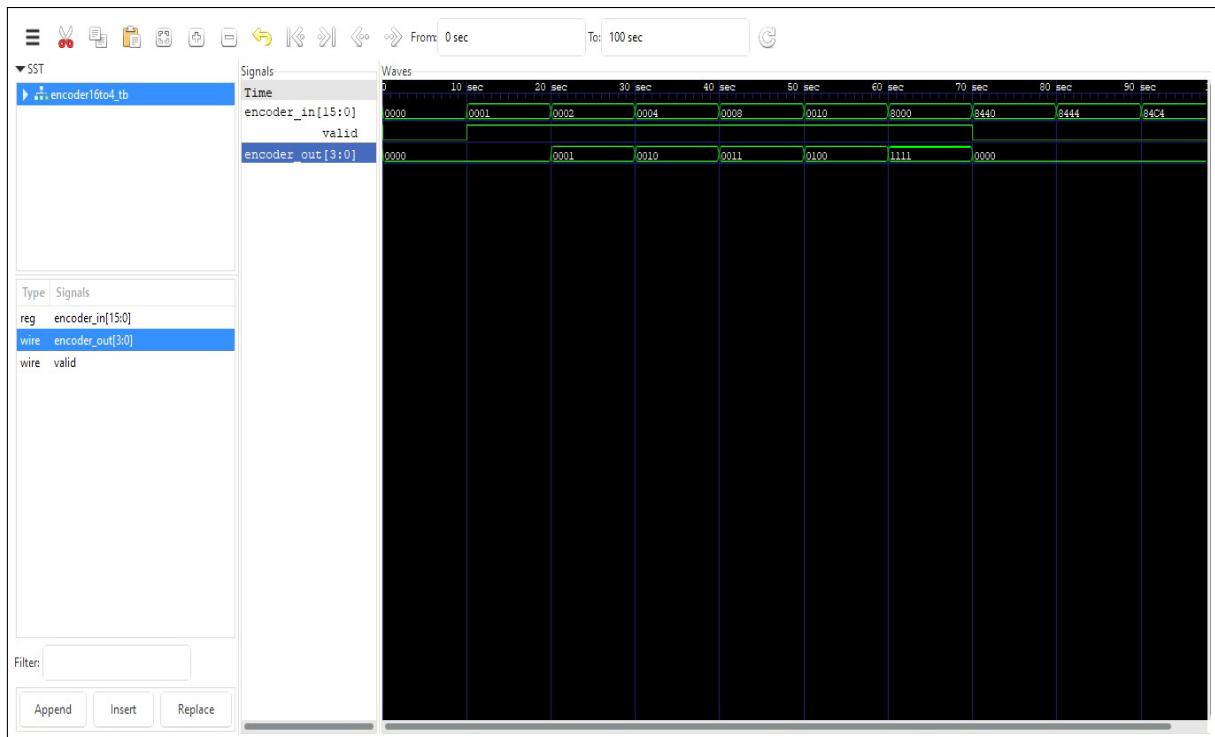


Figure 5.1: Simulation Result of 16:4 Encode

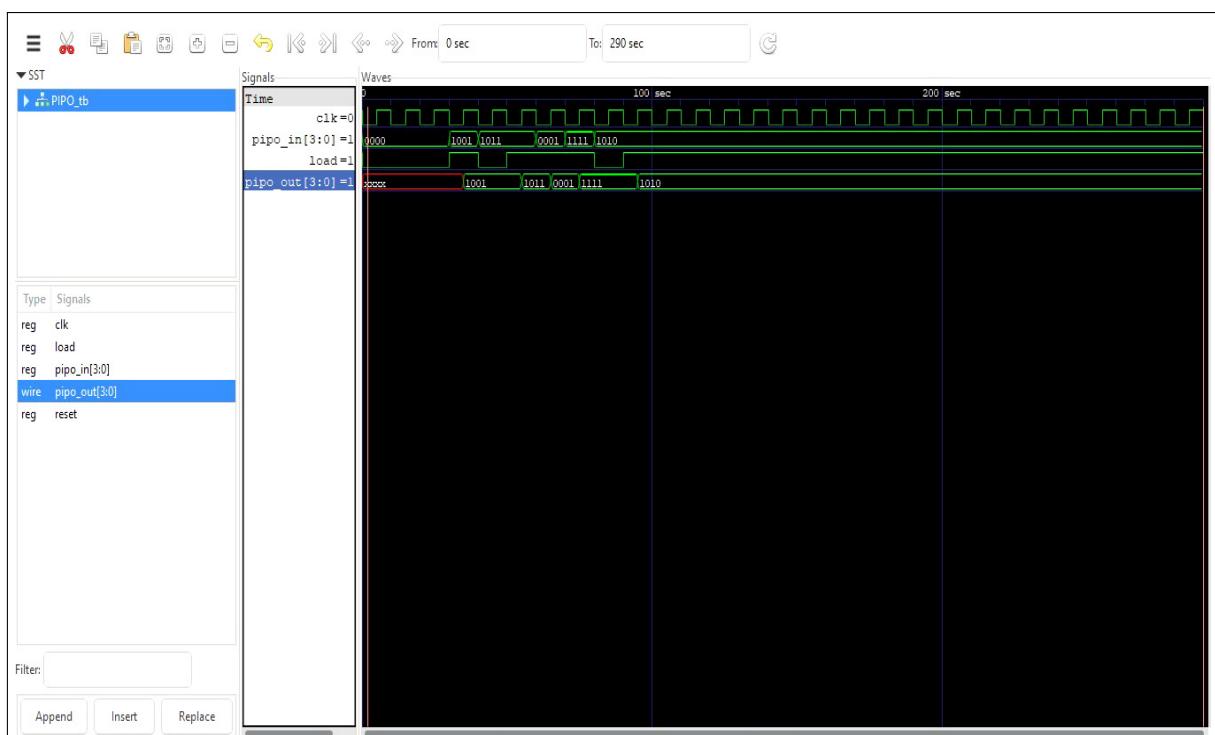


Figure 5.2: Simulation Result of PIPO Shift Registers

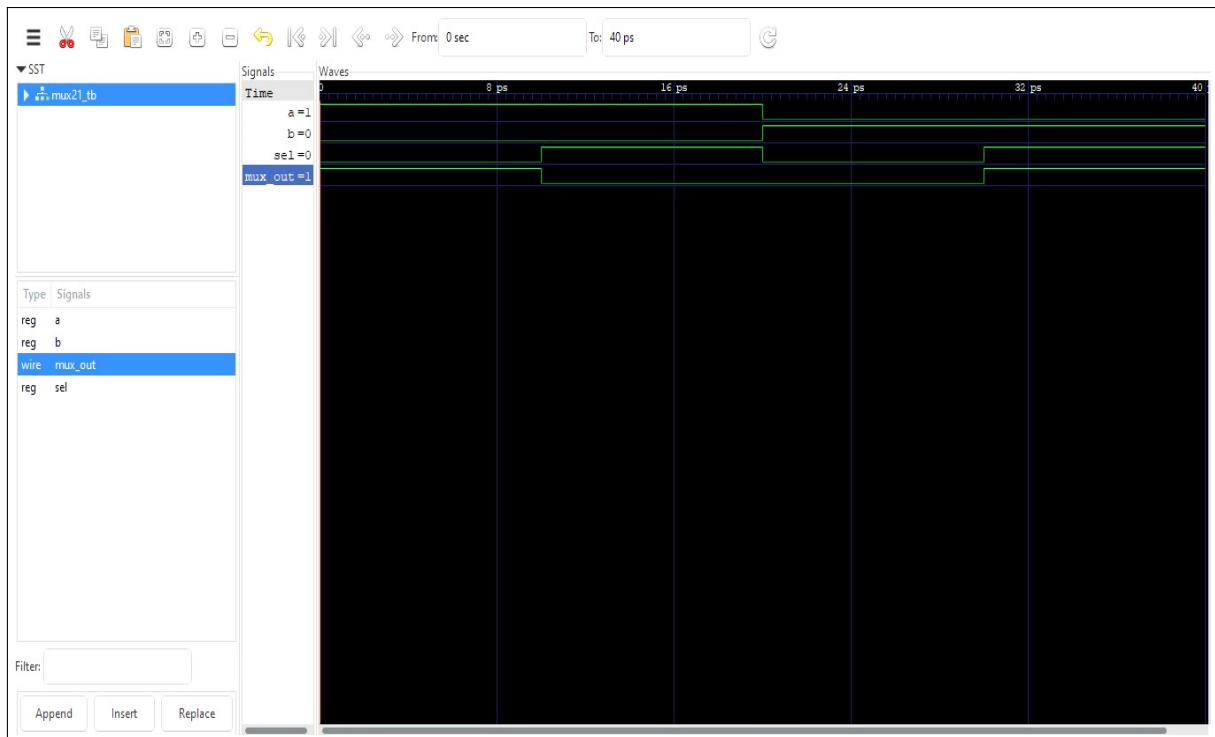


Figure 5.3: Simulation Result of 2:1 Multiplexer

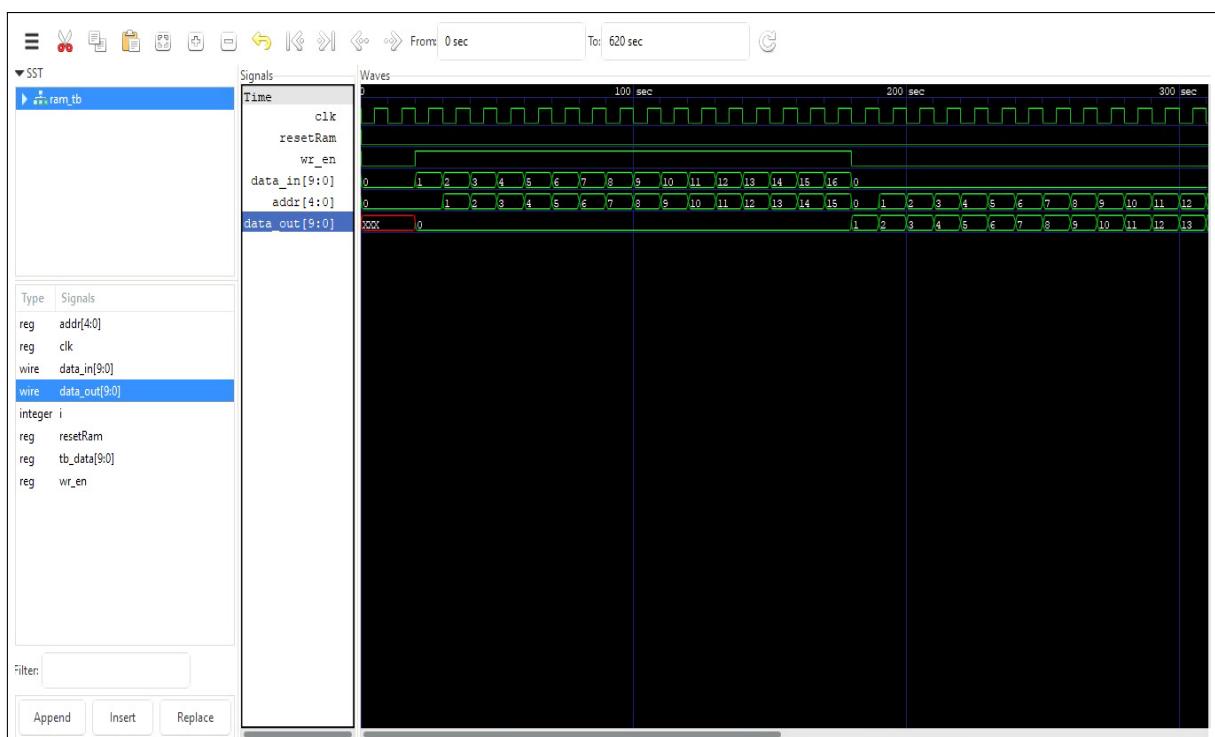


Figure 5.4: Simulation Result of RAM

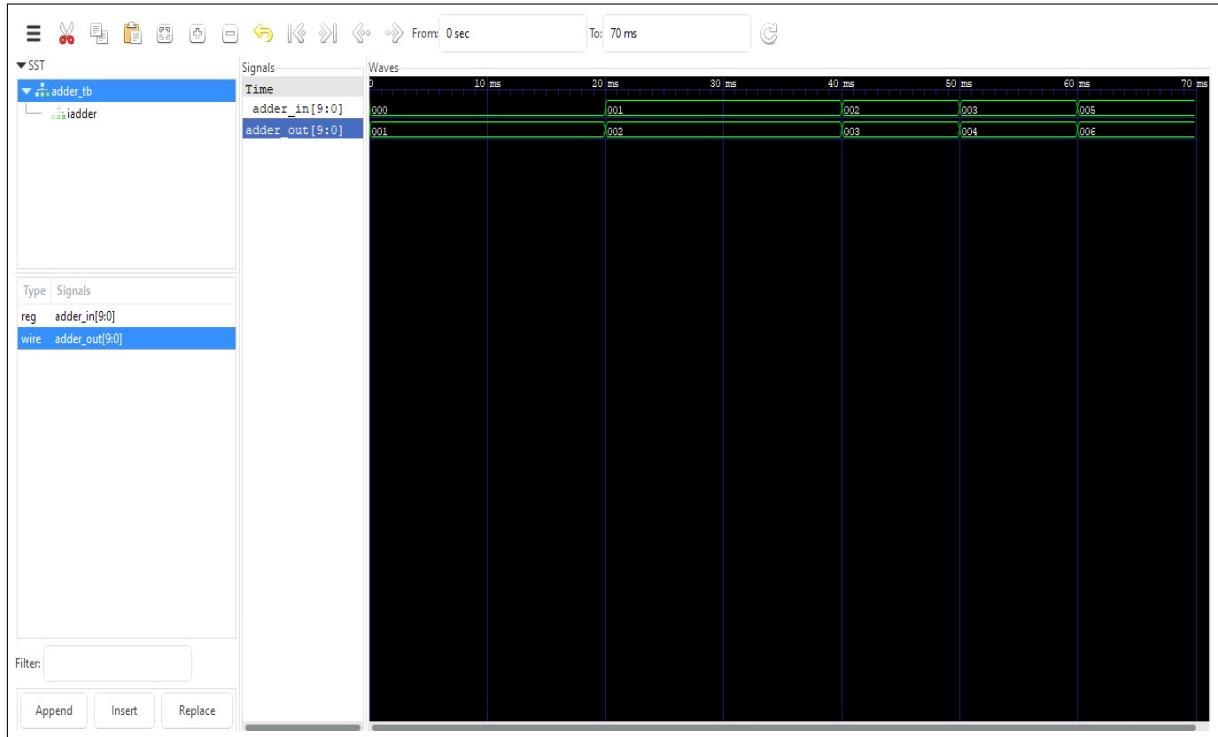


Figure 5.5: Simulation Result of Adder

5.5 Adder

The result of the simulation observed in the GTK waveform after verifying the Adder by verilog code is shown in the above Figure 5.5-

5.6 Counter

The result of the simulation observed in the GTK waveform after verifying the Counter by verilog code is shown in the following Figure 5.6-

5.7 Monostable Multivibrator

The result of the simulation observed in the GTK waveform after verifying the Monostable Multivibrator by verilog code is shown in the following Figure 5.7-

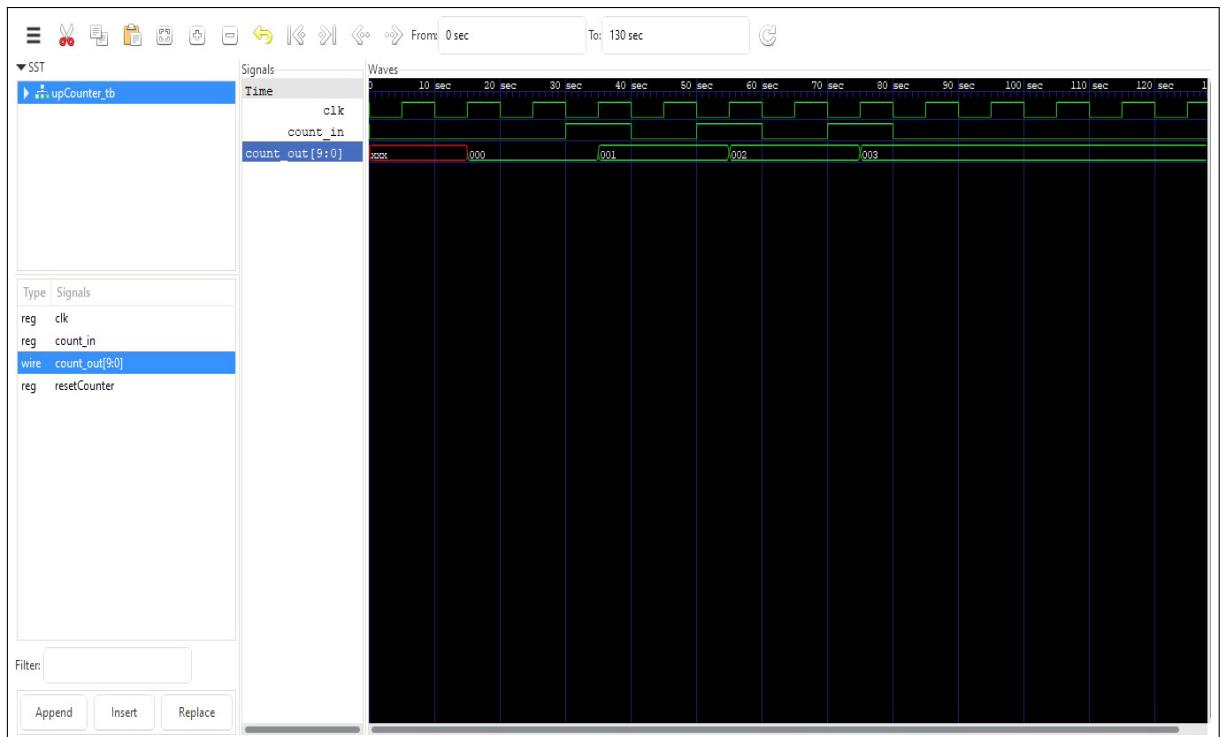


Figure 5.6: Simulation Result of Counter

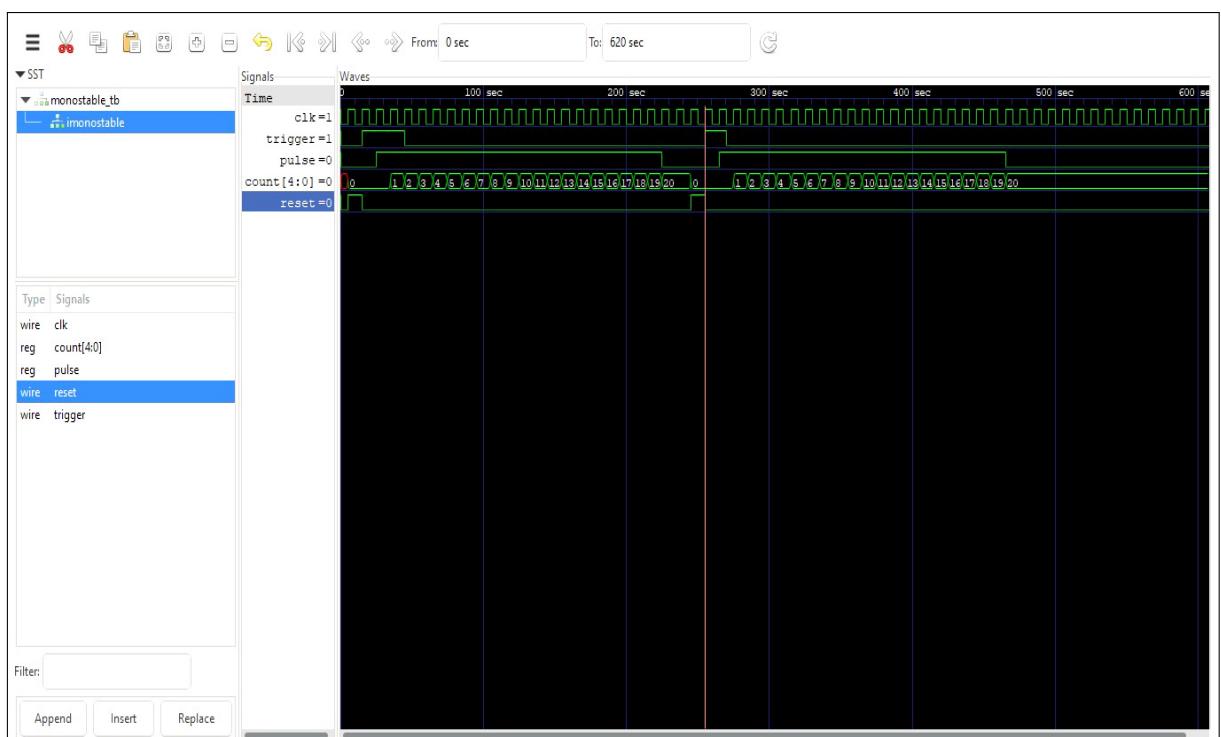


Figure 5.7: Simulation Result of Monostable Multivibrator

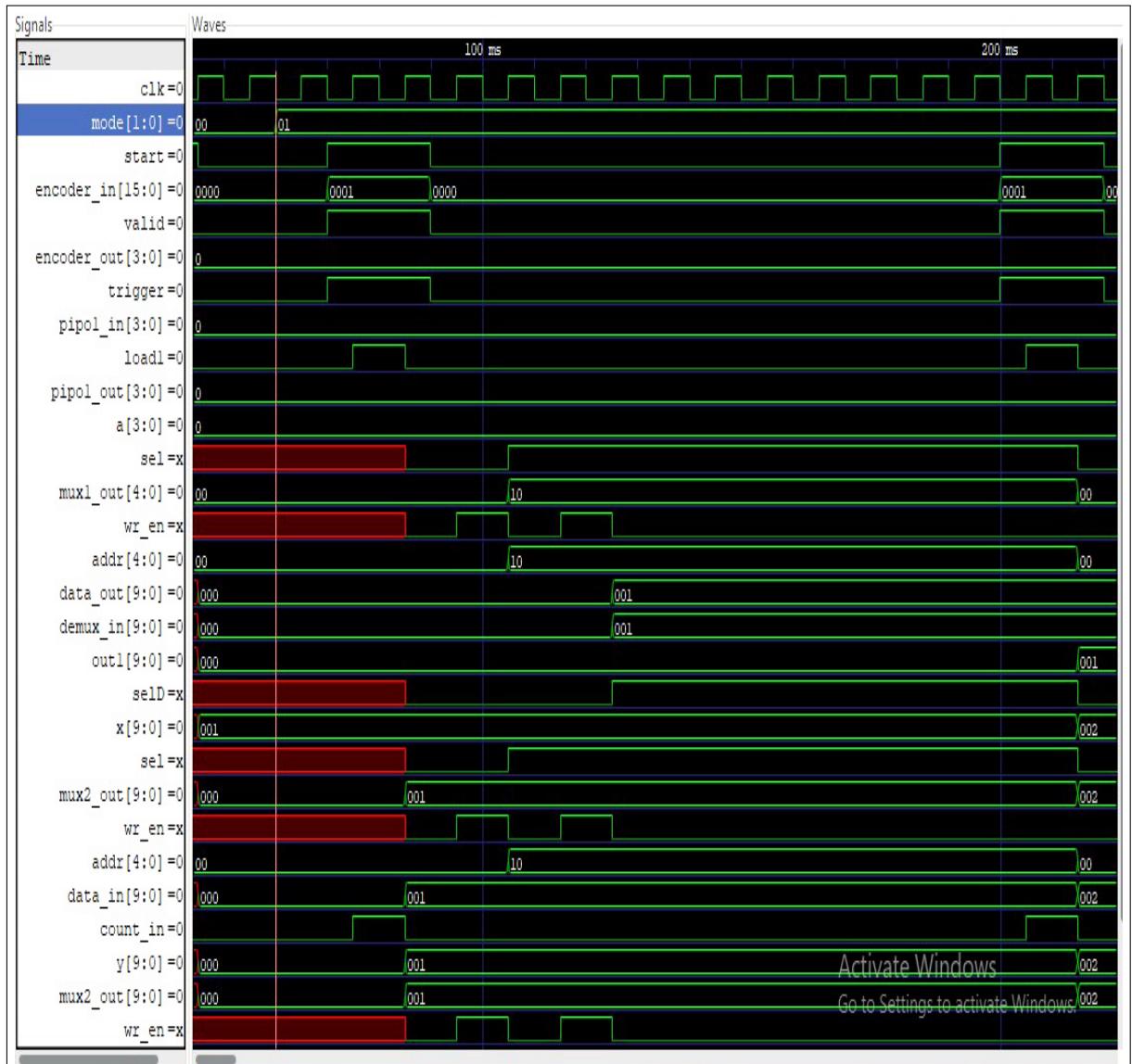


Figure 5.8: Simulation Waveforms showing Clear Mode and Vote Casted by Candidate

5.8 Final Simulation Result of EVM

The final result of the simulation observed in the GTK waveform is shown in the above and below two Figures such as Figure 5.8 & Figure 5.9 -

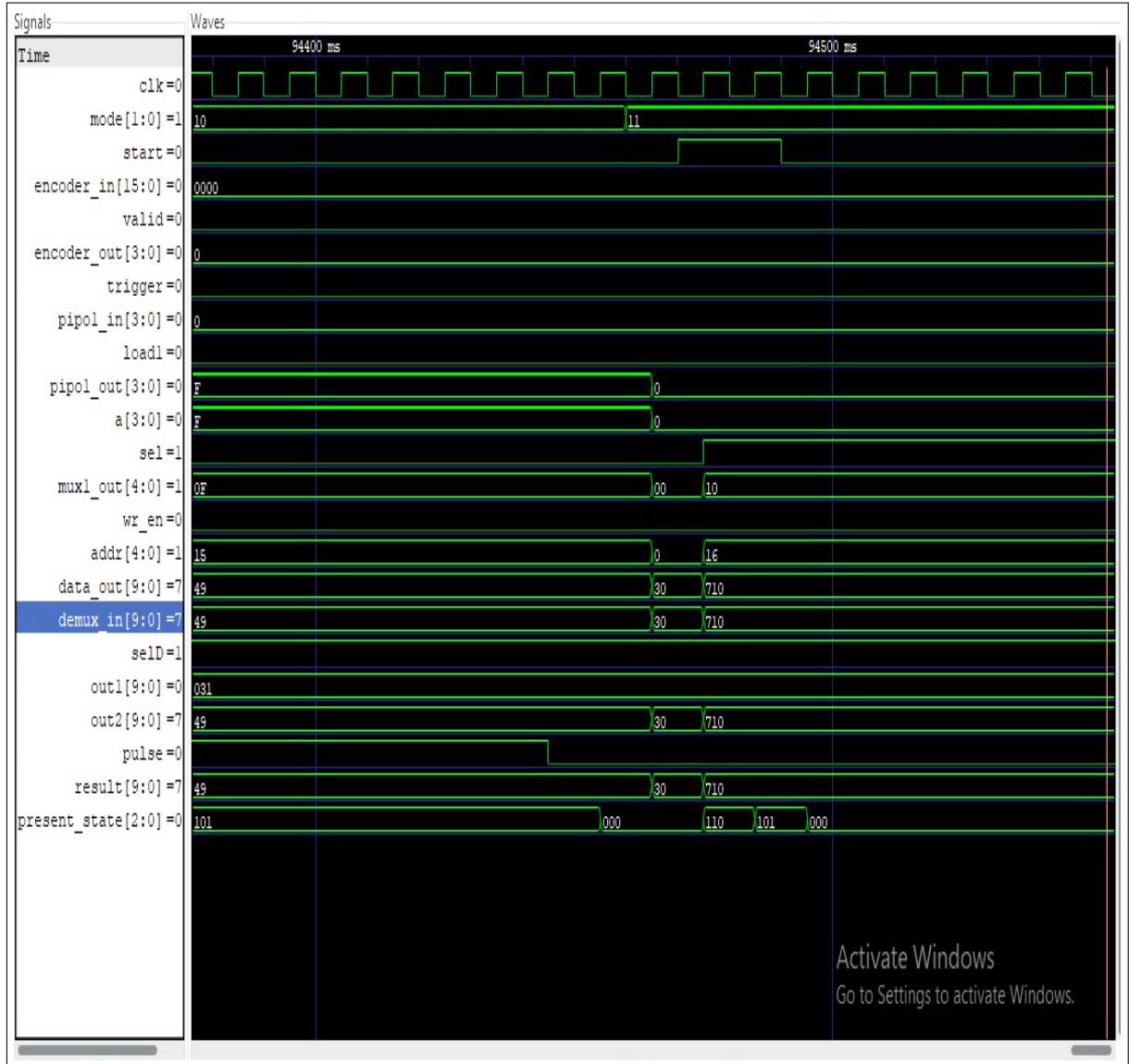


Figure 5.9: Simulation Waveforms showing Individual and Total Counting of Vote

Chapter 6

CONCLUSION

Creating a user-friendly machine is a very complicated task because one has to design a machine which is more familiar with human behaviour. We proposed a procedure to use the machine which is very easy not only for the voter but also for the officers. In our Project, considering the fact of the uncompromising advancement of VLSI technology, we have successfully verify and simulate an Application Specific Integrated Circuit (ASIC) based efficient Electronic Voting Machine by satisfactorily meeting the related issues of security and transparency for an EVM. Our EVM deals with the sensitive cases in voting processes like restriction of an invalid voter, prohibition of same voter and simultaneous vote cast for more than one candidate.

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