中国科学技术大学
University of Science and Technology of China

实验02
简单组合逻辑电路

2021-10-21

实验原理

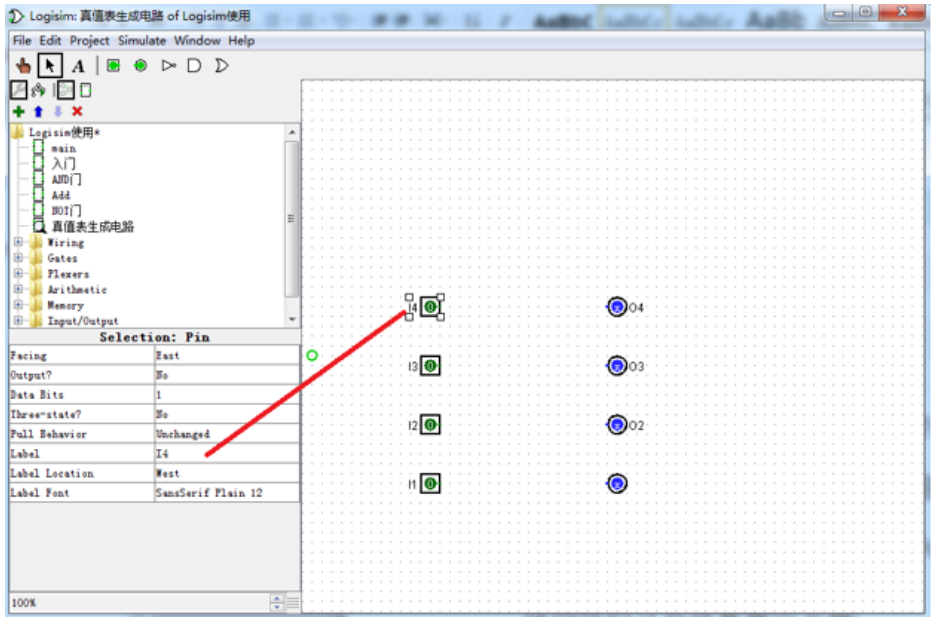
- 熟练掌握Logisim的基本用法
- 进一步熟悉Logisim更多功能
- 用Logisim设计组合逻辑电路并进行仿真
- 初步学习Verilog语法

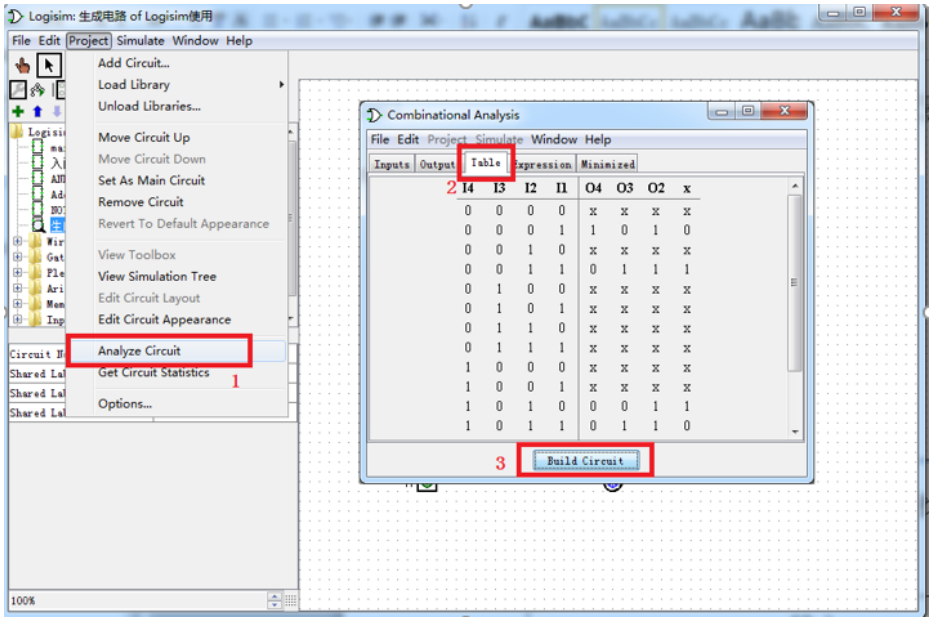
实验环境

- vlab.ustc.edu.cn
- Logisim
- verilogoj.ustc.edu.cn

实验步骤

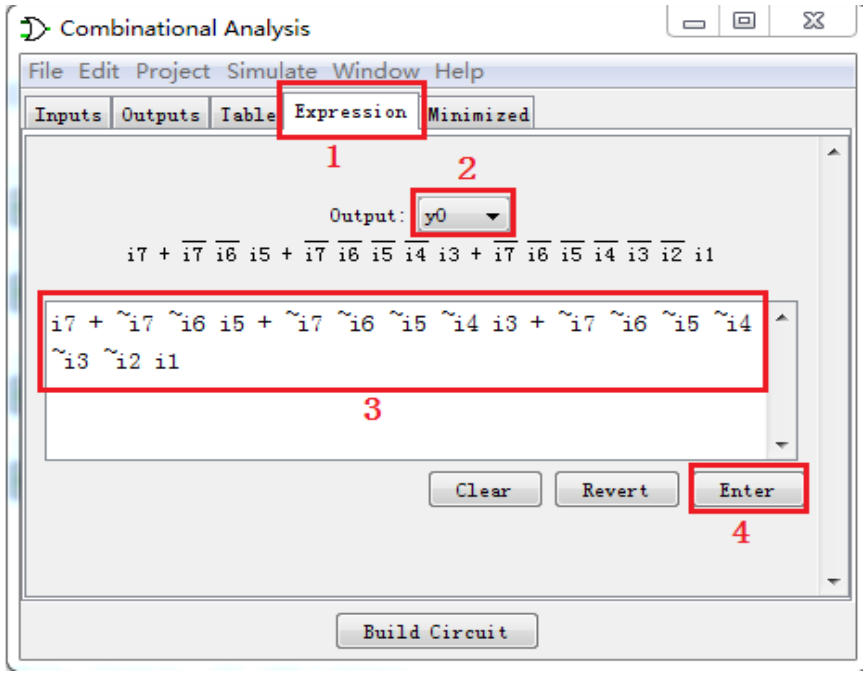
- Step1：在Logisim中用真值表自动生成电路
  - 在电路中放置输入输出引脚，并对其命名
  - 编辑电路真值表：“Project”→ “Analyze Circuit”→“Table”
  - 生成电路：“Build Circuit”

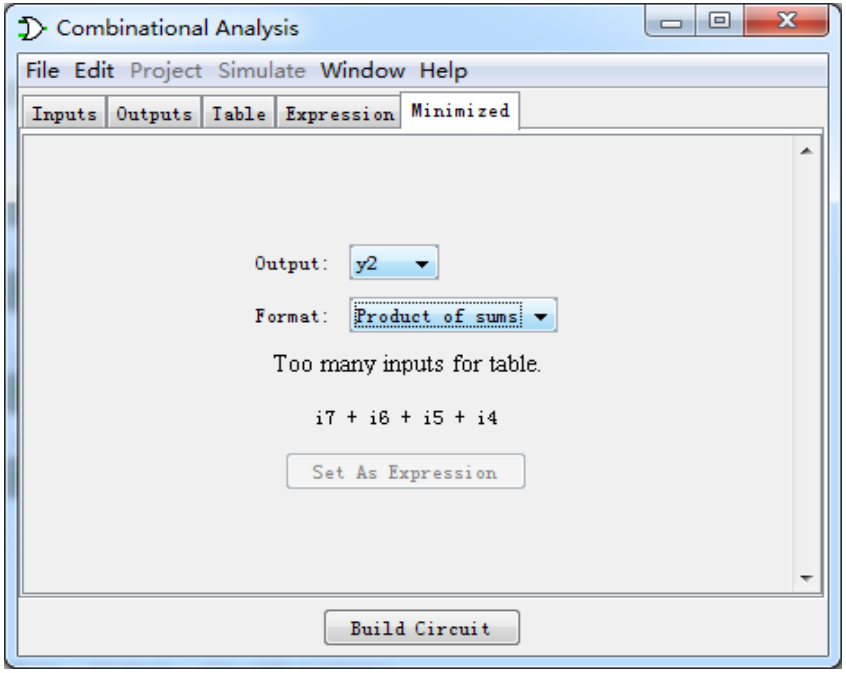




实验步骤

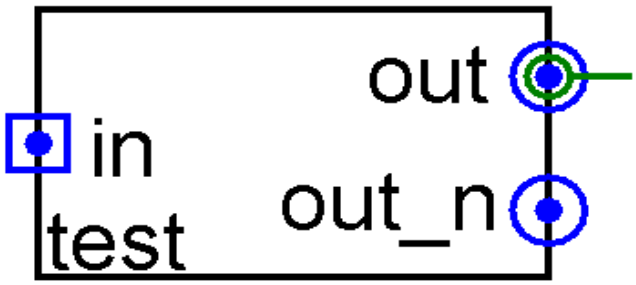
- Step2：用表达式生成电路图
  - 在电路中放置输入输出引脚，并对其命名
  - 编辑电路真值表：“Project”→ “Analyze Circuit”→“Expression”
  - 生成电路：“Build Circuit”

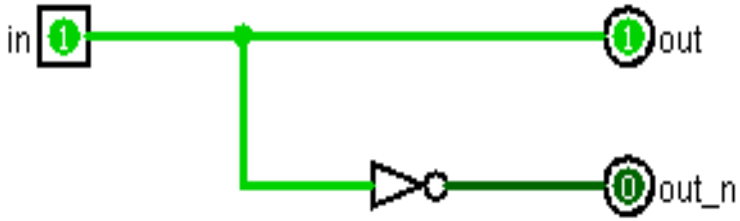




实验步骤

■ Step3：Verilog语法入门_模块结构

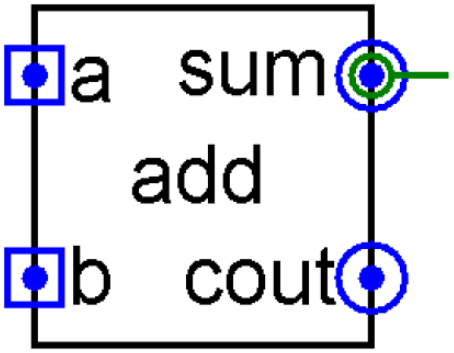


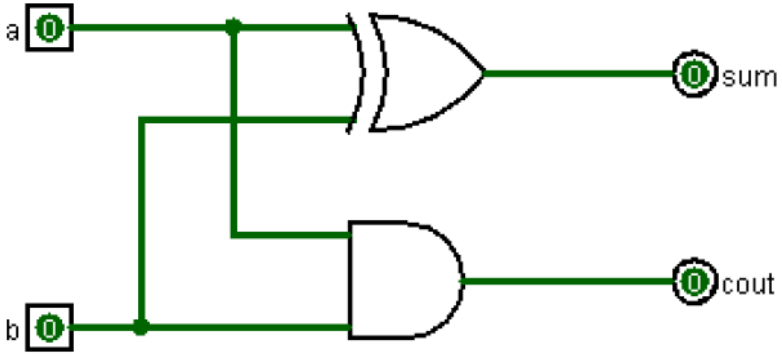



```
module test(  //模块名称
input in,     //输入信号声明
output out,   //输出信号声明
output out_n);
//如需要，可在此处声明内部变量
/*******以下为逻辑描述部分******/
    assign out = in;
    assign out_n = ~in;
/*******逻辑描述部分结束******/
endmodule //模块名结束关键词
```

实验步骤

■ Step3：Verilog语法入门_功能电路设计



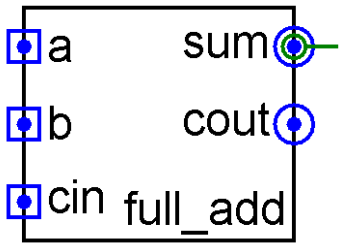


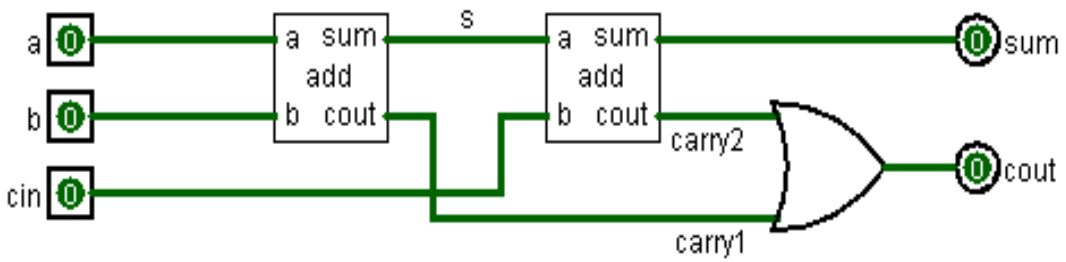

```
module add(
input a,b,
output sum,cout);
assign sum = a ^ b;
assign cout = a & b;
endmodule
```

```
module add(
input a,b,
output sum,cout);
assign {cout,sum} = a + b;
endmodule
```

实验步骤

■ Step3：Verilog语法入门_模块调用






```
module full_add(
input  a,b,cin,
output sum,cout);
wire s,carry1,carry2;
add   add_inst1(
.a     (a    ),
.b     (b    ),
.sum   (s    ),
.cout  (carry1));
add add_inst2(
.a     (s    ),
.b     (cin  ),
.sum   (sum  ),
.cout  (carry2));
assign cout = carry1 | carry2;
endmodule
```

实验步骤

- Step4：完成实验指导手册中的练习题
- Step5：按时提交检查并提交实验报告
- Step6：登录verilogoj.ustc.edu.cn进行编码练习

谢谢！