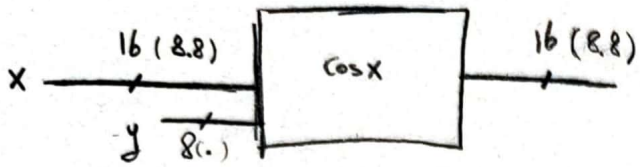
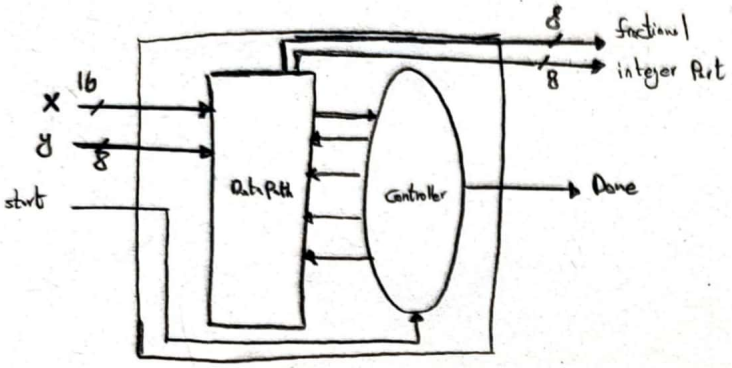
سیستم کنترلی مجزی ۸۱۰۱۰۱۴۹۶

$$\cos x = 1 - \frac{x^2}{2!} + \frac{x^4}{4!} - \frac{x^6}{6!} + \cdots$$

```
r = 1;
t = 1;
for(k=1; k<n ; k++) {
    if(k%2 == 1):
        t = t * x^2 * (1/M)
        r = r + t
    else:
        t = t * x^2 * (1/M)
        r = r - t
}
```

در ابتدا سری تیلور $\cos x$ را نوشته و بعد از آن شبه کد آن را نوشته و با بیتم به جزیایی نیاز داریم و Datapath خود را طبق آن طراحی می‌کنیم.





جزیایی که نیاز داریم: ① محاسبه x^2

② داشتن یک LUT برای محاسبه‌ی $\frac{1}{M}$

③ یک Reg برای ذخیره x و در مرحله بعد x^2

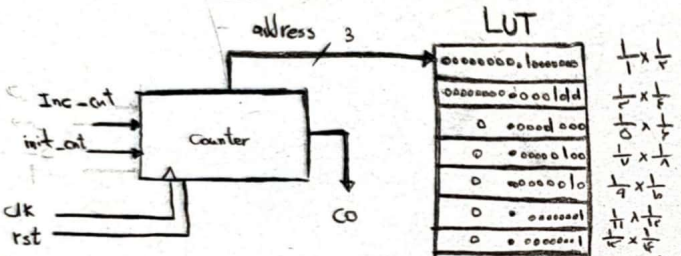
④ یک Reg برای ذخیره y

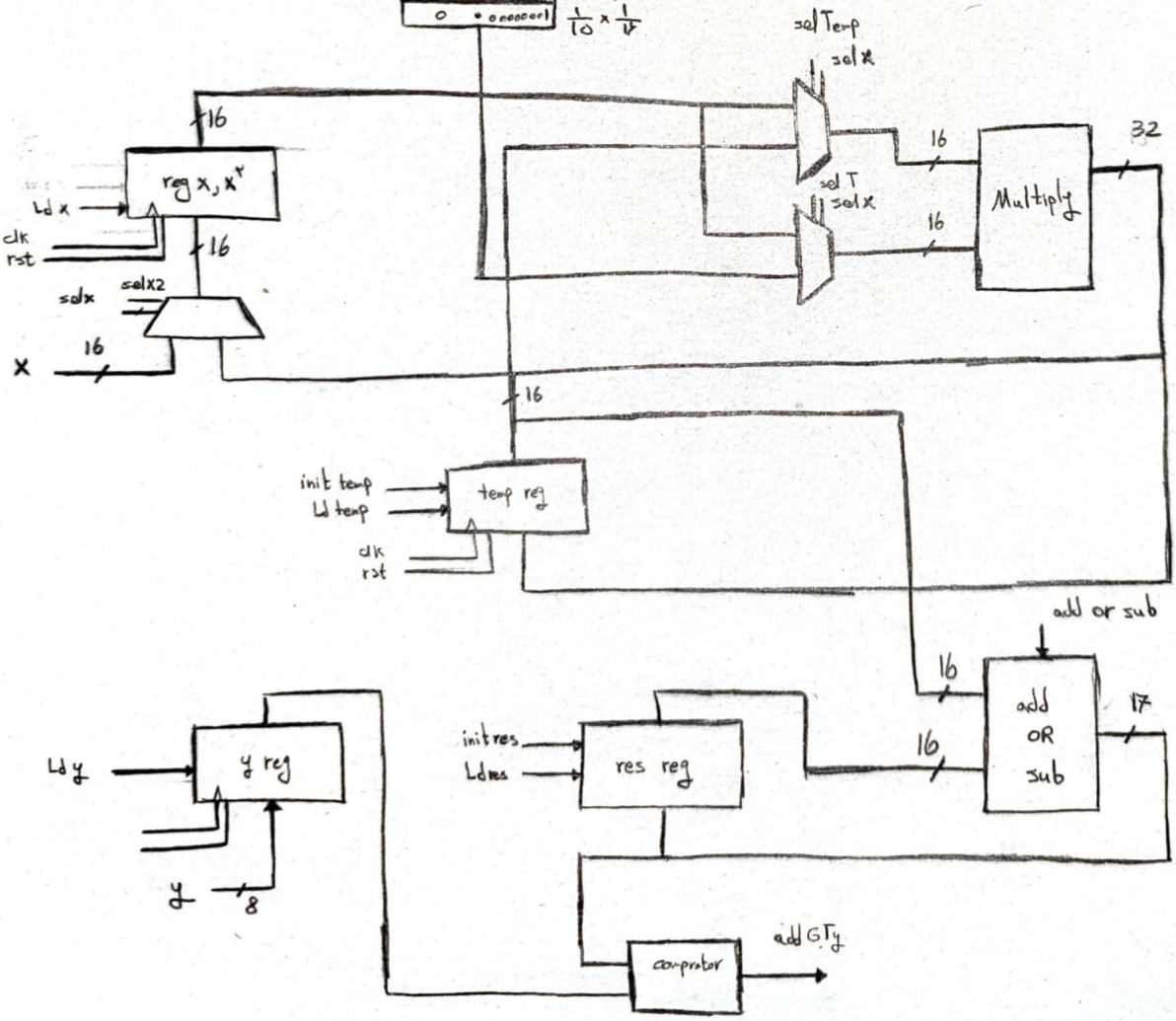
⑤ یک ⊗ برای حاسبه ضرب‌ها

⑥ یک ⊕/⊖ برای محاسبه جمع و تفاضل‌ها

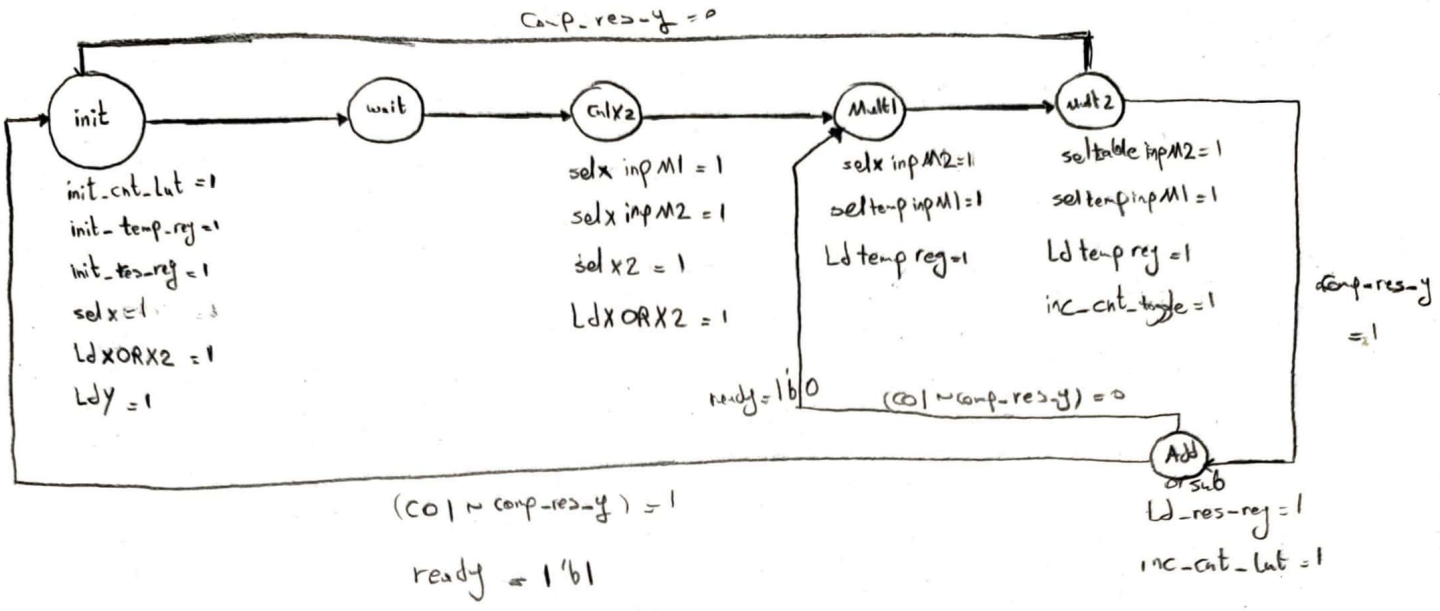
⑦ یک Comparator برای چک کردن پایان عملیات

⑧ چند reg دیگر برای ذخیره متغیرهای بین محاسبات



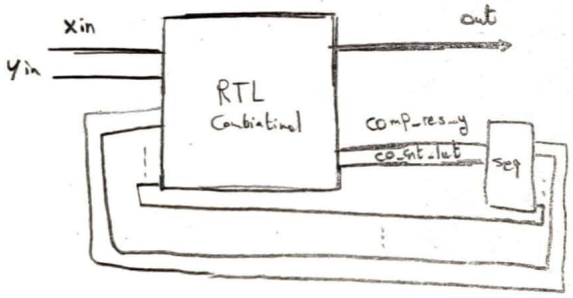


((Controller))

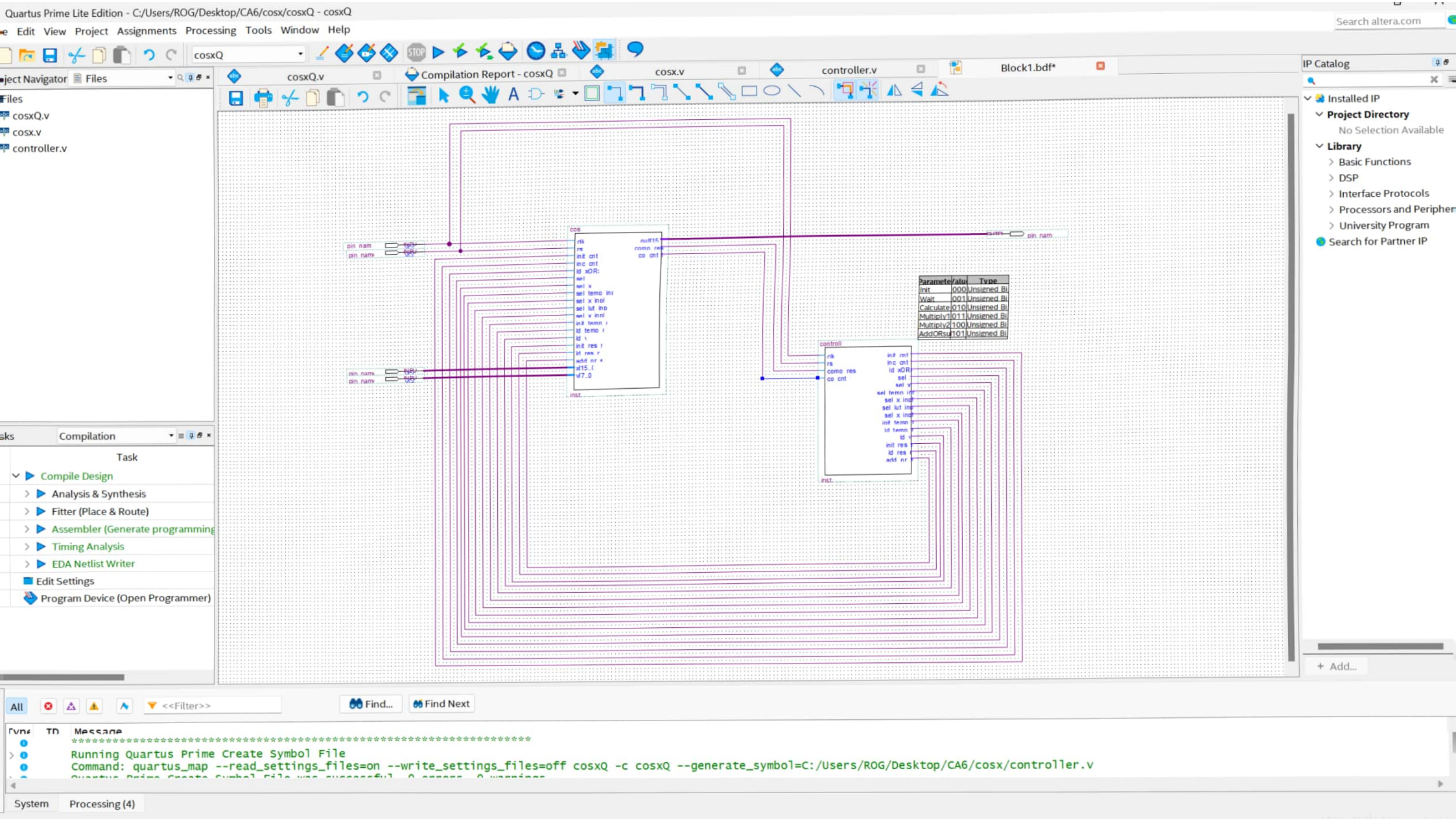


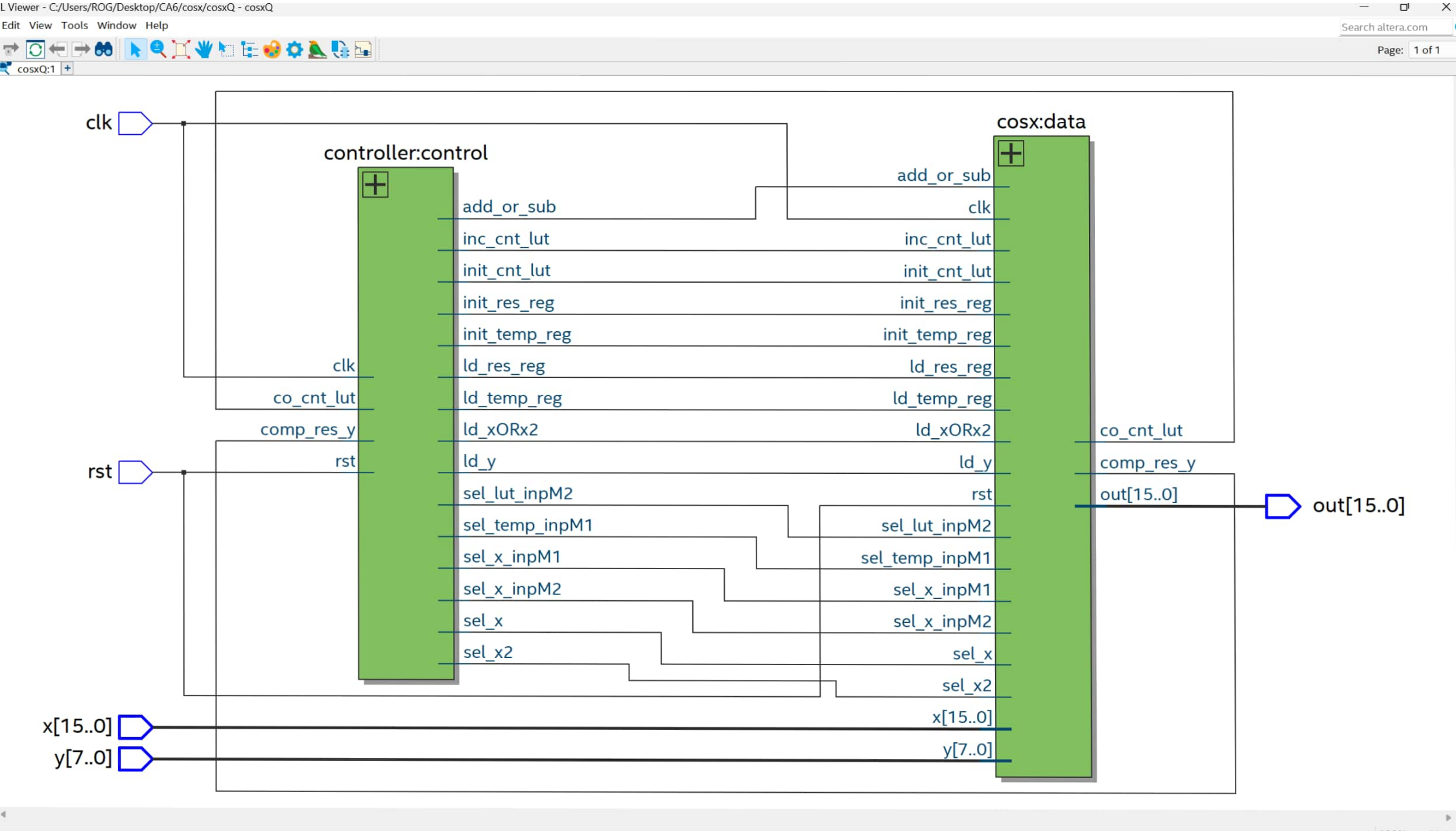
این کنترل را طراحی کرده که در آن سعی شده تا جایی ممکن تعداد state ها کم باشد و حداکثر دقت را داشته باشد.
در مرحله اول state init را راضی کرده تا هنگامی که از state دیگر شروع کرده در داخل بلوک x^2 را حساب کرده و حاصل جمع و منها را انجام دهد.

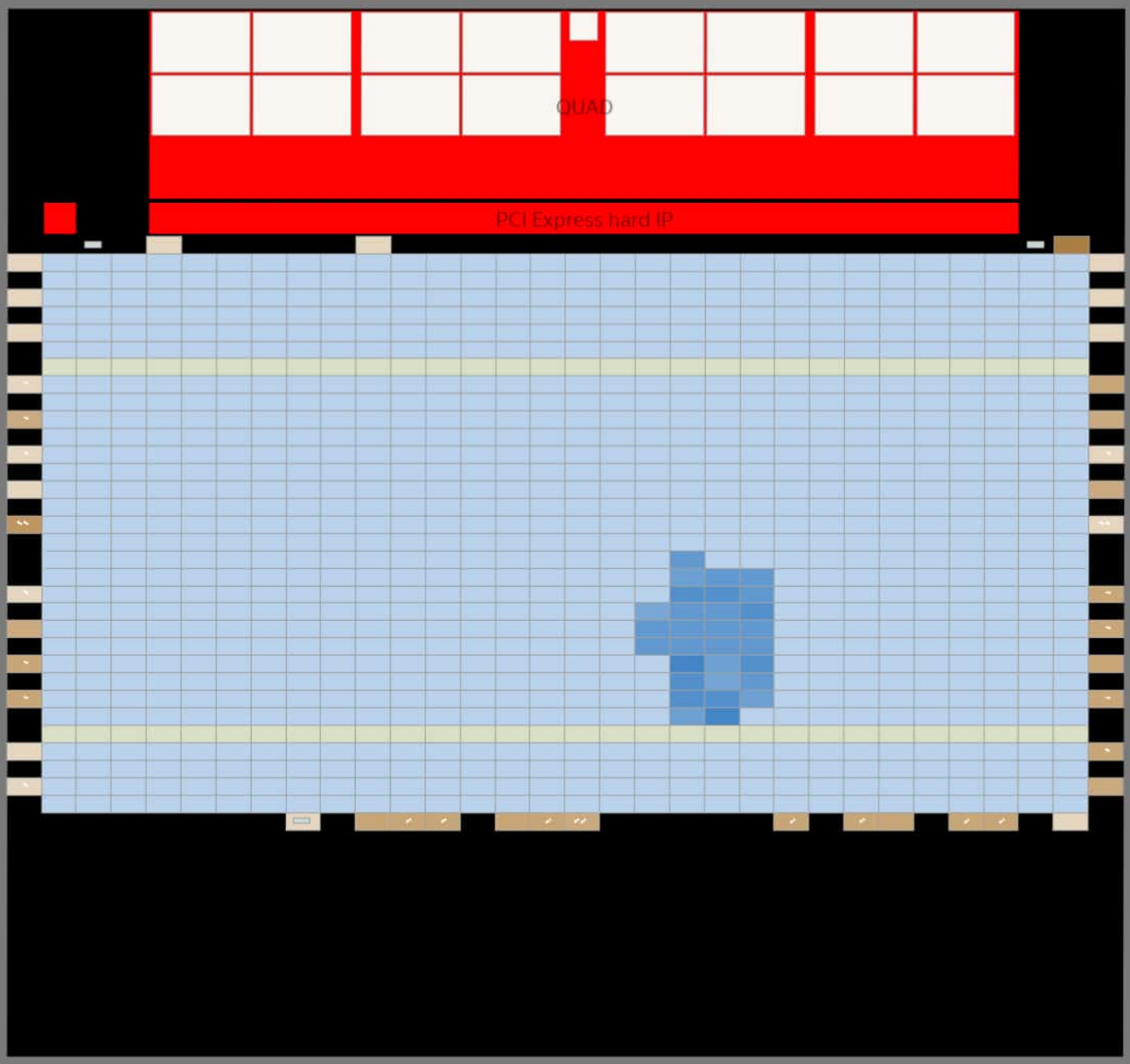
Huffman model

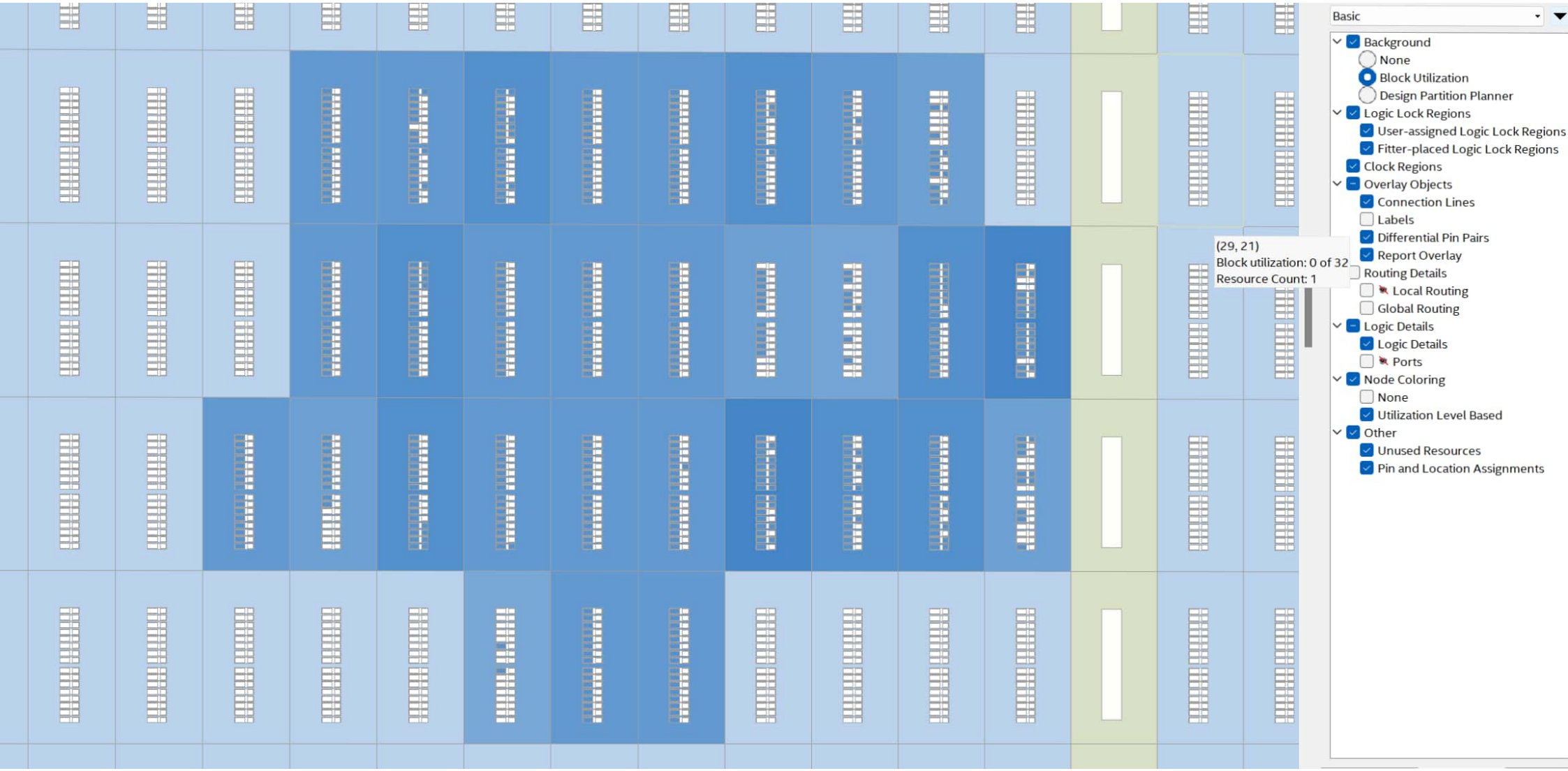


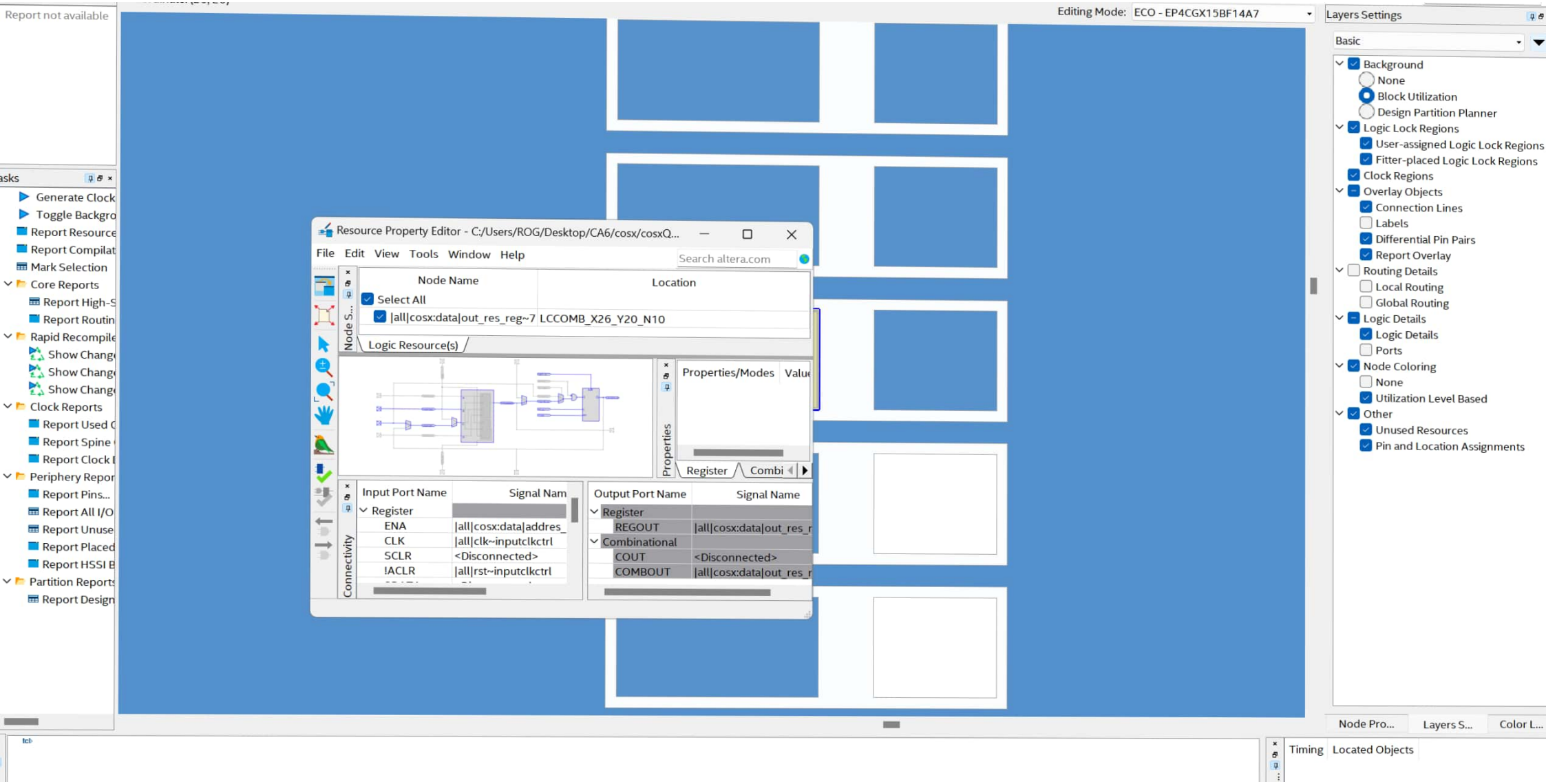
در مدل هافمن هم مدار را به ۲ بلوک کلی comb_ و seq_ تقسیم کرده.

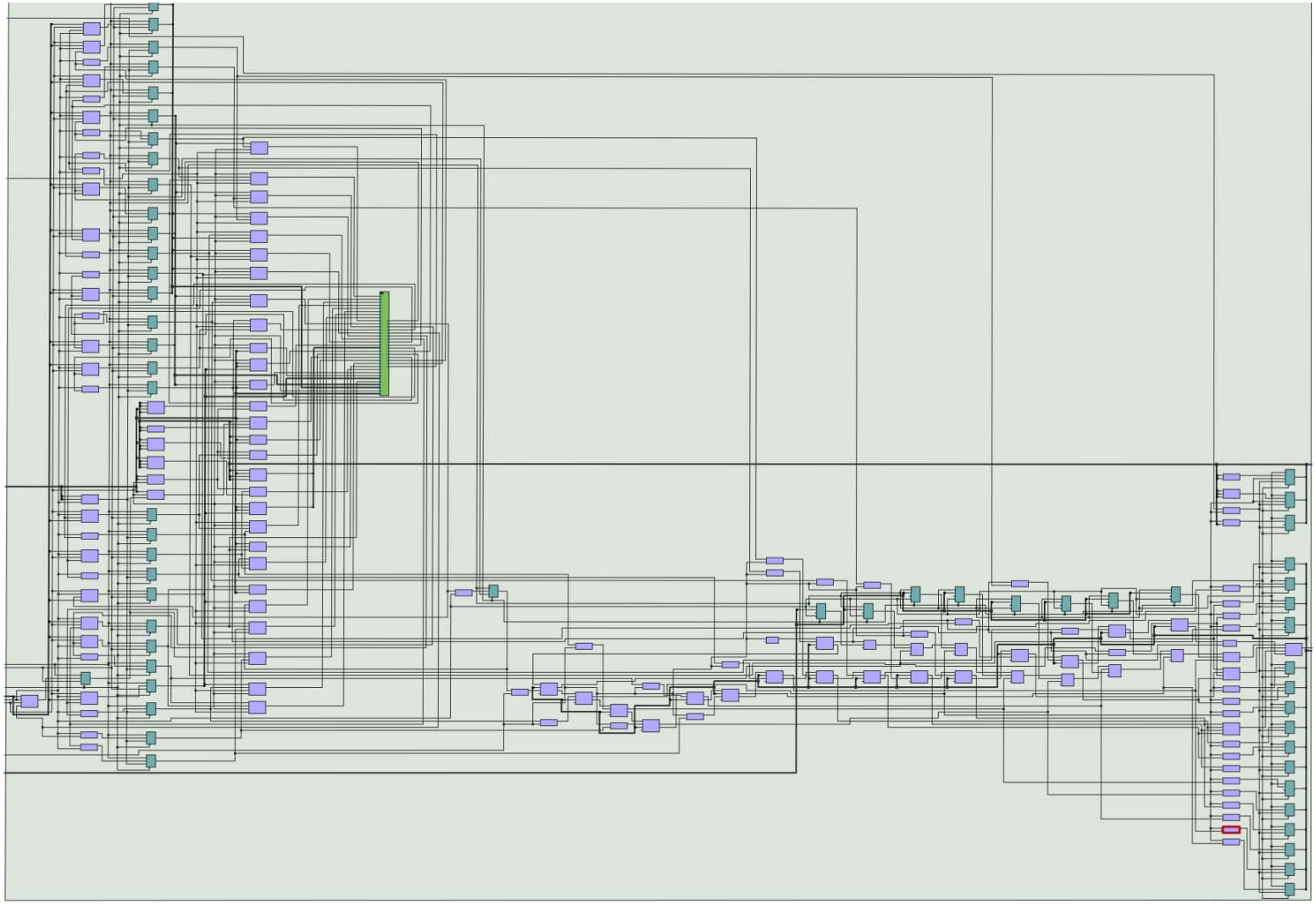

Quartus Prime Lite Edition - C:/Users/ROG/Desktop/CA6/cosx/cosxQ - cosxQ
Edit View Project Assignments Processing Tools Window Help
Search altera.com
cosxQ
cosxQ.v
Compilation Report - cosxQ
cosx.v
controller.v
Block1.bdf*
Files
cosxQ.v
cosx.v
controller.v
Compilation
Task
Compile Design
Analysis & Synthesis
Fitter (Place & Route)
Assembler (Generate programming
Timing Analysis
EDA Netlist Writer
Edit Settings
Program Device (Open Programmer)
IP Catalog
Installed IP
Project Directory
No Selection Available
Library
Basic Functions
DSP
Interface Protocols
Processors and Peripher
University Program
Search for Partner IP
Add...
Parameter
Value
Type
Init
000
Unsigned Bi
Wait
001
Unsigned Bi
Calculate
010
Unsigned Bi
Multiply1
011
Unsigned Bi
Multiply2
100
Unsigned Bi
AddORsu
101
Unsigned Bi
All
<<Filter>>
Find...
Find Next
Type
Message
Running Quartus Prime Create Symbol File
Command: quartus_map --read_settings_files=on --write_settings_files=off cosxQ -c cosxQ --generate_symbol=C:/Users/ROG/Desktop/CA6/cosx/controller.v
System
Processing (4)

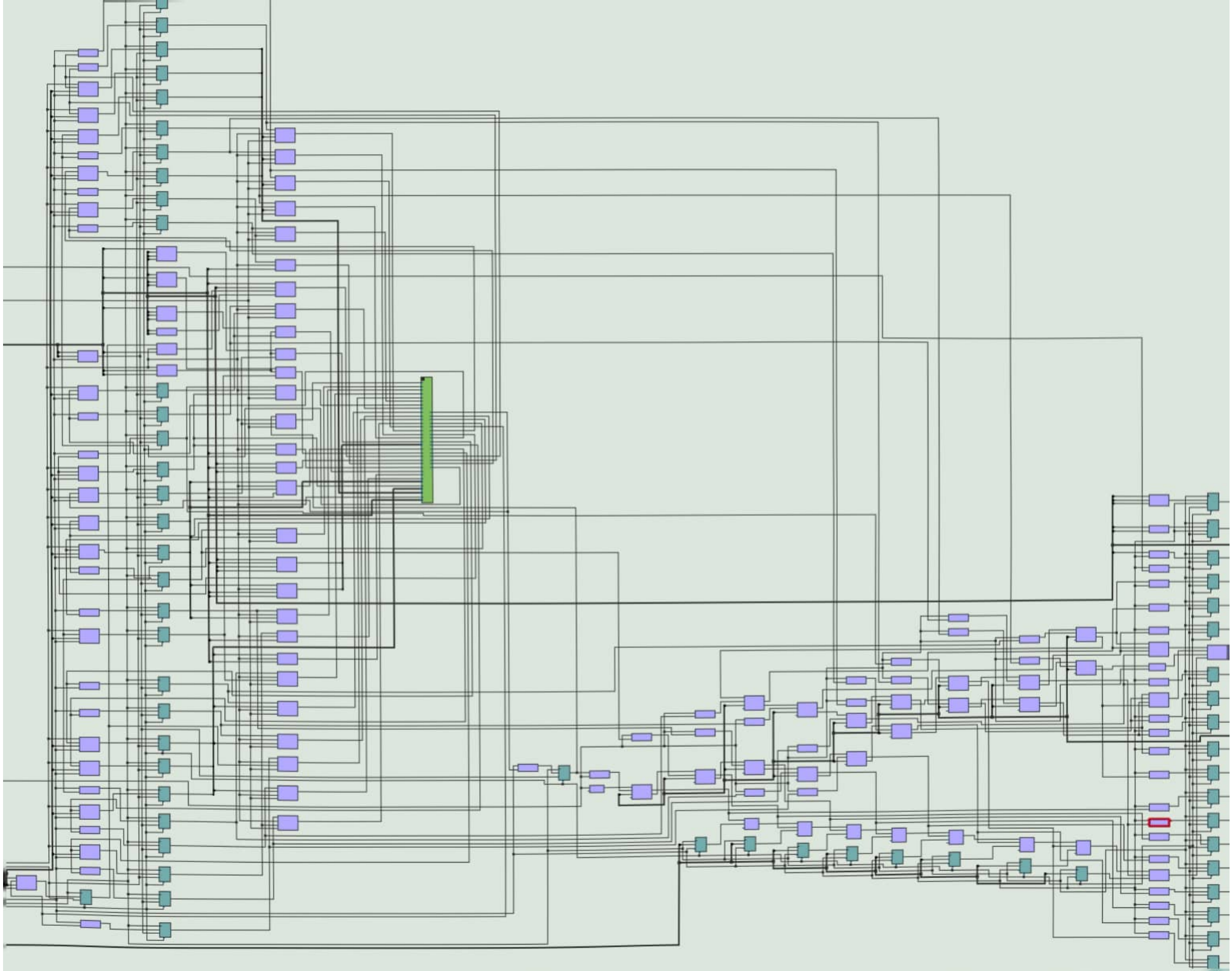

L Viewer - C:/Users/ROG/Desktop/CA6/cosx/cosxQ - cosxQ
Edit View Tools Window Help
Search altera.com
Page: 1 of 1
cosxQ:1
clk
rst
x[15..0]
y[7..0]
controller:control
clk
co_cnt_lut
comp_res_y
rst
add_or_sub
inc_cnt_lut
init_cnt_lut
init_res_reg
init_temp_reg
ld_res_reg
ld_temp_reg
ld_xORx2
ld_y
sel_lut_inpM2
sel_temp_inpM1
sel_x_inpM1
sel_x_inpM2
sel_x
sel_x2
cosx:data
add_or_sub
clk
inc_cnt_lut
init_cnt_lut
init_res_reg
init_temp_reg
ld_res_reg
ld_temp_reg
ld_xORx2
ld_y
rst
sel_lut_inpM2
sel_temp_inpM1
sel_x_inpM1
sel_x_inpM2
sel_x
sel_x2
x[15..0]
y[7..0]
co_cnt_lut
comp_res_y
out[15..0]
out[15..0]


QUAD
PCI Express hard IP


Basic
Background
None
Block Utilization
Design Partition Planner
Logic Lock Regions
User-assigned Logic Lock Regions
Fitter-placed Logic Lock Regions
Clock Regions
Overlay Objects
Connection Lines
Labels
Differential Pin Pairs
Report Overlay
Routing Details
Local Routing
Global Routing
Logic Details
Logic Details
Ports
Node Coloring
None
Utilization Level Based
Other
Unused Resources
Pin and Location Assignments
(29, 21)
Block utilization: 0 of 32
Resource Count: 1


Report not available
Editing Mode: ECO - EP4CGX15BF14A7
Layers Settings
Basic
Background
None
Block Utilization
Design Partition Planner
Logic Lock Regions
User-assigned Logic Lock Regions
Fitter-placed Logic Lock Regions
Clock Regions
Overlay Objects
Connection Lines
Labels
Differential Pin Pairs
Report Overlay
Routing Details
Local Routing
Global Routing
Logic Details
Logic Details
Ports
Node Coloring
None
Utilization Level Based
Other
Unused Resources
Pin and Location Assignments
Generate Clock
Toggle Backgro
Report Resource
Report Compilat
Mark Selection
Core Reports
Report High-S
Report Routin
Rapid Recompile
Show Change
Show Change
Show Change
Clock Reports
Report Used C
Report Spine
Report Clock
Periphery Repor
Report Pins...
Report All I/O
Report Unuse
Report Placed
Report HSSI B
Partition Reports
Report Design
Resource Property Editor - C:/Users/ROG/Desktop/CA6/cosx/cosxQ...
File Edit View Tools Window Help
Search altera.com
Node Name
Location
Select All
|all|cosx:data|out_res_reg~7
LCCOMB_X26_Y20_N10
Logic Resource(s)
Properties/Modes
Value
Register
Combi
Input Port Name
Signal Nam
Register
ENA
|all|cosx:data|addres_
CLK
|all|clk~inputclkctrl
SCLR
<Disconnected>
!ACLR
|all|rst~inputclkctrl
Output Port Name
Signal Name
Register
REGOUT
|all|cosx:data|out_res_r
Combinational
COUT
<Disconnected>
COMBOUT
|all|cosx:data|out_res_r
Node Pro...
Layers S...
Color L...
Timing
Located Objects



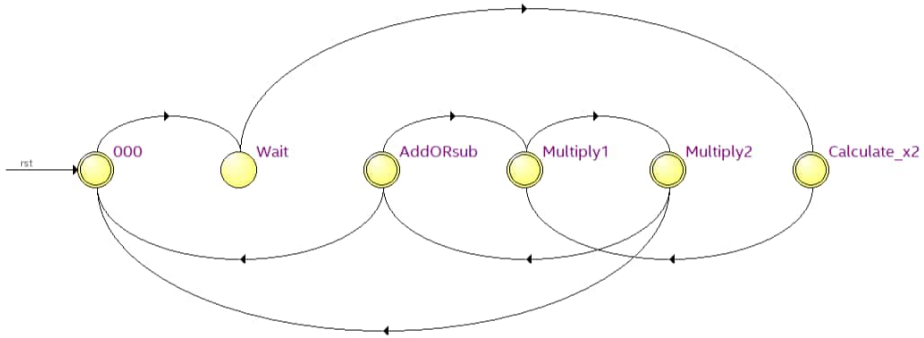


State Machine Viewer - C:/Users/ROG/Desktop/CA6/cosx/cosxQ - cosxQ

le Edit View Tools Window Help

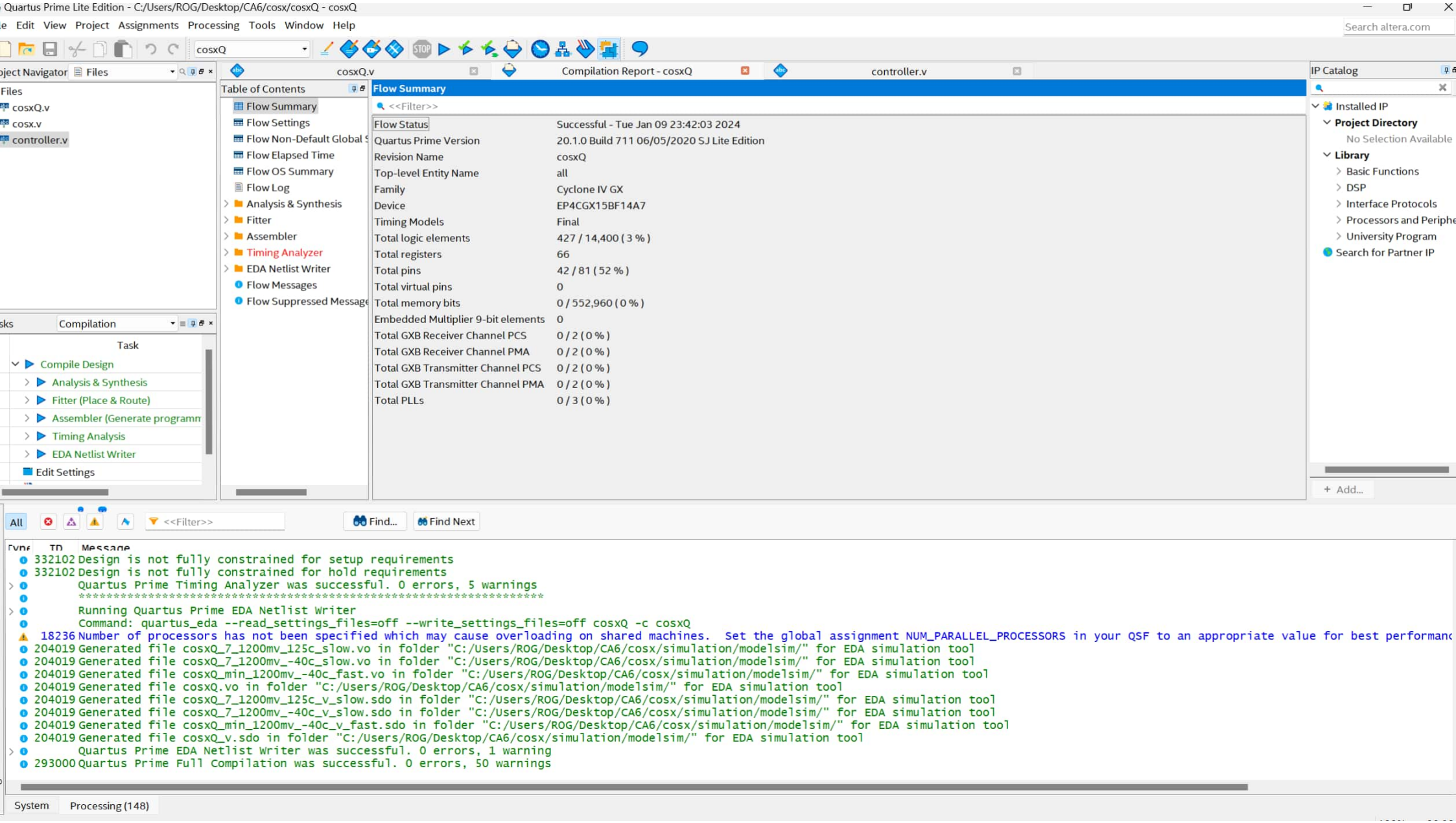
Search altera.com

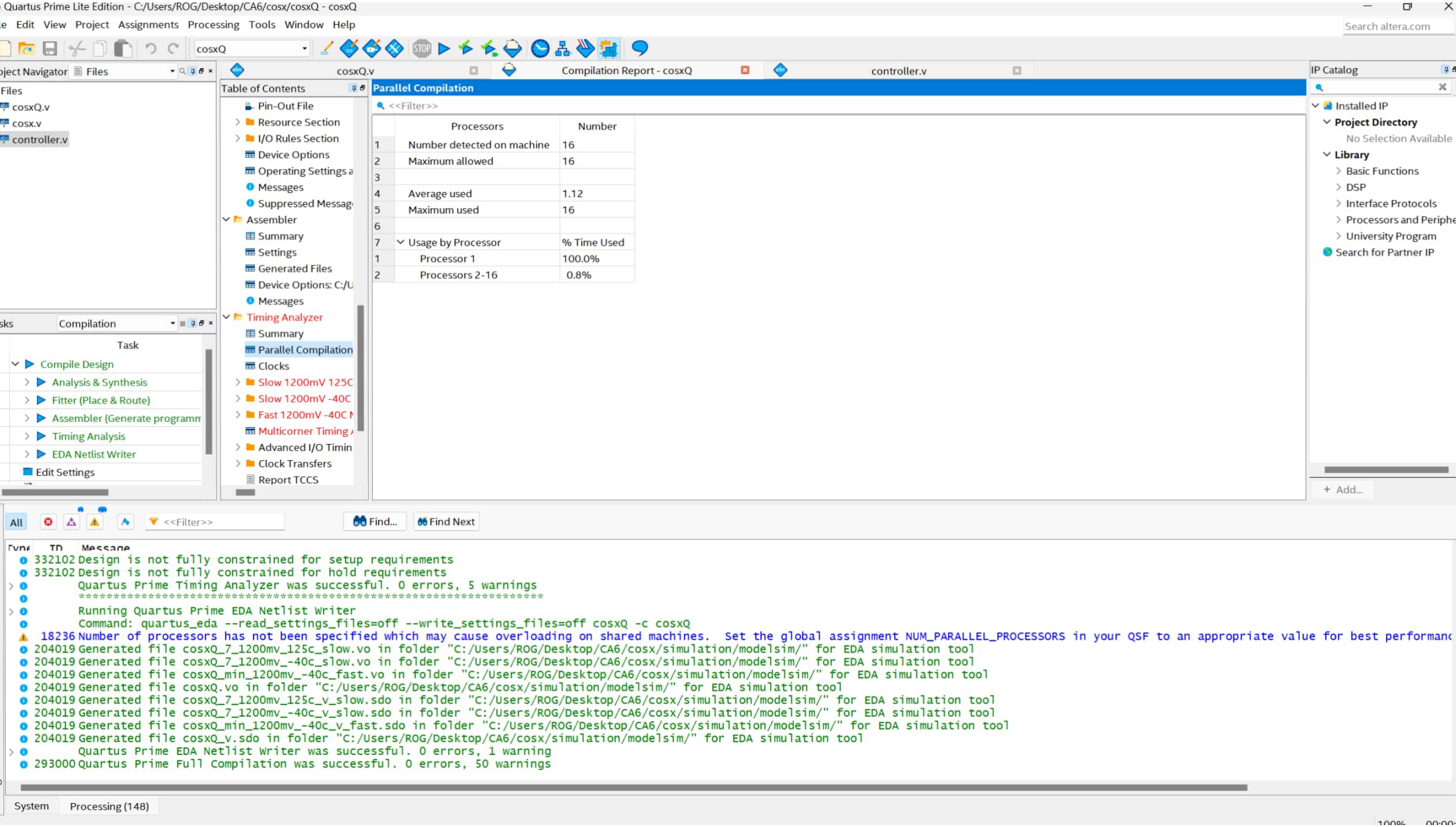
tate Machine: |all|controller:control|pstate

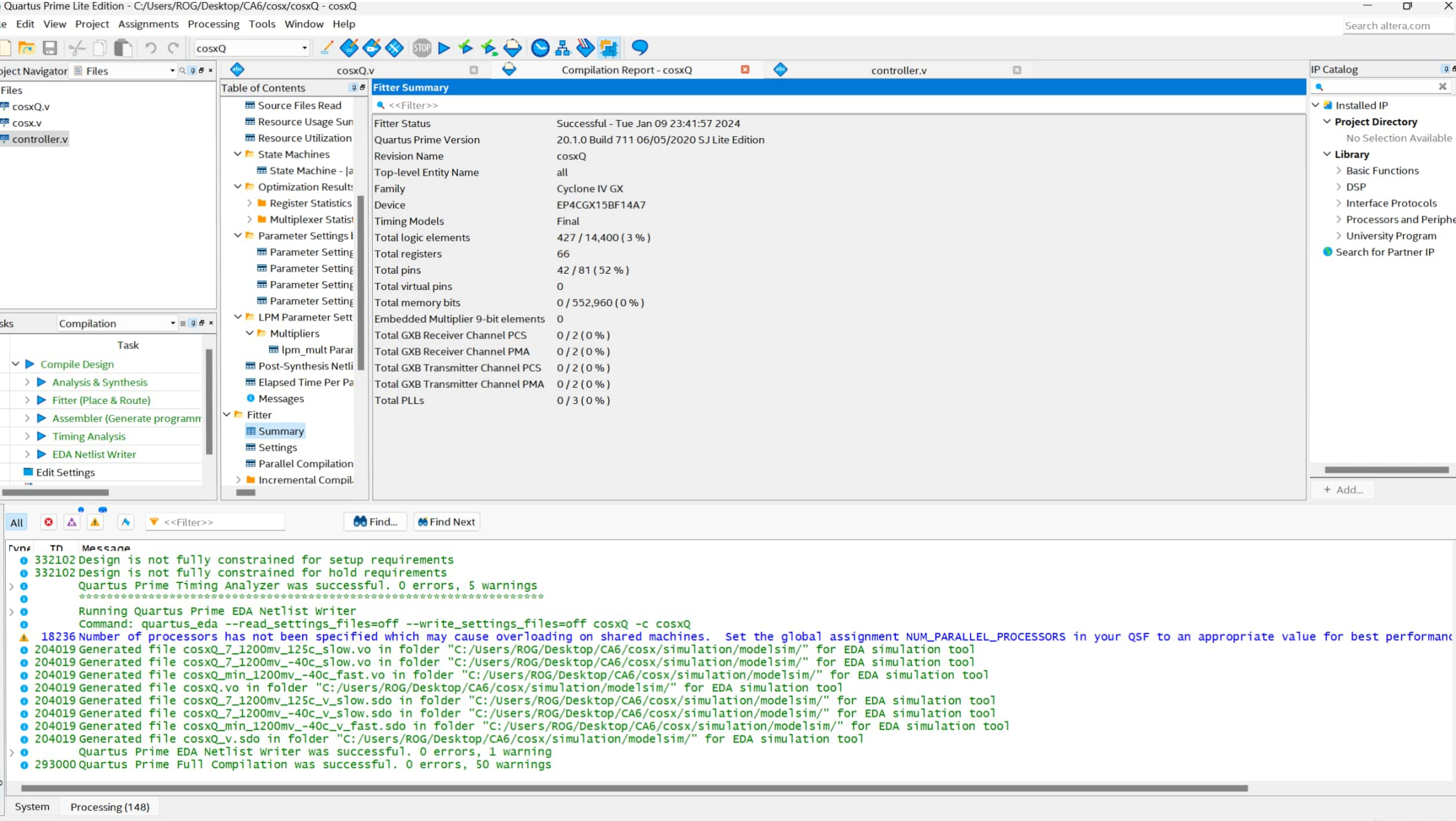


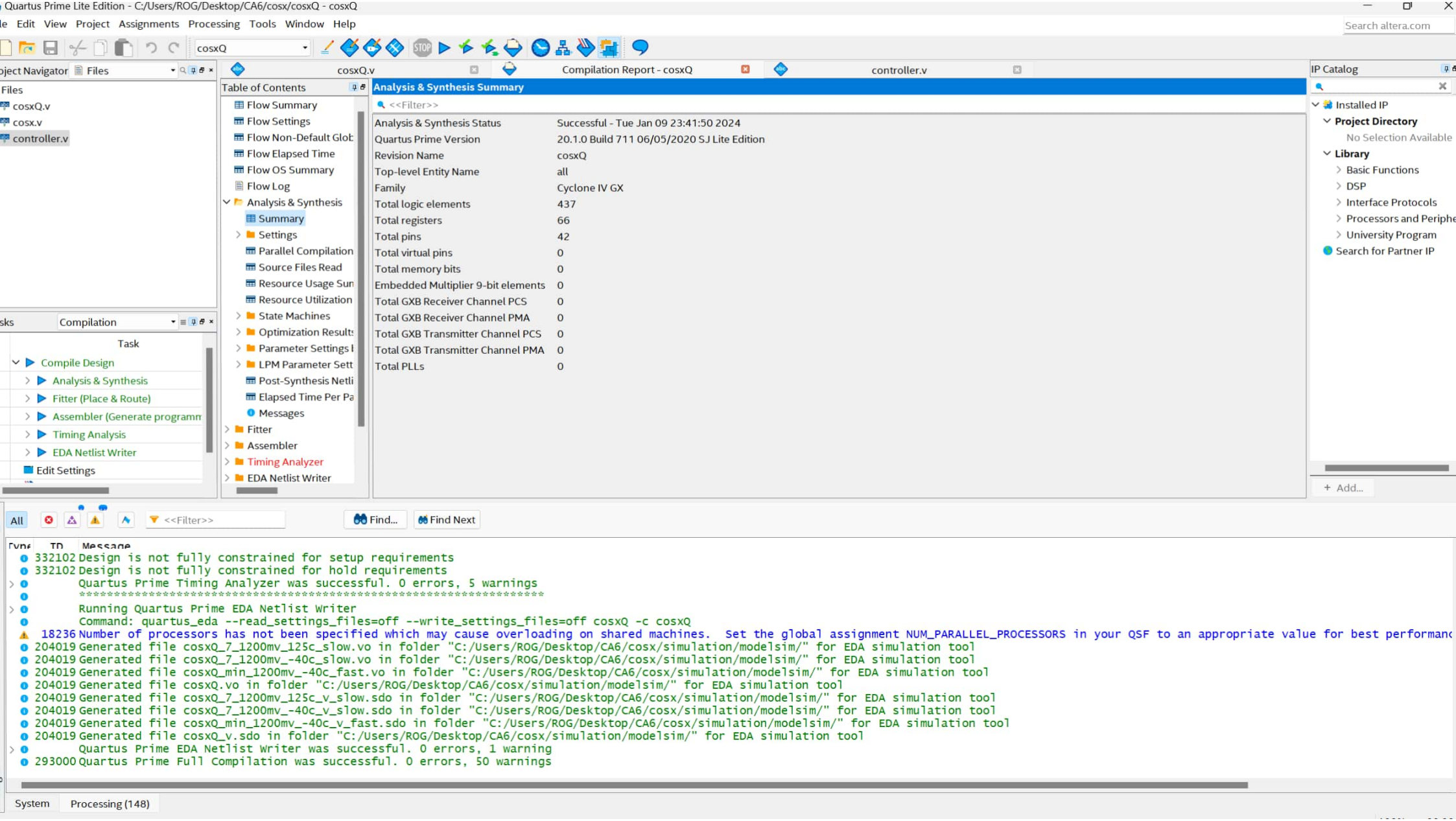
	Source State	Destination State	Condition
1	000	Wait	
2	AddORsub	Multiply1	(!nstate)
3	AddORsub	000	(nstate)
4	Calculate_x2	Multiply1	

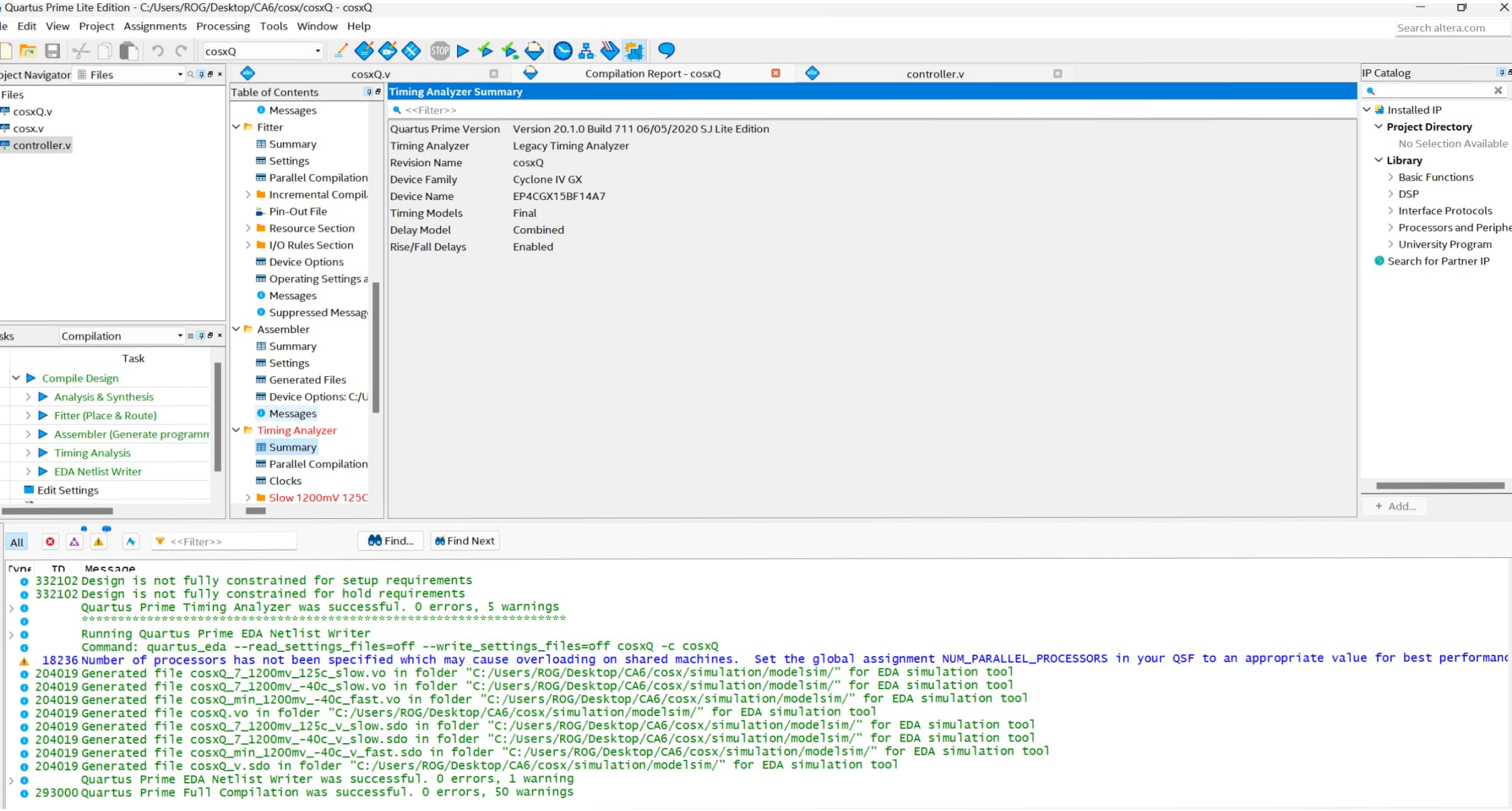
Transitions | Encoding

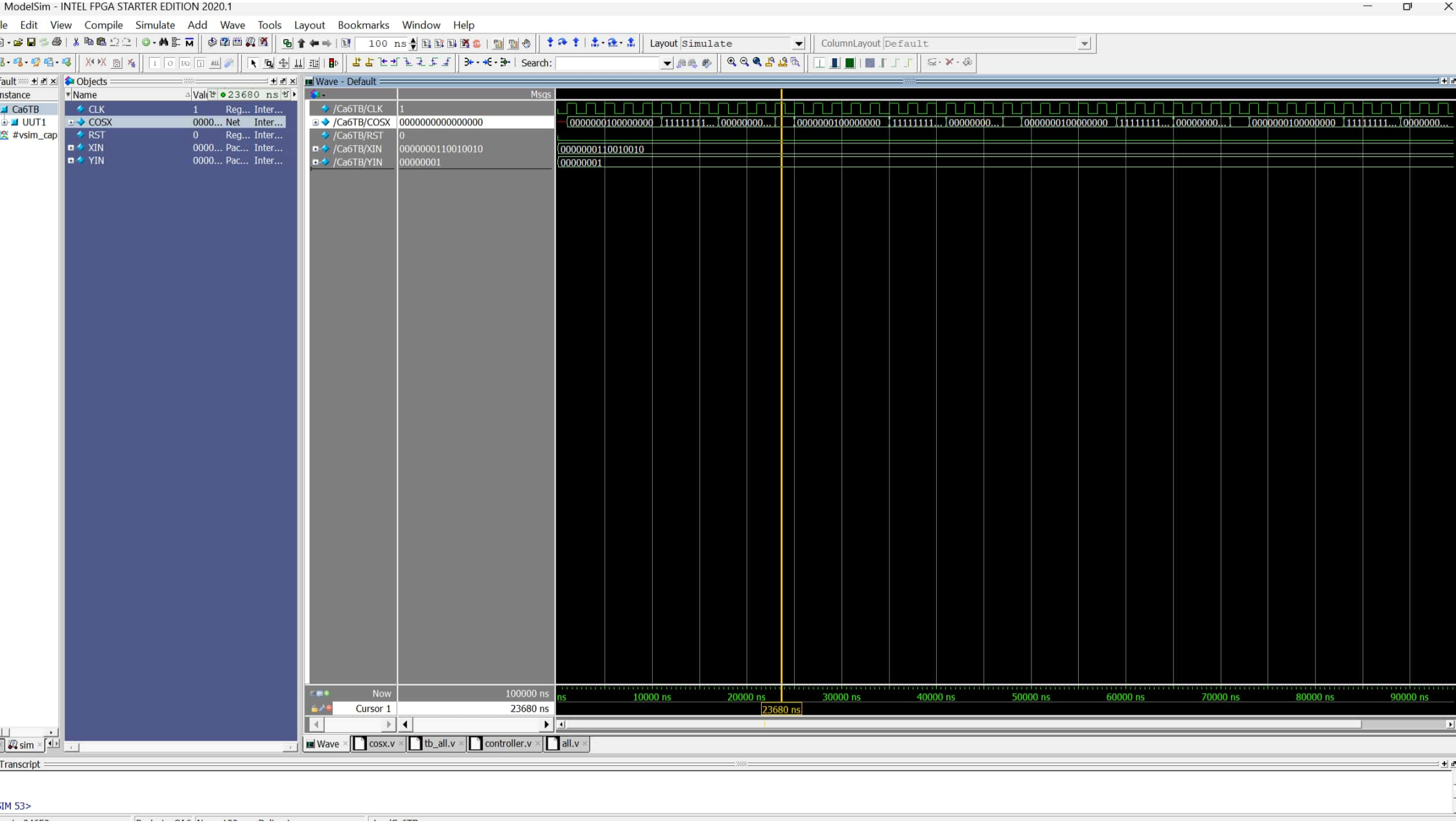

Quartus Prime Lite Edition - C:/Users/ROG/Desktop/CA6/cosx/cosxQ - cosxQ
Edit View Project Assignments Processing Tools Window Help
Search altera.com
cosxQ
Files
cosxQ.v
cosx.v
controller.v
Compilation
Task
Compile Design
Analysis & Synthesis
Fitter (Place & Route)
Assembler (Generate programm
Timing Analysis
EDA Netlist Writer
Edit Settings
cosxQ.v
Compilation Report - cosxQ
controller.v
Table of Contents
Flow Summary
Flow Settings
Flow Non-Default Global S
Flow Elapsed Time
Flow OS Summary
Flow Log
Analysis & Synthesis
Fitter
Assembler
Timing Analyzer
EDA Netlist Writer
Flow Messages
Flow Suppressed Message
Flow Summary
<<Filter>>
Flow Status Successful - Tue Jan 09 23:42:03 2024
Quartus Prime Version 20.1.0 Build 711 06/05/2020 SJ Lite Edition
Revision Name cosxQ
Top-level Entity Name all
Family Cyclone IV GX
Device EP4CGX15BF14A7
Timing Models Final
Total logic elements 427 / 14,400 (3 %)
Total registers 66
Total pins 42 / 81 (52 %)
Total virtual pins 0
Total memory bits 0 / 552,960 (0 %)
Embedded Multiplier 9-bit elements 0
Total GXB Receiver Channel PCS 0 / 2 (0 %)
Total GXB Receiver Channel PMA 0 / 2 (0 %)
Total GXB Transmitter Channel PCS 0 / 2 (0 %)
Total GXB Transmitter Channel PMA 0 / 2 (0 %)
Total PLLs 0 / 3 (0 %)
IP Catalog
Installed IP
Project Directory
No Selection Available
Library
Basic Functions
DSP
Interface Protocols
Processors and Periphe
University Program
Search for Partner IP
+ Add...
All
<<Filter>>
Find...
Find Next
Type ID Message
332102 Design is not fully constrained for setup requirements
332102 Design is not fully constrained for hold requirements
Quartus Prime Timing Analyzer was successful. 0 errors, 5 warnings
Running Quartus Prime EDA Netlist Writer
Command: quartus_eda --read_settings_files=off --write_settings_files=off cosxQ -c cosxQ
18236 Number of processors has not been specified which may cause overloading on shared machines. Set the global assignment NUM_PARALLEL_PROCESSORS in your QSF to an appropriate value for best performanc
204019 Generated file cosxQ_7_1200mv_125c_slow.vo in folder "C:/Users/ROG/Desktop/CA6/cosx/simulation/modelsim/" for EDA simulation tool
204019 Generated file cosxQ_7_1200mv_-40c_slow.vo in folder "C:/Users/ROG/Desktop/CA6/cosx/simulation/modelsim/" for EDA simulation tool
204019 Generated file cosxQ_min_1200mv_-40c_fast.vo in folder "C:/Users/ROG/Desktop/CA6/cosx/simulation/modelsim/" for EDA simulation tool
204019 Generated file cosxQ.vo in folder "C:/Users/ROG/Desktop/CA6/cosx/simulation/modelsim/" for EDA simulation tool
204019 Generated file cosxQ_7_1200mv_125c_v_slow.sdo in folder "C:/Users/ROG/Desktop/CA6/cosx/simulation/modelsim/" for EDA simulation tool
204019 Generated file cosxQ_7_1200mv_-40c_v_slow.sdo in folder "C:/Users/ROG/Desktop/CA6/cosx/simulation/modelsim/" for EDA simulation tool
204019 Generated file cosxQ_min_1200mv_-40c_v_fast.sdo in folder "C:/Users/ROG/Desktop/CA6/cosx/simulation/modelsim/" for EDA simulation tool
204019 Generated file cosxQ_v.sdo in folder "C:/Users/ROG/Desktop/CA6/cosx/simulation/modelsim/" for EDA simulation tool
Quartus Prime EDA Netlist Writer was successful. 0 errors, 1 warning
293000 Quartus Prime Full Compilation was successful. 0 errors, 50 warnings
System
Processing (148)

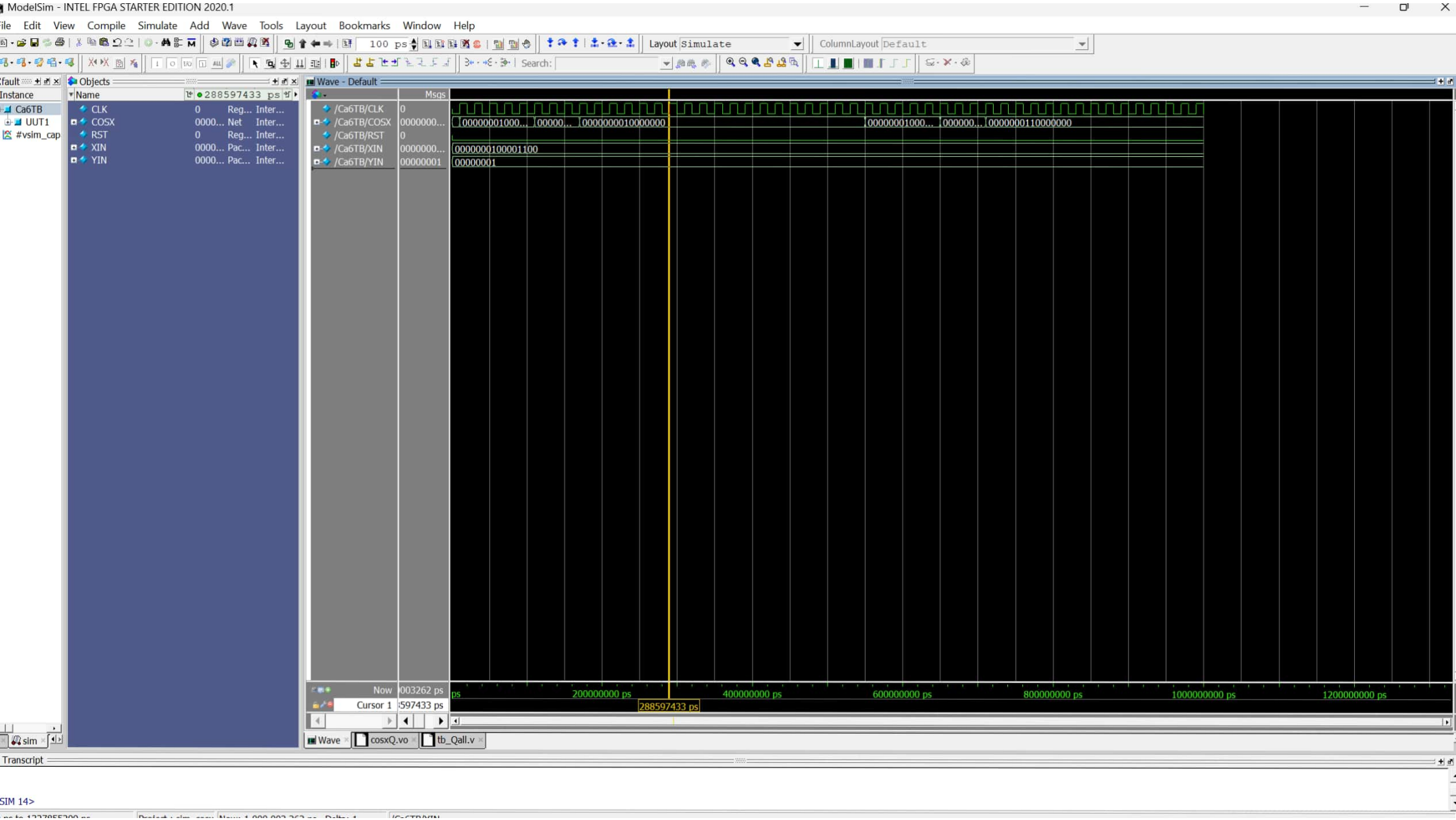

Quartus Prime Lite Edition - C:/Users/ROG/Desktop/CA6/cosx/cosxQ - cosxQ
Edit View Project Assignments Processing Tools Window Help
Search altera.com
cosxQ
Files
cosxQ.v
cosx.v
controller.v
Compilation
Task
Compile Design
Analysis & Synthesis
Fitter (Place & Route)
Assembler (Generate programm
Timing Analysis
EDA Netlist Writer
Edit Settings
cosxQ.v
Compilation Report - cosxQ
controller.v
Table of Contents
Pin-Out File
Resource Section
I/O Rules Section
Device Options
Operating Settings a
Messages
Suppressed Messag
Assembler
Summary
Settings
Generated Files
Device Options: C:/U
Messages
Timing Analyzer
Summary
Parallel Compilation
Clocks
Slow 1200mV 125C
Slow 1200mV -40C
Fast 1200mV -40C M
Multicorner Timing A
Advanced I/O Timin
Clock Transfers
Report TCCS
Parallel Compilation
<<Filter>>
Processors Number
1 Number detected on machine 16
2 Maximum allowed 16
3
4 Average used 1.12
5 Maximum used 16
6
7 Usage by Processor % Time Used
1 Processor 1 100.0%
2 Processors 2-16 0.8%
IP Catalog
Installed IP
Project Directory
No Selection Available
Library
Basic Functions
DSP
Interface Protocols
Processors and Periphe
University Program
Search for Partner IP
+ Add...
All
<<Filter>>
Find...
Find Next
Type ID Message
332102 Design is not fully constrained for setup requirements
332102 Design is not fully constrained for hold requirements
Quartus Prime Timing Analyzer was successful. 0 errors, 5 warnings
Running Quartus Prime EDA Netlist Writer
Command: quartus_eda --read_settings_files=off --write_settings_files=off cosxQ -c cosxQ
18236 Number of processors has not been specified which may cause overloading on shared machines. Set the global assignment NUM_PARALLEL_PROCESSORS in your QSF to an appropriate value for best performanc
204019 Generated file cosxQ_7_1200mv_125c_slow.vo in folder "C:/Users/ROG/Desktop/CA6/cosx/simulation/modelsim/" for EDA simulation tool
204019 Generated file cosxQ_7_1200mv_-40c_slow.vo in folder "C:/Users/ROG/Desktop/CA6/cosx/simulation/modelsim/" for EDA simulation tool
204019 Generated file cosxQ_min_1200mv_-40c_fast.vo in folder "C:/Users/ROG/Desktop/CA6/cosx/simulation/modelsim/" for EDA simulation tool
204019 Generated file cosxQ.vo in folder "C:/Users/ROG/Desktop/CA6/cosx/simulation/modelsim/" for EDA simulation tool
204019 Generated file cosxQ_7_1200mv_125c_v_slow.sdo in folder "C:/Users/ROG/Desktop/CA6/cosx/simulation/modelsim/" for EDA simulation tool
204019 Generated file cosxQ_7_1200mv_-40c_v_slow.sdo in folder "C:/Users/ROG/Desktop/CA6/cosx/simulation/modelsim/" for EDA simulation tool
204019 Generated file cosxQ_min_1200mv_-40c_v_fast.sdo in folder "C:/Users/ROG/Desktop/CA6/cosx/simulation/modelsim/" for EDA simulation tool
204019 Generated file cosxQ_v.sdo in folder "C:/Users/ROG/Desktop/CA6/cosx/simulation/modelsim/" for EDA simulation tool
Quartus Prime EDA Netlist Writer was successful. 0 errors, 1 warning
293000 Quartus Prime Full Compilation was successful. 0 errors, 50 warnings
System
Processing (148)

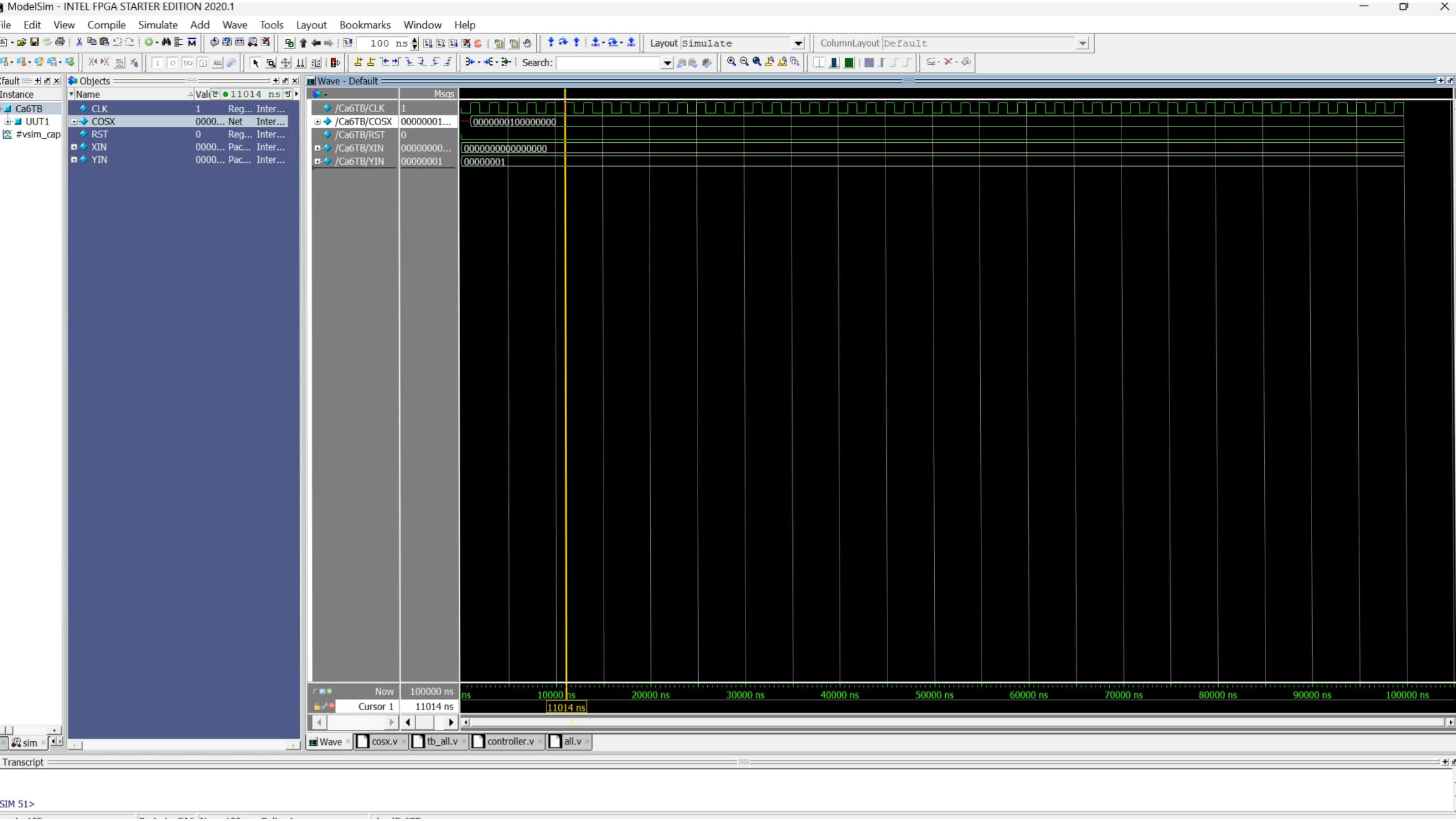

Quartus Prime Lite Edition - C:/Users/ROG/Desktop/CA6/cosx/cosxQ - cosxQ
Edit View Project Assignments Processing Tools Window Help
Search altera.com
cosxQ
Files
cosxQ.v
cosx.v
controller.v
Compilation
Task
Compile Design
Analysis & Synthesis
Fitter (Place & Route)
Assembler (Generate programm
Timing Analysis
EDA Netlist Writer
Edit Settings
cosxQ.v
Compilation Report - cosxQ
controller.v
Table of Contents
Source Files Read
Resource Usage Sun
Resource Utilization
State Machines
State Machine - |a
Optimization Results
Register Statistics
Multiplexer Statist
Parameter Settings I
Parameter Setting
Parameter Setting
Parameter Setting
Parameter Setting
LPM Parameter Sett
Multipliers
lpm_mult Parar
Post-Synthesis Netli
Elapsed Time Per Pa
Messages
Fitter
Summary
Settings
Parallel Compilation
Incremental Compil
Fitter Summary
<<Filter>>
Fitter Status Successful - Tue Jan 09 23:41:57 2024
Quartus Prime Version 20.1.0 Build 711 06/05/2020 SJ Lite Edition
Revision Name cosxQ
Top-level Entity Name all
Family Cyclone IV GX
Device EP4CGX15BF14A7
Timing Models Final
Total logic elements 427 / 14,400 (3 %)
Total registers 66
Total pins 42 / 81 (52 %)
Total virtual pins 0
Total memory bits 0 / 552,960 (0 %)
Embedded Multiplier 9-bit elements 0
Total GXB Receiver Channel PCS 0 / 2 (0 %)
Total GXB Receiver Channel PMA 0 / 2 (0 %)
Total GXB Transmitter Channel PCS 0 / 2 (0 %)
Total GXB Transmitter Channel PMA 0 / 2 (0 %)
Total PLLs 0 / 3 (0 %)
IP Catalog
Installed IP
Project Directory
No Selection Available
Library
Basic Functions
DSP
Interface Protocols
Processors and Periphe
University Program
Search for Partner IP
+ Add...
All
<<Filter>>
Find...
Find Next
Type ID Message
332102 Design is not fully constrained for setup requirements
332102 Design is not fully constrained for hold requirements
Quartus Prime Timing Analyzer was successful. 0 errors, 5 warnings
Running Quartus Prime EDA Netlist Writer
Command: quartus_eda --read_settings_files=off --write_settings_files=off cosxQ -c cosxQ
18236 Number of processors has not been specified which may cause overloading on shared machines. Set the global assignment NUM_PARALLEL_PROCESSORS in your QSF to an appropriate value for best performanc
204019 Generated file cosxQ_7_1200mv_125c_slow.vo in folder "C:/Users/ROG/Desktop/CA6/cosx/simulation/modelsim/" for EDA simulation tool
204019 Generated file cosxQ_7_1200mv_-40c_slow.vo in folder "C:/Users/ROG/Desktop/CA6/cosx/simulation/modelsim/" for EDA simulation tool
204019 Generated file cosxQ_min_1200mv_-40c_fast.vo in folder "C:/Users/ROG/Desktop/CA6/cosx/simulation/modelsim/" for EDA simulation tool
204019 Generated file cosxQ.vo in folder "C:/Users/ROG/Desktop/CA6/cosx/simulation/modelsim/" for EDA simulation tool
204019 Generated file cosxQ_7_1200mv_125c_v_slow.sdo in folder "C:/Users/ROG/Desktop/CA6/cosx/simulation/modelsim/" for EDA simulation tool
204019 Generated file cosxQ_7_1200mv_-40c_v_slow.sdo in folder "C:/Users/ROG/Desktop/CA6/cosx/simulation/modelsim/" for EDA simulation tool
204019 Generated file cosxQ_min_1200mv_-40c_v_fast.sdo in folder "C:/Users/ROG/Desktop/CA6/cosx/simulation/modelsim/" for EDA simulation tool
204019 Generated file cosxQ_v.sdo in folder "C:/Users/ROG/Desktop/CA6/cosx/simulation/modelsim/" for EDA simulation tool
Quartus Prime EDA Netlist Writer was successful. 0 errors, 1 warning
293000 Quartus Prime Full Compilation was successful. 0 errors, 50 warnings
System
Processing (148)

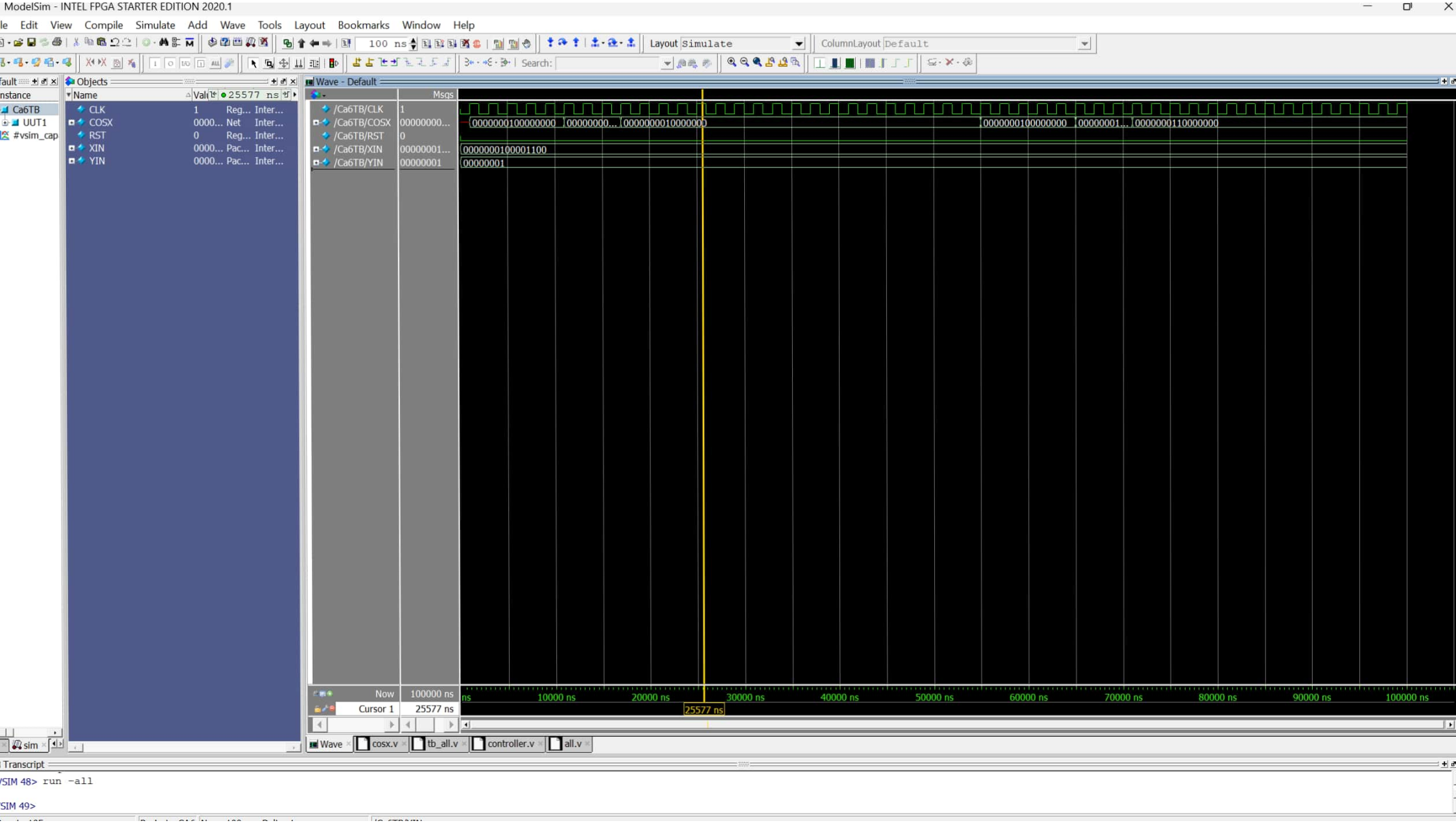

Quartus Prime Lite Edition - C:/Users/ROG/Desktop/CA6/cosx/cosxQ - cosxQ
Edit View Project Assignments Processing Tools Window Help
Search altera.com
cosxQ
Files
cosxQ.v
cosx.v
controller.v
Compilation
Task
Compile Design
Analysis & Synthesis
Fitter (Place & Route)
Assembler (Generate programm
Timing Analysis
EDA Netlist Writer
Edit Settings
cosxQ.v
Compilation Report - cosxQ
controller.v
Table of Contents
Flow Summary
Flow Settings
Flow Non-Default Glob
Flow Elapsed Time
Flow OS Summary
Flow Log
Analysis & Synthesis
Summary
Settings
Parallel Compilation
Source Files Read
Resource Usage Sun
Resource Utilization
State Machines
Optimization Results
Parameter Settings I
LPM Parameter Sett
Post-Synthesis Netli
Elapsed Time Per Pa
Messages
Fitter
Assembler
Timing Analyzer
EDA Netlist Writer
Analysis & Synthesis Summary
<<Filter>>
Analysis & Synthesis Status Successful - Tue Jan 09 23:41:50 2024
Quartus Prime Version 20.1.0 Build 711 06/05/2020 SJ Lite Edition
Revision Name cosxQ
Top-level Entity Name all
Family Cyclone IV GX
Total logic elements 437
Total registers 66
Total pins 42
Total virtual pins 0
Total memory bits 0
Embedded Multiplier 9-bit elements 0
Total GXB Receiver Channel PCS 0
Total GXB Receiver Channel PMA 0
Total GXB Transmitter Channel PCS 0
Total GXB Transmitter Channel PMA 0
Total PLLs 0
IP Catalog
Installed IP
Project Directory
No Selection Available
Library
Basic Functions
DSP
Interface Protocols
Processors and Periphe
University Program
Search for Partner IP
+ Add...
All
<<Filter>>
Find...
Find Next
Type ID Message
332102 Design is not fully constrained for setup requirements
332102 Design is not fully constrained for hold requirements
Quartus Prime Timing Analyzer was successful. 0 errors, 5 warnings
Running Quartus Prime EDA Netlist Writer
Command: quartus_eda --read_settings_files=off --write_settings_files=off cosxQ -c cosxQ
18236 Number of processors has not been specified which may cause overloading on shared machines. Set the global assignment NUM_PARALLEL_PROCESSORS in your QSF to an appropriate value for best performanc
204019 Generated file cosxQ_7_1200mv_125c_slow.vo in folder "C:/Users/ROG/Desktop/CA6/cosx/simulation/modelsim/" for EDA simulation tool
204019 Generated file cosxQ_7_1200mv_-40c_slow.vo in folder "C:/Users/ROG/Desktop/CA6/cosx/simulation/modelsim/" for EDA simulation tool
204019 Generated file cosxQ_min_1200mv_-40c_fast.vo in folder "C:/Users/ROG/Desktop/CA6/cosx/simulation/modelsim/" for EDA simulation tool
204019 Generated file cosxQ.vo in folder "C:/Users/ROG/Desktop/CA6/cosx/simulation/modelsim/" for EDA simulation tool
204019 Generated file cosxQ_7_1200mv_125c_v_slow.sdo in folder "C:/Users/ROG/Desktop/CA6/cosx/simulation/modelsim/" for EDA simulation tool
204019 Generated file cosxQ_7_1200mv_-40c_v_slow.sdo in folder "C:/Users/ROG/Desktop/CA6/cosx/simulation/modelsim/" for EDA simulation tool
204019 Generated file cosxQ_min_1200mv_-40c_v_fast.sdo in folder "C:/Users/ROG/Desktop/CA6/cosx/simulation/modelsim/" for EDA simulation tool
204019 Generated file cosxQ_v.sdo in folder "C:/Users/ROG/Desktop/CA6/cosx/simulation/modelsim/" for EDA simulation tool
Quartus Prime EDA Netlist Writer was successful. 0 errors, 1 warning
293000 Quartus Prime Full Compilation was successful. 0 errors, 50 warnings
System
Processing (148)


Quartus Prime Lite Edition - C:/Users/ROG/Desktop/CA6/cosx/cosxQ - cosxQ
File Edit View Project Assignments Processing Tools Window Help
Search altera.com
cosxQ
Project Navigator
Files
cosxQ.v
cosx.v
controller.v
Tasks
Compilation
Task
Compile Design
Analysis & Synthesis
Fitter (Place & Route)
Assembler (Generate programm
Timing Analysis
EDA Netlist Writer
Edit Settings
cosxQ.v
Compilation Report - cosxQ
controller.v
Table of Contents
Messages
Fitter
Summary
Settings
Parallel Compilation
Incremental Compil
Pin-Out File
Resource Section
I/O Rules Section
Device Options
Operating Settings a
Messages
Suppressed Messag
Assembler
Summary
Settings
Generated Files
Device Options: C:/U
Messages
Timing Analyzer
Summary
Parallel Compilation
Clocks
Slow 1200mV 125C
Timing Analyzer Summary
<<Filter>>
Quartus Prime Version Version 20.1.0 Build 711 06/05/2020 SJ Lite Edition
Timing Analyzer Legacy Timing Analyzer
Revision Name cosxQ
Device Family Cyclone IV GX
Device Name EP4CGX15BF14A7
Timing Models Final
Delay Model Combined
Rise/Fall Delays Enabled
IP Catalog
Installed IP
Project Directory
No Selection Available
Library
Basic Functions
DSP
Interface Protocols
Processors and Periphe
University Program
Search for Partner IP
+ Add...
All
<<Filter>>
Find...
Find Next
Type ID Message
332102 Design is not fully constrained for setup requirements
332102 Design is not fully constrained for hold requirements
Quartus Prime Timing Analyzer was successful. 0 errors, 5 warnings
Running Quartus Prime EDA Netlist Writer
Command: quartus_eda --read_settings_files=off --write_settings_files=off cosxQ -c cosxQ
18236 Number of processors has not been specified which may cause overloading on shared machines. Set the global assignment NUM_PARALLEL_PROCESSORS in your QSF to an appropriate value for best performanc
204019 Generated file cosxQ_7_1200mv_125c_slow.vo in folder "C:/Users/ROG/Desktop/CA6/cosx/simulation/modelsim/" for EDA simulation tool
204019 Generated file cosxQ_7_1200mv_-40c_slow.vo in folder "C:/Users/ROG/Desktop/CA6/cosx/simulation/modelsim/" for EDA simulation tool
204019 Generated file cosxQ_min_1200mv_-40c_fast.vo in folder "C:/Users/ROG/Desktop/CA6/cosx/simulation/modelsim/" for EDA simulation tool
204019 Generated file cosxQ.vo in folder "C:/Users/ROG/Desktop/CA6/cosx/simulation/modelsim/" for EDA simulation tool
204019 Generated file cosxQ_7_1200mv_125c_v_slow.sdo in folder "C:/Users/ROG/Desktop/CA6/cosx/simulation/modelsim/" for EDA simulation tool
204019 Generated file cosxQ_7_1200mv_-40c_v_slow.sdo in folder "C:/Users/ROG/Desktop/CA6/cosx/simulation/modelsim/" for EDA simulation tool
204019 Generated file cosxQ_min_1200mv_-40c_v_fast.sdo in folder "C:/Users/ROG/Desktop/CA6/cosx/simulation/modelsim/" for EDA simulation tool
204019 Generated file cosxQ_v.sdo in folder "C:/Users/ROG/Desktop/CA6/cosx/simulation/modelsim/" for EDA simulation tool
Quartus Prime EDA Netlist Writer was successful. 0 errors, 1 warning
293000 Quartus Prime Full Compilation was successful. 0 errors, 50 warnings


ModelSim - INTEL FPGA STARTER EDITION 2020.1
File Edit View Compile Simulate Add Wave Tools Layout Bookmarks Window Help
Objects
Name
CLK
COSX
RST
XIN
YIN
Wave - Default
Msgs
/Ca6TB/CLK
/Ca6TB/COSX
/Ca6TB/RST
/Ca6TB/XIN
/Ca6TB/YIN
0000000110010010
00000001
Now
100000 ns
Cursor 1
23680 ns
10000 ns
20000 ns
30000 ns
40000 ns
50000 ns
60000 ns
70000 ns
80000 ns
90000 ns
Wave
cosx.v
tb_all.v
controller.v
all.v
Transcript


ModelSim - INTEL FPGA STARTER EDITION 2020.1
File Edit View Compile Simulate Add Wave Tools Layout Bookmarks Window Help
Layout Simulate
ColumnLayout Default
Search:
Objects
Name
288597433 ps
CLK 0 Reg... Inter...
COSX 0000... Net Inter...
RST 0 Reg... Inter...
XIN 0000... Pac... Inter...
YIN 0000... Pac... Inter...
Wave - Default
Msgs
/Ca6TB/CLK 0
/Ca6TB/COSX 0000000...
/Ca6TB/RST 0
/Ca6TB/XIN 0000000...
/Ca6TB/YIN 00000001
00000001000...
00000...
0000000010000000
00000001000...
000000...
0000000110000000
0000000100001100
00000001
Now 003262 ps
Cursor 1 :597433 ps
200000000 ps
400000000 ps
600000000 ps
800000000 ps
1000000000 ps
1200000000 ps
288597433 ps
Wave
cosxQ.vo
tb_Qall.v
Transcript
SIM 14>


ModelSim - INTEL FPGA STARTER EDITION 2020.1
File Edit View Compile Simulate Add Wave Tools Layout Bookmarks Window Help
Objects
Name
CLK
COSX
RST
XIN
YIN
Wave - Default
Msgs
/Ca6TB/CLK
/Ca6TB/COSX
/Ca6TB/RST
/Ca6TB/XIN
/Ca6TB/YIN
00000001000000000
0000000000000000
00000001
Now
100000 ns
Cursor 1
11014 ns
10000 ns
20000 ns
30000 ns
40000 ns
50000 ns
60000 ns
70000 ns
80000 ns
90000 ns
100000 ns
Wave
cosx.v
tb_all.v
controller.v
all.v
Transcript
SIM 51>


ModelSim - INTEL FPGA STARTER EDITION 2020.1
File Edit View Compile Simulate Add Wave Tools Layout Bookmarks Window Help
Objects
Name
CLK
COSX
RST
XIN
YIN
Wave - Default
Msgs
/Ca6TB/CLK
/Ca6TB/COSX
/Ca6TB/RST
/Ca6TB/XIN
/Ca6TB/YIN
0000000100001100
00000001
Now
100000 ns
Cursor 1
25577 ns
10000 ns
20000 ns
30000 ns
40000 ns
50000 ns
60000 ns
70000 ns
80000 ns
90000 ns
100000 ns
Wave
cosx.v
tb_all.v
controller.v
all.v
Transcript
VSIM 48> run -all
VSIM 49>