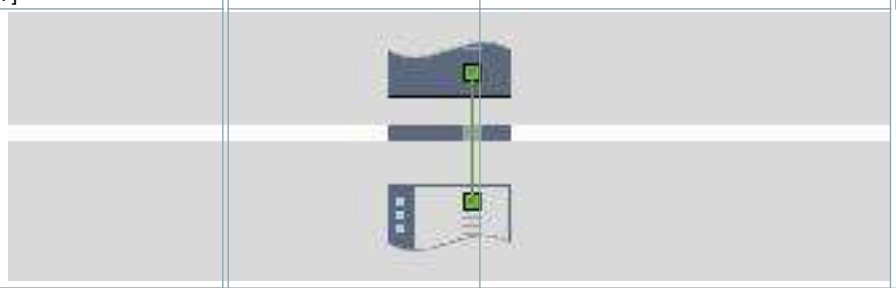
Compressor / PLC_1 [CPU 1212C DC/DC/Rly]

S7-1200 station_1

PLC_1					
General\Project information					
Name	PLC_1	**Author**	Sobhan Sahaf	**Comment**	
Slot	1	**Rack**	0		
General\Catalog information					
Short designation	CPU 1212C DC/DC/Rly	**Description**	Work memory 100 KB; 24VDC power supply with DI8 x 24VDC SINK/SOURCE, DQ6 x relay and AI2 on board; 4 high-speed counters (expandable with digital signal board) and 4 pulse outputs on board; signal board expands on-board I/O; up to 3 communication modules for serial communication; up to 2 signal modules for I/O expansion; PROFINET IO controller, I-device, transport protocol TCP/IP, secure Open User Communication, S7 communication, Web server, OPC UA: Server DA	**Article number**	6ES7 212-1HE40-0XB0
Firmware version	V4.6		False		
General\Identification & Maintenance					
Plant designation		**Location identifier**		**Installation date**	2025-12-07 12:32:43.142
Additional information					
General\Checksums					
Text lists	FA 70 E8 75 1D 5A 8E 29	**Software**	Not available (compile necessary)		
PROFINET interface [X1]\General					
Name	PROFINET interface_1	**Author**	Amin Hashemi	**Comment**	
PROFINET interface [X1]\General\Project information					
Name	DI 8/DQ 6_1	**Comment**		**Name**	AI 2_1
Comment					
PROFINET interface [X1]\Ethernet addresses\Interface networked with					
Subnet:	Not connected				
PROFINET interface [X1]\Ethernet addresses\Internet protocol version 4 (IPv4)					
IP configuration	Set IP address in the project	**IP address:**	192.168.0.1	**Subnet mask:**	255.255.255.0
Use router	False				
PROFINET interface [X1]\Ethernet addresses\PROFINET					
PROFINET device name is set directly at the device	False	**Generate PROFINET device name automatically**	True	**PROFINET device name:**	plc_1
Converted name:	plcxb1d0ed	**Device number:**	0		
PROFINET interface [X1]\Time synchronization					
Enable time synchronization via NTP server	Enable time synchronization via NTP server		IP addresses	**Server 1**	0.0.0.0
Server 2	0.0.0.0	**Server 3**	0.0.0.0	**Server 4**	0.0.0.0
Update interval	10sec			**CPU synchronizes the modules of the device.**	No synchronization
PROFINET interface [X1]\Digital inputs\Channel0					
Channel address	I0.0	**Input filters**	6.4 millisec	**Enable pulse catch**	0
PROFINET interface [X1]\Digital inputs\Channel0					
Enable rising edge detection	0	**Prefix Event Rising Edge**	49152	**Event name:**	0
Hardware interrupt:	0	**Rising edge0**	Rising edge0		
PROFINET interface [X1]\Digital inputs\Channel0					
Enable falling edge detection	0	**Prefix Event Falling Edge**	49280	**Event name:**	0
Hardware interrupt:	0	**Falling edge0**	Falling edge0		
PROFINET interface [X1]\Digital inputs\Channel1					
Channel address	I0.1	**Input filters**	6.4 millisec	**Enable pulse catch**	0
PROFINET interface [X1]\Digital inputs\Channel1					
Enable rising edge detection	0	**Prefix Event Rising Edge**	49153	**Event name:**	0
Hardware interrupt:	0	**Rising edge1**	Rising edge1		
PROFINET interface [X1]\Digital inputs\Channel1					
Enable falling edge detection	0	**Prefix Event Falling Edge**	49281	**Event name:**	0
Hardware interrupt:	0	**Falling edge1**	Falling edge1		
PROFINET interface [X1]\Digital inputs\Channel2					
Channel address	I0.2	**Input filters**	6.4 millisec	**Enable pulse catch**	0
PROFINET interface [X1]\Digital inputs\Channel2					
Enable rising edge detection	0	**Prefix Event Rising Edge**	49154	**Event name:**	0
Hardware interrupt:	0	**Rising edge2**	Rising edge2		
PROFINET interface [X1]\Digital inputs\Channel2					
Enable falling edge detection	0	**Prefix Event Falling Edge**	49282	**Event name:**	0
Hardware interrupt:	0	**Falling edge2**	Falling edge2		
PROFINET interface [X1]\Digital inputs\Channel3					
Channel address	I0.3	**Input filters**	6.4 millisec	**Enable pulse catch**	0
PROFINET interface [X1]\Digital inputs\Channel3					
Enable rising edge detection	0	**Prefix Event Rising Edge**	49155	**Event name:**	0

Hardware interrupt:	0	**Rising edge3**	Rising edge3		
PROFINET interface [X1]\Digital inputs\Channel3					
Enable falling edge detection	0	**Prefix Event Falling Edge**	49283	**Event name:**	0
Hardware interrupt:	0	**Falling edge3**	Falling edge3		
PROFINET interface [X1]\Digital inputs\Channel4					
Channel address	I0.4	**Input filters**	6.4 millisec	**Enable pulse catch**	0
PROFINET interface [X1]\Digital inputs\Channel4					
Enable rising edge detection	0	**Prefix Event Rising Edge**	49156	**Event name:**	0
Hardware interrupt:	0	**Rising edge4**	Rising edge4		
PROFINET interface [X1]\Digital inputs\Channel4					
Enable falling edge detection	0	**Prefix Event Falling Edge**	49284	**Event name:**	0
Hardware interrupt:	0	**Falling edge4**	Falling edge4		
PROFINET interface [X1]\Digital inputs\Channel5					
Channel address	I0.5	**Input filters**	6.4 millisec	**Enable pulse catch**	0
PROFINET interface [X1]\Digital inputs\Channel5					
Enable rising edge detection	0	**Prefix Event Rising Edge**	49157	**Event name:**	0
Hardware interrupt:	0	**Rising edge5**	Rising edge5		
PROFINET interface [X1]\Digital inputs\Channel5					
Enable falling edge detection	0	**Prefix Event Falling Edge**	49285	**Event name:**	0
Hardware interrupt:	0	**Falling edge5**	Falling edge5		
PROFINET interface [X1]\Digital inputs\Channel6					
Channel address	I0.6	**Input filters**	6.4 millisec	**Enable pulse catch**	0
PROFINET interface [X1]\Digital inputs\Channel6					
Enable rising edge detection	0	**Prefix Event Rising Edge**	49158	**Event name:**	0
Hardware interrupt:	0	**Rising edge6**	Rising edge6		
PROFINET interface [X1]\Digital inputs\Channel6					
Enable falling edge detection	0	**Prefix Event Falling Edge**	49286	**Event name:**	0
Hardware interrupt:	0	**Falling edge6**	Falling edge6		
PROFINET interface [X1]\Digital inputs\Channel7					
Channel address	I0.7	**Input filters**	6.4 millisec	**Enable pulse catch**	0
PROFINET interface [X1]\Digital inputs\Channel7					
Enable rising edge detection	0	**Prefix Event Rising Edge**	49159	**Event name:**	0
Hardware interrupt:	0	**Rising edge7**	Rising edge7		
PROFINET interface [X1]\Digital inputs\Channel7					
Enable falling edge detection	0	**Prefix Event Falling Edge**	49287	**Event name:**	0
Hardware interrupt:	0	**Falling edge7**	Falling edge7		
PROFINET interface [X1]\Analog inputs\Noise reduction					
Integration time	50 Hz (20 ms)				
PROFINET interface [X1]\Analog inputs\Channel0					
Channel address	IW64	**Measurement type**	Voltage	**Voltage range**	0..10 V
Smoothing	Weak (4 cycles)			**Enable overflow diag-nostics**	1
PROFINET interface [X1]\Analog inputs\Channel1					
Channel address	IW66	**Measurement type**	Voltage	**Voltage range**	0..10 V
Smoothing	Weak (4 cycles)			**Enable overflow diag-nostics**	1
PROFINET interface [X1]\Digital outputs					
Reaction to CPU STOP	Use substitute value				
PROFINET interface [X1]\Digital outputs\Channel0					
Channel address	Q0.0	**Substitute a value of 1 on a change from RUN to STOP.**	0		
PROFINET interface [X1]\Digital outputs\Channel1					
Channel address	Q0.1	**Substitute a value of 1 on a change from RUN to STOP.**	0		
PROFINET interface [X1]\Digital outputs\Channel2					
Channel address	Q0.2	**Substitute a value of 1 on a change from RUN to STOP.**	0		
PROFINET interface [X1]\Digital outputs\Channel3					
Channel address	Q0.3	**Substitute a value of 1 on a change from RUN to STOP.**	0		
PROFINET interface [X1]\Digital outputs\Channel4					
Channel address	Q0.4	**Substitute a value of 1 on a change from RUN to STOP.**	0		
PROFINET interface [X1]\Digital outputs\Channel5					
Channel address	Q0.5	**Substitute a value of 1 on a change from RUN to STOP.**	0		
PROFINET interface [X1]\Operating mode					
IO controller	True	**IO system**		**Device number**	0
IO device	False				
PROFINET interface [X1]\I/O addresses\Input addresses					
Start address	0.0	**End address**	0.7	**Organization block**	0
Process image	0				
PROFINET interface [X1]\I/O addresses\Input addresses					
Start address	64	**End address**	67	**Organization block**	0

Process image	0				
PROFINET interface [X1]\I/O addresses\Output addresses					
Start address	0.0	**End address**	0.7	**Organization block**	0
Process image	0				
PROFINET interface [X1]\Advanced options\Interface options					
Support device replacement without exchangeable medium	True	**Permit overwriting of device names of all assigned IO devices**	False	**Use IEC V2.2 LLDP mode**	False
Keep-Alive connection monitoring:	30s				
PROFINET interface [X1]\Advanced options\Real time settings\IO communication					
Send clock:	1.000ms				
PROFINET interface [X1]\Advanced options\Real time settings\Real time options					
Calculated bandwidth for cyclic IO data:	0.000ms	**Calculated bandwidth for cyclic IO data:**	0.000%		
PROFINET interface [X1]\Advanced options\Port [X1 P1]\General					
Name	Port_1	**Author**	Amin Hashemi	**Comment**	
PROFINET interface [X1]\Advanced options\Port [X1 P1]\Port interconnection\Local port:					
Local port:	PLC_1\PROFINET interface_1 [X1]\Port_1 [X1 P1]	**Medium:**	Copper	**Cable name:**	---
					
PROFINET interface [X1]\Advanced options\Port [X1 P1]\Port interconnection\Partner port:					
	Monitoring of partner port is not possible	**Partner port:**	Any partner		
PROFINET interface [X1]\Advanced options\Port [X1 P1]\Port options\Activate					
Activate this port for use	True				
PROFINET interface [X1]\Advanced options\Port [X1 P1]\Port options\Connection					
Transmission rate / duplex:	Automatic	**Monitor**	False	**Enable autonegotiation**	True
PROFINET interface [X1]\Advanced options\Port [X1 P1]\Port options\Boundaries					
End of detection of accessible devices	False	**End of topology discovery**	False	**End of the sync domain**	False
PROFINET interface [X1]\Web server access					
Enable Web server for the IP address of this interface	False	**The Web server must also be activated in the properties of the PLC.**			
High speed counters (HSC)\HSC1\General\Enable					
Enable this high speed counter	0	**Enable this high speed counter**	0	**Enable this high speed counter**	0
Enable this high speed counter	0	**Enable this high speed counter**	0	**Enable this high speed counter**	0
High speed counters (HSC)\HSC1\General\Project information					
Name	HSC_1	**Comment**		**Name**	HSC_2
Comment		**Name**	HSC_3	**Comment**	
Name	HSC_4	**Comment**		**Name**	HSC_5
Comment		**Name**	HSC_6	**Comment**	
High speed counters (HSC)\HSC1\I/O addresses\Input addresses					
Start address	1000.0	**End address**	1003.7	**Start address**	1004.0
End address	1007.7	**Organization block**	0	**Start address**	1008.0
End address	1011.7	**Organization block**	0	**Process image**	0
Start address	1012.0	**End address**	1015.7	**Organization block**	0
Process image	0	**Start address**	1016.0	**End address**	1019.7
Organization block	0	**Process image**	0	**Start address**	1020.0
End address	1023.7	**Organization block**	0	**Process image**	0
Organization block	0	**Process image**	0	**Process image**	0
Pulse generators (PTO/PWM)\PTO1/PWM1\General\Enable					
Enable this pulse generator	0	**Enable this pulse generator**	0		
Pulse generators (PTO/PWM)\PTO1/PWM1\General\Project information					
Name	Pulse_1	**Comment**		**Name**	Pulse_2
Comment					
Pulse generators (PTO/PWM)\PTO1/PWM1\I/O addresses\Output addresses					
Start address	1000.0	**End address**	1001.7	**Start address**	1002.0
End address	1003.7	**Organization block**	0	**Organization block**	0
Process image	0	**Process image**	0		
Startup					
Startup after POWER ON	Warm restart - mode before POWER OFF	**Comparison preset to actual configuration**	Startup CPU even if mismatch	**Configuration time**	60000ms
OBs should be interruptible	1				
Cycle					
Cycle monitoring time [ms]	150ms			**Enable minimum cycle time for cyclic OBs**	0
Minimum cycle time	1ms				
Communication load					
Cycle load due to communication [%]	20%				

System and clock memory\System memory bits					
Enable the use of system memory byte	0	Address of system memory byte (MBx)	1	First cycle	
Diagnostic status changed		Always 1 (high)		Always 0 (low)	

System and clock memory\Clock memory bits					
Enable the use of clock memory byte	0	Address of clock memory byte (MBx)	0	10 Hz clock	
5 Hz clock		2.5 Hz clock		2 Hz clock	
1.25 Hz clock		1 Hz clock		0.625 Hz clock	
0.5 Hz clock					

Web server\General			
Activate Web server on all modules of this device	False	Permit access only with HTTPS	True

Web server\Automatic update			
Enable automatic update	True	Update interval	0s

Web server\User management	
User name	User rights
Everybody	

Web server\User-defined web pages					
Application name	HTML source path	Default HTML page	Files with dynamic content	Web DB number	Fragment DB number
		index.htm	.htm;.html	333	334

Web server\Overview of interfaces		
Device	Interface	Enabled web server access
PLC_1	PROFINET interface_1	False

User interface languages	
Assign project language	User interface languages
English (United States)	German
English (United States)	English
English (United States)	French
English (United States)	Spanish
English (United States)	Italian
English (United States)	Chinese (simplified)

Time of day\Local time	
Time zone	(UTC +01:00) Berlin, Bern, Brussels, Rome, Stockholm, Vienna

Time of day\Daylight saving time					
Activate daylight saving time	1	Difference between standard and daylight saving time	60min		

Time of day\Daylight saving time\Start of daylight saving time					
Starting week of the month:	Last		Sunday	in	March
at	1:00 a.m.				

Time of day\Daylight saving time\Start of standard time					
	Last		Sunday	in	October
at	2:00 a.m.				

Protection & Security	
Level of protection	No protection

Protection & Security\Connection mechanisms	
Permit access with PUT/GET communication from remote partner	False

Protection & Security\Security event					
Summarize diagnostics in case of high message volume	True	Length of an interval	20	Unit	seconds

Protection & Security\External load memory	
Disable copying from internal load memory to external load memory	False

Advanced configuration\DnsParameterConfigurationMenu	
The Tree-Node DnsConfigurationMenu was not filled by some ACF	

Advanced configuration\Configuration control\Configuration control for central configuration	
Allow to reconfigure the device via the user program	0

Advanced configuration\SNMP\SNMP configuration (Simple Network Management Protocol).	
Activate SNMP	False

Configuration control\Configuration control for central configuration	
Allow to reconfigure the device via the user program	0

Connection resources\				
	Station resources - Reserved - Maximum	**Station resources - Reserved - Configured**	**Station resources - Dynamic - Configured**	**Module resources - PLC_1 [CPU 1212C DC/DC/Rly] - Configured**
Maximum number of resources:		34	34	68
	Maximum	Configured	Configured	Configured
PG communication:	4	-	-	-
HMI communication:	12	0	0	0
S7 communication:	8	0	0	0
Open user communication:	8	0	0	0
Web communication:	2	-	-	-
OPC UA client/server communication:	0	-	-	-
Other communication:	-	-	0	0
Total resources used:		0	0	0
Available resources:		34	34	68

Overview of addresses\Overview of addresses\Overview of addresses					
Inputs	True	**Outputs**	True	**Address gaps**	False
Slot	True				

Type	Addr. from	Addr. to	Module	PIP	Device name	Device number	Size	Master / IO system	Rack	Slot
I	0	0	DI 8/DQ 6_1	Automatic update	PLC_1 [CPU 1212C DC/DC/Rly]	-	1 Bytes	-	0	1 1
O	0	0	DI 8/DQ 6_1	Automatic update	PLC_1 [CPU 1212C DC/DC/Rly]	-	1 Bytes	-	0	1 1
I	64	67	AI 2_1	Automatic update	PLC_1 [CPU 1212C DC/DC/Rly]	-	4 Bytes	-	0	1 2
I	1000	1003	HSC_1	Automatic update	PLC_1 [CPU 1212C DC/DC/Rly]	-	4 Bytes	-	0	1 16
I	1004	1007	HSC_2	Automatic update	PLC_1 [CPU 1212C DC/DC/Rly]	-	4 Bytes	-	0	1 17
I	1008	1011	HSC_3	Automatic update	PLC_1 [CPU 1212C DC/DC/Rly]	-	4 Bytes	-	0	1 18
I	1012	1015	HSC_4	Automatic update	PLC_1 [CPU 1212C DC/DC/Rly]	-	4 Bytes	-	0	1 19
I	1016	1019	HSC_5	Automatic update	PLC_1 [CPU 1212C DC/DC/Rly]	-	4 Bytes	-	0	1 20
I	1020	1023	HSC_6	Automatic update	PLC_1 [CPU 1212C DC/DC/Rly]	-	4 Bytes	-	0	1 21
O	1000	1001	Pulse_1	Automatic update	PLC_1 [CPU 1212C DC/DC/Rly]	-	2 Bytes	-	0	1 32
O	1002	1003	Pulse_2	Automatic update	PLC_1 [CPU 1212C DC/DC/Rly]	-	2 Bytes	-	0	1 33
O	1004	1005	Pulse_3	Automatic update	PLC_1 [CPU 1212C DC/DC/Rly]	-	2 Bytes	-	0	1 34
O	1006	1007	Pulse_4	Automatic update	PLC_1 [CPU 1212C DC/DC/Rly]	-	2 Bytes	-	0	1 35
O	1	1	DQ 8xRelay_1	Automatic update	PLC_1 [CPU 1212C DC/DC/Rly]	-	1 Bytes	-	0	2
I	68	75	AI 4xRTD_1	Automatic update	PLC_1 [CPU 1212C DC/DC/Rly]	-	8 Bytes	-	0	3

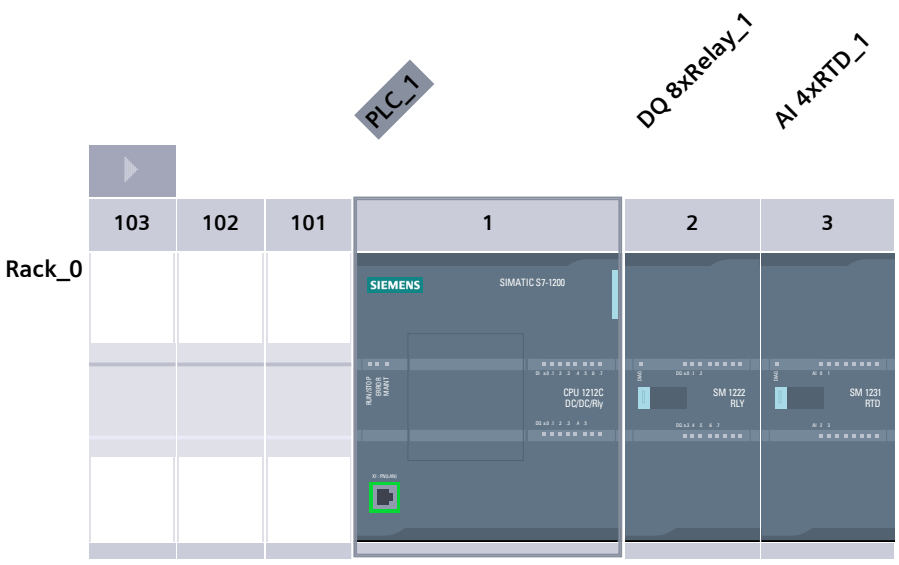
DQ 8xRelay_1					
General\Project information					
Name	DQ 8xRelay_1	**Author**	Amin Hashemi	**Comment**	
Slot	2				
General\Catalog information					
Short designation	SM 1222 DQ8 x relay	**Description**	Digital output module DQ8 x relay; plug-in terminal blocks	**Article number**	6ES7 222-1HF32-0XB0
Firmware version	V2.0		False		
DQ 8\Project information					
Name	DQ 8xRelay_1	**Comment**			
DQ 8\Digital outputs					
Reaction to CPU STOP	Use substitute value				
DQ 8\Digital outputs\Channel0					
Channel address	Q1.0	**Substitute a value of 1 on a change from RUN to STOP.**	0		
DQ 8\Digital outputs\Channel1					
Channel address	Q1.1	**Substitute a value of 1 on a change from RUN to STOP.**	0		
DQ 8\Digital outputs\Channel2					
Channel address	Q1.2	**Substitute a value of 1 on a change from RUN to STOP.**	0		

DQ 8\Digital outputs\Channel3					
Channel address	Q1.3	**Substitute a value of 1 on a change from RUN to STOP.**	0		
DQ 8\Digital outputs\Channel4					
Channel address	Q1.4	**Substitute a value of 1 on a change from RUN to STOP.**	0		
DQ 8\Digital outputs\Channel5					
Channel address	Q1.5	**Substitute a value of 1 on a change from RUN to STOP.**	0		
DQ 8\Digital outputs\Channel6					
Channel address	Q1.6	**Substitute a value of 1 on a change from RUN to STOP.**	0		
DQ 8\Digital outputs\Channel7					
Channel address	Q1.7	**Substitute a value of 1 on a change from RUN to STOP.**	0		
DQ 8\I/O addresses\Output addresses					
Start address	1.0	**End address**	1.7	**Organization block**	0
Process image	0				

AI 4xRTD_1					
General\Project information					
Name	AI 4xRTD_1	**Author**	Amin Hashemi	**Comment**	
Slot	3				
General\Catalog information					
Short designation	SM 1231 AI4 x RTD	**Description**	Analog input module AI4 x RTD	**Article number**	6ES7 231-5PD30-0XB0
Firmware version	V1.0		False		
AI 4xRTD\Project information					
Name	AI 4xRTD_1	**Comment**			
AI 4xRTD\Module diagnostics					
Enable power supply diagnostics	1	**Additional diagnostics may be selected for each input/output.**			
AI 4xRTD\Analog inputs\Noise reduction					
Integration time	50 Hz (20 ms)				
AI 4xRTD\Analog inputs\Channel0					
Channel address	IW68	**Measurement type**	Thermal resistor (4-wire)	**Thermal resistor**	Pt 100 standard range
Temperature coefficient	Pt 0.00385055 ohms/ohms/°C (DIN EN 60751)	**Temperature scale**	Celsius	**Smoothing**	Weak (4 cycles)
		Enable broken wire diagnostics	0	**Enable overflow diagnostics**	1
Enable underflow diagnostics	1				
AI 4xRTD\Analog inputs\Channel1					
Channel address	IW70	**Measurement type**	Thermal resistor (4-wire)	**Thermal resistor**	Pt 100 standard range
Temperature coefficient	Pt 0.00385055 ohms/ohms/°C (DIN EN 60751)	**Temperature scale**	Celsius	**Smoothing**	Weak (4 cycles)
		Enable broken wire diagnostics	0	**Enable overflow diagnostics**	1
Enable underflow diagnostics	1				
AI 4xRTD\Analog inputs\Channel2					
Channel address	IW72	**Measurement type**	Thermal resistor (4-wire)	**Thermal resistor**	Pt 100 standard range
Temperature coefficient	Pt 0.00385055 ohms/ohms/°C (DIN EN 60751)	**Temperature scale**	Celsius	**Smoothing**	Weak (4 cycles)
		Enable broken wire diagnostics	0	**Enable overflow diagnostics**	1
Enable underflow diagnostics	1				
AI 4xRTD\Analog inputs\Channel3					
Channel address	IW74	**Measurement type**	Thermal resistor (4-wire)	**Thermal resistor**	Pt 100 standard range
Temperature coefficient	Pt 0.00385055 ohms/ohms/°C (DIN EN 60751)	**Temperature scale**	Celsius	**Smoothing**	Weak (4 cycles)
		Enable broken wire diagnostics	0	**Enable overflow diagnostics**	1
Enable underflow diagnostics	1				
AI 4xRTD\I/O addresses\Input addresses					
Start address	68	**End address**	75	**Organization block**	0
Process image	0				

Compressor / PLC_1 [CPU 1212C DC/DC/Rly]

Device view


PLC_1
DQ 8xRelay_1
AI 4xRTD_1
103
102
101
1
2
3
Rack_0
SIEMENS
SIMATIC S7-1200
CPU 1212C
DC/DC/Rly
SM 1222
RLY
SM 1231
RTD