



# **Digital Logic**

## **Pocket Data Book**

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*Digital Logic*  
*Pocket Data Book*



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## Little Logic

Series	Supply Voltage Vcc (V)	Operating Free-air Temperature Ta (°C)
SN74AUP1G	0.8~3.6	-40~85
SN74AUC1G/2G/3G	0.8~2.7	-40~85
SN74LVC1G/2G/3G	1.65~5.5	-40~85
SN74AHC1G	2.0~5.5	-40~85
SN74AHCT1G	4.5~5.5	-40~85

## GATE/OCTAL/Widebus™/Widebus+

Series	Supply Voltage Vcc (V)	Operating Free-air Temperature Ta (°C)
SN74ABT	4.5~5.5	-40~85
SN64BCT	4.5~5.5	-40~85
SN74BCT SN74F SN74ALS SN74AS	4.5~5.5	0~70
SN74LS SN74S SN74xx(TTL)	4.75~5.25	0~70
SN74AC SN74AC11xxx SN74AHC	2.0~5.5	-40~85
SN74HC	2.0~6.0	-40~85
SN74LV	2.0~5.5	-40~85
SN74LVC	2.0~3.6	-40~85
SN74LVT	2.7~3.6	-40~85
SN74ALVC	1.65~3.6	-40~85
SN74ALVT	2.3~3.6	-40~85
SN74AVC	1.4~3.6	-40~85
SN74AUC	0.8~2.7	-40~85

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16823	18-BIT EDGE-TRIGGERED D-TYPE FLIP-FLOPS WITH DUAL OUTPUTS	684
16825	18-BIT BUS BUFFERS/DRIVERS WITH 3-STATE OUTPUTS	685
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16835	3.3-V ABT 18-BIT UNIVERSAL BUS DRIVER WITH 3-STATE OUTPUTS	693
16841	20-BIT BUS INTERFACE D-TYPE LATCHES WITH 3-STATE OUTPUTS	694
16843	18-BIT BUS INTERFACE D-TYPE LATCHES WITH 3-STATE OUTPUTS	695
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16861	20-BIT BUS TRANSCIVERS WITH 3-STATE OUTPUTS	698
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29825	8-BIT BUS-INTERFACE FLIP-FLOPS WITH 3-STATE OUTPUTS	712
29827	10-BIT BUFFERS/DRIVERS WITH 3-STATE OUTPUTS	713
29828	10-BIT BUFFERS/DRIVERS WITH 3-STATE OUTPUTS	714
29841	10-BIT BUS INTERFACE D-TYPE LATCHES WITH 3-STATE OUTPUTS	715
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162241	3.3-V ABT 16-BIT BUFFERS/DRIVERS WITH 3-STATE OUTPUTS	745
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162245	16-BIT TRANSCIVER WITH 3-STATE OUTPUTS	747
162260	12-BIT TO 24-BIT MULTIPLEXED D-TYPE LATCH WITH 3-STATE OUTPUTS	748
162268	12-BIT TO 24-BIT REGISTERED BUS EXCHANGER WITH 3-STATE OUTPUTS	750
162280	16-BIT TO 32-BIT REGISTERED BUS EXCHANGER WITH BYTE MASKS AND 3-STATE OUTPUTS	752
162282	18-BIT TO 36-BIT REGISTERED BUS EXCHANGER WITH 3-STATE OUTPUTS	754
162334	16-BIT UNIVERSAL BUS DRIVER WITH 3-STATE OUTPUTS	756
162344	1-BIT TO 4-BIT ADDRESS DRIVER WITH 3-STATE OUTPUTS	758
162373	3.3-V ABT 16-BIT TRANSPARENT D-TYPE LATCHES WITH 3-STATE OUTPUTS	760
162374	3.3-V ABT 16-BIT EDGE-TRIGGERED D-TYPE FLIP-FLOPS WITH 3-STATE OUTPUTS	761
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162501	18-BIT UNIVERSAL BUS TRANSCIVER WITH 3-STATE OUTPUTS	766
162525	18-BIT UNIVERSAL BUS TRANSCIVER WITH 3-STATE OUTPUTS	768
162541	3.3-V ABT 16-BIT BUFFERS/DRIVERS WITH 3-STATE OUTPUTS	770
162601	18-BIT UNIVERSAL BUS TRANSCIVER WITH 3-STATE OUTPUTS	772
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162820	3.3-V 10-BIT FLIP-FLOP WITH DUAL OUTPUTS AND 3-STATE OUTPUTS	775
162823	18-BIT BUS-INTERFACE FLIP-FLOPS WITH 3-STATE OUTPUTS	776
162825	18-BIT BUFFERS/DRIVERS WITH 3-STATE OUTPUTS	777
162827	20-BIT BUS BUFFERS/DRIVERS WITH 3-STATE OUTPUTS	778
162830	1-BIT TO 2-BIT ADDRESS DRIVER WITH 3-STATE OUTPUTS	779
162831	1-BIT TO 4-BIT ADDRESS REGISTER/DRIVER WITH 3-STATE OUTPUTS	780
162832	1-BIT TO 4-BIT ADDRESS REGISTER/DRIVER WITH 3-STATE OUTPUTS	781
162834	18-BIT UNIVERSAL BUS DRIVER WITH 3-STATE OUTPUTS	782
162835	18-BIT UNIVERSAL BUS DRIVER WITH 3-STATE OUTPUTS	783
162836	20-BIT UNIVERSAL BUS DRIVER WITH 3-STATE OUTPUTS	784
162841	20-BIT BUS-INTERFACE D-TYPE LATCH WITH 3-STATE OUTPUTS	785
32244	32-BIT BUFFER/DRIVER WITH 3-STATE OUTPUTS	786
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# **FUNCTION**

**Translation**



### Single-Supply Voltage-Translator

Description	Function	Device	CMOS Technology				
			LV	LVC	ALVC	AVC	AUP
Configurable Gate	2-Input AND gate	1G57					●
	2-Input AND gate with both inputs inverted						
	2-Input NOR gate						
	2-Input NOR gate with both inputs inverted						
	2-Input NAND gate with inverted input						
	2-Input OR gate with inverted input						
	2-Input XNOR						
	Inverter						
	Noninverted buffer						
	2-Input NAND gate						
Configurable Gate	2-Input NAND gate with both inputs inverted						
	2-Input OR gate						
	2-Input OR gate with both inputs inverted						
	2-Input AND gate with inverted input						
	2-Input NOR gate with inverted input						
	2-Input XNOR						
	Inverter						
	Noninverted buffer						
	2-to-1 data selector						
	2-Input AND gate						
Configurable Gate	2-Input AND gate with one inverted input						
	2-Input OR gate						
	2-Input OR gate with one inverted input						
	2-Input NAND gate with one inverted input						
	2-Input NOR gate with one inverted input						
	Inverter						
	Noninverted buffer						
	2-to-1 data selector						
	2-Input AND gate						
	2-Input AND gate with one inverted input						
Configurable Gate	2-Input OR gate						
	2-Input OR gate with one inverted input						
	2-Input NAND gate with one inverted input						
	2-Input NOR gate with one inverted input						
	Inverter						
	Noninverted buffer						
	2-to-1 data selector						
	2-Input AND gate						
	2-Input AND gate with one inverted input						
	2-Input OR gate						
Configurable Gate	2-Input OR gate with one inverted input						
	2-Input NAND gate with one inverted input						
	2-Input NOR gate with one inverted input						
	Inverter						
	Noninverted buffer						
	2-to-1 data selector						
	2-Input AND gate						
	2-Input AND gate with one inverted input						
	2-Input OR gate						
	2-Input OR gate with one inverted input						
Configurable Gate	2-Input NAND gate with one inverted input						
	2-Input NOR gate with one inverted input						
	Inverter						
	Noninverted buffer						
	2-to-1 data selector						
	2-Input AND gate						
	2-Input AND gate with one inverted input						
	2-Input OR gate						
	2-Input OR gate with one inverted input						
	2-Input NAND gate with one inverted input						
Configurable Gate	2-Input NOR gate with one inverted input						
	Inverter						
	Noninverted buffer						
	2-to-1 data selector						
	2-Input AND gate						
	2-Input AND gate with one inverted input						
	2-Input OR gate						
	2-Input OR gate with one inverted input						
	2-Input NAND gate with one inverted input						
	2-Input NOR gate with one inverted input						
Configurable Gate	Inverter						
	Noninverted buffer						
	2-to-1 data selector						
	2-Input AND gate						
	2-Input AND gate with one inverted input						
	2-Input OR gate						
	2-Input OR gate with one inverted input						
	2-Input NAND gate with one inverted input						
	2-Input NOR gate with one inverted input						
	Inverter						
Configurable Gate	Noninverted buffer						
	2-to-1 data selector						
	2-Input AND gate						
	2-Input AND gate with one inverted input						
	2-Input OR gate						
	2-Input OR gate with one inverted input						
	2-Input NAND gate with one inverted input						
	2-Input NOR gate with one inverted input						
	Inverter						
	Noninverted buffer						

### Dual-Supply Bus Transceiver

Description	Device	Technology				
		Low-Voltage CMOS				Low-Power CMOS
LV	LVC	ALVC	AVC	AUP		
Single BusTransceiver	1T45	●				●/H●
Dual BusTransceivers	2T45	●				●/H●
4-Bit BusTransceivers	4T245					●/H●
Voltage-Translation	8T245	●				●/H●
Octal BusTransceivers	3245	C●				
4245	●/C●					
16T245	●/H●				●/H●	
16-Bit BusTransceivers	16A245			●		A●/AH● B●/BH●
20-Bit BusTransceivers	20T245					●/H●
24-Bit BusTransceivers	24T245					●/H●
32T245					●/H●	
324245					B●	

Status ● : Product available in technology indicated \* : New product planned in technology indicated

### APPLICATION SPECIFIC (CompactFlash™, SD CARD, MultiMediaCards, I²C)

Description	Device	Technology				
		Low-Voltage CMOS				Low-Power CMOS
LV	LVC	ALVC	AVC	AUP		
MMC, SD CARD, Memory Stick, SmartMedia, AND xD-Picture Card ±15-kV ESD VOLTAGE TRANSLATION TRANSCEIVER	406				A●	
MMC, SD CARD, Memory Stick™ VOLTAGE TRANSLATION TRANSCEIVER	405L				A●	
LOW-POWER, DUAL-SUPPLY, LEVEL-TRANSLATING CompactFlash™ INTERFACE WITH DATA, 11-BIT ADDRESS, AND 13BIT CONTROL LINES	4320	●A				

Status ● : Product available in technology indicated \* : New product planned in technology indicated



# **PIN ASSIGNMENTS**

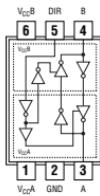
**Translation**



# Pin Assignments

## 1T45

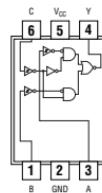
SINGLE-BIT DUAL-SUPPLY BUS TRANSCIEVER WITH CONFIGURABLE VOLTAGE TRANSLATION AND 3-STATE OUTPUTS



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## 1T98

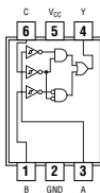
SINGLE-SUPPLY VOLTAGE-LEVEL TRANSLATOR WITH NINE CONFIGURABLE GATE LOGIC FUNCTIONS



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## 1T57

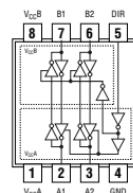
SINGLE-SUPPLY VOLTAGE-LEVEL TRANSLATOR WITH NINE CONFIGURABLE GATE LOGIC FUNCTIONS



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## 2T45

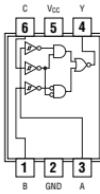
DUAL-BIT DUAL-SUPPLY BUS TRANSCIEVER WITH CONFIGURABLE VOLTAGE TRANSLATION AND 3-STATE OUTPUTS



See page 31

## 1T58

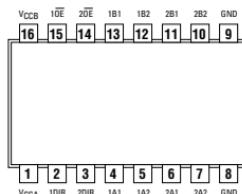
SINGLE-SUPPLY VOLTAGE-LEVEL TRANSLATOR WITH NINE CONFIGURABLE GATE LOGIC FUNCTIONS



See page 28

## 4T245

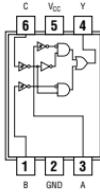
4-BIT DUAL-SUPPLY BUS TRANSCIEVER WITH CONFIGURABLE VOLTAGE TRANSLATION AND 3-STATE OUTPUTS



See page 35

## 1T97

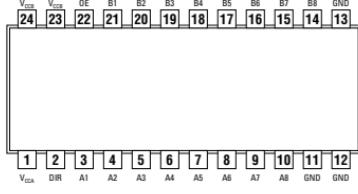
SINGLE-SUPPLY VOLTAGE-LEVEL TRANSLATOR WITH NINE CONFIGURABLE GATE LOGIC FUNCTION



See page 29

## 8T245

8-BIT DUAL-SUPPLY BUS TRANSCIEVER WITH CONFIGURABLE VOLTAGE TRANSLATION AND 3-STATE OUTPUTS



See page 37

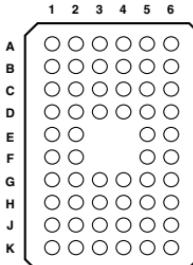
# Pin Assignments

## 16T245

16-BIT DUAL-SUPPLY BUS TRANSCEIVER WITH CONFIGURABLE VOLTAGE TRANSLATION AND 3-STATE OUTPUTS



GQL OR ZQL PACKAGE  
(TOP VIEW)



### terminal assignments

	1	2	3	4	5	6
A	1DIR	NC	NC	NC	NC	$\overline{1OE}$
B	1B2	1B1	GND	GND	1A1	1A2
C	1B4	1B3	VCCB	VCCA	1A3	1A4
D	1B6	1B5	GND	GND	1A5	1A6
E	1B8	1B7			1A7	1A8
F	2B1	2B2			2A2	2A1
G	2B3	2B4	GND	GND	2A4	2A3
H	2B5	2B6	VCCB	VCCA	2A6	2A5
J	2B7	2B8	GND	GND	2A8	2A7
K	2DIR	NC	NC	NC	NC	$\overline{2OE}$

(1) NC - No internal connection

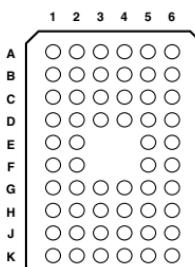
See page 41

## 20T245

20-BIT DUAL-SUPPLY BUS TRANSCEIVER WITH CONFIGURABLE VOLTAGE TRANSLATION AND 3-STATE OUTPUTS



GQL OR ZQL PACKAGE  
(TOP VIEW)



### terminal assignments

	1	2	3	4	5	6
A	1B1	1B2	1DIR	$\overline{1OE}$	1A2	1A1
B	1B3	1B4	GND	GND	1A4	1A3
C	1B5	1B6	VCCB	VCCA	1A6	1A5
D	1B7	1B8	GND	GND	1A8	1A7
E	1B9	1B10			1A10	1A9
F	2B1	2B2			2A2	2A1
G	2B3	2B4	GND	GND	2A4	2A3
H	2B5	2B6	VCCB	VCCA	2A6	2A5
J	2B7	2B8	GND	GND	2A8	2A7
K	2B9	2B10	2DIR	$\overline{2OE}$	2A10	2A9

See page 45

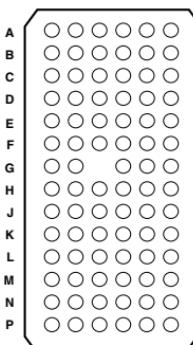
# Pin Assignments

## 24T245

24-BIT DUAL-SUPPLY BUS TRANSCEIVER WITH CONFIGURABLE VOLTAGE TRANSLATION AND 3-STATE OUTPUTS

GRG OR ZRG PACKAGE  
(TOP VIEW)

1 2 3 4 5 6



### terminal assignments

	1	2	3	4	5	6
A	6OE	5OE	4OE	3OE	2OE	1OE
B	1B1	1B2	VCCB	VCCA	1A2	1A1
C	1B3	1B4	GND	GND	1A4	1A3
D	2B1	2B2	VCCB	VCCA	2A2	2A1
E	2B3	2B4	GND	GND	2A4	2A3
F	3B1	3B2	GND	GND	3A2	3A1
G	3B3	3B4		GND	3A4	3A3
H	4B1	4B2	VCCB	VCCA	4A2	4A1
J	4B3	4B4	GND	GND	4A4	4A3
K	5B1	5B2	GND	GND	5A2	5A1
L	5B3	5B4	VCCB	VCCA	5A4	5A3
M	6B1	6B2	GND	GND	6A2	6A1
N	6B3	6B4	VCCB	VCCA	6A4	6A3
P	6DIR	5DIR	4DIR	3DIR	2DIR	1DIR

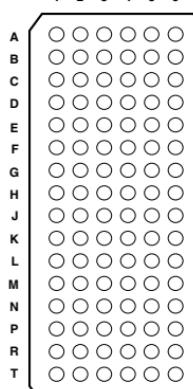
See page 47

## 32T245

32-BIT DUAL-SUPPLY BUS TRANSCEIVER WITH CONFIGURABLE VOLTAGE TRANSLATION AND 3-STATE OUTPUTS WITH 3-STATE DESELECTED OUTPUT

GRG OR ZRG PACKAGE  
(TOP VIEW)

1 2 3 4 5 6



### terminal assignments

	1	2	3	4	5	6
A	1B2	1B1	1DIR	1OE	1A1	1A2
B	1B4	1B3	GND	GND	1A3	1A4
C	1B6	1B5	VCCB	VCCA	1A5	1A6
D	1B8	1B7	GND	GND	1A7	1A8
E	2B2	2B1	GND	GND	2A1	2A2
F	2B4	2B3	VCCB	VCCA	2A3	2A4
G	2B6	2B5	GND	GND	2A5	2A6
H	2B7	2B8	2DIR	2OE	2A8	2A7
J	3B2	3B1	3DIR	3OE	3A1	3A2
K	3B4	3B3	GND	GND	3A3	3A4
L	3B6	3B5	VCCB	VCCA	3A5	3A6
M	3B8	3B7	GND	GND	3A7	3A8
N	4B2	4B1	GND	GND	4A1	4A2
P	4B4	4B3	VCCB	VCCA	4A3	4A4
R	4B6	4B5	GND	GND	4A5	4A6
T	4B7	4B8	4DIR	4OE	4A8	4A7

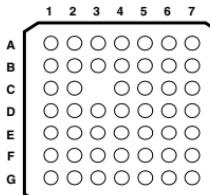
See page 50

# Pin Assignments

**406**

MMC, SD CARD, Memory Stick, SmartMedia, AND xD-Picture Card  
 ±15-kV ESD-PROTECTED VOLTAGE-TRANSLATION TRANCEIVER

**GQC/ZQC PACKAGE  
 (TOP VIEW)**



**TERMINAL ASSIGNMENTS<sup>(1)</sup>**

	1	2	3	4	5	6	7
<b>A</b>	$V_{CCA}$	2A	4DIR	2DIR	MODE1	10B1	$V_{CCB0}$
<b>B</b>	10A1	3A	1A	1DIR	MODE0	9B1	1B
<b>C</b>	9A	10A2		3DIR	GND	2B	3B
<b>D</b>	9DIR	4A	56DIR	GND	4B	11B	12B
<b>E</b>	78DIR	6A	GND	CS0	GND	10B2	9B2
<b>F</b>	7A	8A	12A	13A	7B	5B	14B
<b>G</b>	$V_{CCA}$	5A	11A	CS1	8B	6B	$V_{CCB1}$

(1)  $V_{CCA}$  powers all A-port I/Os and control inputs.

$V_{CCB0}$  powers 1B, 2B, 3B, 4B, 9B1, and 10B1.

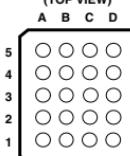
$V_{CCB1}$  powers 5B, 6B, 7B, 8B, 9B2, 10B2, 11B, 12B, and 14B.

See page 53

**406L**

MMC, SD CARD, Memory Stick, SmartMedia, AND xD-Picture Card ±15-kV ESD-PROTECTED VOLTAGE-TRANSLATION TRANCEIVER

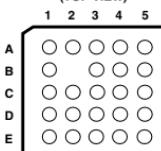
**GXY OR ZXY PACKAGE  
 (TOP VIEW)**



**TERMINAL ASSIGNMENTS  
 (20-Ball GXY/ZXY Package)**

	A	B	C	D
<b>5</b>	$V_{CCA}$	CMD-dir	DAT0-dir	$V_{CCB}$
<b>4</b>	DAT3A	DAT2A	DAT2B	DAT3B
<b>3</b>	CLKA	GND	GND	CLKB
<b>2</b>	DAT1A	DAT0A	CMDB	DAT0B
<b>1</b>	CLK-f	CMDA	DAT123-dir	DAT1B

**GQS OR ZQS PACKAGE  
 (TOP VIEW)**



**TERMINAL ASSIGNMENTS  
 (24-Ball GQS/ZQS Package)**

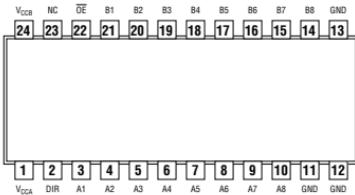
	1	2	3	4	5
<b>A</b>	DAT2A	CMD-dir	DAT0-dir	RSV	DAT2B
<b>B</b>	DAT3A		$V_{CCA}$	$V_{CCB}$	DAT3B
<b>C</b>	CLKA	RSV	GND	GND	CLKB
<b>D</b>	DAT0A	CMDA	RSV	CMDB	DAT0B
<b>E</b>	DAT1A	CLK-f	DAT123-dir	RSV	DAT1B

See page 58

## Pin Assignments

3245

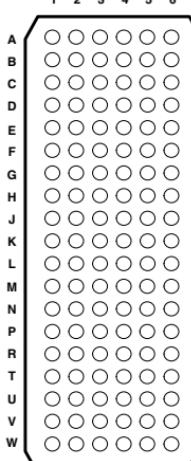
## OCTAL BUS TRANSCEIVER WITH ADJUSTABLE OUTPUT VOLTAGE AND 3-STATE OUTPUTS



See page 61

4320

## **LOW-POWER, DUAL-SUPPLY, LEVEL-TRANSLATING CompactFlash™ INTERFACE WITH 16-BIT DATA, 11-BIT ADDRESS, AND 13-BIT CONTROL LINES**



### terminal assignments

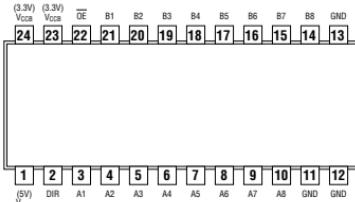
	1	2	3	4	5	6
A	D12	D04	D03	SD14	SD12	SD11
B	D13	D05	D11	SD13	SD10	SD09
C	D14	D06	SD15	SINPACK	SD08	SD07
D	D15	D07	VCC_CF	VCC_S	SD06	SD05
E	CE2	CE1	GND	GND	SD04	SD03
F	OE	A10	VCC_CF	VCC_S	SD02	SD01
G	A09	IORD	GND	GND	SD00	SC1E
H	A08	IOWR	VCC_CF	VCC_S	EN_L	EN_H
J	A07	WE	GND	GND	MASTER_EN	BUF_EN
K	A06	READY	A05	SCE2	SOE	SIORD
L	A04	RESET	GND	GND	SWE	SIOWR
M	A03	WAIT	VCC_CF	VCC_S	SREADY	SRESET
N	A02	INPACK	GND	GND	SWAIT	SREG
P	A01	REG	VCC_CF	GND	SBVD2	SBVD1
R	A00	BVD2	VCC_CF	VCC_S	SA10	SWP
T	D00	BVD1	VCC_SD	DIR ( $\bar{S}/CF$ )	SA08	SA09
U	D01	D08	CD1	DIR_OUT	SA06	SA07
V	D02	D09	CD2	SA00	SA04	SA05
W	WP	D10	SCD	SA01	SA02	SA03

See page 63

4245

## OCTAL BUS TRANSCEIVER AND 3.3-V TO 5-V SHIFTER WITH 3-STATE OUTPUTS (SN74LVC4245A)

**OCTAL DUAL-SUPPLY BUS TRANSCEIVER WITH CONFIGURABLE  
OUTPUT VOLTAGE AND  
3-STATE OUTPUTS (SN74LVCC4245A)**



See page 62

# Pin Assignments

## 164245

### 16-BIT TRANSCEIVER AND 3.3-V TO 5-V SHIFTER WITH 3-STATE OUTPUTS

- SN74ALVC164245:

A port has  $V_{CCA}$ , which is set to operate at 2.5 V and 3.3 V  
B port has  $V_{CCB}$ , which is set to operate at 3.3 V and 5 V

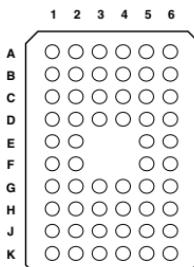
- SN74AVCB164245, SN74AVCBH164245:

The A-port is designed to track  $V_{CCA}$ ,  
 $V_{CCA}$  accepts any supply voltage  
from 1.4 V to 3.6 V

The B-port is designed to track  $V_{CCB}$ ,  
 $V_{CCB}$  accepts any supply voltage  
from 1.4 V to 3.6 V



GQL OR ZQL PACKAGE  
(TOP VIEW)



TERMINAL ASSIGNMENTS <sup>(1)</sup>

	1	2	3	4	5	6
<b>A</b>	1DIR	NC	NC	NC	NC	1OE
<b>B</b>	1B2	1B1	GND	GND	1A1	1A2
<b>C</b>	1B4	1B3	$V_{CCB}$	$V_{CCA}$	1A3	1A4
<b>D</b>	1B6	1B5	GND	GND	1A5	1A6
<b>E</b>	1B8	1B7			1A7	1A8
<b>F</b>	2B1	2B2			2A2	2A1
<b>G</b>	2B3	2B4	GND	GND	2A4	2A3
<b>H</b>	2B5	2B6	$V_{CCB}$	$V_{CCA}$	2A6	2A5
<b>J</b>	2B7	2B8	GND	GND	2A8	2A7
<b>K</b>	2D1R	NC	NC	NC	NC	2OE

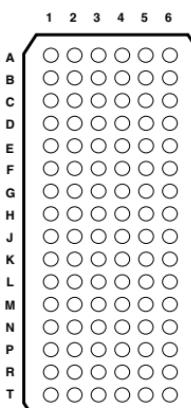
(1) NC - No internal connection

See page 67

## 324245

### 32-BIT DUAL-SUPPLY BUS TRANSCEIVER WITH CONFIGURABLE VOLTAGE TRANSLATION AND 3-STATE OUTPUTS

GKE PACKAGE  
(TOP VIEW)



terminal assignments

	1	2	3	4	5	6
<b>A</b>	1B2	1B1	1DIR	1OE	1A1	1A2
<b>B</b>	1B4	1B3	GND	GND	1A3	1A4
<b>C</b>	1B6	1B5	$V_{CCB}$	$V_{CCA}$	1A5	1A6
<b>D</b>	1B8	1B7	GND	GND	1A7	1A8
<b>E</b>	2B2	2B1	GND	GND	2A1	2A2
<b>F</b>	2B4	2B3	$V_{CCB}$	$V_{CCA}$	2A3	2A4
<b>G</b>	2B6	2B5	GND	GND	2A5	2A6
<b>H</b>	2B7	2B8	2DIR	2OE	2A8	2A7
<b>J</b>	3B2	3B1	3DIR	3OE	3A1	3A2
<b>K</b>	3B4	3B3	GND	GND	3A3	3A4
<b>L</b>	3B6	3B5	$V_{CCB}$	$V_{CCA}$	3A5	3A6
<b>M</b>	3B8	3B7	GND	GND	3A7	3A8
<b>N</b>	4B2	4B1	GND	GND	4A1	4A2
<b>P</b>	4B4	4B3	$V_{CCB}$	$V_{CCA}$	4A3	4A4
<b>R</b>	4B6	4B5	GND	GND	4A5	4A6
<b>T</b>	4B7	4B8	4DIR	4OE	4A8	4A7

See page 69

# **FUNCTION AND ELECTRICAL CHARACTERISTICS**

**Translation**

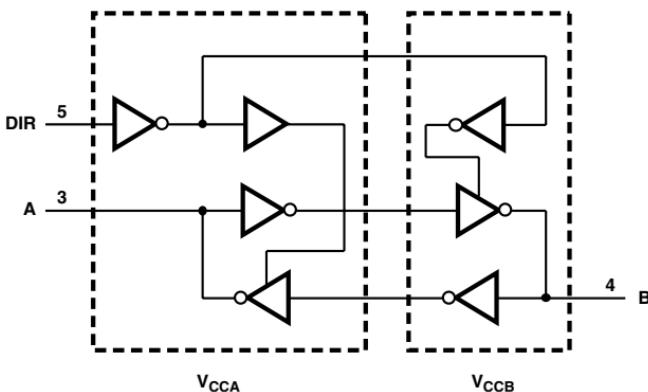


## 1T45

### SINGLE-BIT DUAL-SUPPLY BUS TRANSCEIVER WITH CONFIGURABLE VOLTAGE TRANSLATION AND 3-STATE OUTPUTS

- V<sub>CC</sub> Isolation Feature - If Either V<sub>CC</sub> Input Is at GND, Both Ports Are in the High-Impedance State
- DIR Input Circuit Referenced to V<sub>CCA</sub>
- This Single-Bit Noninverting Bus Transceiver Uses Two Separate Configurable Power-Supply Rails
- Designed for asynchronous Communication Between Two Data Buses

Logic Diagram



FUNCTION TABLE<sup>(1)</sup>

INPUT DIR	OPERATION
L	B data to A bus
H	A data to B bus

(1) Input circuits of the data I/Os always are active.

## RECOMMENDED OPERATING CONDITIONS AND ELECTRICAL CHARACTERISTICS

PARAMETER	MAX or MIN	LVC 5V	LVC 3.3V	LVC 2.5V	LVC 1.8V	AVC 3.3V	AVC 2.5V	AVC 1.8V	AVC 1.5V	AVCH 3.3V	AVCH 2.5V	AVCH 1.8V	AVCH 1.5V	UNIT
I <sub>CC</sub> *	MAX	0.004	0.004	0.004	0.004	0.02	0.02	0.02	0.02	0.02	0.02	0.02	0.02	mA
I <sub>QH</sub>	MAX	-32	-24	-8	-4	-12	-9	-8	-6	-12	-9	-8	-6	mA
I <sub>QL</sub>	MAX	32	24	8	4	12	9	8	6	12	9	8	6	mA

\*I<sub>CCA</sub> + I<sub>CCB</sub>

## SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	V <sub>CCA</sub> = 1.5V							
				AVC 3.3V	AVC 2.5V	AVC 1.8V	AVC 1.5V	AVCH 3.3V	AVCH 2.5V	AVCH 1.8V	AVCH 1.5V
t <sub>PLH</sub>	A	B	MAX	3.3	4.2	5.2	5.6	3.3	4.2	5.2	5.6
t <sub>PHL</sub>				3.8	4.2	5.2	5.6	3.8	4.2	5.2	5.6
t <sub>PUL</sub>	B	A	MAX	4.8	4.9	5.3	5.5	4.8	4.9	5.3	5.5
t <sub>FHL</sub>				4.8	4.9	5.3	5.5	4.8	4.9	5.3	5.5
t <sub>FHZ</sub>	DIR	A	MAX	6.9	6.9	6.8	6.7	6.9	6.9	6.8	6.7
t <sub>FZL</sub>				6.9	6.9	6.8	6.7	6.9	6.9	6.8	6.7
t <sub>FHZ</sub>	DIR	B	MAX	4.5	4.7	7.1	8.1	4.5	4.7	7.1	8.1
t <sub>FZL</sub>				4.5	4.7	7.1	8.1	4.5	4.7	7.1	8.1
t <sub>FZH</sub> *	DIR	A	MAX	9.3	9.6	12.4	13.6	9.3	9.6	12.4	13.6
t <sub>FZL*</sub> *				9.3	9.6	12.4	13.6	9.3	9.6	12.4	13.6
t <sub>FZH*</sub> *	DIR	B	MAX	10.7	11.1	12	12.3	10.7	11.1	12	12.3
t <sub>FZL*</sub> *				10.7	11.1	12	12.3	10.7	11.1	12	12.3

UNIT : ns

\*The enable time is a calculated value, derived using the formula shown in the enable times section.

PARAMETER	INPUT	OUTPUT	MAX or MIN	V <sub>CCA</sub> = 1.8V							
				LVC 5V	LVC 3.3V	LVC 2.5V	LVC 1.8V	AVC 3.3V	AVC 2.5V	AVC 1.8V	AVC 1.5V
t <sub>PLH</sub>	A	B	MAX	7.2	8.3	10.3	17.7	3.4	3.9	5	5.3
t <sub>PHL</sub>				7	7.1	8.5	14.3	3.4	3.9	5	5.3
t <sub>PUL</sub>	B	A	MAX	15.1	15.5	16	17.7	4.4	4.6	5	5.2
t <sub>FHL</sub>				12.2	12.6	12.9	14.3	4.4	4.6	5	5.2
t <sub>FHZ</sub>	DIR	A	MAX	17.1	18.4	18.5	19.4	6	5.9	5.9	5.9
t <sub>FZL</sub>				10.9	10.7	10.5	10.5	6	5.9	5.9	5.9
t <sub>FHZ</sub>	DIR	B	MAX	8.2	10.3	11.5	21.9	5.3	4.4	6.8	7.7
t <sub>FZL</sub>				6.4	8.4	9.2	16	5.3	4.4	6.8	7.7
t <sub>FZH</sub> *	DIR	A	MAX	12.8	23.9	25.2	33.7	8.7	9	11.8	12.9
t <sub>FZL*</sub> *				13.3	22.9	24.4	36.2	8.7	9	11.8	12.9
t <sub>FZH*</sub> *	DIR	B	MAX	10.9	19	20.8	28.2	9.4	9.8	10.9	11.2
t <sub>FZL*</sub> *				12.7	25.5	27	33.7	9.4	9.8	10.9	11.2

PARAMETER	INPUT	OUTPUT	MAX or MIN	V <sub>CCA</sub> = 1.8V			
				AVCH 3.3V	AVCH 2.5V	AVCH 1.8V	AVCH 1.5V
t <sub>FHL</sub>	A	B	MAX	3.4	3.9	5	5.3
t <sub>FHL</sub>				3.4	3.9	5	5.3
t <sub>FZH</sub>	B	A	MAX	4.4	4.6	5	5.2
t <sub>FHL</sub>				4.4	4.6	5	5.2
t <sub>FHZ</sub>	DIR	A	MAX	6	5.9	5.9	5.9
t <sub>FZL</sub>				6	5.9	5.9	5.9
t <sub>FHZ</sub>	DIR	B	MAX	5.3	4.4	6.8	7.7
t <sub>FZL</sub>				5.3	4.4	6.8	7.7
t <sub>FZH</sub> *	DIR	A	MAX	8.7	9	11.8	12.9
t <sub>FZL*</sub> *				8.7	9	11.8	12.9
t <sub>FZH*</sub> *	DIR	B	MAX	9.4	9.8	10.9	11.2
t <sub>FZL*</sub> *				9.4	9.8	10.9	11.2

UNIT : ns

\*The enable time is a calculated value, derived using the formula shown in the enable times section.

V <sub>CCA</sub> =2.5V											
PARAMETER	INPUT	OUTPUT	MAX or MIN	LVC 5V	LVC 3.3V	LVC 2.5V	LVC 1.8V	AVC 3.3V	AVC 2.5V	AVC 1.8V	AVC 1.5V
t <sub>PLH</sub>	A	B	MAX	5.1	6.4	8.5	16	3	3.4	4.6	4.9
t <sub>PLH</sub>				4.6	5.4	7.5	12.9	3	3.4	4.6	4.9
t <sub>PLH</sub>	B	A	MAX	7.5	8	8.5	10.3	3.3	3.4	3.8	4.2
t <sub>PLH</sub>				6.2	7	7.5	8.5	3.3	3.4	3.8	4.2
t <sub>PZH</sub>	DIR	A	MAX	8.1	8.1	8.1	8.1	3.8	3.8	3.8	3.8
t <sub>PZH</sub>				5.8	5.9	5.9	5.9	3.8	3.8	3.8	3.8
t <sub>PLZ</sub>	DIR	B	MAX	7.1	10.2	11.4	23.7	4	4.1	6.5	7.6
t <sub>PLZ</sub>				5.3	8.4	9.6	18.9	4	4.1	6.5	7.6
t <sub>PZH</sub> *	DIR	A	MAX	12.8	16.4	18.1	29.2	7.3	7.5	10.3	11.8
t <sub>PZH</sub> *				13.3	17.2	18.9	32.2	7.3	7.5	10.3	11.8
t <sub>PLZ</sub> *	DIR	B	MAX	10.9	12.3	14.4	21.9	6.6	7	8.1	8.6
t <sub>PLZ</sub> *				12.7	13.5	15.6	21	6.6	7	8.1	8.6

V <sub>CCA</sub> =2.5V											
PARAMETER	INPUT	OUTPUT	MAX or MIN	AVCH 3.3V	AVCH 2.5V	AVCH 1.8V	AVCH 1.5V				
t <sub>PLH</sub>	A	B	MAX	3	3.4	4.6	4.9				
t <sub>PLH</sub>				3	3.4	4.6	4.9				
t <sub>PLH</sub>	B	A	MAX	3.3	3.4	3.8	4.2				
t <sub>PLH</sub>				3.3	3.4	3.8	4.2				
t <sub>PZH</sub>	DIR	A	MAX	3.8	3.8	3.8	3.8				
t <sub>PZH</sub>				3.8	3.8	3.8	3.8				
t <sub>PLZ</sub>	DIR	B	MAX	4	4.1	6.5	7.6				
t <sub>PLZ</sub>				4	4.1	6.5	7.6				
t <sub>PZH</sub> *	DIR	A	MAX	7.3	7.5	10.3	11.8				
t <sub>PZH</sub> *				7.3	7.5	10.3	11.8				
t <sub>PLZ</sub> *	DIR	B	MAX	6.6	7	8.1	8.6				
t <sub>PLZ</sub> *				6.6	7	8.1	8.6				

UNIT : ns

\*The enable time is a calculated value, derived using the formula shown in the enable times section.

V <sub>CCA</sub> =3.3V											
PARAMETER	INPUT	OUTPUT	MAX or MIN	LVC 5V	LVC 3.3V	LVC 2.5V	LVC 1.8V	AVC 3.3V	AVC 2.5V	AVC 1.8V	AVC 1.5V
t <sub>PLH</sub>	A	B	MAX	4.4	5.8	8	15.5	2.8	3.3	4.4	4.7
t <sub>PLH</sub>				4	5	7	12.6	2.8	3.3	4.4	4.7
t <sub>PLH</sub>	B	A	MAX	5.4	5.8	6.4	8.3	2.8	3	3.4	3.8
t <sub>PLH</sub>				4.5	5	5.4	7.1	2.8	3	3.4	3.8
t <sub>PZH</sub>	DIR	A	MAX	7.3	7.3	7.3	7.3	4.3	4.3	4.3	4.3
t <sub>PZH</sub>				5.7	5.7	5.6	5.6	4.3	4.3	4.3	4.3
t <sub>PLZ</sub>	DIR	B	MAX	6.8	8.8	10.1	20.5	4.9	4	6.5	7.4
t <sub>PLZ</sub>				4.9	7.1	7.8	14.5	4.9	4	6.5	7.4
t <sub>PZH</sub> *	DIR	A	MAX	10.3	12.9	14.2	22.8	6.7	7	9.9	11.2
t <sub>PZH</sub> *				11.3	13.8	15.5	27.6	6.7	7	9.9	11.2
t <sub>PLZ</sub> *	DIR	B	MAX	10.1	11.5	13.6	21.1	6.8	7.2	8.5	8.9
t <sub>PLZ</sub> *				11.3	12.3	14.3	19.9	6.8	7.2	8.5	8.9

V <sub>CCA</sub> =3.3V											
PARAMETER	INPUT	OUTPUT	MAX or MIN	AVCH 3.3V	AVCH 2.5V	AVCH 1.8V	AVCH 1.5V				
t <sub>PLH</sub>	A	B	MAX	2.8	3.3	4.4	4.7				
t <sub>PLH</sub>				2.8	3.3	4.4	4.7				
t <sub>PLH</sub>	B	A	MAX	2.8	3	3.4	3.8				
t <sub>PLH</sub>				2.8	3	3.4	3.8				
t <sub>PZH</sub>	DIR	A	MAX	4.3	4.3	4.3	4.3				
t <sub>PZH</sub>				4.3	4.3	4.3	4.3				
t <sub>PLZ</sub>	DIR	B	MAX	4.9	4	6.5	7.4				
t <sub>PLZ</sub>				4.9	4	6.5	7.4				
t <sub>PZH</sub> *	DIR	A	MAX	6.7	7	9.9	11.2				
t <sub>PZH</sub> *				6.7	7	9.9	11.2				
t <sub>PLZ</sub> *	DIR	B	MAX	6.8	7.2	8.5	8.9				
t <sub>PLZ</sub> *				6.8	7.2	8.5	8.9				

UNIT : ns

\*The enable time is a calculated value, derived using the formula shown in the enable times section.

$V_{CCA} = 5.0V$							
PARAMETER	INPUT	OUTPUT	MAX or MIN	LVC 5V	LVC 3.3V	LVC 2.5V	LVC 1.8V
$t_{PLH}$	A	B	MAX	3.9	5.4	7.5	15.1
				3.5	4.5	6.2	12.2
$t_{PHL}$	B	A	MAX	3.9	4.4	5.1	7.2
				3.5	4	4.6	7
$t_{PHZ}$	DIR	A	MAX	5.4	5.5	5.4	5.4
				3.7	3.7	3.8	3.8
$t_{PLZ}$	DIR	B	MAX	6.5	8.5	9.8	20.2
				4.5	7	7.4	14.8
$t_{PZH}^*$	DIR	A	MAX	8.4	11.4	12.5	22
				10	12.5	14.4	27.2
$t_{PLH}^*$	DIR	B	MAX	7.6	9.1	11.3	18.9
				8.6	10	11.6	17.6

UNIT : ns

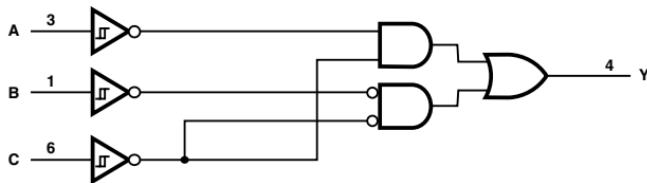
\*The enable time is a calculated value, derived using the formula shown in the enable times section.

# 1T57

## SINGLE-SUPPLY VOLTAGE-LEVEL TRANSLATOR WITH NINE CONFIGURABLE GATE LOGIC FUNCTIONS

- Single-Supply Voltage Translator
- Nine Configurable Gate Logic Functions
- Schmitt-Trigger Inputs Reject Input Noise and Provide Better Output Signal Integrity

**Logic Diagram**



**FUNCTION TABLE**

INPUTS			OUTPUT Y
C	B	A	
L	L	L	H
L	L	H	L
L	H	L	H
L	H	H	L
H	L	L	L
H	L	H	L
H	H	L	H
H	H	H	H

**FUNCTION SELECTION TABLE**

LOGIC FUNCTION
2-input AND gate
2-input NOR gate with both inputs inverted
2-input NAND gate with inverted input
2-input OR gate with inverted input
2-input AND gate with both inputs inverted
2-input NOR gate
2-input XNOR gate
Inverter
Noninverted buffer

### RECOMMENDED OPERATING CONDITIONS AND ELECTRICAL CHARACTERISTICS

PARAMETER	MAX or MIN	AUP 3.3V	AUP 2.5V	UNIT
$I_{CC}$	MAX	0.0009	0.0009	mA
$I_{BH}$	MAX	-4	-3.1	mA
$I_{BL}$	MAX	4	3.1	mA

### SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	AUP 3.3V	AUP 2.5V
$t_{PLH}$	$V_i = 1.8V$	A, B, or C	Y	MAX	8.5 8.5
$t_{PHL}$					7.9 7.9
$t_{PLH}$	$V_i = 2.5V$	A, B, or C	Y	MAX	6.1 6.1
$t_{PHL}$					7.1 7.1

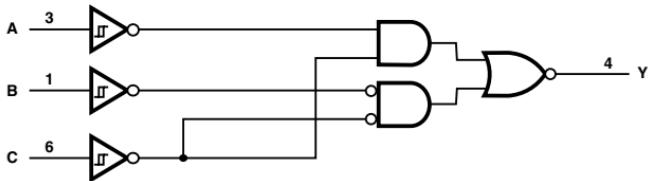
UNIT : ns

# 1T58

## SINGLE-SUPPLY VOLTAGE-LEVEL TRANSLATOR WITH NINE CONFIGURABLE GATE LOGIC FUNCTIONS

- Single-Supply Voltage Translator
- Nine Configurable Gate Logic Functions
- Schmitt-Trigger Inputs Reject Input Noise and Provide Better Output Signal Integrity

Logic Diagram



FUNCTION TABLE

C	B	A	Y
L	L	L	L
L	L	H	H
L	H	L	L
L	H	H	H
H	L	L	H
H	L	H	H
H	H	L	L
H	H	H	L

FUNCTION SELECTION TABLE

LOGIC FUNCTION
2-input NAND gate
2-input OR gate with both inputs inverted
2-input AND gate with inverted input
2-input NOR gate with inverted input
2-input NAND gate with both inputs inverted
2-input OR gate
2-input XOR gate
Inverter
Noninverted buffer

RECOMMENDED OPERATING CONDITIONS AND ELECTRICAL CHARACTERISTICS

PARAMETER	MAX or MIN	AUP 3.3V	AUP 2.5V	UNIT
$I_{CC}$	MAX	0.0009	0.0009	mA
$I_{OH}$	MAX	-4	-3.1	mA
$I_{OL}$	MAX	4	3.1	mA

SWITCHING CHARACTERISTICS

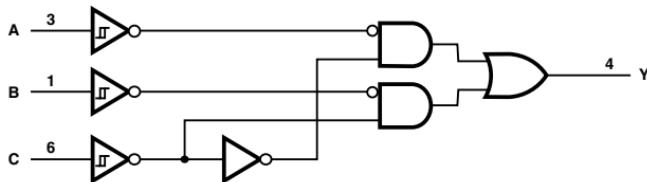
PARAMETER	INPUT	OUTPUT	MAX or MIN	AUP 3.3V	AUP 2.5V
$t_{PLH}$	$V_i = 1.8V$	A, B, or C	Y	MAX	8.5
$t_{PHL}$					7.9
$t_{PLH}$	$V_i = 2.5V$	A, B, or C	Y	MAX	8.5
$t_{PHL}$					7.9
$t_{PLH}$	$V_i = 2.5V$	A, B, or C	Y	MAX	6.1
$t_{PHL}$					7.1

UNIT : ns

## SINGLE-SUPPLY VOLTAGE-LEVEL TRANSLATOR WITH NINE CONFIGURABLE GATE LOGIC FUNCTION

- Single-Supply Voltage Translator
- Nine Configurable Gate Logic Functions
- Schmitt-Trigger Inputs Reject Input Noise and Provide Better Output Signal Integrity

**Logic Diagram**



**FUNCTION TABLE**

INPUTS			OUTPUT Y
C	B	A	
L	L	L	L
L	L	H	L
L	H	L	H
L	H	H	H
H	L	L	L
H	L	H	H
H	H	L	L
H	H	H	H

**FUNCTION SELECTION TABLE**

LOGIC FUNCTION
2-to-1 data selector
2-input AND gate
2-input OR gate with one inverted input
2-input NAND gate with one inverted input
2-input AND gate with one inverted input
2-input NOR gate with one inverted input
2-input OR gate
Inverter
Noninverted buffer

**RECOMMENDED OPERATING CONDITIONS AND ELECTRICAL CHARACTERISTICS**

PARAMETER	MAX or MIN	AUP 3.3V	AUP 2.5V	UNIT
$I_{CC}$	MAX	0.0009	0.0009	mA
$I_{GH}$	MAX	-4	-3.1	mA
$I_{GL}$	MAX	4	3.1	mA

**SWITCHING CHARACTERISTICS**

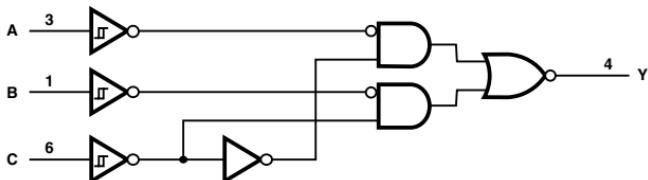
PARAMETER	INPUT	OUTPUT	MAX or MIN	AUP 3.3V	AUP 2.5V
$t_{PLH}$	$V_i = 1.8V$ A, B, or C	Y	MAX	8.5	7.9
$t_{PHL}$				8.5	7.9
$t_{PLH}$	$V_i = 2.5V$ A, B, or C	Y	MAX	6.1	7.1
$t_{PHL}$				6.1	7.1
$t_{PLH}$	$V_i = 3.3V$ A, B, or C	Y	MAX	5.7	6.5
$t_{PHL}$				5.7	6.5

UNIT : ns

## SINGLE-SUPPLY VOLTAGE-LEVEL TRANSLATOR WITH NINE CONFIGURABLE GATE LOGIC FUNCTIONS

- Single-Supply Voltage Translator
- Nine Configurable Gate Logic Functions
- Schmitt-Trigger Inputs Reject Input Noise and Provide Better Output Signal Integrity

**Logic Diagram**



**FUNCTION TABLE**

INPUTS			OUTPUT Y
C	B	A	
L	L	L	H
L	L	H	H
L	H	L	L
L	H	H	L
H	L	L	H
H	L	H	L
H	H	L	H
H	H	H	L

**FUNCTION SELECTION TABLE**

LOGIC FUNCTION
2-to-1 data selector
2-input AND gate
2-input OR gate with one inverted input
2-input NAND gate with one inverted input
2-input AND gate with one inverted input
2-input NOR gate with one inverted input
2-input OR gate
Inverter
Noninverted buffer

### RECOMMENDED OPERATING CONDITIONS AND ELECTRICAL CHARACTERISTICS

PARAMETER	MAX or MIN	AUP 3.3V	AUP 2.5V	UNIT
$I_{CE}$	MAX	0.0009	0.0009	mA
$I_{DS}$	MAX	-4	-3.1	mA
$I_{OL}$	MAX	4	3.1	mA

### SWITCHING CHARACTERISTICS

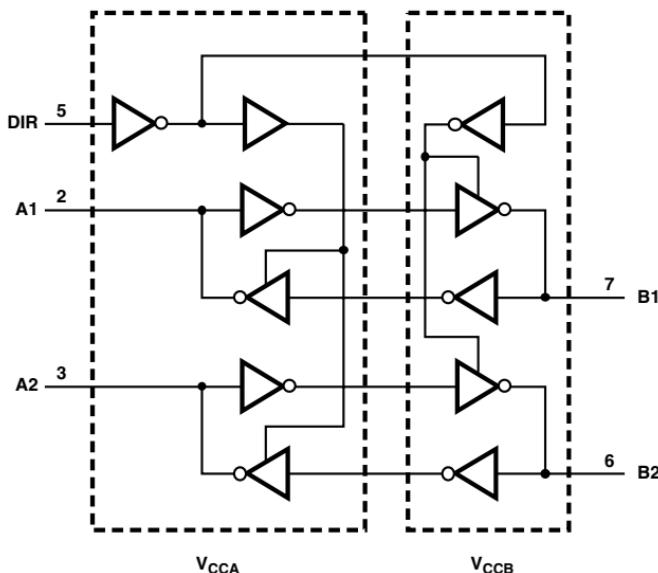
PARAMETER	INPUT	OUTPUT	MAX or MIN	AUP 3.3V	AUP 2.5V
$t_{PLH}$	$V_i = 1.8V$	A, B, or C	Y	MAX	8.5 8.5 6.1 6.1 5.7
$t_{PHL}$					7.9 7.9 7.1 7.1 6.5
$t_{PLH}$	$V_i = 2.5V$	A, B, or C	Y	MAX	6.1 6.1 5.7
$t_{PHL}$					7.1 7.1 6.5
$t_{PLH}$	$V_i = 3.3V$	A, B, or C	Y	MAX	5.7 5.7
$t_{PHL}$					6.5

UNIT : ns

## DUAL-BIT DUAL-SUPPLY BUS TRANSCEIVER WITH CONFIGURABLE VOLTAGE TRANSLATION AND 3-STATE OUTPUTS

- Control Inputs  $V_{IH}/V_{IL}$  Levels Are Referenced to  $V_{CCA}$  Voltage
- This Dual-Bit Noninverting Bus Transceiver Uses Two Separate Configurable Power-Supply Rails
- Designed for asynchronous Communication Between Two Data Buses

**Logic Diagram**



**FUNCTION TABLE<sup>(1)</sup>**  
(each transceiver)

INPUT DIR	OPERATION
L	B data to A bus
H	A data to B bus

(1) Input circuits of the data I/Os always are active.

## RECOMMENDED OPERATING CONDITIONS AND ELECTRICAL CHARACTERISTICS

PARAMETER	MAX or MIN	LVC 5V	LVC 3.3V	LVC 2.5V	LVC 1.8V	AVC 3.3V	AVC 2.5V	AVC 1.8V	AVC 1.5V	AVCH 3.3V	AVCH 2.5V	AVCH 1.8V	AVCH 1.5V	UNIT
I <sub>CC</sub> *	MAX	0.004	0.004	0.004	0.004	0.02	0.02	0.02	0.02	0.02	0.02	0.02	0.02	mA
I <sub>DH</sub>	MAX	-32	-24	-8	-4	-12	-9	-8	-6	-12	-9	-8	-6	mA
I <sub>OL</sub>	MAX	32	24	8	4	12	9	8	6	12	9	8	6	mA

\*I<sub>CCA</sub> + I<sub>CCB</sub>

## SWITCHING CHARACTERISTICS

V <sub>CCA</sub> = 1.5V													
PARAMETER	INPUT	OUTPUT	MAX or MIN	AVC 3.3V	AVC 2.5V	AVC 1.8V	AVC 1.5V	AVCH 3.3V	AVCH 2.5V	AVCH 1.8V	AVCH 1.5V		
t <sub>PLH</sub>	A	B	MAX	3.5	3.7	4.6	5.4	3.5	3.7	4.6	5.4		
t <sub>PHL</sub>				3.5	3.7	4.6	5.4	3.5	3.7	4.6	5.4		
t <sub>PZH</sub>	B	A	MAX	4.7	4.9	5.2	5.4	4.7	4.9	5.2	5.4		
t <sub>PLZ</sub>				4.7	4.9	5.2	5.4	4.7	4.9	5.2	5.4		
t <sub>PHZ</sub>	DIR	A	MAX	7.6	7.7	7.8	8.5	4.6	5.5	7.1	8.5		
t <sub>PLZ</sub>				7.6	7.7	7.8	8.5	4.6	5.5	7.1	8.5		
t <sub>PZH</sub>	DIR	B	MAX	7.1	6.9	6.9	7	7.1	6.9	6.9	7		
t <sub>PLZ</sub>				7.1	6.9	6.9	7	7.1	6.9	6.9	7		
t <sub>PZH</sub> *	DIR	A	MAX	11.8	11.8	12.1	12.4	11.8	11.8	12.1	12.4		
t <sub>PLZ</sub> *				11.8	11.8	12.1	12.4	11.8	11.8	12.1	12.4		
t <sub>PZH</sub> *	DIR	B	MAX	7.8	9.1	11.6	13.9	7.8	9.1	11.6	13.9		
t <sub>PLZ</sub> *				7.8	9.1	11.6	13.9	7.8	9.1	11.6	13.9		

UNIT : ns

\*The enable time is a calculated value, derived using the formula shown in the enable times section.

V <sub>CCA</sub> = 1.8V													
PARAMETER	INPUT	OUTPUT	MAX or MIN	LVC 5V	LVC 3.3V	LVC 2.5V	LVC 1.8V	AVC 3.3V	AVC 2.5V	AVC 1.8V	AVC 1.5V		
t <sub>PLH</sub>	A	B	MAX	7.2	8.3	10.3	17.7	3.1	3.4	4.3	5.2		
t <sub>PHL</sub>				7	7.1	8.5	14.3	3.1	3.4	4.3	5.2		
t <sub>PZH</sub>	B	A	MAX	15.1	15.5	16	17.7	3.8	4	4.4	4.7		
t <sub>PLZ</sub>				12.2	12.6	12.9	14.3	3.8	4	4.4	4.7		
t <sub>PHZ</sub>	DIR	A	MAX	29.3	30.5	30.5	30.9	5.2	5.3	6.9	8.1		
t <sub>PLZ</sub>				19.4	19.5	19.6	19.7	5.2	5.3	6.9	8.1		
t <sub>PHZ</sub>	DIR	B	MAX	8.6	11.3	14.9	27.9	5.9	5.7	5.9	5.8		
t <sub>PLZ</sub>				7.1	9.7	12.6	19.5	5.9	5.7	5.9	5.8		
t <sub>PZH</sub> *	DIR	A	MAX	22.2	25.2	28.6	37.2	9.7	9.7	10.3	10.4		
t <sub>PLZ</sub> *				20.8	23.9	27.8	42.2	9.7	9.7	10.3	10.4		
t <sub>PZH</sub> *	DIR	B	MAX	26.6	27.8	29.9	37.4	8.3	8.6	11.2	13.3		
t <sub>PLZ</sub> *				36.3	37.6	39	45.2	8.3	8.6	11.2	13.3		

V <sub>CCA</sub> = 1.8V													
PARAMETER	INPUT	OUTPUT	MAX or MIN	AVCH 3.3V	AVCH 2.5V	AVCH 1.8V	AVCH 1.5V						
t <sub>PLH</sub>	A	B	MAX	3.1	3.4	4.3	5.2						
t <sub>PHL</sub>				3.1	3.4	4.3	5.2						
t <sub>PZH</sub>	B	A	MAX	3.8	4	4.4	4.7						
t <sub>PLZ</sub>				3.8	4	4.4	4.7						
t <sub>PHZ</sub>	DIR	A	MAX	4.5	5.3	6.9	8.1						
t <sub>PLZ</sub>				4.5	5.3	6.9	8.1						
t <sub>PHZ</sub>	DIR	B	MAX	5.9	5.7	5.9	5.8						
t <sub>PLZ</sub>				5.9	5.7	5.9	5.8						
t <sub>PZH</sub> *	DIR	A	MAX	9.7	9.7	10.3	10.4						
t <sub>PLZ</sub> *				9.7	9.7	10.3	10.4						
t <sub>PZH</sub> *	DIR	B	MAX	7.4	8.6	11.2	13.3						
t <sub>PLZ</sub> *				7.4	8.6	11.2	13.3						

UNIT : ns

\*The enable time is a calculated value, derived using the formula shown in the enable times section.

V <sub>CCA</sub> = 2.5V											
PARAMETER	INPUT	OUTPUT	MAX or MIN	LVC 5V	LVC 3.3V	LVC 2.5V	LVC 1.8V	AVC 3.3V	AVC 2.5V	AVC 1.8V	AVC 1.5V
t <sub>PLH</sub>	A	B	MAX	5.1	6.4	8.5	16	2.6	3	4	4.9
t <sub>PLL</sub>				4.6	5.4	7.5	12.9	2.6	3	4	4.9
t <sub>PHL</sub>	B	A	MAX	7.5	8	8.5	10.3	2.8	3	3.4	3.8
t <sub>PLL</sub>				6.2	7	7.5	8.5	2.8	3	3.4	3.8
t <sub>PZL</sub>	DIR	A	MAX	16.5	16.8	16.8	17.1	4.3	5	6.4	7.9
t <sub>PZL</sub>				12.3	12.3	12.5	12.6	4.3	5	6.4	7.9
t <sub>PZL</sub>	DIR	B	MAX	7.6	10.5	13.9	27.9	4.1	4.2	4.3	4.3
t <sub>PZL</sub>				6.2	8.9	11.2	18.9	4.1	4.2	4.3	4.3
t <sub>ZPH</sub> *	DIR	A	MAX	13.7	16.9	19.7	29.2	6.9	7.2	7.7	7.9
t <sub>ZPL</sub> *				13.8	17.5	21.4	36.4	6.9	7.2	7.7	7.9
t <sub>ZPH</sub> *	DIR	B	MAX	17.4	18.7	21	28.6	6.8	7.9	10.4	12.8
t <sub>ZPL</sub> *				21.1	22.2	24.3	30	6.8	7.9	10.4	12.8

V <sub>CCA</sub> = 2.5V							
PARAMETER	INPUT	OUTPUT	MAX or MIN	AVCH 3.3V	AVCH 2.5V	AVCH 1.8V	AVCH 1.5V
t <sub>PLH</sub>	A	B	MAX	2.6	3	4	4.9
t <sub>PLL</sub>				2.6	3	4	4.9
t <sub>PHL</sub>	B	A	MAX	2.8	3	3.4	3.8
t <sub>PLL</sub>				2.8	3	3.4	3.8
t <sub>PZL</sub>	DIR	A	MAX	4.3	5	6.4	7.9
t <sub>PZL</sub>				4.3	5	6.4	7.9
t <sub>PZL</sub>	DIR	B	MAX	4.1	4.2	4.3	4.3
t <sub>PZL</sub>				4.1	4.2	4.3	4.3
t <sub>ZPH</sub> *	DIR	A	MAX	6.9	7.2	7.7	7.9
t <sub>ZPL</sub> *				6.9	7.2	7.7	7.9
t <sub>ZPH</sub> *	DIR	B	MAX	6.8	7.9	10.4	12.8
t <sub>ZPL</sub> *				6.8	7.9	10.4	12.8

UNIT : ns

\*The enable time is a calculated value, derived using the formula shown in the enable times section.

V <sub>CCA</sub> = 3.3V							
PARAMETER	INPUT	OUTPUT	MAX or MIN	LVC 5V	LVC 3.3V	LVC 2.5V	LVC 1.8V
t <sub>PLH</sub>	A	B	MAX	4.4	5.8	8	15.5
t <sub>PLL</sub>				4	5	7	12.6
t <sub>PHL</sub>	B	A	MAX	5.4	5.8	6.4	8.3
t <sub>PLL</sub>				4.5	5	5.4	7.1
t <sub>PZL</sub>	DIR	A	MAX	10.4	10.8	10.8	10.9
t <sub>PZL</sub>				7.8	8.1	8.4	8.4
t <sub>PZL</sub>	DIR	B	MAX	7.4	10.4	13.7	27.3
t <sub>PZL</sub>				5.6	8.3	11.3	17.7
t <sub>ZPH</sub> *	DIR	A	MAX	11	14.1	17.7	26
t <sub>ZPL</sub> *				11.9	15.4	19.1	34.4
t <sub>ZPH</sub> *	DIR	B	MAX	12.2	13.9	16.4	23.9
t <sub>ZPL</sub> *				14.4	15.8	17.8	23.5

V <sub>CCA</sub> = 3.3V							
PARAMETER	INPUT	OUTPUT	MAX or MIN	AVCH 3.3V	AVCH 2.5V	AVCH 1.8V	AVCH 1.5V
t <sub>PLH</sub>	A	B	MAX	2.4	2.8	3.8	4.7
t <sub>PLL</sub>				2.4	2.8	3.8	4.7
t <sub>PHL</sub>	B	A	MAX	2.4	2.6	3.1	3.6
t <sub>PLL</sub>				2.4	2.6	3.1	3.6
t <sub>PZL</sub>	DIR	A	MAX	4	4.7	6.5	8
t <sub>PZL</sub>				4	4.7	6.5	8
t <sub>PZL</sub>	DIR	B	MAX	3.5	4.6	5.6	6.6
t <sub>PZL</sub>				3.5	4.6	5.6	6.6
t <sub>ZPH</sub> *	DIR	A	MAX	5.9	6.2	6.6	6.9
t <sub>ZPL</sub> *				5.9	6.2	6.6	6.9
t <sub>ZPH</sub> *	DIR	B	MAX	6.3	7.4	10.3	12.7
t <sub>ZPL</sub> *				6.3	7.4	10.3	12.7

UNIT : ns

\*The enable time is a calculated value, derived using the formula shown in the enable times section.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters. See [www.ti.com/sc/logic](http://www.ti.com/sc/logic) for the most current data sheets.

$V_{CCA} = 5.0V$							
PARAMETER	INPUT	OUTPUT	MAX or MIN	LVC 5V	LVC 3.3V	LVC 2.5V	LVC 1.8V
$t_{PLH}$	A	B	MAX	3.9	5.4	7.5	15.1
$t_{PHL}$				3.5	4.5	6.2	12.2
$t_{PLH}$	B	A	MAX	3.9	4.4	5.1	7.2
$t_{PHL}$				3.5	4	4.6	7
$t_{PHZ}$	DIR	A	MAX	5.4	5.5	5.4	5.4
$t_{PLZ}$				3.7	3.7	3.8	3.8
$t_{PHZ}$	DIR	B	MAX	6.5	8.5	9.8	20.2
$t_{PLZ}$				4.5	7	7.4	14.8
$t_{PZH}^*$	DIR	A	MAX	8.4	11.4	12.5	22
$t_{PLH}^*$				10	12.5	14.4	27.2
$t_{PZH}^*$	DIR	B	MAX	7.6	9.1	11.3	18.9
$t_{PLH}^*$				8.6	10	11.6	17.6

UNIT : ns

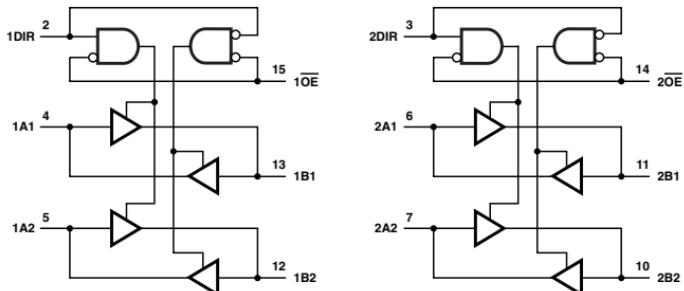
\*The enable time is a calculated value, derived using the formula shown in the enable times section.

# 4T245

## 4-BIT DUAL-SUPPLY BUS TRANSCEIVER WITH CONFIGURABLE VOLTAGE TRANSLATION AND 3-STATE OUTPUTS

- Control Inputs  $V_{IH}/V_{IL}$  Levels Are Referenced to  $V_{CCA}$  Voltage
- This 4-Bit Noninverting Bus Transceiver Uses Two Separate Configurable Power-Supply Rails
- Designed for asynchronous Communication Between Data Buses

**Logic Diagram**



**FUNCTION TABLE**  
(each 4-bit section)

INPUTS		OPERATION
OE	DIR	
L	L	B data to A bus
L	H	A data to B bus
H	X	All output Hi-Z

### RECOMMENDED OPERATING CONDITIONS AND ELECTRICAL CHARACTERISTICS

PARAMETER	MAX or MIN	AVC 3.3V	AVC 2.5V	AVC 1.8V	AVC 1.5V	AVCH 3.3V	AVCH 2.5V	AVCH 1.8V	AVCH 1.5V	UNIT
$I_{CC}^*$	MAX	0.016	0.016	0.016	0.016	0.016	0.016	0.016	0.016	mA
$I_{SH}$	MAX	-12	-9	-8	-6	-12	-9	-8	-6	mA
$I_{SL}$	MAX	12	9	8	6	12	9	8	6	mA

\* $I_{CCA} + I_{CCB}$

### SWITCHING CHARACTERISTICS

V <sub>CCA</sub> = 1.5V											
PARAMETER	INPUT	OUTPUT	MAX or MIN	AVC 3.3V	AVC 2.5V	AVC 1.8V	AVC 1.5V	AVCH 3.3V	AVCH 2.5V	AVCH 1.8V	AVCH 1.5V
$t_{PLH}$	A	B	MAX	4.2	4.2	5.2	6.3	4.2	4.2	5.2	6.3
				4.2	4.2	5.2	6.3	4.2	4.2	5.2	6.3
$t_{PHL}$	B	A	MAX	5.6	5.7	6	6.3	5.6	5.7	6	6.3
				5.6	5.7	6	6.3	5.6	5.7	6	6.3
$t_{PZH}$	$\bar{OE}$	A	MAX	9.4	9.4	9.5	9.6	9.4	9.4	9.5	9.6
				9.4	9.4	9.5	9.6	9.4	9.4	9.5	9.6
$t_{PZL}$	$\bar{OE}$	B	MAX	5.6	5.8	7.7	9.6	5.6	5.8	7.7	9.6
				5.6	5.8	7.7	9.6	5.6	5.8	7.7	9.6
$t_{PZL}$	$\bar{OE}$	A	MAX	10.2	10.2	10.2	10.2	10.2	10.2	10.2	10.2
				10.2	10.2	10.2	10.2	10.2	10.2	10.2	10.2
$t_{PZH}$	$\bar{OE}$	B	MAX	7.6	7.4	9.1	10.3	7.6	7.4	9.1	10.3
				7.6	7.4	9.1	10.3	7.6	7.4	9.1	10.3

UNIT : ns

V <sub>CCA</sub> = 1.8V											
PARAMETER	INPUT	OUTPUT	MAX or MIN	AVC 3.3V	AVC 2.5V	AVC 1.8V	AVC 1.5V	AVCH 3.3V	AVCH 2.5V	AVCH 1.8V	AVCH 1.5V
$t_{PLH}$	A	B	MAX	3.9	3.9	4.9	6	3.9	3.9	4.9	6
$t_{PHL}$				3.9	3.9	4.9	6	3.9	3.9	4.9	6
$t_{PLH}$	B	A	MAX	4.5	4.6	4.9	5.3	4.5	4.6	4.9	5.3
$t_{PHL}$				4.5	4.6	4.9	5.3	4.5	4.6	4.9	5.3
$t_{PZH}$	$\bar{OE}$	A	MAX	7.2	7.3	7.3	7.4	7.2	7.3	7.3	7.4
$t_{PZL}$				7.2	7.3	7.3	7.4	7.2	7.3	7.3	7.4
$t_{PZH}$	$\bar{OE}$	B	MAX	4.6	5.3	7.4	9.2	4.6	5.3	7.4	9.2
$t_{PZL}$				4.6	5.3	7.4	9.2	4.6	5.3	7.4	9.2
$t_{PHZ}$	$\bar{OE}$	A	MAX	8.7	8.7	8.7	8.6	8.7	8.7	8.7	8.6
$t_{PLZ}$				8.7	8.7	8.7	8.6	8.7	8.7	8.7	8.6
$t_{PHZ}$	$\bar{OE}$	B	MAX	6.9	6.9	8.7	9.9	6.9	6.9	8.7	9.9
$t_{PLZ}$				6.9	6.9	8.7	9.9	6.9	6.9	8.7	9.9

UNIT : ns

V <sub>CCA</sub> = 2.5V											
PARAMETER	INPUT	OUTPUT	MAX or MIN	AVC 3.3V	AVC 2.5V	AVC 1.8V	AVC 1.5V	AVCH 3.3V	AVCH 2.5V	AVCH 1.8V	AVCH 1.5V
$t_{PLH}$	A	B	MAX	3.6	3.5	4.6	5.7	3.6	3.5	4.6	5.7
$t_{PHL}$				3.6	3.5	4.6	5.7	3.6	3.5	4.6	5.7
$t_{PLH}$	B	A	MAX	3.3	3.4	3.9	4.2	3.3	3.4	3.9	4.2
$t_{PHL}$				3.3	3.4	3.9	4.2	3.3	3.4	3.9	4.2
$t_{PZH}$	$\bar{OE}$	A	MAX	4.8	4.8	5.2	6.5	4.8	4.8	5.2	6.5
$t_{PZL}$				4.8	4.8	5.2	6.5	4.8	4.8	5.2	6.5
$t_{PZH}$	$\bar{OE}$	B	MAX	4	4.8	7	8.8	4	4.8	7	8.8
$t_{PZL}$				4	4.8	7	8.8	4	4.8	7	8.8
$t_{PHZ}$	$\bar{OE}$	A	MAX	6.6	6.2	8.4	8.4	6.6	6.2	8.4	8.4
$t_{PLZ}$				6.6	6.2	8.4	8.4	6.6	6.2	8.4	8.4
$t_{PHZ}$	$\bar{OE}$	B	MAX	5.2	6.2	8.2	9.4	5.2	6.2	8.2	9.4
$t_{PLZ}$				5.2	6.2	8.2	9.4	5.2	6.2	8.2	9.4

UNIT : ns

V <sub>CCA</sub> = 3.3V											
PARAMETER	INPUT	OUTPUT	MAX or MIN	AVC 3.3V	AVC 2.5V	AVC 1.8V	AVC 1.5V	AVCH 3.3V	AVCH 2.5V	AVCH 1.8V	AVCH 1.5V
$t_{PLH}$	A	B	MAX	2.9	3.3	4.5	5.6	2.9	3.3	4.5	5.6
$t_{PHL}$				2.9	3.3	4.5	5.6	2.9	3.3	4.5	5.6
$t_{PLH}$	B	A	MAX	2.8	3	3.4	4.2	2.8	3	3.4	4.2
$t_{PHL}$				2.8	3	3.4	4.2	2.8	3	3.4	4.2
$t_{PZH}$	$\bar{OE}$	A	MAX	3.8	3.8	5.2	8.7	3.8	3.8	5.2	8.7
$t_{PZL}$				3.8	3.8	5.2	8.7	3.8	3.8	5.2	8.7
$t_{PZH}$	$\bar{OE}$	B	MAX	3.8	4.7	6.8	8.7	3.8	4.7	6.8	8.7
$t_{PZL}$				3.8	4.7	6.8	8.7	3.8	4.7	6.8	8.7
$t_{PHZ}$	$\bar{OE}$	A	MAX	6.6	5.6	8.3	9.3	6.6	5.6	8.3	9.3
$t_{PLZ}$				6.6	5.6	8.3	9.3	6.6	5.6	8.3	9.3
$t_{PHZ}$	$\bar{OE}$	B	MAX	6.2	6.4	8.1	9.3	6.2	6.4	8.1	9.3
$t_{PLZ}$				6.2	6.4	8.1	9.3	6.2	6.4	8.1	9.3

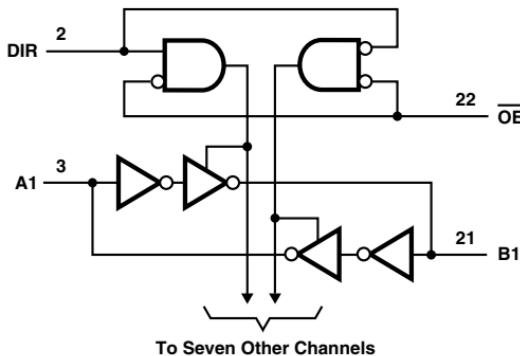
UNIT : ns

## 8T245

### 8-BIT DUAL-SUPPLY BUS TRANSCEIVER WITH CONFIGURABLE VOLTAGE TRANSLATION AND 3-STATE OUTPUTS

- Control Inputs  $V_{IH}/V_{IL}$  Levels Are Referenced to  $V_{CCA}$  Voltage
- $V_{CC}$  Isolation Feature - If Either  $V_{CC}$  Input Is at GND, All I/O Ports Are in the High-Impedance State
- This 8-Bit Noninverting Bus Transceiver Uses Two Separate Configurable Power-Supply Rails
- Designed for asynchronous Communication Between Data Buses

Logic Diagram



FUNCTION TABLE<sup>(1)</sup>  
(each 8-bit section)

CONTROL INPUTS		OUTPUTS CIRCUITS		OPERATION
$\overline{OE}$	DIR	A PORT	B PORT	
L	L	Enabled	Hi-Z	B data to A bus
L	H	Hi-Z	Enabled	A data to B bus
H	X	Hi-Z	Hi-Z	Isolation

(1) Input circuits of the data I/Os are always active.

## RECOMMENDED OPERATING CONDITIONS AND ELECTRICAL CHARACTERISTICS

PARAMETER	MAX or MIN	LVC 5V	LVC 3.3V	LVC 2.5V	LVC 1.8V	LVCH 5V	LVCH 3.3V	LVCH 2.5V	LVCH 1.8V	UNIT
$I_{CC}^*$	MAX	0.025	0.025	0.025	0.025	0.03	0.03	0.03	0.03	mA
$I_{DH}$	MAX	-32	-24	-8	-4	-32	-24	-8	-4	mA
$I_{DL}$	MAX	32	24	8	4	32	24	8	4	mA

PARAMETER	MAX or MIN	AVC 3.3V	AVC 2.5V	AVC 1.8V	AVC 1.5V	AVCH 3.3V	AVCH 2.5V	AVCH 1.8V	AVCH 1.5V	UNIT
$I_{CC}^*$	MAX	0.025	0.025	0.025	0.025	0.025	0.025	0.025	0.025	mA
$I_{DH}$	MAX	-12	-9	-8	-6	-12	-9	-8	-6	mA
$I_{DL}$	MAX	12	9	8	6	12	9	8	6	mA

$$* = I_{CCA} + I_{CCB}$$

## SWITCHING CHARACTERISTICS

$V_{CCA} = 1.5V$											
PARAMETER	INPUT	OUTPUT	MAX or MIN	AVC 3.3V	AVC 2.5V	AVC 1.8V	AVC 1.5V	AVCH 3.3V	AVCH 2.5V	AVCH 1.8V	AVCH 1.5V
$t_{PLH}$	A	B	MAX	6.8	4.9	4.6	5.4	6.8	4.9	4.6	5.4
$t_{PHL}$				6.8	4.9	4.6	5.4	6.8	4.9	4.6	5.4
$t_{PLH}$	B	A	MAX	4.5	4.7	5.1	5.4	4.5	4.7	5.1	5.4
$t_{PHL}$				4.5	4.7	5.1	5.4	4.5	4.7	5.1	5.4
$t_{PZH}$	$\overline{OE}$	A	MAX	8.7	8.7	8.7	8.7	8.7	8.7	8.7	8.7
$t_{ZPL}$				8.7	8.7	8.7	8.7	8.7	8.7	8.7	8.7
$t_{PZH}$	$\overline{OE}$	B	MAX	5.2	5.6	7.1	7.6	5.2	5.6	7.1	7.6
$t_{ZPL}$				5.2	5.6	7.1	7.6	5.2	5.6	7.1	7.6
$t_{PZH}$	$\overline{OE}$	A	MAX	8.6	8.6	8.6	8.6	8.6	8.6	8.6	8.6
$t_{ZPL}$				8.6	8.6	8.6	8.6	8.6	8.6	8.6	8.6
$t_{PZH}$	$\overline{OE}$	B	MAX	7.8	7.2	7.6	8.4	7.8	7.2	7.6	8.4
$t_{ZPL}$				7.8	7.2	7.6	8.4	7.8	7.2	7.6	8.4

UNIT : ns

$V_{CCA} = 1.8V$											
PARAMETER	INPUT	OUTPUT	MAX or MIN	LVC 5V	LVC 3.3V	LVC 2.5V	LVC 1.8V	LVCH 5V	LVCH 3.3V	LVC 2.5V	LVC 1.8V
$t_{PLH}$	A	B	MAX	7.1	7.4	9.2	21.9	7.1	7.4	9.2	21.9
$t_{PHL}$				7.1	7.4	9.2	21.9	7.1	7.4	9.2	21.9
$t_{PLH}$	B	A	MAX	23.4	23.4	23.6	23.8	23.4	23.4	23.6	23.8
$t_{PHL}$				23.4	23.4	23.6	23.8	23.4	23.4	23.6	23.8
$t_{PZH}$	$\overline{OE}$	A	MAX	23.7	23.7	23.8	24	23.7	23.7	23.8	24
$t_{ZPL}$				23.7	23.7	23.8	24	23.7	23.7	23.8	24
$t_{PZH}$	$\overline{OE}$	B	MAX	10.8	12.6	16	32	10.8	12.6	16	32
$t_{ZPL}$				10.8	12.6	16	32	10.8	12.6	16	32
$t_{PZH}$	$\overline{OE}$	A	MAX	29.2	29.3	29.4	29.6	29.2	29.3	29.4	29.6
$t_{ZPL}$				29.2	29.3	29.4	23.6	29.2	29.3	29.4	23.6
$t_{PZH}$	$\overline{OE}$	B	MAX	10.3	12	13.1	32.2	10.3	12	13.1	32.2
$t_{ZPL}$				10.3	12	13.1	32.2	10.3	12	13.1	32.2

$V_{CCA} = 1.8V$											
PARAMETER	INPUT	OUTPUT	MAX or MIN	AVC 3.3V	AVC 2.5V	AVC 1.8V	AVC 1.5V	AVCH 3.3V	AVCH 2.5V	AVCH 1.8V	AVCH 1.5V
$t_{PLH}$	A	B	MAX	3.9	4	4.4	5.1	3.9	4	4.4	5.1
$t_{PHL}$				3.9	4	4.4	5.1	3.9	4	4.4	5.1
$t_{PLH}$	B	A	MAX	3.7	3.9	4.4	4.6	3.7	3.9	4.4	4.6
$t_{PHL}$				3.7	3.9	4.4	4.6	3.7	3.9	4.4	4.6
$t_{PZH}$	$\overline{OE}$	A	MAX	6.8	6.8	6.8	6.8	6.8	6.8	6.8	6.8
$t_{ZPL}$				6.8	6.8	6.8	6.8	6.8	6.8	6.8	6.8
$t_{PZH}$	$\overline{OE}$	B	MAX	4.5	5.1	6.7	8.2	4.5	5.1	6.7	8.2
$t_{ZPL}$				4.5	5.1	6.7	8.2	4.5	5.1	6.7	8.2
$t_{PZH}$	$\overline{OE}$	A	MAX	7.1	7.1	7.1	7.1	7.1	7.1	7.1	7.1
$t_{ZPL}$				7.1	7.1	7.1	7.1	7.1	7.1	7.1	7.1
$t_{PZH}$	$\overline{OE}$	B	MAX	5.8	6	6.9	7.8	5.8	6	6.9	7.8
$t_{ZPL}$				5.8	6	6.9	7.8	5.8	6	6.9	7.8

UNIT : ns

: PREVIEW

V <sub>CCA</sub> = 2.5V											
PARAMETER	INPUT	OUTPUT	MAX or MIN	LVC 5V	LVC 3.3V	LVC 2.5V	LVC 1.8V	LVCH 5V	LVCH 3.3V	LVCH 2.5V	LVCH 1.8V
t <sub>PLH</sub>	A	B	MAX	4.8	6.2	9	21.4	4.8	6.2	9	21.4
				4.8	6.2	9	21.4	4.8	6.2	9	21.4
t <sub>PHL</sub>	B	A	MAX	8.8	8.9	9.1	9.3	8.8	8.9	9.1	9.3
				8.8	8.9	9.1	9.3	8.8	8.9	9.1	9.3
t <sub>PZH</sub>	OE	A	MAX	10.9	10.9	10.9	10.9	10.9	10.9	10.9	10.9
				10.9	10.9	10.9	10.9	10.9	10.9	10.9	10.9
t <sub>PZL</sub>	OE	B	MAX	6.9	9.4	12.9	28.2	6.9	9.4	12.9	28.2
				6.9	9.4	12.9	28.2	6.9	9.4	12.9	28.2
t <sub>PHZ</sub>	OE	A	MAX	9	9	9	9	9	9	9	9
				9	9	9	9	9	9	9	9
t <sub>PZL</sub>	OE	B	MAX	6.9	9.3	11	29.6	6.9	9.3	11	29.6
				6.9	9.3	11	29.6	6.9	9.3	11	29.6

V <sub>CCA</sub> = 2.5V											
PARAMETER	INPUT	OUTPUT	MAX or MIN	AVC 3.3V	AVC 2.5V	AVC 1.8V	AVC 1.5V	AVCH 3.3V	AVCH 2.5V	AVCH 1.8V	AVCH 1.5V
t <sub>PLH</sub>	A	B	MAX	2.8	3.1	3.9	4.7	2.8	3.1	3.9	4.7
				2.8	3.1	3.9	4.7	2.8	3.1	3.9	4.7
t <sub>PHL</sub>	B	A	MAX	2.9	3.1	4	4.9	2.9	3.1	4	4.9
				2.9	3.1	4	4.9	2.9	3.1	4	4.9
t <sub>PZH</sub>	OE	A	MAX	4.8	4.8	4.8	4.8	4.8	4.8	4.8	4.8
				4.8	4.8	4.8	4.8	4.8	4.8	4.8	4.8
t <sub>PZL</sub>	OE	B	MAX	4	4.6	6.4	7.9	4	4.6	6.4	7.9
				4	4.6	6.4	7.9	4	4.6	6.4	7.9
t <sub>PHZ</sub>	OE	A	MAX	5.1	5.1	5.1	5.1	5.1	5.1	5.1	5.1
				5.1	5.1	5.1	5.1	5.1	5.1	5.1	5.1
t <sub>PZL</sub>	OE	B	MAX	3.9	5.1	6.3	7.1	3.9	5.1	6.3	7.1
				3.9	5.1	6.3	7.1	3.9	5.1	6.3	7.1

UNIT : ns

V <sub>CCA</sub> = 3.3V											
PARAMETER	INPUT	OUTPUT	MAX or MIN	LVC 5V	LVC 3.3V	LVC 2.5V	LVC 1.8V	LVCH 5V	LVCH 3.3V	LVCH 2.5V	LVCH 1.8V
t <sub>PLH</sub>	A	B	MAX	4.4	6.3	8.8	21.2	4.4	6.2	8.8	21.2
				4.4	6.3	8.8	21.2	4.4	6.2	8.8	21.2
t <sub>PHL</sub>	B	A	MAX	6	6.1	6.2	7.2	6	6.1	6.2	7.2
				6	6.1	6.2	7.2	6	6.1	6.2	7.2
t <sub>PZH</sub>	OE	A	MAX	8.1	8.1	8.1	8.1	8.1	8.1	8.1	8.1
				8.1	8.1	8.1	8.1	8.1	8.1	8.1	8.1
t <sub>PZL</sub>	OE	B	MAX	6.4	8.5	12.4	27.7	6.4	8.5	12.4	27.7
				6.4	8.5	12.4	27.7	6.4	8.5	12.4	27.7
t <sub>PZH</sub>	OE	A	MAX	8.2	8.2	8.2	8.2	8.2	8.2	8.2	8.2
				8.2	8.2	8.2	8.2	8.2	8.2	8.2	8.2
t <sub>PZL</sub>	OE	B	MAX	6.3	8.6	10.3	29	6.3	8.6	10.3	29
				6.3	8.6	10.3	29	6.3	8.6	10.3	29

V <sub>CCA</sub> = 3.3V											
PARAMETER	INPUT	OUTPUT	MAX or MIN	AVC 3.3V	AVC 2.5V	AVC 1.8V	AVC 1.5V	AVCH 3.3V	AVCH 2.5V	AVCH 1.8V	AVCH 1.5V
t <sub>PLH</sub>	A	B	MAX	2.5	2.9	3.7	4.5	2.5	2.9	3.7	4.5
				2.5	2.9	3.7	4.5	2.5	2.9	3.7	4.5
t <sub>PHL</sub>	B	A	MAX	2.5	2.8	3.9	6.8	2.5	2.8	3.9	6.8
				2.5	2.8	3.9	6.8	2.5	2.8	3.9	6.8
t <sub>PZH</sub>	OE	A	MAX	4	4	4	4	4	4	4	4
				4	4	4	4	4	4	4	4
t <sub>PZL</sub>	OE	B	MAX	3.9	4.5	6.2	7.8	3.9	4.5	6.2	7.8
				3.9	4.5	6.2	7.8	3.9	4.5	6.2	7.8
t <sub>PHZ</sub>	OE	A	MAX	4	4	4	4	4	4	4	4
				4	4	4	4	4	4	4	4
t <sub>PZL</sub>	OE	B	MAX	4.2	4.8	6	6.9	4.2	4.8	6	6.9
				4.2	4.8	6	6.9	4.2	4.8	6	6.9

UNIT : ns

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters. See [www.ti.com/sc/logic](http://www.ti.com/sc/logic) for the most current data sheets.

V <sub>CCA</sub> = 5.0V											
PARAMETER	INPUT	OUTPUT	MAX or MIN	LVC 5V	LVC 3.3V	LVC 2.5V	LVC 1.8V	LVCH 5V	LVCH 3.3V	LVCH 2.5V	LVCH 1.8V
t <sub>PLH</sub>	A	B	MAX	4.2	6	8.8	21.4	4.2	6	8.8	21.4
t <sub>PHE</sub>				4.2	6	8.8	21.4	4.2	6	8.8	21.4
t <sub>FPLH</sub>	B	A	MAX	4.3	4.5	4.8	7	4.3	4.5	4.8	7
t <sub>FPHL</sub>				4.3	4.5	4.8	7	4.3	4.5	4.8	7
t <sub>PZH</sub>	$\overline{OE}$	A	MAX	6.4	6.4	6.4	6.4	6.4	6.4	6.4	6.4
t <sub>PZL</sub>				6.4	6.4	6.4	6.4	6.4	6.4	6.4	6.4
t <sub>ZPH</sub>	$\overline{OE}$	B	MAX	6	8.1	11.4	27.6	6	8.1	11.4	27.6
t <sub>ZPL</sub>				6	8.1	11.4	27.6	6	8.1	11.4	27.6
t <sub>FHZ</sub>	$\overline{OE}$	A	MAX	5.4	5.4	5.4	5.4	5.4	5.4	5.4	5.4
t <sub>FHL</sub>				5.4	5.4	5.4	5.4	5.4	5.4	5.4	5.4
t <sub>HZL</sub>	$\overline{OE}$	B	MAX	5.7	8	9.7	28.7	5.7	8	9.7	28.7
t <sub>HFL</sub>				5.7	8	9.7	28.7	5.7	8	9.7	28.7

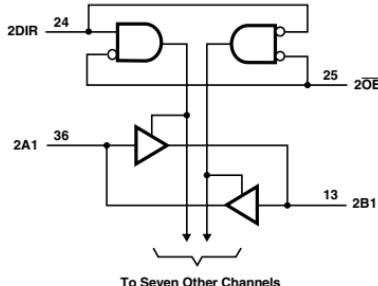
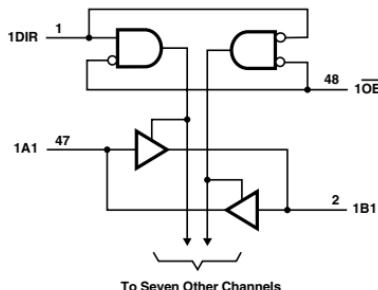
UNIT : ns

# 16T245

## 16-BIT DUAL-SUPPLY BUS TRANSCEIVER WITH CONFIGURABLE VOLTAGE TRANSLATION AND 3-STATE OUTPUTS

- Control Inputs  $V_{IH}/V_{IL}$  Levels Are Referenced to  $V_{CCA}$  Voltage
- $V_{CC}$  Isolation Feature - If Either  $V_{CC}$  Input Is at GND, Both Ports Are in the High-Impedance State
- Overvoltage-Tolerant Inputs / Outputs Allow Mixed-Voltage-Mode Data Communications
- This 16-Bit Noninverting Bus Transceiver Uses Two Separate Configurable Power-Supply Rails
- Designed for asynchronous Communication Between Data Buses

Logic Diagram



FUNCTION TABLE  
(each 8-bit section)

INPUTS		OPERATION
$\overline{OE}$	DIR	
L	L	B data to A bus
L	H	A data to B bus
H	X	Isolation

**RECOMMENDED OPERATING CONDITIONS AND ELECTRICAL CHARACTERISTICS**

PARAMETER	MAX or MIN	LVC 5V	LVC 3.3V	LVC 2.5V	LVC 1.8V	LVCH 5V	LVCH 3.3V	LVCH 2.5V	LVCH 1.8V	UNIT
$I_{CC}^*$	MAX	0.03	0.03	0.03	0.03	0.03	0.03	0.03	0.03	mA
$I_{DH}$	MAX	-32	-24	-8	-4	-32	-24	-8	-4	mA
$I_{DL}$	MAX	32	24	8	4	32	24	8	4	mA

PARAMETER	MAX or MIN	AVC 3.3V	AVC 2.5V	AVC 1.8V	AVC 1.8V	AVCH 3.3V	AVCH 2.5V	AVCH 1.8V	AVCH 1.8V	UNIT
$I_{CC}^*$	MAX	0.045	0.045	0.045	0.045	0.045	0.045	0.045	0.045	mA
$I_{DH}$	MAX	-12	-9	-8	-6	-12	-9	-8	-6	mA
$I_{DL}$	MAX	12	9	8	6	12	9	8	6	mA

 $*I_{CCA} + I_{CCB}$ 
**SWITCHING CHARACTERISTICS**

$V_{CCA} = 1.5V$											
PARAMETER	INPUT	OUTPUT	MAX or MIN	AVC 3.3V	AVC 2.5V	AVC 1.8V	AVC 1.5V	AVCH 3.3V	AVCH 2.5V	AVCH 1.8V	AVCH 1.5V
$t_{PLH}$	A	B	MAX	3.7	4.1	5.2	6.2	3.7	4.1	5.2	6.2
$t_{PHL}$				3.7	4.1	5.2	6.2	3.7	4.1	5.2	6.2
$t_{PLH}$	B	A	MAX	5.5	5.6	5.9	6.2	5.5	5.6	5.9	6.2
$t_{PHL}$				5.5	5.6	5.9	6.2	5.5	5.6	5.9	6.2
$t_{PZH}$	$\overline{OE}$	A	MAX	10.1	10.1	10.1	10.1	10.1	10.1	10.1	10.1
$t_{PZL}$				10.1	10.1	10.1	10.1	10.1	10.1	10.1	10.1
$t_{PZH}$	$\overline{OE}$	B	MAX	5.2	5.9	8.1	10.1	5.2	5.9	8.1	10.1
$t_{PZL}$				5.2	5.9	8.1	10.1	5.2	5.9	8.1	10.1
$t_{PHZ}$	$\overline{OE}$	A	MAX	9.1	9.1	9.1	9.1	9.1	9.1	9.1	9.1
$t_{PLZ}$				9.1	9.1	9.1	9.1	9.1	9.1	9.1	9.1
$t_{PHZ}$	$\overline{OE}$	B	MAX	6.3	6.5	7.5	8.7	6.3	6.5	7.5	8.7
$t_{PLZ}$				6.3	6.5	7.5	8.7	6.3	6.5	7.5	8.7

UNIT : ns

$V_{CCA} = 1.8V$											
PARAMETER	INPUT	OUTPUT	MAX or MIN	LVC 5V	LVC 3.3V	LVC 2.5V	LVC 1.8V	LVCH 5V	LVCH 3.3V	LVCH 2.5V	LVCH 1.8V
$t_{PLH}$	A	B	MAX	7.1	7.4	9.2	21.9	7.1	7.4	9.2	21.9
$t_{PHL}$				7.1	7.4	9.2	21.9	7.1	7.4	9.2	21.9
$t_{PLH}$	B	A	MAX	23.4	23.4	23.6	23.8	23.4	23.4	23.8	23.8
$t_{PHL}$				23.4	23.4	23.6	23.8	23.4	23.4	23.8	23.8
$t_{PZH}$	$\overline{OE}$	A	MAX	23.7	23.7	23.8	24	23.7	23.7	23.8	24
$t_{PZL}$				23.7	23.7	23.8	24	23.7	23.7	23.8	24
$t_{PZH}$	$\overline{OE}$	B	MAX	10.8	12.6	16	32	10.8	12.6	18	32
$t_{PZL}$				10.8	12.6	16	32	10.8	12.6	18	32
$t_{PHZ}$	$\overline{OE}$	A	MAX	29.2	29.3	29.4	29.6	29.2	29.3	29.4	29.6
$t_{PLZ}$				29.2	29.3	29.4	29.6	29.2	29.3	29.4	29.6
$t_{PHZ}$	$\overline{OE}$	B	MAX	10.3	12	13.1	32.2	10.3	12	13.1	32.2
$t_{PLZ}$				10.3	12	13.1	32.2	10.3	12	13.1	32.2

$V_{CCA} = 1.8V$											
PARAMETER	INPUT	OUTPUT	MAX or MIN	AVC 3.3V	AVC 2.5V	AVC 1.8V	AVC 1.5V	AVCH 3.3V	AVCH 2.5V	AVCH 1.8V	AVCH 1.5V
$t_{PLH}$	A	B	MAX	3.3	3.7	4.8	5.9	3.3	3.7	4.8	5.9
$t_{PHL}$				3.3	3.7	4.8	5.9	3.3	3.7	4.8	5.9
$t_{PLH}$	B	A	MAX	4.4	4.5	4.8	5.2	4.4	4.5	4.8	5.2
$t_{PHL}$				4.4	4.5	4.8	5.2	4.4	4.5	4.8	5.2
$t_{PZH}$	$\overline{OE}$	A	MAX	7.8	7.8	7.8	7.8	7.8	7.8	7.8	7.8
$t_{PZL}$				7.8	7.8	7.8	7.8	7.8	7.8	7.8	7.8
$t_{PZH}$	$\overline{OE}$	B	MAX	4.5	5.3	7.4	9.2	4.5	5.3	7.4	9.2
$t_{PZL}$				4.5	5.3	7.4	9.2	4.5	5.3	7.4	9.2
$t_{PHZ}$	$\overline{OE}$	A	MAX	7.7	7.7	7.7	7.7	7.7	7.7	7.7	7.7
$t_{PLZ}$				7.7	7.7	7.7	7.7	7.7	7.7	7.7	7.7
$t_{PHZ}$	$\overline{OE}$	B	MAX	5.7	5.9	7.1	8.4	5.7	5.9	7.1	8.4
$t_{PLZ}$				5.7	5.9	7.1	8.4	5.7	5.9	7.1	8.4

UNIT : ns

$V_{DDA} = 2.5V$											
PARAMETER	INPUT	OUTPUT	MAX or MIN	LVC 5V	LVC 3.3V	LVC 2.5V	LVC 1.8V	LVCH 5V	LVCH 3.3V	LVCH 2.5V	LVCH 1.8V
$t_{PLH}$	A	B	MAX	4.8	6.2	9	21.4	4.8	6.2	9	21.4
				4.8	6.2	9	21.4	4.8	6.2	9	21.4
$t_{PHL}$	B	A	MAX	8.8	8.9	9.1	9.3	8.8	8.9	9.1	9.3
				8.8	8.9	9.1	9.3	8.8	8.9	9.1	9.3
$t_{ZPH}$	$\overline{OE}$	A	MAX	10.9	10.9	10.9	10.9	10.9	10.9	10.9	10.9
				10.9	10.9	10.9	10.9	10.9	10.9	10.9	10.9
$t_{ZPL}$	$\overline{OE}$	B	MAX	6.9	9.4	12.9	28.2	6.9	9.4	12.9	28.2
				6.9	9.4	12.9	28.2	6.9	9.4	12.9	28.2
$t_{PHZ}$	$\overline{OE}$	A	MAX	9	9	9	9	9	9	9	9
				9	9	9	9	9	9	9	9
$t_{PLZ}$	$\overline{OE}$	B	MAX	6.9	9.3	11	29.6	6.9	9.3	11	29.6
				6.9	9.3	11	29.6	6.9	9.3	11	29.6

$V_{DDA} = 2.5V$											
PARAMETER	INPUT	OUTPUT	MAX or MIN	AVC 3.3V	AVC 2.5V	AVC 1.8V	AVC 1.5V	AVCH 3.3V	AVCH 2.5V	AVCH 1.8V	AVCH 1.5V
$t_{PLH}$	A	B	MAX	2.8	3.3	4.5	5.6	2.8	3.3	4.5	5.6
				2.8	3.3	4.5	5.6	2.8	3.3	4.5	5.6
$t_{PHL}$	B	A	MAX	3.2	3.3	3.7	4.1	3.2	3.3	3.7	4.1
				3.2	3.3	3.7	4.1	3.2	3.3	3.7	4.1
$t_{ZPH}$	$\overline{OE}$	A	MAX	5.3	5.3	5.3	5.3	5.3	5.3	5.3	5.3
				5.3	5.3	5.3	5.3	5.3	5.3	5.3	5.3
$t_{ZPL}$	$\overline{OE}$	B	MAX	4.5	5.1	7.3	9.4	4.5	5.1	7.3	9.4
				4.5	5.1	7.3	9.4	4.5	5.1	7.3	9.4
$t_{PHZ}$	$\overline{OE}$	A	MAX	6.1	6.1	6.1	6.1	6.1	6.1	6.1	6.1
				6.1	6.1	6.1	6.1	6.1	6.1	6.1	6.1
$t_{PLZ}$	$\overline{OE}$	B	MAX	5.2	6.1	6.6	7.9	5.2	6.1	6.6	7.9
				5.2	6.1	6.6	7.9	5.2	6.1	6.6	7.9

UNIT : ns

$V_{DDA} = 3.3V$											
PARAMETER	INPUT	OUTPUT	MAX or MIN	LVC 5V	LVC 3.3V	LVC 2.5V	LVC 1.8V	LVCH 5V	LVCH 3.3V	LVCH 2.5V	LVCH 1.8V
$t_{PLH}$	A	B	MAX	4.4	6.1	8.8	21.2	4.4	6.2	8.8	21.2
				4.4	6.1	8.8	21.2	4.4	6.2	8.8	21.2
$t_{PHL}$	B	A	MAX	6	6.1	6.2	7.2	6	6.1	6.2	7.2
				6	6.1	6.2	7.2	6	6.1	6.2	7.2
$t_{ZPH}$	$\overline{OE}$	A	MAX	7.8	7.8	7.8	7.8	8.1	8.1	8.1	7.8
				7.8	7.8	7.8	7.8	8.1	8.1	8.1	7.8
$t_{ZPL}$	$\overline{OE}$	B	MAX	8.4	8.5	12.4	27.7	6.4	8.5	12.4	27.7
				8.4	8.5	12.4	27.7	6.4	8.5	12.4	27.7
$t_{PHZ}$	$\overline{OE}$	A	MAX	8.2	6.2	8.2	8.2	8.2	8.2	8.2	8.2
				8.2	6.2	8.2	8.2	8.2	8.2	8.2	8.2
$t_{PLZ}$	$\overline{OE}$	B	MAX	6.3	8.6	10.3	29	6.3	8.8	10.3	29
				6.3	8.6	10.3	29	6.3	8.8	10.3	29

$V_{DDA} = 3.3V$											
PARAMETER	INPUT	OUTPUT	MAX or MIN	AVC 3.3V	AVC 2.5V	AVC 1.8V	AVC 1.5V	AVCH 3.3V	AVCH 2.5V	AVCH 1.8V	AVCH 1.5V
$t_{PLH}$	A	B	MAX	2.7	3.2	4.4	5.5	2.7	3.2	4.4	5.5
				2.7	3.2	4.4	5.5	2.7	3.2	4.4	5.5
$t_{PHL}$	B	A	MAX	2.7	2.8	3.3	3.7	2.7	2.8	3.3	3.7
				2.7	2.8	3.3	3.7	2.7	2.8	3.3	3.7
$t_{ZPH}$	$\overline{OE}$	A	MAX	4	4.1	4.2	4.3	4	4.1	4.2	4.3
				4	4.1	4.2	4.3	4	4.1	4.2	4.3
$t_{ZPL}$	$\overline{OE}$	B	MAX	4	4.9	7.2	9.3	4	4.9	7.2	9.3
				4	4.9	7.2	9.3	4	4.9	7.2	9.3
$t_{PHZ}$	$\overline{OE}$	A	MAX	5	5	5	5	5	5	5	5
				5	5	5	5	5	5	5	5
$t_{PLZ}$	$\overline{OE}$	B	MAX	5	5.2	6.5	7.7	5	5.2	6.5	7.7
				5	5.2	6.5	7.7	5	5.2	6.5	7.7

UNIT : ns

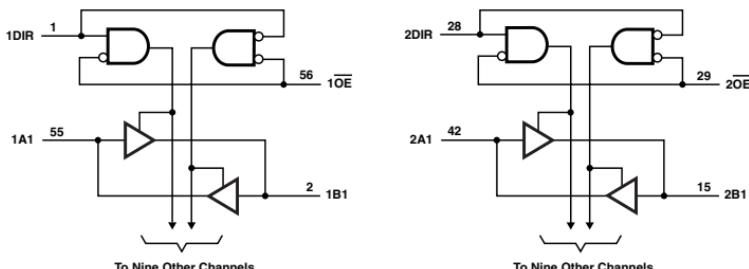
V <sub>CCA</sub> = 5.0V											
PARAMETER	INPUT	OUTPUT	MAX or MIN	LVC 5V	LVC 3.3V	LVC 2.5V	LVC 1.8V	LVCH 5V	LVCH 3.3V	LVCH 2.5V	LVCH 1.8V
$t_{PLH}$	A	B	MAX	4.2	6	8.8	21.4	4.2	6	8.8	21.4
				4.2	6	8.8	21.4	4.2	6	8.8	21.4
$t_{PHL}$	B	A	MAX	4.3	4.5	4.8	6.8	4.3	4.5	4.8	7
				4.3	4.5	4.8	6.8	4.3	4.5	4.8	7
$t_{PZH}$	$\overline{OE}$	A	MAX	5.5	5.5	5.5	5.5	5.4	5.4	5.4	5.4
				5.5	5.5	5.5	5.5	5.4	5.4	5.4	5.4
$t_{PZL}$	$\overline{OE}$	B	MAX	6	8.1	11.4	27.6	6	8.1	11.4	27.6
				6	8.1	11.4	27.6	6	8.1	11.4	27.6
$t_{PHZ}$	$\overline{OE}$	A	MAX	6.4	5.4	5.4	5.4	5.4	5.4	5.4	5.4
				6.4	5.4	5.4	5.4	5.4	5.4	5.4	5.4
$t_{PLZ}$	$\overline{OE}$	B	MAX	5.7	8	9.7	28.7	5.7	8	9.7	28.7
				5.7	8	9.7	28.7	5.7	8	9.7	28.7

UNIT : ns

## 20-BIT DUAL-SUPPLY BUS TRANSCEIVER WITH CONFIGURABLE VOLTAGE TRANSLATION AND 3-STATE OUTPUTS

- Control Inputs  $V_{IH}/V_{IL}$  Levels Are Referenced to  $V_{CCA}$  Voltage
- $V_{CC}$  Isolation Feature - If Either  $V_{CC}$  Input Is at GND, Both Ports Are in the High-Impedance State
- Overtoltage-Tolerant Inputs / Outputs Allow Mixed-Voltage-Mode Data Communications
- This 20-Bit Noninverting Bus Transceiver Uses Two Separate Configurable Power-Supply Rails
- Designed for asynchronous Communication Between Data Buses

Logic Diagram



FUNCTION TABLE  
(each 10-bit section)

INPUTS		OPERATION
$\overline{OE}$	DIR	
L	L	B data to A bus
L	H	A data to B bus
H	X	Isolation

### RECOMMENDED OPERATING CONDITIONS AND ELECTRICAL CHARACTERISTICS

PARAMETER	MAX or MIN	AVC 3.3V	AVC 2.5V	AVC 1.8V	AVC 1.8V	AVCH 3.3V	AVCH 2.5V	AVCH 1.8V	AVCH 1.8V	UNIT
$I_{O^*}$	MAX	0.065	0.065	0.065	0.065	0.065	0.065	0.065	0.065	mA
$I_{OH}$	MAX	-12	-9	-8	-6	-12	-9	-8	-6	mA
$I_{OL}$	MAX	12	9	8	6	12	9	8	6	mA

\* $I_{CCA} + I_{CCB}$

### SWITCHING CHARACTERISTICS

$V_{CCA} = 1.5V$											
PARAMETER	INPUT	OUTPUT	MAX or MIN	AVC 3.3V	AVC 2.5V	AVC 1.8V	AVC 1.5V	AVCH 3.3V	AVCH 2.5V	AVCH 1.8V	AVCH 1.5V
$t_{PLH}$	A	B	MAX	3.9	4.3	5.4	6.4	3.9	4.3	5.4	6.4
				3.9	4.3	5.4	6.4	3.9	4.3	5.4	6.4
$t_{PHL}$	B	A	MAX	5.7	5.8	6.1	6.4	5.7	5.8	6.1	6.4
				5.7	5.8	6.1	6.4	5.7	5.8	6.1	6.4
$t_{PZH}$	$\overline{OE}$	A	MAX	10.2	10.2	10.3	10.3	10.2	10.2	10.3	10.3
				10.2	10.2	10.3	10.3	10.2	10.2	10.3	10.3
$t_{PZL}$	$\overline{OE}$	B	MAX	5.3	6.1	8.4	10.3	5.3	6.1	8.4	10.3
				5.3	6.1	8.4	10.3	5.3	6.1	8.4	10.3
$t_{PZD}$	$\overline{OE}$	A	MAX	9	9	9	9	9	9	9	9
				9	9	9	9	9	9	9	9
$t_{PZU}$	$\overline{OE}$	B	MAX	5.9	6.4	7.8	9	5.9	6.4	7.8	9
				5.9	6.4	7.8	9	5.9	6.4	7.8	9

UNIT : ns

V <sub>CCA</sub> = 1.8V											
PARAMETER	INPUT	OUTPUT	MAX or MIN	AVC 3.3V	AVC 2.5V	AVC 1.8V	AVC 1.5V	AVCH 3.3V	AVCH 2.5V	AVCH 1.8V	AVCH 1.5V
$t_{PLH}$	A	B	MAX	3.5	3.9	5	6.1	3.5	3.9	5	6.1
$t_{PHL}$				3.5	3.9	5	6.1	3.5	3.9	5	6.1
$t_{PLH}$	B	A	MAX	4.6	4.7	5	5.4	4.6	4.7	5	5.4
$t_{PHL}$				4.6	4.7	5	5.4	4.6	4.7	5	5.4
$t_{PZH}$	$\overline{OE}$	A	MAX	7.9	7.9	7.9	8.1	7.9	7.9	7.9	8.1
$t_{ZPL}$				7.9	7.9	7.9	8.1	7.9	7.9	7.9	8.1
$t_{ZPH}$	$\overline{OE}$	B	MAX	4.8	5.7	7.9	10	4.8	5.7	7.9	10
$t_{PZL}$				4.8	5.7	7.9	10	4.8	5.7	7.9	10
$t_{PHZ}$	$\overline{OE}$	A	MAX	7.4	7.4	7.4	7.4	7.4	7.4	7.4	7.4
$t_{PLZ}$				7.4	7.4	7.4	7.4	7.4	7.4	7.4	7.4
$t_{PHZ}$	$\overline{OE}$	B	MAX	5.1	5.8	7.4	8.7	5.1	5.8	7.4	8.7
$t_{PLZ}$				5.1	5.8	7.4	8.7	5.1	5.8	7.4	8.7

UNIT : ns

V <sub>CCA</sub> = 2.5V											
PARAMETER	INPUT	OUTPUT	MAX or MIN	AVC 3.3V	AVC 2.5V	AVC 1.8V	AVC 1.5V	AVCH 3.3V	AVCH 2.5V	AVCH 1.8V	AVCH 1.5V
$t_{PLH}$	A	B	MAX	3	3.5	4.7	5.8	3	3.5	4.7	5.8
$t_{PHL}$				3	3.5	4.7	5.8	3	3.5	4.7	5.8
$t_{PLH}$	B	A	MAX	3.4	3.5	3.9	4.3	3.4	3.5	3.9	4.3
$t_{PHL}$				3.4	3.5	3.9	4.3	3.4	3.5	3.9	4.3
$t_{PZH}$	$\overline{OE}$	A	MAX	5.2	5.2	5.3	5.4	5.2	5.2	5.3	5.4
$t_{ZPL}$				5.2	5.2	5.3	5.4	5.2	5.2	5.3	5.4
$t_{PZH}$	$\overline{OE}$	B	MAX	4.3	5.3	7.6	9.6	4.3	5.3	7.6	9.6
$t_{ZPL}$				4.3	5.3	7.6	9.6	4.3	5.3	7.6	9.6
$t_{PHZ}$	$\overline{OE}$	A	MAX	5.2	5.2	5.2	5.2	5.2	5.2	5.2	5.2
$t_{PLZ}$				5.2	5.2	5.2	5.2	5.2	5.2	5.2	5.2
$t_{PHZ}$	$\overline{OE}$	B	MAX	5	5.3	6.9	8.2	5	5.3	6.9	8.2
$t_{PLZ}$				5	5.3	6.9	8.2	5	5.3	6.9	8.2

UNIT : ns

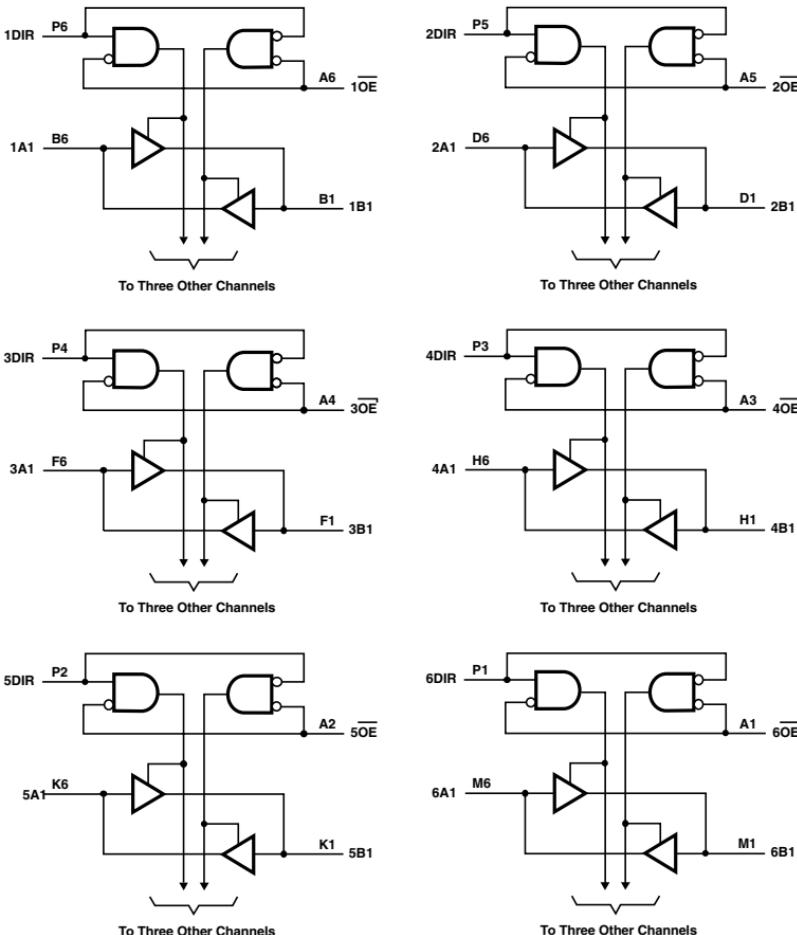
V <sub>CCA</sub> = 3.3V											
PARAMETER	INPUT	OUTPUT	MAX or MIN	AVC 3.3V	AVC 2.5V	AVC 1.8V	AVC 1.5V	AVCH 3.3V	AVCH 2.5V	AVCH 1.8V	AVCH 1.5V
$t_{PLH}$	A	B	MAX	2.9	3.4	4.6	5.7	2.9	3.4	4.6	5.7
$t_{PHL}$				2.9	3.4	4.6	5.7	2.9	3.4	4.6	5.7
$t_{PLH}$	B	A	MAX	2.9	3	3.5	3.9	2.9	3	3.5	3.9
$t_{PHL}$				2.9	3	3.5	3.9	2.9	3	3.5	3.9
$t_{PZH}$	$\overline{OE}$	A	MAX	4.1	4.2	4.3	4.4	4.1	4.2	4.3	4.4
$t_{ZPL}$				4.1	4.2	4.3	4.4	4.1	4.2	4.3	4.4
$t_{PZH}$	$\overline{OE}$	B	MAX	4.1	5.1	7.5	9.6	4.1	5.1	7.5	9.6
$t_{ZPL}$				4.1	5.1	7.5	9.6	4.1	5.1	7.5	9.6
$t_{PHZ}$	$\overline{OE}$	A	MAX	5	5	5	5	5	5	5	5
$t_{PLZ}$				5	5	5	5	5	5	5	5
$t_{PHZ}$	$\overline{OE}$	B	MAX	5	5.1	6.7	8.1	5	5.1	6.7	8.1
$t_{PLZ}$				5	5.1	6.7	8.1	5	5.1	6.7	8.1

UNIT : ns

## 24-BIT DUAL-SUPPLY BUS TRANSCEIVER WITH CONFIGURABLE VOLTAGE TRANSLATION AND 3-STATE OUTPUTS

- Control Inputs  $V_{IH}/V_{IL}$  Levels Are Referenced to  $V_{CCA}$  Voltage
- $V_{CC}$  Isolation Feature - If Either  $V_{CC}$  Input Is at GND, All Outputs Are in the High-Impedance State
- Overvoltage-Tolerant Inputs / Outputs Allow Mixed-Voltage-Mode Data Communications
- This 24-Bit Noninverting Bus Transceiver Uses Two Separate Configurable Power-Supply Rails
- Designed for asynchronous Communication Between Data Buses

**Logic Diagram**



**FUNCTION TABLE**  
(each 4-bit section)

INPUTS		OPERATION
OE	DIR	
L	L	B data to A bus
L	H	A data to B bus
H	X	Isolation

RECOMMENDED OPERATING CONDITIONS AND ELECTRICAL CHARACTERISTICS

PARAMETER	MAX or MIN	AVC 3.3V	AVC 2.5V	AVC 1.8V	AVC 1.8V	AVCH 3.3V	AVCH 2.5V	AVCH 1.8V	AVCH 1.8V	UNIT
I <sub>CC</sub> *	MAX	0.075	0.075	0.075	0.075	0.075	0.075	0.075	0.075	mA
I <sub>OH</sub>	MAX	-12	-9	-8	-6	-12	-9	-8	-6	mA
I <sub>OL</sub>	MAX	12	9	8	6	12	9	8	6	mA

\*I<sub>CCA</sub> + I<sub>CCB</sub>

SWITCHING CHARACTERISTICS

V <sub>CCA</sub> = 1.5V											
PARAMETER	INPUT	OUTPUT	MAX or MIN	AVC 3.3V	AVC 2.5V	AVC 1.8V	AVC 1.5V	AVCH 3.3V	AVCH 2.5V	AVCH 1.8V	AVCH 1.5V
t <sub>PLH</sub>	A	B	MAX	3.7	4.1	5.2	6.2	3.7	4.1	5.2	6.2
t <sub>PHL</sub>				3.7	4.1	5.2	6.2	3.7	4.1	5.2	6.2
t <sub>PLH</sub>	B	A	MAX	5.5	5.6	5.9	6.2	5.5	5.6	5.9	6.2
t <sub>PHL</sub>				5.5	5.6	5.9	6.2	5.5	5.6	5.9	6.2
t <sub>PZH</sub>	OE	A	MAX	10.1	10.1	10.1	10.1	10.1	10.1	10.1	10.1
t <sub>ZPL</sub>				10.1	10.1	10.1	10.1	10.1	10.1	10.1	10.1
t <sub>PZH</sub>	OE	B	MAX	5.2	5.9	8.1	10.1	5.2	5.9	8.1	10.1
t <sub>ZPL</sub>				5.2	5.9	8.1	10.1	5.2	5.9	8.1	10.1
t <sub>PHZ</sub>	OE	A	MAX	9.1	9.1	9.1	9.1	9.1	9.1	9.1	9.1
t <sub>ZPH</sub>				9.1	9.1	9.1	9.1	9.1	9.1	9.1	9.1
t <sub>PHZ</sub>	OE	B	MAX	6.3	6.5	7.5	8.7	6.3	6.5	7.5	8.7
t <sub>ZPH</sub>				6.3	6.5	7.5	8.7	6.3	6.5	7.5	8.7

UNIT : ns

V <sub>CCA</sub> = 1.8V											
PARAMETER	INPUT	OUTPUT	MAX or MIN	AVC 3.3V	AVC 2.5V	AVC 1.8V	AVC 1.5V	AVCH 3.3V	AVCH 2.5V	AVCH 1.8V	AVCH 1.5V
t <sub>PLH</sub>	A	B	MAX	3.3	3.7	4.8	5.9	3.3	3.7	4.8	5.9
t <sub>PHL</sub>				3.3	3.7	4.8	5.9	3.3	3.7	4.8	5.9
t <sub>PLH</sub>	B	A	MAX	4.4	4.5	4.8	5.2	4.4	4.5	4.8	5.2
t <sub>PHL</sub>				4.4	4.5	4.8	5.2	4.4	4.5	4.8	5.2
t <sub>PZH</sub>	OE	A	MAX	7.8	7.8	7.8	7.8	7.8	7.8	7.8	7.8
t <sub>ZPL</sub>				7.8	7.8	7.8	7.8	7.8	7.8	7.8	7.8
t <sub>PZH</sub>	OE	B	MAX	4.5	5.3	7.4	9.2	4.5	5.3	7.4	9.2
t <sub>ZPL</sub>				4.5	5.3	7.4	9.2	4.5	5.3	7.4	9.2
t <sub>PHZ</sub>	OE	A	MAX	7.7	7.7	7.7	7.7	7.7	7.7	7.7	7.7
t <sub>ZPH</sub>				7.7	7.7	7.7	7.7	7.7	7.7	7.7	7.7
t <sub>PHZ</sub>	OE	B	MAX	5.7	5.9	7.1	8.4	5.7	5.9	7.1	8.4
t <sub>ZPH</sub>				5.7	5.9	7.1	8.4	5.7	5.9	7.1	8.4

UNIT : ns

$V_{CCA} = 2.5V$

PARAMETER	INPUT	OUTPUT	MAX or MIN	AVC 3.3V	AVC 2.5V	AVC 1.8V	AVC 1.5V	AVCH 3.3V	AVCH 2.5V	AVCH 1.8V	AVCH 1.5V
$t_{PLH}$	A	B	MAX	2.8	3.3	4.5	5.6	2.8	3.3	4.5	5.6
				2.8	3.3	4.5	5.6	2.8	3.3	4.5	5.6
$t_{PHL}$	B	A	MAX	3.2	3.3	3.7	4.1	3.2	3.3	3.7	4.1
				3.2	3.3	3.7	4.1	3.2	3.3	3.7	4.1
$t_{PZH}$	$\bar{OE}$	A	MAX	5.3	5.3	5.3	5.3	5.3	5.3	5.3	5.3
				5.3	5.3	5.3	5.3	5.3	5.3	5.3	5.3
$t_{PZL}$	$\bar{OE}$	B	MAX	4.5	5.1	7.3	9.4	4.5	5.1	7.3	9.4
				4.5	5.1	7.3	9.4	4.5	5.1	7.3	9.4
$t_{PNC}$	$\bar{OE}$	A	MAX	6.1	6.1	6.1	6.1	6.1	6.1	6.1	6.1
				6.1	6.1	6.1	6.1	6.1	6.1	6.1	6.1
$t_{PNL}$	$\bar{OE}$	B	MAX	5.2	6.1	6.6	7.9	5.2	6.1	6.6	7.9
				5.2	6.1	6.6	7.9	5.2	6.1	6.6	7.9

UNIT : ns

$V_{CCA} = 3.3V$

PARAMETER	INPUT	OUTPUT	MAX or MIN	AVC 3.3V	AVC 2.5V	AVC 1.8V	AVC 1.5V	AVCH 3.3V	AVCH 2.5V	AVCH 1.8V	AVCH 1.5V
$t_{PLH}$	A	B	MAX	2.7	3.2	4.4	5.5	2.7	3.2	4.4	5.5
				2.7	3.2	4.4	5.5	2.7	3.2	4.4	5.5
$t_{PHL}$	B	A	MAX	2.7	2.8	3.3	3.7	2.7	2.8	3.3	3.7
				2.7	2.8	3.3	3.7	2.7	2.8	3.3	3.7
$t_{PZH}$	$\bar{OE}$	A	MAX	4	4.1	4.2	4.3	4	4.1	4.2	4.3
				4	4.1	4.2	4.3	4	4.1	4.2	4.3
$t_{PZL}$	$\bar{OE}$	B	MAX	4	4.9	7.2	9.3	4	4.9	7.2	9.3
				4	4.9	7.2	9.3	4	4.9	7.2	9.3
$t_{PNC}$	$\bar{OE}$	A	MAX	5	5	5	5	5	5	5	5
				5	5	5	5	5	5	5	5
$t_{PNL}$	$\bar{OE}$	B	MAX	5	5.2	6.5	7.7	5	5.2	6.5	7.7
				5	5.2	6.5	7.7	5	5.2	6.5	7.7

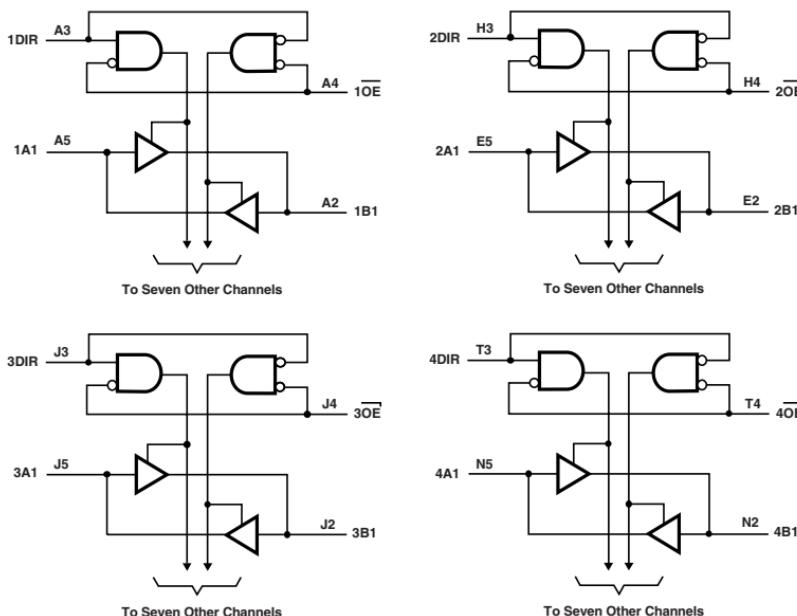
UNIT : ns

# 32T245

## 32-BIT DUAL-SUPPLY BUS TRANSCEIVER WITH CONFIGURABLE VOLTAGE TRANSLATION AND 3-STATE OUTPUTS

- Control Inputs  $V_{IH}/V_{IL}$  Levels Are Referenced to  $V_{CCA}$  Voltage
- $V_{CC}$  Isolation Feature - If Either  $V_{CC}$  Input Is at GND, Both Ports Are in the High-Impedance State
- Overvoltage-Tolerant Inputs / Outputs Allow Mixed-Voltage-Mode Data Communications
- This 24-Bit Noninverting Bus Transceiver Uses Two Separate Configurable Power-Supply Rails
- Designed for asynchronous Communication Between Data Buses

Logic Diagram



FUNCTION TABLE  
(each 8-bit section)

INPUTS		OPERATION
OE	DIR	
L	L	B data to A bus
L	H	A data to B bus
H	X	Isolation

## RECOMMENDED OPERATING CONDITIONS AND ELECTRICAL CHARACTERISTICS

PARAMETER	MAX or MIN	AVC 3.3V	AVC 2.5V	AVC 1.8V	AVC 1.8V	AVCH 3.3V	AVCH 2.5V	AVCH 1.8V	AVCH 1.8V	UNIT
I <sub>CC</sub> *	MAX	0.09	0.09	0.09	0.09	0.09	0.09	0.09	0.09	mA
I <sub>OH</sub>	MAX	-12	-9	-8	-6	-12	-9	-8	-6	mA
I <sub>OL</sub>	MAX	12	9	8	6	12	9	8	6	mA

\*I<sub>CCA</sub> + I<sub>CCS</sub>

## SWITCHING CHARACTERISTICS

V <sub>CCA</sub> = 1.5V											
PARAMETER	INPUT	OUTPUT	MAX or MIN	AVC 3.3V	AVC 2.5V	AVC 1.8V	AVC 1.5V	AVCH 3.3V	AVCH 2.5V	AVCH 1.8V	AVCH 1.5V
t <sub>PLH</sub>	A	B	MAX	3.7	4.1	5.2	6.2	3.7	4.1	5.2	6.2
t <sub>PLH</sub>				3.7	4.1	5.2	6.2	3.7	4.1	5.2	6.2
t <sub>PLH</sub>	B	A	MAX	5.5	5.6	5.9	6.2	5.5	5.6	5.9	6.2
t <sub>PLH</sub>				5.5	5.6	5.9	6.2	5.5	5.6	5.9	6.2
t <sub>PZH</sub>	$\overline{OE}$	A	MAX	10.1	10.1	10.1	10.1	10.1	10.1	10.1	10.1
t <sub>PZH</sub>				10.1	10.1	10.1	10.1	10.1	10.1	10.1	10.1
t <sub>PZH</sub>	$\overline{OE}$	B	MAX	5.2	5.9	8.1	10.1	5.2	5.9	8.1	10.1
t <sub>PZH</sub>				5.2	5.9	8.1	10.1	5.2	5.9	8.1	10.1
t <sub>PZL</sub>	$\overline{OE}$	A	MAX	9.1	9.1	9.1	9.1	9.1	9.1	9.1	9.1
t <sub>PZL</sub>				9.1	9.1	9.1	9.1	9.1	9.1	9.1	9.1
t <sub>PZL</sub>	$\overline{OE}$	B	MAX	6.3	6.5	7.5	8.7	6.3	6.5	7.5	8.7
t <sub>PZL</sub>				6.3	6.5	7.5	8.7	6.3	6.5	7.5	8.7

UNIT : ns

V <sub>CCA</sub> = 1.8V											
PARAMETER	INPUT	OUTPUT	MAX or MIN	AVC 3.3V	AVC 2.5V	AVC 1.8V	AVC 1.5V	AVCH 3.3V	AVCH 2.5V	AVCH 1.8V	AVCH 1.5V
t <sub>PLH</sub>	A	B	MAX	3.3	3.7	4.8	5.9	3.3	3.7	4.8	5.9
t <sub>PLH</sub>				3.3	3.7	4.8	5.9	3.3	3.7	4.8	5.9
t <sub>PLH</sub>	B	A	MAX	4.4	4.5	4.8	5.2	4.4	4.5	4.8	5.2
t <sub>PLH</sub>				4.4	4.5	4.8	5.2	4.4	4.5	4.8	5.2
t <sub>PZH</sub>	$\overline{OE}$	A	MAX	7.8	7.8	7.8	7.8	7.8	7.8	7.8	7.8
t <sub>PZH</sub>				7.8	7.8	7.8	7.8	7.8	7.8	7.8	7.8
t <sub>PZH</sub>	$\overline{OE}$	B	MAX	4.5	5.3	7.4	9.2	4.5	5.3	7.4	9.2
t <sub>PZH</sub>				4.5	5.3	7.4	9.2	4.5	5.3	7.4	9.2
t <sub>PZL</sub>	$\overline{OE}$	A	MAX	7.7	7.7	7.7	7.7	7.7	7.7	7.7	7.7
t <sub>PZL</sub>				7.7	7.7	7.7	7.7	7.7	7.7	7.7	7.7
t <sub>PZL</sub>	$\overline{OE}$	B	MAX	5.7	5.9	7.1	8.4	5.7	5.9	7.1	8.4
t <sub>PZL</sub>				5.7	5.9	7.1	8.4	5.7	5.9	7.1	8.4

UNIT : ns

V <sub>CCA</sub> = 2.5V											
PARAMETER	INPUT	OUTPUT	MAX or MIN	AVC 3.3V	AVC 2.5V	AVC 1.8V	AVC 1.5V	AVCH 3.3V	AVCH 2.5V	AVCH 1.8V	AVCH 1.5V
t <sub>PLH</sub>	A	B	MAX	2.8	3.3	4.5	5.6	2.8	3.3	4.5	5.6
t <sub>PLH</sub>				2.8	3.3	4.5	5.6	2.8	3.3	4.5	5.6
t <sub>PLH</sub>	B	A	MAX	3.2	3.3	3.7	4.1	3.2	3.3	3.7	4.1
t <sub>PLH</sub>				3.2	3.3	3.7	4.1	3.2	3.3	3.7	4.1
t <sub>PZH</sub>	$\overline{OE}$	A	MAX	5.3	5.3	5.3	5.3	5.3	5.3	5.3	5.3
t <sub>PZH</sub>				5.3	5.3	5.3	5.3	5.3	5.3	5.3	5.3
t <sub>PZH</sub>	$\overline{OE}$	B	MAX	4.5	5.1	7.3	9.4	4.5	5.1	7.3	9.4
t <sub>PZH</sub>				4.5	5.1	7.3	9.4	4.5	5.1	7.3	9.4
t <sub>PZL</sub>	$\overline{OE}$	A	MAX	6.1	6.1	6.1	6.1	6.1	6.1	6.1	6.1
t <sub>PZL</sub>				6.1	6.1	6.1	6.1	6.1	6.1	6.1	6.1
t <sub>PZL</sub>	$\overline{OE}$	B	MAX	5.2	6.1	6.6	7.9	5.2	6.1	6.6	7.9
t <sub>PZL</sub>				5.2	6.1	6.6	7.9	5.2	6.1	6.6	7.9

UNIT : ns

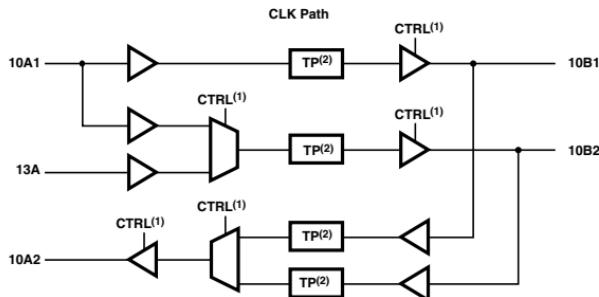
$V_{CCA} = 3.3V$											
PARAMETER	INPUT	OUTPUT	MAX or MIN	AVC 3.3V	AVC 2.5V	AVC 1.8V	AVC 1.5V	AVCH 3.3V	AVCH 2.5V	AVCH 1.8V	AVCH 1.5V
$t_{PLH}$	A	B	MAX	2.7	3.2	4.4	5.5	2.7	3.2	4.4	5.5
$t_{PHL}$				2.7	3.2	4.4	5.5	2.7	3.2	4.4	5.5
$t_{PLH}$	B	A	MAX	2.7	2.8	3.3	3.7	2.7	2.8	3.3	3.7
$t_{PHL}$				2.7	2.8	3.3	3.7	2.7	2.8	3.3	3.7
$t_{PZH}$	$\overline{OE}$	A	MAX	4	4.1	4.2	4.3	4	4.1	4.2	4.3
$t_{ZPI}$				4	4.1	4.2	4.3	4	4.1	4.2	4.3
$t_{PZB}$	$\overline{OE}$	B	MAX	4	4.9	7.2	9.3	4	4.9	7.2	9.3
$t_{ZPB}$				4	4.9	7.2	9.3	4	4.9	7.2	9.3
$t_{PHZ}$	$\overline{OE}$	A	MAX	5	5	5	5	5	5	5	5
$t_{HZP}$				5	5	5	5	5	5	5	5
$t_{PHZ}$	$\overline{OE}$	B	MAX	5	5.2	6.5	7.7	5	5.2	6.5	7.7
$t_{HZP}$				5	5.2	6.5	7.7	5	5.2	6.5	7.7

UNIT : ns

## MMC, SD CARD, Memory Stick, SmartMedia, AND xD-Picture Card ±15-kV ESD-PROTECTED VOLTAGE-TRANSLATION TRANCEIVER

- Transceiver for Memory Card Interface  
[MultiMediaCard (MMC), Secure Digital (SD), Memory Stick™ Compliant Products, SmartMedia Card, and xD-Picture Card™]
- For Low-Power Operation, A ports Are Placed in High-Impedance State When Card-Side Supply Voltage Is Switched Off

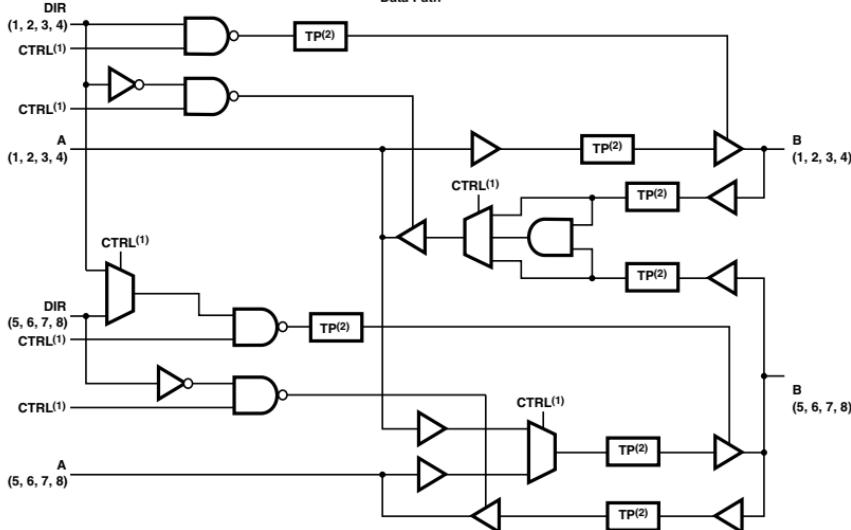
**Logic Diagram**



(1) CTRL represents a decoded MODE0, MODE1,  $\overline{CS0}$ , and  $\overline{CS1}$  state.

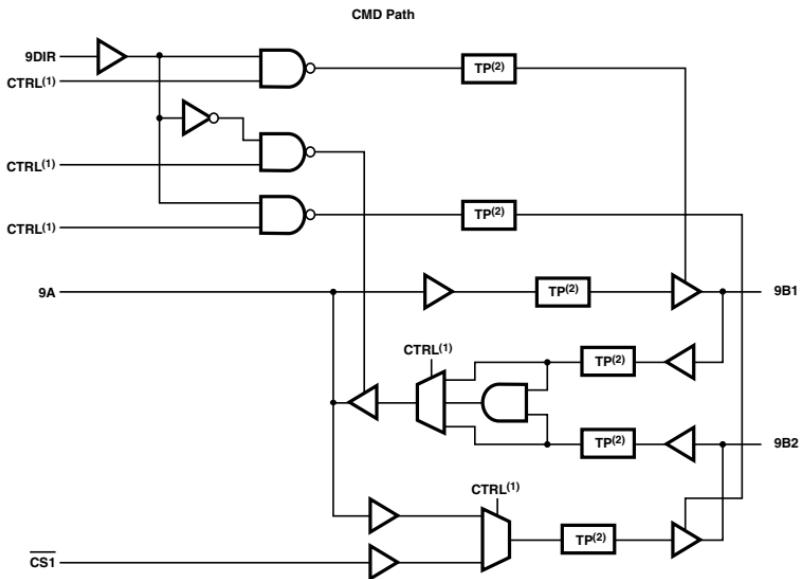
(2) Translation point

**Data Path**



(1) CTRL represents a decoded MODE0, MODE1,  $\overline{CS0}$ , and  $\overline{CS1}$  state.

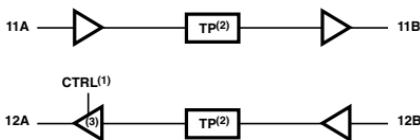
(2) Translation point



(1) CTRL represents a decoded MODE0, MODE1, CS0, and CS1 state.

(2) Translation point

**WP and R/B Paths**

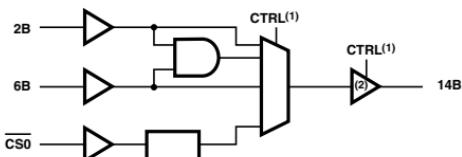


(1) CTRL represents a decoded MODE0, MODE1, CS0, and CS1 state.

(2) Translation point

(3) 12A is open drain in NAND (XD) mode and push/pull in other modes.

**IRQ and CEout Paths**



(1) CTRL represents a decoded MODE0, MODE1, CS0, and CS1 state.

(2) Push/pull in NAND (XD) mode and open drain in other modes

## ELECTRICAL CHARACTERISTICS

PARAMETER	MAX or MIN	AVCA $V_{CCA} = 3.3V$ $V_{CCB} = 0V$	AVCA $V_{CCA} = 3.3V$ $V_{CCB} = 3.3V$	AVCA $V_{CCA} = 2.5V$ $V_{CCB} = 2.5V$	AVCA $V_{CCA} = 1.8V$ $V_{CCB} = 0V$	AVCA $V_{CCA} = 1.8V$ $V_{CCB} = 1.8V$	AVCA $V_{CCA} = 1.5V$ $V_{CCB} = 1.5V$	UNIT
$I_{CCA}$	MAX	0.01	0.01	0.0055	0.005	0.005	0.0045	mA
$I_{CCB}$	MAX	0.01	0.001	0.0075	0.0005	0.007	0.0065	mA

## RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	AVCA 3.3V	AVCA 2.5V	AVCA 1.8V	AVCA 1.5V	UNIT
$I_{IOH}$	MAX	-8	-4	-2	-1	mA
		8	4	2	1	mA
$I_{IOL}$	MAX	-16	-8	-4	-2	mA
		16	8	4	2	mA

\* $I_{IOH,SB} = 0$ 

## SWITCHING CHARACTERISTICS

$V_{CCA} = 1.5V$						
PARAMETER	INPUT (FROM)	OUTPUT (TO)	MAX or MIN	AVCA $V_{CCA}$ 3.3V	AVCA $V_{CCA}$ 2.5V	AVCA $V_{CCA}$ 1.8V
$t_{SU}$	A	B	MAX	4.4	4.9	7.7
$t_{SD}$	B	A	MAX	5	5	6.3
$t_{pd}$	CLK, or SCLK,h	CLK, or SCLK,h	MAX	4.9	5	7.7
$t_{pd}$	CLK, or SCLK,h	CLK, or SCLK-f,h	MAX	9.7	12	19
$t_{pd}$	CMD,h	CMD,h	MAX	3.6	4.1	7.1
$t_{pd}$	CMD,h	CMD,1	MAX	4.2	4.6	7
$t_{pd}$	CMD,0	CMD,h	MAX	4.7	4.9	6.2
$t_{pd}$	CSD	B	MAX	3.9	4.2	6
$t_{pd}$	R/B	R/B,h	MAX	4.8	4.8	5.7
$t_{pd}$	WE	WE,h	MAX	4.2	4.3	7.4
$t_{pd}$	WP	WP,h	MAX	4.3	4.5	6.6
$t_{pd}$	DAT1.0 or DATA1.0	IRQ	MAX	3.3	3.3	4.8
$t_{pd}$	DAT1.0 or DATA1.1	IRQ	MAX	3.3	3.4	4.9
$t_{pd}$	DIR	B	MAX	4.6	4.5	6.7
$t_{pd}$	DIR	A	MAX	9.5	9.6	10.3
$t_{pd}$	R/B	R/B,h open drain	MAX	5.4	5.4	5.9
$t_{pd}$	DAT1.0 or DATA1.0	IRQ	MAX	5.5	4.9	6.7
$t_{pd}$	DAT1.0 or DATA1.1	IRQ	MAX	5.4	4.7	6.5
$t_{pd}$	DIR	B	MAX	6.3	6.4	6.9
$t_{pd}$	DIR	A	MAX	5.2	5.3	5.3
$t_{pd}$	R/B	R/B,h open drain	MAX	4.1	17.4	16.9

UNIT : ns

V <sub>CCA</sub> = 1.8V						
PARAMETER	INPUT (FROM)	OUTPUT (TO)	MAX or MIN	AVCA V <sub>CCA</sub> 3.3V	AVCA V <sub>CCA</sub> 2.5V	AVCA V <sub>CCA</sub> 1.8V
t <sub>pd</sub>	A	B	MAX	3.7	4.6	7.5
t <sub>pd</sub>	B	A	MAX	4	4.2	4.6
t <sub>pd</sub>	CLK, or SCLK.h	CLK, or SCLK.0	MAX	4.2	4.8	8
t <sub>pd</sub>	CLK, or SCLK.h	CLK, or SCLK.-f.h	MAX	8.3	9.4	17.9
t <sub>pd</sub>	CMD.h	CMD.0	MAX	3.3	3.7	7.4
t <sub>pd</sub>	CMD.h	CMD.1	MAX	3.5	4.4	6.2
t <sub>pd</sub>	CMD.0	CMD.h	MAX	3.8	4	4.5
t <sub>pd</sub>	CS0	B	MAX	3.8	4	6.6
t <sub>pd</sub>	R/B	R/B.h	MAX	3.8	4	4.4
t <sub>pd</sub>	WE	WE.h	MAX	3.7	3.9	7.3
t <sub>pd</sub>	WP	WP.h	MAX	3.8	4	5.6
t <sub>on</sub>	DAT1.0 or DATA1.0	IRQ	MAX	3.3	3.3	5
t <sub>on</sub>	DAT1.0 or DATA1.1	IRQ	MAX	3.1	3.1	4.6
t <sub>on</sub>	DIR	B	MAX	3.6	3.8	6.4
t <sub>on</sub>	DIR	A	MAX	6.9	6.9	7.7
t <sub>on</sub>	R/B	R/B.h open drain	MAX	4.1	4.1	4.4
t <sub>dis</sub>	DAT1.0 or DATA1.0	IRQ	MAX	5.5	4.8	6.5
t <sub>dis</sub>	DAT1.0 or DATA1.1	IRQ	MAX	5.3	4.8	6.6
t <sub>dis</sub>	DIR	B	MAX	5.7	5.4	6.3
t <sub>dis</sub>	DIR	A	MAX	5.2	5.3	5.2
t <sub>dis</sub>	R/B	R/B.h open drain	MAX	3.8	19.5	15.9

UNIT : ns

V <sub>CCA</sub> = 2.5V						
PARAMETER	INPUT (FROM)	OUTPUT (TO)	MAX or MIN	AVCA V <sub>CCA</sub> 3.3V	AVCA V <sub>CCA</sub> 2.5V	
t <sub>pd</sub>	A	B	MAX	3.1	4	
t <sub>pd</sub>	B	A	MAX	3.6	3.7	
t <sub>pd</sub>	CLK, or SCLK.h	CLK, or SCLK.0	MAX	3.5	3.9	
t <sub>pd</sub>	CLK, or SCLK.h	CLK, or SCLK.-f.h	MAX	7	8.3	
t <sub>pd</sub>	CMD.h	CMD.0	MAX	2.7	3.2	
t <sub>pd</sub>	CMD.h	CMD.1	MAX	2.8	3.6	
t <sub>pd</sub>	CMD.0	CMD.h	MAX	3	3	
t <sub>pd</sub>	CS0	B	MAX	3.3	4.2	
t <sub>pd</sub>	R/B	R/B.h	MAX	2.9	3.1	
t <sub>pd</sub>	WE	WE.h	MAX	3	3.6	
t <sub>pd</sub>	WP	WP.h	MAX	2.9	3.5	
t <sub>on</sub>	DAT1.0 or DATA1.0	IRQ	MAX	3.2	3.3	
t <sub>on</sub>	DAT1.0 or DATA1.1	IRQ	MAX	3.2	3.6	
t <sub>on</sub>	DIR	B	MAX	3.6	4.7	
t <sub>on</sub>	DIR	A	MAX	5.1	5.3	
t <sub>on</sub>	R/B	R/B.h open drain	MAX	3	3.2	
t <sub>dis</sub>	DAT1.0 or DATA1.0	IRQ	MAX	5.4	7.2	
t <sub>dis</sub>	DAT1.0 or DATA1.1	IRQ	MAX	5.4	7	
t <sub>dis</sub>	DIR	B	MAX	5.1	4.5	
t <sub>dis</sub>	DIR	A	MAX	3.7	3.7	
t <sub>dis</sub>	R/B	R/B.h open drain	MAX	3.9	3.2	

UNIT : ns

V <sub>CCA</sub> = 3.3V						
PARAMETER	INPUT (FROM)	OUTPUT (TO)	MAX or MIN	AVCA V <sub>CCA</sub> 3.3V		
t <sub>pd</sub>	A	B	MAX	2.9		
t <sub>pd</sub>	B	A	MAX	3.8		
t <sub>pd</sub>	CLK, or SCLK.h	CLK, or SCLK.0	MAX	3.3		
t <sub>pd</sub>	CLK, or SCLK.h	CLK, or SCLK.-f.h	MAX	6.1		
t <sub>pd</sub>	CMD.h	CMD.0	MAX	2.7		
t <sub>pd</sub>	CMD.h	CMD.1	MAX	2.7		
t <sub>pd</sub>	CMD.0	CMD.h	MAX	2.6		
t <sub>pd</sub>	CS0	B	MAX	3.7		
t <sub>pd</sub>	R/B	R/B.h	MAX	2.5		
t <sub>pd</sub>	WE	WE.h	MAX	3		
t <sub>pd</sub>	WP	WP.h	MAX	2.8		
t <sub>on</sub>	DAT1.0 or DATA1.0	IRQ	MAX	3.2		
t <sub>on</sub>	DAT1.0 or DATA1.1	IRQ	MAX	3.2		
t <sub>on</sub>	DIR	B	MAX	3.7		
t <sub>on</sub>	DIR	A	MAX	4.7		
t <sub>on</sub>	R/B	R/B.h open drain	MAX	4.9		
t <sub>dis</sub>	DAT1.0 or DATA1.0	IRQ	MAX	5.3		
t <sub>dis</sub>	DAT1.0 or DATA1.1	IRQ	MAX	5.2		
t <sub>dis</sub>	DIR	B	MAX	5		
t <sub>dis</sub>	DIR	A	MAX	4.7		
t <sub>dis</sub>	R/B	R/B.h open drain	MAX	6		

UNIT : ns

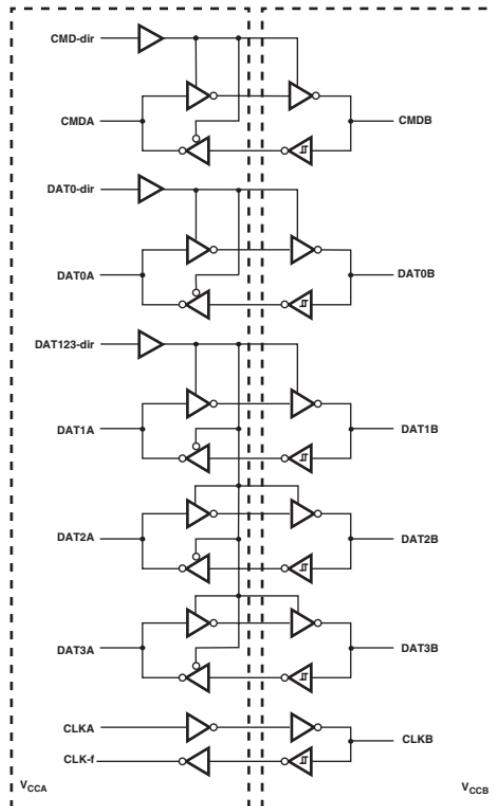
## MAXIMUM FREQUENCY AND OUTPUT SKEW

$V_{CCB} = 3.3V$									
PARAMETER		INPUT (FROM)	OUTPUT T (TO)	MAX or MIN	AVCA $V_{CCA}$ 3.3V	AVCA $V_{CCA}$ 2.5V	AVCA $V_{CCA}$ 1.8V	AVCA $V_{CCA}$ 1.5V	UNIT
$f_{max}$	Clock	A	B	MIN	52	52	52	52	MHz
		B	A		52	52	52	52	MHz
	Data	A	B	MIN	26	26	26	26	MHz
		B	A		26	26	26	26	MHz
$t_{skew}$		A	B	MAX	0.7	0.7	0.8	1.5	ns

UNIT : ns

**MMC, SD CARD, Memory Stick, SmartMedia, AND xD-Picture Card ±15-kV ESD-PROTECTED VOLTAGE-TRANSLATION TRANCEIVER**

- Transceiver for Memory Card Interface  
[MultiMediaCard (MMC), Secure Digital (SD), Memory Stick™ Compliant Products]
- For Low-Power Operation, A and B ports Are Placed in High-Impedance State When Either Supply Voltage Is Switched Off

**Logic Diagram**

**FUNCTION TABLES**

CONTROL INPUT CMD-dir	OUTPUT CIRCUITS		OPERATION
	CMDA	CMDB	
High	Hi-Z	Enabled	CMDA to CMDB
Low	Enabled	Hi-Z	CMDB to CMDA

CONTROL INPUT DAT0-dir	OUTPUT CIRCUITS		FUNCTION
	DAT0A	DAT0B	
High	Hi-Z	Enabled	DAT0A to DAT0B
Low	Enabled	Hi-Z	DAT0B to DAT0A

## ELECTRICAL CHARACTERISTICS

PARAMETER	MAX or MIN	AVCA $V_{CCA} = 3.3V$ $V_{CCB} = 0V$	AVCA $V_{CCA} = 0V$ $V_{CCB} = 3.3V$	AVCA $V_{CCA} = 1.2$ to $3.3V$ $V_{CCB} = 1.2$ to $3.3V$	UNIT
$I_{CCA}$	MAX	0.01	-0.001	10	mA
$I_{CCB}$	MAX	-0.001	0.01	10	mA
$I_{CCA} + I_{CCB}$	MAX	-	-	15	mA

## RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	AVCA 3.3V	AVCA 2.5V	AVCA 1.8V	AVCA 1.5V	UNIT
$I_{DH}$	MAX	-8	-4	-2	-1	mA
$I_{DL}$		8	4	2	1	mA
$I_{DH}$	MAX	-16	-8	-4	-2	mA
$I_{DL}$		16	8	4	2	mA

<sup>\*</sup> $I_{DSD} = 0$ 

## SWITCHING CHARACTERISTICS

V <sub>CCA</sub> = 1.5V							
PARAMETER	INPUT (FROM)	OUTPUT (TO)	MAX or MIN	AVCA V <sub>CCA</sub> 3.3V	AVCA V <sub>CCA</sub> 2.5V	AVCA V <sub>CCA</sub> 1.8V	AVCA V <sub>CCA</sub> 1.5V
$t_{pd}$	A	B	MAX	3.8	3.9	4.8	5.6
$t_{pd}$	B	A	MAX	5.2	5.2	5.6	6
$t_{pd}$	CLKA	CLKB	MAX	3.8	3.9	4.8	5.6
$t_{pd}$		CLK-f	MAX	9	9.1	10.4	116
$t_{pd}$	CMDA	CMDB	MAX	3.8	3.9	4.8	5.6
$t_{pd}$		CMDB	MAX	5.2	5.2	5.6	6
$t_{pd}$	DIR	B	MAX	5.9	6.1	6.9	7.7
$t_{pd}$		A	MAX	7.7	8.2	7.4	7
$t_{pd}$	DIR	B	MAX	11.4	8.7	10.4	8.9
$t_{pd}$		A	MAX	6.6	6.5	6.8	7

UNIT : ns

V <sub>CCA</sub> = 1.8V							
PARAMETER	INPUT (FROM)	OUTPUT (TO)	MAX or MIN	AVCA V <sub>CCA</sub> 3.3V	AVCA V <sub>CCA</sub> 2.5V	AVCA V <sub>CCA</sub> 1.8V	AVCA V <sub>CCA</sub> 1.5V
$t_{pd}$	A	B	MAX	3.1	3.5	4.4	5.2
$t_{pd}$	B	A	MAX	4.3	4.3	4.8	5.2
$t_{pd}$	CLKA	CLKB	MAX	3.1	3.5	4.4	5.2
$t_{pd}$		CLK-f	MAX	7.4	7.8	9.1	10.4
$t_{pd}$	CMDA	CMDB	MAX	3.1	3.5	4.4	5.2
$t_{pd}$		CMDB	MAX	4.3	4.3	4.8	5.2
$t_{pd}$	DIR	B	MAX	4.8	5.1	6	6.8
$t_{pd}$		A	MAX	5.3	5.1	5.2	4.7
$t_{pd}$	DIR	B	MAX	8.2	8.2	9.5	8.4
$t_{pd}$		A	MAX	7.6	7.5	7.9	7.7

UNIT : ns

V <sub>CCA</sub> = 2.5V							
PARAMETER	INPUT (FROM)	OUTPUT (TO)	MAX or MIN	AVCA V <sub>CCA</sub> 3.3V	AVCA V <sub>CCA</sub> 2.5V	AVCA V <sub>CCA</sub> 1.8V	AVCA V <sub>CCA</sub> 1.5V
$t_{pd}$	A	B	MAX	2.5	2.9	3.8	4.7
$t_{pd}$	B	A	MAX	3.2	3.3	3.9	4.4
$t_{pd}$	CLKA	CLKB	MAX	2.5	2.9	3.8	4.7
$t_{pd}$		CLK-f	MAX	5.7	6.2	7.7	9.1
$t_{pd}$	CMDA	CMDB	MAX	2.5	2.9	3.8	4.7
$t_{pd}$		CMDB	MAX	3.2	3.3	3.9	4.4
$t_{pd}$	DIR	B	MAX	3.6	3.9	4.8	5.7
$t_{pd}$		A	MAX	4.7	4.4	4.3	3.5
$t_{pd}$	DIR	B	MAX	7.5	7.2	8.4	7.6
$t_{pd}$		A	MAX	5.8	5.5	5.4	5.6

UNIT : ns

V <sub>CCA</sub> = 3.3V							
PARAMETER	INPUT (FROM)	OUTPUT (TO)	MAX or MIN	AVCA V <sub>CCA</sub> 3.3V	AVCA V <sub>CCA</sub> 2.5V	AVCA V <sub>CCA</sub> 1.8V	AVCA V <sub>CCA</sub> 1.5V
t <sub>pd</sub>	A	B	MAX	2.3	2.7	3.6	4.5
t <sub>pd</sub>	B	A	MAX	2.7	3	3.7	4.3
t <sub>pd</sub>	CLKA	CLKB	MAX	2.3	2.7	3.6	4.5
t <sub>pd</sub>	CLK-f	CLK-f	MAX	5	5.7	7.3	8.8
t <sub>pd</sub>	CMDA	CMDB	MAX	2.3	2.7	3.6	4.5
t <sub>pd</sub>	CMDB	CMDA	MAX	2.7	3	3.7	4.3
t <sub>en</sub>	DIR	B	MAX	3	3.4	4.3	5.1
t <sub>en</sub>		A	MAX	5.4	5.4	5.4	3.1
t <sub>dis</sub>	DIR	B	MAX	7.3	7	8.3	7.4
t <sub>dis</sub>		A	MAX	8	7.9	7.9	8.1

UNIT : ns

#### MAXIMUM FREQUENCY

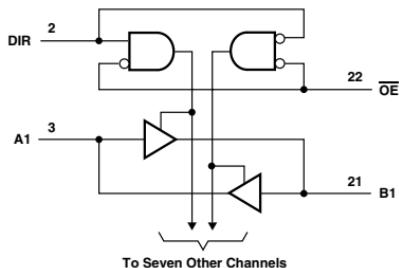
PARAMETER	INPUT (FROM)	OUTPUT (TO)	MAX or MIN	AVCA V <sub>CCA</sub> 3.3V	AVCA V <sub>CCA</sub> 2.5V	AVCA V <sub>CCA</sub> 1.8V	AVCA V <sub>CCA</sub> 1.5V	UNIT	
f <sub>max</sub>	Clock	CLKA	CLKB	MIN	95	95	95	95	MHz
		CLK-f	CLK-f		95	95	95	95	MHz
	Data	A	B	MIN	95	95	95	95	MHz
		B	A		95	95	95	95	MHz

#### OUTPUT SKEW

PARAMETER	V <sub>CCA</sub>	INPUT (FROM)	OUTPUT (TO)	MAX or MIN	AVCA V <sub>CCA</sub> 3.3V	AVCA V <sub>CCA</sub> 2.5V	AVCA V <sub>CCA</sub> 1.8V	AVCA V <sub>CCA</sub> 1.5V	UNIT
t <sub>skew</sub>	3.3V	DIR	B	MIN	0.4	0.3	0.4	0.3	ns
	2.5V	DIR	B	MIN	0.3	0.2	0.3	0.3	ns
	1.8V	DIR	B	MIN	0.3	0.3	0.3	0.3	ns
	1.5V	DIR	B	MIN	0.4	0.3	0.3	0.3	ns

## OCTAL BUS TRANSCEIVER WITH ADJUSTABLE OUTPUT VOLTAGE AND 3-STATE OUTPUTS

Logic Diagram



FUNCTION TABLE

INPUTS	OPERATION	
OE	DIR	
L	L	B data to A bus
L	H	A data to B bus
H	X	Isolation

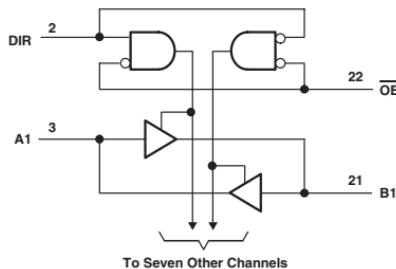
ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER		MAX or MIN	V <sub>CCA</sub> (V)	V <sub>CCB</sub> (V)	LVCC	UNIT
I <sub>CCA</sub>	B to A	MAX	3.6	3.6	0.05	mA
				5.5	0.05	mA
I <sub>CCB</sub>	A to B	MAX	3.6	3.6	0.05	mA
				5.5	0.08	mA
I <sub>lOA</sub>		MAX		2.3	-8	mA
				2.7	-12	
				3.3	-24	
I <sub>lOB</sub>		MAX		2.3	3.3	mA
				2.7	-12	
				3.3	-24	
I <sub>lOA</sub>		MAX		2.3	8	mA
				2.7	12	
				3.3	24	
I <sub>lOB</sub>		MAX		2.3	8	mA
				2.7	12	
				3.3	24	

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	LVCC	LVCC	LVCC	LVCC	LVCC
				V <sub>CCA</sub> = 2.3V V <sub>CCB</sub> = 3.0V	V <sub>CCA</sub> = 2.7V V <sub>CCB</sub> = 5.5V	V <sub>CCA</sub> = 3.6V V <sub>CCB</sub> = 5.5V	V <sub>CCA</sub> = 2.7V V <sub>CCB</sub> = 3.0V	V <sub>CCA</sub> = 3.6V V <sub>CCB</sub> = 3.0V
I <sub>PZH</sub>	A	B	MAX	9.4	6.0	6.0	7.1	7.1
				9.1	5.3	5.3	7.2	7.2
I <sub>PZL</sub>	B	A	MAX	11.2	5.8	5.8	6.4	6.4
				9.9	7.0	7.0	7.6	7.6
I <sub>PZL</sub>	OE	Ā	MAX	14.5	9.2	9.2	9.7	9.7
				12.9	9.5	9.5	9.5	9.5
I <sub>PZL</sub>	OE	B̄	MAX	13	8.1	8.1	9.2	9.2
				12.8	8.4	8.4	9.9	9.9
I <sub>PZL</sub>	OE	Ā	MAX	7.1	7.0	7.0	6.6	6.6
				6.9	7.8	7.8	6.9	6.9
I <sub>PZL</sub>	OE	B̄	MAX	8.8	7.3	7.3	7.5	7.5
				8.9	7.0	7.0	7.9	7.9

UNIT: ns

**OCTAL BUS TRANSCEIVER AND 3.3-V TO 5-V SHIFTER WITH 3-STATE OUTPUTS  
(SN74LVC4245A)**
**OCTAL DUAL-SUPPLY BUS TRANSCEIVER WITH CONFIGURABLE OUTPUT VOLTAGE AND  
3-STATE OUTPUTS (SN74LVCC4245A)**
**Logic Diagram****FUNCTION TABLE**

INPUTS	OUTPUTS	OPERATION
OE	DIR	
L	L	B data to A bus
L	H	A data to B bus
H	X	Isolation

**ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS**

PARAMETER	MAX or MIN	LVC		UNIT
		VCCA=5.5V	VCCB=5.5V	
ICCA	MAX	0.08	0.08	mA
	VCCA=5.5V VCCB=3.6V	0.08	0.08	mA
ICCB	MAX	0.05	0.08	mA
	VCCA=5.5V VCCB=3.6V	0.05	0.05	mA
IOH	VCCB=3.3V	MAX	-24	mA
			24	
IOL	VCCB=2.7V	MAX	-12	mA
			12	
IOL	VCCA=4.5V	MAX	-24	mA
			24	

**SWITCHING CHARACTERISTICS**

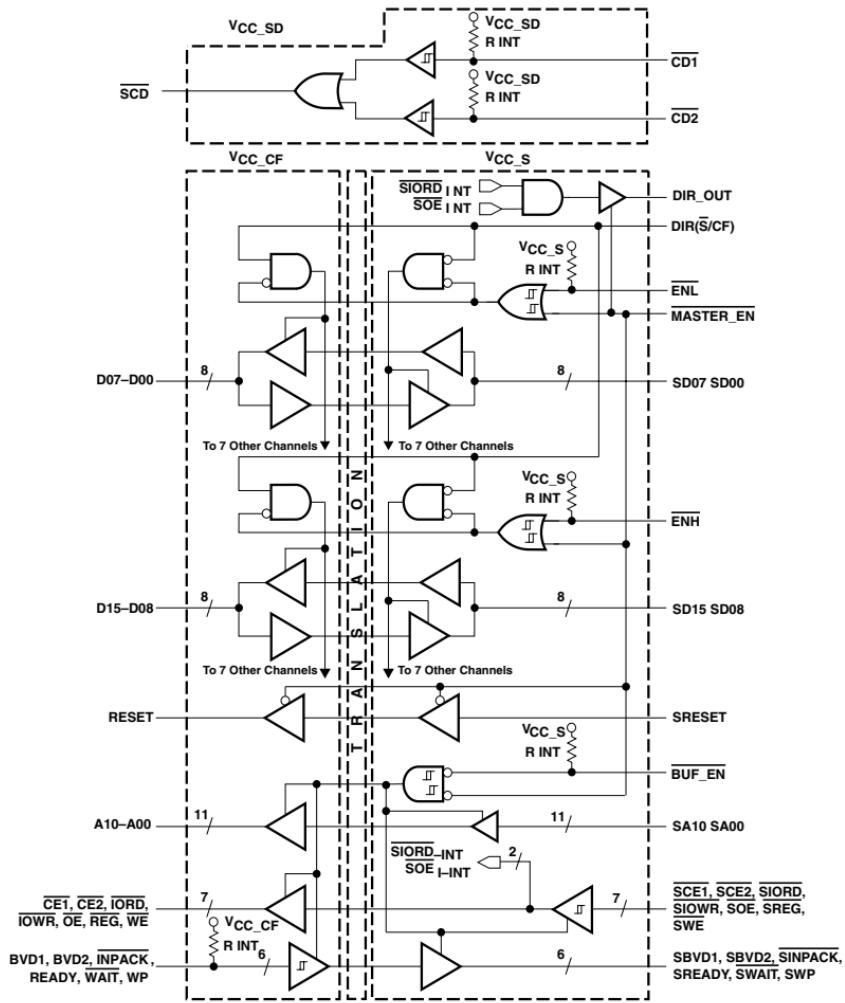
PARAMETER	INPUT	OUTPUT	MAX or MIN	LVC		LVCC		
				VCCA=5.5V VCCB=2.7V	VCCA=5.5V VCCB=3.6V	VCCA=5.5V VCCB=5.5V	VCCA=5.5V VCCB=2.7V	VCCA=5.5V VCCB=3.6V
TPLH	A	B	MAX	6.3	6.3	7.1	7.0	7.0
				6.7	6.7	6.0	7.0	7.0
TPHL	B	A	MAX	6.1	6.1	6.8	6.2	6.2
				5.0	5.0	6.1	5.3	5.3
TPZL	OE	A	MAX	9.0	9.0	9.0	9.0	9.0
				8.1	8.1	8.3	8.0	8.0
TPZH	OE	B	MAX	8.8	8.8	8.2	10.0	10.0
				9.8	9.8	8.1	10.2	10.2
TPLZ	OE	A	MAX	7.0	7.0	4.7	5.2	5.2
				5.8	5.8	4.9	5.2	5.2
TPLZ	OE	B	MAX	7.7	7.7	5.4	5.4	5.4
				7.8	7.8	6.3	7.4	7.4

UNIT: ns

## **LOW-POWER, DUAL-SUPPLY, LEVEL-TRANSLATING CompactFlash™ INTERFACE WITH 16-BIT DATA, 11-BIT ADDRESS, AND 13-BIT CONTROL LINES**

- Designed to Optimize Power Savings in Portable Applications
  - Matched Pinout with CompactFlash™ (CF) Connector Pin Configurations to Optimize PCB Layout
  - Input-Disable Feature Allows Floating Input Conditions

## Logic Diagram



NOTE:  $R_{INT} \geq 100\text{ k}\Omega$

## FUNCTION TABLES

**Lower 8-Bit Data Bus Transceivers (D07-D00, SD07-SD00)**

INPUTS			OPERATION
MASTER_EN	ENL	DIR ( $\bar{S}/CF$ )	
L	L	H	SD data to D bus
L	L	L	D data to SD bus
L	H	X	Isolation. D07-D00 and SD07-SD00 inputs can float.
H	X	X	Isolation, low power mode

X = H or L

**Upper 8-Bit Data Bus Transceivers (D15-D08, SD15-SD08)**

INPUTS			OPERATION
MASTER_EN	ENH	DIR ( $\bar{S}/CF$ )	
L	L	H	SD data to D bus
L	L	L	D data to SD bus
L	H	X	Isolation. D15-D08 and SD15-SD08 inputs can float.
H	X	X	Isolation, low power mode

X = H or L

**Address Bus Buffers**

INPUTS			OUTPUT
MASTER_EN	BUF_EN	SA	A
L	L	H	H
L	L	L	L
L	H	X	Z. SA inputs can float.
H	X	X	Z, low power mode

X = H or L

**Command Line Buffers**

(BVD1, BVD2, INPACK, OE, IORD, IOWR,  
READY, REG, CE1, CE2, WAIT, WE, WP, )

INPUTS			OUTPUT
MASTER_EN	BUF_EN	INPUT	
L	L	H	H
L	L	L	L
L	H	X	Z. Command line buffer inputs can float.
H	X	X	Z, low power mode

X = H or L

**Reset**

INPUTS		OUTPUT
MASTER_EN	SRESET	RESET
L	H	H
L	L	L
H	X	Z, low power mode

X = H or L

**DIR\_OUT**

INPUTS				OUTPUT
BUF_EN	MASTER_EN	SOE	SIORD	DIR_OUT
L	L	L	L	L
L	L	L	H	L
L	L	H	L	L
L	L	H	H	H
H	L	X	X	L
X	H	X	X	Z, low power mode

X = H or L

## ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER				MAX or MIN	LV 5V	LV 3.3V	LV 2.5V	LV 1.8V	UNIT
I <sub>CC_SD</sub>	CD1 and CD2 = V <sub>CC_SD</sub>			MAX	0.001	-	-	-	mA
	CD1 or CD2 = GND, CD1 or CD2 = V <sub>CC_SD</sub>			MAX	0.01	-	-	-	mA
I <sub>CC_S</sub> *	Inputs SD12-SD00, SA10-SA00, SCE1, SCE2, SIORD SIORWR, SOE, SREG, SWE			MAX	-	0.003	0.003	0.003	mA
	Control inputs ( ENL, ENH, BUF_EN )	V <sub>CC_S</sub>		MAX	-	0.003	0.003	0.003	mA
		GND, Other = V <sub>CC_S</sub>			-	0.036	0.036	0.036	mA
I <sub>CC_CF</sub>	Input ( D15- D00 )			MAX	-	0.003	0.003	0.003	mA
	Input ( BVD1, BVD2, INPACK, READY, WAIT, WP )	V <sub>CC_CF</sub>		MAX	-	0.003	0.003	0.003	mA
		GND, Other = V <sub>CC_CF</sub>			-	0.06	0.06	0.06	mA
I <sub>OH</sub>	Card detect			MAX	-12	-8	-4	-2	mA
I <sub>OL</sub>					12	8	4	2	mA
I <sub>OH</sub>	System port			MAX	-	12	6	2	mA
I <sub>OL</sub>					-	12	6	2	mA
I <sub>OH</sub>	CF port			MAX	16	12	-	-	mA
I <sub>OL</sub>					16	12	-	-	mA

\*I<sub>O\_SD</sub> = 0

## SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	V <sub>CC_SD</sub>	LV 5V	LV 3.3V	LV 2.5V	LV 1.8V
t <sub>PLH</sub>				5.5	5.5	6.8	9.1	15.5
t <sub>PHL</sub>	CD1 or CD2	SCD	MAX	5.5	5.5	6.8	9.1	15.5

PARAMETER	INPUT	OUTPUT	MAX or MIN	V <sub>CC_CF</sub>	LV V <sub>CC_S</sub> 3.3V	LV V <sub>CC_S</sub> 2.5V	LV V <sub>CC_S</sub> 1.8V
t <sub>PLH</sub>				3.3V	8.8	10	12.9
t <sub>PHL</sub>	CF input	S output	MAX	3.3V	8.8	10	12.9
t <sub>PLH</sub>				5V	7	8.6	13.9
t <sub>PHL</sub>	CF input	S output	MAX	5V	7	8.6	13.9
t <sub>PZH</sub>				3.3V	18.3	22.6	35.5
t <sub>PZL</sub>	MASTER_EN	S output	MAX	3.3V	18.3	22.6	35.5
t <sub>PZH</sub>				5V	18.2	22.6	35.6
t <sub>PZL</sub>	MASTER_EN	S output	MAX	5V	18.2	22.6	35.6
t <sub>PZH</sub>				3.3V	13.2	14.5	25.1
t <sub>PZL</sub>	MASTER_EN	S output	MAX	3.3V	13.2	14.5	25.1
t <sub>PZH</sub>				5V	18.2	14.5	23.3
t <sub>PZL</sub>	MASTER_EN	S output	MAX	5V	18.2	14.5	23.3
t <sub>PZH</sub>				3.3V	18.3	22.6	35.5
t <sub>PZL</sub>	BUF_EN	S output	MAX	3.3V	18.3	22.6	35.5
t <sub>PZH</sub>				5V	18.2	22.6	35.6
t <sub>PZL</sub>	BUF_EN	S output	MAX	5V	18.2	22.6	35.6
t <sub>PHZ</sub>				3.3V	12.3	14.5	24.2
t <sub>PZL</sub>	BUF_EN	S output	MAX	3.3V	12.3	14.5	24.2
t <sub>PHZ</sub>				5V	12.4	14.2	22.8
t <sub>PZL</sub>	BUF_EN	S output	MAX	5V	12.4	14.2	22.8
t <sub>PZH</sub>				3.3V	8.8	10	13.7
t <sub>PHL</sub>	D	SD	MAX	3.3V	8.8	10	13.7
t <sub>PHL</sub>				5V	7	12.4	13.9
t <sub>PZH</sub>	D	SD	MAX	5V	7	12.4	13.9
t <sub>PHL</sub>				3.3V	7.6	8.2	11.1
t <sub>PZH</sub>	SD	D	MAX	3.3V	7.6	8.2	11.1
t <sub>PHL</sub>				5V	6	7	9.6
t <sub>PHL</sub>	SD	D	MAX	5V	6	7	9.6

UNIT : ns

PARAMETER	INPUT	OUTPUT	MAX or MIN	V <sub>CC_CF</sub>	LV V <sub>CC_S</sub> 3.3V	LV V <sub>CC_S</sub> 2.5V	LV V <sub>CC_S</sub> 1.8V
tpZH	MASTER_EN	D	MAX	3.3V	21.4	23	27.9
tpZL					21.4	23	27.9
tpZH	MASTER_EN	D	MAX	5V	20.3	21.8	31
tpZL					20.3	21.8	31
tpZH	MASTER_EN	SD	MAX	3.3V	18.3	22.6	36.3
tpZL					18.3	22.6	36.3
tpZH	MASTER_EN	SD	MAX	5V	18.2	22.6	36.2
tpZL					18.2	22.6	36.2
tpHZ	MASTER_EN	D	MAX	3.3V	15	16.4	20.2
tpLZ					15	16.4	20.2
tpHZ	MASTER_EN	D	MAX	5V	12.5	13.8	17.8
tpLZ					12.5	13.8	17.8
tpHZ	MASTER_EN	SD	MAX	3.3V	12	14.5	24.2
tpLZ					12	14.5	24.2
tpHZ	MASTER_EN	SD	MAX	5V	18.2	14.2	22.8
tpLZ					18.2	14.2	22.8
tpZH	ENL or ENH	D	MAX	3.3V	21.4	22.8	27.2
tpZL					21.4	22.8	27.2
tpZH	ENL or ENH	D	MAX	5V	20.3	21.6	27.8
tpZL					20.3	21.6	27.8
tpZH	ENL or ENH	SD	MAX	3.3V	18.3	22.6	35.5
tpZL					18.3	22.6	35.5
tpZH	ENL or ENH	SD	MAX	5V	18.2	22.6	35.6
tpZL					18.2	22.6	35.6
tpHZ	ENL or ENH	D	MAX	3.3V	15	16.4	20.2
tpLZ					15	16.4	20.2
tpHZ	ENL or ENH	D	MAX	5V	12	13.1	16.6
tpLZ					12	13.1	16.6
tpHZ	ENL or ENH	SD	MAX	3.3V	12	14.5	24.2
tpLZ					12	14.5	24.2
tpHZ	ENL or ENH	SD	MAX	5V	18.2	14.2	22.8
tpLZ					18.2	14.2	22.8

UNIT : ns

# 164245

## 16-BIT TRANSCEIVER AND 3.3-V TO 5-V SHIFTER WITH 3-STATE OUTPUTS

- SN74ALVC164245:

A port has VCCA, which is set to operate at 2.5 V and 3.3 V

B port has VCCB, which is set to operate at 3.3 V and 5 V

- SN74AVCB164245, SN74AVCBH164245:

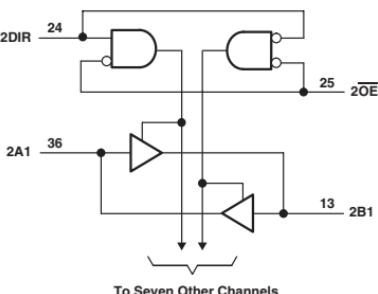
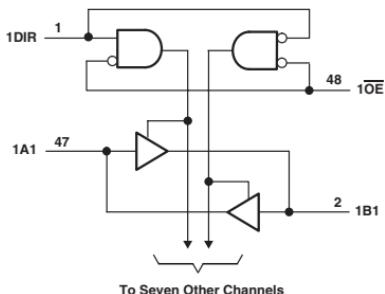
The A-port is designed to track VCCA, VCCA accepts any supply voltage from 1.4 V to 3.6 V

The B-port is designed to track VCCB, VCCB accepts any supply voltage from 1.4 V to 3.6 V

**FUNCTION TABLE**  
(each 8-bit section)

INPUTS	OPERATION		
OE	DIR		
L	L	B data to A bus	
L	H	A data to B bus	
H	X	Isolation	

**Logic Diagram**



### ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	ALVC	AVCA	AVCAH	AVCB	AVCBH	UNIT
Icc	VCCA=3.6V VCCB=5.5V	MAX	0.04	-	-	-	mA
	VCCA=2.3V VCCB=3.3V	MAX	0.02	-	-	-	mA
	VCCA=3.6V VCCB=3.6V	MAX	-	0.04	0.04	0.04	mA
	VCCA=3.6V VCCB=0V	MAX	-	-0.04	-0.04	-0.04	mA
	VCCA=0V VCCB=3.6V	MAX	-	0.04	0.04	0.04	mA
	VCCA=2.7V VCCB=2.7V	MAX	-	0.03	0.03	0.03	mA
Ioh	VCCA=1.6V VCCB=1.6V	MAX	-	0.02	0.02	0.02	mA
	VCCB=3.3V	MAX	-24	-12	-12	-12	mA
		24	12	12	12	12	mA
	VCCA=3.0V	MAX	-24	-12	-12	-12	mA
		24	12	12	12	12	mA
	VCCA=2.3V	MAX	-18	-8	-8	-8	mA
		18	8	8	8	8	mA
Iol	VCCA=1.4V	MAX	-	-2	-2	-2	mA
			-	2	2	2	mA

## SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	ALVC			
				VCCB=3.3V	VCCB=5.5V	VCCB=5.5V	VCCA=3.3V
tPLH	A	B	MAX	7.6	5.9	5.8	
				7.6	5.9	5.8	
tPHL	B	A	MAX	7.6	6.7	5.8	
				7.6	6.7	5.8	
tPZL	OE	B	MAX	11.5	9.3	8.9	
tPZH	OE	A	MAX	11.5	9.3	8.9	
tPZL	OE	B	MAX	12.3	10.2	9.1	
tPZH	OE	A	MAX	12.3	10.2	9.1	
tPLZ	OE	B	MAX	10.5	9.2	9.5	
tPHZ	OE	B	MAX	10.5	9.2	9.5	
tPLZ	OE	A	MAX	9.3	9.0	8.6	
tPHZ	OE	A	MAX	9.3	9.0	8.6	

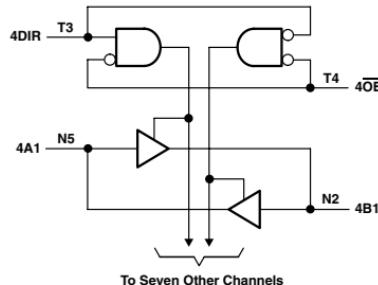
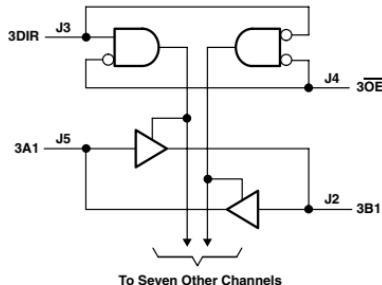
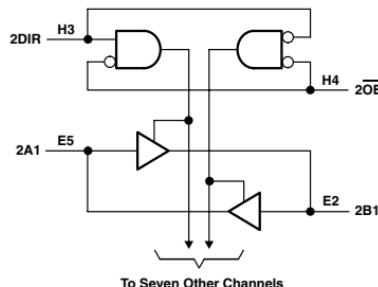
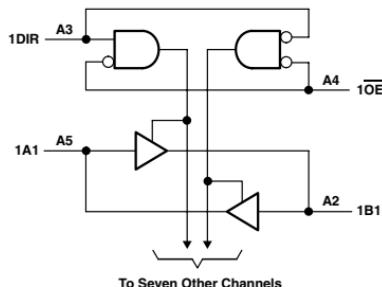
PARAMETER	INPUT	OUTPUT	MAX or MIN	AVCA/AVCAH					
				VCCA=1.4V VCCB=2.3V	VCCA=1.4V VCCB=3.6V	VCCA=2.3V VCCB=1.4V	VCCA=2.3V VCCB=3.6V	VCCA=3.6V VCCB=1.4V	VCCA=3.6V VCCB=2.3V
tPLH	A	B	MAX	5.5	5.8	6.0	3.4	5.9	3.7
				5.5	5.8	6.0	3.4	5.9	3.7
tPHL	B	A	MAX	7.6	7.3	4.6	3.7	4.5	3.3
				7.6	7.3	4.6	3.7	4.5	3.3
tPZL	OE	B	MAX	10.8	10.7	4.1	5.3	2.6	4.1
tPZH	OE	A	MAX	10.8	10.7	4.1	5.3	2.6	4.1
tPZL	OE	A	MAX	6.3	5.6	7.4	4.5	7.0	5.0
				6.3	5.6	7.4	4.5	7.0	5.0
tPZH	OE	B	MAX	6.5	6.4	4.5	3.7	5.4	3.6
tPLZ	OE	B	MAX	6.5	6.4	4.5	3.7	5.4	3.6
tPLZ	OE	A	MAX	5.3	6.1	5.7	4.0	5.4	3.3
tPHZ	OE	A	MAX	5.3	6.1	5.7	4.0	5.4	3.3

PARAMETER	INPUT	OUTPUT	MAX or MIN	AVCB/AVCBH					
				VCCA=1.4V VCCB=2.3V	VCCA=1.4V VCCB=3.6V	VCCA=2.3V VCCB=1.4V	VCCA=2.3V VCCB=3.6V	VCCA=3.6V VCCB=1.4V	VCCA=3.6V VCCB=2.3V
tPLH	A	B	MAX	5.5	5.8	6.0	3.4	5.9	3.7
				5.5	5.8	6.0	3.4	5.9	3.7
tPHL	B	A	MAX	7.6	7.3	4.6	3.7	4.5	3.3
				7.6	7.3	4.6	3.7	4.5	3.3
tPZL	OE	B	MAX	10.0	9.8	5.7	5.1	4.9	4.3
tPZH	OE	A	MAX	10.0	9.8	5.7	5.1	4.9	4.3
tPZL	OE	A	MAX	5.2	4.2	8.5	4.2	8.3	5.2
				5.2	4.2	8.5	4.2	8.3	5.2
tPZH	OE	B	MAX	5.1	4.8	5.8	3.3	6.9	3.8
tPLZ	OE	B	MAX	5.1	4.8	5.8	3.3	6.9	3.8
tPLZ	OE	A	MAX	3.6	3.0	7.0	3.0	7.0	3.5
tPHZ	OE	A	MAX	3.6	3.0	7.0	3.0	7.0	3.5

UNIT: ns

**32-BIT DUAL-SUPPLY BUS TRANSCEIVER WITH CONFIGURABLE VOLTAGE TRANSLATION AND 3-STATE OUTPUTS**

**Logic Diagram**



**FUNCTION TABLE**  
(each 8-bit section)

INPUTS		OPERATION
$\overline{OE}$	DIR	
L	L	B data to A bus
L	H	A data to B bus
H	X	Isolation

## ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	AVCB	UNIT
I <sub>CC</sub>	VCCA=3.6V VCCB=3.6V	MAX	0.08 mA
	VCCA=3.6V VCCB=0V	MAX	-0.08 mA
	VCCA=0V VCCB=3.6V	MAX	0.08 mA
	VCCA=2.7V VCCB=2.7V	MAX	0.04 mA
	VCCA=1.6V VCCB=1.6V	MAX	0.04 mA
I <sub>OH</sub>	VCCB=3.3V	MAX	-12 mA
I <sub>OL</sub>			12
I <sub>OH</sub>	VCCA=3.0V	MAX	-12 mA
I <sub>OL</sub>			12
I <sub>OH</sub>	VCCA=2.3V	MAX	-8 mA
I <sub>OL</sub>			8
I <sub>OH</sub>	VCCA=1.4V	MAX	-2 mA
I <sub>OL</sub>			2

## SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	AVCB					
				VCCA=1.4V VCCB=2.3V	VCCA=1.4V VCCB=3.6V	VCCA=2.3V VCCB=1.4V	VCCA=2.3V VCCB=3.6V	VCCA=3.6V VCCB=1.4V	VCCA=3.6V VCCB=2.3V
t <sub>PLH</sub>	A	B	MAX	5.5	5.8	6.0	3.4	5.9	3.7
				5.5	5.8	6.0	3.4	5.9	3.7
t <sub>PHL</sub>	B	A	MAX	5.9	5.9	5.4	3.7	5.8	3.3
				5.9	5.9	5.4	3.7	5.8	3.3
t <sub>PZL</sub>	OE	B	MAX	7.6	7.5	6.1	4.2	5.1	5.2
				7.6	7.5	6.1	4.2	5.1	5.2
t <sub>PZH</sub>	OE	A	MAX	10.0	9.8	5.7	5.1	4.9	4.3
				10.0	9.8	5.7	5.1	4.9	4.3
t <sub>PZL</sub>	OE	B	MAX	5.8	5.7	6.0	3.0	5.5	3.5
				5.8	5.7	6.0	3.0	5.5	3.5
t <sub>PZL</sub>	OE	A	MAX	5.1	4.8	5.8	3.3	6.9	3.8
				5.1	4.8	5.8	3.3	6.9	3.8

UNIT: ns

# **FUNCTION**

**1G / 2G / 3G**



### LITTLE LOGIC GATE (AND/NAND/OR/NOR/EX-OR)

Description	No. of Input	Circuit	Input	Output	Device	Technology				
						Advanced CMOS		Low-Voltage CMOS		Low-Power CMOS
						AHC	AHCT	LVC	AUC	AUP
POSITIVE AND	2	1			1008	●	●	●	●	●
		2			2008			●	●	
		3	1		1G11		●		●	
POSITIVE NAND	2	1			1000	●	●	●	●	●
			OD		1G38			●		
		SCH			1G132			●		
	3	2			2000		●		●	
			OD		2G38		●			
		SCH			2G132					
		3	1		1G10		●		●	
POSITIVE OR	2	1			1G32	●	●	●	●	●
		2			2G32		●	●	●	
		3	1		1G332		●			
POSITIVE NOR	2	1			1G02	●	●	●	●	●
		2			2G02		●		●	
		3	1		1G27		●			
EXCLUSIVE OR	2	1			1G86	●	●	●	●	
		2			2G86		●	●	●	
		3	1		1G386		●			
POSITIVE AND-OR	3	1			1G0632			●		
POSITIVE OR-AND	3	1			1G3208			●		

Explanatory notes [Input] SCH: Schmitt-Trigger Inputs

[Output] BUF: Buffered Output OC: Open-Collector Output 3S: 3-State Output

Status ●: Product available in technology indicated \*: New product planned in technology indicated

### LITTLE LOGIC GATE (INVERTER / NON-INVERTER)

Description	No. of Input	Circuit	Input	Output	Device	Technology				
						Advanced CMOS		Low-Voltage CMOS		Low-Power CMOS
						AHC	AHCT	LVC	AUC	AUP
INVERTING	1	1		BUF	1G04	●	●	●	●	●
				UBF	1GU04	●		●	●	
				UBF/BUF	1GX04			●		
				OC	1G06			●	●	
		2		SCH	1G14	●	●	●	●	●
				BUF	2G04			●	●	
				UBF	2GU04			●	●	
		3		OC	2G06			●	●	
				SCH	2G14			●		
				BUF	3G04			●		
				UBF	3GU04			●		
				OC	3G06			●		
				SCH	3G14			●		
NON-INVERTING	1	1		OC	1G07			●	●	●
				SCH	1G17			●	●	●
				BUF	1G34			●		●
				OC	2G07			●	●	
		2		SCH	2G17			●		
				BUF	2G34			●	●	
				OC	3G07			●		
				SCH	3G17			●		
				BUF	3G34			●		

Explanatory notes [Input] SCH: Schmitt-Trigger Inputs

[Output] BUF: Buffered Output OC: Open-Collector Output 3S: 3-State Output

Status ●: Product available in technology indicated \*: New product planned in technology indicated

### LITTLE LOGIC BUFFER/DRIVER

Description	Circuit	Output	Device	Technology				
				Advanced CMOS		Low-Voltage CMOS		Low-Power CMOS
				AHC	AHCT	LVC	AUC	AUP
NON-INVERTING	1	3S	1G125	●	●	●	●	●
		3S	1G126	●	●	●	●	●
		3S	2G125			●	●	
	2	3S	2G126			●	●	
		3S	2G241			●	●	
INVERTING	1	3S	1G240			●	●	●
	2	3S	2G240			●	●	

Explanatory notes [Output] 3S: 3-State Output R3S: Series Resistor and 3-State output OC: Open-Collector Output

Status ●: Product available in technology indicated \*: New product planned in technology indicated

### LITTLE LOGIC LATCH

Type	Circuit	PRE - CLR	Output	Q - Q̄	Device	Technology				
						Advanced CMOS		Low-Voltage CMOS		Low-Power CMOS
						AHC	AHCT	LVC	AUC	AUP
D	4		3S	Q	373			●		

Explanatory notes [Type] S-R: S-R Latch AD: Addressable Latch BIS: Bistable Latch

R-B: Read-Back Latch D: D-Type Transparent Latch

### LITTLE LOGIC D-TYPE FLIP-FLOP

Trigger	Circuit	Edge	PRE + CLR	Output	Q + Q̄	Device	Technology				
							Advanced CMOS		Low-Voltage CMOS		Low-Power CMOS
							AHC	AHCT	LVC	AUC	AUP
POS	1	S	B	2S	B	1G74			●		●
		S		2S	Q	1G79			●	●	●
		S		2S	Q̄	1G80			●	●	●
		C		2S	Q	1G175			●		
				3S	Q	1G374			●		
		S	B	2S	B	2G74			●		
		D		2S	Q	2G79			●	●	
		D		2S	Q̄	2G80			●	●	

Explanatory notes [Trigger] POS: POSITIVE EDGE, NEG: NEGATIVE EDGE

[PRE + CLR] B: Preset and Clear, C: Clear only

[Edge] S: Single Edge Triggered, D: Dual Edge Triggered

[Output] 2S: Totem pole Output 3S: 3-State Output

[Q + Q̄] B: Q + Q̄-Output Q: Q-Output Q̄: Q̄-Output

Status ●: Product available in technology indicated \*: New product planned in technology indicated

### LITTLE LOGIC DATA SELECTOR/MULTIPLEXER

No. of Input/Output	Output	Circuit	Device	Technology				
				Advanced CMOS		Low-Voltage CMOS		Low-Power CMOS
				AHC	AHCT	LVC	AUC	AUP
1/2	3S	1	1G18			●		
2/1	2S	1	2G157			●		

Explanatory notes [Output] 2S: Totem Pole Output 3S: 3-State Output OC: Open-Collector Output

Status ●: Product available in technology indicated \*: New product planned in technology indicated

### LITTLE LOGIC MONOSTABLE MULTIVIBRATOR

Circuit	CLR	Retrigger	Device	Technology				
				Advanced CMOS		Low-Voltage CMOS		Low-Power CMOS
				AHC	AHCT	LVC	AUC	AUP
1	C		1G123			●		

Explanatory notes [CLR] C: With Clear

[Retrigger] R: With Retrigger

### LITTLE LOGIC DECODER/DEMUTIPLEXER

No. of Input/Output	Output	Circuit	Type	Technology				
				Advanced CMOS		Low-Voltage CMOS		Low-Power CMOS
AHC	AHCT	LVC	AUC	AUP				
1/1	2S	1	1G119		●	●		
2/3	2S	1	1G229		●			
2/4	2S	1	1G139		●			

Explanatory notes [Output] 2S: Totem Pole Output 3S: 3-State Output OC: Open-Collector Output  
 Status ●: Product available in technology indicated \*: New product planned in technology indicated

### LITTLE LOGIC ANALOG SWITCH

Description	Type	Technology				
		Advanced CMOS		Low-Voltage CMOS		Low-Power CMOS
AHC	AHCT	LVC	AUC	AUP		
DUAL ANALOG MULTIPLEXER/DEMUTIPLEXER	1G3157		●			
DUAL ANALOG MULTIPLEXER/DEMUTIPLEXER	2G53		●	●		
SINGLE BILATERAL ANALOG SWITCH	1G66		●	●		
DUAL BILATERAL ANALOG SWITCH	2G66		●	●		

Status ●: Product available in technology indicated \*: New product planned in technology indicated

### LITTLE LOGIC MULTIFUNCTION GATE

Description	Input	Type	Technology				
			Advanced CMOS		Low-Voltage CMOS		Low-Power CMOS
AHC	AHCT	LVC	AUC	AUP			
CONFIGURABLE MULTI-FUNCTION GATE AND gate/AND with both inputs inverted NAND with inverted input OR with inverted input NOR gate / NOR with both inputs inverted XNOR	3	1G57		●			●
CONFIGURABLE MULTI-FUNCTION GATE AND with inverted input NAND gate, NAND with both inputs inverted OR gate / OR with both inputs inverted NOR with inverted input XOR gate	3	1G58		●			●
CONFIGURABLE MULTI-FUNCTION GATE 2-to-1 data selector AND gate OR gate with one inverted input NAND gate with one inverted input AND gate with one inverted input NOR gate with one inverted input OR gate Inverter Noninverted buffer	3	1G97		●			●
CONFIGURABLE MULTI-FUNCTION GATE 2-to-1 data selector with inverted output NAND gate NOR gate with one inverted input AND gate with one inverted input NAND gate with one inverted input OR gate with one inverted input NOR gate Noninverted buffer Inverter	3	1G98		●			●
ULTRA-CONFIGURABLE MULTI-FUNCTION GATE PRIMARY FUNCTION 3-state buffer 3-state inverter 3-state 2-in-1 data selector MUX 3-state 2-in-1 data selector MUX, inverted out 3-state 2-input AND 3-state 2-input AND, one input inverted 3-state 2-input AND, both inputs inverted 3-state 2-input NAND 3-state 2-input NAND, one input inverted 3-state 2-input NAND, both inputs inverted 3-state 2-input XOR 3-state 2-input XNOR COMPLEMENTARY FUNCTION 3-state 2-input NOR 3-state 2-input NOR, one input inverted 3-state 2-input NOR, both inputs inverted 3-state 2-input OR 3-state 2-input OR, one input inverted 3-state 2-input OR, both inputs inverted 3-state 2-input XOR, one input inverted	4	1G99		●			●

Status ●: Product available in technology indicated \*: New product planned in technology indicated



# **PIN ASSIGNMENTS**

**1G / 2G / 3G**

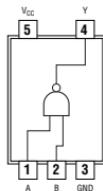


# Pin Assignments

**1G00**

SINGLE 2-INPUT POSITIVE-NAND GATE

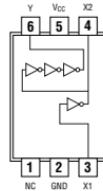
$$Y = \bar{A} \bar{B}$$



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**1GX04**

CRYSTAL OSCILLATOR DRIVER

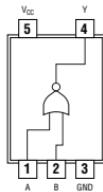


NC-No internal connection

**1G02**

SINGLE 2-INPUT POSITIVE-NOR GATE

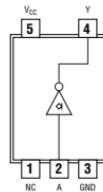
$$Y = A + B$$



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**1G06**

SINGLE INVERTER BUFFER/DRIVER  
WITH OPEN-DRAIN OUTPUT

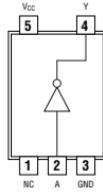


NC-No internal connection

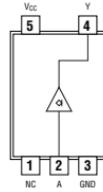
**1G04**

SINGLE INVERTER GATE

$$Y = \bar{A}$$



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NC-No internal connection

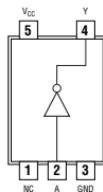
**1G07**

SINGLE BUFFER/DRIVER  
WITH OPEN-DRAIN OUTPUT

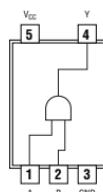
**1GU04**

SINGLE INVERTER

$$Y = \bar{A}$$



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**1G08**

SINGLE 2-INPUT POSITIVE-AND GATE

$$Y = A * B$$

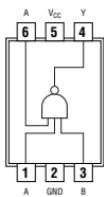
See page 95

# Pin Assignments

## 1G10

SINGLE 3-INPUT POSITIVE-NAND GATE

$$Y = A \cdot B \cdot C$$

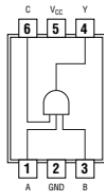


See page 95

## 1G11

SINGLE 3-INPUT POSITIVE-AND GATE

$$Y = A \cdot B \cdot C$$

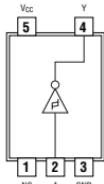


See page 96

## 1G14

SINGLE SCHMITT-TRIGGER INVERTER GATE

$$Y = \bar{A}$$



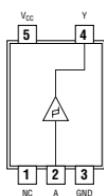
See page 96

NC-No internal connection

## 1G17

SINGLE SCHMITT-TRIGGER BUFFER

$$Y = A$$



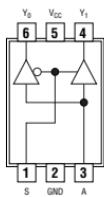
See page 97

NC-No internal connection

## 1G18

1-OF-2 NONINVERTING DEMULTIPLEXER

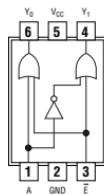
WITH 3-STATE Deselected Output



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## 1G19

1-OF-2 DECODER/DEMUTIPLEXER

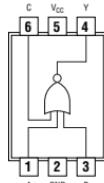


See page 98

## 1G27

3-INPUT POSITIVE-NOR GATE

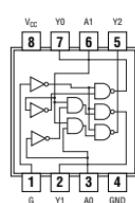
$$Y = A + B + C$$



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## 1G29

2-OF-3 DECODER/DEMUTIPLEXER



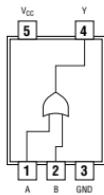
See page 99

# Pin Assignments

**1G32**

SINGLE 2-INPUT POSITIVE-OR GATE

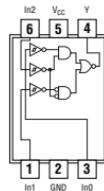
$$Y = A + B$$



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**1G58**

CONFIGURABLE MULTIPLE-FUNCTION GATE

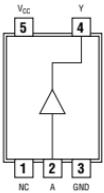


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**1G34**

SINGLE BUFFER GATE

$$Y = A$$

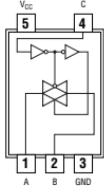


See page 100

NC-No internal connection

**1G66**

SINGLE BILATERAL ANALOG SWITCH

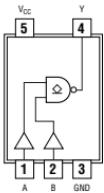


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**1G38**

SINGLE 2-INPUT NAND GATE WITH OPEN-DRAIN OUTPUT

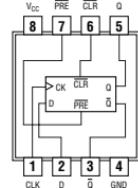
$$Y = \bar{A} \cdot \bar{B} \text{ or } Y = \bar{A} + \bar{B}$$



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**1G74**

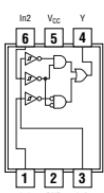
SINGLE POSITIVE-EDGE-TRIGGERED D-TYPE FLIP-FLOP WITH CLEAR AND PRESET



See page 103

**1G57**

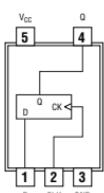
CONFIGURABLE MULTIPLE-FUNCTION GATE



See page 101

**1G79**

SINGLE POSITIVE-EDGE-TRIGGERED D-TYPE FLIP-FLOP

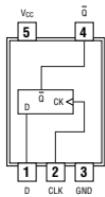


See page 104

## Pin Assignments

### **1G80**

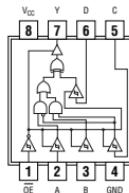
SINGLE POSITIVE-EDGE-TRIGGERED  
D-TYPE FLIP-FLOP



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### **1G99**

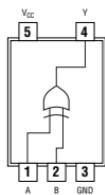
SINGLE RETRIGGERABLE MONOSTABLE MULTIVIBRATOR  
WITH SCHMITT-TRIGGER INPUTS



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### **1G86**

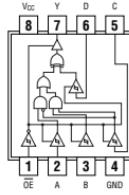
SINGLE 2-INPUT EXCLUSIVE-OR GATE  
 $Y = A \oplus B$



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### **1G123**

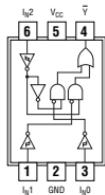
SINGLE RETRIGGERABLE MONOSTABLE MULTIVIBRATOR  
WITH SCHMITT-TRIGGER INPUTS



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### **1G97**

CONFIGURABLE MULTIPLE-FUNCTION GATE

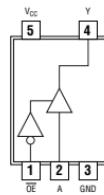


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### **1G125**

SINGLE BUS BUFFER GATE  
WITH 3-STATE OUTPUT

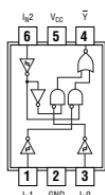
Y = A



See page 110

### **1G98**

CONFIGURABLE MULTIPLE-FUNCTION GATE

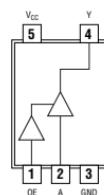


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### **1G126**

SINGLE BUS BUFFER GATE  
WITH 3-STATE OUTPUT

Y = A



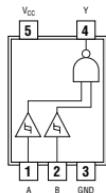
See page 110

## Pin Assignments

### **1G132**

SINGLE 2-INPUT NAND GATE WITH SCHMITT-TRIGGER INPUTS

$$Y = \overline{A} \cdot \overline{B} \text{ or } Y = \overline{A} + \overline{B}$$

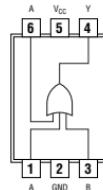


See page 111

### **1G332**

SINGLE 3-INPUT POSITIVE-OR GATE

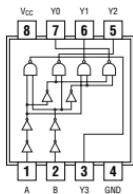
$$Y = A + B + C$$



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### **1G139**

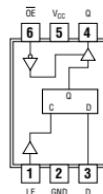
2-TO-4 LINE DECODER



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### **1G373**

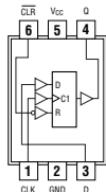
SINGLE D-TYPE LATCH WITH 3-STATE OUTPUT



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### **1G175**

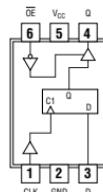
SINGLE D-TYPE FLIP-FLOP WITH ASYNCHRONOUS CLEAR



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### **1G374**

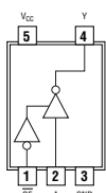
SINGLE D-TYPE FLIP-FLOP WITH 3-STATE OUTPUT



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### **1G240**

SINGLE BUFFER/DRIVER WITH 3-STATE OUTPUT

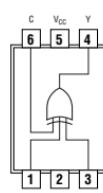


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### **1G386**

SINGLE 3-INPUT EXCLUSIVE-XOR GATE

$$Y = A = B = C$$



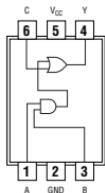
See page 117

## Pin Assignments

**1G0832**

SINGLE 3-INPUT POSITIVE AND-OR GATE

$$Y = (A \bullet B) + C$$

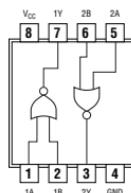


See page 117

**2G02**

DUAL 2-INPUT POSITIVE-NOR GATE

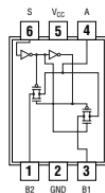
$$Y = \bar{A} + \bar{B}$$



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**1G3157**

SINGLE-POLE, DOUBLE-THROW ANALOG SWITCH

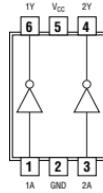


See page 118

**2G04**

DUAL INVERTER GATE

$$Y = \bar{A}$$

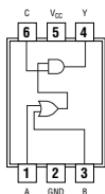


See page 121

**1G3208**

SINGLE 3-INPUT POSITIVE OR-AND GATE

$$Y = (A + B) \bullet C$$

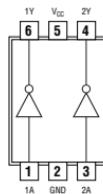


See page 119

**2GU04**

DUAL INVERTER GATE

$$Y = \bar{A}$$

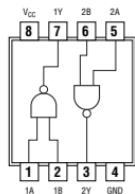


See page 121

**2G00**

DUAL 2-INPUT POSITIVE-NAND GATE

$$Y = \bar{A} \bullet \bar{B}$$

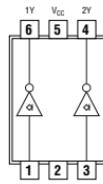


See page 120

**2G06**

DUAL INVERTER BUFFER/DRIVER

WITH OPEN-DRAIN OUTPUTS

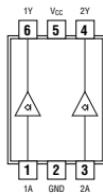


See page 122

## Pin Assignments

**2G07**

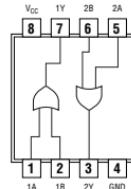
DUAL BUFFER/DRIVER  
WITH OPEN-DRAIN OUTPUTS



See page 122

**2G32**

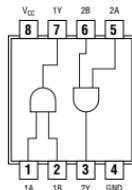
DUAL 2-INPUT POSITIVE-OR GATE  
 $Y = A + B$



See page 124

**2G08**

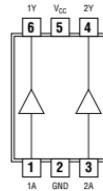
DUAL 2-INPUT POSITIVE-AND GATE  
 $Y = A \cdot B$



See page 123

**2G34**

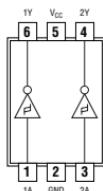
DUAL INVERTER GATE  
 $Y = A$



See page 125

**2G14**

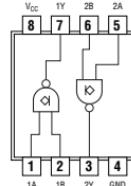
DUAL INVERTER GATE  
 $Y = \bar{A}$



See page 123

**2G38**

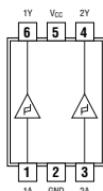
SINGLE 2-INPUT NAND GATE WITH OPEN-DRAIN OUTPUT  
 $Y = A \cdot B$  or  $Y = \bar{A} + \bar{B}$



See page 125

**2G17**

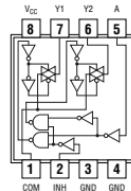
DUAL SCHMITT-TRIGGER BUFFER  
 $Y = A$



See page 124

**2G53**

SINGLE-POLE DOUBLE-THROW (SPDT) ANALOG SWITCH OR  
2:1 ANALOG MULTIPLEXER/DEMULTIPLEXER

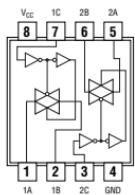


See page 126

# Pin Assignments

## 2G66

DUAL BILATERAL ANALOG SWITCH

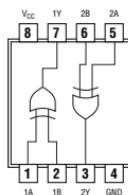


See page 126

## 2G86

DUAL 2-INPUT EXCLUSIVE-OR GATE

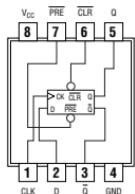
$$Y = A \oplus B$$



See page 130

## 2G74

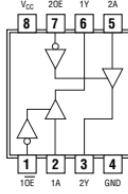
SINGLE POSITIVE-EDGE-TRIGGERED D-TYPE FLIP-FLOP WITH CLEAR AND PRESET



See page 127

## 2G125

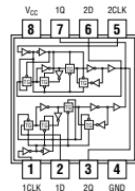
DUAL BUS BUFFER GATE WITH 3-STATE OUTPUTS



See page 130

## 2G79

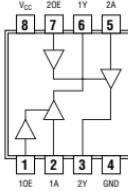
DUAL POSITIVE-EDGE-TRIGGERED D-TYPE FLIP-FLOP



See page 128

## 2G126

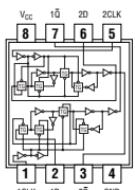
DUAL BUS BUFFER GATE WITH 3-STATE OUTPUTS



See page 131

## 2G80

DUAL POSITIVE-EDGE-TRIGGERED D-TYPE FLIP-FLOP

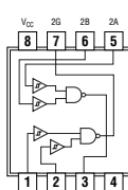


See page 129

## 2G132

SINGLE 2-INPUT NAND GATE WITH OPEN-DRAIN OUTPUT

$$Y = \overline{A} \cdot \overline{B} \text{ or } Y = \overline{A} + \overline{B}$$

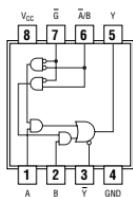


See page 131

# Pin Assignments

## 2G157

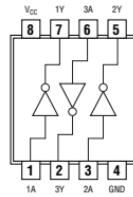
SINGLE 2-LINE TO 1-LINE DATA  
SELECTOR/MULTIPLEXER



See page 132

## 3GU04

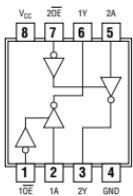
TRIPLE INVERTER GATE  
 $Y = \bar{A}$



See page 134

## 2G240

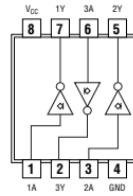
DUAL BUFFERS/DRIVERS WITH 3-STATE OUTPUTS



See page 133

## 3G06

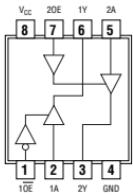
TRIPLE INVERTER BUFFER/DRIVER  
WITH OPEN-DRAIN OUTPUTS



See page 135

## 2G241

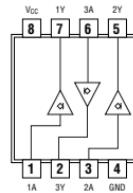
DUAL BUFFER/DRIVER WITH 3-STATE OUTPUTS



See page 133

## 3G07

TRIPLE BUFFER/DRIVER  
WITH OPEN-DRAIN OUTPUTS

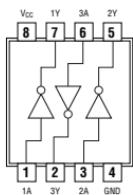


See page 135

## 3G04

TRIPLE INVERTER GATE

$Y = \bar{A}$

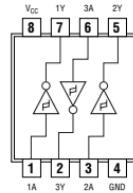


See page 134

## 3G14

TRIPLE SCHMITT-TRIGGER INVERTER

$Y = \bar{A}$



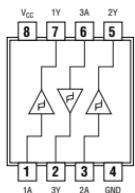
See page 136

## Pin Assignments

**3G17**

TRIPLE SCHMITT-TRIGGER BUFFER

Y = A

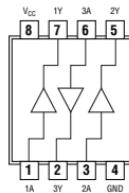


See page 136

**3G34**

TRIPLE BUFFER GATE

Y = A



See page 137

# **FUNCTION AND ELECTRICAL CHARACTERISTICS**

**1G / 2G / 3G**



# 1G00

## SINGLE 2-INPUT POSITIVE-NAND GATE

$$\bullet Y = \overline{A \cdot B}$$

**Logic Diagram****FUNCTION TABLE**

INPUTS		OUTPUT
A	B	Y
H	H	L
L	X	H
X	L	H

**ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS**

PARAMETER	MAX or MIN	AHC	AHCT	LVC 5V	LVC 3.3V	LVC 2.5V	LVC 1.8V	AUC 2.5V	AUC 1.8V	AUP 3.3V	AUP 2.5V	AUP 1.8V	AUP 1.1V	UNIT
I <sub>CC</sub>	MAX	0.01	0.01	0.01	0.01	0.01	0.01	0.01	0.01	0.0009	0.0009	0.0009	0.0009	mA
I <sub>OH</sub>	MAX	-8	-8	-32	-24	-8	-4	-9	-8	-4	-3.1	-1.9	-1.1	mA
I <sub>OL</sub>	MAX	8	8	32	24	8	4	9	8	4	3.1	1.9	1.1	mA

**SWITCHING CHARACTERISTICS**

PARAMETER	INPUT	OUTPUT	MAX or MIN	AHC	AHCT	LVC 5V	LVC 3.3V	LVC 2.5V	LVC 1.8V	AUC 2.5V	AUC 1.8V	AUP 3.3V	AUP 2.5V	AUP 1.8V	AUP 1.1V
I <sub>PLH</sub>	A or B	Y	MAX	8.5	9	4	4.7	5.5	9	2	2.2	5.2	6.8	9.8	18.8
I <sub>PHL</sub>				8.5	9	4	4.7	5.5	9	2	2.2	5.2	6.8	9.8	18.8

UNIT:ns

# 1G02

## SINGLE 2-INPUT POSITIVE-NOR GATE

$$\bullet Y = \overline{A + B}$$

**Logic Diagram (positive logic)****FUNCTION TABLE**

INPUTS		OUTPUT
A	B	Y
H	X	L
X	H	L
L	L	H

**ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS**

PARAMETER	MAX or MIN	AHC	AHCT	LVC 5V	LVC 3.3V	LVC 2.5V	LVC 1.8V	AUC 2.5V	AUC 1.8V	AUP 3.3V	AUP 2.5V	AUP 1.8V	AUP 1.1V	UNIT
I <sub>CC</sub>	MAX	0.01	0.01	0.01	0.01	0.01	0.01	0.01	0.01	0.0009	0.0009	0.0009	0.0009	mA
I <sub>OH</sub>	MAX	-8	-8	-32	-24	-8	-4	-9	-8	-4	-3.1	-1.9	-1.1	mA
I <sub>OL</sub>	MAX	8	8	32	24	8	4	9	8	4	3.1	1.9	1.1	mA

**SWITCHING CHARACTERISTICS**

PARAMETER	INPUT	OUTPUT	MAX or MIN	AHC	AHCT	LVC 5V	LVC 3.3V	LVC 2.5V	LVC 1.8V	AUC 2.5V	AUC 1.8V	AUP 3.3V	AUP 2.5V	AUP 1.8V	AUP 1.1V
I <sub>PLH</sub>	A or B	Y	MAX	8.5	9	4	4.5	5.5	8	2.1	2.4	5	6.5	9.5	17.9
I <sub>PHL</sub>				8.5	9	4	4.5	5.5	8	2.1	2.4	5	6.5	9.5	17.9

UNIT:ns

# 1G04

## SINGLE INVERTER GATE

- $Y = \bar{A}$

### FUNCTION TABLE

INPUT A	OUTPUT Y
H	L
L	H

### Logic Diagram

5pin Package



4pin Package



### ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	AHC	AHCT	LVC 5V	LVC 3.3V	LVC 2.5V	LVC 1.8V	AUC 2.5V	AUC 1.8V	AUP 3.3V	AUP 2.5V	AUP 1.8V	AUP 1.1V	UNIT
$I_{CC}$	MAX	0.01	0.01	0.01	0.01	0.01	0.01	0.01	0.01	0.0009	0.0009	0.0009	0.0009	mA
$I_{OH}$	MAX	-8	-8	-32	-24	-8	-4	-9	-8	-4	-3.1	-1.9	-1.1	mA
$I_{OL}$	MAX	8	8	32	24	8	4	9	8	4	3.1	1.9	1.1	mA

### SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	AHC	AHCT	LVC 5V	LVC 3.3V	LVC 2.5V	LVC 1.8V	AUC 2.5V	AUC 1.8V	AUP 3.3V	AUP 2.5V	AUP 1.8V	AUP 1.1V
$t_{PLH}$	A	Y	MAX	8.5	8.5	3.7	4.2	5.2	7.5	1.9	2.2	4.5	5.6	7.9	15
$t_{PHL}$				8.5	8.5	3.7	4.2	5.2	7.5	1.9	2.2	4.5	5.6	7.9	15

UNIT:ns

# 1GU04

## SINGLE INVERTER GATE

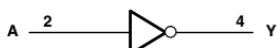
- $Y = \bar{A}$
- Unbuffered Output
- Supply Voltage Range : 2V to 5.5V

### FUNCTION TABLE

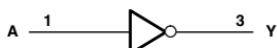
INPUT A	OUTPUT Y
H	L
L	H

### Logic Diagram

5pin Package



4pin Package



### ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	AHC	LVC 5V	LVC 3.3V	LVC 2.5V	LVC 1.8V	AUC 2.5V	AUC 1.8V	UNIT
$I_{CC}$	MAX	0.01	0.01	0.01	0.01	0.01	0.01	0.01	mA
$I_{OH}$	MAX	-8	-32	-24	-8	-4	-9	-8	mA
$I_{OL}$	MAX	8	32	24	8	4	9	8	mA

### SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	AHC	LVC 5V	LVC 3.3V	LVC 2.5V	LVC 1.8V	AUC 2.5V	AUC 1.8V
$t_{PLH}$	A	Y	MAX	8	3	3.7	4	5	2.1	2.4
$t_{PHL}$				8	3	3.7	4	5	2.1	2.4

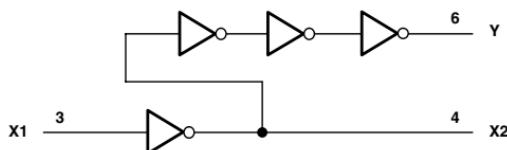
UNIT:ns

# 1GX04

## CRYSTAL OSCILLATOR DRIVER

- One Unbuffered Inverter (1GU04)
- One Buffered Inverter (1G04)
- Suitable for Commonly Used Clock Frequencies
- Optimized for Use in Crystal Oscillator Applications

**Logic Diagram**



### FUNCTION TABLE

OUTPUT	INPUTS	
X1	X2	Y
H	L	H
L	H	L

### ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	LVC 5V	LVC 3.3V	LVC 2.5V	LVC 1.8V	UNIT
I <sub>CC</sub>	MAX	0.01	0.01	0.01	0.01	mA
I <sub>OH</sub>	MAX	-32	-24	-8	-4	mA
I <sub>OL</sub>	MAX	32	24	8	4	mA

### SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	LVC 5V	LVC 3.3V	LVC 2.5V	LVC 1.8V
t <sub>PLH</sub>	X1	X2	MAX	3	3.7	4	7
t <sub>PHL</sub>				3	3.7	4	7
t <sub>PLH</sub>	X1	Y+	MAX	5	7.8	7.4	18
t <sub>PHL</sub>				5	7.8	7.4	18

UNIT : ns

\*X2 : no external load

# 1G06

## SINGLE INVERTER BUFFER/DRIVER WITH OPEN-DRAIN OUTPUT

### Logic Diagram

5pin Package



4pin Package



### FUNCTION TABLE

INPUT A	OUTPUT Y
H	L
L	H

### ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	LVC 5V	LVC 3.3V	LVC 2.5V	LVC 1.8V	AUC 2.5V	AUC 1.8V	AUP 3.3V	AUP 2.5V	AUP 1.8V	AUP 1.1V	UNIT
I <sub>CC</sub>	MAX	0.01	0.01	0.01	0.01	0.01	0.01	0.0009	0.0009	0.0009	0.0009	mA
V <sub>O</sub>	MAX	5.5	5.5	5.5	5.5	3.6	3.6	3.6	3.6	3.6	3.6	V
I <sub>OL</sub>	MAX	32	24	8	4	9	8	4	3.1	1.9	1.1	mA

### SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	LVC 5V	LVC 3.3V	LVC 2.5V	LVC 1.8V	AUC 2.5V	AUC 1.8V	AUP 3.3V	AUP 2.5V	AUP 1.8V	AUP 1.1V
t <sub>PLH</sub>	A	Y	MAX	3	4	4	6.5	1.8	2.5	4.9	4.5	6.7	14.1
t <sub>PHL</sub>				3	4	4	6.5	1.8	2.5	4.9	4.5	6.7	14.1

UNIT:ns

# 1G07

## SINGLE BUFFER/DRIVER WITH OPEN-DRAIN OUTPUT

### Logic Diagram

5pin Package



4pin Package



### FUNCTION TABLE

INPUT A	OUTPUT Y
H	H
L	L

### ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	LVC 5V	LVC 3.3V	LVC 2.5V	LVC 1.8V	AUC 2.5V	AUC 1.8V	AUP 3.3V	AUP 2.5V	AUP 1.8V	AUP 1.1V	UNIT
I <sub>CC</sub>	MAX	0.01	0.01	0.01	0.01	0.01	0.01	0.0009	0.0009	0.0009	0.0009	mA
I <sub>OH</sub>	MAX	5.5	5.5	5.5	5.5	3.6	3.6	3.6	3.6	3.6	3.6	V
I <sub>OL</sub>	MAX	32	24	8	4	9	8	4	3.1	1.9	1.1	mA

### SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	LVC 5V	LVC 3.3V	LVC 2.5V	LVC 1.8V	AUC 2.5V	AUC 1.8V	AUP 3.3V	AUP 2.5V	AUP 1.8V	AUP 1.1V
t <sub>PLH</sub>	A	Y	MAX	3.5	4.2	5.5	8.3	1.8	2.5	4.5	4.8	7.1	16.2
t <sub>PHL</sub>				3.5	4.2	5.5	8.3	1.8	2.5	4.5	4.8	7.1	16.2

UNIT:ns

# 1G08

## SINGLE 2-INPUT POSITIVE-AND GATE

$$\bullet Y = A \cdot B$$

### Logic Diagram



### FUNCTION TABLE

INPUTS		OUTPUT
A	B	Y
H	H	H
L	X	L
X	L	L

### ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	AHC	AHCT	LVC 5V	LVC 3.3V	LVC 2.5V	LVC 1.8V	AUC 2.5V	AUC 1.8V	AUP 3.3V	AUP 2.5V	AUP 1.8V	AUP 1.1V	UNIT
I <sub>CC</sub>	MAX	0.01	0.01	0.01	0.01	0.01	0.01	0.01	0.01	0.0009	0.0009	0.0009	0.0009	mA
I <sub>OH</sub>	MAX	-8	-8	-32	-24	-8	-4	-9	-8	-4	-3.1	-1.9	-1.1	mA
I <sub>OL</sub>	MAX	8	8	32	24	8	4	9	8	4	3.1	1.9	1.1	mA

### SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	AHC	AHCT	LVC 5V	LVC 3.3V	LVC 2.5V	LVC 1.8V	AUC 2.5V	AUC 1.8V	AUP 3.3V	AUP 2.5V	AUP 1.8V	AUP 1.1V
I <sub>PLH</sub>	A or B	Y	MAX	9	9	4	4.5	5.5	8	2	2.4	4.7	6.1	9	17.2
I <sub>PHL</sub>				9	9	4	4.5	5.5	8	2	2.4	4.7	6.1	9	17.2

UNIT:ns

# 1G10

## SINGLE 3-INPUT POSITIVE-NAND GATE

$$\bullet Y = \overline{A \cdot B \cdot C}$$

### Logic Diagram



### FUNCTION TABLE

INPUTS			OUTPUT
A	B	C	Y
H	H	H	L
L	X	X	H
X	L	X	H
X	X	L	H

### ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	LVC 5V	LVC 3.3V	LVC 2.5V	LVC 1.8V	AUC 2.5V	AUC 1.8V	UNIT
I <sub>CC</sub>	MAX	0.01	0.01	0.01	0.01	0.01	0.01	mA
I <sub>OH</sub>	MAX	-32	-24	-8	-4	-9	-8	mA
I <sub>OL</sub>	MAX	32	24	8	4	9	8	mA

### SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	LVC 5V	LVC 3.3V	LVC 2.5V	LVC 1.8V	AUC 2.5V	AUC 1.8V
I <sub>PLH</sub>	A, B or C	Y	MAX	3.6	5.0	6.5	18.0	TBD	TBD
I <sub>PHL</sub>				3.6	5.0	6.5	18.0	TBD	TBD

UNIT:ns

# 1G11

## Logic Diagram

### SINGLE 3-INPUT POSITIVE-AND GATE

- $Y = A \cdot B \cdot C$



#### FUNCTION TABLE

INPUTS			OUTPUT
A	B	C	Y
H	H	H	H
L	X	X	L
X	L	X	L
X	X	L	L

#### ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	LVC 5V	LVC 3.3V	LVC 2.5V	LVC 1.8V	AUC 2.5V	AUC 1.8V	UNIT
$I_{CC}$	MAX	0.01	0.01	0.01	0.01	0.01	0.01	mA
$I_{OH}$	MAX	-32	-24	-8	-4	-9	-8	mA
$I_{OL}$	MAX	32	24	8	4	9	8	mA

#### SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	LVC 5V	LVC 3.3V	LVC 2.5V	LVC 1.8V	AUC 2.5V	AUC 1.8V
$t_{PLH}$	A, B or C	Y	MAX	3.5	4.9	6.2	17.2	TBD	TBD
$t_{PHL}$				3.5	4.9	6.2	17.2	TBD	TBD

UNIT:ns

# 1G14

## Logic Diagram

### SINGLE SCHMITT-TRIGGER INVERTER GATE

- $Y = \overline{A}$



#### FUNCTION TABLE

INPUT A	OUTPUT Y
H	L
L	H

#### ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	AHC	AHCT	LVC 5V	LVC 3.3V	LVC 2.5V	LVC 1.8V	AUC 2.5V	AUC 1.8V	AUP 3.3V	AUP 2.5V	AUP 1.8V	AUP 1.1V	UNIT
$I_{CC}$	MAX	0.01	0.01	0.01	0.01	0.01	0.01	0.01	0.01	0.0009	0.0009	0.0009	0.0009	mA
$I_{OH}$	MAX	-8	-8	-32	-24	-8	-4	-9	-8	-4	-3.1	-1.9	-1.1	mA
$I_{OL}$	MAX	8	8	32	24	8	4	9	8	4	3.1	1.9	1.1	mA

#### SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	AHC	AHCT	LVC 5V	LVC 3.3V	LVC 2.5V	LVC 1.8V	AUC 2.5V	AUC 1.8V	AUP 3.3V	AUP 2.5V	AUP 1.8V	AUP 1.1V
$t_{PLH}$	A	Y	MAX	12	9	5	5.5	6.5	11	2.5	2.5	5.6	6.8	9.5	16.7
$t_{PHL}$				12	9	5	5.5	6.5	11	2.5	2.5	5.6	6.8	9.5	16.7

UNIT:ns

## 1G17

### SINGLE SCHMITT-TRIGGER BUFFER

● Y = A

#### Logic Diagram

5pin Package



4pin Package



#### FUNCTION TABLE

INPUT A	OUTPUT Y
H	H
L	L

#### ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	LVC 5V	LVC 3.3V	LVC 2.5V	LVC 1.8V	AUC 2.5V	AUC 1.8V	AUP 3.3V	AUP 2.5V	AUP 1.8V	AUP 1.1V	UNIT
I <sub>CC</sub>	MAX	0.01	0.01	0.01	0.01	0.01	0.01	0.0009	0.0009	0.0009	0.0009	mA
I <sub>OH</sub>	MAX	-32	-24	-8	-4	-9	-8	-4	-3.1	-1.9	-1.1	mA
I <sub>OL</sub>	MAX	32	24	8	4	9	8	4	3.1	1.9	1.1	mA

#### SWITCHING CHARACTERISTICS

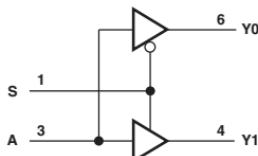
PARAMETER	INPUT	OUTPUT	MAX or MIN	LVC 5V	LVC 3.3V	LVC 2.5V	LVC 1.8V	AUC 2.5V	AUC 1.8V	AUP 3.3V	AUP 2.5V	AUP 1.8V	AUP 1.1V
I <sub>PLH</sub>	A	Y	MAX	5	5.5	6.5	11	2.5	2.4	5.7	6.8	9	15.6
I <sub>PHL</sub>				5	5.5	6.5	11	2.5	2.4	5.7	6.8	9	15.6

UNIT:ns

## 1G18

### 1-OF-2 NONINVERTING DEMULTIPLEXER WITH 3-STATE DESELECTED OUTPUT

#### Logic Diagram



#### FUNCTION TABLE

INPUTS S A	OUTPUTS Y0 Y1
L L	L Z
L H	H Z
H L	Z L
H H	Z H

#### ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	LVC 5V	LVC 3.3V	LVC 2.5V	LVC 1.8V	UNIT
I <sub>CC</sub>	MAX	0.01	0.01	0.01	0.01	mA
I <sub>OH</sub>	MAX	-32	-24	-8	-4	mA
I <sub>OL</sub>	MAX	32	24	8	4	mA

#### SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	LVC 5V	LVC 3.3V	LVC 2.5V	LVC 1.8V
I <sub>PLH</sub>	A	Y	MAX	3.2	4.2	5	9.3
I <sub>PHL</sub>				3.2	4.2	5	9.3
I <sub>PZL</sub>	S	Y	MAX	3.4	4.6	5.6	10.2
I <sub>PZH</sub>				3.4	4.6	5.6	10.2
I <sub>PZL</sub>	S	Y	MAX	3.3	4.9	5.3	12.7
I <sub>PZH</sub>				3.3	4.9	5.3	12.7

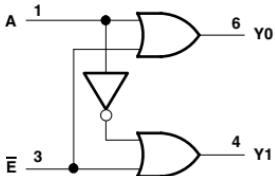
UNIT:ns

# 1G19

## 1-OF-2 DECODER/DEMULTIPLEXER

**FUNCTION TABLE**

INPUTS		OUTPUTS	
E	A	Y0	Y1
L	L	L	H
L	H	H	L
H	X	H	H

**Logic Diagram****ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS**

PARAMETER	MAX or MIN	LVC 5V	LVC 3.3V	LVC 2.5V	LVC 1.8V	UNIT	AUC 2.5V	AUC 1.8V
Icc	MAX	0.01	0.01	0.01	0.01	mA	0.01	0.01
IoH	MAX	-32	-24	-8	-4	mA	-9	-8
IoL	MAX	32	24	8	4	mA	9	8

**SWITCHING CHARACTERISTICS**

PARAMETER	INPUT	OUTPUT	MAX or MIN	LVC 5V	LVC 3.3V	LVC 2.5V	LVC 1.8V	AUC 2.5V	AUC 1.8V
tPLH	A or E	Y	MAX	3.9	5.2	6.5	16.1	2.0	2.8
tPHL				3.9	5.2	6.5	16.1	2.0	2.8

UNIT:ns

# 1G27

## SINGLE 3-INPUT POSITIVE-NOR GATE

$$\bullet \quad Y = \overline{A + B + C}$$

**Logic Diagram****FUNCTION TABLE**

INPUTS			OUTPUT
A	B	C	Y
H	X	X	L
X	H	X	L
X	X	H	L
L	L	L	H

**ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS**

PARAMETER	MAX or MIN	LVC 5V	LVC 3.3V	LVC 2.5V	LVC 1.8V	UNIT
Icc	MAX	0.01	0.01	0.01	0.01	mA
IoH	MAX	-32	-24	-8	-4	mA
IoL	MAX	32	24	8	4	mA

**SWITCHING CHARACTERISTICS**

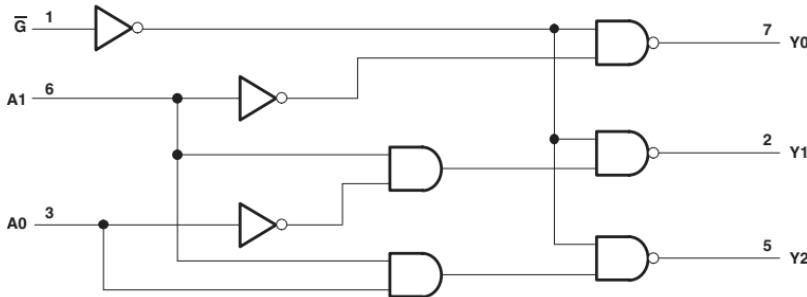
PARAMETER	INPUT	OUTPUT	MAX or MIN	LVC 5V	LVC 3.3V	LVC 2.5V	LVC 1.8V
tPLH	A, B or C	Y	MAX	3.6	5.4	7.1	20.5
tPHL				3.6	5.4	7.1	20.5

UNIT:ns

1G29

## **2-OF-3 DECODER/DEMULTIPLEXER**

## Logic Diagram



## FUNCTION TABLE

INPUTS			OUTPUTS		
<u>G</u>	A1	A0	Y0	Y1	Y2
L	L	X	L	H	H
L	H	L	H	L	H
L	H	H	H	H	L
H	X	X	H	H	H

## ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	LVC 5V	LVC 3.3V	LVC 2.5V	LVC 1.8V	UNIT
$I_{CC}$	MAX	0.01	0.01	0.01	0.01	mA
$I_{OH}$	MAX	-32	-24	-8	-4	mA
$I_{OL}$	MAX	32	24	8	4	mA

## SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	LVC 5V	LVC 3.3V	LVC 2.5V	LVC 1.8V
$t_{PLH}$	A or G	Y	MAX	5.1	6.1	7.5	15.8
$t_{PHL}$				5.1	6.1	7.5	15.8

UNIT : ns

## 1G32

### SINGLE 2-INPUT POSITIVE-OR GATE

- $\bullet Y = A + B$

**Logic Diagram****FUNCTION TABLE**

INPUTS	OUTPUT	
A	B	Y
H	X	H
X	H	H
L	L	L

**ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS**

PARAMETER	MAX or MIN	AHC	AHCT	LVC 5V	LVC 3.3V	LVC 2.5V	LVC 1.8V	AUC 2.5V	AUC 1.8V	AUP 3.3V	AUP 2.5V	AUP 1.8V	AUP 1.1V	UNIT
$I_{CC}$	MAX	0.01	0.01	0.01	0.01	0.01	0.01	0.01	0.01	0.0009	0.0009	0.0009	0.0009	mA
$I_{OH}$	MAX	-8	-8	-32	-24	-8	-4	-9	-8	-4	-3.1	-1.9	-1.1	mA
$I_{OL}$	MAX	8	8	32	24	8	4	9	8	4	3.1	1.9	1.1	mA

**SWITCHING CHARACTERISTICS**

PARAMETER	INPUT	OUTPUT	MAX or MIN	AHC	AHCT	LVC 5V	LVC 3.3V	LVC 2.5V	LVC 1.8V	AUC 2.5V	AUC 1.8V	AUP 3.3V	AUP 2.5V	AUP 1.8V	AUP 1.1V
$t_{PLH}$	A or B	Y	MAX	8.5	9	4	4.5	5.5	8	2.1	2.4	5	6.6	9.6	18.4
$t_{PHL}$				8.5	9	4	4.5	5.5	8	2.1	2.4	5	6.6	9.6	18.4

UNIT:ns

## 1G34

### SINGLE BUFFER GATE

- $\bullet Y = A$

**Logic Diagram****FUNCTION TABLE**

INPUT	OUTPUT
A	Y
H	H
L	L

**ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS**

PARAMETER	MAX or MIN	LVC 5V	LVC 3.3V	LVC 2.5V	LVC 1.8V	AUP 3.3V	AUP 2.5V	AUP 1.8V	AUP 1.1V	UNIT
$I_{CC}$	MAX	0.001	0.001	0.001	0.001	0.009	0.009	0.009	0.009	mA
$I_{OH}$	MAX	-32	-24	-8	-4	-4	-3.1	-1.9	-1.1	mA
$I_{OL}$	MAX	32	24	8	4	4	3.1	1.9	1.1	mA

**SWITCHING CHARACTERISTICS**

PARAMETER	INPUT	OUTPUT	MAX or MIN	LVC 5V	LVC 3.3V	LVC 2.5V	LVC 1.8V	AUP 3.3V	AUP 2.5V	AUP 1.8V	AUP 1.1V
$t_{PLH}$	A	Y	MAX	3.2	4.1	4.4	8.6	4.8	5.8	8.3	15.4
$t_{PHL}$				3.2	4.1	4.4	8.6	4.8	5.8	8.3	15.4

UNIT : ns

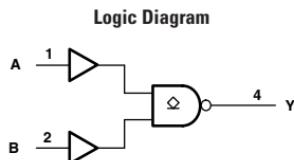
# 1G38

## SINGLE 2-INPUT NAND GATE WITH OPEN-DRAIN OUTPUT

- $Y = \overline{A} \cdot \overline{B}$  or  $Y = \overline{A} + \overline{B}$

### FUNCTION TABLE

INPUTS	A	B	OUTPUT	Y
L	L	H		H
L	H	H		H
H	L	H		H
H	H	L		L



### ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	LVC 5V	LVC 3.3V	LVC 2.5V	LVC 1.8V	UNIT
I <sub>CC</sub>	MAX	0.01	0.01	0.01	0.01	mA
V <sub>O</sub>	MAX	5.5	5.5	5.5	5.5	mA
I <sub>OL</sub>	MAX	32	24	8	4	mA

### SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	LVC 5V	LVC 3.3V	LVC 2.5V	LVC 1.8V
t <sub>PLH</sub>	A or B	Y	MAX	3.9	4.5	6	10
t <sub>PHL</sub>				3.9	4.5	6	10

UNIT : ns

# 1G57

## CONFIGURABLE MULTIPLE-FUNCTION GATE

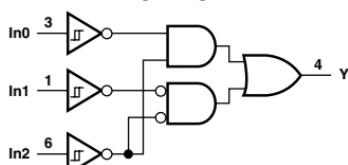
### FUNCTION SELECTION TABLE

2-input AND
2-input AND with both inputs inverted
2-input NAND with inverted input
2-input OR with inverted input
2-input NOR
2-input NOR with both inputs inverted
2-input XNOR

### FUNCTION TABLE

INPUTS	In2	In1	In0	OUTPUT	Y
L	L	L	L		H
L	L	H	H		L
L	H	L	L		H
L	H	H	H		L
H	L	L	L		L
H	L	H	H		L
H	H	L	L		H
H	H	H	H		H

### Logic Diagram



### ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	LVC 5V	LVC 3.3V	LVC 2.5V	LVC 1.8V	AUP 3.3V	AUP 2.5V	AUP 1.8V	AUP 1.1V	UNIT
I <sub>CC</sub>	MAX	0.01	0.01	0.01	0.01	0.0009	0.0009	0.0009	0.0009	mA
I <sub>OH</sub>	MAX	-32	-24	-8	-4	-4	-3.1	-1.9	-1.1	mA
I <sub>OL</sub>	MAX	32	24	8	4	4	3.1	1.9	1.1	mA

### SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	LVC 5V	LVC 3.3V	LVC 2.5V	LVC 1.8V	AUP 3.3V	AUP 2.5V	AUP 1.8V	AUP 1.1V
t <sub>PLH</sub>	Any In	Y	MAX	5.1	6.3	8.3	14.4	6.1	7.3	10	18.1
t <sub>PHL</sub>				5.1	6.3	8.3	14.4	6.1	7.3	10	18.1

UNIT:ns

# 1G58

## CONFIGURABLE MULTIPLE-FUNCTION GATE

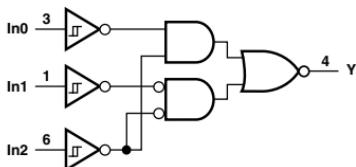
### FUNCTION SELECTION TABLE

2-input AND with inverted input
2-input NAND
2-input NAND with both inputs inverted
2-input OR
2-input OR with both inputs inverted
2-input NOR with inverted input
2-input XOR

### FUNCTION TABLE

INPUTS			OUTPUT Y
In2	In1	In0	
L	L	L	L
L	L	H	H
L	H	L	L
L	H	H	H
H	L	L	H
H	L	H	H
H	H	L	L
H	H	H	L

### Logic Diagram



### ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	LVC 5V	LVC 3.3V	LVC 2.5V	LVC 1.8V	AUP 3.3V	AUP 2.5V	AUP 1.8V	AUP 1.1V	UNIT
I <sub>CC</sub>	MAX	0.01	0.01	0.01	0.0009	0.0009	0.0009	0.0009	0.0009	mA
I <sub>OH</sub>	MAX	-32	-24	-8	-4	-4	-3.1	-1.9	-1.1	mA
I <sub>OL</sub>	MAX	32	24	8	4	4	3.1	1.9	1.1	mA

### SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	LVC 5V	LVC 3.3V	LVC 2.5V	LVC 1.8V	AUP 3.3V	AUP 2.5V	AUP 1.8V	AUP 1.1V
I <sub>PLH</sub>	Any In	Y	MAX	5.1	6.3	8.3	14.4	6.3	7.6	10.2	19
I <sub>PHL</sub>				5.1	6.3	8.3	14.4	6.3	7.6	10.2	19

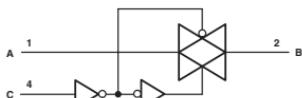
UNIT: ns

# 1G66

## SINGLE BILATERAL ANALOG SWITCH

- High On-Off Outputs Voltage Ratio
- High Degree of Linearity

### Logic Diagram



### FUNCTION TABLE

CONTROL INPUT (C)	SWITCH1
L	OFF
H	ON

### ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	LVC 5V	LVC 3.3V	LVC 2.5V	LVC 1.8V	AUC 2.5V	AUC 1.8V	UNIT
I <sub>CC</sub>	MAX	0.01	0.01	0.01	0.01	0.01	0.01	mA
R <sub>ON</sub>	MAX	10	15	20	30	15	20	Ω
R <sub>ON(P)</sub>	MAX	15	20	30	120	20	80	Ω

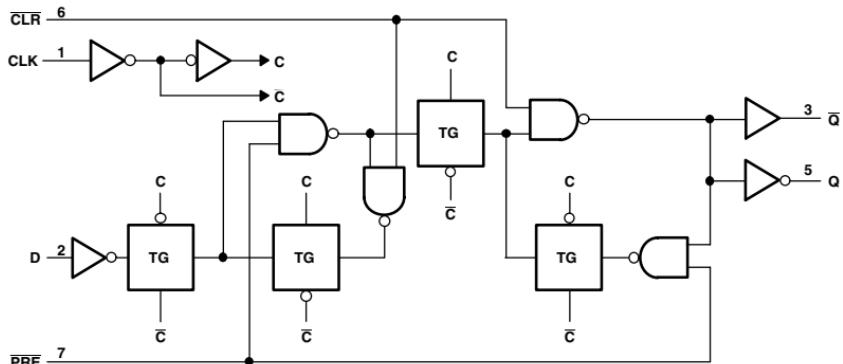
### SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	LVC 5V	LVC 3.3V	LVC 2.5V	LVC 1.8V	AUC 2.5V	AUC 1.8V
I <sub>PLH</sub>	A or B	B or A	MAX	0.6	0.8	1.2	2	0.3	0.3
I <sub>PHL</sub>				0.6	0.8	1.2	2	0.3	0.3
I <sub>PZH</sub>	C	B or A	MAX	4.2	5	6.5	12	1.4	2.3
I <sub>PZL</sub>				4.2	5	6.5	12	1.4	2.3
I <sub>PZH</sub>	C	B or A	MAX	5	6.5	6.9	10	1.5	2.9
I <sub>PZL</sub>				5	6.5	6.9	10	1.5	2.9

UNIT : ns

## SINGLE POSITIVE-EDGE-TRIGGERED D-TYPE FLIP-FLOP WITH CLEAR AND PRESET

Logic Diagram



FUNCTION TABLE

INPUTS			OUTPUTS	
PRE	CLR	CLK	Q	Q̄
L	H	X	X	H L
X	L	X	X	L H
H	H	↑	H	H L
H	H	↑	L	L H
H	H	L	X	Q <sub>0</sub> Q̄ <sub>0</sub>

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	AUC 2.5V	AUC 1.8V	AUP 3.3V	AUP 2.5V	AUP 1.8V	AUP 1.1V	UNIT
I <sub>CC</sub>	MAX	0.01	0.01	0.0009	0.0009	0.0009	0.0009	mA
I <sub>OH</sub>	MAX	-9	-8	-4	-3.1	-1.9	-1.1	mA
I <sub>OL</sub>	MAX	9	8	4	3.1	1.9	1.1	mA

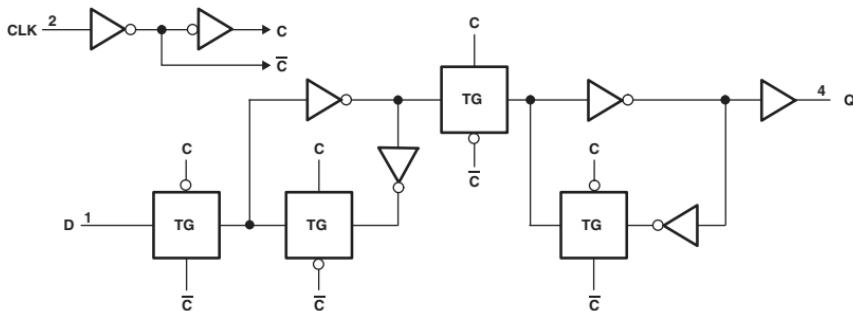
TIMING REQUIREMENTS AND SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT		MAX or MIN	AUC 2.5V	AUC 1.8V	AUP 3.3V	AUP 2.5V	AUP 1.8V	AUP 1.1V
f <sub>max</sub>			MIN		275	250	160	130	60	50
t <sub>w</sub>	Pulse duration		CLK	MIN	1	1	2	2	2	2
			PRE or CLR	low	MIN	1	1	2	2	2
t <sub>su</sub>	Setup time, before CLK ↑		Data	high	MIN	0.4	0.5	0.5	0.5	1.3
			low	MIN	0.4	0.5	1	1	1	1.2
			PRE or CLR	inactive	MIN	0.4	0.7	0.5	0.5	0.5
t <sub>h</sub>	Hold time, data after CLK ↑		MIN		0.3	0.3	0	0	0	0
IPLH	CLK	Q		MAX	1.8	2.4	5.3	7	10.4	21.8
IPLHL		Q̄		MAX	1.8	2.4	5.3	7	10.4	21.8
IPLH	CLK	Q		MAX	1.8	2.4	5.2	6.7	9.9	20.3
IPLHL		Q̄		MAX	1.8	2.4	5.2	6.7	9.9	20.3
IPLH	PRE or CLR	Q or Q̄		MAX	2.1	2.8	5.8	7.4	10.8	21.4
IPLHL		Q or Q̄		MAX	2.1	2.8	5.8	7.4	10.8	21.4

UNIT f<sub>max</sub>: MHz other : ns

## SINGLE POSITIVE-EDGE-TRIGGERED D-TYPE FLIP-FLOP

Logic Diagram



## FUNCTION TABLE

INPUTS		OUTPUT
CLK	D	Q
↑ H	H	
↑ L	L	
L X		Q <sub>0</sub>

## ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

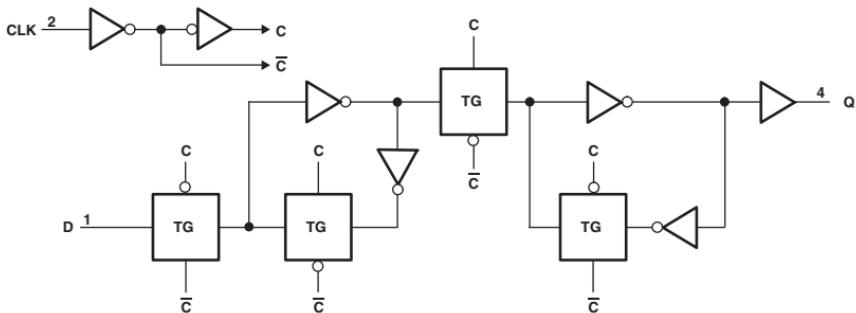
PARAMETER	MAX or MIN	LVC 5V	LVC 3.3V	LVC 2.5V	LVC 1.8V	AUC 2.5V	AUC 1.8V	AUP 3.3V	AUP 2.5V	AUP 1.8V	AUP 1.1V	UNIT
I <sub>CC</sub>	MAX	0.01	0.01	0.01	0.01	0.01	0.01	0.0009	0.0009	0.0009	0.0009	mA
I <sub>OH</sub>	MAX	-32	-24	-8	-4	-9	-8	-4	-3.1	-1.9	-1.1	mA
I <sub>OL</sub>	MAX	32	24	8	4	9	8	4	3.1	1.9	1.1	mA

## TIMING REQUIREMENTS AND SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	LVC 5V			LVC 3.3V			LVC 2.5V			LVC 1.8V			AUC 2.5V			AUC 1.8V			AUP 3.3V			AUP 2.5V			AUP 1.8V				
				MIN	160	160	160	160	275	250	260	250	240	160	2.5	2.5	2.5	2.5	1.7	1.7	1.9	1.7	1.6	2.2	2.5	2.5	2.5	2.5	1.7	1.7	1.9	
f <sub>max</sub>				MIN																												
t <sub>w</sub>	CLK high or low			MIN	2.5	2.5	2.5	2.5	1.7	1.7	1.9	1.7	1.6	2.2																		
t <sub>su</sub>	Before CLK ↑, Data high			MIN	1.2	1.3	1.4	2.2	0.7	0.5	0.6	0.7	0.9	1.4																		
Before CLK ↑, Data low					1.2	1.3	1.4	2.6	0.7	0.5	1	1	1.1	1.8																		
t <sub>th</sub>	Data after CLK ↑			MIN	0.5	1.0	0.4	0.3	0.1	0	0	0	0	0																		
t <sub>PLH</sub>	CLK	Q	MAX		4.5	5	7	9.9	1.8	2.4	4.5	5.7	8	14.4																		
UNIT f <sub>max</sub> : MHz other : ns					4.5	5	7	9.9	1.8	2.4	4.5	5.7	8	14.4																		

## SINGLE POSITIVE-EDGE-TRIGGERED D-TYPE FLIP-FLOP

Logic Diagram



FUNCTION TABLE

INPUTS	OUTPUT	
CLK	D	Q
↑ H	L	
↑ L	H	
L X		Q <sub>0</sub>

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	LVC 5V	LVC 3.3V	LVC 2.5V	LVC 1.8V	AUC 2.5V	AUC 1.8V	AUP 3.3V	AUP 2.5V	AUP 1.8V	AUP 1.1V	UNIT
I <sub>CC</sub>	MAX	0.01	0.01	0.01	0.01	0.01	0.01	0.0009	0.0009	0.0009	0.0009	mA
I <sub>OH</sub>	MAX	-32	-24	-8	-4	-9	-8	-4	-3.1	-1.9	-1.1	mA
I <sub>OL</sub>	MAX	32	24	8	4	9	8	4	3.1	1.9	1.1	mA

TIMING REQUIREMENTS AND SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	LVC 5V	LVC 3.3V	LVC 2.5V	LVC 1.8V	AUC 2.5V	AUC 1.8V	AUP 3.3V	AUP 2.5V	AUP 1.8V	AUP 1.1V
f <sub>max</sub>			MIN	160	160	160	160	275	250	260	250	240	170
t <sub>w</sub>	CLK high or low		MIN	2.5	2.5	2.5	2.5	1.7	1.7	1.9	1.7	1.6	2.5
t <sub>su</sub>	Before CLK ↑, Data high		MIN	1.1	1.3	1.5	2.3	0.5	0.6	0.4	0.6	0.8	1.2
	Before CLK ↑, Data low			1.1	1.3	1.5	2.5	0.5	0.6	0.7	0.8	1.1	2
t <sub>th</sub>	Data after CLK ↑		MIN	0.4	0.9	0.2	0	0.1	0.1	0	0	0	0
t <sub>PLH</sub>	CLK	Q̄	MAX	4.5	5.2	7	9.9	1.8	2.4	4.9	6.3	7.3	17.7
t <sub>PHL</sub>				4.5	5.2	7	9.9	1.8	2.4	4.9	6.3	7.3	17.7

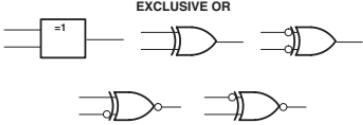
UNIT f<sub>max</sub> : MHz other : ns

# 1G86

## SINGLE 2-INPUT EXCLUSIVE-OR GATE

- $Y = A \oplus B$

### Logic Diagram



An exclusive-OR gate has many applications, some of which can be represented better by alternative logic symbols.

### FUNCTION TABLE

INPUTS	OUTPUT	
A	B	Y
L	L	L
L	H	H
H	L	H
H	H	L

### ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	AHC	AHCT	LVC 5V	LVC 3.3V	LVC 2.5V	LVC 1.8V	AUC 2.5V	AUC 1.8V	UNIT
$I_{CC}$	MAX	0.01	0.01	0.01	0.01	0.01	0.01	0.01	0.01	mA
$I_{OH}$	MAX	-8	-8	-32	-24	-8	-4	-9	-8	mA
$I_{OL}$	MAX	8	8	32	24	8	4	9	8	mA

### SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	AHC	AHCT	LVC 5V	LVC 3.3V	LVC 2.5V	LVC 1.8V	AUC 2.5V	AUC 1.8V
$t_{PLH}$	A or B	Y	MAX	10	9	4	5	5.5	9.9	2	2.6
$t_{PHL}$				10	9	4	5	5.5	9.9	2	2.6

UNIT:ns

# 1G97

## CONFIGURABLE MULTIPLE-FUNCTION GATE

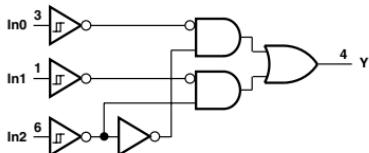
### FUNCTION SELECTION TABLE

2-to-1 data selector
2-input AND gate
2-input OR gate with one inverted input
2-input NAND gate with one inverted input
2-input AND gate with one inverted input
2-input NOR gate with one inverted input
2-input OR gate
Inverter
Noninverted buffer

### FUNCTION TABLE

INPUTS	OUTPUT		
In2	In1	In0	Y
L	L	L	L
L	L	H	L
L	H	L	H
L	H	H	H
H	L	L	L
H	L	H	H
H	H	L	L
H	H	H	H

### Logic Diagram



### ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	LVC 5V	LVC 3.3V	LVC 2.5V	LVC 1.8V	AUP 3.3V	AUP 2.5V	AUP 1.8V	AUP 1.1V	UNIT
$I_{CC}$	MAX	0.01	0.01	0.01	0.01	0.0009	0.0009	0.0009	0.0009	mA
$I_{OH}$	MAX	-32	-24	-8	-4	-4	-3.1	-1.9	-1.1	mA
$I_{OL}$	MAX	32	24	8	4	4	3.1	1.9	1.1	mA

### SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	LVC 5V	LVC 3.3V	LVC 2.5V	LVC 1.8V	AUP 3.3V	AUP 2.5V	AUP 1.8V	AUP 1.1V
$t_{PLH}$	Any In	Y	MAX	5.1	6.3	8.3	14.4	6.4	7.8	10.5	19.2
$t_{PHL}$				5.1	6.3	8.3	14.4	6.4	7.8	10.5	19.2

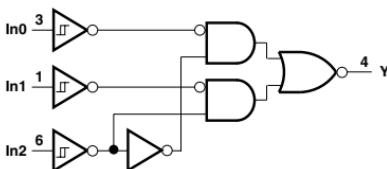
UNIT:ns

## CONFIGURABLE MULTIPLE-FUNCTION GATE

## FUNCTION SELECTION TABLE

2-to-1 data selector with inverted output
2-input NAND gate
2-input NOR gate with one inverted input
2-input AND gate with one inverted input
2-input NAND gate with one inverted input
2-input OR gate with one inverted input
2-input NOR gate
Noninverted buffer
Inverter

## Logic Diagram



## FUNCTION TABLE

INPUTS			OUTPUT
In2	In1	In0	Y
L	L	L	H
L	L	H	H
L	H	L	L
L	H	H	L
H	L	L	H
H	L	H	L
H	H	L	H
H	H	H	L

## ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	LVC 5V	LVC 3.3V	LVC 2.5V	LVC 1.8V	AUP 3.3V	AUP 2.5V	AUP 1.8V	AUP 1.1V	UNIT
I <sub>CC</sub>	MAX	0.01	0.01	0.01	0.01	0.0009	0.0009	0.0009	0.0009	mA
I <sub>OH</sub>	MAX	-32	-24	-8	-4	-4	-3.1	-1.9	-1.1	mA
I <sub>OL</sub>	MAX	32	24	8	4	4	3.1	1.9	1.1	mA

## SWITCHING CHARACTERISTICS

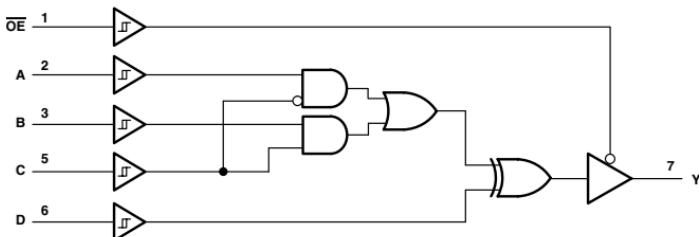
PARAMETER	INPUT	OUTPUT	MAX or MIN	LVC 5V	LVC 3.3V	LVC 2.5V	LVC 1.8V	AUP 3.3V	AUP 2.5V	AUP 1.8V	AUP 1.1V
t <sub>PLH</sub>	Any In	Y	MAX	5.1	6.3	8.3	14.4	6	7.3	10.2	19
t <sub>PHL</sub>				5.1	6.3	8.3	14.4	6	7.3	10.2	19

UNIT:ns

## SINGLE RETRIGGERABLE MONOSTABLE MULTIVIBRATOR WITH SCHMITT-TRIGGER INPUTS

- Offers Nine Different Logic Functions in a Single Package

Logic Diagram



FUNCTION TABLE

INPUTS					OUTPUT Y
$\overline{OE}$	D	C	B	A	
L	L	L	L	L	L
L	L	L	L	H	H
L	L	L	H	L	L
L	L	L	H	H	H
L	L	H	L	L	L
L	L	H	L	H	L
L	L	H	H	L	H
L	L	H	H	H	H
L	H	L	L	L	H
L	H	L	L	H	L
L	H	L	H	L	H
L	H	L	H	H	L
L	H	H	L	L	H
L	H	H	H	L	L
L	H	H	H	H	H
H	H or L				Z

PRIMARY FUNCTION

3-state buffer
3-state inverter
3-state 2-in-1 data selector MUX
3-state 2-in-1 data selector MUX, inverted out
3-state 2-input AND
3-state 2-input AND, one input inverted
3-state 2-input AND, both inputs inverted
3-state 2-input NAND
3-state 2-input NAND, one input inverted
3-state 2-input NAND, both inputs inverted
3-state 2-input XOR
3-state 2-input XNOR

COMPLEMENTARY FUNCTION

3-state 2-input NOR, both inputs inverted
3-state 2-input NOR, one input inverted
3-state 2-input OR
3-state 2-input OR, one input inverted
3-state 2-input OR
3-state 2-input XOR, one input inverted

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	LVC 5V	LVC 3.3V	LVC 2.5V	LVC 1.8V	AUP 3.3V	AUP 2.5V	AUP 1.8V	AUP 1.1V	UNIT
$I_{CC}$	MAX	0.01	0.01	0.01	0.01	0.0009	0.0009	0.0009	0.0009	mA
$I_{OH}$	MAX	-32	-24	-8	-4	-4	-3.1	-1.9	-1.1	mA
$I_{OL}$	MAX	32	24	8	4	4	3.1	1.9	1.1	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	LVC 5V	LVC 3.3V	LVC 2.5V	LVC 1.8V	AUP 3.3V	AUP 2.5V	AUP 1.8V	AUP 1.1V
$t_{PLH}$	A	Y	MAX	5.5	8.4	11.7	30.8	8.4	10.5	14.5	29.8
				5.5	8.4	11.7	30.8	8.4	10.5	14.5	29.8
$t_{PHL}$	B	Y	MAX	5.4	8.2	11.3	28.9	8.4	10.5	14.5	29.8
				5.4	8.2	11.3	28.9	8.4	10.5	14.5	29.8
$t_{PLH}$	C	Y	MAX	5.7	8.6	12.3	29.8	8.4	10.5	14.5	29.8
				5.7	8.6	12.3	29.8	8.4	10.5	14.5	29.8
$t_{PLH}$	D	Y	MAX	5.2	7.6	10.7	25.7	8.4	10.5	14.5	29.8
				5.2	7.6	10.7	25.7	8.4	10.5	14.5	29.8
$t_{PZH}$	$\overline{OE}$	Y	MAX	4.7	7	11.3	25.2	8.2	9.9	14.8	29.3
				4.7	7	11.3	25.2	8.2	9.9	14.8	29.3
$t_{PZL}$	$\overline{OE}$	Y	MAX	4.5	5.6	5.8	15	5.8	5.5	7.9	10
				4.5	5.6	5.8	15	5.8	5.5	7.9	10

UNIT : ns

## SINGLE RETRIGGERABLE MONOSTABLE MULTIVIBRATOR WITH SCHMITT-TRIGGER INPUTS

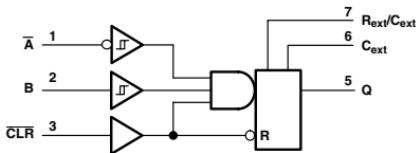
- Schmitt-Triggered Circuitry on  $\bar{A}$  and B Inputs for Slow Input Transition Rates
- Edge Triggered From Active-High or Active-Low Gated Logic Inputs
- Retriggerable for Very Long Outputs Pulses, up to 100% Duty Cycle
- Overriding Clear Terminates Output Pulse
- Glitch-Free Power-Up Reset on Outputs

## Logic Diagram

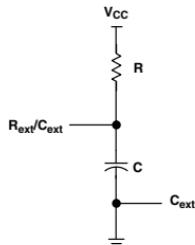
## FUNCTION TABLE

INPUTS			OUTPUT Q
CLR	$\bar{A}$	B	
L	X	X	L
X	H	X	$L^{(1)}$
X	X	L	$L^{(1)}$
H	L	↑	↑
H	↓	H	↑
↑	L	H	↑

(1) These outputs are based on the assumption that the indicated steady-state conditions at the A and B inputs have been set up long enough to complete any pulse started before the setup.



## REQUIRED TIMING CIRCUIT



## ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER		MAX or MIN	LVC 5V	LVC 3.3V	LVC 2.5V	LVC 1.8V	UNIT
Icc	Quiescent	MAX	0.01	-	-	-	mA
Icc	Active State	MAX	0.975	0.65	0.28	0.22	mA
IoH		MAX	-32	-24	-8	-4	mA
IoL		MAX	32	24	8	4	mA

## TIMING REQUIREMENTS

PARAMETER		MAX or MIM	LVC 5V	LVC 3.3V	LVC 2.5V	LVC 1.8V
twIN	CLR	MAX	2.5	3	4	8
	$\bar{A}$ or B trigger	MAX	2.5	3	4	8

UNIT : ns

## SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	LVC 5V	LVC 3.3V	LVC 2.5V	LVC 1.8V
tPLH	$\bar{A}$ or B	Q	MAX	8.2	12.5	18.5	57
tPHL				8.2	12.5	18.5	57
tPLH	$\bar{C}\bar{L}$	Q	MAX	6	8.6	12.5	36.5
tPHL				6	8.6	12.5	36.5
tPLH	$\bar{C}\bar{L}$ trigger	Q	MAX	7.5	11.5	17	59
tPHL				7.5	11.5	17	59

UNIT : ns

# 1G125

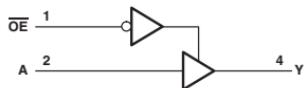
## Logic Diagram

### SINGLE BUS BUFFER GATE WITH 3-STATE OUTPUT

- $Y = A$

#### FUNCTION TABLE

INPUTS	OUTPUT	
OE	A	Y
L	H	H
L	L	L
H	X	Z



#### ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	AHC	AHCT	LVC 5V	LVC 3.3V	LVC 2.5V	LVC 1.8V	AUC 2.5V	AUC 1.8V	AUP 3.3V	AUP 2.5V	AUP 1.8V	AUP 1.1V	UNIT
I <sub>CC</sub>	MAX	0.01	0.01	0.01	0.01	0.01	0.01	0.01	0.0009	0.0009	0.0009	0.0009	mA	
I <sub>OH</sub>	MAX	-8	-8	-32	-24	-8	-4	-9	-8	-4	-3.1	-1.9	-1.1	mA
I <sub>OL</sub>	MAX	8	8	32	24	8	4	9	8	4	3.1	1.9	1.1	mA

#### SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	AHC	AHCT	LVC 5V	LVC 3.3V	LVC 2.5V	LVC 1.8V	AUC 2.5V	AUC 1.8V	AUP 3.3V	AUP 2.5V	AUP 1.8V	AUP 1.1V
t <sub>PLH</sub>	A	Y	MAX	8.5	8.5	4	4.5	5.5	9	1.7	2.5	5.2	6.4	9.1	16.6
t <sub>PHL</sub>				8.5	8.5	4	4.5	5.5	9	1.7	2.5	5.2	6.4	9.1	16.6
t <sub>PZH</sub>	OE	Y	MAX	8	8	5	5.3	6.6	10.1	1.9	2.6	6.4	7.8	11	20.2
t <sub>PZL</sub>				8	8	5	5.3	6.6	10.1	1.9	2.6	6.4	7.8	11	20.2
t <sub>PHZ</sub>	OE	Y	MAX	10	10	4.2	5	5	9.2	1.7	3.1	5.6	5.4	7.5	14
t <sub>PZL</sub>				10	10	4.2	5	5	9.2	1.7	3.1	5.6	5.4	7.5	14

UNIT:ns

# 1G126

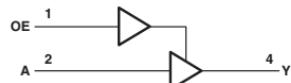
## Logic Diagram

### SINGLE BUS BUFFER GATE WITH 3-STATE OUTPUT

- $Y = A$

#### FUNCTION TABLE

INPUTS	OUTPUT	
OE	A	Y
H	H	H
H	L	L
L	X	Z



#### ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	AHC	AHCT	LVC 5V	LVC 3.3V	LVC 2.5V	LVC 1.8V	AUC 1.8V	AUC 1.8V	AUP 3.3V	AUP 2.5V	AUP 1.8V	AUP 1.1V	UNIT
I <sub>CC</sub>	MAX	0.01	0.01	0.01	0.01	0.01	0.01	0.01	0.0009	0.0009	0.0009	0.0009	mA	
I <sub>OH</sub>	MAX	-8	-8	-32	-24	-8	-4	-9	-8	-4	-3.1	-1.9	-1.1	mA
I <sub>OL</sub>	MAX	8	8	32	24	8	4	9	8	4	3.1	1.9	1.1	mA

#### SWITCHING CHARACTERISTICS

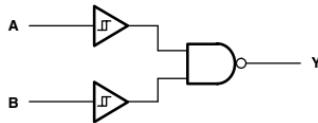
PARAMETER	INPUT	OUTPUT	MAX or MIN	AHC	AHCT	LVC 5V	LVC 3.3V	LVC 2.5V	LVC 1.8V	AUC 2.5V	AUC 1.8V	AUP 3.3V	AUP 2.5V	AUP 1.8V	AUP 1.1V
t <sub>PLH</sub>	A	Y	MAX	8.5	8.5	4	4.5	5.5	8	1.7	2.5	5.2	6.4	9.1	16.6
t <sub>PHL</sub>				8.5	8.5	4	4.5	5.5	8	1.7	2.5	5.2	6.4	9.1	16.6
t <sub>PZH</sub>	OE	Y	MAX	8	8	5	5.3	6.6	9.4	1.9	2.5	6.4	7.8	11	20.2
t <sub>PZL</sub>				8	8	5	5.3	6.6	9.4	1.9	2.5	6.4	7.8	11	20.2
t <sub>PHZ</sub>	OE	Y	MAX	10	10	4.2	5.5	5.5	9.8	2.1	3.1	5.6	5.4	7.5	14
t <sub>PZL</sub>				10	10	4.2	5.5	5.5	9.8	2.1	3.1	5.6	5.4	7.5	14

UNIT:ns

## SINGLE 2-INPUT NAND GATE WITH SCHMITT-TRIGGER INPUTS

- $Y = \overline{A \cdot B}$  or  $Y = \overline{A} + \overline{B}$

Logic Diagram



## FUNCTION TABLE

INPUTS		OUTPUT
A	B	Y
L	L	H
L	H	H
H	L	H
H	H	L

## ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	LVC 5V	LVC 3.3V	LVC 2.5V	LVC 1.8V	UNIT
I <sub>CC</sub>	MAX	0.01	0.01	0.01	0.01	mA
I <sub>OH</sub>	MAX	-32	-24	-8	-4	mA
I <sub>OL</sub>	MAX	32	24	8	4	mA

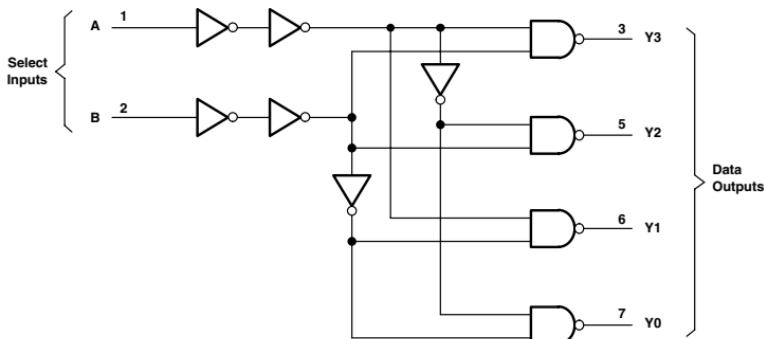
## SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	LVC 5V	LVC 3.3V	LVC 2.5V	LVC 1.8V
t <sub>IPLH</sub>	A or B	Y	MAX	5	6	7.5	16
t <sub>IPHL</sub>				5	6	7.5	16

UNIT : ns

## 2-TO-4 LINE DECODER

Logic Diagram



FUNCTION TABLE

INPUTS B    A	OUTPUTS			
	Y0	Y1	Y2	Y3
L    L	L	H	H	H
L    H	H	L	H	H
H    L	H	H	L	H
H    H	H	H	H	L

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	LVC 5V	LVC 3.3V	LVC 2.5V	LVC 1.8V	UNIT
I <sub>CC</sub>	MAX	0.01	0.01	0.01	0.01	mA
I <sub>OH</sub>	MAX	-32	-24	-8	-4	mA
I <sub>OL</sub>	MAX	32	24	8	4	mA

SWITCHING CHARACTERISTICS

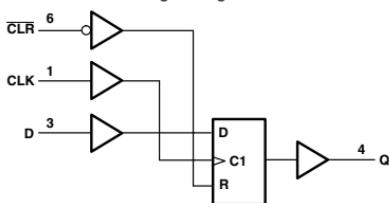
PARAMETER	INPUT	OUTPUT	MAX or MIN	LVC 5V	LVC 3.3V	LVC 2.5V	LVC 1.8V
t <sub>PLH</sub>	A or B	Y	MAX	4.2	5.9	8.2	16.7
t <sub>PHL</sub>				4.2	5.9	8.2	16.7

UNIT : ns

## SINGLE D-TYPE FLIP-FLOP WITH ASYNCHRONOUS CLEAR

- Complementary Outputs ( $Q$ ,  $\bar{Q}$ )
- Buffered Clock and Direct Clear Inputs
- Asynchronous Clear Function

Logic Diagram



FUNCTION TABLE

INPUTS		OUTPUT	
CLR	CLK	D	Q
H	↑	L	L
H	↑	H	H
H	H or L	X	$Q_O$
L	X	X	L

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	LVC 5V	LVC 3.3V	LVC 2.5V	LVC 1.8V	UNIT
$I_{CC}$	MAX	0.01	0.01	0.01	0.01	mA
$I_{OH}$	MAX	-32	-24	-8	-4	mA
$I_{OL}$	MAX	32	24	8	4	mA

TIMING REQUIREMENTS AND SWITCHING CHARACTERISTICS

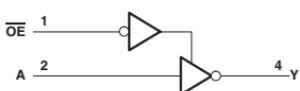
PARAMETER	INPUT	OUTPUT	MAX or MIN	LVC 5V	LVC 3.3V	LVC 2.5V	LVC 1.8V
$f_{max}$			MIN	175	150	125	100
$t_w$ Pulse duration	$\overline{CLR}$ Low		MIN	2.5	2.8	3	5.6
	CLK High or low		MIN	2.5	2.8	3	3.5
$t_{su}$ Setup time, before CLK ↑	Data		MIN	1.5	2	2.5	3
	$\overline{CLR}$ inactive		MIN	0.5	0.5	0	0
$t_h$	Hold time, data after CLK ↑		MIN	0.5	0.5	0	0
$t_{PLH}$	CLK	Q	MAX	4	5.7	7.1	13.4
				4	5.7	7.1	13.4
$t_{PHL}$	$\overline{CLR}$	Q	MAX	4.1	5.8	7	12.9
				4.1	5.8	7	12.9

UNIT  $f_{max}$ : MHz other : ns

# 1G240

## Logic Diagram

### SINGLE BUFFER/DRIVER WITH 3-STATE OUTPUT



#### FUNCTION TABLE

INPUTS	OUTPUT	
OE	A	Y
L	H	L
L	L	H
H	X	Z

#### ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	LVC 5V	LVC 3.3V	LVC 2.5V	LVC 1.8V	AUC 2.5V	AUC 1.8V	AUP 3.3V	AUP 2.5V	AUP 1.8V	AUP 1.1V	UNIT
I <sub>CC</sub>	MAX	0.01	0.01	0.01	0.01	0.0009	0.0009	0.0009	0.0009	0.0009	0.0009	mA
I <sub>OH</sub>	MAX	-32	-24	-8	-4	-9	-8	-4	-3.1	-1.9	-1.1	mA
I <sub>OL</sub>	MAX	32	24	8	4	9	8	4	3.1	1.9	1.1	mA

#### SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	LVC 5V	LVC 3.3V	LVC 2.5V	LVC 1.8V	AUC 2.5V	AUC 1.8V	AUP 3.3V	AUP 2.5V	AUP 1.8V	AUP 1.1V
t <sub>PLH</sub>	A	Y	MAX	4	4.5	5.5	8.6	1.7	2.5	5.2	6.3	9.1	17.3
t <sub>PHL</sub>				4	4.5	5.5	8.6	1.7	2.5	5.2	6.3	9.1	17.3
t <sub>PZH</sub>	OE	Y	MAX	5.2	5.4	6.5	10.0	1.9	2.6	6.3	7.7	10.9	20.9
t <sub>PZL</sub>				5.2	5.4	6.5	10.0	1.9	2.6	6.3	7.7	10.9	20.9
t <sub>PHZ</sub>	OE	Y	MAX	4.1	5.2	4.9	9.4	1.7	3.1	9.1	7.3	10.1	12.9
t <sub>PZL</sub>				4.1	5.2	4.9	9.4	1.7	3.1	9.1	7.3	10.1	12.9

UNIT:ns

# 1G332

## Logic Diagram

### SINGLE 3-INPUT POSITIVE-OR GATE

$$\bullet \quad Y = A + B + C$$



#### FUNCTION TABLE

INPUTS	OUTPUT		
A	B	C	Y
H	X	X	H
X	H	X	H
X	X	H	H
L	L	L	L

#### ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	LVC 5V	LVC 3.3V	LVC 2.5V	LVC 1.8V	UNIT
I <sub>CC</sub>	MAX	0.01	0.01	0.01	0.01	mA
I <sub>OH</sub>	MAX	-32	-24	-8	-4	mA
I <sub>OL</sub>	MAX	32	24	8	4	mA

#### SWITCHING CHARACTERISTICS

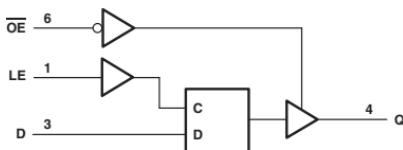
PARAMETER	INPUT	OUTPUT	MAX or MIN	LVC 5V	LVC 3.3V	LVC 2.5V	LVC 1.8V
t <sub>PLH</sub>	A, B or C	Y	MAX	3.5	4.8	6.2	17.2
t <sub>PHL</sub>				3.5	4.8	6.2	17.2

UNIT:ns

# 1G373

## SINGLE D-TYPE LATCH WITH 3-STATE OUTPUT

- 3-State Outputs
- Buffered Control Inputs

**Logic Diagram****FUNCTION TABLE**

INPUTS			OUTPUT
OE	LE	D	Q
L	H	L	L
L	H	H	H
L	L	X	Q <sub>O</sub>
H	X	X	Z

**ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS**

PARAMETER	MAX or MIN	LVC 5V	LVC 3.3V	LVC 2.5V	LVC 1.8V	UNIT
I <sub>CC</sub>	MAX	0.01	0.01	0.01	0.01	mA
I <sub>OH</sub>	MAX	-32	-24	-8	-4	mA
I <sub>OL</sub>	MAX	32	24	8	4	mA

**TIMING REQUIREMENTS AND SWITCHING CHARACTERISTICS**

PARAMETER	INPUT	OUTPUT	MAX or MIN	LVC 5V	LVC 3.3V	LVC 2.5V	LVC 1.8V
t <sub>w</sub>	Pulse duration, LE high		MIN	3	3	3	3
t <sub>su</sub>	Setup time, data before LE ↓		MIN	1.5	1.5	2	2.4
t <sub>th</sub>	Hold time, data after LE ↓		MIN	1.5	1.5	1.5	2.5
t <sub>PLH</sub>	D	Q	MAX	4	5.4	7.3	16
t <sub>PHL</sub>				4	5.4	7.3	16
t <sub>PLH</sub>	LE	Q	MAX	4	5.5	7.4	16.3
t <sub>PHL</sub>				4	5.5	7.4	16.3
t <sub>PZH</sub>	OĒ	Q	MAX	3.7	5.1	6.3	13
t <sub>PZL</sub>				3.7	5.1	6.3	13
t <sub>PHZ</sub>	OĒ	Q	MAX	4.6	6.5	5.9	17.4
t <sub>PLZ</sub>				4.6	6.5	5.9	17.4

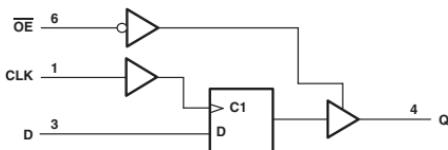
UNIT : ns

# 1G374

## SINGLE D-TYPE FLIP-FLOP WITH 3-STATE OUTPUT

- 3-State Outputs
- Buffered Control Inputs

**Logic Diagram**



**FUNCTION TABLE**

INPUTS			OUTPUT Q
<u>OE</u>	CLK	D	
L	↑	L	L
L	↑	H	H
L	H or L	X	Q
H	X	X	Z

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	LVC 5V	LVC 3.3V	LVC 2.5V	LVC 1.8V	UNIT
$I_{CC}$	MAX	0.01	0.01	0.01	0.01	mA
$I_{OH}$	MAX	-32	-24	-8	-4	mA
$I_{OL}$	MAX	32	24	8	4	mA

TIMING REQUIREMENTS AND SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	LVC 5V	LVC 3.3V	LVC 2.5V	LVC 1.8V
$f_{max}$			MIN	175	150	125	100
$t_w$	Pulse duration, CLK high or low		MIN	2.5	2.8	3	3.3
$t_{su}$	Setup time, data before CLK ↑		MIN	1.5	2	2.5	3.5
$t_h$	Hold time, data after CLK ↑		MIN	1.5	1.5	1.6	3.4
$t_{PLH}$	CLK	Q	MAX	4	6	8.2	18.3
$t_{PHL}$				4	6	8.2	18.3
$t_{PZH}$	$\overline{OE}$	Q	MAX	3.5	5	6.3	13
$t_{PZL}$				3.5	5	6.3	13
$t_{PHZ}$	$\overline{OE}$	Q	MAX	3.1	4.5	5.3	14
$t_{PLZ}$				3.1	4.5	5.3	14

UNIT  $f_{max}$ : MHz other : ns

## SINGLE 3-INPUT EXCLUSIVE-XOR GATE

- $Y = A \oplus B \oplus C$



FUNCTION TABLE

INPUTS			OUTPUT
A	B	C	Y
L	L	L	L
L	L	H	H
L	H	L	H
L	H	H	L
H	L	L	H
H	L	H	L
H	H	L	L
H	H	H	H

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	LVC 5V	LVC 3.3V	LVC 2.5V	LVC 1.8V	UNIT
$I_{CC}$	MAX	0.01	0.01	0.01	0.01	mA
$I_{OH}$	MAX	-32	-24	-8	-4	mA
$I_{OL}$	MAX	32	24	8	4	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	LVC 5V	LVC 3.3V	LVC 2.5V	LVC 1.8V
$t_{PLH}$	A, B or C	Y	MAX	4	5	5.5	12

UNIT:ns

## 1G0832

Logic Diagram

## SINGLE 3-INPUT POSITIVE AND-OR GATE

- $Y = (A \cdot B) + C$
  - Can Be Used in Three Combinations
- AND-OR Gate  
AND Gate  
OR Gate



FUNCTION SELECTION TABLE

2-Input AND Gate
2-Input OR Gate
$Y = (A \cdot B) + C$

FUNCTION TABLE

INPUTS			OUTPUT
A	B	C	Y
X	X	H	H
H	H	X	H
X	L	L	L
L	X	L	L

X = Valid H or L

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	LVC 5V	LVC 3.3V	LVC 2.5V	LVC 1.8V	UNIT
$I_{CC}$	MAX	0.01	0.01	0.01	0.01	mA
$I_{OH}$	MAX	-32	-24	-8	-4	mA
$I_{OL}$	MAX	32	24	8	4	mA

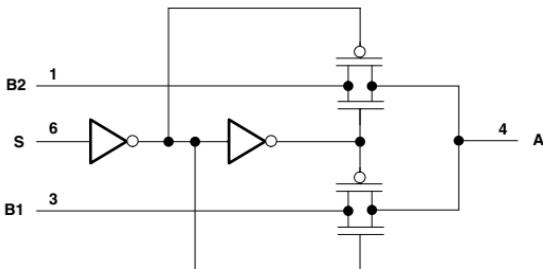
SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	LVC 5V	LVC 3.3V	LVC 2.5V	LVC 1.8V
$t_{PLH}$	A, B, or C	Y	MAX	4	5.9	7.6	17.5

UNIT : ns

**SINGLE-POLE, DOUBLE-THROW ANALOG SWITCH**

- Useful for Both Analog and Digital Applications
- Specified Break-Before-Make Switching
- Rail-to-Rail Signal Handling
- High Degree of Linearity

**Logic Diagram****FUNCTION TABLE**

CONTROL INPUT S	ON CHANNEL
L	B1
H	B2

**RECOMMENDED OPERATING CONDITIONS**

PARAMETER	MAX or MIN	LVC 5V	LVC 3.3V	LVC 2.5V	LVC 1.8V	UNIT
Icc	MAX	0.01	0.01	0.01	0.01	mA

**ELECTRICAL CHARACTERISTICS**

PARAMETER	MAX or MIN	LVC 5V	LVC 3.3V		LVC 2.5V		LVC 1.8V		UNIT
Io		30	-30	24	-24	8	-8	4	-4 mA
Ron	MAX	7	15	9	20	12	30	20	50 W

UNIT:ns

**SWITCHING CHARACTERISTICS**

PARAMETER	INPUT	OUTPUT	MAX or MIN	LVC 5V	LVC 3.3V	LVC 2.5V	LVC 1.8V
tPLH	A or Bn	Bn or A	MAX	0.3	0.8	1.2	2
tPHL				0.3	0.8	1.2	2
tPZH	S	Bn	MAX	5.7	7.6	14	24
tPZI				5.7	7.6	14	24
tPHZ	S	Bn	MAX	3.8	5.3	7.5	13
tPLZ				3.8	5.3	7.5	13

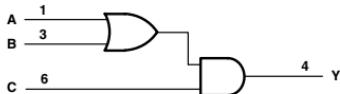
UNIT:ns

# 1G3208

## SINGLE 3-INPUT POSITIVE OR-AND GATE

- $Y = (A + B) \bullet C$
- Can Be Used in Three Combinations  
OR-AND Gate  
OR Gate  
AND Gate

Logic Diagram



## FUNCTION SELECTION TABLE

2-Input AND Gate
2-Input OR Gate
$Y = (A + B) \bullet C$

## FUNCTION TABLE

INPUTS			OUTPUT Y
A	B	C	
H	X	H	H
X	H	H	H
X	X	L	L
L	L	H	L

X = Valid H or L

## ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	LVC 5V	LVC 3.3V	LVC 2.5V	LVC 1.8V	UNIT
$I_{CC}$	MAX	0.01	0.01	0.01	0.01	mA
$I_{OH}$	MAX	-32	-24	-8	-4	mA
$I_{OL}$	MAX	32	24	8	4	mA

## SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	LVC 5V	LVC 3.3V	LVC 2.5V	LVC 1.8V
$t_{PLH}$	A, B, or C	Y	MAX	4	5.9	7.6	17.5
$t_{PHL}$				4	5.9	7.6	17.5

UNIT: ns

## 2G00

### DUAL 2-INPUT POSITIVE-NAND GATE

●  $Y = \overline{A \cdot B}$

**FUNCTION TABLE**  
(each gate)

INPUTS	OUTPUT	
A	B	Y
H	H	L
L	X	H
X	L	H

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	LVC 5V	LVC 3.3V	LVC 2.5V	LVC 1.8V	AUC 2.5V	AUC 1.8V	UNIT
I <sub>CC</sub>	MAX	0.01	0.01	0.01	0.01	0.01	0.01	mA
I <sub>OH</sub>	MAX	-32	-24	-8	-4	-9	-8	mA
I <sub>OL</sub>	MAX	32	24	8	4	9	8	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	LVC 5V	LVC 3.3V	LVC 2.5V	LVC 1.8V	AUC 2.5V	AUC 1.8V
t <sub>PLH</sub>	A or B	Y	MAX	3.3	4.3	4.8	8.6	1.7	2.1
t <sub>PHL</sub>				3.3	4.3	4.8	8.6	1.7	2.1

UNIT:ns

## 2G02

### DUAL 2-INPUT POSITIVE-NOR GATE

●  $Y = \overline{A + B}$

**FUNCTION TABLE**  
(each gate)

INPUTS	OUTPUT	
A	B	Y
H	X	L
X	H	L
L	L	H

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

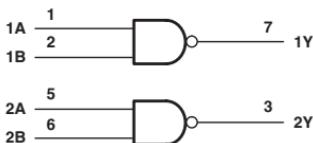
PARAMETER	MAX or MIN	LVC 5V	LVC 3.3V	LVC 2.5V	LVC 1.8V	AUC 2.5V	AUC 1.8V	UNIT
I <sub>CC</sub>	MAX	0.01	0.01	0.01	0.01	0.01	0.01	mA
I <sub>OH</sub>	MAX	-32	-24	-8	-4	-9	-8	mA
I <sub>OL</sub>	MAX	32	24	8	4	9	8	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	LVC 5V	LVC 3.3V	LVC 2.5V	LVC 1.8V	AUC 2.5V	AUC 1.8V
t <sub>PLH</sub>	A or B	Y	MAX	4.4	4.9	5.4	8.9	1.9	2.4
t <sub>PHL</sub>				4.4	4.9	5.4	8.9	1.9	2.4

UNIT:ns

### Logic Diagram

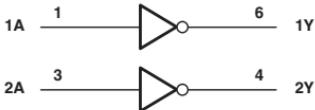


## 2G04

### DUAL INVERTER GATE

●  $Y = \overline{A}$

**Logic Diagram**



#### FUNCTION TABLE

(each inverter)

INPUT A	OUTPUT Y
H	L
L	H

#### ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	LVC 5V	LVC 3.3V	LVC 2.5V	LVC 1.8V	AUC 2.5V	AUC 1.8V	UNIT
I <sub>CC</sub>	MAX	0.01	0.01	0.01	0.01	0.01	0.01	mA
I <sub>OH</sub>	MAX	-32	-24	-8	-4	-9	-8	mA
I <sub>OL</sub>	MAX	32	24	8	4	9	8	mA

#### SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	LVC 5V	LVC 3.3V	LVC 2.5V	LVC 1.8V	AUC 2.5V	AUC 1.8V
I <sub>PLH</sub>	A	Y	MAX	3.2	4.1	4.4	8	1.5	2
I <sub>PHL</sub>				3.2	4.1	4.4	8	1.5	2

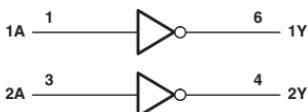
UNIT:ns

## 2GU04

### DUAL INVERTER GATE

●  $Y = \overline{A}$

**Logic Diagram**



#### FUNCTION TABLE

(each inverter)

INPUT A	OUTPUT Y
H	L
L	H

#### ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	LVC 5V	LVC 3.3V	LVC 2.5V	LVC 1.8V	AUC 2.5V	AUC 1.8V	UNIT
I <sub>CC</sub>	MAX	0.01	0.01	0.01	0.01	0.01	0.01	mA
I <sub>OH</sub>	MAX	-32	-24	-8	-4	-9	-8	mA
I <sub>OL</sub>	MAX	32	24	8	4	9	8	mA

#### SWITCHING CHARACTERISTICS

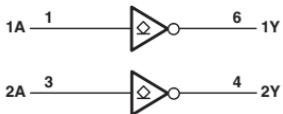
PARAMETER	INPUT	OUTPUT	MAX or MIN	LVC 5V	LVC 3.3V	LVC 2.5V	LVC 1.8V	AUC 2.5V	AUC 1.8V
I <sub>PLH</sub>	A	Y	MAX	3	3.7	4	5.5	2	2.7
I <sub>PHL</sub>				3	3.7	4	5.5	2	2.7

UNIT:ns

## 2G06

### DUAL INVERTER BUFFER/DRIVER WITH OPEN-DRAIN OUTPUTS

Logic Diagram



#### FUNCTION TABLE

(each inverter)

INPUT A	OUTPUT Y
H	L
L	H

#### ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	LVC 5V	LVC 3.3V	LVC 2.5V	LVC 1.8V	AUC 2.5V	AUC 1.8V	UNIT
I <sub>CC</sub>	MAX	0.01	0.01	0.01	0.01	0.01	0.01	mA
V <sub>O</sub>	MAX	5.5	5.5	5.5	5.5	3.6	3.6	V
I <sub>OL</sub>	MAX	32	24	8	4	9	8	mA

#### SWITCHING CHARACTERISTICS

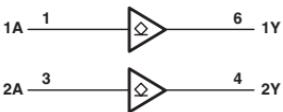
PARAMETER	INPUT	OUTPUT	MAX or MIN	LVC 5V	LVC 3.3V	LVC 2.5V	LVC 1.8V	AUC 2.5V	AUC 1.8V
				2.9	3.4	3.9	7.2	1.2	2.5
t <sub>PLH</sub>	A	Y	MAX	2.9	3.4	3.9	7.2	1.8	2.3
t <sub>PHL</sub>				2.9	3.4	3.9	7.2	1.8	2.3

UNIT:ns

## 2G07

### DUAL BUFFER/DRIVER WITH OPEN-DRAIN OUTPUTS

Logic Diagram



#### FUNCTION TABLE

(each buffer/drive)

INPUT A	OUTPUT Y
H	H
L	L

#### ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	LVC 5V	LVC 3.3V	LVC 2.5V	LVC 1.8V	AUC 2.5V	AUC 1.8V	UNIT
I <sub>CC</sub>	MAX	0.01	0.01	0.01	0.01	0.01	0.01	mA
V <sub>O</sub>	MAX	5.5	5.5	5.5	5.5	3.6	3.6	V
I <sub>OL</sub>	MAX	32	24	8	4	9	8	mA

#### SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	LVC 5V	LVC 3.3V	LVC 2.5V	LVC 1.8V	AUC 2.5V	AUC 1.8V
				2.9	3.7	4.4	8.6	1.2	2.5
t <sub>PLH</sub>	A	Y	MAX	2.9	3.7	4.4	8.6	1.8	2.3
t <sub>PHL</sub>				2.9	3.7	4.4	8.6	1.8	2.3

UNIT:ns

## 2G08

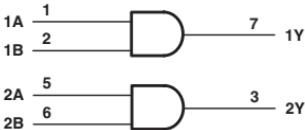
### DUAL 2-INPUT POSITIVE-AND GATE

●  $Y = A \cdot B$

**FUNCTION TABLE**  
(each gate)

INPUTS	OUTPUT	
A	B	Y
H	H	H
L	X	L
X	L	L

**Logic Diagram**



ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	LVC 5V	LVC 3.3V	LVC 2.5V	LVC 1.8V	AUC 2.5V	AUC 1.8V	UNIT
I <sub>CC</sub>	MAX	0.01	0.01	0.01	0.01	0.01	0.01	mA
I <sub>OH</sub>	MAX	-32	-24	-8	-4	-9	-8	mA
IoL	MAX	32	24	8	4	9	8	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	LVC 5V	LVC 3.3V	LVC 2.5V	LVC 1.8V	AUC 2.5V	AUC 1.8V
t <sub>PLH</sub>	A or B	Y	MAX	3.8	4.7	5.1	9	1.6	2.1
t <sub>PHL</sub>				3.8	4.7	5.1	9	1.6	2.1

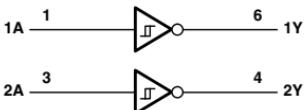
UNIT:ns

## 2G14

### DUAL SCHMITT-TRIGGER INVERTER

●  $Y = \bar{A}$

**Logic Diagram**



**FUNCTION TABLE**  
(each inverter)

INPUT	OUTPUT
A	Y
H	L
L	H

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	LVC 5V	LVC 3.3V	LVC 2.5V	LVC 1.8V	AUC 2.5V	AUC 1.8V	UNIT
I <sub>CC</sub>	MAX	0.01	0.01	0.01	0.01	0.01	0.01	mA
I <sub>OH</sub>	MAX	-32	-24	-8	-4	-9	-8	mA
IoL	MAX	32	24	8	4	9	8	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	LVC 5V	LVC 3.3V	LVC 2.5V	LVC 1.8V	AUC 2.5V	AUC 1.8V
t <sub>PLH</sub>	A	Y	MAX	4.3	5.4	5.7	9.5	TBD	TBD
t <sub>PHL</sub>				4.3	5.4	5.7	9.5	TBD	TBD

UNIT:ns

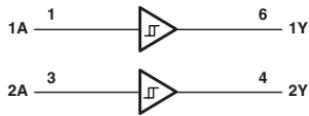
## 2G17

### DUAL SCHMITT-TRIGGER BUFFER

●  $Y = A$

**FUNCTION TABLE**  
(each inverter)

INPUT A	OUTPUT Y
H	H
L	L

**Logic Diagram**

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	LVC 5V	LVC 3.3V	LVC 2.5V	LVC 1.8V	UNIT
I <sub>cc</sub>	MAX	0.01	0.01	0.01	0.01	mA
I <sub>OH</sub>	MAX	-32	-24	-8	-4	mA
I <sub>OL</sub>	MAX	32	24	8	4	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	LVC 5V	LVC 3.3V	LVC 2.5V	LVC 1.8V
t <sub>PLH</sub>	A	Y	MAX	4.3	5.4	5.7	9.3
t <sub>PHL</sub>				4.3	5.4	5.7	9.3
UNIT:ns							

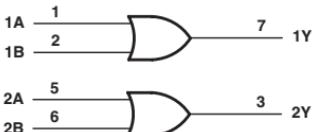
## 2G32

### DUAL 2-INPUT POSITIVE-OR GATE

●  $Y = A + B$

**FUNCTION TABLE**  
(each gate)

INPUTS		OUTPUT
A	B	Y
H	X	H
X	H	H
L	L	L

**Logic Diagram**

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	LVC 5V	LVC 3.3V	LVC 2.5V	LVC 1.8V	AUC 2.5V	AUC 1.8V	UNIT
I <sub>cc</sub>	MAX	0.01	0.01	0.01	0.01	0.01	0.01	mA
I <sub>OH</sub>	MAX	-32	-24	-8	-4	-9	-8	mA
I <sub>OL</sub>	MAX	32	24	8	4	9	8	mA

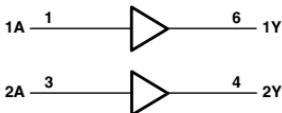
SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	LVC 5V	LVC 3.3V	LVC 2.5V	LVC 1.8V	AUC 2.5V	AUC 1.8V
t <sub>PLH</sub>	A or B	Y	MAX	3.2	3.8	4.4	8	1.7	2.1
t <sub>PHL</sub>				3.2	3.8	4.4	8	1.7	2.1
UNIT:ns									

## 2G34

### DUAL BUFFER GATE

- $Y = A$

**Logic Diagram**

**FUNCTION TABLE**  
(each gate)

INPUT A	OUTPUT Y
H	H
L	L

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	LVC 5V	LVC 3.3V	LVC 2.5V	LVC 1.8V	AUC 2.5V	AUC 1.8V	UNIT
$I_{CC}$	MAX	0.01	0.01	0.01	0.01	0.01	0.01	mA
$I_{OH}$	MAX	-32	-24	-8	-4	-9	-8	mA
$I_{OL}$	MAX	32	24	8	4	9	8	mA

SWITCHING CHARACTERISTICS

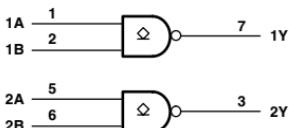
PARAMETER	INPUT	OUTPUT	MAX or MIN	LVC 5V	LVC 3.3V	LVC 2.5V	LVC 1.8V	AUC 2.5V	AUC 1.8V
$t_{PLH}$	A	Y	MAX	3.2	4.1	4.4	8.6	1.8	2.4
$t_{PHL}$				3.2	4.1	4.4	8.6	1.8	2.4

UNIT:ns

## 2G38

### SINGLE 2-INPUT NAND GATE WITH OPEN-DRAIN OUTPUT

- $Y = \overline{A \cdot B}$  or  $Y = \overline{A} + \overline{B}$

**Logic Diagram**

**FUNCTION TABLE**  
(each gate)

INPUTS A B	OUTPUT Y
L L	H
L H	H
H L	H
H H	L

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	LVC 5V	LVC 3.3V	LVC 2.5V	LVC 1.8V	UNIT
$I_{CC}$	MAX	0.01	0.01	0.01	0.01	mA
$V_O$	MAX	5.5	5.5	5.5	5.5	mA
$I_{OL}$	MAX	32	24	8	4	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	LVC 5V	LVC 3.3V	LVC 2.5V	LVC 1.8V
$t_{PLH}$	A or B	Y	MAX	3.9	4.5	6	10
$t_{PHL}$				3.9	4.5	6	10

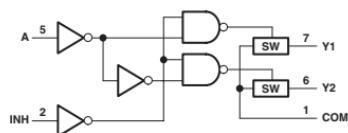
UNIT : ns

## 2G53

### SINGLE-POLE DOUBLE-THROW (SPDT) ANALOG SWITCH 2:1 ANALOG MULTIPLEXER/DEMULTIPLEXER

- High On-Off Outputs Voltage Ratio
- High Degree of Linearity

Logic Diagram



FUNCTION TABLE

CONTROL INPUTS	ON CHANNEL
INH	A
L	L
L	H
H	X

Y1  
Y2  
None

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	LVC 5V	LVC 3.3V	LVC 2.5V	LVC 1.8V	AUC 2.5V	AUC 1.8V	UNIT
I <sub>CC</sub>	MAX	0.001	0.001	0.001	0.001	0.01	0.01	mA
R <sub>ON</sub>	MAX	13	17	20	30	15	20	mA
R <sub>ON(P)</sub>	MAX	15	20	30	120	20	80	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	LVC 5V	LVC 3.3V	LVC 2.5V	LVC 1.8V	AUC 2.5V	AUC 1.8V
I <sub>PZH</sub>	COM or Y	Y or COM	MAX	0.6	0.8	1.2	2	0.2	0.4
I <sub>PHL</sub>				0.6	0.8	1.2	2	0.2	0.4
I <sub>PZL</sub>	INH	COM or Y	MAX	4.5	5.4	6.1	9	2.2	3.1
I <sub>PHZ</sub>				4.5	5.4	6.1	9	2.2	3.1
I <sub>PLZ</sub>	A	COM or Y	MAX	8	8.1	8.3	10.9	2.2	3.4
I <sub>PZH</sub>				8	8.1	8.3	10.9	2.2	3.4
I <sub>PHL</sub>	A	COM or Y	MAX	5.4	5.8	7.2	10.3	2.2	3.0
I <sub>PZL</sub>				5.4	5.8	7.2	10.3	2.2	3.0
I <sub>PHZ</sub>	A	COM or Y	MAX	5	7.2	7.9	9.4	2.3	3.0
I <sub>PLZ</sub>				5	7.2	7.9	9.4	2.3	3.0

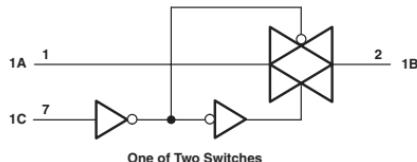
UNIT: ns

## 2G66

### DUAL BILATERAL ANALOG SWITCH

- High On-Off Outputs Voltage Ratio
- High Degree of Linearity
- Rail-to-Rail Input/Output

Logic Diagram, each switch



### FUNCTION TABLE (each section)

CONTROL INPUT (C)	SWITCH1
L	OFF
H	ON

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	LVC 5V	LVC 3.3V	LVC 2.5V	LVC 1.8V	AUC 2.5V	AUC 1.8V	UNIT
I <sub>CC</sub>	MAX	0.01	0.01	0.01	0.01	0.01	0.01	mA
R <sub>ON</sub>	MAX	10	15	20	30	15	20	mA
R <sub>ON(P)</sub>	MAX	15	20	30	120	20	80	mA

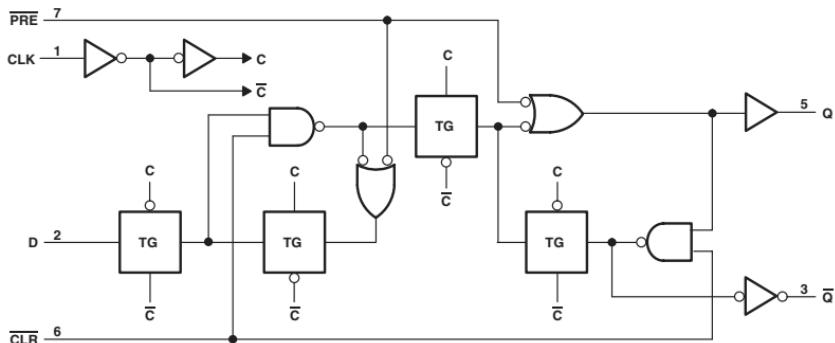
SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	LVC 5V	LVC 3.3V	LVC 2.5V	LVC 1.8V	AUC 2.5V	AUC 1.8V
I <sub>PZH</sub>	A or B	B or A	MAX	0.6	0.8	1.2	2	0.7	0.7
I <sub>PHL</sub>				0.6	0.8	1.2	2	0.7	0.7
I <sub>PZL</sub>	C	A or B	MAX	3.9	4.4	5.6	10	2.3	2.7
I <sub>PHZ</sub>				3.9	4.4	5.6	10	2.3	2.7
I <sub>PLZ</sub>	C	A or B	MAX	6.3	7.2	6.9	10.5	2	3.4
I <sub>PZH</sub>				6.3	7.2	6.9	10.5	2	3.4

UNIT: ns

## SINGLE POSITIVE-EDGE-TRIGGERED D-TYPE FLIP-FLOP WITH CLEAR AND PRESET

Logic Diagram



FUNCTION TABLE

INPUTS			OUTPUTS	
PRE	CLR	CLK	D	Q      Q̄
L	H	X	X	H      L
H	L	X	X	L      H
L	L	X	X	H†      H†
H	H	↑	H	H      L
H	H	L	L	L      H
H	H	L	X	Q <sub>0</sub> Q̄ <sub>0</sub>

† This configuration is nonstable; that is, it does not persist when PRE or CLR returns to its inactive (high) level.

## ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	LVC 5V	LVC 3.3V	LVC 2.5V	LVC 1.8V	UNIT
I <sub>CC</sub>	MAX	0.01	0.01	0.01	0.01	mA
I <sub>OH</sub>	MAX	-32	-16	-8	-4	mA
I <sub>OL</sub>	MAX	32	16	8	4	mA

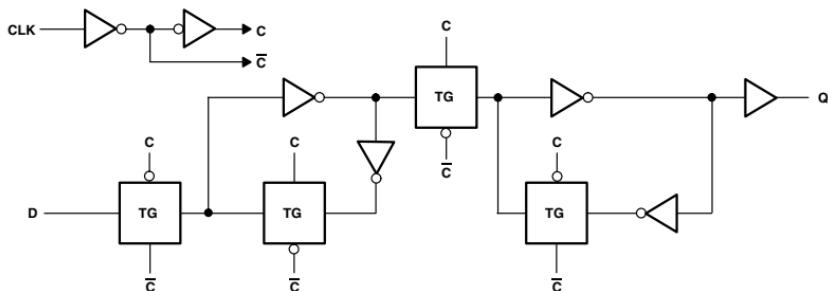
## TIMING REQUIREMENTS AND SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	LVC 5V	LVC 3.3V	LVC 2.5V	LVC 1.8V
f <sub>max</sub>			MIN	200	175	175	80
t <sub>w</sub>	CLK		MIN	2	2.7	2.7	6.2
	PRE or CLR low			2	2.7	2.7	6.2
t <sub>su</sub>	Data		MIN	1.1	1.3	1.7	2.9
	PRE or CLR inactive			1	1.2	1.4	1.9
t <sub>th</sub>			MIN	0.5	1.2	0.3	0
t <sub>PLH</sub>	CLK	Q	MAX	4.1	5.9	7.1	13.4
				4.1	5.9	7.1	13.4
t <sub>PHL</sub>	CLK	Q̄	MAX	4.4	6.2	7.7	14.4
				4.4	6.2	7.7	14.4
t <sub>PLH</sub>	PRE or CLR	Q or Q̄	MAX	4.1	5.9	7	12.9
				4.1	5.9	7	12.9

UNIT: ns

## DUAL POSITIVE-EDGE-TRIGGERED D-TYPE FLIP-FLOP

Logic Diagram



## FUNCTION TABLE

INPUTS	OUTPUT	
CLK	D	Q
↑ H	H	H
↑ L	L	L
L X	Q <sub>0</sub>	

## ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	LVC 5V	LVC 3.3V	LVC 2.5V	LVC 1.8V	AUC 2.5V	AUC 1.8V	UNIT
I <sub>CC</sub>	MAX	0.005	0.005	0.005	0.005	0.01	0.01	mA
I <sub>DH</sub>	MAX	-32	-24	-8	-4	-9	-8	mA
I <sub>OL</sub>	MAX	32	24	8	4	9	8	mA

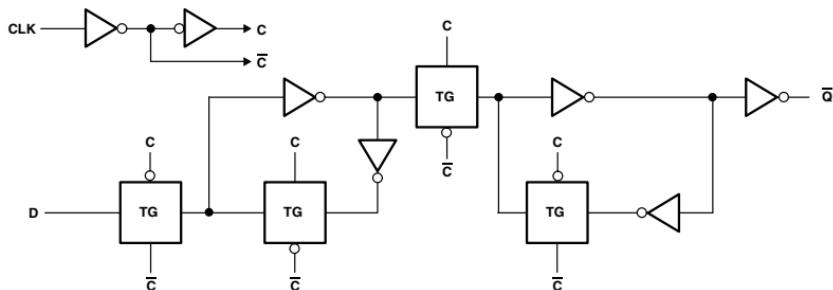
## TIMING REQUIREMENTS AND SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	LVC 5V	LVC 3.3V	LVC 2.5V	LVC 1.8V	AUC 2.5V	AUC 1.8V
				MIN	160	160	160	160	275
t <sub>max</sub>			MIN	160	160	160	160	275	250
t <sub>W</sub>	CLK high or low		MIN	2.5	2.5	2.5	2.5	1	1
t <sub>SU</sub>	Before CLK ↑, Data high		MIN	0.9	1.1	1.4	2.2	0.5	0.6
	Before CLK ↑, Data low			0.9	1.1	1.4	2.2	0.5	0.6
t <sub>th</sub>	Data after CLK ↑		MIN	0.5	0.7	0.8	1.4	0.1	0.1
t <sub>PLH</sub>	CLK	Q	MAX	4.5	5.2	7.0	9.9	1.8	2.4
t <sub>PHL</sub>				4.5	5.2	7.0	9.9	1.8	2.4

UNIT f<sub>max</sub> : MHz other : ns

## DUAL POSITIVE-EDGE-TRIGGERED D-TYPE FLIP-FLOP

Logic Diagram

FUNCTION TABLE  
(each flip-flop)

INPUTS	OUTPUT	
CLK	D	Q
↑ H	L	L
↑ L	H	H
L X	Q <sub>0</sub>	Q <sub>0</sub>

## ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	LVC 5V	LVC 3.3V	LVC 2.5V	LVC 1.8V	AUC 2.5V	AUC 1.8V	UNIT
I <sub>CC</sub>	MAX	0.005	0.005	0.005	0.005	0.01	0.01	mA
I <sub>OH</sub>	MAX	-32	-24	-8	-4	-9	-8	mA
I <sub>OL</sub>	MAX	32	24	8	4	9	8	mA

## TIMING REQUIREMENTS AND SWITCHING CHARACTERISTICS

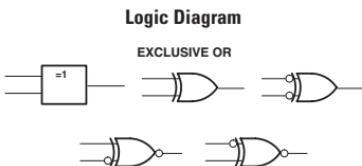
PARAMETER	INPUT	OUTPUT	MAX or MIN	LVC 5V	LVC 3.3V	LVC 2.5V	LVC 1.8V	AUC 2.5V	AUC 1.8V
f <sub>max</sub>			MIN	160	160	160	160	275	250
t <sub>w</sub>	CLK high or low		MIN	2.5	2.5	2.5	2.5	1	1
t <sub>su</sub>	Before CLK ↑, Data high		MIN	0.9	1.1	1.4	2.2	0.5	0.6
	Before CLK ↑, Data low			0.9	1.1	1.4	2.2	0.5	0.6
t <sub>th</sub>	Data after CLK ↑		MIN	0.6	0.8	1.0	1.6	0.5	0.1
t <sub>plh</sub>	CLK	Q̄	MAX	4.5	5.2	7.0	13.9	1.8	2.4
t <sub>phl</sub>				4.5	5.2	7.0	13.9	1.8	2.4

UNIT f<sub>max</sub> : MHz other : ns

## 2G86

### DUAL 2-INPUT EXCLUSIVE-OR GATE

- $Y = A \oplus B$



#### FUNCTION TABLE

(each gate)

INPUTS	OUTPUT	
A	B	Y
L	L	L
L	H	H
H	L	H
H	H	L

An exclusive-OR gate has many applications, some of which can be represented better by alternative logic symbols.

#### ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	LVC 5V	LVC 3.3V	LVC 2.5V	LVC 1.8V	AUC 2.5V	AUC 1.8V	UNIT
$I_{CC}$	MAX	0.01	0.01	0.01	0.01	0.01	0.01	mA
$I_{OH}$	MAX	-32	-24	-8	-4	-9	-8	mA
$I_{OL}$	MAX	32	24	8	4	9	8	mA

#### SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	LVC 5V	LVC 3.3V	LVC 2.5V	LVC 1.8V	AUC 2.5V	AUC 1.8V
$t_{PLH}$	A or B	Y	MAX	3.6	4.7	5.7	9.9	2.0	2.6
$t_{PHL}$				3.6	4.7	5.7	9.9	2.0	2.6

UNIT:ns

## 2G125

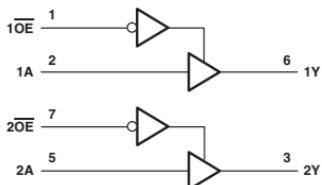
### DUAL BUS BUFFER GATE WITH 3-STATE OUTPUTS

#### FUNCTION TABLE

(each buffer)

INPUTS	OUTPUT	
OE	A	Y
L	H	H
L	L	L
H	X	Z

#### Logic Diagram



#### ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	LVC 5V	LVC 3.3V	LVC 2.5V	LVC 1.8V	AUC 2.5V	AUC 1.8V	UNIT
$I_{CC}$	MAX	0.01	0.01	0.01	0.01	0.01	0.01	mA
$I_{OH}$	MAX	-32	-24	-8	-4	-9	-8	mA
$I_{OL}$	MAX	32	24	8	4	9	8	mA

#### SWITCHING CHARACTERISTICS

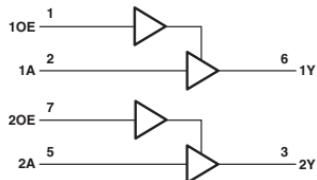
PARAMETER	INPUT	OUTPUT	MAX or MIN	LVC 5V	LVC 3.3V	LVC 2.5V	LVC 1.8V	AUC 2.5V	AUC 1.8V
$t_{PLH}$	A	Y	MAX	3.7	4.3	4.8	9.1	1.8	2.6
$t_{PHL}$				3.7	4.3	4.8	9.1	1.8	2.6
$t_{PZH}$	$\overline{OE}$	Y	MAX	3.8	4.7	5.6	9.9	2.2	2.9
$t_{PZL}$	$\overline{OE}$	Y	MAX	3.8	4.7	5.6	9.9	2.2	2.9
$t_{PHZ}$	$\overline{OE}$	Y	MAX	3.4	4.6	5.8	11.6	2	3.6
$t_{PLZ}$	$\overline{OE}$	Y	MAX	3.4	4.6	5.8	11.6	2	3.6

UNIT:ns

## 2G126

### DUAL BUS BUFFER GATE WITH 3-STATE OUTPUTS

Logic Diagram



#### FUNCTION TABLE (each buffer)

INPUTS	OUTPUT	
OE	A	Y
H	H	H
H	L	L
L	X	Z

#### ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	LVC 5V	LVC 3.3V	LVC 2.5V	LVC 1.8V	AUC 2.5V	AUC 1.8V	UNIT
I <sub>CC</sub>	MAX	0.01	0.01	0.01	0.01	0.01	0.01	mA
I <sub>OH</sub>	MAX	-32	-24	-8	-4	-9	-8	mA
I <sub>OL</sub>	MAX	32	24	8	4	9	8	mA

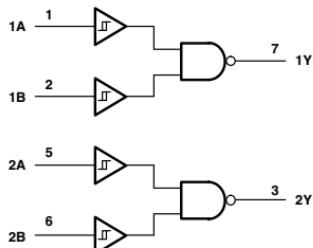
#### SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	LVC 5V	LVC 3.3V	LVC 2.5V	LVC 1.8V	AUC 2.5V	AUC 1.8V
t <sub>PLH</sub>	A	Y	MAX	3.2	4	4.9	9.8	1.8	2.3
t <sub>PHL</sub>				3.2	4	4.9	9.8	1.8	2.3
t <sub>PZH</sub>	OE	Y	MAX	3.1	4.1	5	10	2.2	2.4
t <sub>PZL</sub>				3.1	4.1	5	10	2.2	2.4
t <sub>PHZ</sub>	OE	Y	MAX	3.3	4.4	5.7	12.6	1.8	3.3
t <sub>PZL</sub>				3.3	4.4	5.7	12.6	1.8	3.3
UNIT: ns									

## 2G132

### DUAL 2-INPUT NAND GATE WITH SCHMITT-TRIGGER INPUT

Logic Diagram



#### FUNCTION TABLE (each gate)

INPUTS	OUTPUT	
A	B	Y
L	L	H
L	H	H
H	L	H
H	H	L

#### ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	LVC 5V	LVC 3.3V	LVC 2.5V	LVC 1.8V	UNIT
I <sub>CC</sub>	MAX	0.01	0.01	0.01	0.01	mA
I <sub>OH</sub>	MAX	-32	-24	-8	-4	mA
I <sub>OL</sub>	MAX	32	24	8	4	mA

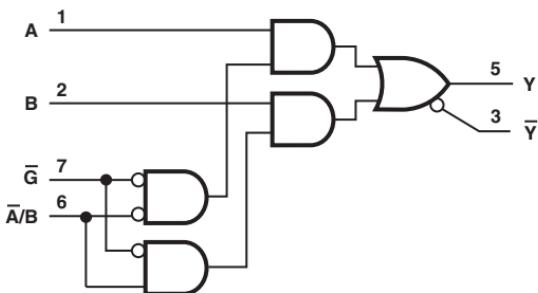
#### SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	LVC 5V	LVC 3.3V	LVC 2.5V	LVC 1.8V
t <sub>PLH</sub>	A or B	Y	MAX	5	6	7.5	16
t <sub>PHL</sub>				5	6	7.5	16

UNIT: ns

## SINGLE 2-LINE TO 1-LINE DATA SELECTOR/MULTIPLEXER

Logic Diagram



FUNCTION TABLE

INPUTS			OUTPUTS		
$\bar{G}$	$\bar{A}/B$	A	B	Y	$\bar{Y}$
H	X	X	X	L	L
L	L	L	X	L	H
L	L	H	X	H	L
L	H	X	L	L	H
L	H	X	H	H	L

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	LVC 5V	LVC 3.3V	LVC 2.5V	LVC 1.8V	UNIT
$I_{CC}$	MAX	0.01	0.01	0.01	0.01	mA
$I_{OH}$	MAX	-32	-24	-8	-4	mA
$I_{OL}$	MAX	32	24	8	4	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	LVC 5V	LVC 3.3V	LVC 2.5V	LVC 1.8V
$t_{PLH}$	A or B	$Y$ or $\bar{Y}$	MAX	4	6	8	14
$t_{PHL}$				4	6	8	14
$t_{PLH}$	$\bar{A}/B$	$Y$ or $\bar{Y}$	MAX	4	6	9	16
$t_{PHL}$				4	6	9	16
$t_{PLH}$	$\bar{G}$	$Y$ or $\bar{Y}$	MAX	4	6	8	14
$t_{PHL}$				4	6	8	14

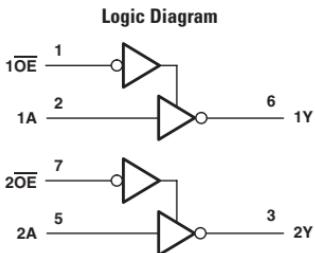
UNIT:ns

## 2G240

### DUAL BUFFERS/DRIVERS WITH 3-STATE OUTPUTS

#### FUNCTION TABLE (each buffer)

INPUTS	OUTPUT	
OE	A	Y
L	H	L
L	L	H
H	X	Z



#### ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	LVC 5V	LVC 3.3V	LVC 2.5V	LVC 1.8V	AUC 2.5V	AUC 1.8V	UNIT
I <sub>CC</sub>	MAX	0.01	0.01	0.01	0.01	0.01	0.01	mA
I <sub>OH</sub>	MAX	-32	-24	-8	-4	-9	-8	mA
I <sub>OL</sub>	MAX	32	24	8	4	9	8	mA

#### SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	LVC 5V	LVC 3.3V	LVC 2.5V	LVC 1.8V	AUC 2.5V	AUC 1.8V
I <sub>PLH</sub>	A	Y	MAX	4	4.6	5.5	11.3	1.7	2.5
I <sub>PHL</sub>				4	4.6	5.5	11.3	1.7	2.5
I <sub>PZH</sub>	OE	Y	MAX	5	5.4	6.6	11.7	2.1	3.1
I <sub>PZL</sub>				5	5.4	6.6	11.7	2.1	3.1
I <sub>PLZ</sub>	OE	Y	MAX	4.2	5.5	5.7	12.8	1.9	3.7
I <sub>PHZ</sub>				4.2	5.5	5.7	12.8	1.9	3.7

UNIT:ns

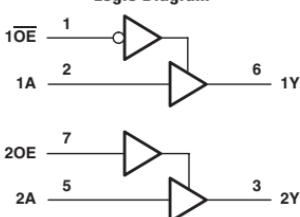
## 2G241

### DUAL BUFFER/DRIVER WITH 3-STATE OUTPUTS

#### FUNCTION TABLE

INPUTS	OUTPUT	INPUTS	OUTPUT
OE	1A	2OE	2Y
L	H	H	H
L	L	H	L
H	X	L	Z

#### Logic Diagram



#### ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	LVC 5V	LVC 3.3V	LVC 2.5V	LVC 1.8V	AUC 2.5V	AUC 1.8V	UNIT
I <sub>CC</sub>	MAX	0.01	0.01	0.01	0.01	0.01	0.01	mA
I <sub>OH</sub>	MAX	-32	-24	-8	-4	-9	-8	mA
I <sub>OL</sub>	MAX	32	24	8	4	9	8	mA

#### SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	LVC 5V	LVC 3.3V	LVC 2.5V	LVC 1.8V	AUC 2.5V	AUC 1.8V
I <sub>PLH</sub>	A	Y	MAX	3.7	4.3	4.8	8.8	1.8	2.5
I <sub>PHL</sub>				3.7	4.3	4.8	8.8	1.8	2.5
I <sub>PZH</sub>	OE	Y	MAX	3.8	4.7	5.6	9.9	2	2.8
I <sub>PZL</sub>				3.8	4.7	5.6	9.9	2	2.8
I <sub>PLZ</sub>	OE	Y	MAX	3.4	4.4	5.8	11.6	2.1	3.6
I <sub>PHZ</sub>				3.4	4.4	5.8	11.6	2.1	3.6
I <sub>PZL</sub>	OE	Y	MAX	3.3	4.1	4.7	8.8	2	2.8
I <sub>PZH</sub>				3.3	4.1	4.7	8.8	2	2.8
I <sub>PLZ</sub>	OE	Y	MAX	3.3	4.2	5.2	12.5	2.1	8.6
I <sub>PHZ</sub>				3.3	4.2	5.2	12.5	2.1	8.6

UNIT:ns

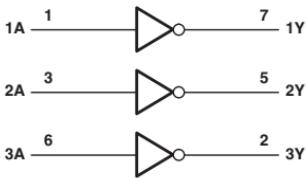
## 3G04

### TRIPLE INVERTER GATE

$$\bullet Y = \overline{A}$$

**FUNCTION TABLE**  
(each inverter)

INPUT A	OUTPUT Y
H	L
L	H

**Logic Diagram**

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	LVC 5V	LVC 3.3V	LVC 2.5V	LVC 1.8V	UNIT
I <sub>CC</sub>	MAX	0.01	0.01	0.01	0.01	mA
I <sub>OH</sub>	MAX	-32	-24	-8	-4	mA
I <sub>OL</sub>	MAX	32	24	8	4	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	LVC 5V	LVC 3.3V	LVC 2.5V	LVC 1.8V
t <sub>PLH</sub>	A	Y	MAX	3.2	4.1	4.4	7.9
t <sub>PHL</sub>				3.2	4.1	4.4	7.9

UNIT:ns

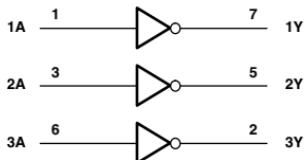
## 3GU04

### TRIPLE INVERTER GATE

$$\bullet Y = \overline{A}$$

**FUNCTION TABLE**  
(each inverter)

INPUT A	OUTPUT Y
H	L
L	H

**Logic Diagram**

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	LVC 5V	LVC 3.3V	LVC 2.5V	LVC 1.8V	UNIT
I <sub>CC</sub>	MAX	0.01	0.01	0.01	0.01	mA
I <sub>OH</sub>	MAX	-32	-24	-8	-4	mA
I <sub>OL</sub>	MAX	32	24	8	4	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	LVC 5V	LVC 3.3V	LVC 2.5V	LVC 1.8V
t <sub>PLH</sub>	A	Y	MAX	3.2	3.9	4	9.2
t <sub>PHL</sub>				3.2	3.9	4	9.2

UNIT : ns

## 3G06

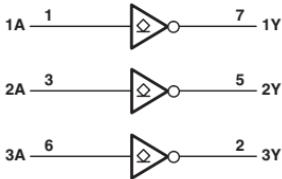
### TRIPLE INVERTER BUFFER/DRIVER WITH OPEN-DRAIN OUTPUTS

#### FUNCTION TABLE

(each inverter)

INPUT A	OUTPUT Y
H	L
L	H

#### Logic Diagram



#### ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	LVC 5V	LVC 3.3V	LVC 2.5V	LVC 1.8V	UNIT
I <sub>CC</sub>	MAX	0.01	0.01	0.01	0.01	mA
V <sub>O</sub>	MAX	5.5	5.5	5.5	5.5	mA
I <sub>OL</sub>	MAX	32	24	8	4	mA

#### SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	LVC 5V	LVC 3.3V	LVC 2.5V	LVC 1.8V
I <sub>PLH</sub>	A	Y	MAX	2.9	3.4	3.9	7.2
I <sub>PHL</sub>				2.9	3.4	3.9	7.2

UNIT:ns

## 3G07

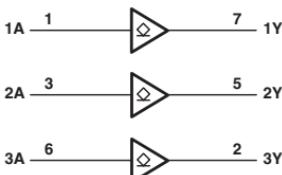
### TRIPLE BUFFER/DRIVER WITH OPEN-DRAIN OUTPUTS

#### FUNCTION TABLE

(each buffer/driver)

INPUT A	OUTPUT Y
H	H
L	L

#### Logic Diagram



#### ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	LVC 5V	LVC 3.3V	LVC 2.5V	LVC 1.8V	UNIT
I <sub>CC</sub>	MAX	0.01	0.01	0.01	0.01	mA
V <sub>O</sub>	MAX	5.5	5.5	5.5	5.5	mA
I <sub>OL</sub>	MAX	32	24	8	4	mA

#### SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	LVC 5V	LVC 3.3V	LVC 2.5V	LVC 1.8V
I <sub>PLH</sub>	A	Y	MAX	2.9	3.7	4.3	7.8
I <sub>PHL</sub>				2.9	3.7	4.3	7.8

UNIT:ns

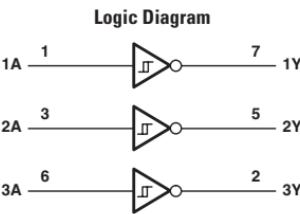
## 3G14

### TRIPLE SCHMITT-TRIGGER INVERTER

●  $Y = \bar{A}$

#### FUNCTION TABLE (each inverter)

INPUT A	OUTPUT Y
H	L



#### ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	LVC 5V	LVC 3.3V	LVC 2.5V	LVC 1.8V	UNIT
$I_{CC}$	MAX	0.01	0.01	0.01	0.01	mA
$I_{OH}$	MAX	-32	-24	-8	-4	mA
$I_{OL}$	MAX	32	24	8	4	mA

#### SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	LVC 5V	LVC 3.3V	LVC 2.5V	LVC 1.8V
$t_{PLH}$	A	Y	MAX	4.3	5.4	5.7	9.2
$t_{PHL}$				4.3	5.4	5.7	9.2

UNIT:ns

## 3G17

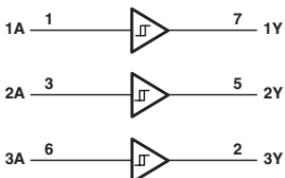
### TRIPLE SCHMITT-TRIGGER BUFFER

●  $Y = A$

#### FUNCTION TABLE

INPUT A	OUTPUT Y
H	H

#### Logic Diagram



#### ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	LVC 5V	LVC 3.3V	LVC 2.5V	LVC 1.8V	UNIT
$I_{CC}$	MAX	0.01	0.01	0.01	0.01	mA
$I_{OH}$	MAX	-32	-24	-8	-4	mA
$I_{OL}$	MAX	32	24	8	4	mA

#### SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	LVC 5V	LVC 3.3V	LVC 2.5V	LVC 1.8V
$t_{PLH}$	A	Y	MAX	4.1	5.4	6.2	9.2
$t_{PHL}$				4.1	5.4	6.2	9.2

UNIT:ns

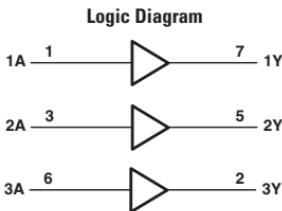
# 3G34

## TRIPLE BUFFER GATE

- $Y = A$

### FUNCTION TABLE (each gate)

INPUT A	OUTPUT Y
H	H
L	L



### ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	LVC 5V	LVC 3.3V	LVC 2.5V	LVC 1.8V	UNIT
$I_{CC}$	MAX	0.01	0.01	0.01	0.01	mA
$ I_{OH} $	MAX	-32	-24	-8	-4	mA
$ I_{OL} $	MAX	32	24	8	4	mA

### SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	LVC 5V	LVC 3.3V	LVC 2.5V	LVC 1.8V
$t_{PLH}$	A	Y	MAX	3.2	4.1	4.4	7.9
$t_{PHL}$				3.2	4.1	4.4	7.9

UNIT:ns



# **FUNCTION**

**Standard**



**GATE (AND / NAND / OR / NOR)**

Description	No. of Input	Circuit	Input	Output	Device	Technology																	
						Bipolar						CMOS				BiCMOS		Advanced CMOS					
						TTL	LS	S	ALS	AS	F	HC	HCT	BCT	ABT	LVT	ALVT	AC	ACT	AHC	AHCT		
POS-AND	2	4			08	×	●	●	●	●	●	●	●	●	●	●	●	●	●	●			
			OC		09	×	●	●	●	●	●	●	●	X/-				●	●	●	●		
			OC		15	×	×	×															
			BUF		1008				X/A	●A													
			SCH		7001																		
	3	6	BUF		808				X/B	X/-													
			BUF		1808				X	X													
					11	●	×	●A	●	●	●	●	●	-/-			X/-	X/-	X/-	X/-			
					1011				X														
					21	●	●	●A	●	●	●	●	●	X/-			X/-	X/-	X/-	X/-			
POS-NAND	2	4			8003				X	●													
			00	●	●	●	●A	●	●	●	●	●	●	●			●	●	●A	●A	●		
			01	×	OC				X														
			03	×	OC	●	●	●B															
			SCH		24	×																	
			OC		26	×	●																
			BUF		37	×	●	●	●A	X													
			OC		38	●	●	●	●B	●													
			SCH		132	×	●	●															
			BUF		1000				X/A	●A								X/-	X/-	●	●	●A	
	3	6	OC		1003				X/A														
			SCH	OC	7003																		
			OC		39	X																	
			BUF		804				●A	●B	X/-												
			BUF		1804				X/A	X													
					10	●	●	●	●A	●	●	●	●	●	-/-			X/-	X/-	●A	●A	●	
			OC		12	×	X											X/-	X/-	●	●		
			BUF		1010				X														
POS-OR	4	2	SCH		13	X	X											X/-	-X/-				
			SCH		18	X																	
					20	×	●	●	●A	●	●	●	●	●	-/-		X/X/●	X/X/●	●	●	●A		
			OC		22	×	X	X	X									X/X/●	X/X/●				
			BUF		40	×	X	X	X	X													
			BUF		140	●																	
			BUF		1020				X														
			SCH		618	X																	
					30	●	●	●A	●	●	●	●	●	●	-/-		X/H	X/H					
					12	1	3S				X												
	3	3			134	X												X/-	X/H				
					133	X	●																
POS-NOR	2	4			32	●	●	●	●	●	●	●	●	●	●	●		●	●	●	●A	●A	●
			BUF		1032				X	●A													
			SCH		7032																		
			BUF		832				●A	●B	X/-												
			BUF		1832				X/A	X													
	3	6			4075													X/-	-/-				
					02	●	●	●	●A	●	●	●	●	●	●	●		X/H	X/H	●	●	●A	●A
			BUF		28	×	X																
			OC		33	×	●	●A															
					36																		
			BUF		128	●																	
			BUF		1002				X/A														
			SCH		7002																		
			BUF		1036				X/A														
			BUF		805				●A	●B	X/-												
POS-NOR	2	4	BUF		1805				X	X													
					27	×	●	●A	●	●	●	●	●	●	-/-			X/H	X/H	●	●		
					23	X																	
					25	●																	
					4002																		
	3	2			260	●																	

Explanatory notes [Input] SCH: Schmitt-Trigger Inputs

Explanatory notes [Output] BUF: Buffered Output OC: Open-Collector Output

●: Product available in technology indicated \*: New product planned in technology indicated

✗: Discontinued ■: Not recommended for new designs

HC: SN74HCxx / CD74HCxx

HCT: SN74HCxx / CD74HCTxx

BCT: SN74BCTxx / SN64BCTxx

AC: 74AC11xx (Product available in reduced-noise advanced CMOS: 11000 Series) / SN74ACxx / CD74ACxx

ACT: 74ACT11xx (Product available in reduced-noise advanced CMOS: 11000 Series) / SN74ACTxx / CD74ACTxx

**GATE (EX-OR / EX-NOR / INVERTER / NONINVERTER / etc.)**

Description	No. of Input	Circuit	Input	Output	Device	Technology																					
						Bipolar				CMOS				BiCMOS			Advanced CMOS			Low-Voltage CMOS							
						TTL	LS	S	ALS	AS	F	HC	HCT	BCT	ABT	LVT	ALVT	AC	ACT	AHC	AHCT	LV	LVC	ALVC	AVC	AUC	
EX-OR	2	4		OC		86	X	●A	●	●	●A	●	●/●	✓/●			●/●	●/●	●	●	●A	●A					
						135	X	●	●	●	●	●	✓/●														
						365	X						X/-														
EX-NOR	2	4		OC		266	●																				
						810							X/-														
						OC							X/-														
						811							X/-														
						7266							X/-														
EX-OR/NOR	2	4				135		X																			
INVERTING	1	6				04	●	●	●	●B	●	●	●/●	●/●			●/●	●/●	●/●	●	●A	●A	●	●	●		
						OC	05	●	●	●	●A	●	●/●				✓/●	✓/●	●	●A	●A	●	●	●	●		
						OC	06	●	●	●	●	●	●/●														
						SCH	14	●	●	●	●	●	●/●	✓/●			✓/●	✓/●	●	●A	●A	●	●	●			
						OC	16	●	●X																		
						SCH	19	●																			
						BUF	1004	X		●	●A																
						OC	1005	X		●																	
							4049						-/●														
							U04						●/●														
NON-INVERTING	1	4				619	X																				
							425	X																			
							426	X																			
						OC	07	●	●																		
						OC	17	●																			
							34						X/-														
						OC	35						●A														
						BUF	1034						●A														
						OC	1035						●														
							4050						-/●														
OTHER		6	1	6		63	X																				
			2	6		31	●																				
						50	X																				
			4	2		51	X	●	●				X/-														
						60	X																				
						53	X																				
						55	X																				
						4078																					
						54	X	X																			
						64	X																				
						OC	65	X																			
						BUF	800																				
						BUF	802																				
							7096																				
						7098																					
						7074																					
						7075																					
						7076																					

Explanatory notes [Input] SCH: Schmitt-Trigger Inputs

Explanatory notes [Output] BUF: Buffered Output OC: Open-Collector Output

Status ●: Product available in technology indicated \*: New product planned in technology indicated

X: Discontinued ■: Not recommended for new designs

HC: SN74HCxx / CD74HCxx

HCT: SN74HCTxx / CD74HCTxx

BCT: SN74BCTxx / SN64BCTxx

AC: 74AC1xxx (Product available in reduced-noise advanced CMOS: 11000 Series) / SN74ACxx / CD74ACxx

ACT: 74ACT11xxx (Product available in reduced-noise advanced CMOS: 11000 Series) / SN74ACTxx / CD74ACTxx

## BUFFER / DRIVER (NON-INVERTING)

Description	No. of Output	Output	Device	Technology																					
				Bipolar				CMOS				BiCMOS				Advanced CMOS									
				TTL	LS	S	ALS	AS	F	HC	HCT	BCT	ABT	LVT	ALVT	AC	ACT	AHC	AHCT	LV	LV-AT	LVC	ALVC	AVC	AUC
NON-INVERTING	4	3S	125	X	●A					●	●/●	●/●	●/●A	●	H●			●	●	●A	●	●A	●	●	
	6	3S	126	X	●A					●	●/●	●/●	●/●A	●	H●			●	●	●A	●	●A	●	●	
	3S	365	X	●A						●	●/●														
	3S	367	X	●A						●	●/●														
	3S	241		●	●	●C	●A	●		X/●	●/●	●/●	●A	H●	X/●-	X/●/●							-		
	3S	244		●	●	●C1	●A	●		●	●/●	●/●	●/●	●A	●B	H●A	●/●/●	●/●/●	●	●	●A	●A	●B	H●	
	3S	455																							
	3S	465																							
	3S	467			X	X																			
	3S	541																							
NON-INVERTING	8	3S	656																						
	3S	747																							
	OC	757																							
	OC	760																							
	3S	1241																							
	3S	1244																							
	R3S	2241																							
	R3S	2244																							
	R3S	2541																							
	3S	25241																							
NON-INVERTING	10	3S	25244																						
	3S	25757																							
	3S	25760																							
	3S	827																							
	R3S	2827																							
	3S	29287																							
	11	R3S	5400																						
	12	R3S	5402																						
	R3S	16903																							
	3S	16241																							
NON-INVERTING	16	3S	16244																						
	3S	16541																							
	R3S	162241																							
	R3S	162244																							
	R3S	162541																							
	3S	16825																							
	R3S	162825																							
	18	3S	16835																						
	R3S	162835																							
	20	3S	16827																						
32	3S	162827																							
	3S	32244																							
	R3S	32244																							

Explanatory notes [Output] 3S: 3-State Output R3S: Series Resistor and 3-State Output OC: Open-Collector Output

Status ●: Product available in technology indicated ■: New product planned in technology indicated

X: Discontinued ■: Not recommended for new designs

HC: SN74HCxx / CD74HCxx

HCT: SN74HCTxx / CD74HCTxx

BCT: SN74BCTx / SN64BCTx

AC: 74AC11xxx (Product available in reduced-noise advanced CMOS: 11000 Series) / SN74ACxx / CD74ACxx

ACT: 74ACT11xxx (Product available in reduced-noise advanced CMOS: 11000 Series) / SN74ACTxx / CD74ACTxx

## BUFFER / DRIVER (INVERTING, INVERTING AND NON-INVERTING, ADDRESS DRIVERS)

Description	No. of Output	Output	Device	Technology																				
				Bipolar				CMOS				BiCMOS				Advanced CMOS								
				TTL	LS	S	ALS	AS	F	HC	HCT	BCT	ABT	LVT	ALVT	AC	ACT	AHC	AHCT	LV	LV-AT	LVC	ALVC	AVC
INVERTING	6	3S	366	X	X					X/H														
		3S	368	X/A	●A					●/●	-/●													
		3S	436			X																		
		3S	437	X																				
	8	3S	231			X	X																	
		3S	240	●	●	●	●A	●A	●	●/●	●/●	●/●	●/-	●A	●A	H●	●/●/●	●/●/●	●	●	●A	●A	Z●A	H●
		3S	456											X/-										
		3S	466	X	X																			
		3S	468	X	X																			
		3S	540	●		●	●1	X	●/●	●/●	●A/-	●	H●		-/-●	-/-●	●	●	●A		●A			
		3S	655			X											X/H-	X/H-						
		3S	746																					
	10	OC	756				●																	
		OC	763																					
		SS	1240																					
		R3S	2240																					
		R3S	2540																					
		3S	25240																					
		OC	25756																					
		3S	628														X/H-	X/H-						
INVERTING AND NON-INVERTING	8	R3S	2828																					
		3S	29628		X					X/B/-														
	11	R3S	5461																					
		R3S	5463																					
ADDRESS DRIVERS	1-2	3S	16240																					
		3S	16540																					
		R3S	162240																					
		R3S	162540																					
	1-4	20	3S	16828															X					
		32	3S	32240																				
		3S	230			X	X																	
		OC	762			X																		

Explanatory notes [Output] 3S: 3-State Output R3S: Series Resistor and 3-State Output OC: Open-Collector Output

Status ●: Product available in technology indicated \*: New product planned in technology indicated

X: Discontinued ■: Not recommended for new designs

HC: SN74HCxx / CD74HCxx

HCT: SN74HCxx / CD74HCTxx

BCT: SN74BCTxx / SN64BCTxx

AC: 74AC11xxx (Product available in reduced-noise advanced CMOS: 11000 Series) / SN74ACxx / CD74ACxx

ACT: 74ACT11xxx (Product available in reduced-noise advanced CMOS: 11000 Series) / SN74ACTxx / CD74ACTxx

## BUS TRANSCEIVER (NON-INVERTING)

Description	No. of Output	Output	Device	Technology																
				Bipolar				CMOS				BiCMOS				Advanced CMOS				
				TTL	LS	S	ALS	AS	F	HC	HCT	BCT	ABT	LVT	ALVT	AC	ACT	AHC	AHCT	LV
NON-INVERTING	4	3S	226			X														
		3S	440																	
		OC	441																	
		3S	442																	
		3S	443																	
		3S	444																	
		OC	448																	
		3S	449																	
	8	3S	243																	
		3S	245																	
		OC	615																	
		OC	621																	
		3S	623																	
		3SOC	639																	
		OC	641																	
		3S	645																	
	8+1P	3S	646																	
		OC	647																	
		3S	652																	
		3SOC	654																	
		3S	657																	
		3S	659																	
		3S	665																	
		3S	852																	
		3S	856																	
		3S	877																	
	9	3S	899																	
		3S	1245																	
		3S	1645																	
		3S	2245															R●A		
		3S	2623																	
		3S	2645															●A		
		3S	2952																	
		3S	25245																	
		3S	25543																	
		3S	25621																	
	10	3S	25623																	
		3S	25641																	
	9 x 4	3S	25646																	
		3S	25647																	
	10	3S	25652																	
		3S	25654																	
	8+1P	3SOC	833														XH●	XH●		
		3SOC	853														XH●	XH●		
	9	3SOC	29833														XH●	XH●		
		3SOC	29853														XH●	XH●		
	9	3S	963														XH●	XH●		●A
		3S	29863														●B			
	9 x 4	3S	16409																H●	H●
		3S	861														●			●A
	10	3S	29861														XB			

Explanatory notes [No. of Output] +P: With Parity Bit

[Output] 3S: 3-State Output R3S: Series Resistor and 3-State Output

[Output] OC: Open-Collector Output 3SOC: 3-State Output / Open-Collector Output

Status ●: Product available in technology indicated ■: Discontinued ■: Not recommended for new designs

HC: SN74HCxx / CD74HCxx

HCT: SN74HCxx / CD74HCTxx

BCT: SN74BCTxx / SN64BCTxx

AC: 74AC11xxx (Product available in reduced-noise advanced CMOS: 11000 Series) / SN74ACxx / CD74ACxx

ACT: 74ACT11xxx (Product available in reduced-noise advanced CMOS: 11000 Series) / SN74ACTxx / CD74ACTxx

## BUS TRANSCEIVER (NON-INVERTING)

Description	No. of Output	Output	Device	Technology																							
				Bipolar				CMOS				BiCMOS				Advanced CMOS											
				TTL	LS	S	ALS	AS	F	HC	HCT	BCT	ABT	LVT	ALVT	AC	ACT	AHC	AHCT	LV	LV-AT	LVC	ALVC	AVC	AUC		
12/24	3S	16268																				X					
	3S	16269																				H● HR●A ●					
	3S	16270																				H●					
	3S	16271																				H●					
	3S	16272																				X					
	3S	16268																				H●					
	16/32	3S	162280																			HG●					
16	3S	16245															●A H●	●B H●	H● HR●	●	●	●	●	●A H●A HR●A R●A Z●A	● H●	●	●
	3S	16334																						● H●	●		
	3S	16470															●										
	3S	16543															●● H●	●	●	●	●						
	3S	16623															●● H●		●	●							
	3S	16646															●● H●		●	●							
	3S	16652															●● H●	●	●	●							
	3S	16952															●● H●		●	●							
	R3S	162245															●● H●	●A H●	H●						RX		
	R3S	162334																						● H●			
NON-INVERTING	16X3	3S	32316														H●										
	16X3	3S	32318														H●										
	3S	16657															●● H●										
	16+2P	3S	16833														●● H●										
	3S	16853															●● H●										
	3S	16472																	●								
	3S	16474																									
18	3S	16500															●B H●										
	3S	16501															●● H●										
	3S	16525																									
	3S	16600																									
	3S	16601															●● H●										
	3S	16634																	●● H●								
	3S	16683															●● H●		●	●							
	3S	16901																									
	R3S	162500																									
	R3S	162501																									
18/36	3S	162525																									
	3S	162600																									
	R3S	162601																									
	R3S	162834																									
	3S	16282																									
	R3S	162282																									
	3S	16836																									
20	3S	16861																	●● H●								
	R3S	162836																									
	3S	32543															H●										
32	3S	32952															X										
	3S	32245															H●	H●									
	3S	32500																									
	3S	32501															H●										

Explanatory notes [No. of Output] +P: With Parity Bit

[Output] 3S: 3-State Output R3S: Series Resistor and 3-State Output

[Output] OC: Open-Collector Output 3SOC: 3-State Output / Open-Collector Output

Status ●: Product available in technology indicated \*: New product planned in technology indicated

X: Discontinued ■: Not recommended for new designs

HC: SN74HCxx / CD74HCxx

HCT: SN74HCTxx / CD74HCTxx

BCT: SN74BCTx / SN64BCTx

AC: 74AC11xxx (Product available in reduced-noise advanced CMOS: 11000 Series) / SN74ACxx / CD74ACxx

ACT: 74ACT11xxx (Product available in reduced-noise advanced CMOS: 11000 Series) / SN74ACTxx / CD74ACTxx

BUS TRANSCEIVER (INVERTING, NON-INVERTING / INVERTING)

Description	No. of Output	Output	Device	Technology																
				Bipolar				CMOS				BiCMOS				Advanced CMOS				
				TTL	LS	S	ALS	AS	F	HC	HCT	BCT	ABT	LVT	ALVT	AC	ACT	AHC	AHCT	LV
INVERTING	4	3S	242	X	X	X	X	X	X/-	X/-										
		3S	446	X																
		3S	1242			X														
		R3S	2242	X																
	8	3S	544							X		X/-			X/-	X/-	X/-	X/-		
		3S	471													X/-	X/-	X/-	X/-	
		3S	473													X/-	X/-	X/-	X/-	
		3S	475													X/-	X/-	X/-	X/-	
		OC	614							X										
		3S	620	X	●A	X	X	X/-	X/-	X/-	●				X/-	X/-	X/-	X/-	X/-	
		OC	622	X	X	X	X													
		3SOC	638	X	●A	●A	●A													
	8+1P	3S	640	●1	●B	●1	●B	●1	●B	●1	●1	X/-	X/-	●	X/-	X/-	X/-	X/-	X/-	
		OC	642	●1	●A	●1	●A	●1	●A	●1	●1	X/-	X/-							
		3S	648	●1	●A	●1	●A	●1	●A	●1	●1	X/-	X/-	X/-	X/-	X/-	X/-	X/-	X/-	
		OC	649	X	X	X	X													
		3S	651	X	●A	X	●A	X	●A	X	●1	X/-	X/-	X/-	●	X/-	X/-	X/-	X/-	●
		3SOC	653	X	●1															
		3S	656							X/-	X/-									
		3S	664							X/-	X/-									
		3S	1640							X/-	X/-									
		3S	2620							X/-	X/-									
		3S	2640							X/-										
		3S	2953								X/-									
	16	3S	25620								X/-									
		3S	25622								X/-									
		3S	25640								X/-									
		3S	25642								X/-									
		3S	25848								X/-									
		3S	25849								X/-									
		3S	25851								X/-									
		3S	25853								X/-									
		3SOC	834												X/-	X/-	X/-	X/-	X/-	
		3SOC	854												X/-	X/-	X/-	X/-	X/-	
	9	3SOC	29834							X/-										
		3SOC	29854							●1										
		3S	864												X/-	X/-	X/-	X/-	X/-	
	10	3S	29854								●B/-									
		3S	862												X/-	X/-	X/-	X/-	X/-	
	18	3S	29862							X/B/-										●
		3S	16471												X					
		3S	16544												X	X				
		3S	16620												X	X				
		3S	16640												●	X	X	X	X	
		3S	16648												X					
		3S	16651												●	X				
		3S	16682												X					
		3S	16953												X					
		3S	16475												X					
	NON-INVERTING/INVERTING	3S	15624																	
		3S	16864												X					

Explanatory notes [No. of Output] +P: With Parity Bit

[Output] 3S: 3-State Output R3S: Series Resistor and 3-State Output

[Output] OC: Open-Collector Output 3SOC: 3-State Output / Open-Collector Output

Status ●: Product available in technology indicated -: New product planned in technology indicated

×: Discontinued ■: Not recommended for new designs

HC: SN74HCxx / CD74HCxx

HCT: SN74HCxx / CD74HCTxx

BCT: SN74BCTx / SN64BCTx

AC: 74AC11xx (Product available in reduced-noise advanced CMOS: 11000 Series) / SN74ACxx / CD74ACxx

ACT: 74ACT11xx (Product available in reduced-noise advanced CMOS: 11000 Series) / SN74ACTxx / CD74ACTxx

## J/K/FIF-FLOP

Trigger	Circuit	PRE • CLR	Output	Q • Q̄	Device	Technology																					
						Bipolar				CMOS				BiCMOS				Advanced CMOS									
						TTL	LS	S	ALS	AS	F	HC	HCT	BCT	ABT	LVT	ALVT	AC	ACT	AHC	AHCT	LV	LV-AT	LVC	ALVC	AVC	AUC
POS	1	B	25	B	72	X																					
		B	25	B	70	X																					
		B	25	B	73	X	●A																				
		B	25	B	109	X	●A	●A	●A	●A	●A																
	2	B	25	B	110	X																					
		B	25	B	111	X																					
NEG	4	B	25	Q	376	X																					
		B	25	B	76	X																					
		B	25	B	78	X																					
		B	25	B	107	●	●A																				
	2	B	25	B	112	X	●A	●A	●A	●A	●A																
		B	25	B	113	X	X	X	X	X	X																
	4	B	25	B	114	X	X	X	X	X	X																
		B	25	Q	276	X																					

## D-TYPE FLIP-FLOP

Trigger	Circuit	PRE • CLR	Output	Q • Q̄	Device	Technology																					
						Bipolar				CMOS				BiCMOS				Advanced CMOS									
						TTL	LS	S	ALS	AS	F	HC	HCT	BCT	ABT	LVT	ALVT	AC	ACT	AHC	AHCT	LV	LV-AT	LVC	ALVC	AVC	AUC
POS	2	B	25	B	74	X	●A	●A	●A	●A	●A	●A	●A	●A	●A	●A	●A	●A	●A	●A	●A	●A	●A	●A	●A	●A	
		C	25	B	171	X																					
		C	25	B	175	X	●	●	●	●B	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	
		B	25	B	376	X																					
	4	C	25	B	174	X	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	
		B	25	Q	376	X	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	
	6	C	25	Q	534	X	●A	●A	●A	●A	●A	●A	●A	●A	●A	●A	●A	●A	●A	●A	●A	●A	●A	●A	●A	●A	
		B	25	Q	564	X	●B	●B	●B	●B	●B	●B	●B	●B	●B	●B	●B	●B	●B	●B	●B	●B	●B	●B	●B	●B	
	8	C	25	Q	574	X	●B	●B	●B	●B	●B	●B	●B	●B	●B	●B	●B	●B	●B	●B	●B	●B	●B	●B	●B	●B	
		B	25	Q	575	X	●A	●A	●A	●A	●A	●A	●A	●A	●A	●A	●A	●A	●A	●A	●A	●A	●A	●A	●A	●A	
	9	C	35	Q	576	X	●B	●B	●B	●B	●B	●B	●B	●B	●B	●B	●B	●B	●B	●B	●B	●B	●B	●B	●B	●B	
		B	35	Q	577	X	●A	●A	●A	●A	●A	●A	●A	●A	●A	●A	●A	●A	●A	●A	●A	●A	●A	●A	●A	●A	
	10	C	35	Q	825	X	●A	●A	●A	●A	●A	●A	●A	●A	●A	●A	●A	●A	●A	●A	●A	●A	●A	●A	●A	●A	
		B	35	Q	826	X																					
	10X2	C	35	Q	874	X	●B	●B	●B	●B	●B	●B	●B	●B	●B	●B	●B	●B	●B	●B	●B	●B	●B	●B	●B	●B	
		P	35	Q	876	X	●A	●A	●A	●A	●A	●A	●A	●A	●A	●A	●A	●A	●A	●A	●A	●A	●A	●A	●A	●A	
	16	C	35	Q	878	X																					
		B	35	Q	16374	X																					
	18	C	35	Q	16534	X																					
		B	35	Q	162374	X																					
	20	C	35	Q	162823	X																					
		B	35	Q	162721	X																					
	22	C	35	Q	162821	X																					
		B	35	Q	162722	X																					
	32	C	35	Q	32374	X																					
		B	35	Q	322374	X																					

Explanatory notes [Trigger] POS: Positive edge NEG: Negative Edge

[PRE • CLR] B: Preset and Clear C: Clear Only

[Output] 2S: Totem pole Output 3S: 3-State Output

[Q • Q̄]: B: Q̄-Output Q: Q-Output Q̄: Q̄-Output

Status ●: Product available in technology indicated \*: New product planned in technology indicated

X: Discontinued ■: Not recommended for new designs

HC: SN74HCxx / CD74HCxx

HCT: SN74HCxx / CD74HCTxx

BCT: SN74BCTxx / SN64BCTxx

AC: 74AC11xxx (Product available in reduced-noise advanced CMOS: 11000 Series) / SN74ACxx / CD74ACxx

ACT: 74ACT11xxx (Product available in reduced-noise advanced CMOS: 11000 Series) / SN74ACTxx / CD74ACTxx

## LATCH

Type	Circuit	Output	PRE • CLR	Q • Q̄	Device	Technology																							
						Bipolar			CMOS			BiCMOS			Advanced CMOS														
						TTL	LS	S	ALS	AS	F	HC	HCT	BCT	ABT	LVT	ALVT	AC	ACT	AHC	AHCT	LV	LV-AT	LVC	ALVC	AVC	AUC		
S-R	4	2S		Q	279	X	●A																						
AD	8	2S	Q	259	X	●B	●		●/●	-/●						X/H-	X/H-												
	8	2S		4724																									
BIS	4	2S	Q	78	X	●						X/I●	X/I●				X/H-												
	4	2S	Q	77								X/L																	
	4	2S	Q	375		●						X/L																	
	8	2S	Q	100	X																								
R/B	8	3S	Q	990			●																						
	8	3S	Q	991			X																						
	8	3S	Q	666				●																					
	8	3S	C	996					●																				
	8	3S	B	657					●																				
	9	3S	C	992						●																			
	9	3S	C	993						X																			
	10	3S	Q	994						●																			
	10	3S	Q	995	X																								
	10	3S	Q	996	X																								
D	8	2S	C	116	X																								
	8	3S	Q	372		●	●	●A	●	●	●/●	●/●	●/●	●/●	●	H●		X/I●●	X/I●●	●	●	●A	●	●A	H●				
	8	3S	Q	2375				●										X/I●●	X/I●●										
	8	3S	Q	533		●A	●A	X	X/I●	X/I●	X/I●	X/I●	X/I●	X/I●	●A														
	8	3S	Q	573		●C	●A	●	●/●	●/●	●/●	●/●	●/●	●/●	●A	●	H●	X/I●●	X/I●●	●	●	●A	●	●A					
	8	3S	Q	563		●B	X	●/●	X/I●	X/I●	X/I●	X/I●	X/I●	X/I●	X/I●			X/I●●	X/I●●										
	8	3S	Q	590		●B	X											X/H-	X/H-										
	8	3S	C	873		●B	X/A																						
	8	3S	P	890		X/A	X																						
	8	3S	B	845		X/X												X/H-	X/H-										
	8	3S	B	29845		X/X											X/I-												
	8	3S	D	846		X/X											X/H-	X/H-											
	8	3S	B	29846		X/X											X/I-												
	9	3S	B	841		●	X										●												
	9	3S	B	1843																									
	9	3S	B	29843		X/X											●/●												
	9	3S	B	844		X/X												X/H-	X/H-										
	9	3S	B	29844		X/X											X/I-												
	10	3S	Q	841		●	X/A										●A		X/H-	X/H-									
	10	3S	Q	29841		X/X											X/I-												
	10	3S	Q	842		X/X												X/H-	X/H-										
	10	3S	Q	29842		X											X/I-												
	12/24	3S	Q	16260														H●											
	12/24	3S	Q	16260													H●												
	16	3S	Q	16373													●A	H●	H●	●	●	●	●	●	●A	H●A	H●	●	●
	16	3S	Q	16533																									
	16	3S	Q	162373													H●												
	18	3S	B	16843													●			X									
	20	3S	Q	16841													●			●									
	20	3S	Q	162841													●												
	32	3S	Q	32373													H●	H●											

Explanatory notes [Type] S-R: S-R Latch AD: Addressable Latch BIS: Bistable Latch

[Type] R-B: Read-Back Latch D: D-Type Transparent Latch

[PRE • CLR] B: Preset and Clear C: Clear Only

[Output] 2S: Totem pole Output 3S: 3-State Output

[Q • Q̄] B: Q̄-Output Q: Q-Output Q̄: Q̄-Output

Status ●: Product available in technology indicated \*: New product planned in technology indicated

X: Discontinued ■: Not recommended for new designs

HC: SN74HCxx / CD74HCxx

HCT: SN74HCTxx / CD74HCTxx

**SHIFT REGISTER**

Input Type	Output Type	No. of Bit	CLR	Shift	Output	Device	Technology																			
							Bipolar				CMOS				BiCMOS				Advanced CMOS							
							TTL	LS	S	ALS	AS	F	HC	HCT	BCT	ABT	LVT	ALVT	AC	ACT	AHC	AHCT	LV	LVC	ALVC	AVC
S/P	S/P	4	R	25	178	X																				
			C	25	179	X																				
			I	25	195	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	
			I	25	95	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	
			B	25	295	X	C																			
			B	35	395	X	A																			
			C	B	194	X	●	A	X	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	
			C	25	96	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	
		8	C	35	322	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	
			C	B	198	X																				
			B	35	299	●	X	●	X	●	X	●	●	●	●	●	●	●	●	●	●	●	●	●	●	
			C	B	323	X	●	●	X	●	●	X	X	X	X	X	X	X	X	X	X	X	X	X	X	
			C	25	199	X																				
S/P	S	8		R	25	165	X	●	A	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	
				C	25	166	X	●	A	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	
S	S/P	8	C	R	25	164	X	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	
S	P	10	C		25	898																				
S	S	8		R	25	91	X	X																		
P	S	4	C	R	25	94	X																			
		16		R	3S	674	●																			

**SHIFT REGISTER WITH LATCH**

Input Type	Output Type	No. of Bit	CLR	Shift	Output	Device	Technology																			
							Bipolar				CMOS				BiCMOS				Advanced CMOS							
							TTL	LS	S	ALS	AS	F	HC	HCT	BCT	ABT	LVT	ALVT	AC	ACT	AHC	AHCT	LV	LVC	ALVC	AVC
S	S/P	4	C	B	35	671	X																			
			C	B	35	672	X																			
			C	R	25	598	●																			
			C	R	35	673	●																			
			C	R	35	595	●																			
			C	R	OC	599	X																			
			C	R	OC	596	●																			
			C	R	25	594	●																			
		8	C	B	35	674	●																			
			C	R	35	597	●																			
			C	R	35	598	●																			
			C	R	35	599	●																			
			C	R	35	600	●																			
			C	R	35	601	●																			
			C	R	35	602	●																			
			C	R	35	603	●																			

Explanatory notes [Input/Output Type] S: Serial P: Parallel S/P: Alternative Serial/Parallel

[CLR] C: With Clear  
[Shift] R: Right-Shift B: Alternative Shift Right/Left

[Output] 2S: Totem-Pole Output 3S: 3-State Output

Status ●: Product available in technology indicated \*: New product planned in technology indicated

X: Discontinued ■: Not recommended for new designs

HC: SN74HCxx / CD74HCxx

HCT: SN74HCTxx / CD74HCTxx

BCT: SN74BCTx / SN64BCTx

AC: 74AC11xxx (Product available in reduced-noise advanced CMOS: 11000 Series) / SN74ACxx / CD74ACxx

ACT: 74ACT11xxx (Product available in reduced-noise advanced CMOS: 11000 Series) / SN74ACTxx / CD74ACTxx

## REGISTER (ETC)

Description	Device	Technology																		
		Bipolar						CMOS			BiCMOS				Advanced CMOS					
		TTL	LS	S	ALS	AS	F	HC	HCT	BCT	ABT	LVT	ALVT	AC	ACT	AHC	AHCT	LV	LVC	ALVC
REGISTER FILES 8W x 2B	172	×																		
REGISTER FILES 4W x 4B	170	×	×																	
REGISTER FILES 4W x 4B	670	●						-/- ●	-/- ●											
REGISTER FILES 16W x 5B	870		●	×													X/-	X/-		
REGISTER FILES 16W x 5B	858																X/-	X/-		
REGISTER FILES 16W x 6B	871		×	×													X/-	X/-		
REGISTER FILES 32W x 4B	859																X/-	X/-		
MUX WITH STRAGE	298	×	●			●A														
MUX WITH STRAGE	398	×																		
4BIT BUS-BUFFER REGISTER	173	×	●A																	
8BIT STORAGE REGISTER	396	×																		
	818																X/-	X/-		
	819																X/-	X/-		
	29818																X/-			

Status ●: Product available in technology indicated   \*: New product planned in technology indicated

×: Discontinued   ■: Not recommended for new designs

HC: SN74HCxx / CD74HCxx

HCT: SN74HCxx / CD74HCTxx

BCT: SN74BCTx / SN64BCTx

AC: 74AC11xxx (Product available in reduced-noise advanced CMOS: 11000 Series) / SN74ACxx / CD74ACxx

ACT: 74ACT11xxx (Product available in reduced-noise advanced CMOS: 11000 Series) / SN74ACTxx / CD74ACTxx

## MONOSTABLE MULTIVIBRATOR

Circuit	CLR	Retrigger	Device	Technology																		
				Bipolar						CMOS			BiCMOS				Advanced CMOS					
				TTL	LS	S	ALS	AS	F	HC	HCT	BCT	ABT	LVT	ALVT	AC	ACT	AHC	AHCT	LV	LVC	ALVC
1				121	●																	
	C	R		122	×	●																
	C	R		422	×																	
2	C	R		123	●	●							-/- ●	-/- ●					●A	●A	●A	
	C			221	●	●							-/- ●	-/- ●					●A			
	C	R		423	●								-/- ●	-/- ●								
	C	R		4538									-/- ●	-/- ●								

Explanatory notes [CLR] C: With Clear

[Retrigger] R: With Retrigger

Status ●: Product available in technology indicated   \*: New product planned in technology indicated

×: Discontinued   ■: Not recommended for new designs

HC: SN74HCxx / CD74HCxx

HCT: SN74HCxx / CD74HCTxx

BCT: SN74BCTx / SN64BCTx

AC: 74AC11xxx (Product available in reduced-noise advanced CMOS: 11000 Series) / SN74ACxx / CD74ACxx

ACT: 74ACT11xxx (Product available in reduced-noise advanced CMOS: 11000 Series) / SN74ACTxx / CD74ACTxx

## DECade/Binary Counter

DEC BIN	ASYN SYN	No. of Bit	UP/DOWN Mode	CLR	LOAD	ETC	Device	Technology																							
								Bipolar				CMOS				BiCMOS				Advanced CMOS											
								TTL	LS	S	ALS	AS	F	HC	HCT	BCT	ABT	LVT	ALVT	AC	ACT	AHC	AHCT	LV	LVC	ALVC	AVC	AUC			
DEC	A	4	A	D	S	Y	A	68	X																						
							9	90	X	●																					
							290	X	X																						
							A	390	X	●						X/A	-/-														
							A	176	X																						
							A	196	X	X																					
							A	490	X	X																					
							560																								
	S	4	Y	A	S	S	S	162	X	A	X	X	B	X	X	X/-									X/H-	X/H-					
							A	160	X	A	X	X	B	X	X	X/-									X/H-	X/H-					
							A	690																							
							S	692																							
							S	568								X	X								X/H-	X/H-					
							S	168	X	X	X	X	X	X	X										X/H-	X/H-					
							A	190	X	X	X	X	X	X	X	X/A	X/-								X/H-	X/H-					
							S	696																							
							S	698																							
							A	192	X	X	X	X	X	X	X	X/-									X/H-	X/H-					
							A	4017	J							X/-															
BIN	A	4	A	D	S	Y	A	68	X							-/-	-/-									●A					
							93	X	●																						
							293	X	●																						
							173	X	●							●/●	-/-														
							A	177	X																						
							A	197	X	X	X	X	X	X	X												●A				
							7	A	4024							X/-	-/-														
							12	A	4040							●/●	-/-										●A				
	S	4	Y	A	S	S	A	4020								●/●	-/-										●A				
							A	4060								●/●	-/-														
							A	4061								X/-															
							S	561								●/A															
							S	163	X	●	A	●	B	●	A	●/●	-/-									X/H	●	X/H	●		
							S	693																							
							A	161	X	●	A	●	B	●	A	●/●	-/-									X/H	●	X/H	●		
							A	691																							
	S	8	Y	A	S	S	D	4516								-/-															
							S	569																							
							S	699																							
							S	169	X	●	B	X	●	B	●	A	●/●	-/-								X/H-	X/H-				
							A	191	X	●	A	●				●/●	-/-									X/H-	X/H-				
							A	697																							
							A	193	X	●	A	●				X/A	●/●	-/-								X/H-	X/H-				
							A	561								●/A	X														
	Y	A	S	A	R	S	A	461																							
							S	463																							
							A	490																							
							A	591																							
							A	592																							
							A	593																							
							J	4022									X/-														
							J	4520								-/-	-/-														
	Y	A	J	S	S	S	A	7022									X/-														
							J	40103									-/-	-/-													
							S	469																							
							S	579																							
							S	869									●	●													
							A	867								●/A	●														
							12	92	X	●																					

Explanatory notes [DEC-BIN] DEC: Decoder BIN: Binary Counter OHE: Other

[ASYN-SYN] ASYN: Asynchronous SYN: Synchronous

[Up/Down] Y: Up/Down

[CLR] A: With Asynchronous Clear S: With Synchronous Clear 9: Preset 9

[LOAD] A: With Asynchronous Clear S: With Synchronous Clear 12: Devide By-Twelve Counter

[ETC] D: 2-Circuit R: With Series Register J: Johnson Counter

Status ●: Product available in technology indicated \*: New product planned in technology indicated

X: Discontinued ■: Not recommended for new designs

HC: SN74HCxx / CD74HCxx

HCT: SN74HCTxx / CD74HCTxx

BCT: SN74BCTx / SN64BCTx

AC: 74AC1xxx (Product available in reduced-noise advanced CMOS: 11000 Series) / SN74ACxx / CD74ACxx

ACT: 74ACT1xxx (Product available in reduced-noise advanced CMOS: 11000 Series) / SN74ACTxx / CD74ACTxx

## RATE MULTIPLIER/FREQUENCY DIVIDERS

Description	Device	Technology														Advanced CMOS				
		Bipolar				CMOS				BiCMOS				Advanced CMOS						
TTL	LS	S	ALS	AS	F	HC	HCT	BCT	ABT	LVT	ALVT	AC	ACT	AHC	AHCT	LV	LVC	ALVC	AVC	AUC
FREQUENCY DIVIDERS		56																		
FREQUENCY DIVIDERS		57																		
6BIT BINARY RATE MULTIPLIER		97	●																	
DECADATE RATE MULTIPLIER		167																		
PROGRAMMABLE FREQUENCY DIVIDER/DIGITAL TIMERS		292																		
		294		●																

Status ●: Product available in technology indicated \*: New product planned in technology indicated

×: Discontinued ■: Not recommended for new designs

HC: SN74HCxx / CD74HCxx

HCT: SN74HCxx / CD74HCTxx

BCT: SN74BCxx / SN64BCTx

AC: 74AC11xxx (Product available in reduced-noise advanced CMOS: 11000 Series) / SN74ACxx / CD74ACxx

ACT: 74ACT11xxx (Product available in reduced-noise advanced CMOS: 11000 Series) / SN74ACTxx / CD74ACTxx

## DATA SELECTOR/MULTIPLEXER

No. of Input/output	Output	Circuit	ETC	Device	Technology															
					Bipolar				CMOS				BiCMOS				Advanced CMOS			
TTL	LS	S	ALS	AS	F	HC	HCT	BCT	ABT	LVT	ALVT	AC	ACT	AHC	AHCT	LV	LVC	ALVC	AVC	AUC
16/1	2S	1		150	●											X/H-	X/H-			
	3S	1		250			●A									X/H-	X/H-			
	3S	1		850		×										X/H-	X/H-			
	3S	1		851		×														
	2S	1		4067					X/H-	●	●									
8/1	2S	1		151	×	A	●	●	●	●	●	●	●			X/H-	X/H-			
	2S	1		152					X/H-											
	3S	1		251	×	●	×	●	×	●	●	●	●	●		X/H-	X/H-			
	3S	1		354		×				X/H-										
	3S	1		356					X/H-											
	3S	1		4051					X/H-											
	3S	1		4351					X/H-											
	OC	1		355		×														
4/1	OC	1		357		×														
	2S	2		352	×		×	×	×	×	X/H-					X/H-	X/H-			
	3S	2		153	×	●	×	●	●	●	●	●	●	●		X/H-	X/H-			
	3S	2		253	●			●	●	●	●	●	●	●		X/H-	X/H-			
	3S	2		353	×		×	×	×	X/H-						X/H-	X/H-			
	3S	2		4052					X/H-											
	3S	2		4352					X/H-											
2/1	3S	4		16460							H●									
	3S	4		162460						H●										
	2S	1		157	×		●	●	●	●	●	●	●	●		X/H-	X/H-	●	●	●
	2S	1		158	●	×	●	●	●	●	●	●	●	●		X/H-	X/H-	●	●	-
	2S	4	S	399	●															
16	3S	1		257	●B	×	●A	●	●	●	●	●	●	●		●/H-	●/H-	●	●	●A
	3S	1		258	●B	×	●A	●	●	●	●	●	●	●		X/H-	X/H-	●	●	-
	3S	4		4053						X/H-										
	3S	6	U	857					X/H-											
	3S	8	S	604		×				X/H-										
	OC	8	S	605		×														
	3S	8	S	606		×														
	OC	8	S	607		×														

Explanatory notes [Output] 2S: Totem pole Output 3S: 3-State Output OC: Open-Collector Output

[ETC] S: Storage Register

Status ●: Product available in technology indicated \*: New product planned in technology indicated

×: Discontinued ■: Not recommended for new designs

HC: SN74HCxx / CD74HCxx

HCT: SN74HCxx / CD74HCTxx

BCT: SN74BCxx / SN64BCTx

## DECODER / DEMULTIPLEXER

No. of Input/output	Output	Circuit	ETC	Device	Technology																				
					Bipolar				CMOS				BiCMOS				Advanced CMOS								
					TTL	LS	S	ALS	AS	F	HC	HCT	BCT	ABT	LVT	ALVT	AC	ACT	AHC	AHCT	LV	LV-AT	LVC	ALVC	AVC
4/16	2S	1	AD	4514							X/●	X/●													
	2S	1	AD	4515							X/●	✓/●													
	3S	1		154	●						X/●	✓/●					X/H-	X/H-							
	OC	1		159	●																				
4/10	2S	1	BD	42	× A	●					●/●	✓/●													
	2S	1	BD	43	×																				
	2S	1	BD	44	×																				
3/8	2S	1		238							X/●	✓/●					X/H ●	X/H ●							
	2S	1		138	● A	● A	●	●	●	●	●/●	●/●					● H ●	● H ●	●	●	● A	● A			
	2S	1	AD	237							X/●	✓/●													
	2S	1	AD	137	×		● A	×			X/●	✓/●													*
	2S	1	AD	131							X/●	✓/●													
2/4	2S	2		139	● A	● A	●	×	×		●/●	●/●					X/H ●	● H ●	●	●	● A	● A			
	2S	2		239													X/H-	X/H-							
	2S	2		155	×	● A																			
	OC	2		156	×	●																			

Explanatory notes [Output]: 2S: Totem pole Output 3S: 3-State Output OC: Open-Collector Output

[ETC] AD: Address Latch BD: BCD TO DECIMAL

Status ●: Product available in technology indicated \*: New product planned in technology indicated

✗: Discontinued ■: Not recommended for new designs

HC: SN74HCxx / CD74HCxx

HCT: SN74HCTxx / CD74HCTxx

BCT: SN74BCTx / SN64BCTx

AC: 74AC11xxx (Product available in reduced-noise advanced CMOS: 11000 Series) / SN74ACxx / CD74ACxx

ACT: 74ACT11xxx (Product available in reduced-noise advanced CMOS: 11000 Series) / SN74ACTxx / CD74ACTxx

## CODE CONVERTER / PRIORITY ENCODER / REGISTER

Description	Device	Technology												BiCMOS				Advanced CMOS						
		Bipolar				CMOS				BiCMOS				Advanced CMOS										
		TTL	LS	S	ALS	AS	F	HC	HCT	BCT	ABT	LVT	ALVT	AC	ACT	AHC	AHCT	LV	LV-AT	LVC	ALVC	AVC	AUC	
CODE CONVERTER	184	×																						
CODE CONVERTER	185	×																						
10-4 PRIORITY ENCODER	147	×									-●	✓/●												
8-3 PRIORITY ENCODER	148	×	●								×	●/-												
8-3 PRIORITY ENCODER	348	●															X							
4BIT CASCADABLE PRIORITY REGISTER	278	×																						

Status ●: Product available in technology indicated \*: New product planned in technology indicated

✗: Discontinued ■: Not recommended for new designs

HC: SN74HCxx / CD74HCxx

HCT: SN74HCTxx / CD74HCTxx

BCT: SN74BCTx / SN64BCTx

AC: 74AC11xxx (Product available in reduced-noise advanced CMOS: 11000 Series) / SN74ACxx / CD74ACxx

ACT: 74ACT11xxx (Product available in reduced-noise advanced CMOS: 11000 Series) / SN74ACTxx / CD74ACTxx

## Display Decoder / Driver

Function	V <sub>DD</sub> (V)	Device	Technology																		
			Bipolar				CMOS				BiCMOS				Advanced CMOS						
			TTL	LS	S	ALS	AS	F	HC	HCT	BCT	ABT	LVT	ALVT	AC	ACT	AHC	AHCT	LV	LVC	ALVC
D	30	45	●																		
D	60	141	×																		
D	15	145	●	●																	
D	7	445	×																		
7	30	46	×																		
7	15	47	●	●																	
7	5.5	48	×	×																	
7	5.5	49	×																		
7	30	246	×																		
7	15	247	×	●																	
7	7	347																			
7	7	447																			
7	5.5	248	×																		
7	5.5	249	×																		
B	7	142	×																		
B	7	143	×																		
B	7	144	×																		

Explanatory notes [Function] D: BCD TO DECIMAL, 7: BCD TO 7-SEGMENT, B: COUNTER/LATCH/DECODER/DRIVER

[VOH] Off-Stage Output Voltage (V)

Status ●: Product available in technology indicated \*: New product planned in technology indicated

✗: Discontinued ■: Not recommended for new designs

HC: SN74HCxx / CD74HCxx

HCT: SN74HCTxx / CD74HCTxx

BCT: SN74BCTx / SN64BCTx

AC: 74AC11xxx (Product available in reduced-noise advanced CMOS: 11000 Series) / SN74ACxx / CD74ACxx

ACT: 74ACT11xxx (Product available in reduced-noise advanced CMOS: 11000 Series) / SN74ACTxx / CD74ACTxx

## COMPARATOR

No. of Bit	Input	P=Q	P=Q	P>Q	P<Q	Output	Device	Technology																				
								Bipolar				CMOS				BiCMOS				Advanced CMOS								
								TTL	LS	S	ALS	AS	F	HC	HCT	BCT	ABT	LVT	ALVT	AC	ACT	AHC	AHCT	LV	LVC	ALVC	AVC	AUC
4	S	Y	N	Y	Y	2S	85	✗	●	●	✗				✗/A	●	✗											
6	S	N	Y	N	N	2S	29806																					
8	20	Y	N	N	N	OC	518			●																		
8	20	N	Y	N	N	2S	520			●																		
8	20	N	Y	N	N	OC	522																					
8	20	N	Y	Y	N	2S	682		●																			
8	20	N	Y	Y	N	OC	683	✗																				
8	S	Y	N	N	N	OC	519				✗	✗																
8	S	N	Y	N	N	2S	521			●	●	●																
8	S	N	Y	Y	N	2S	684		●																			
8	S	N	Y	Y	N	OC	685																					
8	S	N	Y	Y	N	2S	686																					
8	S	N	Y	Y	N	OC	687																					
8	S	N	Y	N	N	2S	688		●	●	●	●	●	●														
8	S	N	Y	N	N	OC	689	✗	✗																			
8	S	Y	N	Y	Y	2S	860																					
8	S	N	N	Y	Y	2S	865																					
8	LP	N	N	Y	Y	2S	885			●																		
8	LPQ	Y	N	Y	Y	OC	866																					
9	-	N	Y	N	N	2S	29809				✗	A																

Explanatory notes [Input] S: Standard 20: 20-kW Pullup Resistors LP: P-Port Latch LPQ: L,P-port Latch

[P=Q, P=Q, P>Q, P<Q] Y: Yes N: No

[Output] 2S: Totem Pole Output, OC: Open-Collector Output

Status ●: Product available in technology indicated \*: New product planned in technology indicated

✗: Discontinued ■: Not recommended for new designs

HC: SN74HCxx / CD74HCxx

HCT: SN74HCTxx / CD74HCTxx

BCT: SN74BCTx / CD74BCTx

**ADRESS COMPARATOR / FUSE-PROGRAMMABLE IDENTITY COMPARATOR**

Description	No. of Bit	ETC	Device	Technology																
				Bipolar				CMOS				BiCMOS				Advanced CMOS				
				TTL	LS	S	ALS	AS	F	HC	HCT	BCT	ABT	LVT	ALVT	AC	ACT	AHC	AHCT	LV
A	16-4	OE	677			X	A												X	A
A	16-4	L	678			X													X	A
A	12-4	OE	679			●													X	A
A	12-4	L	680			X													X	A
F	16		526			X														
F	12		528			X														
F	8		527			X														

Explanatory notes [Function] A: Adress Comparator F: Fuse-Programmable Identity Comparators

[ETC] OE: Output-With Enable L: Output-With Latch

Status ●: Product available in technology indicated \*: New product planned in technology indicated

✗: Discontinued ■: Not recommended for new designs

HC: SN74HCxx / CD74HCxx

HCT: SN74HCxx / CD74HCTxx

BCT: SN74BCTx / SN64BCTx

AC: 74AC11xxx (Product available in reduced-noise advanced CMOS: 11000 Series) / SN74ACxx / CD74ACxx

ACT: 74ACT11xxx (Product available in reduced-noise advanced CMOS: 11000 Series) / SN74ACTxx / CD74ACTxx

**PARTY GENERATOR / CHECKER**

No. of Bit	Device	Technology																			
		Bipolar				CMOS				BiCMOS				Advanced CMOS							
		TTL	LS	S	ALS	AS	F	HC	HCT	BCT	ABT	LVT	ALVT	AC	ACT	AHC	AHCT	LV	LVC	ALVC	AVC
8	180	X																			
9	280		●	●	●	●	●	●	●	●	●	●	●			X	●	X	●		
9	286			●	X											X	●	●	●		

Status ●: Product available in technology indicated \*: New product planned in technology indicated

✗: Discontinued ■: Not recommended for new designs

HC: SN74HCxx / CD74HCxx

HCT: SN74HCxx / CD74HCTxx

BCT: SN74BCTx / SN64BCTx

AC: 74AC11xxx (Product available in reduced-noise advanced CMOS: 11000 Series) / SN74ACxx / CD74ACxx

ACT: 74ACT11xxx (Product available in reduced-noise advanced CMOS: 11000 Series) / SN74ACTxx / CD74ACTxx

**VOLTAGE CONTROLLED OSCILLATOR (VCO)**

Circuit	Fmax (MHz)	COMPL Z OUT	ENABLE	RANGE INPUT	Rext	PLL	Device	Technology																
								Bipolar				CMOS				BiCMOS				Advanced CMOS				
								TTL	LS	S	ALS	AS	F	HC	HCT	BCT	ABT	LVT	ALVT	AC	ACT	AHC	AHCT	LV
1	20	Y	Y	Y			624													●				
	20	Y	Y	Y	Y		628													●				
	20	Y	Y	Y	Y	Y	7046												-●A	-●A				
2	20						627		X															
	20	Y	Y	Y	Y	Y	629		●															
	20	Y	Y	Y	Y	Y	625		X															
	20	Y	Y	Y	Y	Y	626		X															
	60	Y	Y	Y	Y	Y	124												●					
	24	Y	Y	Y	Y	Y	4046												-●A	-●A				

Status ●: Product available in technology indicated \*: New product planned in technology indicated

✗: Discontinued ■: Not recommended for new designs

HC: SN74HCxx / CD74HCxx

HCT: SN74HCxx / CD74HCTxx

BCT: SN74BCTx / SN64BCTx

AC: 74AC11xxx (Product available in reduced-noise advanced CMOS: 11000 Series) / SN74ACxx / CD74ACxx

ACT: 74ACT11xxx (Product available in reduced-noise advanced CMOS: 11000 Series) / SN74ACTxx / CD74ACTxx

**ACCUMULATORS / ARITHMETIC LOGIC UNIT (ALU) / LOOK-AHEAD CARRY GENERATOR**

Description	Device	Technology																				
		Bipolar				CMOS				BiCMOS				Advanced CMOS								
		TTL	LS	S	ALS	AS	F	HC	HCT	BCT	ABT	LVT	ALVT	AC	ACT	AHC	AHCT	LV	LVC	ALVC	AVC	AUC
4BIT PARALLEL BINARY ACCUMULATORS	281			X																		
4BIT PARALLEL BINARY ACCUMULATORS	681		X																			
4BIT ALU/FUNCTION GENERATORS	181	X	●	X		●A									X/-	X/-						
4BIT ALU/FUNCTION GENERATORS	381	X	X	X			X								X/-	X/-						
4BIT ALU/FUNCTION GENERATORS	681					X	A								X/-	X/-						
4BIT ALU WITH RIPPLE CARRY	382	X		X			X															
LOOK AHEAD CARRY GENERATORS	264						X															
LOOK AHEAD CARRY GENERATORS	182	X		X			X															
LOOK AHEAD CARRY GENERATORS	282						X															
LOOK AHEAD CARRY GENERATORS	882						X	A							X/-	X/-						
QUAD SERIAL ADDER/SUBTRACTOR	385	X													X/-	X/-						

Status ●: Product available in technology indicated \*: New product planned in technology indicated

×: Discontinued ■: Not recommended for new designs

HC: SN74HCxx / CD74HCxx

HCT: SN74HCxx / CD74HCTxx

BCT: SN74BCTxX / SN64BCTxX

AC: 74AC11xxx (Product available in reduced-noise advanced CMOS: 11000 Series) / SN74ACxx / CD74ACxx

ACT: 74ACT11xxx (Product available in reduced-noise advanced CMOS: 11000 Series) / SN74ACTxx / CD74ACTxx

**ADDER**

Description	Device	Technology																				
		Bipolar				CMOS				BiCMOS				Advanced CMOS								
		TTL	LS	S	ALS	AS	F	HC	HCT	BCT	ABT	LVT	ALVT	AC	ACT	AHC	AHCT	LV	LVC	ALVC	AVC	AUC
4BIT BINARY FULL ADDER	83	X	X																			
4BIT BINARY FULL ADDER	283	X	●	●		●	-●	-●						-/-●	-/-●							
DUAL CARRY SAVE FULL ADDER	183	X																				
GATED FULL ADDER	80	X																				
2BIT BINARY FULL ADDER	82	X																				

Status ●: Product available in technology indicated \*: New product planned in technology indicated

×: Discontinued ■: Not recommended for new designs

HC: SN74HCxx / CD74HCxx

HCT: SN74HCxx / CD74HCTxx

BCT: SN74BCTxX / SN64BCTxX

AC: 74AC11xxx (Product available in reduced-noise advanced CMOS: 11000 Series) / SN74ACxx / CD74ACxx

ACT: 74ACT11xxx (Product available in reduced-noise advanced CMOS: 11000 Series) / SN74ACTxx / CD74ACTxx

**MULTIPLIER**

Description	Device	Technology																				
		Bipolar				CMOS				BiCMOS				Advanced CMOS								
		TTL	LS	S	ALS	AS	F	HC	HCT	BCT	ABT	LVT	ALVT	AC	ACT	AHC	AHCT	LV	LVC	ALVC	AVC	AUC
2-4 PARALLEL BINARY MULTIPLIERS	261	X																				
4-4 PARALLEL BINARY MULTIPLIERS	284	X																				
4-4 PARALLEL BINARY MULTIPLIERS	285	X																				
2S COMPLEMENT MULTIPLIERS	384	X																				

Status ●: Product available in technology indicated \*: New product planned in technology indicated

×: Discontinued ■: Not recommended for new designs

HC: SN74HCxx / CD74HCxx

HCT: SN74HCxx / CD74HCTxx

BCT: SN74BCTxX / SN64BCTxX

AC: 74AC11xxx (Product available in reduced-noise advanced CMOS: 11000 Series) / SN74ACxx / CD74ACxx

ACT: 74ACT11xxx (Product available in reduced-noise advanced CMOS: 11000 Series) / SN74ACTxx / CD74ACTxx

## MEMORY

Description	Device	Technology																					
		Bipolar						CMOS				BiCMOS				Advanced CMOS							
		TTL	LS	S	ALS	AS	F	HC	HCT	BCT	ABT	LVT	ALVT	AC	ACT	AHC	AHCT	LV	LVC	ALVC	AVC	AUC	
MEMORY REFRESH CONTROLLERS	600	X																					
MEMORY REFRESH CONTROLLERS	601	X																					
MEMORY REFRESH CONTROLLERS	602	X																					
MEMORY CYCLE CONTROLLER	608																						
MEMMEMORY MAPERS	612	X																					
MEMMEMORY MAPERS	613	X																					
MEMMEMORY MAPERS WITH LATCH	610	X																					
MEMMEMORY MAPERS WITH LATCH	611	X																					
MULTI-MODE LATCH	412	X																					
3-8 MEMORY DECIDER	2414																						

Status   ●: Product available in technology indicated   \*: New product planned in technology indicated

X: Discontinued   ■: Not recommended for new designs

HC: SN74HCxx / CD74HCxx

HCT: SN74HCxx / CD74HCTxx

BCT: SN74BCTx / SN64BCTx

AC: 74AC11xx (Product available in reduced-noise advanced CMOS: 11000 Series) / SN74ACxx / CD74ACxx

ACT: 74ACT11xx (Product available in reduced-noise advanced CMOS: 11000 Series) / SN74ACTxx / CD74ACTxx

## CLOCK GENERATOR CIRCUIT

Description	Device	Technology																					
		Bipolar						CMOS				BiCMOS				Advanced CMOS							
		TTL	LS	S	ALS	AS	F	HC	HCT	BCT	ABT	LVT	ALVT	AC	ACT	AHC	AHCT	LV	LVC	ALVC	AVC	AUC	
QUAD COMPLEMENTARY-OUTPUT LOGIC	265	X																					
DUAL PULSE SYNCHRONIZERS/DRIVERS	120	X																					
CRYSTAL-CONTROLLED OSCILLATORS	320	X																					
CRYSTAL-CONTROLLED OSCILLATORS	321	X																					
DIGITAL PHASE-LOCK LOOP	297	●																					

Status   ●: Product available in technology indicated   \*: New product planned in technology indicated

X: Discontinued   ■: Not recommended for new designs

HC: SN74HCxx / CD74HCxx

HCT: SN74HCxx / CD74HCTxx

BCT: SN74BCTx / SN64BCTx

AC: 74AC11xx (Product available in reduced-noise advanced CMOS: 11000 Series) / SN74ACxx / CD74ACxx

ACT: 74ACT11xx (Product available in reduced-noise advanced CMOS: 11000 Series) / SN74ACTxx / CD74ACTxx

## SWITCH, SHIFTER, ERROR DETECTION CORRECTION CIRCUIT, HARD DISK DRIVER

Description	Device	Technology																					
		Bipolar						CMOS				BiCMOS				Advanced CMOS							
		TTL	LS	S	ALS	AS	F	HC	HCT	BCT	ABT	LVT	ALVT	AC	ACT	AHC	AHCT	LV	LVC	ALVC	AVC	AUC	
QUAD BILATERAL SWITCHES	4016							-●															
ANALOG SWITCHES WITH LEVEL TRANSLATION	4066							●●	-●								●	●A					
4BIT SHIFTERS	350	X																					
8BIT PARALLEL ERROR DETECTION CORRECTION CIRCUIT	636	X																					
16BIT PARALLEL ERROR DETECTION CORRECTION CIRCUIT	637	X																					
32BIT PARALLEL ERROR DETECTION CORRECTION CIRCUIT	616																						
HARD DISK DRIVER	1250																						

Status   ●: Product available in technology indicated   \*: New product planned in technology indicated

X: Discontinued   ■: Not recommended for new designs

HC: SN74HCxx / CD74HCxx

HCT: SN74HCxx / CD74HCTxx

BCT: SN74BCTx / SN64BCTx

AC: 74AC11xx (Product available in reduced-noise advanced CMOS: 11000 Series) / SN74ACxx / CD74ACxx

ACT: 74ACT11xx (Product available in reduced-noise advanced CMOS: 11000 Series) / SN74ACTxx / CD74ACTxx

# **PIN ASSIGNMENTS**

**Standard**

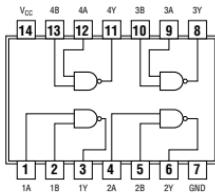


# Pin Assignments

**00**

**QUADRUPLE 2-INPUT  
POSITIVE-NAND GATES**

positive logic:  
 $Y = \bar{A} \cdot \bar{B}$

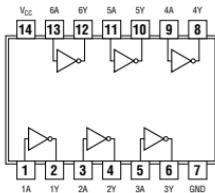


See page 231

**04**

**HEX INVERTERS**

positive logic:  
 $Y = \bar{A}$

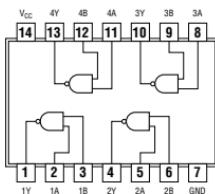


See page 235

**01**

**QUADRUPLE 2-INPUT POSITIVE-NAND GATES  
WITH OPEN-COLLECTOR OUTPUTS**

positive logic:  
 $Y = \bar{A} \cdot \bar{B}$

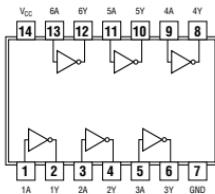


See page 232

**U04**

**HEX INVERTERS**

positive logic:  
 $Y = \bar{A}$

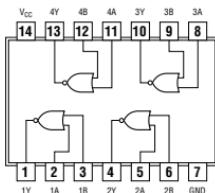


See page 236

**02**

**QUADRUPLE 2-INPUT  
POSITIVE-NOR GATES**

positive logic:  
 $Y = \bar{A} + \bar{B}$

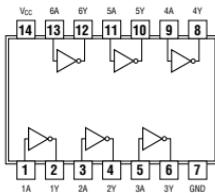


See page 233

**05**

**HEX INVERTERS  
WITH OPEN-RAIN OUTCOMES**

positive logic:  
 $Y = \bar{A}$

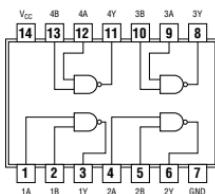


See page 236

**03**

**QUADRUPLE 2-INPUT POSITIVE-NAND GATES  
WITH OPEN-COLLECTOR OUTPUTS**

positive logic:  
 $Y = \bar{A} \cdot \bar{B}$

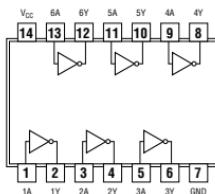


See page 234

**06**

**HEX INVERTER BUFFERS/DRIVERS  
WITH OPEN-RAIN OUTCOMES**

positive logic:  
 $Y = \bar{A}$



See page 237

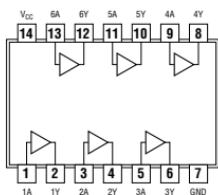
# Pin Assignments

**07**

## HEX BUFFERS/DRIVERS WITH OPEN-DRAIN OUTPUTS

positive logic:

$$Y = \bar{A}$$



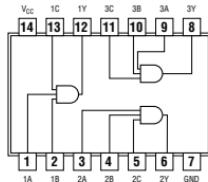
See page 237

**11**

## TRIPLE 3-INPUT POSITIVE-AND GATES

positive logic:

$$Y = A \bullet B \bullet C$$



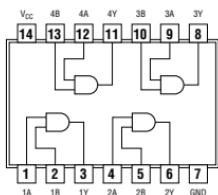
See page 241

**08**

## QUADRUPLE 2-INPUT POSITIVE-AND GATES

positive logic:

$$Y = A \bullet B$$



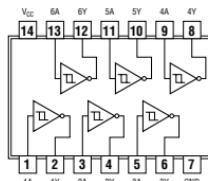
See page 238

**14**

## HEX SCHMITT-TRIGGER INVERTERS

positive logic:

$$Y = \bar{A}$$



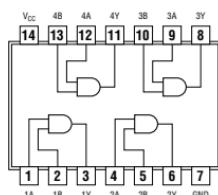
See page 242

**09**

## QUADRUPLE 2-INPUT POSITIVE-AND GATES WITH OPEN-COLLECTOR OUTPUTS

positive logic:

$$Y = A \bullet B$$



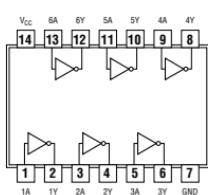
See page 239

**16**

## HEX INVERTER BUFFERS/DRIVERS WITH OPEN-COLLECTOR HIGH-VOLTAGE OUTPUTS

positive logic:

$$Y = \bar{A}$$



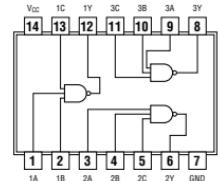
See page 243

**10**

## TRIPLE 3-INPUT POSITIVE-NAND GATES

positive logic:

$$Y = A \bullet B \bullet C$$



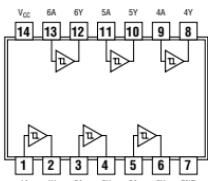
See page 240

**17**

## HEX SCHMITT-TRIGGER BUFFER

positive logic:

$$Y = A$$



See page 243

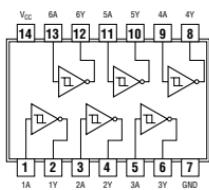
# Pin Assignments

**19**

## HEX SCHMITT-TRIGGER INVERTERS

positive logic:

$$Y = \bar{A}$$



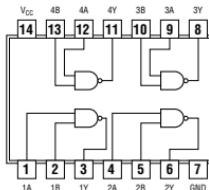
See page 244

**26**

## QUADRUPLE 2-INPUT HIGH-VOLTAGE INTERFACE POSITIVE-NAND GATES

positive logic:

$$Y = \bar{AB}$$



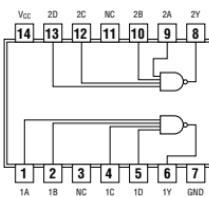
See page 247

**20**

## DUAL 4-INPUT POSITIVE-NAND GATES

positive logic:

$$Y = \bar{AB} \bullet \bar{C} \bullet \bar{D}$$



See page 245

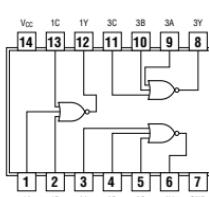
NC-No internal connection

**27**

## TRIPLE 3-INPUT POSITIVE-NOR GATES

positive logic:

$$Y = A + B + \bar{C}$$



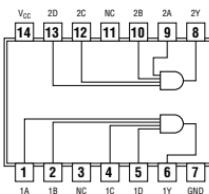
See page 247

**21**

## DUAL 4-INPUT POSITIVE-AND GATES

positive logic:

$$Y = A \bullet B \bullet C \bullet D$$



See page 246

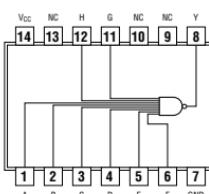
NC-No internal connection

**30**

## 8-INPUT POSITIVE-NAND GATES

positive logic:

$$Y = \bar{AB} \bullet \bar{C} \bullet \bar{D} \bullet \bar{E} \bullet \bar{F} \bullet \bar{G} \bullet \bar{H}$$



See page 248

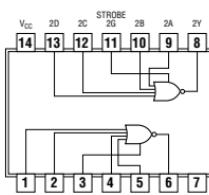
NC-No internal connection

**25**

## DUAL 4-INPUT POSITIVE-NOR GATES WITH STROBE

positive logic:

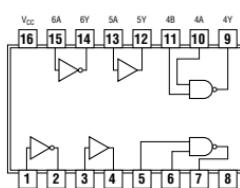
$$Y = G (A + B + C + D)$$



See page 246

**31**

## DELAY ELEMENTS



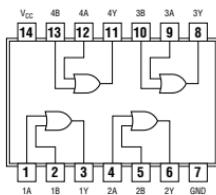
See page 248

# Pin Assignments

**32**

**QUADRUPLE 2-INPUT  
POSITIVE-OR GATES**

positive logic:  
 $Y = A + B$

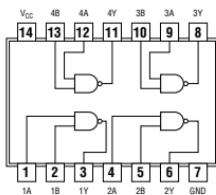


See page 249

**37**

**QUADRUPLE 2-INPUT  
POSITIVE-NAND BUFFERS**

positive logic:  
 $Y = \bar{A} \cdot \bar{B}$

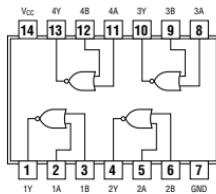


See page 252

**33**

**QUADRUPLE 2-INPUT POSITIVE-NOR BUFFERS  
WITH OPEN-COLLECTOR OUTPUTS**

positive logic:  
 $Y = \bar{A} + \bar{B}$

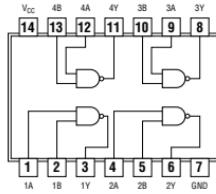


See page 250

**38**

**QUADRUPLE 2-INPUT POSITIVE-NAND BUFFERS  
WITH OPEN-COLLECTOR OUTPUTS**

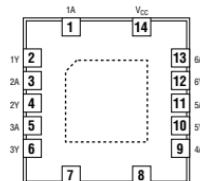
positive logic:  
 $Y = \bar{A} \cdot \bar{B}$



See page 253

**34**

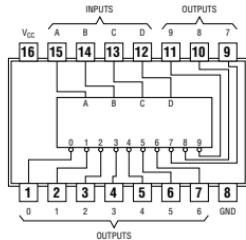
**HEX BUFFER GATE**



See page 250

**42**

**4-LINE-TO-10-LINE DECODERS (1 of 10)**

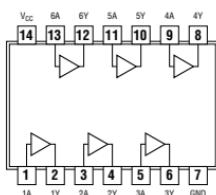


See page 254

**35**

**HEX NONINVERTERS  
WITH OPEN-COLLECTOR OUTPUTS**

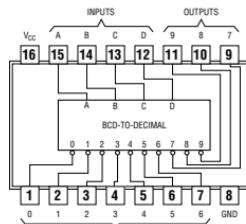
positive logic:  
 $Y = A$



See page 251

**45**

**BCD-TO-DECIMAL DECODERS/DRIVERS**

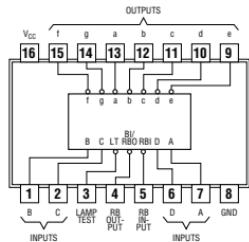


See page 256

# Pin Assignments

**47**

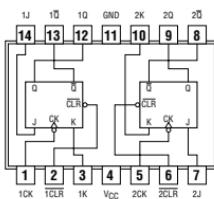
**BCD-TO-SEVEN-SEGMENT DECODERS/DRIVERS**



See page 258

**73**

**DUAL J-K FLIP-FLOPS WITH CLEAR**



See page 262

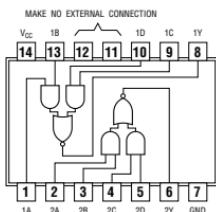
**51**

**AND-OR-INVERT GATES**

**'51, S51 DUAL 2-WIDE 2-INPUT**

positive logic:

$$Y = \overline{AB} + \overline{CD}$$



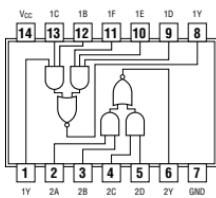
**AND-OR-INVERT GATES**

**'LS51 2-WIDE 3-INPUT, 2-WIDE 2-INPUT**

positive logic:

$$1Y = (1A 1B 1C) + (1D 1E 1F)$$

$$2Y = (2A 2B) + (2C 2D)$$

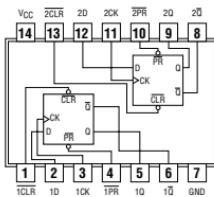


See page 260

**74**

**DUAL D-TYPE POSITIVE-EDGE-TRIGGERED FLIP-FLOPS**

**WITH CLEAR AND PRESET**



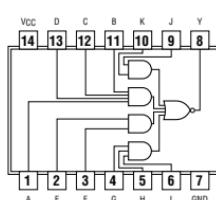
See page 264

**64**

**4-2-3-2 INPUT AND-OR INVERT GATES**

positive logic:

$$Y = \overline{ABCD} + \overline{EF} + \overline{GHI} + \overline{JK}$$

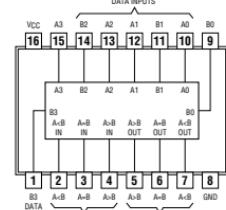


See page 261

**85**

**4-BIT MAGNITUDE COMPARATORS**

DATA INPUTS



See page 267

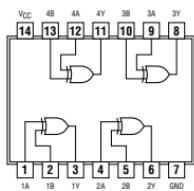
# Pin Assignments

**86**

## QUADRUPLE 2-INPUT EXCLUSIVE-OR GATES

positive logic:

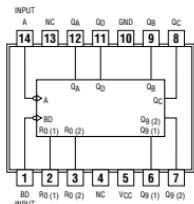
$$Y = A = B \text{ or } Y = \overline{A}\overline{B} + \overline{AB}$$



See page 268

**90**

## DECADE COUNTER

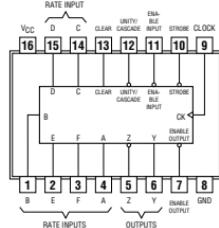


See page 269

NC-No internal connection

**97**

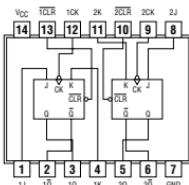
## SYNCHRONOUS 6-BIT BINARY RATE MULTIPLIERS



See page 272

**107**

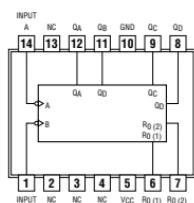
## DUAL J-K FLIP-FLOPS WITH CLEAR



See page 274

**92**

## DIVIDE-BY-TWELVE DECODE COUNTERS

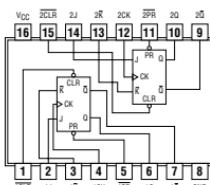


See page 270

NC-No internal connection

**109**

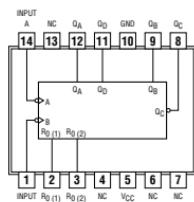
## DUAL J-K POSITIVE-EDGE-TRIGGERED FLIP-FLOPS WITH CLEAR AND PRESET



See page 276

**93**

## 4-BIT BINARY COUNTERS

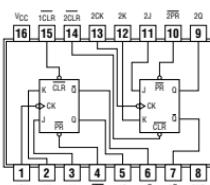


See page 271

NC-No internal connection

**112**

## DUAL J-K NEGATIVE-EDGE-TRIGGERED FLIP-FLOPS WITH CLEAR AND PRESET

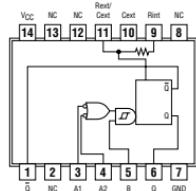


See page 278

# Pin Assignments

**121**

MONOSTABLE MULTIVIBRATORS WITH SCHMITT-TRIGGER INPUTS



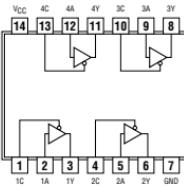
See page 280

NC-No internal connection

**125**

QUADRUPLE BUS BUFFER GATES  
WITH 3-STATE OUTPUTS

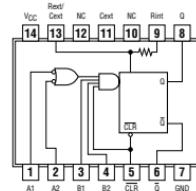
positive logic:  
 $Y = A$



See page 284

**122**

RETRIGGERABLE MONOSTABLE MULTIVIBRATORS



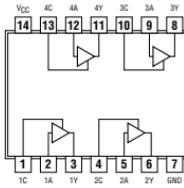
See page 281

NC-No internal connection

**126**

QUADRUPLE BUS BUFFER GATES  
WITH 3-STATE OUTPUTS

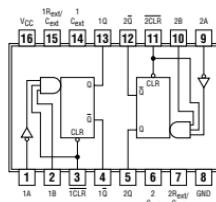
positive logic:  
 $Y = A$



See page 285

**123**

DUAL RETRIGGERABLE MONOSTABLE  
MULTIVIBRATORS WITH SCHMITT-TRIGGER INPUTS

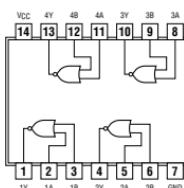


See page 282

**128**

SN54128...75- $\Omega$  LINE DRIVER  
SN74128...50- $\Omega$  LINE DRIVER

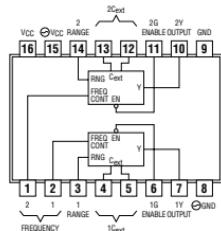
positive logic:  
 $Y = \bar{A} + B$



See page 286

**124**

DUAL VOLTAGE-CONTROLLED OSCILLATORS

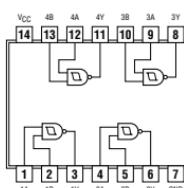


See page 283

**132**

QUADRUPLE POSITIVE-NAND GATES  
WITH SCHMITT TRIGGER INPUTS

positive logic:  
 $Y = A \cdot B$



See page 286

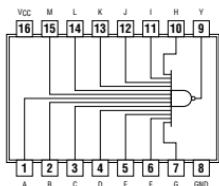
# Pin Assignments

**133**

**13-INPUT POSITIVE-NAND GATES**

positive logic:

$$Y = A \cdot B \cdot C \cdot D \cdot E \cdot F \cdot G \cdot H \cdot I \cdot J \cdot K \cdot L \cdot M$$



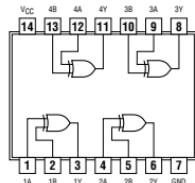
See page 287

**136**

**QUADRUPLE 2-INPUT EXCLUSIVE-OR GATES  
WITH OPEN COLLECTOR OUTPUTS**

positive logic:

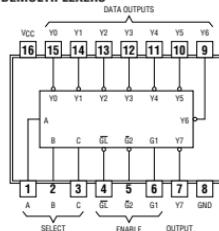
$$Y = A \cdot B = \bar{A}B + A\bar{B}$$



See page 287

**137**

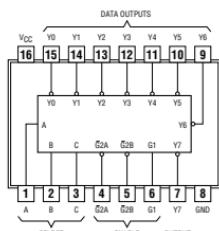
**3-LINE TO 8-LINE DECODERS/DEMULITPLEXERS  
WITH ADDRESS LATCHES**



See page 288

**138**

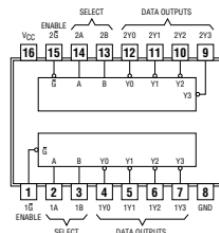
**3-LINE TO 8-LINE DECODERS/DEMULITPLEXERS**



See page 290

**139**

**DUAL 2-LINE TO 4-LINE DECODERS/DEMULITPLEXERS**



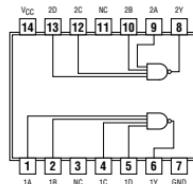
See page 292

**140**

**DUAL 4-INPUT POSITIVE-NAND  
50-Ω LINE DRIVERS**

positive logic:

$$Y = ABCD$$

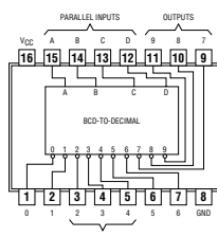


NC-No internal connection

See page 294

**145**

**BCD-TO-DECIMAL DECODERS/DRIVERS**

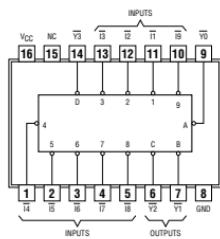


See page 295

# Pin Assignments

**147**

10-LINE TO 4-LINE BCD PRIORITY ENCODER

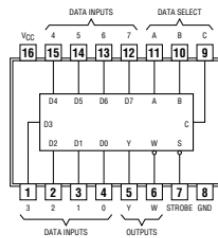


NC-No internal connection

See page 296

**151**

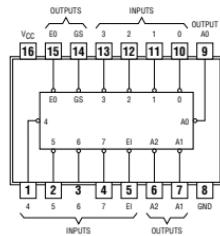
8-LINE TO 1-LINE DATA SELECTORS/MULTIPLEXERS



See page 302

**148**

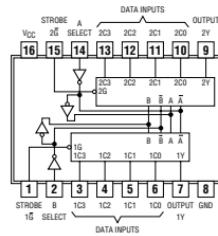
8-LINE TO 3-LINE PRIORITY ENCODERS



See page 298

**153**

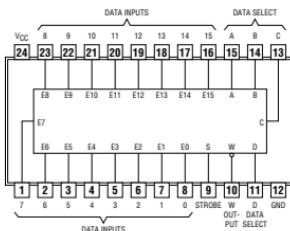
DUAL 4-LINE TO 1-LINE DATA SELECTORS/MULTIPLEXERS



See page 304

**150**

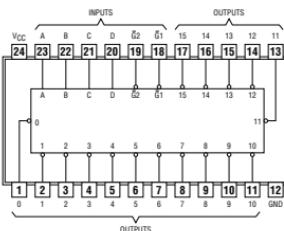
16-LINE TO 1-LINE DATA SELECTOR/MULTIPLEXER



See page 300

**154**

4-LINE TO 16-LINE DECODERS/DEMULTIPLEXERS



See page 306

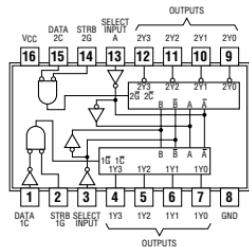
# Pin Assignments

**155**

DUAL 2-LINE TO 4-LINE DECODERS/DEMULITPLEXERS

**156**

DUAL 2-LINE TO 4-LINE DECODERS/DEMULITPLEXERS  
WITH OPEN-COLLECTOR OUTPUTS

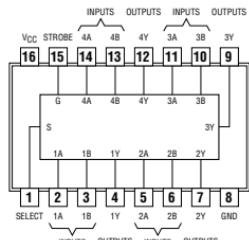


See page 308, 310

**157**

**158**

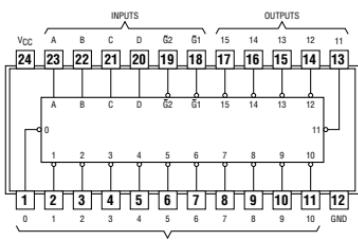
QUADRUPLE 2-LINE TO 1-LINE DATA SELECTORS/MULTIPLEXERS



See page 312, 314

**159**

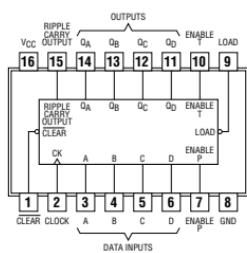
4-LINE TO 16-LINE DECODERS/DEMULITPLEXERS  
WITH OPEN-COLLECTOR OUTPUTS



See page 316

**161**

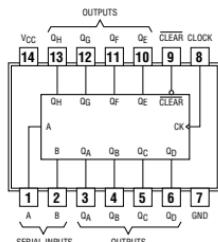
4-BIT SYNCHRONOUS BINARY COUNTERS



See page 318, 320

**164**

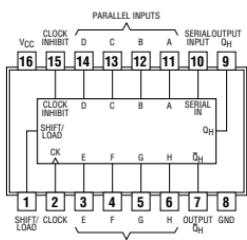
8-BIT PARALLEL-OUT SERIAL SHIFT REGISTERS



See page 322

**165**

PARALLEL-LOAD 8-BIT SHIFT REGISTERS

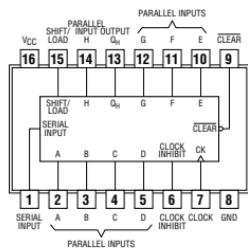


See page 324

# Pin Assignments

**166**

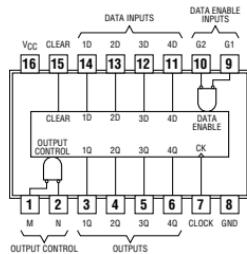
8-BIT PARALLEL-LOAD SHIFT REGISTERS



See page 326

**173**

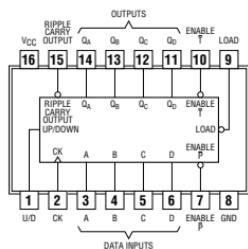
4-BIT D-TYPE REGISTERS WITH 3-STATE OUTPUTS



See page 332

**169**

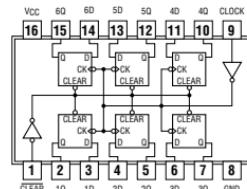
SYNCHRONOUS 4-BIT UP/DOWN BINARY COUNTERS



See page 328

**174**

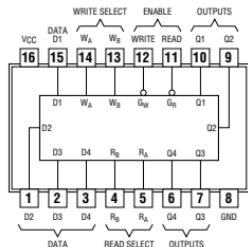
HEX D-TYPE FLIP-FLOPS WITH CLEAR



See page 334

**170**

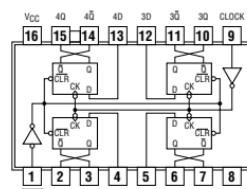
4-BY-4-REGISTER FILES WITH OPEN-COLLECTOR OUTPUTS



See page 330

**175**

QUADRUPLE D-TYPE FLIP-FLOPS WITH CLEAR

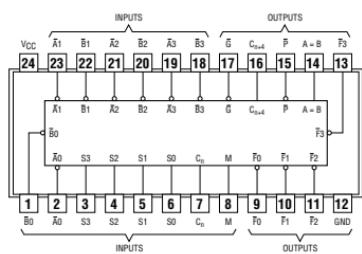


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## Pin Assignments

181

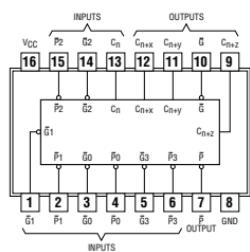
## ARITHMETIC LOGIC UNITS/FUNCTION GENERATORS



See page 336

182

## LOOK-AHEAD CARRY GENERATOR



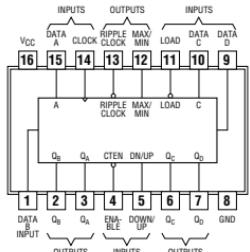
See page 338

190

## SYNCHRONOUS 4-BIT UP/DOWN DECADE AND BINARY COUNTERS

191

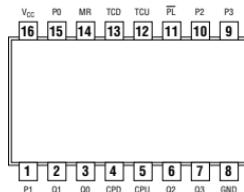
## 4-BIT SYNCHRONOUS UP/DOWN BINARY COUNTERS



See page 340, 342

192

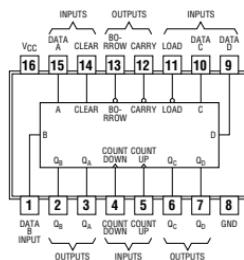
## **PRESETTABLE SYNCHRONOUS 4-BIT UP/DOWN COUNTERS**



See page 344

193

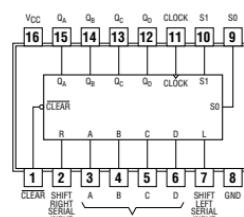
## 4-BIT SYNCHRONOUS UP/DOWN COUNTERS (DUAL CLOCK WITH CLEAR)



See page 346

194

## 4-BIT BIDIRECTIONAL UNIVERSAL SHIFT REGISTERS

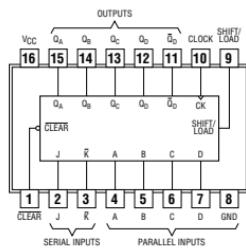


See page 348

# Pin Assignments

**195**

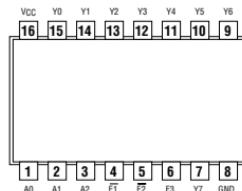
4-BIT PARALLEL-ACCESS SHIFT REGISTERS



See page 350

**238**

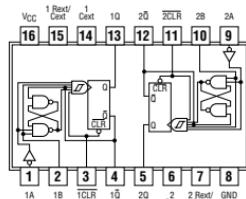
3-LINE TO 8-LINE DECODERS/DEMULTIPLEXERS



See page 356

**221**

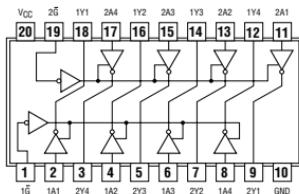
DUAL MONOSTABLE MULTIVIBRATORS WITH SCHMITT-TRIGGER INPUTS



See page 352

**240**

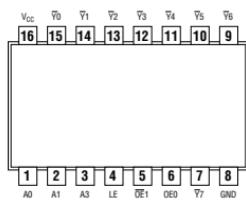
OCTAL BUFFERS/DRIVERS WITH 3-STATE OUTPUTS



See page 358

**237**

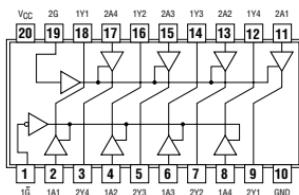
3-LINE TO 8-LINE DECODERS/DEMULTIPLEXERS WITH ADDRESS LATCHES



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**241**

OCTAL BUFFERS/DRIVERS WITH 3-STATE OUTPUTS

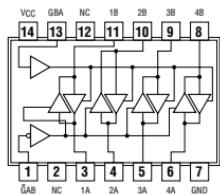


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## Pin Assignments

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## QUADRUPLE BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

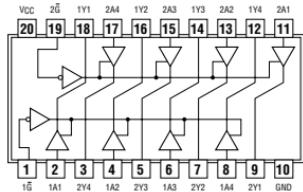


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NC-No internal connection

244

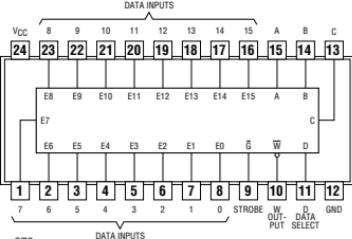
## OCTAL BUFFERS/DRIVERS WITH 3-STATE OUTPUTS



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250

## **1-OF-16 DATA GENERATORS/MULTIPLEXERS WITH 3-STATE OUTPUTS**

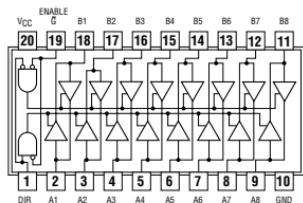


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DATA INPUTS

245

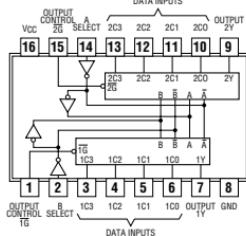
#### **E10 OCTAL BUS TRANSCEIVERS WITH 3-STATE OUTPUTS**



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253

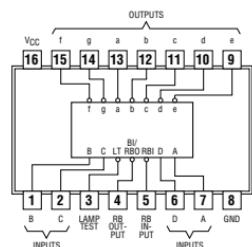
## **DUAL 4-LINE TO 1-LINE DATA SELECTORS/MULTIPLEXERS WITH 3-STATE OUTPUTS**



See page 374

247

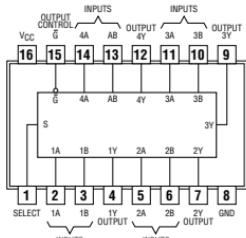
#### **BCD-TO-SEVEN-SEGMENT DECODERS/DRIVERS**



See page 269

257

## **QUADRUPLE 2-LINE TO 1-LINE DATA SELECTORS/MULTIPLEXERS WITH 3-STATE OUTPUTS**

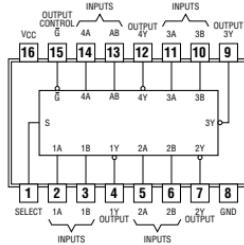


See page 376

# Pin Assignments

**258**

QUADRUPLE 4-LINE TO 1-LINE DATA SELECTORS/MUXES  
WITH 3-STATE OUTPUTS

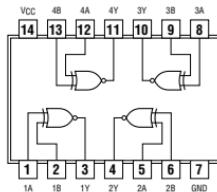


See page 378

**266**

QUADRUPLE 2-INPUT EXCLUSIVE-NOR GATES  
WITH OPEN-DRain OUTPUTS

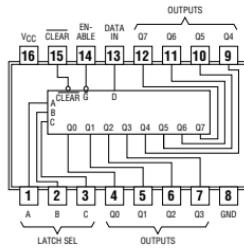
positive logic:  
 $Y = \bar{A} - B$



See page 383

**259**

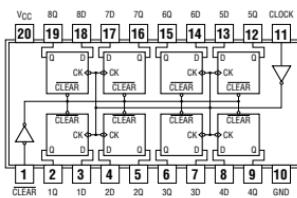
8-BIT ADDRESSABLE LATCHES



See page 380

**273**

OCTAL D-TYPE FLIP-FLOPS WITH CLEAR



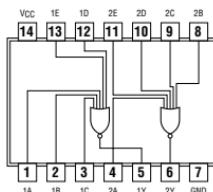
See page 384

**260**

DUAL 5-INPUT POSITIVE-NOR GATES

positive logic:

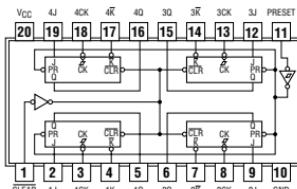
$$Y = A + B + C + D + E$$



See page 382

**276**

QUADRUPLE J-K FLIP-FLOPS



See page 386

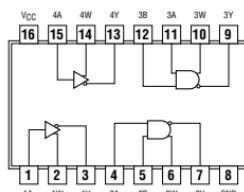
**265**

QUADRUPLE COMPLEMENTARY-OUTPUT ELEMENTS

positive logic:

$$Y = \bar{A}, W = A$$

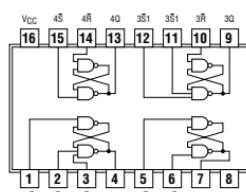
$$Y = AB, W = AB$$



See page 382

**279**

QUADRUPLE S-R LATCHES

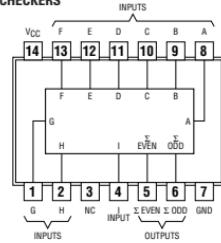


See page 387

# Pin Assignments

**280**

9-BIT PARITY GENERATORS/CHECKERS

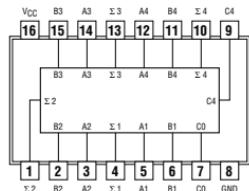


See page 388

NC-No internal connection

**283**

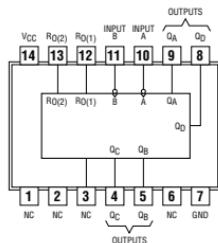
4-BIT BINARY FULL ADDERS WITH FAST CARRY



See page 390

**293**

4-BIT BINARY COUNTERS

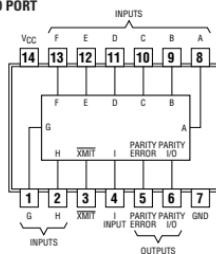


See page 396

NC-No internal connection

**286**

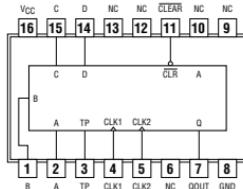
9-BIT ODD/EVEN PARITY GENERATORS/CHECKERS  
WITH BUS DRIVER I/O PORT



See page 392

**297**

DIGITAL PHASE-LOCKED-LOOP FILTERS

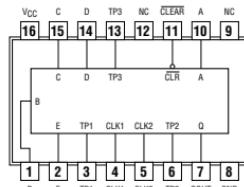


See page 400

NC-No internal connection

**292**

PROGRAMMABLE FREQUENCY DIVIDERS/DIGITAL TIMERS

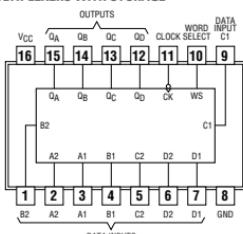


See page 394

NC-No internal connection

**298**

QUADRUPLE 2-INPUT MULTIPLEXERS WITH STORAGE

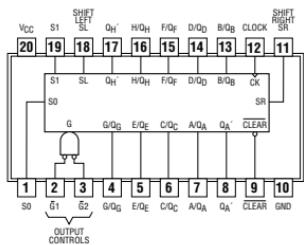


See page 402

# Pin Assignments

**299**

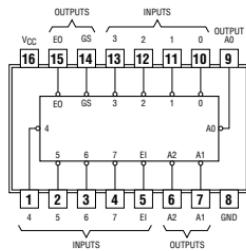
8-BIT UNIVERSAL SHIFT/STORAGE REGISTERS WITH 3-STATE OUTPUTS



See page 404

**348**

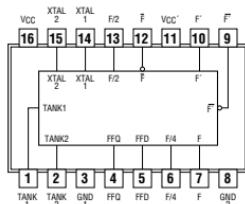
8-LINE TO 3-LINE PRIORITY ENCODERS WITH 3-STATE OUTPUTS



See page 410

**321**

CRYSTAL-CONTROLLED OSCILLATORS



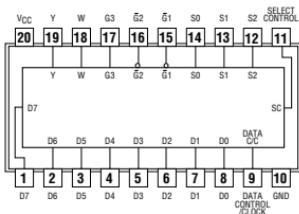
See page 406

**354**

8-LINE TO 1-LINE DATA SELECTORS/MULTIPLEXERS/TRANSPARENT/REGISTERS WITH 3-STATE OUTPUTS

**356**

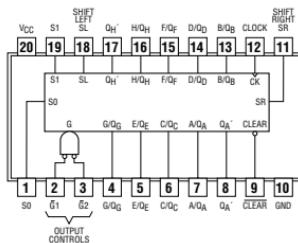
8-INPUT MULTIPLEXER/REGISTERS 3-STATE



See page 412, 414

**323**

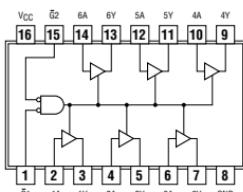
8-BIT UNIVERSAL SHIFT/STORAGE REGISTERS WITH SYNCHRONOUS CLEAR AND 3-STATE OUTPUTS



See page 408

**365**

HEX BUFFERS AND LINE DRIVERS WITH 3-STATE OUTPUTS

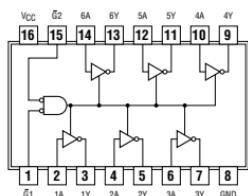


See page 416

# Pin Assignments

**366**

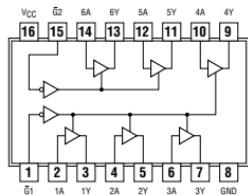
HEX BUFFERS AND LINE DRIVERS WITH 3-STATE OUTPUTS



See page 417

**367**

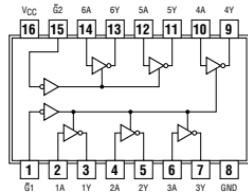
HEX BUFFERS AND LINE DRIVERS WITH 3-STATE OUTPUTS



See page 418

**368**

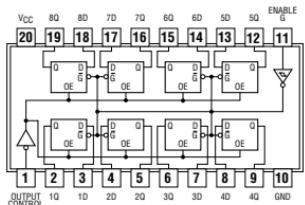
HEX INVERTING BUFFERS AND LINE DRIVERS WITH 3-STATE OUTPUTS



See page 419

**373**

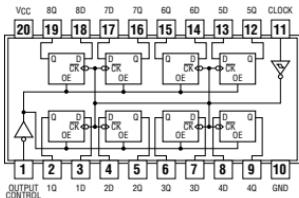
OCTAL TRANSPARENT D-TYPE LATCHES WITH 3-STATE OUTPUTS



See page 420

**374**

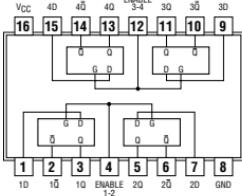
OCTAL EDGE-TRIGGERED D-TYPE FLIP-FLOPS WITH 3-STATE OUTPUTS



See page 422

**375**

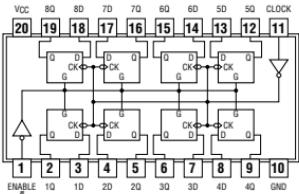
4-BIT BISTABLE LATCHES



See page 424

**377**

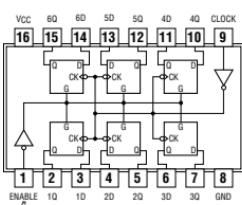
OCTAL D-TYPE FLIP-FLOPS WITH CLOCK ENABLE



See page 425

**378**

HEX D-TYPE FLIP-FLOPS WITH CLOCK ENABLE

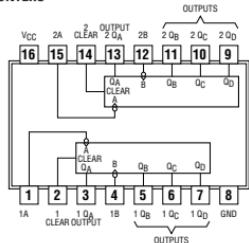


See page 426

# Pin Assignments

**390**

DUAL 4-BIT DECADE COUNTERS

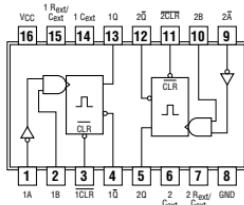


See page 427

**423**

RETRIGGERABLE MONOSTABLE MULTIVIBRATORS

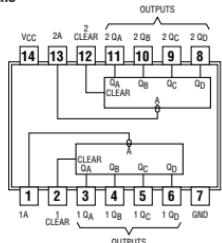
positive logic:  
 $Y = A$



See page 431

**393**

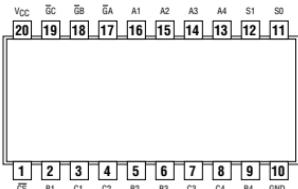
DUAL 4-BIT BINARY COUNTERS



See page 428

**442**

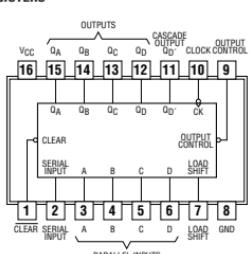
QUADRUPLE TRIDIRECTIONAL BUS TRANSCEIVERS



See page 432

**395**

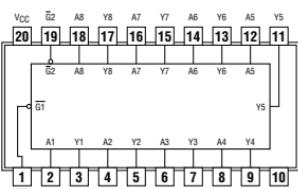
CASCADABLE SHIFT REGISTERS



See page 429

**465**

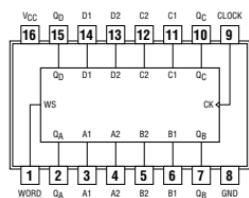
OCTAL BUFFERS WITH 3-STATE OUTPUTS



See page 433

**399**

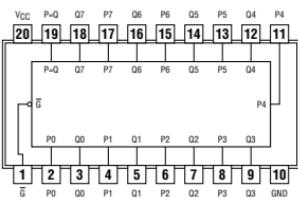
QUADRUPLE 2-INPUT MULTIPLEXERS WITH STORAGE



See page 430

**518**

OCTAL BINARY/BCD IDENTITY COMPARATORS WITH ENABLE



See page 433

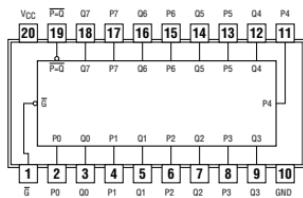
# Pin Assignments

**520**

OCTAL BINARY/BCD IDENTITY COMPARATORS WITH ENABLE

**521**

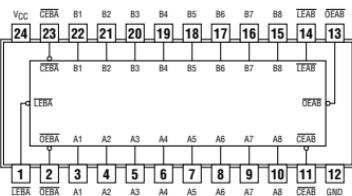
8-BIT IDENTITY COMPARATORS WITH OPEN-COLLECTOR OUTPUTS



See page 434, 435

**543**

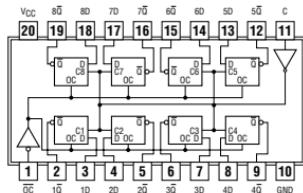
OCTAL REGISTERED TRANSCEIVERS WITH 3-STATE OUTPUTS



See page 440

**533**

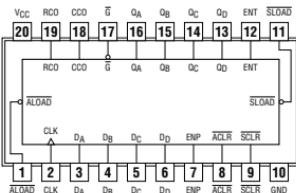
OCTAL TRANSPARENT D-TYPE LATCHES WITH 3-STATE OUTPUTS



See page 436

**561**

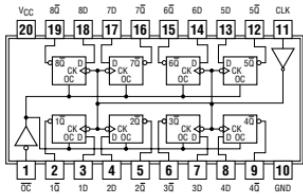
SYNCHRONOUS 4-BIT COUNTERS WITH 3-STATE OUTPUTS



See page 442

**534**

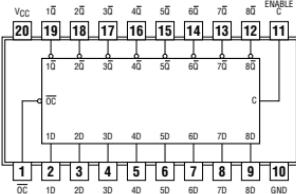
OCTAL EDGE-TRIGGERED D-TYPE FLIP-FLOPS WITH 3-STATE OUTPUTS



See page 437

**563**

OCTAL D-TYPE TRANSPARENT LATCHES WITH 3-STATE OUTPUTS

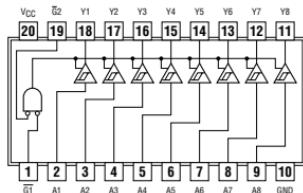


See page 444

**540**

**541**

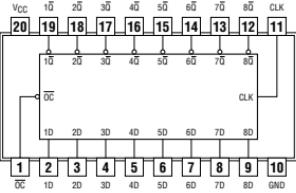
OCTAL BUFFERS/DRIVERS WITH 3-STATE OUTPUTS



See page 438, 439

**564**

OCTAL D-TYPE EDGE-TRIGGERED FLIP-FLOPS WITH 3-STATE OUTPUTS

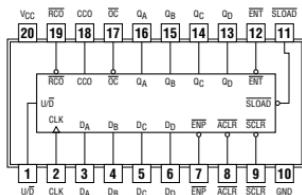


See page 445

# Pin Assignments

**569**

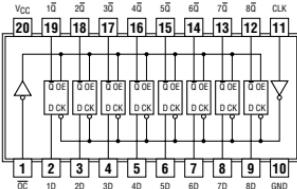
SYNCHRONOUS 4-BIT UP/DOWN BINARY COUNTERS WITH 3-STATE OUTPUTS



See page 446

**576**

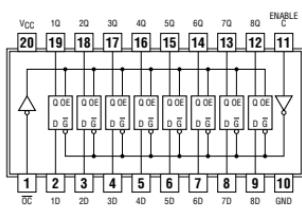
OCTAL D-TYPE EDGE-TRIGGERED FLIP-FLOPS WITH 3-STATE OUTPUTS



See page 453

**573**

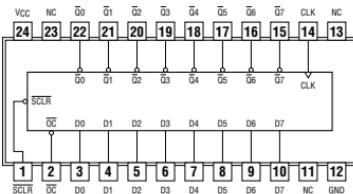
OCTAL TRANSPARENT D-TYPE LATCHES WITH 3-STATE OUTPUTS



See page 448

**577**

OCTAL D-TYPE EDGE-TRIGGERED FLIP-FLOPS WITH 3-STATE OUTPUTS

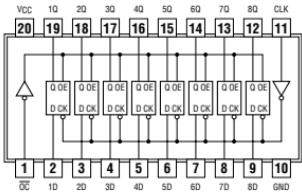


See page 454

NC-No internal connection

**574**

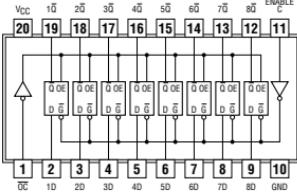
OCTAL EDGE-TRIGGERED D-TYPE FLIP-FLOPS WITH 3-STATE OUTPUTS



See page 450

**580**

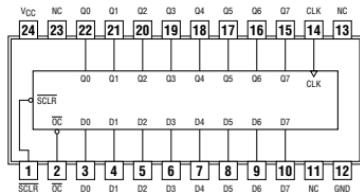
OCTAL D-TYPE TRANSPARENT LATCHES WITH 3-STATE OUTPUTS



See page 455

**575**

OCTAL D-TYPE EDGE-TRIGGERED FLIP-FLOPS WITH 3-STATE OUTPUTS

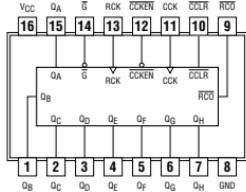


See page 452

NC-No internal connection

**590**

8-BIT BINARY COUNTERS WITH 3-STATE OUTPUT REGISTERS

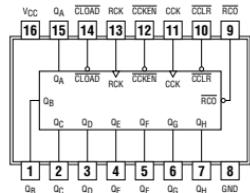


See page 456

# Pin Assignments

**592**

8-BIT BINARY COUNTERS WITH INPUT REGISTERS



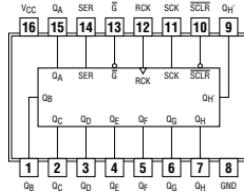
See page 458

**595**

8-BIT SHIFT REGISTERS WITH 3-STATE OUTPUT REGISTERS

**596**

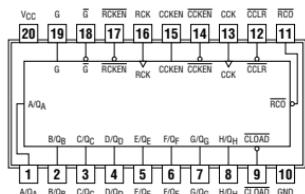
8-BIT SHIFT REGISTERS WITH OUTPUT LATCHES



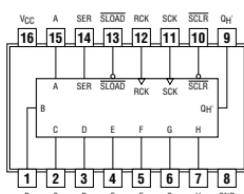
See page 464, 466

**593**

8-BIT BINARY COUNTERS WITH INPUT REGISTERS



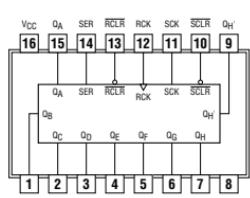
See page 460



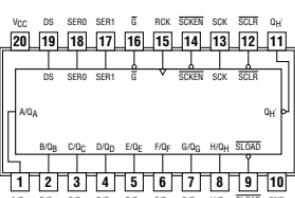
See page 468

**594**

8-BIT SHIFT REGISTERS WITH OUTPUT REGISTERS



See page 462



See page 470

# Pin Assignments

**620**

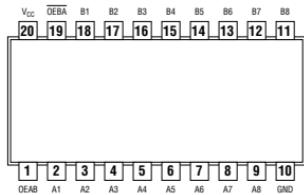
OCTAL BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

**621**

OCTAL BUS TRANSCEIVERS

**623**

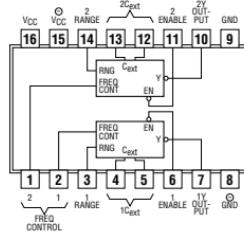
OCTAL BUS TRANSCEIVERS WITH 3-STATE OUTPUTS



See page 472, 473, 474

**629**

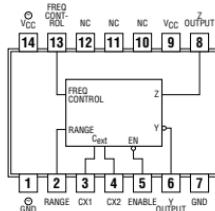
DUAL VOLTAGE-CONTROLLED OSCILLATORS



See page 477

**624**

VOLTAGE-CONTROLLED OSCILLATORS

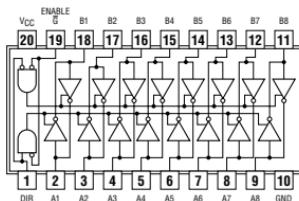


NC-No internal connection

See page 475

**638**

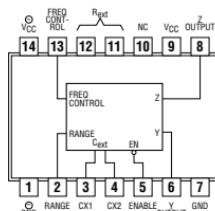
OCTAL BUS TRANSCEIVERS



See page 478

**628**

VOLTAGE-CONTROLLED OSCILLATORS

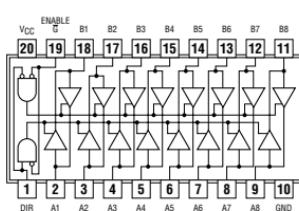


NC-No internal connection

See page 476

**639**

OCTAL BUS TRANSCEIVERS



See page 479

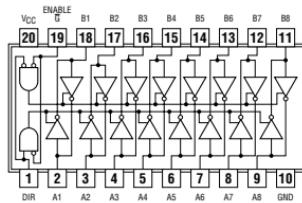
# Pin Assignments

**640**

OCTAL BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

**642**

OCTAL BUS TRANSCEIVERS WITH OPEN-COLLECTOR OUTPUTS



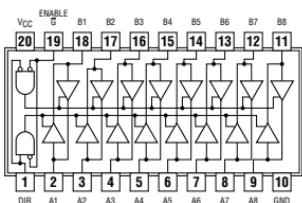
See page 480, 482

**641**

OCTAL BUS TRANSCEIVERS WITH OPEN-COLLECTOR OUTPUTS

**645**

OCTAL BUS TRANSCEIVERS WITH 3-STATE OUTPUTS



See page 481, 483

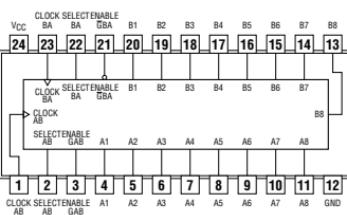
**651**

**652**

**653**

**654**

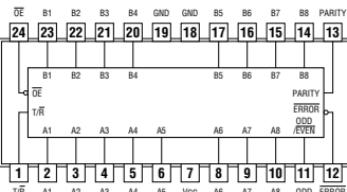
OCTAL BUS TRANSCEIVERS AND REGISTERS WITH 3-STATE OUTPUTS



See page 490, 492, 494, 496

**657**

OCTAL BUS TRANSCEIVERS WITH PARITY GENERATORS/CHECKERS AND 3-STATE OUTPUTS



See page 498

**666**

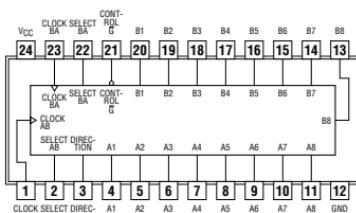
OCTAL BUS TRANSCEIVERS AND REGISTERS WITH 3-STATE OUTPUTS

**667**

OCTAL BUS TRANSCEIVERS AND REGISTERS WITH OPEN-COLLECTOR OUTPUTS

**668**

OCTAL BUS TRANSCEIVERS AND REGISTERS WITH 3-STATE OUTPUTS

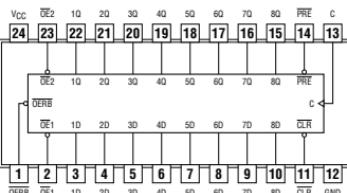


See page 484, 486, 488

**666**

**667**

8-BIT D-TYPE TRANSPARENT READ-BACK LATCHES WITH 3-STATE OUTPUTS

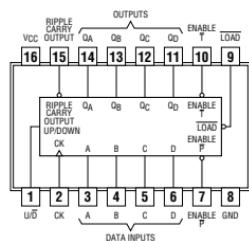


See page 500, 501

# Pin Assignments

**669**

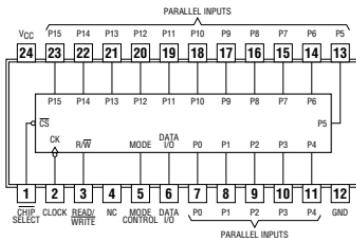
SYNCHRONOUS 4-BIT UP/DOWN COUNTERS



See page 502

**674**

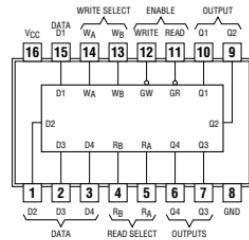
16-BIT SHIFT REGISTERS



See page 508

**670**

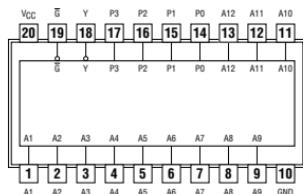
4-BY-4 REGISTER FILES WITH 3-STATE OUTPUTS



See page 504

**679**

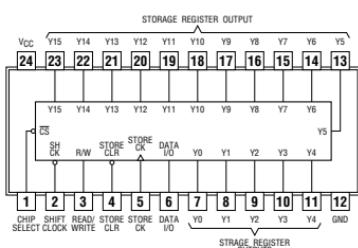
12-BIT ADDRESS COMPARATOR



See page 510

**673**

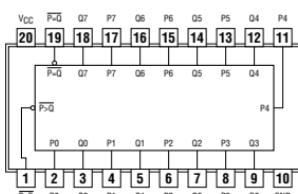
16-BIT SHIFT REGISTERS



See page 506

**682**

8-BIT MAGNITUDE COMPARATORS

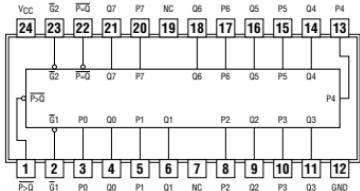


See page 512, 514

# Pin Assignments

**686**

8-BIT MAGNITUDE/IDENTITY COMPARATORS

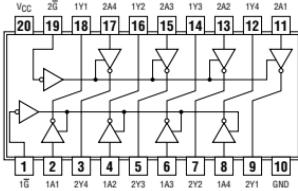


NC-No internal connection

See page 516

**756**

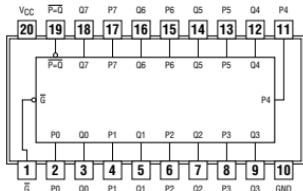
OCTAL BUFFER/DRIVER WITH OPEN-COLLECTOR OUTPUTS



See page 524

**688**

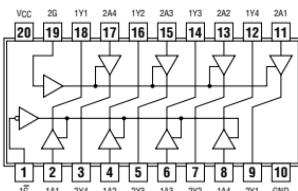
8-BIT IDENTITY COMPARATORS



See page 518

**757**

OCTAL BUFFER/DRIVER WITH OPEN-COLLECTOR OUTPUTS

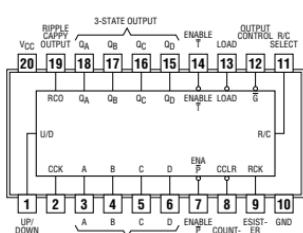


See page 525

**697**

**699**

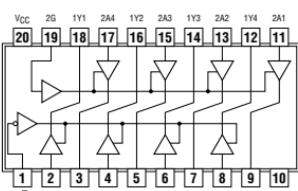
SYNCHRONOUS UP/DOWN COUNTERS WITH OUTPUT REGISTERS AND MULTIPLEXED 3-STATE OUTPUTS



See page 520, 522

**760**

OCTAL BUFFERS/DRIVERS WITH OPEN-COLLECTOR OUTPUTS



See page 526

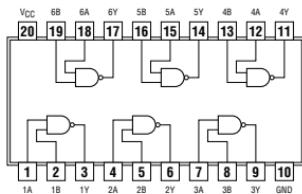
# Pin Assignments

**804**

HEX 2-INPUT NAND DRIVERS

positive logic:

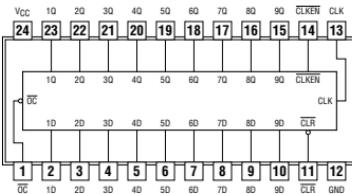
$$Y = \bar{A} \cdot \bar{B}$$



See page 527

**823**

9-BIT BUS-INTERFACE FLIP-FLOPS WITH 3-STATE OUTPUTS



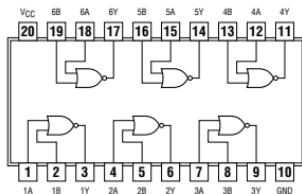
See page 530

**805**

HEX 2-INPUT NOR DRIVERS

positive logic:

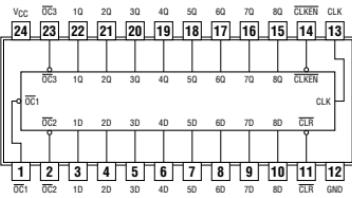
$$Y = A + B$$



See page 528

**825**

8-BIT BUS-INTERFACE FLIP-FLOPS WITH 3-STATE OUTPUTS



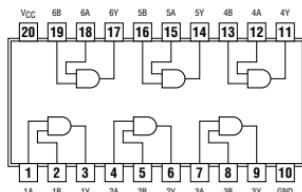
See page 531

**808**

HEX 2-INPUT AND DRIVERS

positive logic:

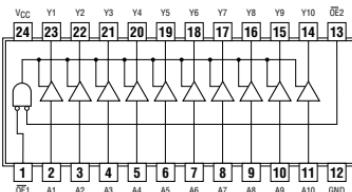
$$Y = A + B$$



See page 528

**827**

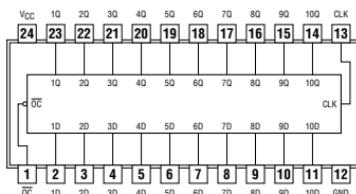
10-BIT BUFFERS/DRIVERS WITH 3-STATE OUTPUTS



See page 532

**821**

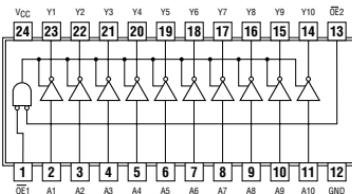
10-BIT BUS-INTERFACE FLIP FLOPS WITH 3-STATE OUTPUTS



See page 529

**828**

10-BIT BUFFERS/DRIVERS WITH 3-STATE OUTPUTS



See page 532

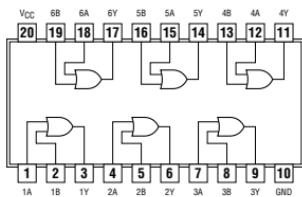
# Pin Assignments

**832**

HEX 2-INPUT OR DRIVERS

positive logic:

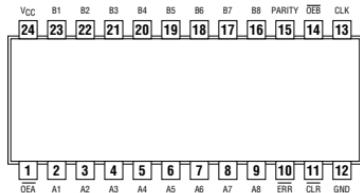
$Y = A + B$



See page 533

**833**

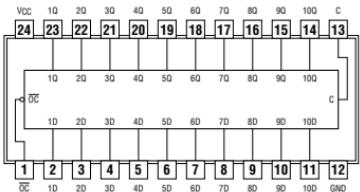
8-BIT TO 9-BIT PARITY BUS TRANSCEIVERS



See page 534

**841**

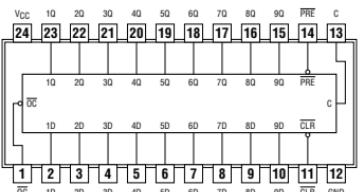
10-BIT BUS-INTERFACE D-TYPE LATCHES WITH 3-STATE OUTPUTS



See page 536

**843**

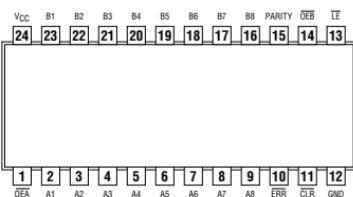
9-BIT BUS-INTERFACE D-TYPE LATCHES WITH 3-STATE OUTPUTS



See page 537

**853**

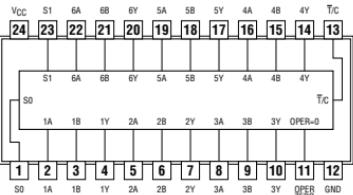
8-BIT TO 9-BIT PARITY BUS TRANSCEIVERS



See page 538

**857**

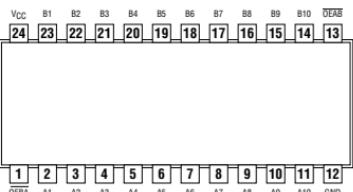
HEX 2-TO-1 UNIVERSAL MULTIPLEXERS WITH 3-STATE OUTPUTS



See page 540

**861**

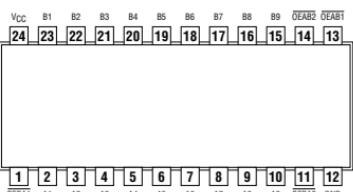
10-BIT TRANSCEIVERS WITH 3-STATE OUTPUTS



See page 542

**863**

9-BIT BUS TRANSCEIVERS WITH 3-STATE OUTPUTS



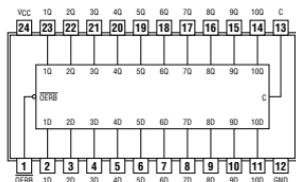
See page 543



# Pin Assignments

**994**

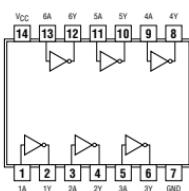
10-BIT D-TYPE TRANSPARENT READ-BACK LATCH



See page 558

**1005**

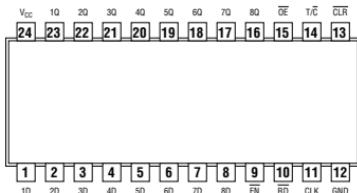
HEX INVERTING BUFFERS WITH OPEN-COLLECTOR OUTPUTS



See page 561

**996**

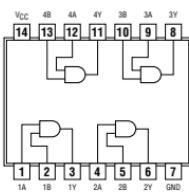
8-BIT D-TYPE EDGE-TRIGGERED READ-BACK LATCHES



See page 559

**1008**

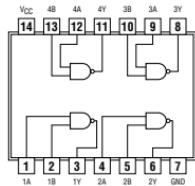
QUADRUPLE 2-INPUT POSITIVE-AND BUFFER/DRIVER



See page 561

**1000**

QUADRUPLE 2-INPUT POSITIVE-NAND BUFFERS/DRIVERS

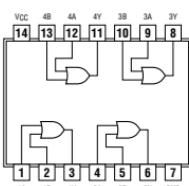


See page 560

**1032**

QUADRUPLE 2-INPUT POSITIVE-OR BUFFERS/DRIVERS

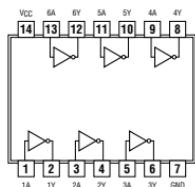
positive logic:  
 $Y = A + B$



See page 562

**1004**

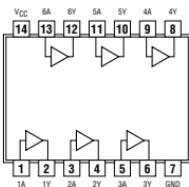
HEX INVERTING DRIVERS



See page 560

**1034**

HEX DRIVERS

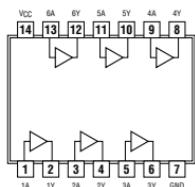


See page 562

# Pin Assignments

**1035**

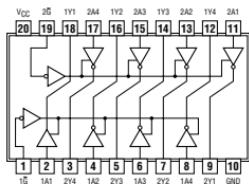
HEX NONINVERTING BUFFERS WITH OPEN-COLLECTOR OUTPUTS



See page 563

**1240**

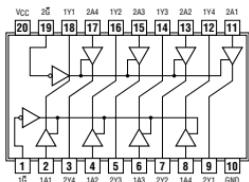
OCTAL BUFFER AND LINE DRIVER WITH 3-STATE OUTPUTS



See page 563

**1244**

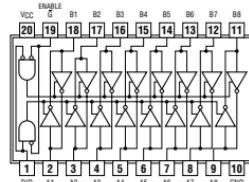
OCTAL BUFFERS AND DRIVERS WITH 3-STATE OUTPUTS



See page 564

**1245**

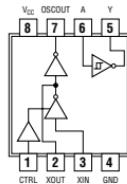
OCTAL BUS TRANSCEIVERS WITH 3-STATE OUTPUTS



See page 564

**1404**

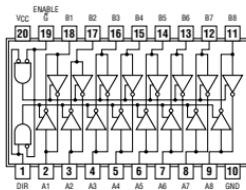
OSCILLATOR DRIVER FOR CRYSTAL OSCILLATOR OR CERAMIC RESONATOR



See page 565

**1640**

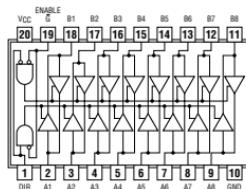
OCTAL BUS TRANSCEIVERS WITH 3-STATE OUTPUTS



See page 566

**1645**

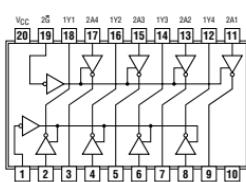
OCTAL BUS TRANSCEIVERS WITH 3-STATE OUTPUTS



See page 567

**2240**

OCTAL BUFFERS AND LINE/MOS DRIVERS WITH 3-STATE OUTPUTS

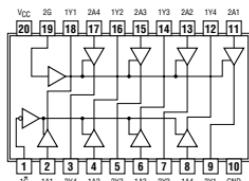


See page 568

# Pin Assignments

## 2241

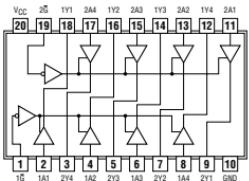
OCTAL BUFFERS AND LINE/MOS DRIVERS WITH 3-STATE OUTPUTS



See page 569

## 2244

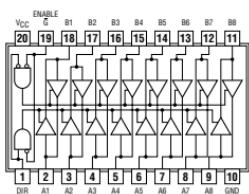
OCTAL BUFFERS AND LINE/MOS DRIVERS WITH 3-STATE OUTPUTS



See page 570

## 2245

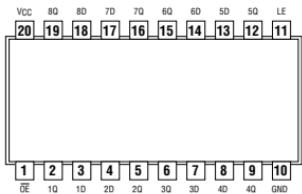
OCTAL TRANSCEIVER AND LINE/MOS DRIVERS WITH 3-STATE OUTPUTS



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## 2373

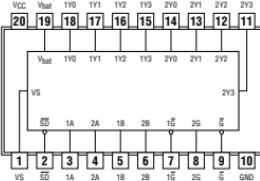
25- $\Omega$  OCTAL TRANSPARENT D-TYPE LATCH WITH 3-STATE OUTPUTS



See page 572

## 2414

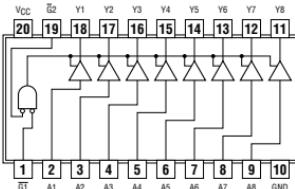
MEMORY DECODER WITH ON-CHIP SUPPLY VOLTAGE MONITOR



See page 573

## 2541

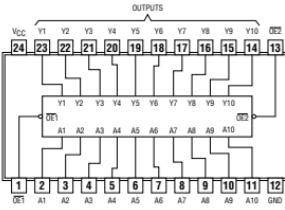
OCTAL LINE DRIVER/MOS DRIVER WITH 3-STATE OUTPUTS



See page 574

## 2827

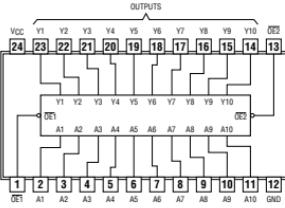
10-BIT BUFFERS/DRIVERS WITH 3-STATE OUTPUTS



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## 2828

10-BIT BUS/MOS MEMORY DRIVERS WITH 3-STATE INVERTING

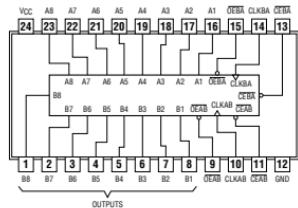


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# Pin Assignments

## 2952

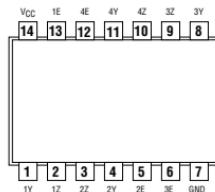
OCTAL BUS TRANSCEIVERS AND REGISTERS WITH 3-STATE OUTPUTS



See page 576

## 4016

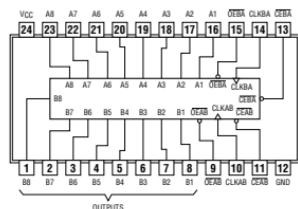
QUAD BILATERAL SWITCH



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## 2953

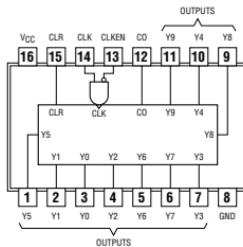
OCTAL BUS TRANSCEIVER AND REGISTER WITH 3-STATE OUTPUTS



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## 4017

DECADE COUNTERS/DIVIDER

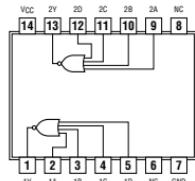


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## 4002

DUAL 4-INPUT POSITIVE-NOR GATES

positive logic:  
 $Y = \overline{A} + \overline{B} + \overline{C} + \overline{D}$

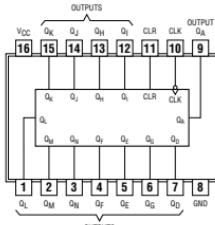


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NC-No internal connection

## 4020

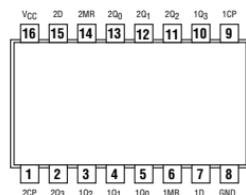
14-STAGE BINARY COUNTERS



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## 4015

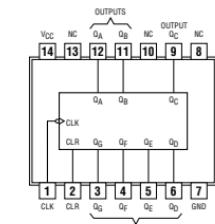
DUAL 4-STAGE STATIC SHIFT REGISTER



See page 580

## 4024

7-STAGE BINARY COUNTERS



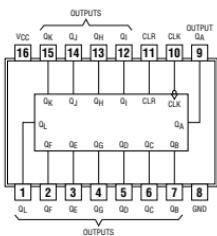
See page 584

NC-No internal connection

# Pin Assignments

## 4040

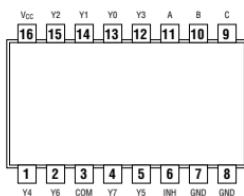
12-STAGE BINARY COUNTERS



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## 4051

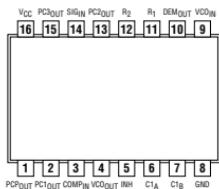
8-CHANNEL ANALOG MULTIPLEXERS/DEMULITPLEXERS



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## 4046

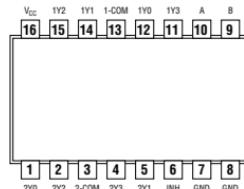
PHASE-LOCKED-LOOP WITH VCO



See page 586

## 4052

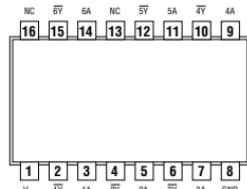
DUAL 4-CHANNEL ANALOG MULTIPLEXERS/DEMULITPLEXERS



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## 4049

HEX INVERTING BUFFERS

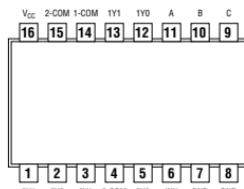


See page 588

NC-No internal connection

## 4053

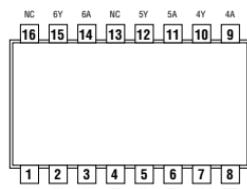
TRIPLE 2-CHANNEL ANALOG MULTIPLEXERS/DEMULITPLEXERS



See page 591

## 4050

HEX NON-INVERTING BUFFERS

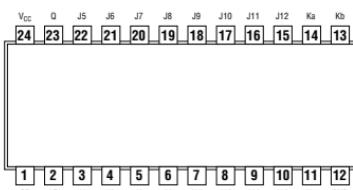


See page 588

NC-No internal connection

## 4059

CMOS PROGRAMMABLE DIVIDE-BY-N COUNTER

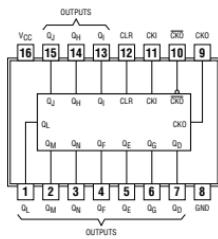


See page 592

# Pin Assignments

## 4060

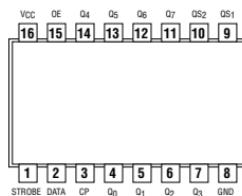
ASYNCHRONOUS 14-STAGE BINARY COUNTERS  
AND OSCILLATORS



See page 593

## 4094

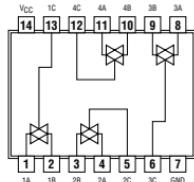
8-STAGE SHIFT AND STORE BUS REGISTER,  
THREE-STATE



See page 597

## 4066

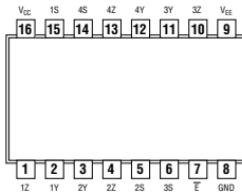
QUADRUPLE BILATERAL SWITCHES



See page 594

## 4316

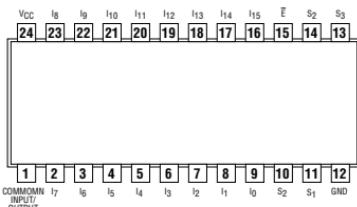
QUAD ANALOG SWITCH WITH LEVEL TRANSLATION



See page 598

## 4067

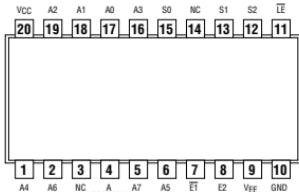
16-CHANNEL ANALOG MULTIPLEXER/DEMULTIPLEXER



See page 595

## 4351

ANALOG MULTIPLEXERS/DEMULTIPLEXERS  
WITH LATCH



See page 599

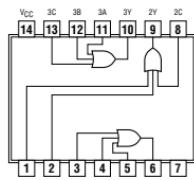
NC-No internal connection

## 4075

TRIPLE 3-INPUT OR GATES

positive logic:

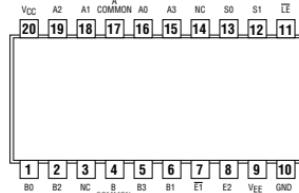
$$Y = A + B + C$$



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## 4352

ANALOG MULTIPLEXERS/DEMULTIPLEXERS  
WITH LATCH



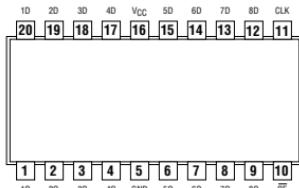
See page 600

NC-No internal connection

# Pin Assignments

## 4374

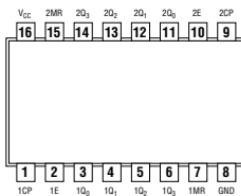
OCTAL EDGE-TRIGGERED D-TYPE DUAL-RANK  
FLIP-FLOP WITH 3-STATE OUTPUTS



See page 601

## 4518

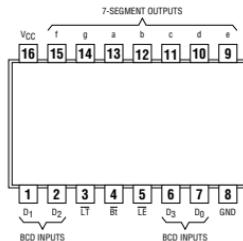
DUAL SYNCHRONOUS COUNTERS



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## 4511

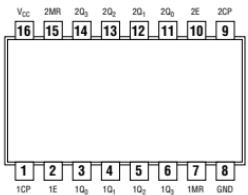
BCD-TO-7 SEGMENT LATCH/DECODER/DRIVERS



See page 602

## 4520

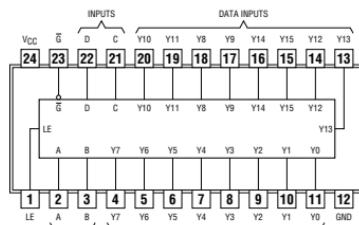
DUAL SYNCHRONOUS COUNTERS



See page 607

## 4514

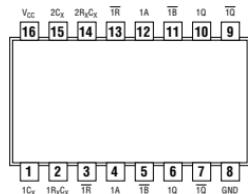
4-LINE TO 16-LINE DECODERS/DEMUTIPLEXERS WITH INPUT LATCHES



See page 604

## 4538

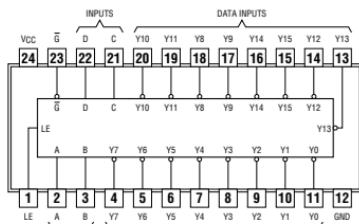
DUAL RETRIGGERRABLE PRECISION MONO STABLE MULTIVIBRATOR



See page 608

## 4515

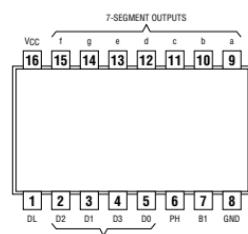
4-LINE TO 16-LINE DECODERS/DEMUTIPLEXERS WITH INPUT LATCHES



See page 605

## 4543

BCD-TO-7 SEGMENT LATCH/DECODER/DRIVERS

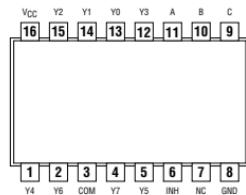


See page 610

# Pin Assignments

## 4851

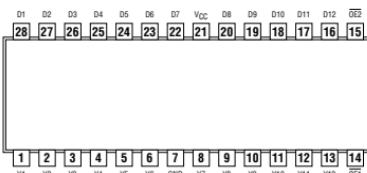
8-CHANNEL ANALOG MULTIPLEXER/DEMULTIPLEXER WITH INJECTION-CURRENT EFFECT CONTROL



See page 612

## 5402

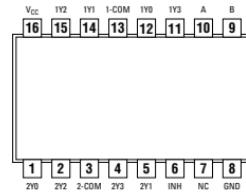
12-BIT LINE/MEMORY DRIVERS WITH 3-STATE OUTPUTS



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## 4852

DUAL 4-TO-1 CHANNEL ANALOG MULTIPLEXER/DEMULTIPLEXER WITH INJECTION-CURRENT EFFECT CONTROL

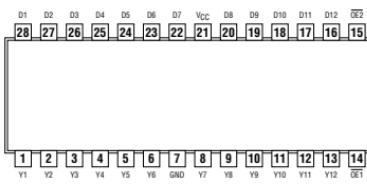


See page 612

NC-No internal connection

## 5403

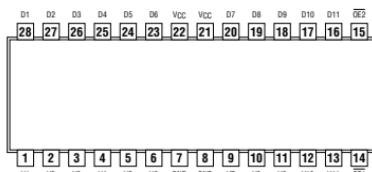
12-BIT LINE/MEMORY DRIVERS WITH 3-STATE OUTPUTS



See page 615

## 5400

11-BIT LINE/MEMORY DRIVERS WITH 3-STATE OUTPUTS

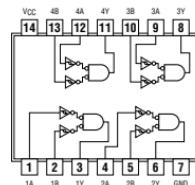


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## 7001

QUADRUPLE POSITIVE-AND GATES WITH SCHMITT-TRIGGER INPUTS

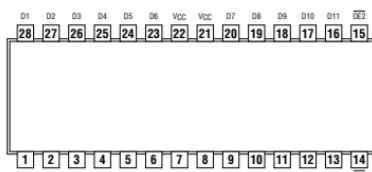
positive logic:  
 $Y = A \cdot B$



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## 5401

11-BIT LINE/MEMORY DRIVERS WITH 3-STATE OUTPUTS

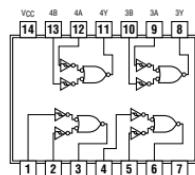


See page 614

## 7002

QUADRUPLE POSITIVE-NOR GATES WITH SCHMITT-TRIGGER INPUTS

positive logic:  
 $Y = \overline{A + B}$



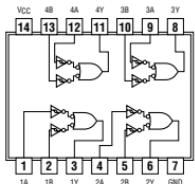
See page 616

## Pin Assignments

### **7032**

QUADRUPLE POSITIVE-OR GATES  
WITH SCHMITT-TRIGGER INPUTS

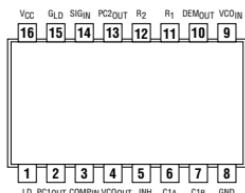
positive logic:  
 $Y = A + B$



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### **7046**

PHASE-LOCKED LOOP WITH VCO AND LOCK DETECTOR

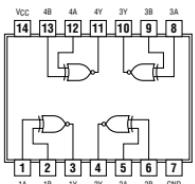


See page 618

### **7266**

QUAD 2-INPUT EXCLUSIVE-NOR GATES

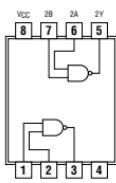
positive logic:  
 $Y = \overline{A} - \overline{B}$



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### **8003**

DUAL 2-INPUT POSITIVE-NAND GATES

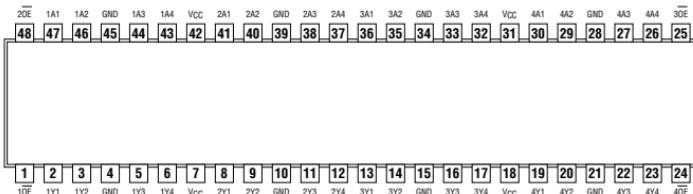


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## Pin Assignments

### 16240

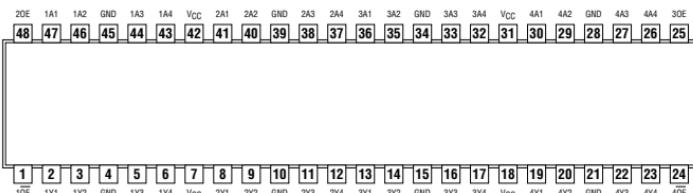
16-BIT BUS BUFFERS/DRIVERS  
WITH 3-STATE OUTPUTS



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### 16241

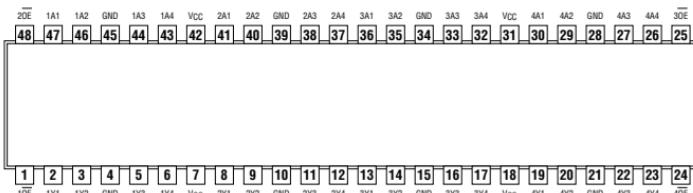
16-BIT BUS BUFFERS/DRIVERS  
WITH 3-STATE OUTPUTS



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### 16244

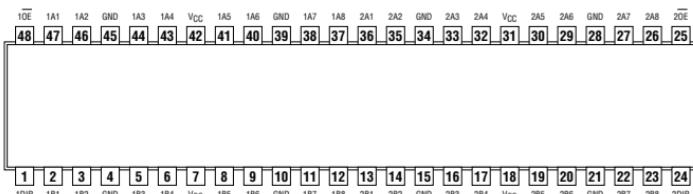
16-BIT BUS BUFFERS/DRIVERS  
WITH 3-STATE OUTPUTS



See page 624

### 16245

16-BIT BUS TRANSCEIVER  
WITH 3-STATE OUTPUTS



See page 626

## Pin Assignments

### 16260

12-BIT TO 24-BIT MULTIPLEXES D-TYPE LATCH  
WITH 3-STATE OUTPUTS

DEB	LEA2	284	GND	285	286	V <sub>CC</sub>	287	288	289	GND	2810	2811	2812	1811	1810	GND	189	188	187	V <sub>CC</sub>	186	185	GND	184	LEA18	DE18	
56	55	54	53	52	51	50	49	48	47	46	45	44	43	42	41	40	39	38	37	36	35	34	33	32	31	30	29

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### 16269

12-BIT TO 24-BIT REGISTERED BUS TRANSCEIVER  
WITH 3-STATE OUTPUTS

DEB	CLKENA2	284	GND	285	286	V <sub>CC</sub>	287	288	289	GND	2810	2811	2812	1811	1810	GND	189	188	187	V <sub>CC</sub>	186	185	GND	184	CLKENAT	CLK	
56	55	54	53	52	51	50	49	48	47	46	45	44	43	42	41	40	39	38	37	36	35	34	33	32	31	30	29

See page 630

NC-No internal connection

### 16270

12-BIT TO 24-BIT REGISTERED BUS EXCHANGER  
WITH 3-STATE OUTPUTS

DEB	CLKENA2	284	GND	285	286	V <sub>CC</sub>	287	288	289	GND	2810	2811	2812	1811	1810	GND	189	188	187	V <sub>CC</sub>	186	185	GND	184	CLKENAT	CLK	
56	55	54	53	52	51	50	49	48	47	46	45	44	43	42	41	40	39	38	37	36	35	34	33	32	31	30	29

See page 632

### 16271

12-BIT TO 24-BIT MULTIPLEXED BUS EXCHANGER  
WITH 3-STATE OUTPUTS

DEB	CLKENA2	284	GND	285	286	V <sub>CC</sub>	287	288	289	GND	2810	2811	2812	1811	1810	GND	189	188	187	V <sub>CC</sub>	186	185	GND	184	CLKENAT	CLK	
56	55	54	53	52	51	50	49	48	47	46	45	44	43	42	41	40	39	38	37	36	35	34	33	32	31	30	29

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## Pin Assignments

16282

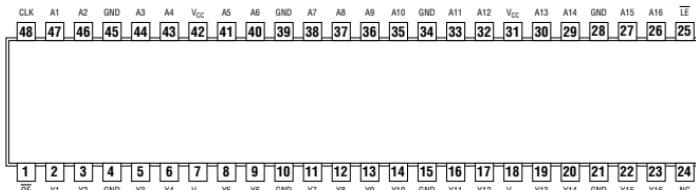
## **18-BIT TO 36-BIT REGISTERED BUS EXCHANGER WITH 3-STATE OUTPUTS**



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16334

**16-BIT UNIVERSAL BUS DRIVER  
WITH 3-STATE OUTPUTS**

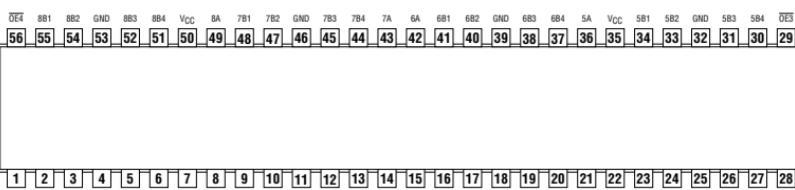


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NC-No internal connection

16344

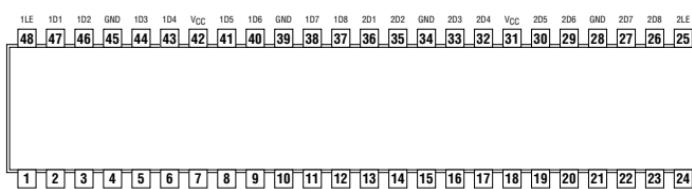
## **10544** 1-BIT TO 4-BIT ADDRESS DRIVER WITH 3-STATE OUTPUTS



See page 640

16373

### **10373** 16-BIT TRANSPARENT LATCHES WITH 3-STATE OUTPUTS



Gas para 640

## Pin Assignments

### 16374

16-BIT EDGE-TRIGGERED D-TYPE FLIP-FLOPS  
WITH 3-STATE OUTPUTS

1CLK	1D1	1D2	GND	1D3	1D4	V <sub>CC</sub>	1D5	1D6	GND	1D7	1D8	2D1	2D2	GND	2D3	2D4	V <sub>CC</sub>	2D5	2D6	GND	2D7	2D8	2CLK
48	47	46	45	44	43	42	41	40	39	38	37	36	35	34	33	32	31	30	29	28	27	26	25

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### 16409

9-BIT, 4-PORT UNIVERSAL BUS EXCHANGER  
WITH 3-STATE OUTPUTS

CLK	SELEN	1B1	GND	1B2	1B3	V <sub>CC</sub>	1B4	1B5	GND	1B7	1B8	1B9	2B1	2B2	2B3	GND	2B4	2B5	2B6	V <sub>CC</sub>	2B7	2B8	GND	2B9	SEL4	SEL3	
56	55	54	53	52	51	50	49	48	47	46	45	44	43	42	41	40	39	38	37	36	35	34	33	32	31	30	29

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### 16460

4-TO-1 MULTIPLEXED/DEMULTIPLEXED TRANSCEIVERS  
WITH 3-STATE OUTPUTS

OE <sub>B1</sub>	OE <sub>B2</sub>	SEL0	GND	1B1	1B2	V <sub>CC</sub>	1B3	1B4	GND	2B2	2B3	2B4	3B1	3B2	3B3	GND	3B4	4B1	4B2	V <sub>CC</sub>	4B3	4B4	GND	SEL1	OE <sub>B3</sub>	OE <sub>B4</sub>	
56	55	54	53	52	51	50	49	48	47	46	45	44	43	42	41	40	39	38	37	36	35	34	33	32	31	30	29

1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26 27 28  
LEA<sub>B1</sub> LEA<sub>B2</sub> LEBA GND LEB1 LEB2 V<sub>CC</sub> CLK<sub>B1</sub> CLK<sub>B2</sub> SEL0 GND 1A 2A CE SEL0 CE SEL1 3A 4A GND CLK<sub>E1B</sub> CLK<sub>E2B</sub> CLK<sub>E3B</sub> CLK<sub>E4B</sub> V<sub>CC</sub> LEB3 LEB4 GND OE<sub>A</sub> LEA<sub>B3</sub> LEA<sub>B4</sub>

See page 648

### 16470

16-BIT REGISTERED TRANSCEIVERS  
WITH 3-STATE OUTPUTS

OE <sub>A</sub>	1CLK <sub>A</sub>	1CLK <sub>B</sub>	GND	1B1	1B2	V <sub>CC</sub>	1B3	1B4	1B5	GND	1B6	1B7	1B8	2B1	2B2	2B3	GND	2B4	2B5	2B6	V <sub>CC</sub>	2B7	2B8	GND	2CLK <sub>A</sub>	2CLK <sub>B</sub>	
56	55	54	53	52	51	50	49	48	47	46	45	44	43	42	41	40	39	38	37	36	35	34	33	32	31	30	29

1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26 27 28  
1OE<sub>A</sub> 1CLK<sub>A</sub> 1CLK<sub>B</sub> GND 1A1 1A2 V<sub>CC</sub> 1A3 1A4 1A5 GND 1A6 1A7 1A8 2A1 2A2 2A3 GND 2A4 2A5 2A6 V<sub>CC</sub> 2A7 2A8 GND 2CLK<sub>A</sub> 2CLK<sub>B</sub> 2OE<sub>A</sub>

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# Pin Assignments

## 16500

18-BIT UNIVERSAL BUS TRANSCEIVER  
WITH 3-STATE OUTPUTS

GND	CLKAB	B1	GND	B2	B3	VCC	B4	B5	B6	GND	B7	B8	B9	B10	B11	B12	GND	B13	B14	B15	VCC	B16	B17	GND	B18	CLKBA	GND
56	55	54	53	52	51	50	49	48	47	46	45	44	43	42	41	40	39	38	37	36	35	34	33	32	31	30	29

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## 16501

18-BIT UNIVERSAL BUS TRANSCEIVER  
WITH 3-STATE OUTPUTS

GND	CLKAB	B1	GND	B2	B3	VCC	B4	B5	B6	GND	B7	B8	B9	B10	B11	B12	GND	B13	B14	B15	VCC	B16	B17	GND	B18	CLKBA	GND
56	55	54	53	52	51	50	49	48	47	46	45	44	43	42	41	40	39	38	37	36	35	34	33	32	31	30	29

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## 16524

18-BIT REGISTERED BUS TRANSCEIVER  
WITH 3-STATE OUTPUTS

GND	SEL	B1	GND	B2	B3	VCC	B4	B5	B6	GND	B7	B8	B9	B10	B11	B12	GND	B13	B14	B15	VCC	B16	B17	GND	B18	CLK	GND
56	55	54	53	52	51	50	49	48	47	46	45	44	43	42	41	40	39	38	37	36	35	34	33	32	31	30	29

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## 16525

18-BIT REGISTERED BUS TRANSCEIVER  
WITH 3-STATE OUTPUTS

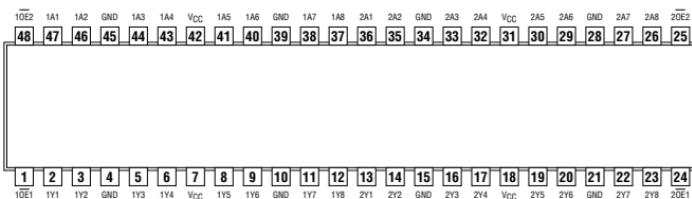
SEL	CLKAB	B1	GND	B2	B3	VCC	B4	B5	B6	GND	B7	B8	B9	B10	B11	B12	GND	B13	B14	B15	VCC	B16	B17	GND	B18	CLKBA	CLKCBA
56	55	54	53	52	51	50	49	48	47	46	45	44	43	42	41	40	39	38	37	36	35	34	33	32	31	30	29

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## Pin Assignments

### 16540

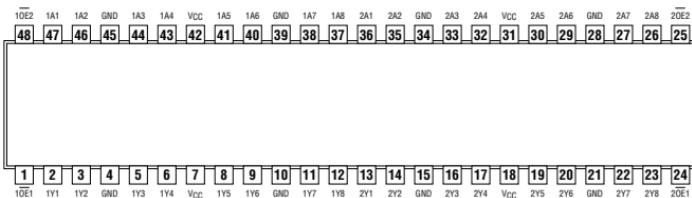
16-BIT BUFFERS/DRIVERS  
WITH 3-STATE OUTPUTS



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### 16541

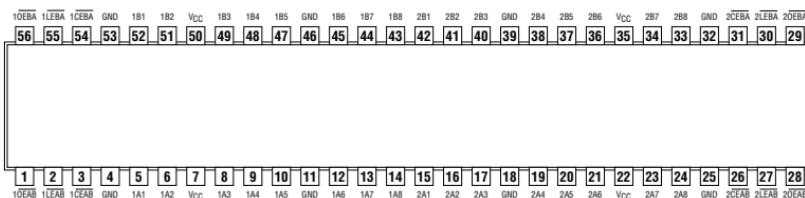
16-BIT BUFFERS/DRIVERS  
WITH 3-STATE OUTPUTS



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### 16543

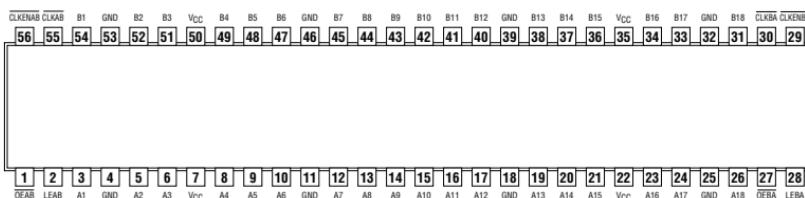
16-BIT REGISTERED TRANSCEIVERS  
WITH 3-STATE OUTPUTS



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### 16600

18-BIT UNIVERSAL BUS TRANSCEIVERS  
WITH 3-STATE OUTPUTS



See page 664

## Pin Assignments

### **16601**

**18-BIT UNIVERSAL BUS TRANSCEIVERS  
WITH 3-STATE OUTPUTS**

CLKENB	CLKAB	B1	GND	B2	B3	V <sub>CC</sub>	B4	B5	B6	GND	B7	B8	B9	B10	B11	B12	GND	B13	B14	B15	V <sub>CC</sub>	B16	B17	GND	B18	CLKB	CLKENBA
56	55	54	53	52	51	50	49	48	47	46	45	44	43	42	41	40	39	38	37	36	35	34	33	32	31	30	29

1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28
DEAB	LEAB	A1	GND	A2	A3	V <sub>CC</sub>	A4	A5	A6	GND	A7	A8	A9	A10	A11	A12	GND	A13	A14	A15	V <sub>CC</sub>	A16	A17	GND	A18	DEBA	LEBA

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### **16620**

**16-BIT BUS TRANSCEIVERS  
WITH 3-STATE OUTPUTS**

1OEBA	1A1	1A2	GND	1A3	1A4	V <sub>CC</sub>	1A5	1A6	GND	1A7	1AB	2A1	2A2	GND	2A3	2A4	V <sub>CC</sub>	2A5	2A6	GND	2A7	2A8	2OEBA
48	47	46	45	44	43	42	41	40	39	38	37	36	35	34	33	32	31	30	29	28	27	26	25

1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24
1OEAB	1B1	1B2	GND	1B3	1B4	V <sub>CC</sub>	1B5	1B6	GND	1B7	1B8	2B1	2B2	GND	2B3	2B4	V <sub>CC</sub>	2B5	2B6	GND	2B7	2B8	2OEAB

See page 668

### **16623**

**16-BIT BUS TRANSCEIVERS  
WITH 3-STATE OUTPUTS**

1OEBA	1A1	1A2	GND	1A3	1A4	V <sub>CC</sub>	1A5	1A6	GND	1A7	1AB	2A1	2A2	GND	2A3	2A4	V <sub>CC</sub>	2A5	2A6	GND	2A7	2A8	2OEBA
48	47	46	45	44	43	42	41	40	39	38	37	36	35	34	33	32	31	30	29	28	27	26	25

1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24
1OEAB	1B1	1B2	GND	1B3	1B4	V <sub>CC</sub>	1B5	1B6	GND	1B7	1B8	2B1	2B2	GND	2B3	2B4	V <sub>CC</sub>	2B5	2B6	GND	2B7	2B8	2OEAB

See page 670

### **16640**

**16-BIT BUS TRANSCEIVER  
WITH 3-STATE OUTPUTS**

1OE	1A1	1A2	GND	1A3	1A4	V <sub>CC</sub>	1A5	1A6	GND	1A7	1AB	2A1	2A2	GND	2A3	2A4	V <sub>CC</sub>	2A5	2A6	GND	2A7	2A8	2OE
48	47	46	45	44	43	42	41	40	39	38	37	36	35	34	33	32	31	30	29	28	27	26	25

1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24
1OIR	1B1	1B2	GND	1B3	1B4	V <sub>CC</sub>	1B5	1B6	GND	1B7	1B8	2B1	2B2	GND	2B3	2B4	V <sub>CC</sub>	2B5	2B6	GND	2B7	2B8	2OIR

See page 671

# Pin Assignments

## 16646

**16-BIT BUS TRANSCEIVERS AND REGISTERS  
WITH 3-STATE OUTPUTS**

1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28
10E	1CLKBA	1SAB	GND	1B1	1B2	VCC	1B3	1B4	1B5	GND	1B6	1B7	1B8	2B1	2B2	2B3	GND	2B4	2B5	2B6	VCC	2B7	2B8	GND	2SBA	2CLKBA	2OE

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## 16651

**16-BIT BUS TRANSCEIVERS AND REGISTERS  
WITH 3-STATE OUTPUTS**

1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28
10E	1CLKAB	1SAB	GND	1A1	1A2	VCC	1A3	1A4	1A5	GND	1A6	1A7	1A8	2A1	2A2	2A3	GND	2A4	2A5	2A6	VCC	2A7	2A8	GND	2SAB	2CLKAB	2OEAB

See page 674

## 16652

**16-BIT BUS TRANSCEIVERS AND REGISTERS  
WITH 3-STATE OUTPUTS**

1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28
10E	1CLKAB	1SAB	GND	1A1	1A2	VCC	1A3	1A4	1A5	GND	1A6	1A7	1A8	2A1	2A2	2A3	GND	2A4	2A5	2A6	VCC	2A7	2A8	GND	2SAB	2CLKAB	2OEAB

See page 676

## 16657

**16-BIT TRANSCEIVERS  
WITH PARITY GENERATORS/CHECKERS AND 3-STATE OUTPUTS**

1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28
10E	NC	1ERR	GND	1A1	1A2	VCC	1A3	1A4	1A5	GND	1A6	1A7	1A8	2A1	2A2	2A3	GND	2A4	2A5	2A6	VCC	2A7	2A8	GND	2ERR	NC	2OE

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NC-No internal connection

# Pin Assignments

## 16721

20-BIT FLIP-FLOP  
WITH 3-STATE OUTPUTS

CLK	D1	D2	GND	D3	D4	V <sub>CC</sub>	D5	D6	D7	GND	D8	D9	D10	D11	D12	D13	GND	D14	D15	D16	V <sub>CC</sub>	D17	D18	GND	D19	D20	CLKEN
56	55	54	53	52	51	50	49	48	47	46	45	44	43	42	41	40	39	38	37	36	35	34	33	32	31	30	29

See page 680

NC-No internal connection

## 16722

22-BIT FLIP-FLOP WITH 3-STATE OUTPUTS

CLK	D1	D2	GND	D3	D4	V <sub>CC</sub>	D5	D6	D7	GND	D8	D9	D10	D11	D12	D13	GND	D14	D15	D16	V <sub>CC</sub>	D17	D18	GND	D19	D20	V <sub>CC</sub>	D21	D22	GND	D23	CLKEN
64	63	62	61	60	59	58	57	56	55	54	53	52	51	50	49	48	47	46	45	44	43	42	41	40	39	38	37	36	35	34	33	

See page 681

NC-No internal connection

## 16820

10-BIT EDGE-TRIGGERED D-TYPE FLIP-FLOPS  
WITH DUAL OUTPUTS

CLK	D1	NC	GND	D2	NC	V <sub>CC</sub>	D3	NC	D4	GND	NC	D5	NC	D6	NC	D7	GND	NC	D8	NC	V <sub>CC</sub>	D9	NC	GND	D10	NC	NC
56	55	54	53	52	51	50	49	48	47	46	45	44	43	42	41	40	39	38	37	36	35	34	33	32	31	30	29

See page 682

NC-No internal connection

## 16821

20-BIT BUS INTERFACE FLIP-FLOPS  
WITH 3-STATE OUTPUTS

1CLK	1D1	1D2	GND	1D3	1D4	V <sub>CC</sub>	1D5	1D6	1D7	GND	1D8	1D9	1D10	1D11	1D12	1D13	GND	1D14	1D15	1D16	V <sub>CC</sub>	1D17	1D18	GND	1D19	1D20	1D21	1D22	1D23	1D24	1D25	1D26	1D27	1D28	2CLK
56	55	54	53	52	51	50	49	48	47	46	45	44	43	42	41	40	39	38	37	36	35	34	33	32	31	30	29								

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# Pin Assignments

## 16823

18-BIT EDGE-TRIGGERED D-TYPE FLIP-FLOPS  
WITH DUAL OUTPUTS

1	CLX	1CLKEN	1D1	GND	1D2	1D3	V <sub>CC</sub>	1D4	1D5	GND	1D6	1D7	1D8	1D9	2D1	2D2	2D3	GND	2D4	2D5	2D6	2D7	2D8	GND	2D9	2D10	2CLKEN	2CLK
56	55	54	53	52	51	50	49	48	47	46	45	44	43	42	41	40	39	38	37	36	35	34	33	32	31	30	29	

See page 684

## 16825

18-BIT BUS BUFFERS/DRIVERS  
WITH 3-STATE OUTPUTS

1	̄OE2	1A1	1A2	GND	1A3	1A4	V <sub>CC</sub>	1A5	1A6	1A7	GND	1A8	1A9	GND	2A1	2A2	GND	2A3	2A4	2A5	V <sub>CC</sub>	2A6	2A7	GNA	2A8	2A9	2OE3
56	55	54	53	52	51	50	49	48	47	46	45	44	43	42	41	40	39	38	37	36	35	34	33	32	31	30	29

See page 685

## 16827

20-BIT BUS BUFFERS/DRIVERS  
WITH 3-STATE OUTPUTS

1	̄OE3	1A1	1A2	GND	1A3	1A4	V <sub>CC</sub>	1A5	1A6	1A7	GND	1A8	1A9	1A10	2A1	2A2	2A3	GND	2A4	2A5	2A6	V <sub>CC</sub>	2A7	2A8	GNA	2A9	2A10	2OE2
56	55	54	53	52	51	50	49	48	47	46	45	44	43	42	41	40	39	38	37	36	35	34	33	32	31	30	29	

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## 16831

1-TO-4 ADDRESS REGISTER/DRIVER  
WITH 3-STATE OUTPUTS

1Y2	2Y2	GND	4Y2	4Y2	5Y2	7Y2	1Y3	2Y3	2GND	3Y3	4Y3	GND	1Y4	2Y4	2Y4	2Y5	2Y5	2Y6	2Y6	2Y7	2Y7	2Y8	2Y8	2Y9	2Y10	2OE1													
69	70	78	77	76	75	74	73	72	71	70	69	68	67	66	65	64	63	62	61	60	59	58	57	56	55	54	53	52	51	50	49	48	47	46	45	44	43	42	41

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NC-No internal connection

# Pin Assignments

## 16832

1-TO-4 ADDRESS REGISTER/DRIVER  
WITH 3-STATE OUTPUTS

1Y2	2Y2	GND	3Y2	4Y2	V <sub>CC</sub>	1Y3	2Y3	GND	3Y3	4Y3	GND	V <sub>CC</sub>	GND	1Y4	2Y4	3Y4	4Y4	GND	1Y5	2Y5	3Y5	4Y5	GND	1Y6	2Y6	3Y6	4Y6				
64	63	62	61	60	59	58	57	56	55	54	53	52	51	50	49	48	47	46	45	44	43	42	41	40	39	38	37	36	35	34	33

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NC-No internal connection

## 16833

DUAL 8-BIT TO 9-BIT PARITY BUS TRANSCEIVERS

1OE <sub>A</sub>	1CLR <sub>A</sub>	1PAR <sub>A</sub>	GND	1B1	1B2	V <sub>CC</sub>	1B3	1B4	1B5	GND	1B6	1B7	1B8	2B1	2B2	2B3	2B4	2B5	2B6	V <sub>CC</sub>	2B7	2B8	GND	2PAR <sub>B</sub>	2CLR <sub>B</sub>	2OE <sub>A</sub>	
56	55	54	53	52	51	50	49	48	47	46	45	44	43	42	41	40	39	38	37	36	35	34	33	32	31	30	29

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## 16834

16-BIT UNIVERSAL BUS DRIVER  
WITH 3-STATE OUTPUTS

GND	NC	A1	GND	A2	A3	V <sub>CC</sub>	A4	A5	A6	GND	A7	A8	A9	A10	A11	A12	GND	A13	A14	A15	V <sub>CC</sub>	A16	A17	GND	A18	CLK	GND
56	55	54	53	52	51	50	49	48	47	46	45	44	43	42	41	40	39	38	37	36	35	34	33	32	31	30	29

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NC-No internal connection

## 16835

33-V ABT 18-BIT UNIVERSAL BUS DRIVER  
WITH 3-STATE OUTPUTS

GND	NC	A1	GND	A2	A3	V <sub>CC</sub>	A4	A5	A6	GND	A7	A8	A9	A10	A11	A12	GND	A13	A14	A15	V <sub>CC</sub>	A16	A17	GND	A18	CLK	GND
56	55	54	53	52	51	50	49	48	47	46	45	44	43	42	41	40	39	38	37	36	35	34	33	32	31	30	29

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NC-No internal connection

## Pin Assignments

### 16841

20-BIT BUS INTERFACE D-TYPE LATCHES  
WITH 3-STATE OUTPUTS

1LE	1D1	1D2	GND	1D3	1D4	V <sub>CC</sub>	1D5	1D6	1D7	GND	1D8	1D9	1D10	2D1	2D2	GND	2D4	2D5	2D6	V <sub>CC</sub>	2D7	2D8	GND	2D9	2D10	2LE	
56	55	54	53	52	51	50	49	48	47	46	45	44	43	42	41	40	39	38	37	36	35	34	33	32	31	30	29

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### 16843

18-BIT BUS INTERFACE D-TYPE LATCHES WITH 3-STATE OUTPUTS

1OE	1PRE	1D1	GND	1D2	1D3	V <sub>CC</sub>	1D4	1D5	1D6	GND	1D7	1D8	1D9	2D1	2D2	2D3	GND	2D4	2D5	2D6	V <sub>CC</sub>	2D7	2D8	GND	2D9	2D10	2LE
56	55	54	53	52	51	50	49	48	47	46	45	44	43	42	41	40	39	38	37	36	35	34	33	32	31	30	29

See page 695

### 16853

DUAL 8-BIT TO 9-BIT PARITY BUS TRANSCEIVERS

1DEA	1CLR	1PARITY	GND	1B1	1B2	V <sub>CC</sub>	1B3	1B4	1B5	GND	1B6	1B7	1B8	2B1	2B2	2B3	GND	2B4	2B5	2B6	V <sub>CC</sub>	2B7	2B8	GND	2PARITY	2CLR	2DEA
56	55	54	53	52	51	50	49	48	47	46	45	44	43	42	41	40	39	38	37	36	35	34	33	32	31	30	29

See page 696

### 16861

20-BIT BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

1OEAB	1A1	1A2	GND	1A3	1A4	V <sub>CC</sub>	1A5	1A6	1A7	GND	1A8	1A9	1A10	2A1	2A2	2A3	GND	2A4	2A5	2A6	V <sub>CC</sub>	2A7	2A8	GNA	2A9	2A10	2OEAB
56	55	54	53	52	51	50	49	48	47	46	45	44	43	42	41	40	39	38	37	36	35	34	33	32	31	30	29

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# Pin Assignments

## 16863

18-BIT BUS TRANSCEIVERS  
WITH 3-STATE OUTPUTS

1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28
10E8A	1A1	1A2	GND	1A3	1A4	VCC	1A5	1A6	1A7	GND	1A8	1A9	GND	1A10	2A1	2A2	GND	2A3	2A4	2A5	2A6	2A7	GNA	2A8	2A9	20E8A	
56	55	54	53	52	51	50	49	48	47	46	45	44	43	42	41	40	39	38	37	36	35	34	33	32	31	30	29

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## 16901

18-BIT UNIVERSAL BUS TRANSCEIVER  
WITH PARITY GENERATORS/CHECKERS

1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32
10E8B	LE8A	CLK8A	16901	18PAR	GND	1B1	1B2	1B3	VCC	1B4	1B5	1B6	GND	1B7	1B8	2B1	2B2	GND	2B3	2B4	2B5	VCC	2B6	2B7	2B8	GND	2B9PAR	2E9B	DE8A	10E8B	
64	63	62	61	60	59	58	57	56	55	54	53	52	51	50	49	48	47	46	45	44	43	42	41	40	39	38	37	36	35	34	33

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## 16903

3.3-V 12-BIT UNIVERSAL BUS DRIVER  
WITH PARITY CHECKER AND DUAL 3-STATE OUTPUTS

1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28
DE	Y1Y	Y2Y	GND	2Y1	2Y2	V <sub>CC</sub>	3Y1	3Y2	4Y1	GND	4Y2	5Y1	5Y2	6Y1	6Y2	7Y1	7Y2	8Y1	8Y2	V <sub>CC</sub>	9Y1	9Y2	GND	10Y1	10Y2	PAROE	
56	55	54	53	52	51	50	49	48	47	46	45	44	43	42	41	40	39	38	37	36	35	34	33	32	31	30	29

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## 16952

16-BIT REGISTERED TRANSCEIVERS  
WITH 3-STATE OUTPUTS

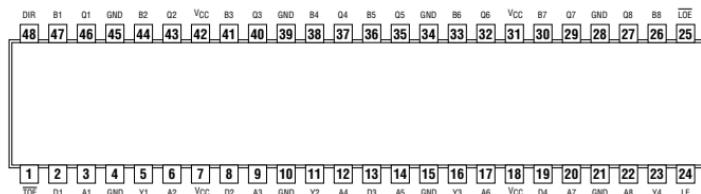
1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28
10E8B	1CLKA8B	1CLKB8A	GND	1A1	1A2	VCC	1B3	1B4	1B5	GND	1B6	1B7	1B8	2B1	2B2	2B3	2B4	2B5	2B6	VCC	2B7	2B8	GND	2CLKB8A	20E8A		
56	55	54	53	52	51	50	49	48	47	46	45	44	43	42	41	40	39	38	37	36	35	34	33	32	31	30	29

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# Pin Assignments

## 16973

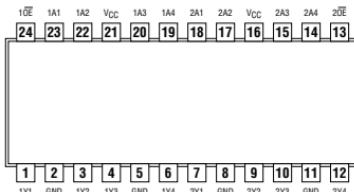
8-BIT BUS TRANSCEIVER AND TRANSPARENT D-TYPE LATCH  
WITH FOUR INDEPENDENT BUFFERS



See page 706

## 25244

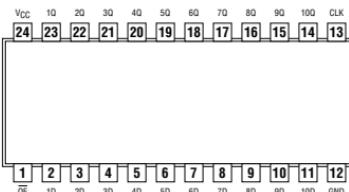
25- $\Omega$  OCTAL BUFFER/DRIVER WITH 3-STATE OUTPUTS



See page 708

## 29821

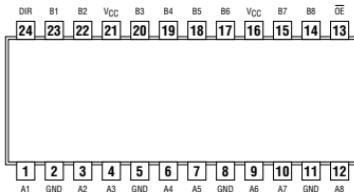
10-BIT BUS-INTERFACE FLIP-FLOPS WITH 3-STATE OUTPUTS



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## 25245

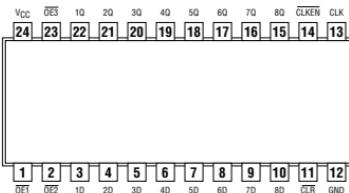
25- $\Omega$  OCTAL BUS TRANSCEIVERS WITH 3-STATE OUTPUTS



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## 29825

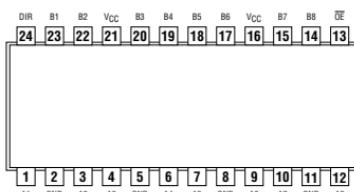
8-BIT BUS-INTERFACE FLIP-FLOPS WITH 3-STATE OUTPUTS



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## 25642

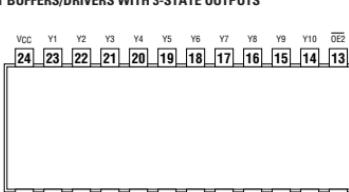
25- $\Omega$  OCTAL BUS TRANSCEIVER



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## 29827

10-BIT BUFFERS/DRIVERS WITH 3-STATE OUTPUTS

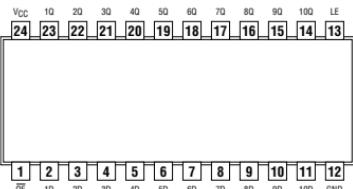


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# Pin Assignments

## **29841**

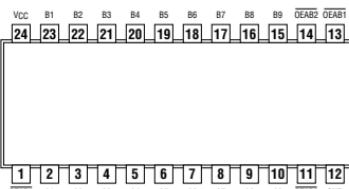
10-BIT BUS INTERFACE D-TYPE LATCHES WITH 3-STATE OUTPUTS



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## **29864**

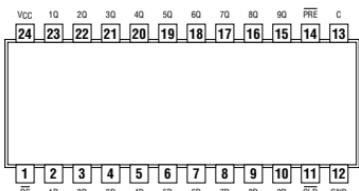
9-BIT BUS TRANSCEIVER WITH 3-STATE OUTPUTS



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## **29843**

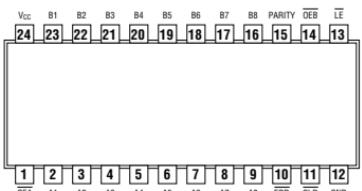
9-BIT BUS INTERFACE D-TYPE LATCHES WITH 3-STATE OUTPUTS



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## **29854**

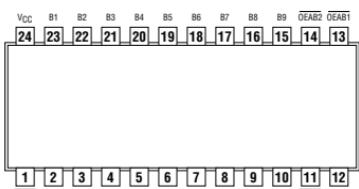
8-BIT TO 9-BIT PARITY BUS TRANSCEIVER



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## **29863**

9-BIT BUS TRANSCEIVERS WITH 3-STATE OUTPUTS



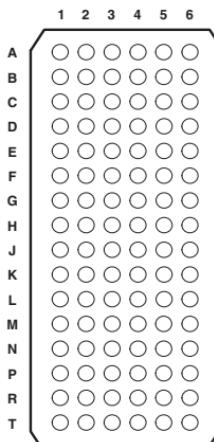
See page 720

# Pin Assignments

## 32240

32-BIT BUFFER/DRIVER

GKE PACKAGE  
(TOP VIEW)



### terminal assignments

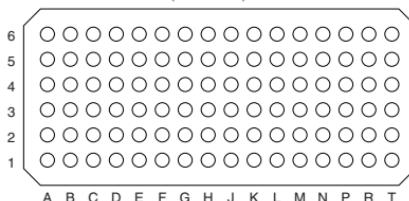
	1	2	3	4	5	6
A	1Y2	1Y1	1OE	2OE	1A1	1A2
B	1Y4	1Y3	GND	GND	1A3	1A4
C	2Y2	2Y1	1VCC	1VCC	2A1	2A2
D	2Y2	2Y3	GND	GND	2A3	2A4
E	3Y2	3Y1	GND	GND	3A1	3A2
F	3Y4	3Y3	1VCC	1VCC	3A3	3A4
G	4Y2	4Y1	GND	GND	4A1	4A2
H	4Y3	4Y4	4OE	3OE	4A4	4A3
J	5Y2	5Y1	5OE	6OE	5A1	5A2
K	5Y4	5Y3	GND	GND	5A3	5A4
L	6Y2	6Y1	2VCC	2VCC	6A1	6A2
M	6Y4	6Y3	GND	GND	6A3	6A4
N	7Y2	7Y1	GND	GND	7A1	7A2
P	7Y4	7Y3	2VCC	2VCC	7A3	7A4
R	8Y2	8Y1	GND	GND	8A1	8A2
T	8Y3	8Y4	8OE	7OE	8A4	8A3

See page 722

## 32244

32-BIT BUFFER/DRIVER  
WITH 3-STATE OUTPUTS

GKE PACKAGE  
(TOP VIEW)



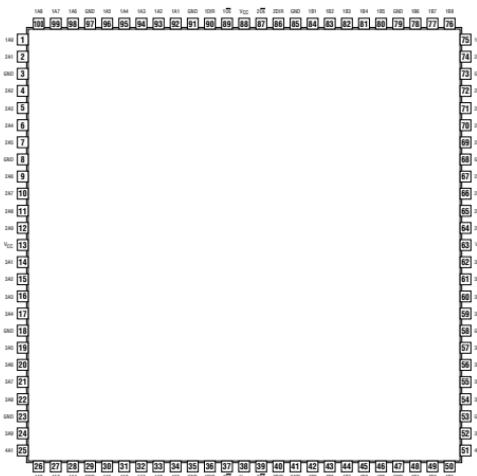
6	1A2	1A4	2A2	2A4	3A2	3A4	4A2	4A3	5A2	5A4	6A2	6A4	7A2	7A4	8A2	8A3
5	1A1	1A3	2A1	2A3	3A1	3A3	4A1	4A4	5A1	5A3	6A1	6A3	7A1	7A3	8A1	8A4
4	2OE	GND	V <sub>CC</sub>	GND	V <sub>CC</sub>	GND	V <sub>CC</sub>	3OE	6OE	GND	V <sub>CC</sub>	GND	V <sub>CC</sub>	GND	7OE	
3	1OE	GND	V <sub>CC</sub>	GND	V <sub>CC</sub>	GND	V <sub>CC</sub>	4OE	5DIR	GND	V <sub>CC</sub>	GND	V <sub>CC</sub>	GND	8DIR	
2	1Y1	1Y3	2Y1	2Y3	3Y1	3Y3	4Y1	4Y4	5Y1	5Y3	6Y1	6Y3	7Y1	7Y3	8Y1	8Y4
1	1Y2	1Y4	2Y2	2Y4	3Y2	3Y4	4Y2	4Y3	5Y2	5Y4	6Y2	6Y4	7Y2	7Y4	8Y2	8Y3
	A	B	C	D	E	F	G	H	J	K	L	M	N	P	R	T

See page 724

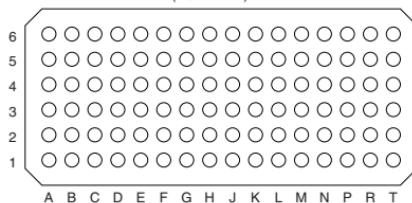
# Pin Assignments

**32245**

32-BIT BUS TRANSCEIVER  
WITH 3-STATE OUTPUTS



**GKE PACKAGE  
(TOP VIEW)**



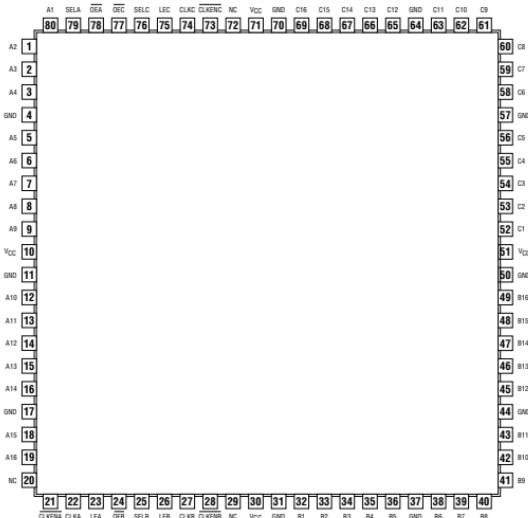
6	1A2	1A4	1A6	1A8	2A2	2A4	2A6	2A7	3A2	3A4	3A6	3A8	4A2	4A4	4A6	4A7
5	1A1	1A3	1A5	1A7	2A1	2A3	2A5	2A8	3A1	3A3	3A5	3A7	4A1	4A3	4A5	4A8
4	1OE	GND	V <sub>CC</sub>	GND	GND	V <sub>CC</sub>	GND	2OE	3OE	GND	V <sub>CC</sub>	GND	GND	V <sub>CC</sub>	GND	4OE
3	1DIR	GND	V <sub>CC</sub>	GND	GND	V <sub>CC</sub>	GND	2DIR	3DIR	GND	V <sub>CC</sub>	GND	GND	V <sub>CC</sub>	GND	4DIR
2	1B1	1B3	1B5	1B7	2B1	2B3	2B5	2B8	3B1	3B3	3B5	3B7	4B1	4B3	4B5	4B8
1	1B2	1B4	1B6	1B8	2B2	2B4	2B6	2B7	3B2	3B4	3B6	3B8	4B2	4B4	4B6	4B7
	A	B	C	D	E	F	G	H	J	K	L	M	N	P	R	T

See page 726

# Pin Assignments

## 32316

16-BIT TRI-PORT UNIVERSAL BUS EXCHANGERS

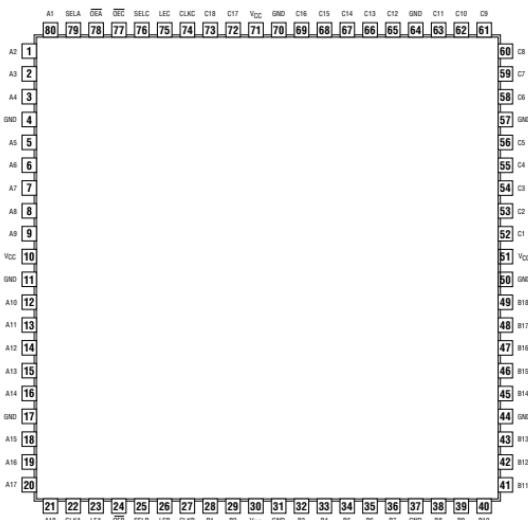


See page 728

NC-No internal connection

## 32318

18-BIT TRI-PORT UNIVERSAL BUS EXCHANGERS



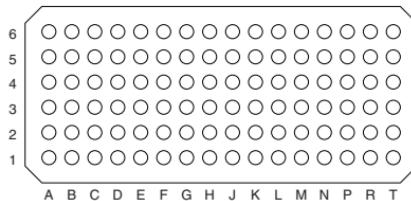
See page 730

# Pin Assignments

**32373**

32-BIT TRANSPARENT D-TYPE LATCH  
WITH 3-STATE OUTPUTS

GKE PACKAGE  
(TOP VIEW)



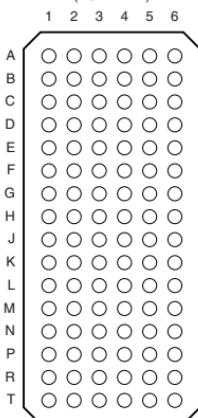
6	1D2	1D4	1D6	1D8	2D2	2D4	2D6	2D7	3D2	3D4	3D6	3D8	4D2	4D4	4D6	4D7
5	1D1	1D3	1D5	1D7	2D1	2D3	2D5	2D8	3D1	3D3	3D5	3D7	4D1	4D3	4D5	4D8
4	1LE	GND	V <sub>CC</sub>	GND	V <sub>CC</sub>	GND	2LE	3LE	GND	V <sub>CC</sub>	GND	GND	V <sub>CC</sub>	GND	4LE	
3	GND	V <sub>CC</sub>	GND	V <sub>CC</sub>	GND	V <sub>CC</sub>	2OE	3OE	GND	V <sub>CC</sub>	GND	GND	V <sub>CC</sub>	GND	4OE	
2	1OE	GND	V <sub>CC</sub>	GND	V <sub>CC</sub>	GND	3OE	3OE	GND	V <sub>CC</sub>	GND	GND	V <sub>CC</sub>	GND	4OE	
1	1Q1	1Q3	1Q5	1Q7	2Q1	2Q3	2Q5	2Q8	3Q1	3Q3	3Q5	3Q7	4Q1	4Q3	4Q5	4Q8
	1Q2	1Q4	1Q6	1Q8	2Q2	2Q4	2Q6	2Q7	3Q2	3Q4	3Q6	3Q8	4Q2	4Q4	4Q6	4Q7
	A	B	C	D	E	F	G	H	J	K	L	M	N	P	R	T

See page 732

**32374**

32-BIT EDGE-TRIGGERED D-TYPE FLIP-FLOP  
WITH 3-STATE OUTPUTS

GKE PACKAGE  
(TOP VIEW)



terminal assignments

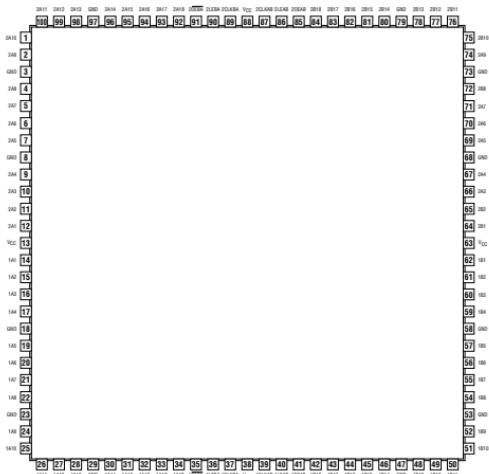
	1	2	3	4	5	6
A	1Q2	1Q1	1OE	1CLK	1D1	1D2
B	1Q4	1Q3	GND	GND	1D3	1D4
C	1Q6	1Q5	V <sub>CC</sub>	V <sub>CC</sub>	1D5	1D6
D	1Q8	1Q7	GND	GND	1D7	1D8
E	2Q2	2Q1	GND	GND	2D1	2D2
F	2Q4	2Q3	V <sub>CC</sub>	V <sub>CC</sub>	2D3	2D4
G	2Q6	2Q5	GND	GND	2D5	2D6
H	2Q8	2Q7	2OE	2CLK	2D7	2D8
J	3Q2	3Q1	3OE	3CLK	3D1	3D2
K	3Q4	3Q3	GND	GND	3D3	3D4
L	3Q6	3Q5	V <sub>CC</sub>	V <sub>CC</sub>	3D5	3D6
M	3Q8	3Q7	GND	GND	3D7	3D8
N	4Q2	4Q1	GND	GND	4D1	4D2
P	4Q4	4Q3	V <sub>CC</sub>	V <sub>CC</sub>	4D3	4D4
R	4Q6	4Q5	GND	GND	4D5	4D6
T	4Q7	4Q8	4OE	4CLK	4D8	4D7

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## Pin Assignments

32501

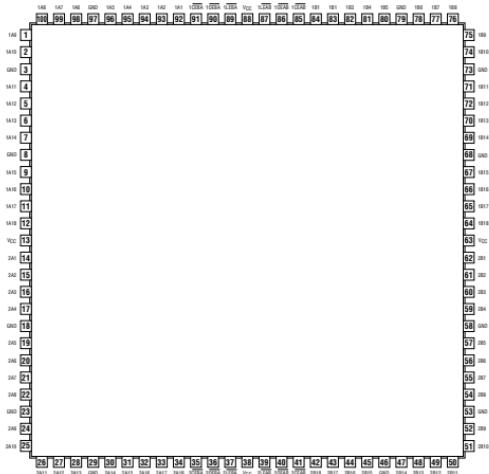
## 36-BIT UNIVERSAL BUS TRANSCEIVERS WITH 3-STATE OUTPUTS



See page 736

32543

## 36-BIT REGISTERED BUS TRANSCEIVERS WITH 3-STATE OUTPUTS



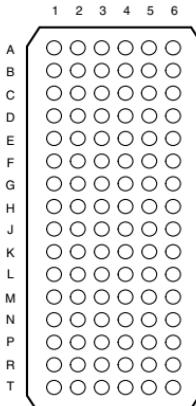
See page 738

# Pin Assignments

**32973**

16-BIT BUS TRANSCIEVER AND TRANSPARENT D-TYPE LATCH  
WITH EIGHT INDEPENDENT BUFFERS

GKE PACKAGE  
(TOP VIEW)



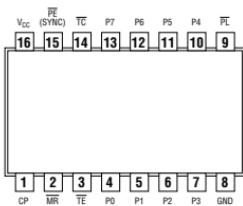
terminal assignments

	1	2	3	4	5	6
A	1A1	D1	1TOE	1DIR	1B1	1Q1
B	1A2	Y1	GND	GND	1B2	1Q2
C	1A3	D2	VCC	VCC	1B3	1Q3
D	1A4	Y2	GND	GND	1B4	1Q4
E	1A5	D3	GND	GND	1B5	1Q5
F	1A6	Y3	VCC	VCC	1B6	1Q6
G	1A7	D4	GND	GND	1B7	1Q7
H	1A8	Y4	1LE	1LOE	1B8	1Q8
J	2A1	D5	2TOE	2DIR	2B1	2Q1
K	2A2	Y5	GND	GND	2B2	2Q2
L	2A3	D6	VCC	VCC	2B3	2Q3
M	2A4	Y6	GND	GND	2B4	2Q4
N	2A5	D7	GND	GND	2B5	2Q5
P	2A6	Y7	VCC	VCC	2B6	2Q6
R	2A7	D8	GND	GND	2B7	2Q7
T	2A8	Y8	2LE	2LOE	2B8	2Q8

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**40103**

8-STAGE SYNCHRONOUS DOWN COUNTERS

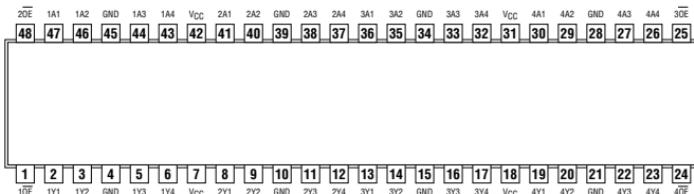


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## Pin Assignments

### 162240

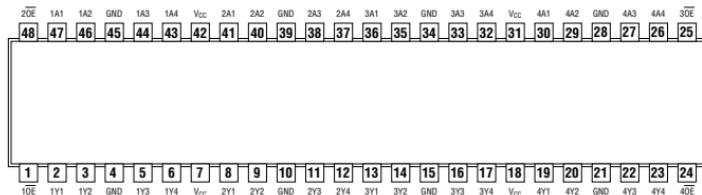
3.3-V ABT 16-BIT BUFFERS/DRIVERS  
WITH 3-STATE OUTPUTS



See page 744

### 162241

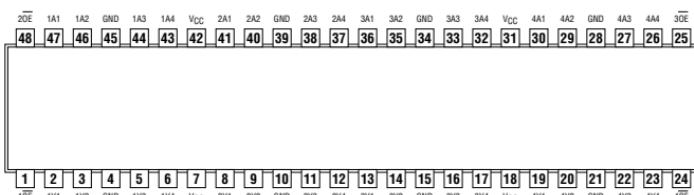
3.3-V ABT 16-BIT BUFFERS/DRIVERS  
WITH 3-STATE OUTPUTS



See page 745

### 162244

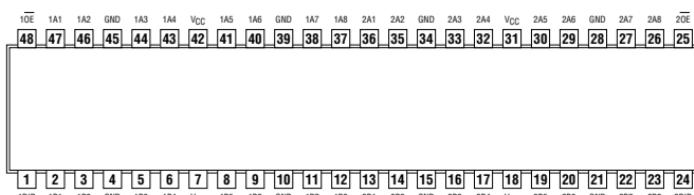
16-BIT BUFFERS/DRIVERS  
WITH 3-STATE OUTPUTS



See page 746

### 162245

16-BIT TRANSCEIVER  
WITH 3-STATE OUTPUTS



See page 747

## Pin Assignments

162260

## **12-BIT TO 24-BIT MULTIPLEXED D-TYPE LATCH WITH 3-STATE OUTPUTS**

OE2B	LEA2B	2B4	GND	2B5	2B6	V <sub>CC</sub>	2B7	2B8	2B9	GND	2B10	2B11	2B12	1B11	1B10	GND	1B9	1B8	1B7	V <sub>CC</sub>	1B6	1B5	GND	1B4	LEA1B	OE1	
56	55	54	53	52	51	50	49	48	47	46	45	44	43	42	41	40	39	38	37	36	35	34	33	32	31	30	29
1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28
OE1A	LE1B	2B3	GND	2B2	2B1	V <sub>CC</sub>	A1	A2	A3	GND	A4	A5	A6	A7	A8	A9	GND	A10	A11	A12	V <sub>CC</sub>	1B1	1B2	GND	1B3	LE2B	SEL

See page 748

162268

## **12-BIT TO 24-BIT REGISTERED BUS EXCHANGER WITH 3-STATE OUTPUTS**

DEB	CLKENA2	284	GND	285	286	V <sub>CC</sub>	287	288	289	GND	2810	2811	2812	1812	1811	1810	GND	189	188	187	V <sub>CC</sub>	186	185	GND	184	CLKENAT2	CL
56	55	54	53	52	51	50	49	48	47	46	45	44	43	42	41	40	39	38	37	36	35	34	33	32	31	30	29

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162280

## **16-BIT TO 32-BIT REGISTERED BUS EXCHANGER WITH BYTE MASKS AND 3-STATE OUTPUTS**

Yer	GND	188	288	180	GND	289	182	289	2010	Yer	1811	2811	1822	2812	GND	1813	2813	1814	2814	Yer	GND	1815	2815	1816	2816	Yer	A16	A15	A14	GND	A13	A12	A11	Yer	A10	A9	A8	GND	A7	DIF
89	79	78	77	76	75	74	73	72	71	70	69	68	67	66	65	64	63	62	61	60	59	58	57	56	55	54	53	52	51	50	49	48	47	46	45	44	43	42	41	

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162282

## **18-BIT TO 36-BIT REGISTERED BUS EXCHANGER WITH 3-STATE OUTPUTS**

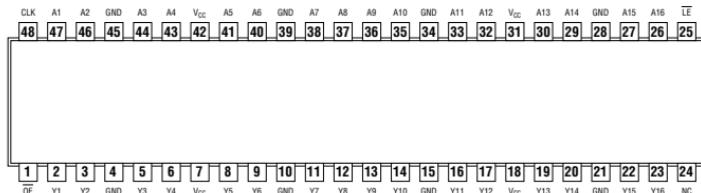
Vcc	GND	1810	2810	1821	GND	2811	1812	Vcc	1813	2812	1814	2814	GND	1815	2813	1816	2816	Vcc	GND	1817	2817	1818	2818	Vcc	A15	A17	A16	GND	A15	A13	A14	A12	Vcc	A11	A10	GND	A10	A09	A08	A07	D1
1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36	37	38	39	40		
80	79	78	77	76	75	74	73	72	71	70	69	68	67	66	65	64	63	62	61	60	59	58	57	56	55	54	53	52	51	50	49	48	47	46	45	44	43	42	41		

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# Pin Assignments

## 162334

16-BIT UNIVERSAL BUS DRIVER  
WITH 3-STATE OUTPUTS

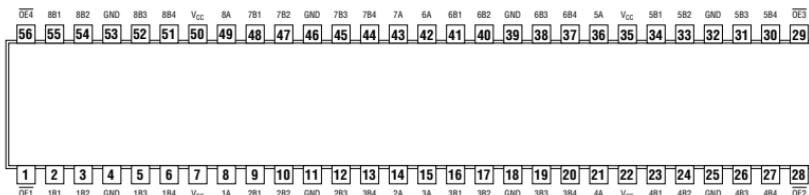


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NC-No internal connection

## 162344

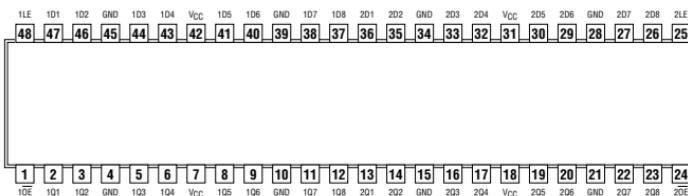
1-BIT TO 4-BIT ADDRESS DRIVER  
WITH 3-STATE OUTPUTS



See page 758

## 162373

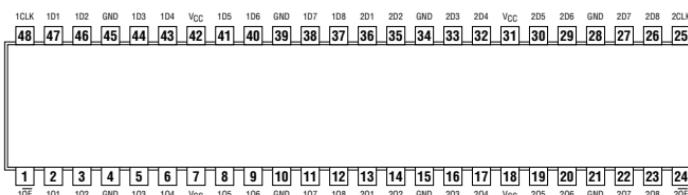
3.3-V ABT 16-BIT TRANSPARENT D-TYPE LATCHES  
WITH 3-STATE OUTPUTS



See page 760

## 162374

3.3-V ABT 16-BIT EDGE-TRIGGERED D-TYPE FLIP-FLOPS  
WITH 3-STATE OUTPUTS



See page 761

# Pin Assignments

## 162460

4-TO-1 MULTIPLEXED/DEMUTIPLEXED REGISTERED TRANSCEIVERS  
WITH 3-STATE OUTPUTS

OE <sub>B1</sub>	OE <sub>B2</sub>	SEL <sub>0</sub>	GND	B1	B2	B3	V <sub>CC</sub>	B3	B4	B5	B6	GND	B7	B8	B9	B10	B11	B12	GND	B13	B14	B15	B16	B17	B18	B19	B20	B21	B22	B23	B24	B25	B26	B27	B28	OE <sub>B3</sub>	OE <sub>B4</sub>
56	55	54	53	52	51	50	49	48	47	46	45	44	43	42	41	40	39	38	37	36	35	34	33	32	31	30	29										

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## 162500

18-BIT UNIVERSAL BUS TRANSCEIVER  
WITH 3-STATE OUTPUTS

GND	CLKAB	B1	GND	B2	B3	V <sub>CC</sub>	B4	B5	B6	GND	B7	B8	B9	B10	B11	B12	GND	B13	B14	B15	B16	B17	GND	B18	CLKBA	GND											
56	55	54	53	52	51	50	49	48	47	46	45	44	43	42	41	40	39	38	37	36	35	34	33	32	31	30	29										

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## 162501

18-BIT UNIVERSAL BUS TRANSCEIVERS  
WITH 3-STATE OUTPUTS

GND	CLKAB	B1	GND	B2	B3	V <sub>CC</sub>	B4	B5	B6	GND	B7	B8	B9	B10	B11	B12	GND	B13	B14	B15	B16	B17	GND	B18	CLKBA	GND											
56	55	54	53	52	51	50	49	48	47	46	45	44	43	42	41	40	39	38	37	36	35	34	33	32	31	30	29										

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## 162525

18-BIT REGISTERED BUS TRANSCEIVER  
WITH 3-STATE OUTPUTS

SEL	CLKAB	B1	GND	B2	B3	V <sub>CC</sub>	B4	B5	B6	GND	B7	B8	B9	B10	B11	B12	GND	B13	B14	B15	B16	B17	GND	B18	CLKBA	CLKSA											
56	55	54	53	52	51	50	49	48	47	46	45	44	43	42	41	40	39	38	37	36	35	34	33	32	31	30	29										

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# Pin Assignments

## 162541

3.3-V ABT 16-BIT BUFFERS/DRIVERS  
WITH 3-STATE OUTPUTS

10E2	1A1	1A2	GND	1A3	1A4	V <sub>CC</sub>	1A5	1A6	GND	1A7	1A8	2A1	2A2	GND	2A3	2A4	V <sub>CC</sub>	2A5	2A6	GND	2A7	2A8	20E2
48	47	46	45	44	43	42	41	40	39	38	37	36	35	34	33	32	31	30	29	28	27	26	25

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## 162601

18-BIT UNIVERSAL BUS TRANSCEIVER  
WITH 3-STATE OUTPUTS

CLXENAB	CLKAB	B1	GND	B2	B3	V <sub>CC</sub>	B4	B5	B6	GND	B7	B8	B9	B10	B11	B12	GND	B13	B14	B15	V <sub>CC</sub>	B16	B17	GND	B18	CLKBA	CLXENBA
56	55	54	53	52	51	50	49	48	47	46	45	44	43	42	41	40	39	38	37	36	35	34	33	32	31	30	29

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## 162721

3.3-V 20-BIT FLIP-FLOP  
WITH 3-STATE OUTPUTS

CLK	D1	D2	GND	D3	D4	V <sub>CC</sub>	D5	D6	D7	GND	D8	D9	D10	D11	D12	D13	GND	D14	D15	D16	V <sub>CC</sub>	D17	D18	GND	D19	D20	CLKEN
56	55	54	53	52	51	50	49	48	47	46	45	44	43	42	41	40	39	38	37	36	35	34	33	32	31	30	29

See page 774

NC-No internal connection

## 162820

3.3-V 10-BIT FLIP-FLOP WITH DUAL OUTPUTS  
AND 3-STATE OUTPUTS

CLK	D1	NC	GND	D2	NC	V <sub>CC</sub>	D3	NC	D4	GND	NC	D5	NC	D6	NC	D7	GND	NC	D8	NC	V <sub>CC</sub>	D9	NC	GND	D10	NC	NC
56	55	54	53	52	51	50	49	48	47	46	45	44	43	42	41	40	39	38	37	36	35	34	33	32	31	30	29

See page 775

NC-No internal connection

# Pin Assignments

## 162823

18-BIT BUS-INTERFACE FLIP-FLOPS  
WITH 3-STATE OUTPUTS

1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28
1CLR	1OE	101	GND	102	103	V <sub>CC</sub>	104	105	106	GND	107	108	109	201	202	203	GND	204	205	206	V <sub>CC</sub>	207	208	GND	209	210	2CLK

See page 776

## 162825

18-BIT BUFFERS/DRIVERS WITH 3-STATE OUTPUTS

1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28
1OE1	1Y1	1Y2	GND	1Y3	1Y4	V <sub>CC</sub>	1Y5	1Y6	1Y7	GND	1Y8	1Y9	1Y10	2Y1	2Y2	2Y3	GND	2A4	2A5	V <sub>CC</sub>	2A7	2A8	GND	2A9	2A10	2OE2	

See page 777

## 162827

20-BIT BUS BUFFERS/DRIVERS WITH 3-STATE OUTPUTS

1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28
1OE1	1Y1	1Y2	GND	1Y3	1Y4	V <sub>CC</sub>	1Y5	1Y6	1Y7	GND	1Y8	1Y9	GND	2Y1	2Y2	GND	2A3	2A4	V <sub>CC</sub>	2A6	2A7	GND	2A8	2A9	2A10	2OE2	

See page 778

## 162830

1-BIT TO 2-BIT ADDRESS DRIVER WITH 3-STATE OUTPUTS

1Y3	2Y3	GND	1Y4	2Y4	V <sub>CC</sub>	1Y5	2Y5	GND	1Y6	2Y6	GND	1Y7	2Y7	V <sub>CC</sub>	1Y8	2Y8	GND	1Y9	2Y9	GND	1Y10	2Y10	GND	1Y11	2Y11	GND	1Y12	2Y12	GND	1Y13	2Y13	GND	1Y14	2Y14	V <sub>CC</sub>	1Y15	2Y15	GND	1Y16	2Y16	V <sub>CC</sub>	1Y17	2Y17	GND	1Y18	2Y18	V <sub>CC</sub>
89	79	78	77	76	75	74	73	72	71	70	69	68	67	66	65	64	63	62	61	60	59	58	57	56	55	54	53	52	51	50	49	48	47	46	45	44	43	42	41								

See page 779

# Pin Assignments

## 162831

1-BIT TO 4-BIT ADDRESS REGISTER/DRIVER  
WITH 3-STATE OUTPUTS

112	2Y2	GND	4Y2	V<sub>CC</sub>	1Y3	2Y3	GND	3Y3	4Y3	GND	1Y4	2Y4	GND	3Y4	4Y4	GND	1Y5	2Y5	GND	3Y5	4Y5	GND	1Y6	2Y6	GND	3Y6	4Y6	GND	1Y7	2Y7	GND	3Y7	4Y7	GND	1Y8	2Y8	GND	3Y8	4Y8	GND	1Y9	2Y9	GND	3Y9	4Y9	GND	1Y10	2Y10	GND	3Y10	4Y10	GND	1Y11	2Y11	GND	3Y11	4Y11	GND	1Y12	2Y12	GND	3Y12	4Y12	GND	1Y13	2Y13	GND	3Y13	4Y13	GND	1Y14	2Y14	GND	3Y14	4Y14	GND	1Y15	2Y15	GND	3Y15	4Y15	GND	1Y16	2Y16	GND	3Y16	4Y16	GND	1Y17	2Y17	GND	3Y17	4Y17	GND	1Y18	2Y18	GND	3Y18	4Y18	GND	1Y19	2Y19	GND	3Y19	4Y19	GND	1Y20	2Y20	GND	3Y20	4Y20	GND	1Y21	2Y21	GND	3Y21	4Y21	GND	1Y22	2Y22	GND	3Y22	4Y22	GND	1Y23	2Y23	GND	3Y23	4Y23	GND	1Y24	2Y24	GND	3Y24	4Y24	GND	1Y25	2Y25	GND	3Y25	4Y25	GND	1Y26	2Y26	GND	3Y26	4Y26	GND	1Y27	2Y27	GND	3Y27	4Y27	GND	1Y28	2Y28	GND	3Y28	4Y28	GND	1Y29	2Y29	GND	3Y29	4Y29	GND	1Y30	2Y30	GND	3Y30	4Y30	GND	1Y31	2Y31	GND	3Y31	4Y31	GND	1Y32	2Y32	GND	3Y32	4Y32	GND	1Y33	2Y33	GND	3Y33	4Y33	GND	1Y34	2Y34	GND	3Y34	4Y34	GND	1Y35	2Y35	GND	3Y35	4Y35	GND	1Y36	2Y36	GND	3Y36	4Y36	GND	1Y37	2Y37	GND	3Y37	4Y37	GND	1Y38	2Y38	GND	3Y38	4Y38	GND	1Y39	2Y39	GND	3Y39	4Y39	GND	1Y40	2Y40	GND	3Y40	4Y40	GND	1Y41	2Y41	GND	3Y41	4Y41	GND	1Y42	2Y42	GND	3Y42	4Y42	GND	1Y43	2Y43	GND	3Y43	4Y43	GND	1Y44	2Y44	GND	3Y44	4Y44	GND	1Y45	2Y45	GND	3Y45	4Y45	GND	1Y46	2Y46	GND	3Y46	4Y46	GND	1Y47	2Y47	GND	3Y47	4Y47	GND	1Y48	2Y48	GND	3Y48	4Y48	GND	1Y49	2Y49	GND	3Y49	4Y49	GND	1Y50	2Y50	GND	3Y50	4Y50	GND	1Y51	2Y51	GND	3Y51	4Y51	GND	1Y52	2Y52	GND	3Y52	4Y52	GND	1Y53	2Y53	GND	3Y53	4Y53	GND	1Y54	2Y54	GND	3Y54	4Y54	GND	1Y55	2Y55	GND	3Y55	4Y55	GND	1Y56	2Y56	GND	3Y56	4Y56	GND	1Y57	2Y57	GND	3Y57	4Y57	GND	1Y58	2Y58	GND	3Y58	4Y58	GND	1Y59	2Y59	GND	3Y59	4Y59	GND	1Y60	2Y60	GND	3Y60	4Y60	GND	1Y61	2Y61	GND	3Y61	4Y61	GND	1Y62	2Y62	GND	3Y62	4Y62	GND	1Y63	2Y63	GND	3Y63	4Y63	GND	1Y64	2Y64	GND	3Y64	4Y64	GND	1Y65	2Y65	GND	3Y65	4Y65	GND	1Y66	2Y66	GND	3Y66	4Y66	GND	1Y67	2Y67	GND	3Y67	4Y67	GND	1Y68	2Y68	GND	3Y68	4Y68	GND	1Y69	2Y69	GND	3Y69	4Y69	GND	1Y70	2Y70	GND	3Y70	4Y70	GND	1Y71	2Y71	GND	3Y71	4Y71	GND	1Y72	2Y72	GND	3Y72	4Y72	GND	1Y73	2Y73	GND	3Y73	4Y73	GND	1Y74	2Y74	GND	3Y74	4Y74	GND	1Y75	2Y75	GND	3Y75	4Y75	GND	1Y76	2Y76	GND	3Y76	4Y76	GND	1Y77	2Y77	GND	3Y77	4Y77	GND	1Y78	2Y78	GND	3Y78	4Y78	GND	1Y79	2Y79	GND	3Y79	4Y79	GND	1Y80	2Y80	GND	3Y80	4Y80	GND	1Y81	2Y81	GND	3Y81	4Y81	GND	1Y82	2Y82	GND	3Y82	4Y82	GND	1Y83	2Y83	GND	3Y83	4Y83	GND	1Y84	2Y84	GND	3Y84	4Y84	GND	1Y85	2Y85	GND	3Y85	4Y85	GND	1Y86	2Y86	GND	3Y86	4Y86	GND	1Y87	2Y87	GND	3Y87	4Y87	GND	1Y88	2Y88	GND	3Y88	4Y88	GND	1Y89	2Y89	GND	3Y89	4Y89	GND	1Y90	2Y90	GND	3Y90	4Y90	GND	1Y91	2Y91	GND	3Y91	4Y91	GND	1Y92	2Y92	GND	3Y92	4Y92	GND	1Y93	2Y93	GND	3Y93	4Y93	GND	1Y94	2Y94	GND	3Y94	4Y94	GND	1Y95	2Y95	GND	3Y95	4Y95	GND	1Y96	2Y96	GND	3Y96	4Y96	GND	1Y97	2Y97	GND	3Y97	4Y97	GND	1Y98	2Y98	GND	3Y98	4Y98	GND	1Y99	2Y99	GND	3Y99	4Y99	GND	1Y100	2Y100	GND	3Y100	4Y100	GND	1Y101	2Y101	GND	3Y101	4Y101	GND	1Y102	2Y102	GND	3Y102	4Y102	GND	1Y103	2Y103	GND	3Y103	4Y103	GND	1Y104	2Y104	GND	3Y104	4Y104	GND	1Y105	2Y105	GND	3Y105	4Y105	GND	1Y106	2Y106	GND	3Y106	4Y106	GND	1Y107	2Y107	GND	3Y107	4Y107	GND	1Y108	2Y108	GND	3Y108	4Y108	GND	1Y109	2Y109	GND	3Y109	4Y109	GND	1Y110	2Y110	GND	3Y110	4Y110	GND	1Y111	2Y111	GND	3Y111	4Y111	GND	1Y112	2Y112	GND	3Y112	4Y112	GND	1Y113	2Y113	GND	3Y113	4Y113	GND	1Y114	2Y114	GND	3Y114	4Y114	GND	1Y115	2Y115	GND	3Y115	4Y115	GND	1Y116	2Y116	GND	3Y116	4Y116	GND	1Y117	2Y117	GND	3Y117	4Y117	GND	1Y118	2Y118	GND	3Y118	4Y118	GND	1Y119	2Y119	GND	3Y119	4Y119	GND	1Y120	2Y120	GND	3Y120	4Y120	GND	1Y121	2Y121	GND	3Y121	4Y121	GND	1Y122	2Y122	GND	3Y122	4Y122	GND	1Y123	2Y123	GND	3Y123	4Y123	GND	1Y124	2Y124	GND	3Y124	4Y124	GND	1Y125	2Y125	GND	3Y125	4Y125	GND	1Y126	2Y126	GND	3Y126	4Y126	GND	1Y127	2Y127	GND	3Y127	4Y127	GND	1Y128	2Y128	GND	3Y128	4Y128	GND	1Y129	2Y129	GND	3Y129	4Y129	GND	1Y130	2Y130	GND	3Y130	4Y130	GND	1Y131	2Y131	GND	3Y131	4Y131	GND	1Y132	2Y132	GND	3Y132	4Y132	GND	1Y133	2Y133	GND	3Y133	4Y133	GND	1Y134	2Y134	GND	3Y134	4Y134	GND	1Y135	2Y135	GND	3Y135	4Y135	GND	1Y136	2Y136	GND	3Y136	4Y136	GND	1Y137	2Y137	GND	3Y137	4Y137	GND	1Y138	2Y138	GND	3Y138	4Y138	GND	1Y139	2Y139	GND	3Y139	4Y139	GND	1Y140	2Y140	GND	3Y140	4Y140	GND	1Y141	2Y141	GND	3Y141	4Y141	GND	1Y142	2Y142	GND	3Y142	4Y142	GND	1Y143	2Y143	GND	3Y143	4Y143	GND	1Y144	2Y144	GND	3Y144	4Y144	GND	1Y145	2Y145	GND	3Y145	4Y145	GND	1Y146	2Y146	GND	3Y146	4Y146	GND	1Y147	2Y147	GND	3Y147	4Y147	GND	1Y148	2Y148	GND	3Y148	4Y148	GND	1Y149	2Y149	GND	3Y149	4Y149	GND	1Y150	2Y150	GND	3Y150	4Y150	GND	1Y151	2Y151	GND	3Y151	4Y151	GND	1Y152	2Y152	GND	3Y152	4Y152	GND	1Y153	2Y153	GND	3Y153	4Y153	GND	1Y154	2Y154	GND	3Y154	4Y154	GND	1Y155	2Y155	GND	3Y155	4Y155	GND	1Y156	2Y156	GND	3Y156	4Y156	GND	1Y157	2Y157	GND	3Y157	4Y157	GND	1Y158	2Y158	GND	3Y158	4Y158	GND	1Y159	2Y159	GND	3Y159	4Y159	GND	1Y160	2Y160	GND	3Y160	4Y160	GND	1Y161	2Y161	GND	3Y161	4Y161	GND	1Y162	2Y162	GND	3Y162	4Y162	GND	1Y163	2Y163	GND	3Y163	4Y163	GND	1Y164	2Y164	GND	3Y164	4Y164	GND	1Y165	2Y165	GND	3Y165	4Y165	GND	1Y166	2Y166	GND	3Y166	4Y166	GND	1Y167	2Y167	GND	3Y167	4Y167	GND	1Y168	2Y168	GND	3Y168	4Y168	GND	1Y169	2Y169	GND	3Y169	4Y169	GND	1Y170	2Y170	GND	3Y170	4Y170	GND	1Y171	2Y171	GND	3Y171	4Y171	GND	1Y172	2Y172	GND	3Y172	4Y172	GND	1Y173	2Y173	GND	3Y173	4Y173	GND	1Y174	2Y174	GND	3Y174	4Y174	GND	1Y175	2Y175	GND	3Y175	4Y175	GND	1Y176	2Y176	GND	3Y176	4Y176	GND	1Y177	2Y177	GND	3Y177	4Y177	GND	1Y178	2Y178	GND	3Y178	4Y178	GND	1Y179	2Y179	GND	3Y179	4Y179	GND	1Y180	2Y180	GND	3Y180	4Y180	GND	1Y181	2Y181	GND	3Y181	4Y181	GND	1Y182	2Y182	GND	3Y182	4Y182	GND	1Y183	2Y183	GND	3Y183	4Y183	GND	1Y184	2Y184	GND	3Y184	4Y184	GND	1Y185	2Y185	GND	3Y185	4Y185	GND	1Y186	2Y186	GND	3Y186	4Y186	GND	1Y187	2Y187	GND	3Y187	4Y187	GND	1Y188	2Y188	GND	3Y188	4Y188	GND	1Y189	2Y189	GND	3Y189	4Y189	GND	1Y190	2Y190	GND	3Y190	4Y190	GND	1Y191	2Y191	GND	3Y191	4Y191	GND	1Y192	2Y192	GND	3Y192	4Y192	GND	1Y193	2Y193	GND	3Y193	4Y193	GND	1Y194	2Y194	GND	3Y194	4Y194	GND	1Y195	2Y195	GND	3Y195	4Y195	GND	1Y196	2Y196	GND	3Y196	4Y196	GND	1Y197	2Y197	GND	3Y197	4Y197	GND	1Y198	2Y198	GND	3Y198	4Y198	GND	1Y199	2Y199	GND	3Y199	4Y199	GND	1Y200	2Y200	GND	3Y200	4Y200	GND	1Y201	2Y201	GND	3Y201	4Y201	GND	1Y202	2Y202	GND	3Y202	4Y202	GND	1Y203	2Y203	GND	3Y203	4Y203	GND	1Y204	2Y204	GND	3Y204	4Y204	GND	1Y205	2Y205	GND	3Y205	4Y205	GND	1Y206	2Y206	GND	3Y206	4Y206	GND	1Y207	2Y207	GND	3Y207	4Y207	GND	1Y208	2Y208	GND	3Y208	4Y208	GND	1Y209	2Y209	GND	3Y209	4Y209	GND	1Y210	2Y210	GND	3Y210	4Y210	GND	1Y211	2Y211	GND	3Y211	4Y211	GND	1Y212	2Y212	GND	3Y212	4Y212	GND	1Y213	2Y213	GND	3Y213	4Y213	GND	1Y214	2Y214	GND	3Y214	4Y214	GND	1Y215	2Y215	GND	3Y215	4Y215	GND	1Y216	2Y216	GND	3Y216	4Y216	GND	1Y217	2Y217	GND	3Y217	4Y217	GND	1Y218	2Y218	GND	3Y218	4Y218	GND	1Y219	2Y219	GND	3Y219	4Y219	GND	1Y220	2Y220	GND	3Y220	4Y220	GND	1Y221	2Y221	GND	3Y221	4Y221	GND	1Y222	2Y222	GND	3Y222	4Y222	GND	1Y223	2Y223	GND	3Y223	4Y223	GND	1Y224	2Y224	GND	3Y224	4Y224	GND	1Y225	2Y225	GND	3Y225	4Y225	GND	1Y226	2Y226	GND	3Y226	4Y226	GND	1Y227	2Y227	GND	3Y227	4Y227	GND	1Y228	2Y228	GND	3Y228	4Y228	GND	1Y229	2Y229	GND	3Y229	4Y229	GND	1Y230	2Y230	GND	3Y230	4Y230	GND	1Y231	2Y231	GND	3Y231	4Y231	GND	1Y232	2Y232	GND	3Y232	4Y232	GND	1Y233	2Y233	GND	3Y233	4Y233	GND	1Y234	2Y234	GND	3Y234	4Y234	GND	1Y235	2Y235	GND	3Y235	4Y235	GND	1Y236	2Y236	GND	3Y236	4Y236	GND	1Y237	2Y237	GND	3Y237	4Y237	GND	1Y238	2Y238	GND	3Y238	4Y238	GND	1Y239	2Y239	GND	3Y239	4Y239	GND	1Y240	2Y240	GND	3Y240	4Y240	GND	1Y241	2Y241	GND	3Y241	4Y241	GND	1Y242	2Y242	GND	3Y242	4Y242	GND	1Y243	2Y243	GND	3Y243	4Y243	GND	1Y244	2Y244	GND	3Y244	4Y244	GND</td

## Pin Assignments

**162841**

20-BIT BUS-INTERFACE D-TYPE LATCH  
WITH 3-STATE OUTPUTS

1LE	1D1	1D2	GND	1D3	1D4	V <sub>CC</sub>	1D5	1D6	1D7	GND	1D8	1D9	1D10	2D1	2D2	2D3	GND	2D4	2D5	2D6	V <sub>CC</sub>	2D7	2D8	GND	2D9	2D10	2LE
56	55	54	53	52	51	50	49	48	47	46	45	44	43	42	41	40	39	38	37	36	35	34	33	32	31	30	29
1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28
1OE	1D1	1D2	GND	1D3	1D4	V <sub>CC</sub>	1D5	1D6	1D7	GND	1D8	1D9	1D10	2D1	2D2	2D3	GND	2D4	2D5	2D6	V <sub>CC</sub>	2D7	2D8	GND	2D9	2D10	2OE

See page 785

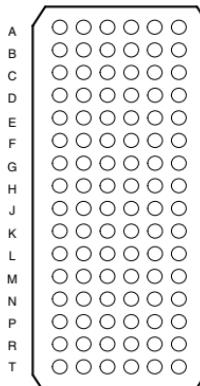
# Pin Assignments

**322244**

32-BIT BUFFER/DRIVER  
WITH 3-STATE OUTPUTS

GKE PACKAGE  
(TOP VIEW)

1 2 3 4 5 6



terminal assignments

	1	2	3	4	5	6
A	1Y2	1Y1	1OE	2OE	1A1	1A2
B	1Y4	1Y3	GND	GND	1A3	1A4
C	2Y2	2Y1	VCC	VCC	2A1	2A2
D	2Y4	2Y3	GND	GND	2A3	2A4
E	3Y2	3Y1	GND	GND	3A1	3A2
F	3Y4	3Y3	VCC	VCC	3A3	3A4
G	4Y2	4Y1	GND	GND	4A1	4A2
H	4Y3	4Y4	4OE	3OE	4A4	4A3
J	5Y2	5Y1	5OE	6OE	5A1	5A2
K	5Y4	5Y3	GND	GND	5A3	5A4
L	6Y2	6Y1	VCC	VCC	6A1	6A2
M	6Y4	6Y3	GND	GND	6A3	6A4
N	7Y2	7Y1	GND	GND	7A1	7A2
P	7Y4	7Y3	VCC	VCC	7A3	7A4
R	8Y2	8Y1	GND	GND	8A1	8A2
T	8Y3	8Y4	8OE	7OE	8A4	8A3

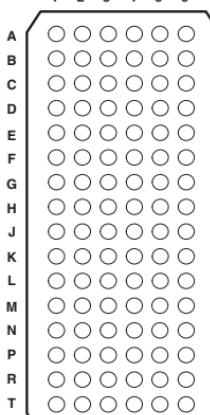
See page 786

**322374**

3.3-V ABT 32-BIT EDGE-TRIGGERED D-TYPE FLIP-FLOP WITH 3-STATE OUTPUTS

GKE PACKAGE  
(TOP VIEW)

1 2 3 4 5 6



terminal assignments

	1	2	3	4	5	6
A	1Q2	1Q1	1OE	1CLK	1D1	1D2
B	1Q4	1Q3	GND	GND	1D3	1D4
C	1Q6	1Q5	VCC	VCC	1D5	1D6
D	1Q8	1Q7	GND	GND	1D7	1D8
E	2Q2	2Q1	GND	GND	2D1	2D2
F	2Q4	2Q3	VCC	VCC	2D3	2D4
G	2Q6	2Q5	GND	GND	2D5	2D6
H	2Q7	2Q8	2OE	2CLK	2D8	2D7
J	3Q2	3Q1	3OE	3CLK	3D1	3D2
K	3Q4	3Q3	GND	GND	3D3	3D4
L	3Q6	3Q5	VCC	VCC	3D5	3D6
M	3Q8	3Q7	GND	GND	3D7	3D8
N	4Q2	4Q1	GND	GND	4D1	4D2
P	4Q4	4Q3	VCC	VCC	4D3	4D4
R	4Q6	4Q5	GND	GND	4D5	4D6
T	4Q7	4Q8	4OE	4CLK	4D8	4D7

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# **FUNCTION AND ELECTRICAL CHARACTERISTICS**

**Standard**



## QUADRUPLE 2-INPUT POSITIVE-NAND GATES

- Y =  $\overline{A \cdot B}$
- 74AC11xxx: Product Available in Reduced-Noise Advanced CMOS (11000 Series)
- 74ACT11xxx: Product Available in Reduced-Noise Advanced CMOS (11000 Series)



## ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	TTL	LS	S	ALS	AS	F	SN74 HC	CD74 HC	SN74 HCT	CD74 HCT	AC 11	SN74 AC	CD74 AC	UNIT
I <sub>CC</sub>	MAX	22	4.4	36	3	17.4	10.2	0.02	0.04	0.02	0.04	0.04	0.02	0.08	mA
I <sub>OH</sub>	MAX	-0.4	-0.4	-1	-0.4	-2	-1	-4	-4	-4	-4	-24	-24	-24	mA
I <sub>OL</sub>	MAX	16	8	20	8	20	20	4	4	4	4	24	24	24	mA

PARAMETER	MAX or MIN	ACT 11	SN74 ACT	CD74 ACT	AHC	AHCT	LV 3V	LV 5V	LVC 3V	ALVC 3V	AUC 1.8V	AUC 2.3V	UNIT
I <sub>CC</sub>	MAX	0.04	0.02	0.08	0.02	0.02	-	0.02	0.01	0.01	0.01	0.01	mA
I <sub>OH</sub>	MAX	-24	-24	-24	-8	-8	-6	-12	-24	-24	-8	-9	mA
I <sub>OL</sub>	MAX	24	24	24	8	8	6	12	24	24	8	9	mA

## SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	TTL	LS	S	ALS	AS	F	SN74 HC	CD74 HC	SN74 HCT
I <sub>PLH</sub>	A or B	Y	MAX	22	15	4.5	11	4.5	6	23	27	25
I <sub>PHL</sub>	A or B	Y	MAX	15	15	5	8	4	5.3	23	27	25

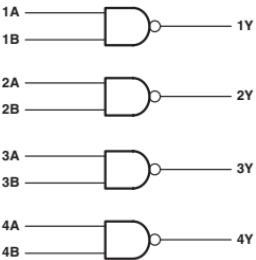
PARAMETER	INPUT	OUTPUT	MAX or MIN	CD74 HCT	AC 11	SN74 AC	CD74 AC	ACT 11	SN74 ACT	CD74 ACT	AHC	AHCT
I <sub>PLH</sub>	A or B	Y	MAX	30	7.4	8.5	7.3	12.3	9.5	10.8	8.5	9
I <sub>PHL</sub>	A or B	Y	MAX	30	6.8	7	7.3	8.8	8	13.2	8.5	9

PARAMETER	INPUT	OUTPUT	MAX or MIN	LV 3V	LV 5V	LVC 3V	ALVC 3V	AUC 1.8V	AUC 2.3V
I <sub>PLH</sub>	A or B	Y	MAX	13	8.5	4.3	3	2.4	2
I <sub>PHL</sub>	A or B	Y	MAX	13	8.5	4.3	3	2.4	2

UNIT:ns

**QUADRUPLE 2-INPUT POSITIVE-NAND GATES  
WITH OPEN-COLLECTOR OUTPUTS**

- Y =  $\overline{A \oplus B}$


**ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS**

PARAMETER	MAX or MIN	TTL	LS	ALS	HC	UNIT
I <sub>CC</sub>	MAX	22	4.4	3	0.02	mA
V <sub>DH</sub>	MAX	5.5	5.5	5.5	V <sub>CC</sub>	V
I <sub>OL</sub>	MAX	16	8	8	4	mA

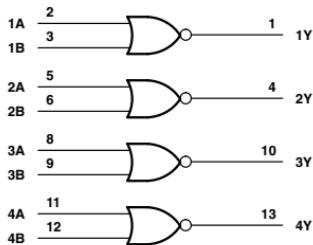
**SWITCHING CHARACTERISTICS**

PARAMETER	INPUT	OUTPUT	MAX or MIN	TTL	LS	ALS	HC
t <sub>PLH</sub>	A or B	Y	MAX	55	32	54	31
t <sub>PHL</sub>	A or B	Y	MAX	15	28	28	25

UNIT:ns

## QUADRUPLE 2-INPUT POSITIVE-NOR GATES

- $Y = \overline{A + B}$
- 74AC11xxx: Product Available in Reduced-Noise Advanced CMOS (11000 Series)
- 74ACT11xxx: Product Available in Reduced-Noise Advanced CMOS (11000 Series)



## ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	TTL	LS	S	ALS	AS	F	SN74 HC	CD74 HC	SN74 HCT	CD74 HCT	UNIT
I <sub>CC</sub>	MAX	27	5.4	45	4	20.1	13	0.02	0.04	0.02	0.04	mA
I <sub>OH</sub>	MAX	-0.4	-0.4	-1	-0.4	-2	-1	-4	-4	-4	-4	mA
I <sub>OL</sub>	MAX	16	8	20	8	20	20	4	4	4	4	mA

PARAMETER	MAX or MIN	AC 11	CD74 AC	ACT 11	CD74 ACT	AHC	AHCT	LV 3V	LV 5V	LVC 3V	AUC 1.8V	AUC 2.3V	UNIT
I <sub>CC</sub>	MAX	0.04	0.08	0.04	0.08	0.02	0.02	-	0.02	0.01	0.01	0.01	mA
I <sub>OH</sub>	MAX	-24	-24	-24	-24	-8	-8	-6	-12	-24	-8	-9	mA
I <sub>OL</sub>	MAX	24	24	24	24	8	8	6	12	24	8	9	mA

## SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	TTL	LS	S	ALS	AS	F	SN74 HC	CD74 HC	SN74 HCT	CD74 HCT
I <sub>PLH</sub>	A or B	Y	MAX	22	15	5.5	12	4.5	6.5	23	27	25	32
I <sub>PHL</sub>	A or B	Y	MAX	15	15	5.5	10	4.5	5.3	23	27	25	32

PARAMETER	INPUT	OUTPUT	MAX or MIN	AC 11	CD74 AC	ACT 11	CD74 ACT	AHC	AHCT	LV 3V	LV 5V	LVC 3V
I <sub>PLH</sub>	A or B	Y	MAX	6.9	11.5	10.6	12.2	8.5	8.5	13	8.5	4.4
I <sub>PHL</sub>	A or B	Y	MAX	6.4	11.5	8.7	12.2	8.5	8.5	13	8.5	4.4

PARAMETER	INPUT	OUTPUT	MAX or MIN	AUC 1.8V	AUC 2.3V
I <sub>PLH</sub>	A or B	Y	MAX	2.4	2
I <sub>PHL</sub>	A or B	Y	MAX	2.4	2

UNIT: ns

**QUADRUPLE 2-INPUT POSITIVE-NAND GATES  
WITH OPEN-COLLECTOR OUTPUTS**

- $Y = \overline{A \oplus B}$



ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	TTL	LS	S	ALS	SN74 HC	CD74 HC	CD74 HCT	UNIT
I <sub>CC</sub>	MAX	22	4.4	36	4	0.02	0.04	0.04	mA
V <sub>OH</sub>	MAX	5.5	8	5.5	8	V <sub>CC</sub>	V <sub>CC</sub>	V <sub>CC</sub>	V
I <sub>OL</sub>	MAX	16	0.1	20	0.1	4	4	4	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	TTL	LS	S	ALS	SN74 HC	CD74 HC	CD74 HCT
t <sub>PLH</sub>	A or B	Y	MAX	45	32	7.5	50	31	30	36
t <sub>PHL</sub>	A or B	Y	MAX	15	28	7	13	25	30	36

UNIT: ns

## HEX INVERTERS



- $Y = \bar{A}$
- 74AC11xxx: Product Available in Reduced-Noise Advanced CMOS (11000 Series)
- 74ACT11xxx: Product Available in Reduced-Noise Advanced CMOS (11000 Series)

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	TTL	LS	S	ALS	AS	F	SN74 HC	CD74 HC	SN74 HCT	CD74 HCT	AC 11	SN74 AC	UNIT
$I_{CC}$	MAX	33	6.6	54	4.2	26.3	15.3	0.02	0.04	0.02	0.04	0.04	0.02	mA
$I_{OH}$	MAX	-0.4	-0.4	-1	-0.4	-2	-1	-4	-4	-4	-4	-24	-24	mA
$I_{OL}$	MAX	16	8	20	8	20	20	4	4	4	4	24	24	mA

PARAMETER	MAX or MIN	CD74 AC	ACT 11	SN74 ACT	CD74 ACT	AHC	AHCT	LV 3V	LV 5V	LVC 3V	ALVC 3V	AUC 1.8V	AUC 2.3V	UNIT
$I_{CC}$	MAX	0.08	0.04	0.02	0.08	0.02	0.02	-	0.02	0.01	0.01	0.01	0.01	mA
$I_{OH}$	MAX	-24	-24	-24	-24	-8	-8	-6	-12	-24	-24	-8	-9	mA
$I_{OL}$	MAX	24	24	24	24	8	8	6	12	24	24	8	9	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	TTL	LS	S	ALS	AS	F	SN74 HC	CD74 HC	SN74 HCT
$t_{PLH}$	A or B	Y	MAX	22	15	4.5	11	5	6	24	26	25
$t_{PHL}$	A or B	Y	MAX	15	15	5	8	4	5.3	24	26	25

PARAMETER	INPUT	OUTPUT	MAX or MIN	CD74 HCT	AC 11	SN74 AC	CD74 AC	ACT 11	SN74 ACT	CD74 ACT	AHC	AHCT
$t_{PLH}$	A or B	Y	MAX	29	7.1	7.5	6.5	9.7	9	9.3	8.5	8.5
$t_{PHL}$	A or B	Y	MAX	29	6	7	6.5	9.6	8.5	9.3	8.5	8.5

PARAMETER	INPUT	OUTPUT	MAX or MIN	LV 3V	LV 5V	LVC 3V	ALVC 3V	AUC 1.8V	AUC 2.3V
$t_{PLH}$	A or B	Y	MAX	12	8.5	4.5	2.8	2.5	2.0
$t_{PHL}$	A or B	Y	MAX	12	8.5	4.5	2.8	2.5	2.0

UNIT: ns

# U04

## HEX INVERTERS

- $Y = \bar{A}$
- Unbuffered Output

### Logic Diagram (SN74)



ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	SN74 HC	CD74 HC	AHC	LV 3V	LV 5V	LVC 3V	AUC 1.8V	AUC 2.3V	UNIT
$I_{CC}$	MAX	0.02	0.04	0.02	-	0.02	0.01	0.01	0.01	mA
$I_{OH}$	MAX	-4	-4	-8	-6	-12	-24	-8	-9	mA
$I_{OL}$	MAX	4	4	8	6	12	24	8	9	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	SN74 HC	CD74 HC	AHC	LV 3V	LV 5V	LVC 3V	AUC 1.8V	AUC 2.3V
$t_{PLH}$	A or B	Y	MAX	20	21	8	13	8	3.8	2.0	1.7
$t_{PHL}$	A or B	Y	MAX	20	21	8	13	8	3.8	2.0	1.7

UNIT: ns

# 05

## HEX INVERTERS WITH OPEN-DRAIN OUTPUTS

- $Y = \bar{A}$

### Logic Diagram (SN74)



ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	TTL	LS	S	ALS	SN74 HC	CD74 AC	CD74 ACT	AHC	LV 3V	LV 5V	UNIT
$I_{CC}$	MAX	33	6.6	54	4.2	0.02	0.08	0.08	0.02	-	0.02	mA
$I_{OH}$	MAX	0.25	0.1	0.25	-	-	-24	-24	-	-	-	mA
$V_{OH}$	MAX	5.5	5.5	5.5	5.5	5.5	5.5	5.5	Vcc	5.5	5.5	V
$I_{OL}$	MAX	16	8	20	8	4	24	24	8	6	12	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	TTL	LS	S	ALS	SN74 HC	CD74 AC	CD74 ACT	AHC	LV 3V	LV 5V
$t_{PLH}$	A or B	Y	MAX	55	32	7.5	54	29	-	-	-	12	8.5
$t_{PHL}$	A or B	Y	MAX	15	28	7	14	21	-	-	-	12	8.5
$t_{PLZ}$	A	Y	MAX	-	-	-	-	-	8.2	9.3	8.5	-	-
$t_{PZL}$	A	Y	MAX	-	-	-	-	-	6.5	10.8	8.5	-	-

UNIT: ns

## HEX INVERTER BUFFERS/DRIVERS WITH OPEN-DRAIN OUTPUTS

- $Y = \bar{A}$

### Logic Diagram



ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	TTL	LS	LV 3V	LV 5V	LVC 3V	AUC 1.8V	AUC 2.5V	UNIT
I <sub>CC</sub>	MAX	51	60	-	0.02	0.01	0.01	0.01	mA
I <sub>OH</sub>	MAX	0.25	0.25	-	±0.0025	-	-	-	mA
V <sub>OH</sub>	MAX	30	30	5.5	5.5	5.5	3.6	3.6	V
I <sub>OL</sub>	MAX	40	40	8	16	24	8	9	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	TTL	LS	LV 3V	LV 5V	LVC 3V	AUC 1.8V	AUC 2.5V
t <sub>PLH</sub>	A or B	Y	MAX	15	15	12	8.5	3.7	2.8	1.3
t <sub>PHL</sub>	A or B	Y	MAX	23	20	12	8.5	3.7	2.8	1.3

UNIT: ns

## HEX BUFFERS/DRIVERS WITH OPEN-DRAIN OUTPUTS

### Logic Diagram



- $Y = A$

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	TTL	LS	LV 3V	LV 5V	LVC 3V	AUC 1.8V	AUC 2.5V	UNIT
I <sub>CC</sub>	MAX	41	45	-	0.02	0.01	0.01	0.01	mA
I <sub>OH</sub>	MAX	0.25	0.25	-	±0.0025	-	-	-	mA
V <sub>OH</sub>	MAX	30	30	5.5	5.5	5.5	3.6	3.6	V
I <sub>OL</sub>	MAX	40	40	8	16	24	8	9	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	TTL	LS	LV 3V	LV 5V	LVC 3V	AUC 1.8V	AUC 2.5V
t <sub>PLH</sub>	A or B	Y	MAX	15	10	12	8.5	2.9	2.3	1.3
t <sub>PHL</sub>	A or B	Y	MAX	26	30	12	8.5	2.9	2.3	1.3

UNIT: ns

**QUADRUPLE 2-INPUT  
POSITIVE-AND GATES**


- Y = A•B
- 74AC11xxx: Product Available in Reduced-Noise Advanced CMOS (11000 Series)
- 74ACT11xxx: Product Available in Reduced-Noise Advanced CMOS (11000 Series)

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	TTL	LS	S	ALS	AS	F	SN74 HC	CD74 HC	SN74 HCT	CD74 HCT	AC 11	UNIT
I <sub>CC</sub>	MAX	33	8.8	57	4	24	12.9	0.02	0.04	0.02	0.04	0.04	mA
I <sub>OH</sub>	MAX	-0.8	-0.4	-1	-0.4	-2	-1	-4	-4	-4	-4	-24	mA
I <sub>OL</sub>	MAX	16	8	20	8	20	20	4	4	4	4	24	mA

PARAMETER	MAX or MIN	SN74 AC	CD74 AC	ACT 11	SN74 ACT	CD74 ACT	AHC	AHCT	LV 3V	LV 5V	LVC 3.3V	ALVC 3V	AUC 1.8V	AUC 2.3V	UNIT
I <sub>CC</sub>	MAX	0.02	0.08	0.04	0.02	0.08	0.02	0.02	-	0.02	0.01	0.01	0.01	0.01	mA
I <sub>OH</sub>	MAX	-24	-24	-24	-24	-24	-8	-8	-6	-12	-24	-24	-8	-9	mA
I <sub>OL</sub>	MAX	24	24	24	24	24	8	8	6	12	24	24	8	9	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	TTL	LS	S	ALS	AS	F	SN74 HC	CD74 HC	SN74 HCT
t <sub>PLH</sub>	A or B	Y	MAX	27	15	7	14	5.5	6.6	25	27	30
t <sub>PHL</sub>	A or B	Y	MAX	19	20	7.5	10	5.5	6.3	25	27	30

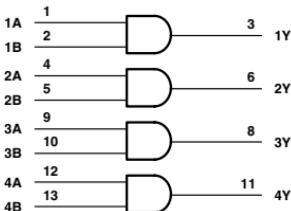
PARAMETER	INPUT	OUTPUT	MAX or MIN	CD74 HCT	AC 11	SN74 AC	CD74 AC	ACT 11	SN74 ACT	CD74 ACT	AHC	AHCT
t <sub>PLH</sub>	A or B	Y	MAX	38	6.9	8.5	8.7	9	10	12.9	9	9
t <sub>PHL</sub>	A or B	Y	MAX	38	6.5	7.5	8.7	8.2	10	12.9	9	9

PARAMETER	INPUT	OUTPUT	MAX or MIN	LV 3V	LV 5V	LVC 3.3V	ALVC 3V	AUC 1.8V	AUC 2.3V
t <sub>PLH</sub>	A or B	Y	MAX	14	9	4.1	2.9	2.3	1.8
t <sub>PHL</sub>	A or B	Y	MAX	14	9	4.1	2.9	2.3	1.8

UNIT: ns

**QUADRUPLE 2-INPUT  
POSITIVE-AND GATES  
WITH OPEN-COLLECTOR  
OUTPUTS**

●  $Y = A \cdot B$



ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	TTL	LS	S	ALS	F	SN74 HC	UNIT
I <sub>CC</sub>	MAX	33	8.8	57	4.2	26.3	15.3	mA
I <sub>OH</sub>	MAX	-	0.1	0.25	0.1	-	-	mA
V <sub>OH</sub>	MAX	5.5	5.5	5.5	5.5	5.5	V <sub>cc</sub>	mA
I <sub>OL</sub>	MAX	16	8	20	8	20	4	mA

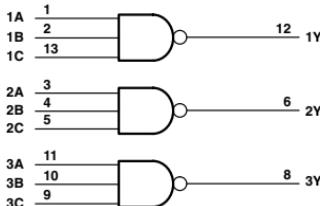
SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	TTL	LS	S	ALS	F	SN74 HC
t <sub>PLH</sub>	A or B	Y	MAX	32	35	10	54	9.6	31
t <sub>PHL</sub>	A or B	Y	MAX	24	35	10	15	4.8	25

UNIT: ns

### TRIPLE 3-INPUT POSITIVE-NAND GATES

- Y =  $\overline{A \cdot B \cdot C}$
- 74AC11xxx: Product Available in Reduced-Noise Advanced CMOS (11000 Series)
- 74ACT11xxx: Product Available in Reduced-Noise Advanced CMOS (11000 Series)



**FUNCTION TABLE**  
(each gate)

INPUTS			OUTPUT
A	B	C	Y
H	H	H	L
L	X	X	H
X	L	X	H
X	X	L	H

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	TTL	LS	S	ALS	AS	F	SN74 HC	CD74 HC	SN74 HCT	CD74 HCT	AC 11	SN74 AC	CD74 AC	UNIT
I <sub>CC</sub>	MAX	16.5	3.3	27	2.2	13	7.7	0.02	0.04	0.02	0.04	0.04	0.02	0.08	mA
I <sub>OH</sub>	MAX	-0.4	-0.4	-1	-0.4	-2	-1	-4	-4	-4	-4	-24	-24	-24	mA
I <sub>OL</sub>	MAX	16	8	20	8	20	20	4	4	4	4	24	24	24	mA

PARAMETER	MAX or MIN	ACT 11	SN74 ACT	CD74 ACT	LV 3V	LV 5V	LVC 3V	ALVC 3V	UNIT
I <sub>CC</sub>	MAX	0.04	0.04	0.08	-	0.02	0.01	0.01	mA
I <sub>OH</sub>	MAX	-24	-24	-24	-6	-12	-24	-24	mA
I <sub>OL</sub>	MAX	24	24	24	6	12	24	24	mA

SWITCHING CHARACTERISTICS

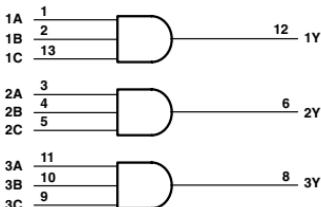
PARAMETER	INPUT	OUTPUT	MAX or MIN	TTL	LS	S	ALS	AS	F	SN74 HC	CD74 HC	SN74 HCT	CD74 HCT
t <sub>PLH</sub>	A, B or C	Y	MAX	22	15	4.5	11	4.5	6	24	30	19	36
t <sub>PHL</sub>	A, B or C	Y	MAX	15	15	5	10	4.5	5.3	24	30	19	36

PARAMETER	INPUT	OUTPUT	MAX or MIN	AC 11	SN74 AC	CD74 AC	ACT 11	SN74 ACT	CD74 ACT	LV 3V	LV 5V	LVC 3V	ALVC 3V	
t <sub>PLH</sub>	A, B or C	Y	MAX	6.7	8	12.2	8.9	10	13.5	13.5	9	4.9	3	
t <sub>PHL</sub>	A, B or C	Y	MAX	7	6.5	12.2	8.2	9.5	13.5	13.5	9	4.9	3	

UNIT: ns

### TRIPLE 3-INPUT POSITIVE-AND GATES

- Y = A•B•C
- 74AC11xxx: Product Available in Reduced-Noise Advanced CMOS (11000 Series)
- 74ACT11xxx: Product Available in Reduced-Noise Advanced CMOS (11000 Series)



**FUNCTION TABLE**  
(each gate)

INPUTS			OUTPUT
A	B	C	Y
H	H	H	H
L	X	X	L
X	L	X	L
X	X	L	L

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	LS	S	ALS	AS	F	SN74 HC	CD74 HC	SN74 HCT	CD74 HCT	AC 11	SN74 AC	UNIT
I <sub>CC</sub>	MAX	6.6	42	3	18	9.7	0.02	0.04	0.02	0.04	0.04	0.02	mA
I <sub>OH</sub>	MAX	-0.4	-1	-0.4	-2	-1	-4	-4	-4	-4	-24	-24	mA
I <sub>OL</sub>	MAX	8	20	8	20	20	4	4	4	4	24	24	mA

PARAMETER	MAX or MIN	ACT 11	SN74 ACT	LV 3V	LV 5V	UNIT
I <sub>CC</sub>	MAX	0.04	0.02	-	0.02	mA
I <sub>OH</sub>	MAX	-24	-24	-6	-12	mA
I <sub>OL</sub>	MAX	24	24	6	12	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	LS	S	ALS	AS	F	SN74 HC	CD74 HC	SN74 HCT	CD74 HCT
I <sub>PLH</sub>	A, B or C	Y	MAX	15	7	13	6	6.6	25	30	21	42
I <sub>PHL</sub>	A, B or C	Y	MAX	20	7.5	10	5.5	6.5	25	30	21	42

PARAMETER	INPUT	OUTPUT	MAX or MIN	AC 11	SN74 AC	ACT 11	SN74 ACT	LV 3V	LV 5V
I <sub>PLH</sub>	A, B or C	Y	MAX	6.5	8.5	9.6	10.5	14	9
I <sub>PHL</sub>	A, B or C	Y	MAX	6.9	7.5	8.7	10.5	14	9

UNIT: ns

**HEX SCHMITT-TRIGGER  
INVERTERS**


- $Y = \bar{A}$
- 74AC11xxx: Product Available in Reduced-Noise Advanced CMOS (Series)
- 74ACT11xxx: Product Available in Reduced-Noise Advanced CMOS (11000 Series)

**ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS**

PARAMETER	MAX or MIN	TTL	LS	SN74 HC	CD74 HC	SN74 HCT	CD74 HCT	SN74 AC	CD74 AC	SN74 ACT	CD74 ACT	AHC	AHCT	UNIT
$I_{CC}$	MAX	60	21	0.02	0.04	0.02	0.04	0.02	0.08	0.02	0.08	0.02	0.02	mA
$I_{OH}$	MAX	-0.8	-0.4	-4	-4	-4	-4	-24	-24	-24	-24	-8	-8	mA
$I_{OL}$	MAX	16	8	4	4	4	4	24	24	24	24	8	8	mA

PARAMETER	MAX or MIN	LV 3V	LV 5V	LVC 3V	ALVC 3V	AUC 1.8V	AUC 2.5V	UNIT
$I_{CC}$	MAX	-	0.02	0.01	0.01	0.01	0.01	mA
$I_{OH}$	MAX	-6	-12	-24	-24	-8	-9	mA
$I_{OL}$	MAX	6	12	24	24	8	9	mA

**SWITCHING CHARACTERISTICS**

PARAMETER	INPUT	OUTPUT	MAX or MIN	TTL	LS	SN74 HC	CD74 HC	SN74 HCT	CD74 HCT	SN74 AC	CD74 AC	SN74 ACT	CD74 ACT
$t_{PLH}$	A or B	Y	MAX	22	22	31	41	40	57	11	10.5	12.5	14.5
$t_{PHL}$	A or B	Y	MAX	22	22	31	41	40	57	9.5	10.5	11	9.5

PARAMETER	INPUT	OUTPUT	MAX or MIN	AHC	AHCT	LV 3V	LV 5V	LVC 3V	ALVC 3V	AUC 1.8V	AUC 2.5V
$t_{PLH}$	A or B	Y	MAX	12	9	18.5	12	6.4	3.4	3.5	2.7
$t_{PHL}$	A or B	Y	MAX	12	9	18.5	12	6.4	3.4	3.5	2.7

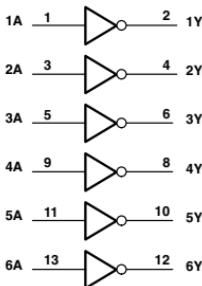
UNIT: ns

## 16

### HEX INVERTER BUFFERS/DRIVERS WITH OPEN-COLLECTOR HIGH-VOLTAGE OUTPUTS

●  $Y = \bar{A}$

#### Logic Diagram



#### ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	TTL	UNIT
$I_{CC}$	MAX	51	mA
$V_{OH}$	MAX	15	V
$I_{OL}$	MAX	40	mA

#### SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	TTL
$t_{PLH}$	A	Y	MAX	15
$t_{PHL}$	A	Y	MAX	23

UNIT: ns

## 17

### HEX SCHMITT-TRIGGER BUFFER

●  $Y = A$

#### Logic Diagram



#### ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	TTL	AUC 1.8V	AUC 2.5V	UNIT
$I_{CC}$	MAX	41	0.01	0.01	mA
$I_{OH}$	MAX	0.25	-8	-9	mA
$I_{OL}$	MAX	40	8	9	mA

#### SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	TTL	AUC 1.8V	AUC 2.5V
$t_{PLH}$	A	Y	MAX	15	2.4	1.9
$t_{PHL}$	A	Y	MAX	26	2.4	1.9

UNIT: ns

## HEX SCHMITT-TRIGGER INVERTERS

- $Y = \overline{A}$
- P-N-P Input Reduce System Loading ( $I_{IL} = -0.05\text{mA MAX}$ )
- Excellent Noise Immunity with Typical Hysteresis of 0.8V

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

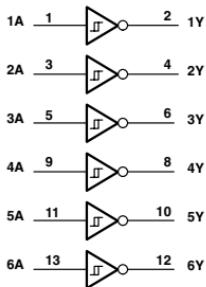
PARAMETER	MAX or MIN	LS	UNIT
$I_{CC}$	MAX	30	mA
$I_{OH}$	MAX	-0.4	mA
$I_{OL}$	MAX	8	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	LS
$t_{PLH}$	A or B	Y	MAX	20
$t_{PHL}$	A or B	Y	MAX	30

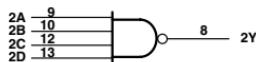
UNIT: ns

## Logic Diagram



**DUAL 4-INPUT  
POSITIVE-NAND  
GATES**

- Y =  $\overline{A \cdot B \cdot C \cdot D}$
- 74AC11xxx: Product Available in Reduced-Noise Advanced CMOS (11000 Series)
- 74ACT11xxx: Product Available in Reduced-Noise Advanced CMOS (11000 Series)


**FUNCTION TABLE  
(each gate)**

INPUTS				OUTPUT Y
A	B	C	D	
H	H	H	H	L
L	X	X	X	H
X	L	X	X	H
X	X	L	X	H
X	X	X	L	H

**ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS**

PARAMETER	MAX or MIN	TTL	LS	S	ALS	AS	F	SN74 HC	CD74 HC	CD74 HCT	UNIT
I <sub>CC</sub>	MAX	11	2.2	18	1.5	8.7	5.1	0.02	0.04	0.04	mA
I <sub>OH</sub>	MAX	-0.4	-0.4	-1	-0.4	-2	-1	-4	-4	-4	mA
I <sub>OL</sub>	MAX	16	8	20	8	20	20	4	4	4	mA

PARAMETER	MAX or MIN	AC 11	CD74 AC	ACT 11	CD74 ACT	LV 3V	LV 5V	UNIT
I <sub>CC</sub>	MAX	0.04	0.08	0.04	0.08	-	0.02	mA
I <sub>OH</sub>	MAX	-24	-24	-24	-24	-6	-12	mA
I <sub>OL</sub>	MAX	24	24	24	24	6	12	mA

**SWITCHING CHARACTERISTICS**

PARAMETER	INPUT	OUTPUT	MAX or MIN	TTL	LS	S	ALS	AS	F	SN74 HC	CD74 HC	CD74 HCT
I <sub>PLH</sub>	A, B, C or D	Y	MAX	22	15	4.5	11	5	6	28	30	42
I <sub>PHL</sub>	A, B, C or D	Y	MAX	15	15	5	10	4.5	5.3	28	30	42

PARAMETER	INPUT	OUTPUT	MAX or MIN	AC 11	CD74 AC	ACT 11	CD74 ACT	LV 3V	LV 5V
I <sub>PLH</sub>	A, B, C or D	Y	MAX	6.7	12.2	9.1	13.5	11.5	8
I <sub>PHL</sub>	A, B, C or D	Y	MAX	7.3	12.2	9.2	13.5	11.5	8

UNIT: ns

# 21

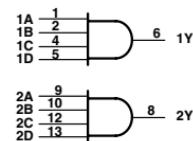
## DUAL 4-INPUT POSITIVE-AND GATES

- Y = A•B•C•D
- 74AC11xxx: Product Available in Reduced-Noise Advanced CMOS (11000 Series)
- 74ACT11xxx: Product Available in Reduced-Noise Advanced CMOS (11000 Series)

FUNCTION TABLE  
(each gate)

INPUTS				OUTPUT
A	B	C	D	
H	H	H	H	H
L	X	X	X	L
X	L	X	X	L
X	X	L	X	L
X	X	X	L	L

Logic Diagram (SN74)



### ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	LS	ALS	AS	F	SN74 HC	CD74 HC	CD74 HCT	AC 11	ACT 11	LV 3V	LV 5V	UNIT
I <sub>CC</sub>	MAX	4.4	2.3	12	7.3	0.02	0.04	0.04	0.04	0.04	-	0.02	mA
I <sub>OH</sub>	MAX	-0.4	-0.4	-2	-1	-4	-4	-4	-24	-24	-6	-12	mA
I <sub>OL</sub>	MAX	8	8	20	20	4	4	4	24	24	6	12	mA

### SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	LS	ALS	AS	F	SN74 HC	CD74 HC	CD74 HCT	AC 11	ACT 11
t <sub>PLH</sub>	A, B, C or D	Y	MAX	15	15	6	5.3	28	33	41	8.8	9.8
t <sub>PHL</sub>	A, B, C or D	Y	MAX	20	10	6	5.5	28	33	41	6.9	8.9

PARAMETER	INPUT	OUTPUT	MAX or MIN	LV 3V	LV 5V
t <sub>PLH</sub>	A, B, C or D	Y	MAX	12	8
t <sub>PHL</sub>	A, B, C or D	Y	MAX	12	8

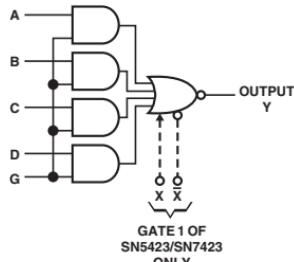
UNIT: ns

# 25

## DUAL 4-INPUT POSITIVE-NOR GATES WITH STROBE

- Y =  $\overline{G} (A + B + C + D)$

Logic Diagram (SN74)



GATE 1 OF  
SN5423/SN7423  
ONLY

FUNCTION TABLE  
(each gate)

INPUTS					OUTPUT
A	B	C	D	G	Y
H	X	X	X	H	L
X	H	X	X	H	L
X	X	H	X	H	L
X	X	X	H	H	L
L	L	L	L	X	H
X	X	X	X	L	H

### ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	TTL	UNIT
I <sub>CC</sub>	MAX	19	mA
I <sub>OH</sub>	MAX	-0.8	mA
I <sub>OL</sub>	MAX	16	mA

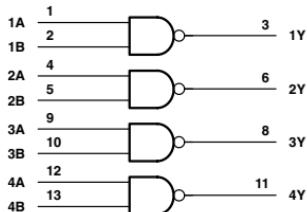
### SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	TTL
t <sub>PLH</sub>	A or B	Y	MAX	22
t <sub>PHL</sub>	A or B	Y	MAX	15

UNIT: ns

**QUADRUPLE 2-INPUT  
HIGH-VOLTAGE INTERFACE  
POSITIVE-NAND GATES**

- $Y = \overline{AB}$

**Logic Diagram****ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS**

PARAMETER	MAX or MIN	TTL	LS	UNIT
I <sub>CC</sub>	MAX	22	4.4	mA
V <sub>OH</sub>	MAX	15	15	V
I <sub>OL</sub>	MAX	16	8	mA

**SWITCHING CHARACTERISTICS**

PARAMETER	INPUT	OUTPUT	MAX or MIN	TTL	LS
I <sub>PLH</sub>	A or B	Y	MAX	24	32
I <sub>PHL</sub>	A or B	Y	MAX	17	28

UNIT: ns

**TRIPLE 3-INPUT POSITIVE-NOR GATES**

- $Y = \overline{A + B + C}$
- 74AC11xxx: Product Available in Reduced-Noise Advanced CMOS (11000 Series)
- 74ACT11xxx: Product Available in Reduced-Noise Advanced CMOS (11000 Series)

**FUNCTION TABLE  
(each gate)**

INPUTS			OUTPUT
A	B	C	Y
H	X	X	L
X	H	X	L
X	X	H	L
L	L	L	H

**Logic Diagram (SN74)****ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS**

PARAMETER	MAX or MIN	TTL	LS	ALS	AS	F	SN74 HC	CD74 HC	CD74 HCT	AC 11	ACT 11	LV 3V	LV 5V	UNIT
I <sub>CC</sub>	MAX	26	6.8	4	17.1	12	0.02	0.04	0.04	0.04	0.04	-	0.02	mA
I <sub>OL</sub>	MAX	-0.8	-0.4	-0.4	-2	-1	-4	-4	-4	-24	-24	-6	-12	mA
I <sub>OL</sub>	MAX	16	8	8	20	20	4	4	4	24	24	6	12	mA

**SWITCHING CHARACTERISTICS**

PARAMETER	INPUT	OUTPUT	MAX or MIN	TTL	LS	ALS	AS	F	SN74 HC	CD74 HC	CD74 HCT	AC 11
I <sub>PLH</sub>	A, B or C	Y	MAX	15	15	15	5.5	5.5	23	29	35	7.7
I <sub>PHL</sub>	A, B or C	Y	MAX	11	15	9	4.5	4.5	23	29	35	8.1

PARAMETER	INPUT	OUTPUT	MAX or MIN	ACT 11	LV 3V	LV 5V
I <sub>PLH</sub>	A, B or C	Y	MAX	10.1	14	9
I <sub>PHL</sub>	A, B or C	Y	MAX	9.4	14	9

UNIT: ns

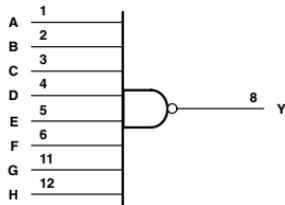
## 8-INPUT POSITIVE-NAND GATES

- Y =  $\overline{A \cdot B \cdot C \cdot D \cdot E \cdot F \cdot G \cdot H}$
- 74AC11xxx: Product Available in Reduced-Noise Advanced CMOS (11000 Series)
- 74ACT11xxx: Product Available in Reduced-Noise Advanced CMOS (11000 Series)

FUNCTION TABLE

INPUTS A-H	OUTPUT Y
All inputs H	L
One or more inputs L	H

Logic Diagram (SN74)



ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

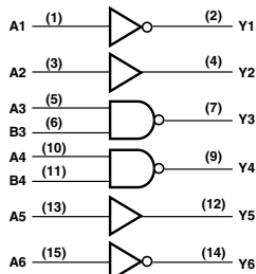
PARAMETER	MAX or MIN	TTL	LS	S	ALS	AS	F	SN74 HC	CD74 HC	CD74 HCT	AC 11	ACT 11	UNIT
$I_{CC}$	MAX	6	1.1	10	0.9	4.9	4	0.02	0.04	0.04	0.04	0.04	mA
$I_{OH}$	MAX	-0.4	-0.4	-1	-0.4	-2	-1	-4	-4	-4	-24	-24	mA
$I_{OL}$	MAX	16	8	20	8	20	20	4	4	4	24	24	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	TTL	LS	S	ALS	AS	F	SN74 HC	CD74 HC	CD74 HCT	AC 11	ACT 11
$t_{PLH}$	A thru H	Y	MAX	22	15	6	10	5	5.5	33	39	42	7.2	8.5
$t_{PHL}$	A thru H	Y	MAX	15	20	7	12	4.5	5	33	39	42	7.4	8.7

UNIT: ns

Logic Diagram



## DELAY ELEMENTS

- Delay Elements for Generating Delay Line
- Inverting and Non-inverting Elements
- Buffer NAND Elements Rated at  $I_{OL}$  of 12/24mA
- P-N-P Inputs Reduce Fan-In ( $I_{IL} = -0.2$ mA MAX)
- Worst Case MIN/MAX Delays Guaranteed Across Temperature and  $V_{CC}$  Range

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	LS	UNIT
$I_{CC}$	MAX	20	mA
$I_{OH}$	Y3, Y4 outputs All other outputs	MAX -0.4	mA
$I_{OL}$	Y3, Y4 outputs All other outputs	MAX 8	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	LS
$t_{PLH}$	A1, A6	Y1, Y6	MAX	65
$t_{PHL}$	A2, A5	Y2, Y5	MAX	45
$t_{PLH}$	A3, B3	Y3, Y4	MAX	80
$t_{PHL}$	A4, Y4	Y3, Y4	MAX	95
$t_{PLH}$	A3, B3	Y3, Y4	MAX	15
$t_{PHL}$	A4, Y4	Y3, Y4	MAX	15

UNIT: ns

## QUADRUPLE 2-INPUT POSITIVE-OR GATES

$$\bullet Y = A + B$$



## ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	TTL	LS	S	ALS	AS	F	SN74 HC	CD74 HC	SN74 HCT	CD74 HCT	AC 11	UNIT
I <sub>CC</sub>	MAX	38	9.8	68	4.9	26.6	15.5	0.02	0.04	0.02	0.04	0.04	mA
I <sub>OH</sub>	MAX	-0.8	-0.4	-1	-0.4	-2	-1	-4	-4	-4	-4	-24	mA
I <sub>OL</sub>	MAX	16	8	20	8	20	20	4	4	4	4	24	mA

PARAMETER	MAX or MIN	SN74 AC	CD74 AC	ACT 11	SN74 ACT	CD74 ACT	AHC	AHCT	LV 3V	LV 5V	LVC 3V	ALVC 3V	AUC 1.8V	AUC 2.3V	UNIT
I <sub>CC</sub>	MAX	0.02	0.08	0.04	0.02	0.08	0.02	0.02	0.02	0.02	0.01	0.01	0.01	0.01	mA
I <sub>OH</sub>	MAX	-24	-24	-24	-24	-24	-8	-8	-6	-12	-24	-24	-8	-9	mA
I <sub>OL</sub>	MAX	24	24	24	24	24	8	8	6	12	24	24	8	9	mA

## SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	TTL	LS	S	ALS	AS	F	SN74 HC	CD74 HC	SN74 HCT
I <sub>PLH</sub>	A or B	Y	MAX	15	22	7	14	5.8	6.6	25	27	30
I <sub>PHL</sub>	A or B	Y	MAX	22	22	7	12	5.8	-	25	27	30

PARAMETER	INPUT	OUTPUT	MAX or MIN	CD74 HCT	AC 11	SN74 AC	CD74 AC	ACT 11	SN74 ACT	CD74 ACT	AHC	AHCT
I <sub>PLH</sub>	A or B	Y	MAX	36	6.7	8.5	9.5	9	10	12.1	8.5	9
I <sub>PHL</sub>	A or B	Y	MAX	36	5.9	7.5	9.5	8	10	12.1	8.5	9

PARAMETER	INPUT	OUTPUT	MAX or MIN	LV 3V	LV 5V	LVC 3V	ALVC 3V	AUC 1.8V	AUC 2.3V
I <sub>PLH</sub>	A or B	Y	MAX	13	8.5	3.8	2.8	2.5	2.1
I <sub>PHL</sub>	A or B	Y	MAX	13	8.5	3.8	2.8	2.5	2.1

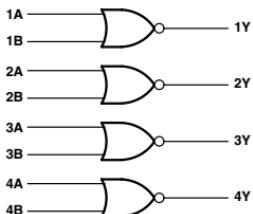
UNIT: ns

### 33

**QUADRUPLE 2-INPUT  
POSITIVE-NOR BUFFERS  
WITH OPEN-COLLECTOR  
OUTPUTS**

●  $Y = \overline{A} + \overline{B}$

**Logic Diagram**



ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	TTL	LS	ALS	UNIT
$I_{CC}$	MAX	16.5	13.8	9	mA
$V_{OH}$	MAX	5.5	5.5	5.5	V
$I_{OL}$	MAX	48	24	24	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	TTL	LS	ALS
$t_{PLH}$	A or B	Y	MAX	15	32	33
$t_{PHL}$	A or B	Y	MAX	18	28	12

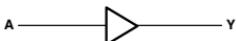
UNIT: ns

### 34

**HEX BUFFER GATE**

●  $Y = A$

**Logic Diagram**



**FUNCTION TABLE  
(each gate)**

INPUT	OUTPUT
A	Y
H	H
L	L

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	AUC 1.8V	AUC 2.5V	UNIT
$I_{CC}$	MAX	0.01	0.01	mA
$I_{OH}$	MAX	-8	-9	mA
$I_{OL}$	MAX	8	9	mA

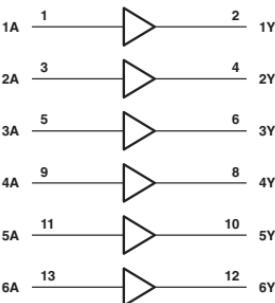
SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	AUC 1.8V	AUC 2.5V
$t_{PLH}$	A	Y	MAX	2.4	1.8
$t_{PHL}$				2.4	1.8

UNIT: ns

**HEX NONINVERTERS  
WITH OPEN-COLLECTOR  
OUTPUTS**

● Y = A

**Logic Diagram**

**ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS**

PARAMETER	MAX or MIN	ALS	UNIT
I <sub>CC</sub>	MAX	63	mA
V <sub>OH</sub>	MAX	5.5	V
I <sub>OL</sub>	MAX	8	mA

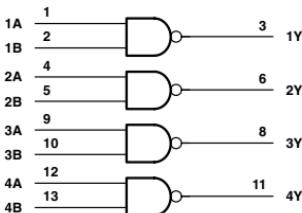
**SWITCHING CHARACTERISTICS**

PARAMETER	INPUT	OUTPUT	MAX or MIN	ALS
t <sub>PLH</sub>	A	Y	MAX	50
t <sub>PHL</sub>	A	Y	MAX	14

UNIT: ns

**QUADRUPLE 2-INPUT  
POSITIVE-NAND BUFFERS**

- Y =  $\overline{A \oplus B}$



## ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	TTL	LS	S	ALS	F	UNIT
I <sub>CC</sub>	MAX	54	12	80	7.8	33	mA
I <sub>OH</sub>	MAX	-1.2	-1.2	-3	-2.6	-15	mA
I <sub>OL</sub>	MAX	48	24	60	24	64	mA

## SWITCHING CHARACTERISTICS

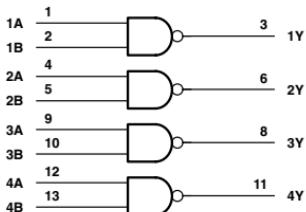
PARAMETER	INPUT	OUTPUT	MAX or MIN	TTL	LS	S	ALS	F
t <sub>PLH</sub>	A or B	Y	MAX	22	24	6.5	8	6.5
t <sub>PHL</sub>	A or B	Y	MAX	15	24	6.5	7	5

UNIT: ns

**QUADRUPLE 2-INPUT  
POSITIVE-NAND BUFFERS  
WITH OPEN-COLLECTOR OUTPUTS**

●  $Y = \overline{A \cdot B}$

**Logic Diagram**



ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	TTL	LS	S	ALS	F	UNIT
I <sub>CC</sub>	MAX	54	12	80	7.8	30	mA
V <sub>OH</sub>	MAX	5.5	5.5	5.5	5.5	4.5	V
I <sub>OL</sub>	MAX	48	24	60	24	64	mA

SWITCHING CHARACTERISTICS

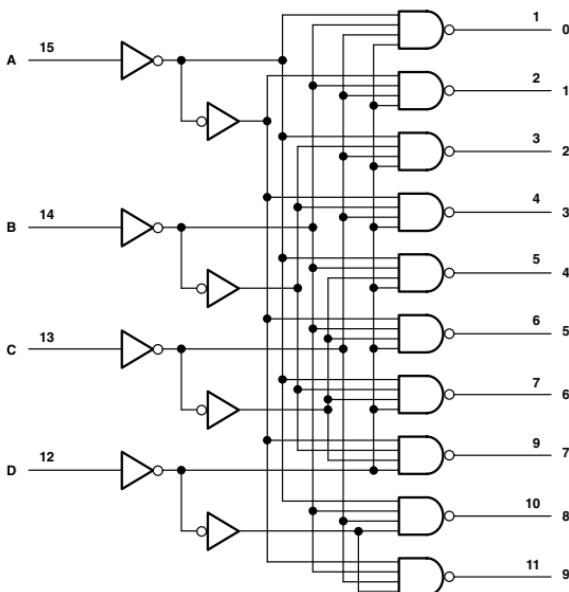
PARAMETER	INPUT	OUTPUT	MAX or MIN	TTL	LS	S	ALS	F
t <sub>PLH</sub>	A or B	Y	MAX	22	32	10	33	13
t <sub>PHL</sub>	A or B	Y	MAX	18	28	10	12	5.5

UNIT: ns

## 4-LINE-TO-10-LINE DECODERS (1 of 10)

- All Outputs Are High for Invalid Input Conditions
- Also for Applications as
  - 3-Line to 8-Line Decoders
  - 4-Line to 16-Line Decoders
- Full Decoding of Valid Input Logic Ensures That All Inputs Remain Off for All Invalid Input Conditions

Logic Diagram (SN74)



FUNCTION TABLE (SN74)

No.	INPUTS				OUTPUTS									
	D	C	B	A	0	1	2	3	4	5	6	7	8	9
0	L	L	L	L	L	H	H	H	H	H	H	H	H	H
1	L	L	L	H	H	L	H	H	H	H	H	H	H	H
2	L	L	H	L	H	H	L	H	H	H	H	H	H	H
3	L	L	H	H	H	H	H	L	H	H	H	H	H	H
4	L	H	L	L	H	H	H	H	L	H	H	H	H	H
5	L	H	L	H	H	H	H	H	H	L	H	H	H	H
6	L	H	H	L	H	H	H	H	H	H	L	H	H	H
7	L	H	H	H	H	H	H	H	H	H	L	H	H	H
8	H	L	L	L	H	H	H	H	H	H	H	L	H	H
9	H	L	L	H	H	H	H	H	H	H	H	H	L	H
INVALID	H	L	H	L	H	H	H	H	H	H	H	H	H	H
	H	L	H	H	H	H	H	H	H	H	H	H	H	H
	H	H	L	L	H	H	H	H	H	H	H	H	H	H
	H	H	L	H	H	H	H	H	H	H	H	H	H	H
	H	H	H	L	H	H	H	H	H	H	H	H	H	H
	H	H	H	H	H	H	H	H	H	H	H	H	H	H
	H	H	H	H	H	H	H	H	H	H	H	H	H	H

## ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	TTL	LS	SN74 HC	CD74 HC	CD74 HCT	UNIT
I <sub>CC</sub>	MAX	56	13	0.08	0.16	0.16	mA
I <sub>OH</sub>	MAX	-0.8	-0.4	-4	-4	-4	mA
I <sub>OL</sub>	MAX	16	8	4	4	4	mA

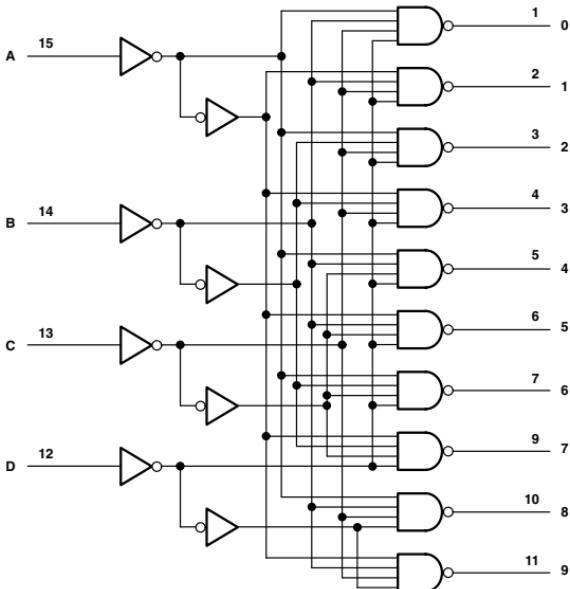
## SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	TTL	LS	SN74 HC	CD74 HC	CD74 HCT
I <sub>PLH</sub> 2Level - Logic	A, B, C or D	0-9	MAX	25	25	38	45	53
		0-9		25	25	38	45	53
I <sub>PHL</sub> 2Level - Logic	A, B, C or D	0-9	MAX	30	30	38	45	53
		0-9		30	30	38	45	53
I <sub>PLH</sub> 3Level - Logic	A, B, C or D	0-9	MAX	30	30	38	45	53
		0-9		30	30	38	45	53

UNIT: ns

**BCD-TO-DECIMAL DECODERS/DRIVERS**

- 80-mA Sink-Current Capability
- All Outputs Are Off for Invalid BCD Input Conditions

**Logic Diagram (SN74)**

FUNCTION TABLE

No.	INPUTS				OUTPUTS									
	D	C	B	A	0	1	2	3	4	5	6	7	8	9
0	L	L	L	L	L	H	H	H	H	H	H	H	H	H
1	L	L	L	H	H	L	H	H	H	H	H	H	H	H
2	L	L	H	L	H	H	L	H	H	H	H	H	H	H
3	L	L	H	H	H	H	H	L	H	H	H	H	H	H
4	L	H	L	L	H	H	H	H	L	H	H	H	H	H
5	L	H	L	H	H	H	H	H	H	L	H	H	H	H
6	L	H	H	L	H	H	H	H	H	H	L	H	H	H
7	L	H	H	H	H	H	H	H	H	H	H	L	H	H
8	H	L	L	L	H	H	H	H	H	H	H	H	L	H
9	H	L	L	H	H	H	H	H	H	H	H	H	H	L
INVALID	H	L	H	L	H	H	H	H	H	H	H	H	H	H
INVALID	H	L	H	H	H	H	H	H	H	H	H	H	H	H
INVALID	H	H	L	L	H	H	H	H	H	H	H	H	H	H
INVALID	H	H	L	H	H	H	H	H	H	H	H	H	H	H
INVALID	H	H	H	L	H	H	H	H	H	H	H	H	H	H
INVALID	H	H	H	H	H	H	H	H	H	H	H	H	H	H

## ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING C

PARAMETER	MAX or MIN	TTL	UNIT
I <sub>CC</sub>	MAX	70	mA
V <sub>O(on)</sub>	MAX	0.9	V
I <sub>OL</sub>	MAX	80	mA

UNIT: ns

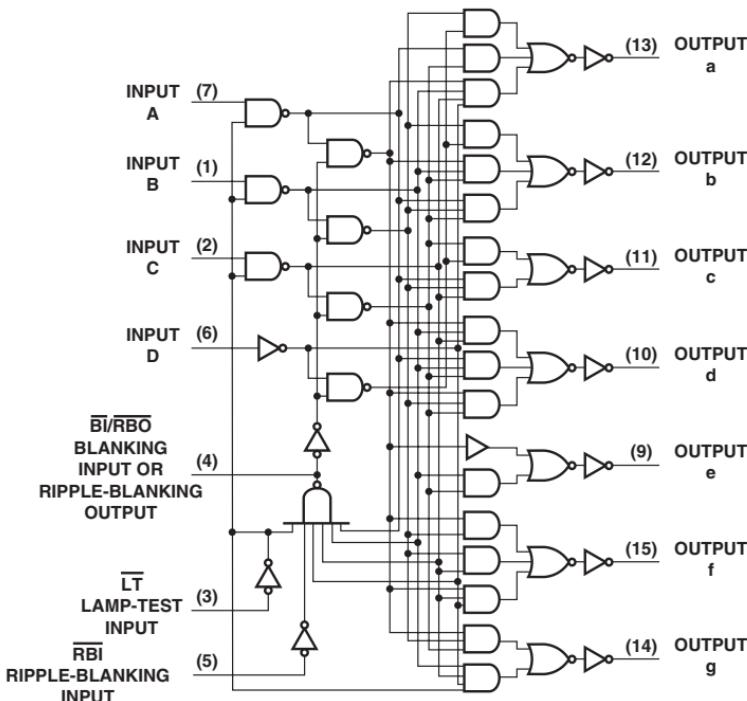
## SWITCHING CHARACTERISTICS

PARAMETER	MAX or MIN	TTL
t <sub>PLH</sub>	MAX	25
t <sub>PHL</sub>		25

## BCD-TO-SEVEN-SEGMENT DECODERS/DRIVERS

- Open-Collector Outputs
- Lamp-Test Provision
- Leading/Trailing Zero Suppression

Logic Diagram



FUNCTION TABLE

No.	INPUTS					$\overline{BI/RBO}$ <sup>†</sup>	OUTPUTS							
	LT	RBI	D	C	B	A	a	b	c	d	e	f	g	
0	H	H	L	L	L	L	H	ON	ON	ON	ON	ON	ON	OFF
1	H	X	L	L	L	H	H	OFF	ON	ON	OFF	OFF	OFF	OFF
2	H	X	L	L	H	L	H	ON	ON	OFF	ON	OFF	ON	ON
3	H	X	L	L	H	H	H	ON	ON	ON	ON	ON	OFF	ON
4	H	X	L	H	L	L	H	OFF	ON	ON	OFF	OFF	ON	ON
5	H	X	L	H	L	H	H	ON	OFF	ON	ON	OFF	ON	ON
6	H	X	L	H	H	L	H	OFF	OFF	ON	ON	ON	ON	ON
7	H	X	L	H	H	H	H	ON	ON	ON	OFF	OFF	ON	OFF
8	H	X	H	L	L	L	H	ON						
9	H	X	H	L	L	H	H	ON	ON	OFF	ON	ON	ON	ON
10	H	X	H	L	H	L	H	OFF	OFF	OFF	ON	OFF	ON	ON
11	H	X	H	L	H	H	H	OFF	ON	ON	ON	OFF	ON	ON
12	H	X	H	H	L	L	H	OFF	ON	OFF	OFF	OFF	ON	ON
13	H	X	H	H	L	H	H	ON	OFF	ON	OFF	ON	ON	ON
14	H	X	H	H	H	L	H	OFF	OFF	OFF	ON	ON	ON	ON
15	H	X	H	H	H	H	H	OFF	OFF	OFF	OFF	OFF	OFF	ON
BI	X	X	X	X	X	X	L	OFF						
RBI	H	L	L	L	L	L	L	OFF						
LT	L	X	X	X	X	X	H	ON						

H = high level, L = low level, irrelevant

- NOTES:
- The blanking input ( $\overline{BI}$ ) must be open held at high logic level when output functions 0 through 15 are desired. The ripple-blanking input ( $\overline{RBI}$ ) must be open or high if blanking of a decimal zero is not desired.
  - When a low logic level is applied directly to the blanking input ( $\overline{BI}$ ), all segment outputs are off regardless of the level of any other inputs.
  - When ripple-blanking input ( $\overline{RBI}$ ) and inputs A, B, C, and D are at a low level with the lamp test input high, all segment outputs go off and the ripple-blanking input/ripple blanking output ( $\overline{BI/RBI}$ ) is open or held high and a low is applied to the lamp-test input, all segment outputs are on.

†  $\overline{BI/RBO}$  is wire AND logic serving as blanking input ( $\overline{BI}$ ) and/or ripple-blanking output ( $\overline{RBI}$ ).

## ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX OR MIN	TTL	LS	UNIT
I <sub>CC</sub>	MAX	103	13	mA
I <sub>OH</sub>	MAX	-0.2	-0.05	mA
I <sub>OL</sub>	MAX	8	3.2	mA

## TIMING REQUIREMENTS AND SWITCHING CHARACTERISTICS

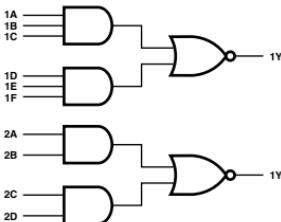
PARAMETER	INPUT	OUTPUT	MAX OR MIN	TTL	LS
t <sub>off</sub>	A	A to g	MAX	100	100
t <sub>on</sub>	A	A to g	MAX	100	100
t <sub>off</sub>	$\overline{RBI}$	A to g	MAX	100	100
t <sub>on</sub>	$\overline{RBI}$	A to g	MAX	100	100

UNIT: ns

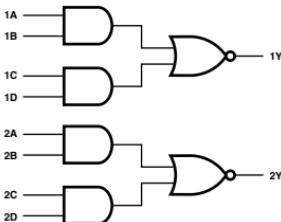
## AND-OR-INVERT GATES

- '51, 'S51:  $Y = \overline{AB + CD}$
- 'F51, 'LS51:  $1Y = (\overline{1A} \cdot \overline{1B} \cdot \overline{1C}) + (\overline{1D} \cdot \overline{1E} \cdot \overline{1F})$
- 'HC51:  $2Y = (2A \cdot 2B) + (2C \cdot 2D)$

LS51



S51



## ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	TTL	LS	S	F	SN74 HC	UNIT
I <sub>CC</sub>	MAX	14	2.8	22	7.5	0.08	mA
I <sub>OH</sub>	MAX	-0.4	-0.4	-1	-1	-4	mA
I <sub>OL</sub>	MAX	16	8	20	20	4	mA

## SWITCHING CHARACTERISTICS

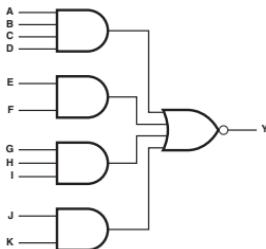
PARAMETER	INPUT	OUTPUT	MAX or MIN	TTL	LS	S	F	SN74 HC
t <sub>PLH</sub>	Any	Y	MAX	22	20	5.5	6.5	35
t <sub>PHL</sub>	Any	Y	MAX	15	20	5.5	4.5	35

UNIT: ns

## 4-2-3-2 INPUT AND-OR INVERT GATES

- Y =  $\overline{ABCD} + EF + GHI + JK$

Logic Diagram



ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	S	F	UNIT
I <sub>CC</sub>	MAX	16	4.7	mA
I <sub>OH</sub>	MAX	-1	-1	mA
I <sub>OL</sub>	MAX	20	20	mA

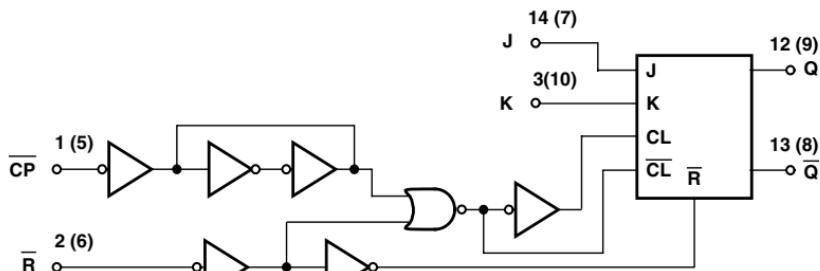
SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	S	F
t <sub>PLH</sub>	Any	Y	MAX	5.5	7
t <sub>PHL</sub>	Any	Y	MAX	5.5	5.5

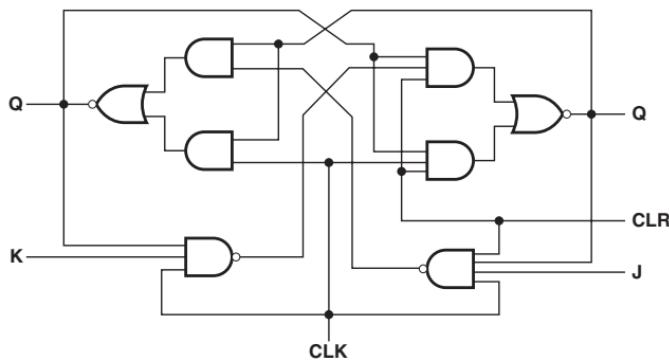
UNIT: ns

## DUAL J-K FLIP-FLOPS WITH CLEAR

Logic Diagram



CD74HC/HCT73



SN74LS73

FUNCTION TABLE (SN74)

INPUTS			OUTPUTS	
CLEAR	CLOCK	J K	Q	$\bar{Q}$
L	X	X X	L H	
H	↓	L L	$Q_0$	$\bar{Q}_0$
H	↓	H L	H L	
H	↓	L H	L H	
H	↓	H H	TOGGLE	
H	H	X X	$Q_0$	$\bar{Q}_0$

TRUTH TABLE (CD74)

INPUTS				OUTPUTS	
R	CP	J	K	Q	$\bar{Q}$
L	X	X	X	L	H
H	↓	L	L	No Change	
H	↓	H	L	H	L
H	↓	L	H	L	H
H	↓	H	H	Toggle	
H	H	X	X	No Change	

## NOTE:

H = High Level (Steady State)

L = Low Level (Steady State)

X = Irrelevant

↓ = High-to-Low Transition

## ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	TTL	LS	SN74 HC	CD74 HC	CD74 HCT	UNIT
I <sub>CC</sub>	MAX	20	6	0.04	0.08	0.08	mA
I <sub>OH</sub>	MAX	16	8	4	4	4	mA
I <sub>OL</sub>	MAX	-0.4	-0.4	-4	-4	-4	mA

## TIMING REQUIREMENTS AND SWITCHING CHARACTERISTICS

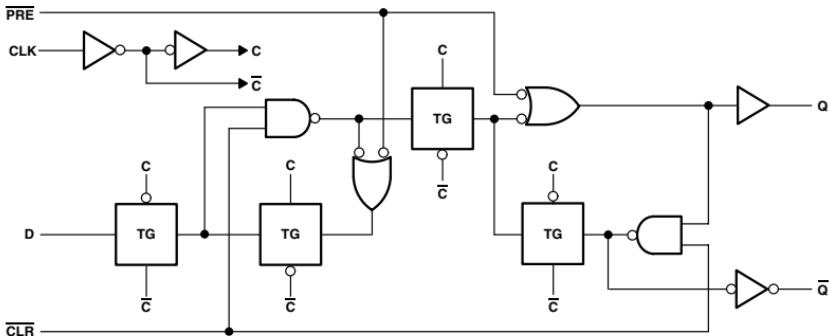
PARAMETER	INPUT	OUTPUT	MAX or MIN	TTL	LS	SN74 HC	CD74 HC	CD74 HCT
fmax			MIN	15	30	25	20	20
t <sub>w</sub>	CLOCK'L"			20	-	20	-	-
	CLOCK'H"		MIN	47	20	20	-	-
	$\bar{CP}$ Pulse Wide			-	-	-	24	24
	CLEAR 'L"			25	20	20	24	27
t <sub>su</sub>	CLK		MIN	0↑	20↓	25↓	-	-
	J.K to $\bar{CP}$			-	-	-	24	24
t <sub>th</sub>	CLK		MIN	0↓	0↓	0↓	-	-
	J.K to $\bar{CP}$			-	-	-	3	3
t <sub>PLH</sub>	CLEAR	$\bar{Q}$	MAX	25	20	39	44	51
t <sub>PLH</sub>				-	20	39	44	51
t <sub>PLH</sub>	CLEAR	Q	MAX	-	20	39	44	51
t <sub>PLH</sub>				40	20	39	44	51
t <sub>PLH</sub>	CLOCK	Q or $\bar{Q}$	MAX	25	20	32	-	-
t <sub>PLH</sub>				40	20	32	-	-
t <sub>PLH</sub>	$\bar{CP}$	Q	MAX	-	-	-	48	57
t <sub>PLH</sub>				-	-	-	48	57
t <sub>PLH</sub>	$\bar{CP}$	$\bar{Q}$	MAX	-	-	-	48	54
t <sub>PLH</sub>				-	-	-	48	54

UNIT fmax : MHz, other : ns

## DUAL D-TYPE POSITIVE-EDGE-TRIGGERED FLIP-FLOPS WITH CLEAR AND PRESET

- 74AC11xxx: Product Available in Reduced-Noise Advanced CMOS (11000 Series)
- 74ACT11xxx: Product Available in Reduced-Noise Advanced CMOS (11000 Series)

Logic Diagram (SN74)



FUNCTION TABLE (SN74)

INPUTS			OUTPUTS	
PRE	CLR	CLOCK	D	Q    Q̄
L	H	X	X	H   L
H	L	X	X	L   H
L	L	X	X	H*   H*
H	H	↑	H	H   L
H	H	↑	L	L   H
H	H	L	X	Q <sub>0</sub> Q̄ <sub>0</sub>

† This configuration is unstable; that is, it does not persist when PRE or CLR returns to its inactive (high) level.

## ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	TTL	LS	S	ALS	AS	F	SN74 HC	CD74 HC	SN74 HCT	CD74 HCT	AC 11	SN74 AC	UNIT
I <sub>CC</sub>	MAX	15	8	25	4	16	16	0.04	0.08	0.04	0.08	0.04	0.02	mA
I <sub>OH</sub>	MAX	-0.4	-0.4	-1	-0.4	-2	-1	-4	-4	-4	-4	-24	-24	mA
I <sub>OL</sub>	MAX	16	8	20	8	20	20	4	4	4	4	24	24	mA

PARAMETER	MAX or MIN	CD74 AC	ACT 11	SN74 ACT	CD74 ACT	AHC	AHCT	LV 3V	LV 5V	LVC 3V	AUC 1.8V	AUC 2.5V	UNIT
I <sub>CC</sub>	MAX	0.08	0.04	0.02	0.08	0.02	0.02	-	0.02	0.01	0.01	0.01	mA
I <sub>OH</sub>	MAX	-24	-24	-24	-24	-8	-8	-6	-12	-24	-8	-9	mA
I <sub>OL</sub>	MAX	24	24	24	24	8	8	6	12	24	8	9	mA

## TIMING REQUIREMENTS AND SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	TTL	LS	S	ALS	AS	F	SN74 HC	CD74 HC			
fmax				MIN	15	25	75	34	105	100	25	20		
				MIN	30	25	6	14.5	4	4	20	24		
				MIN	37	-	7.3	14.5	5.5	5	20	24		
				MIN	30	25	7	15	4	4	25	24		
				MIN	20	20	3	15	4.5	3	25	18		
				MIN	20	-	-	10	2	2	6	-		
tsu				MIN	5	5	2	0	0	1	0	3		
				PRE	Q or $\bar{Q}$	MAX	25	25	6	13	7.5	7.1	58	60
				PRE			40	40	13.5	15	10.5	10.5	58	60
				CLR	Q or $\bar{Q}$	MAX	25	25	6	13	7.5	7.1	58	60
				CLR			40	40	13.5	15	10.5	10.5	58	60
				CLOCK	Q or $\bar{Q}$	MAX	25	25	9	16	8	7.8	44	53
				CLOCK			40	40	9	18	9	9.2	44	53

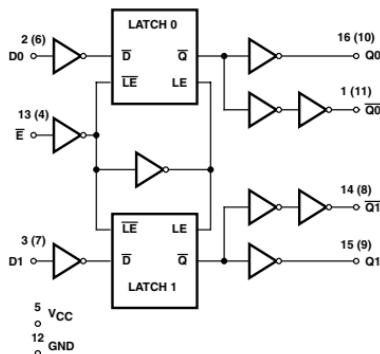
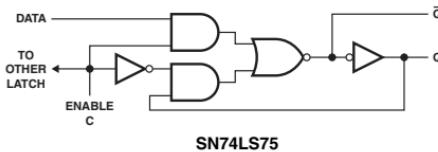
PARAMETER	INPUT	OUTPUT	MAX or MIN	SN74 HCT	CD74 HCT	AC 11	SN74 AC	CD74 AC	ACT 11	SN74 ACT	CD74 ACT			
fmax				MIN	22	16	125	125	110	100	125	85		
				MIN	23	27	4	5	4.5	5	6	5.7		
				MIN	23	27	4	5	4.5	5	6	5.7		
				MIN	20	24	4	5	4	5	6	5		
				MIN	15	18	3.5	3	3.5	4.5	3.5	4		
				MIN	0	-	1	0	-	2	0	-		
tsu				MIN	0	3	0	0.5	0	0	1	0		
				PRE	Q or $\bar{Q}$	MAX	44	60	7.1	10	10.5	9.6	10.5	11.5
				PRE			44	60	9	10.5	11.5	12.5	11.5	12.5
				CLR	Q or $\bar{Q}$	MAX	44	60	7.1	10	10.5	9.6	10.5	11.5
				CLR			44	60	9	10.5	11.5	12.5	11.5	12.5
				CLOCK	Q or $\bar{Q}$	MAX	35	53	8.2	10.5	10	9.4	13.0	9.5
				CLOCK			35	53	7.5	10.5	10	8.8	11.5	9.5

PARAMETER	INPUT	OUTPUT	MAX or MIN	AHC	AHCT	LV 3V	LV 5V	LVC 3V	AUC 1.8V	AUC 2.5V			
fmax				MIN	75	65	45	75	100	300	350		
				MIN	5	5	7	5	3.3	0.5	0.5		
				MIN	5	5	7	5	3.3	0.5	0.5		
				MIN	5	5	7	5	3.3	1.5	1.5		
				MIN	5	5	7	5	3	0.6	0.7		
				MIN	3	3.5	5	3	2	0.2	0.3		
tsu				MIN	0.5	0	0.5	0.5	0	0.3	0.3		
				PRE	Q or $\bar{Q}$	MAX	11	13	18	11	5.4	3.1	2.5
				PRE			11	13	18	11	5.4	3.1	2.5
				CLR	Q or $\bar{Q}$	MAX	11	13	18	11	5.4	3	2.4
				CLR			11	13	18	11	5.4	3	2.4
				CLOCK	Q or $\bar{Q}$	MAX	10.5	10	17.5	10.5	5.2	2.8	2.2
				CLOCK			10.5	10	17.5	10.5	5.2	2.8	2.2

UNIT fmax : MHz, other : ns

## 4-BIT BISTABLE LATCHES

Logic Diagram

FUNCTION TABLE  
(SN74)

INPUTS		OUTPUTS	
D	C	Q	Q̄
L	H	L	H
H	H	H	L
X	L	Q <sub>0</sub>	Q̄ <sub>0</sub>

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

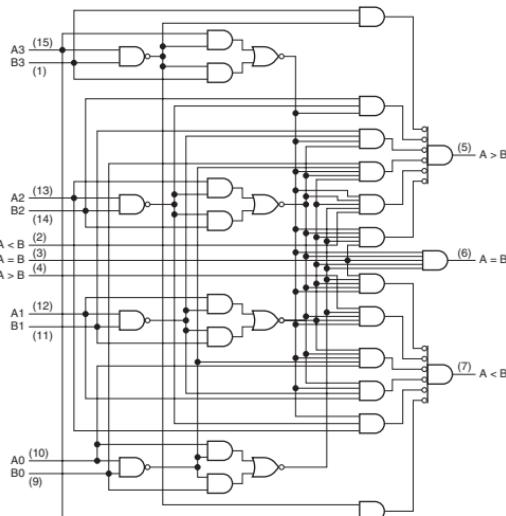
PARAMETER	MAX or MIN	TTL	LS	SN74 HC	CD74 HC	CD74 HCT	UNIT
I <sub>CC</sub>	MAX	53	12	0.04	0.08	0.08	mA
I <sub>OH</sub>	MAX	-0.4	-0.4	-4	-4	-4	mA
I <sub>OL</sub>	MAX	16	8	4	4	4	mA

TIMING REQUIREMENTS AND SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	TTL	LS	SN74 HC	CD74 HC	CD74 HCT
t <sub>w</sub>			MIN		20	20	20	24
			MIN		20	20	25	18
			MIN		5	5	5	3
t <sub>su</sub>		D	Q	MAX		30	27	30
				MAX		25	17	33
t <sub>th</sub>		D	Q̄	MAX		40	20	39
				MAX		15	15	39
t <sub>PLH</sub>	G	Q	MAX		30	27	33	42
			MAX		15	25	33	42
t <sub>PLH</sub>	G	Q̄	MAX		30	30	33	45
			MAX		15	15	39	45

UNIT: ns

## 4-BIT MAGNITUDE COMPARATORS



FUNCTION TABLE (SN74)

COMPARING INPUTS		CASCADING INPUTS		OUTPUTS			
A3, B3	A2, B2	A1, B1	A0, B0	A>B	A=B	A<B	A>B
A3>B3	X	X	X	X	X	H	L
A3>B3	X	X	X	X	X	L	L
A3>B3	A2>B2	X	X	X	X	H	L
A3>B3	A2>B2	X	X	X	X	L	L
A3>B3	A2>B2	A1>B1	X	X	X	H	L
A3>B3	A2>B2	A1>B1	X	X	X	L	H
A3>B3	A2>B2	A1>B1	A0=B0	X	X	H	L
A3>B3	A2>B2	A1>B1	A0=B0	X	X	L	L
A3>B3	A2>B2	A1>B1	A0=B0	H	L	H	L
A3>B3	A2>B2	A1>B1	A0=B0	L	H	L	H
A3>B3	A2>B2	A1>B1	A0=B0	H	H	L	L
A3>B3	A2>B2	A1>B1	A0=B0	L	L	H	H
A3>B3	A2>B2	A1>B1	A0=B0	X	X	L	H

## ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	TTL	LS	S	SN74 HC	CD74 HC	CD74 HCT	UNIT
Icc	MAX	88	20	115	0.08	0.16	0.16	mA
IoH	MAX	-0.4	-0.4	-1	-4	-4	-4	mA
IoL	MAX	16	8	20	4	4	4	mA

## SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	Number of Gate Levels	MAX or MIN	TTL	LS	S	SN74 HC	CD74 HC	CD74 HCT
t <sub>PLH</sub>	Any A or B data input	A < B, A > B	3	MAX	26	36	16	58	59	56
		A = B	4		35	45	18	50	53	60
t <sub>PHL</sub>	Any A or B data input	A < B, A > B	3	MAX	30	30	16.5	58	59	56
		A = B	4		30	45	16.5	50	53	60
t <sub>PLH</sub>	A < B, A = B	A > B	1	MAX	11	22	7.5	44	42	45
t <sub>PHL</sub>	A < B, A = B	A > B	1		17	17	8.5	44	42	45
t <sub>PLH</sub>	A = B	A = B	2	MAX	20	20	10.5	37	-	-
t <sub>PHL</sub>	A = B	A = B	2		17	26	7.5	37	-	-
t <sub>PLH</sub>	A > B, A = B	A < B	1	MAX	11	22	7.5	44	42	45
t <sub>PHL</sub>	A > B, A = B	A < B	1		17	17	8.5	44	42	45

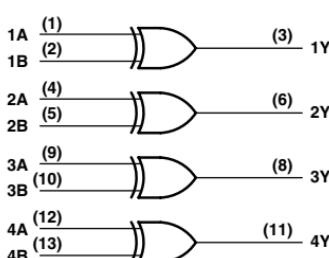
UNIT: ns

## QUADRUPLE 2-INPUT EXCLUSIVE-OR GATES

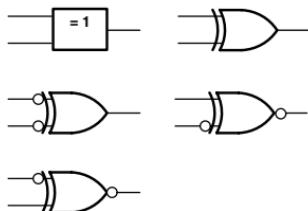
- $Y = A \oplus B$  or  $Y = \bar{A}B + \bar{A}\bar{B}$
- 74AC11xxx : Product Available in Reduced-Noise Advanced CMOS (11000 Series)
- 74ACT11xxx: Product Available in Reduced-Noise Advanced CMOS (11000 Series)

An exclusive-OR gate has many applications, some of which can be represented better by alternative logic symbols.

Logic Diagram (SN74)



Exclusive OR



## ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	TTL	LS	S	ALS	AS	F	SN74 HC	CD74 HC	CD74 HCT	AC 11	SN74 AC	CD74 AC	ACT 11	UNIT
$I_{CC}$	MAX	50	10	75	5.9	38	28	0.02	0.04	0.04	0.04	0.02	0.08	0.04	mA
$I_{OH}$	MAX	16	8	20	8	20	20	4	4	4	24	24	24	24	mA
$I_{OL}$	MAX	-0.8	-0.4	-1	-0.4	-2	-1	-4	-4	-4	-24	-24	-24	-24	mA

PARAMETER	MAX or MIN	SN74 ACT	CD74 ACT	AHC	AHCT	LV 3V	LV 5V	LVC 3V	UNIT
$I_{CC}$	MAX	0.04	0.08	0.02	0.02	-	0.02	0.01	mA
$I_{OH}$	MAX	24	24	-10	8	6	12	24	mA
$I_{OL}$	MAX	-24	-24	10	-8	-6	-12	-24	mA

## SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	TTL	LS	S	ALS	AS	F	SN74 HC	CD74 HC	CD74 HCT	AC 11
$t_{PLH}$ Input Low	A or B	Y	MAX	23	23	10.5	17	7.5	6.5	25	36	48	7.6
$t_{PHL}$ Input Low		Y	MAX	17	17	10	12	6.5	6.5	25	36	48	6.8
$t_{PLH}$ Input High	A or B	Y	MAX	30	30	10.5	17	6.5	8	25	36	48	7.6
$t_{PHL}$ Input High		Y	MAX	22	22	10	10	7	7.5	25	36	48	6.8

PARAMETER	INPUT	OUTPUT	MAX or MIN	SN74 AC	CD74 AC	ACT 11	SN74 ACT	CD74 ACT	AHC	AHCT	LV 3V	LV 5V	LVC 3V
$t_{PLH}$ Input Low	A or B	Y	MAX	9	10.8	9.6	10	14.6	10	10	16.5	10	4.6
$t_{PHL}$ Input Low		Y	MAX	9.5	10.8	9	10.5	14.6	10	10	16.5	10	4.6
$t_{PLH}$ Input High	A or B	Y	MAX	9	10.8	9.6	10	14.6	10	10	16.5	10	4.6
$t_{PHL}$ Input High		Y	MAX	9.5	10.8	9	10.5	14.6	10	10	16.5	10	4.6

UNIT: ns

90

## DECADE COUNTER

FUNCTION TABLE

BCD COUNT SEQUENCE

Count	OUTPUTS			
	$Q_D$	$Q_C$	$Q_B$	$Q_A$
0	L	L	L	L
1	L	L	H	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	H	H
6	L	H	H	L
7	L	H	H	H
8	H	L	L	L
9	H	L	L	H

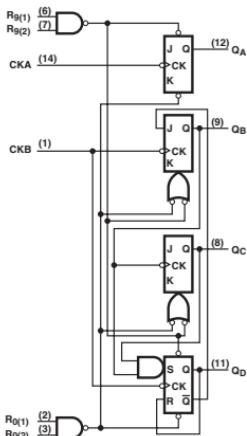
BI-QUINARY

Count	OUTPUTS			
	$Q_A$	$Q_D$	$Q_C$	$Q_B$
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	H	L	L	L
6	H	L	L	H
7	H	L	H	L
8	H	L	H	H
9	H	H	L	L

RESET/COUNT

RESET INPUTS			OUTPUTS				
$R_{0(1)}$	$R_{0(2)}$	$R_{9(1)}$	$R_{9(2)}$	$Q_D$	$Q_C$	$Q_B$	$Q_A$
H	H	L	X	L	L	L	L
H	H	X	L	L	L	L	H
X	X	H	H	H	L	L	H
X	L	X	L	Count			
L	X	L	X	Count			
L	X	X	L	Count			
X	L	L	X	Count			

## Logic Diagram



ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	TTL	LS	UNIT
$I_{CC}$	MAX	39	15	mA
$I_{OH}$	MAX	-0.8	-0.4	mA
$I_{OL}$	MAX	16	8	mA

TIMING REQUIREMENTS AND SWITCHING CHARACTERISTICS

PARAMETER		INPUT	OUTPUT	MAX or MIN	TTL	LS
$f_{max}$		A	QA	MIN	32	32
		B	QB		16	16
$t_w$	A			MIN	15	15
	B				30	30
	RESET				15	30
$t_{su}$	RESET INACTIVE			MIN	25	25
$t_{PLH}$	A	QA	MAX	MAX	16	16
					18	18
$t_{PHL}$	A	QD	MAX	MAX	48	48
					50	50
$t_{PLH}$	B	QB	MAX	MAX	16	16
					21	21
$t_{PLH}$	B	QC	MAX	MAX	32	32
					35	35
$t_{PLH}$	B	QC	MAX	MAX	32	32
					35	35
$t_{PHL}$	Set to 0	Any	MAX	MAX	40	40
					30	30
$t_{PLH}$	Set to 9	QA, QD	MAX	MAX	40	40
					OB, QC	

UNIT  $f_{max}$  : MHz, other : ns

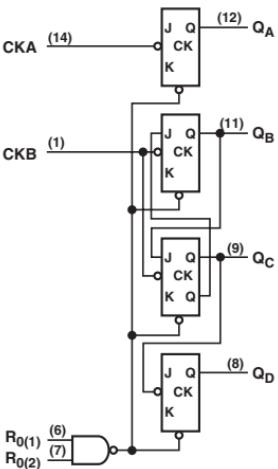
## DIVIDE-BY-TWELVE DECODE COUNTERS

FUNCTION TABLE  
COUNT SEQUENCE

COUNT	OUTPUTS			
	Q <sub>D</sub>	Q <sub>C</sub>	Q <sub>B</sub>	Q <sub>A</sub>
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	H	L	L	L
7	H	L	L	H
8	H	L	H	L
9	H	L	H	H
10	H	H	L	L
11	H	H	L	H

RESET/COUNT

RESET INPUTS	OUTPUTS
R <sub>0(1)</sub> R <sub>0(2)</sub>	Q <sub>D</sub> Q <sub>C</sub> Q <sub>B</sub> Q <sub>A</sub>
H H	L L L L
L X	COUNT
X L	COUNT



ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	TTL	LS	UNIT
I <sub>CC</sub>	MAX	39	15	mA
I <sub>OH</sub>	MAX	-0.8	-0.4	mA
I <sub>OL</sub>	MAX	16	8	mA

TIMING REQUIREMENTS AND SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	TTL	LS
f <sub>max</sub>	A	Q <sub>A</sub>	MIN	32	32
	B	Q <sub>B</sub>		16	16
t <sub>W</sub>	A		MIN	15	15
	B			30	30
	RESET			15	30
t <sub>SU</sub>	RESET INACTIVE		MIN	25	25
t <sub>PLH</sub>	A	Q <sub>A</sub>	MAX	16	16
t <sub>PHL</sub>				18	18
t <sub>PLH</sub>	A	Q <sub>D</sub>	MAX	48	48
t <sub>PHL</sub>				50	50
t <sub>PLH</sub>	B	Q <sub>B</sub>	MAX	16	16
t <sub>PHL</sub>				21	21
t <sub>PLH</sub>	B	Q <sub>C</sub>	MAX	16	16
t <sub>PHL</sub>				21	21
t <sub>PLH</sub>	B	Q <sub>D</sub>	MAX	32	32
t <sub>PHL</sub>				35	35
t <sub>PLH</sub>	Set to 0		MAX	40	40

UNIT f<sub>max</sub> : MHz, other : ns

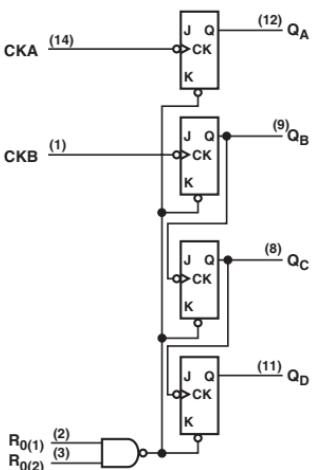
## 4-BIT BINARY COUNTERS

FUNCTION TABLE (SN74)  
COUNT SEQUENCE

COUNT	OUTPUTS			
	Q <sub>D</sub>	Q <sub>C</sub>	Q <sub>B</sub>	Q <sub>A</sub>
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	L	H	H	L
7	L	H	H	H
8	H	L	L	L
9	H	L	L	H
10	H	L	H	L
11	H	L	H	H
12	H	H	L	L
13	H	H	L	H
14	H	H	H	L
15	H	H	H	H

RESET/COUNT

RESET INPUTS	OUTPUTS					
	R <sub>0(1)</sub>	R <sub>0(2)</sub>	Q <sub>D</sub>	Q <sub>C</sub>	Q <sub>B</sub>	Q <sub>A</sub>
H H			L	L	L	L
L X			COUNT			
X L			COUNT			



ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	TTL	LS	CD74 HC	CD74 HCT	UNIT
I <sub>CC</sub>	MAX	39	15	0.16	0.16	mA
I <sub>OH</sub>	MAX	-0.8	-0.4	-4	-4	mA
I <sub>OL</sub>	MAX	16	8	4	4	mA

TIMING REQUIREMENTS AND SWITCHING CHARACTERISTICS

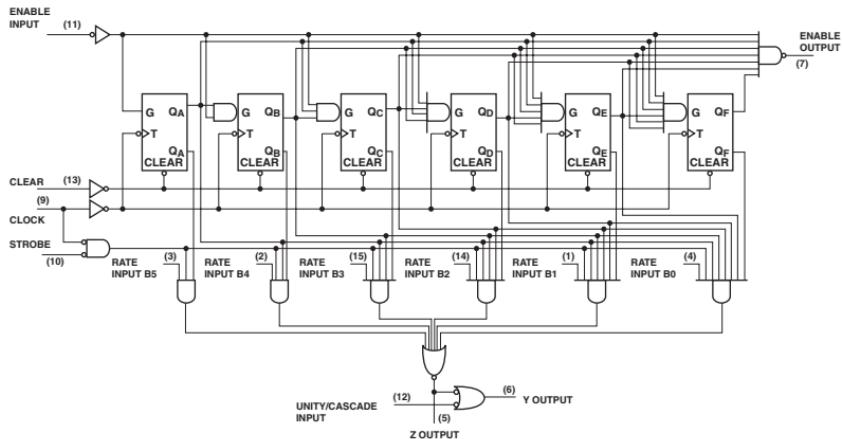
PARAMETER	INPUT	OUTPUT	MAX or MIN	TTL	LS	CD74 HC	CD74 HCT
fmax	A (CD74:CP0)	QA (CD74:Q <sub>0</sub> )	MIN	32	32	20	20
	B (CD74:CP1)	QB (CD74:Q <sub>1</sub> )		16	16	20	20
tw	A (CP0)		MIN	15	15	24	24
	B (CP1)			30	30	24	24
	RESET			15	30	24	24
tsu	RESET INACTIVE		MIN	25	25	-	-
tPHL	CKA (CP0)	QA (Q <sub>0</sub> )	MAX	16	16	38	51
	(CP1)			18	18	38	51
tPLH	CKA (CP0)	QD (Q <sub>3</sub> )	MAX	70	70	-	-
	(CP1)			70	70	-	-
tPLH	CKB (CP0)	QB (Q <sub>1</sub> )	MAX	16	16	41	51
	(CP1)			21	21	41	51
tPLH	CKB (CP1)	QC (Q <sub>2</sub> )	MAX	32	32	56	69
	(CP0)			35	35	56	69
tPLH	CKB (CP0)	QD (Q <sub>3</sub> )	MAX	51	51	74	87
	(CP1)			51	51	74	87
tPHL	Set to 0	ANY	MAX	40	40	-	-

UNIT fmax : MHz, other : ns

## SYNCHRONOUS 6-BIT BINARY RATE MULTIPLIERS

- Perform Fixed-Rate or Variable-Rate Frequency Division
- Typical Maximum Clock Frequency: 32MHz

**Logic Diagram**



FUNCTION TABLE

			INPUTS					OUTPUTS				
CLEAR	ENABLE	STROBE	BINARY RATE		NUMBER OF CLOCK PULSES	UNITY/ CASCADE	LOGI LEVEL OR NUMBER OF PULSES					
			B <sub>5</sub>	B <sub>4</sub>			B <sub>3</sub>	B <sub>2</sub>	B <sub>1</sub>	B <sub>0</sub>	Y	Z
H	X	H	X	X	X	X	X	X	X	X	H	L
L	L	L	L	L	L	L	L	L	L	L	H	H
L	L	L	L	L	L	L	L	L	L	L	H	1
L	L	L	L	L	L	L	L	L	L	L	H	2
L	L	L	L	L	L	L	L	L	L	L	H	4
L	L	L	L	L	L	L	L	L	L	L	H	8
L	L	L	L	L	L	L	L	L	L	L	H	16
L	L	L	L	L	L	L	L	L	L	L	H	32
L	L	L	L	L	L	L	L	L	L	L	H	63
L	L	L	L	L	L	L	L	L	L	L	H	63
L	L	L	H	H	H	H	H	H	H	H	L	63
L	L	L	H	L	H	L	L	L	L	L	H	1
L	L	L	H	L	H	L	L	L	L	L	H	40
L	L	L	H	L	H	L	L	L	L	L	H	1

## ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	TTL	UNIT
I <sub>CC</sub>	MAX	120	mA
I <sub>OL</sub>	MAX	16	mA
I <sub>OL</sub>	MAX	-0.4	mA

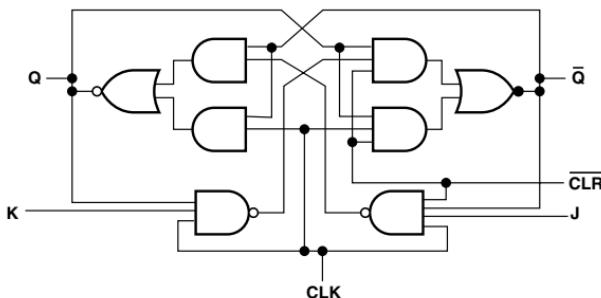
## TIMING REQUIREMENTS AND SWITCHING CHARACTERISTICS

PARAMETER		INPUT	OUTPUT	MAX or MIN	TTL
fmax		A	QA	MIN	25
tw	CLK			MIN	20
	CLR			MIN	15
tsu	Positive			MIN	25
	Negative			MIN	0
th	Positive			MIN	0
	Negative			MIN	20
tPLH		ENABLE	ENABLE	MAX	20
tPHL				MAX	21
tPLH		STRB	Z	MAX	18
tPHL				MAX	23
tPLH		CLK	Y	MAX	39
tPHL				MAX	30
tPLH		CLK	Z	MAX	18
tPHL				MAX	26
tPLH		RATE	Z	MAX	10
tPHL				MAX	14
tPLH		UNITY/CAS	Y	MAX	14
tPHL				MAX	10
tPLH		STRB	Y	MAX	30
tPHL				MAX	33
tPLH		CLK	ENABLE	MAX	30
tPHL				MAX	33
tPLH		CLR	Y	MAX	36
tPHL			Z	MAX	23
tPLH		RATE	Y	MAX	23
tPHL				MAX	23

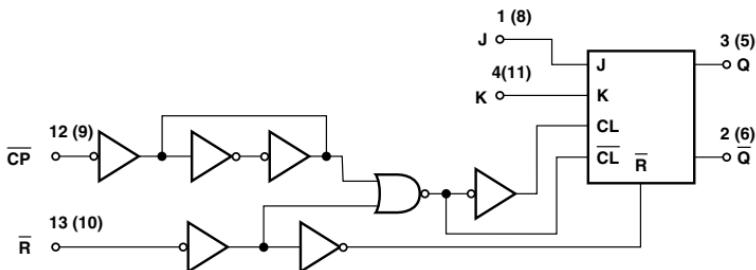
UNIT fmax : MHz, other : ns

## DUAL J-K FLIP-FLOPS WITH CLEAR

Logic Diagram  
SN74LS



Logic Diagram  
CD74HC/HCT



**FUNCTION TABLES  
(SN74LS107A)**

INPUTS				OUTPUTS	
CLR	CLK	J	K	Q	$\bar{Q}$
L	X	X	X	L	H
H	↓	L	L	$\bar{Q}_0$	$\bar{Q}_0$
H	↓	H	L	H	L
H	↓	L	H	L	H
H	↓	H	H	TOGGLE	
H	H	X	X	$\bar{Q}_0$	$\bar{Q}_0$

**ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS**

PARAMETER	MAX or MIN	TTL	LS	SN74 HC	CD74 HC	CD74 HCT	UNIT
I <sub>CC</sub>	MAX	20	6	0.04	0.08	0.08	mA
I <sub>OH</sub>	MAX	-0.4	-0.4	-4	-4	-4	mA
IOL	MAX	16	8	4	4	4	mA

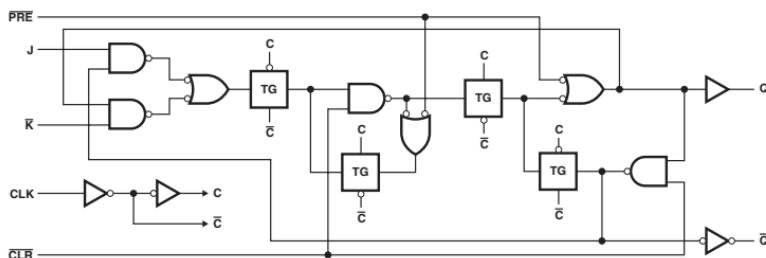
**TIMING REQUIREMENTS AND SWITCHING CHARACTERISTICS**

PARAMETER		INPUT	OUTPUT	MAX or MIN	TTL	LS	SN74 HC	CD74 HC	CD74 HCT
fmax				MIN	15	30	25	20	19
tw	CLK H			MIN	20	20	20	-	-
	CLK L			MIN	47	-	20	-	-
	$\bar{CP}$			MIN	-	-	-	24	27
	CLR L (or $\bar{R}$ )			MIN	25	25	20	24	36
	J, K			MIN	0	20	25	30	30
	CLR INACTIVE			MIN	0	25	25	-	-
th				MIN	0	0	0	3	5
I <sub>PLH</sub>	CLR (or $\bar{R}$ )		$\bar{Q}$	MAX	25	20	39	47	57
			Q	MAX	40	20	39	47	57
I <sub>PLH</sub>	CLK		$\bar{Q}$	MAX	25	20	32	-	-
			Q	MAX	40	20	32	-	-
I <sub>PLH</sub>	$\bar{CP}$		Q	MAX	-	-	-	51	65
			Q	MAX	-	-	-	51	65
I <sub>PLH</sub>	$CP$		$\bar{Q}$	MAX	-	-	-	51	60
			Q	MAX	-	-	-	51	60

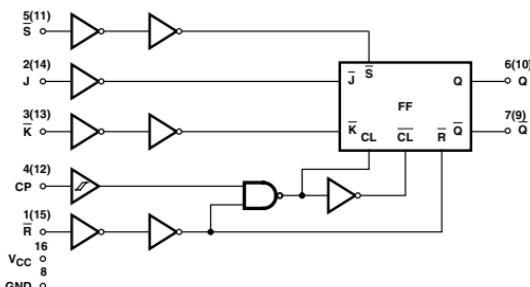
UNIT fmax : MHz, other : ns

## DUAL J-K POSITIVE-EDGE-TRIGGERED FLIP-FLOPS WITH CLEAR AND PRESET

**Logic Diagram  
SN74, CD74AC/ACT**



**Logic Diagram  
CD74HC/HCT**



**FUNCTION TABLE  
(SN74, CD74AC/ACT)**

INPUTS				OUTPUTS	
PRE	CLR	CLOCK	J K	Q	$\bar{Q}$
L	H	X	X X	H	L
H	L	X	X X	L	H
L	L	X	X X	H <sup>†</sup>	H <sup>†</sup>
H	H	↑	L L	L	H
H	H	↑	H L	TOGGLE	
H	H	↑	L H	Q <sub>0</sub>	$\bar{Q}_0$
H	H	↑	H H	H	L
H	H	L	X X	Q <sub>0</sub>	$\bar{Q}_0$

† The output levels in this configuration are not guaranteed to meet the minimum levels for  $V_{OH}$ . Furthermore, this configuration is nonstable; that is, it will not persist when either PRE or CLR returns to its inactive (high) level.

## ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	TTL	LS	ALS	AS	F	SN74 HC	CD74 HC	CD74 HCT	CD74 AC	CD74 ACT	UNIT
I <sub>CC</sub>	MAX	15	8	4	17	17	0.04	0.08	0.08	0.08	0.08	mA
I <sub>OH</sub>	MAX	-0.8	-0.4	-0.4	-2	-1	-4	-4	-4	-24	-24	mA
I <sub>OL</sub>	MAX	16	4	8	20	20	4	4	4	24	24	mA

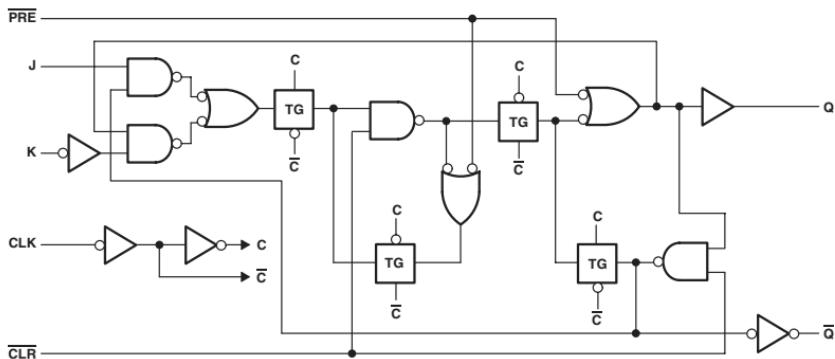
## TIMING REQUIREMENTS AND SWITCHING CHARACTERISTICS

PARAMETER		INPUT	OUTPUT	MAX or MIN	TTL	LS	ALS	AS	F	SN74 HC	CD74 HC	CD74 HCT
fmax				MIN	25	25	34	105	90	25	20	18
tw	CLK H			MIN	20	25	14.5	4	4	20	-	-
	CLK L			MIN	20	-	14.5	5.5	5	20	-	-
	CP			MIN	-	-	-	-	-	24	27	-
	PRE L			MIN	20	25	15	4	4	25	-	-
	CLR L			MIN	20	25	15	4	4	25	-	-
	R			MIN	-	-	-	-	-	24	27	-
	J, K			MIN	10	25	15	5.5	3	25	-	-
tsu	PRE, CLR			MIN	10	-	10	2	2	6	-	-
	J, K to CP			MIN	-	-	-	-	-	24	27	-
	th			MIN	6	5	0	0	1	0	3	3
tphl	PRE		Q	MAX	15	25	13	8	8	58	-	-
			Q̄	MAX	35	40	15	10.5	10.5	58	-	-
	CLR		Q̄	MAX	15	25	13	8	8	58	-	-
			Q	MAX	25	40	15	10.5	10.5	58	-	-
	CLK		Q̄, Q	MAX	16	25	16	9	8	44	-	-
			Q	MAX	28	40	18	9	9.2	44	-	-
	CP		Q	MAX	-	-	-	-	-	53	60	-
			Q̄	MAX	-	-	-	-	-	53	60	-
	CP		Q	MAX	-	-	-	-	-	53	60	-
			Q̄	MAX	-	-	-	-	-	53	60	-
	R		Q	MAX	-	-	-	-	-	56	68	-
			Q̄	MAX	-	-	-	-	-	56	68	-
	R̄		Q	MAX	-	-	-	-	-	51	56	-
			Q̄	MAX	-	-	-	-	-	51	56	-

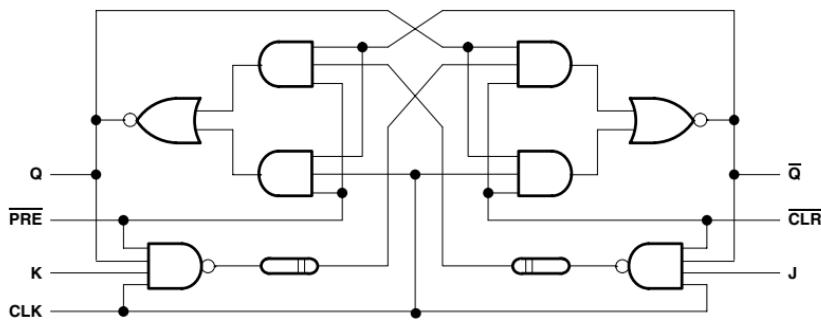
PARAMETER		INPUT	OUTPUT	MAX or MIN	CD74 AC	CD74 ACT
fmax				MIN	100	100
tw	CLK H			MIN	5	5
	CLK L			MIN	5	5
	CP			MIN	-	-
	PRE L			MIN	4.5	5.5
	CLR L			MIN	4.5	5.5
	R			MIN	-	-
	J, K			MIN	5.5	5.5
tsu	PRE, CLR			MIN	-	5.5
	J, K to CP			MIN	-	-
	th			MIN	0	0
tphl	PRE		Q	MAX	12.2	12.2
			Q̄	MAX	12.2	12.2
	CLR		Q̄	MAX	12.2	12.2
			Q	MAX	12.2	12.2
	CLK		Q̄, Q	MAX	10.3	10.3
			Q	MAX	10.3	10.3
	CP		Q	MAX	-	-
			Q̄	MAX	-	-
	CP		Q	MAX	-	-
			Q̄	MAX	-	-
	R		Q	MAX	-	-
			Q̄	MAX	-	-
	R̄		Q	MAX	-	-
			Q̄	MAX	-	-

UNIT fmax : MHz, other : ns

Logic Diagram (SN74HC112)



Logic Diagram (SN74LVC112A)



**FUNCTION TABLE (SN74)**

INPUTS					OUTPUTS	
PRE	CLR	CLK	J	K	Q	$\bar{Q}$
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H†	H†
H	H	↓	L	L	Q <sub>0</sub>	$\bar{Q}_0$
H	H	↓	H	L	H	L
H	H	↓	L	H	L	H
H	H	↓	H	H	Toggle	
H	H	H	X	X	Q <sub>0</sub>	$\bar{Q}_0$

†The output levels in this configuration may not meet the minimum levels for  $V_{QH}$ . Furthermore, this configuration is nonstable; that is, it does not persist when either PRE or CLR returns to its inactive (high) level.

**ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS**

PARAMETER	MAX or MIN	LS	S	ALS	F	SN74 HC	CD74 HC	CD74 HCT	CD74 AC	CD74 ACT	LVC 3V	UNIT
I <sub>CC</sub>	MAX	6	25	4.5	19	0.04	0.08	0.08	0.08	0.08	0.01	mA
I <sub>OH</sub>	MAX	-0.4	-1	-0.4	-1	-4	-4	-4	-24	-24	-24	mA
I <sub>OL</sub>	MAX	8	20	8	20	4	4	4	24	24	24	mA

**TIMING REQUIREMENTS AND SWITCHING CHARACTERISTICS**

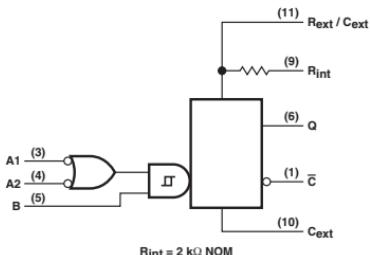
PARAMETER	INPUT	OUTPUT	MAX or MIN	LS	S	ALS	F	SN74 HC	CD74 HC	CD74 HCT	CD74 AC	CD74 ACT	LVC 3V
				MIN	30	80	30	100	20	20	20	100	150
fmax	t <sub>w</sub>		MIN	25	8	10	5	25	24	27	4.5	4.5	-
			MIN	20	6	16.5	5	25	-	-	4.5	4.5	3.3
			MIN	-	6.5	16.5	5	25	-	-	4.5	4.5	3.3
			MIN	-	-	-	-	-	24	30	-	-	-
tsu	t <sub>su</sub>		MIN	20	7	22	5	25	24	24	4	4	2.3
			MIN	25	-	20	5	25	-	-	-	-	1.1
			MIN	20	-	20	5	25	-	-	-	-	1.1
			MIN	0	0	0	0	0	0	3	0	0	0.7
t <sub>th</sub>	t <sub>PLH</sub>	<u>PRE</u> or <u>CLR</u>	Q or $\bar{Q}$	MAX	20	7	15	7.5	41	-	-	10.3	10.3
			Q or $\bar{Q}$	MAX	20	7	18	7.5	41	-	-	12.2	12.2
		CLK	Q or $\bar{Q}$	MAX	20	7	15	7.5	31	-	-	10.3	10.3
			Q or $\bar{Q}$	MAX	20	7	19	7.5	31	-	-	12.2	12.2
t <sub>PLH</sub>	t <sub>PHL</sub>	<u>CP</u>	Q or $\bar{Q}$	MAX	-	-	-	-	-	53	53	-	-
			Q or $\bar{Q}$	MAX	-	-	-	-	-	53	53	-	-
		<u>S</u>	Q or $\bar{Q}$	MAX	-	-	-	-	-	47	48	-	-
			Q or $\bar{Q}$	MAX	-	-	-	-	-	47	48	-	-
t <sub>PLH</sub>	t <sub>PHL</sub>	<u>R</u>	Q or $\bar{Q}$	MAX	-	-	-	-	-	54	56	-	-
			Q or $\bar{Q}$	MAX	-	-	-	-	-	54	56	-	-

UNIT fmax : MHz, other : ns

## MONOSTABLE MULTIVIBRATORS WITH SCHMITT-TRIGGER INPUTS

- Internal Timing Resistors ( $2k\Omega$ )
- Programmable Output Pulse Width with  $R_{ext}/C_{ext}$ : 40ns to 28s

Logic Diagram



NOTES: 1. An external capacitor may be connected between  $C_{ext}$  (positive) and  $R_{ext}/C_{ext}$ .  
 2. To use the internal timing resistor, connect  $R_{int}$  to  $V_{CC}$ . For improved pulse width accuracy and repeatability, connect an external resistor between  $R_{ext}/C_{ext}$  and  $V_{CC}$  with  $R_{int}$  open-circuited.

FUNCTION TABLE

INPUTS				
A1	A2	B	Q	$\bar{Q}$
L	X	H	L	H
X	L	H	L <sup>†</sup>	H <sup>†</sup>
X	X	L	L <sup>†</sup>	H <sup>†</sup>
H	H	X	L <sup>†</sup>	H <sup>†</sup>
H	↓	H	square wave	square wave
↓	H	H	square wave	square wave
L	X	T	square wave	square wave
X	L	↑	square wave	square wave

See explanation of function table on page

<sup>†</sup> These lines of the functional tables assume that the indicated steady-state conditions at the A and B inputs have been set up long enough to complete any pulse started before the set up.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	TTL	UNIT
$I_{CC}$	MAX	40	mA
$I_{OH}$	MAX	-0.4	mA
$I_{OL}$	MAX	16	mA

TIMING REQUIREMENTS AND SWITCHING CHARACTERISTICS

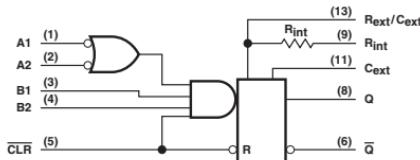
PARAMETER	INPUT	OUTPUT	MAX or MIN	TTL
$t_{W(out)}$	Pulse width obtained with zero timing capacitance		MIN	50
$t_{PLH}$	A B	Q	MAX	70
$t_{PHL}$				80
$t_{PLH}$	A B	$\bar{Q}$	MAX	55
$t_{PHL}$				65

UNIT: NS

## RETRIGGERABLE MONOSTABLE MULTIVIBRATORS

- Retriggerable for Very Long Output Pulse, Up to 100% Duty Cycle
- Internal Timing Resistors ( $5\text{k}\Omega$ )

Logic Diagram



$R_{int}$  is nominally  $10\text{k}\Omega$  for '122 and 'LS122

FUNCTION TABLE

CLEAR	INPUTS				OUTPUTS	
	A1	A2	B	B2	Q	$\bar{Q}$
L	X	X	X	X	L	H
X	H	H	X	X	L↑	H↑
X	X	X	L	X	L↑	H↑
X	X	X	X	L	L↑	H↑
H	L	X	↑	H	[Pulse]	[Pulse]
H	L	X	H	↑	[Pulse]	[Pulse]
H	X	L	↑	H	[Pulse]	[Pulse]
H	X	L	H	↑	[Pulse]	[Pulse]
H	H	↓	H	H	[Pulse]	[Pulse]
H	↓	↓	H	H	[Pulse]	[Pulse]
H	↓	H	H	H	[Pulse]	[Pulse]
↑	L	X	H	H	[Pulse]	[Pulse]
X	L	H	H	H	[Pulse]	[Pulse]

See explanation of function table on page

† These lines of the functional tables assume that the indicated steady-state conditions at the A and B inputs have been set up long enough to complete any pulse started before the set up.

## ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	TTL	LS	UNIT
$I_{CC}$	MAX	66	11	mA
$I_{OH}$	MAX	-0.8	-0.4	mA
$I_{OL}$	MAX	16	8	mA

## TIMING REQUIREMENTS AND SWITCHING CHARACTERISTICS

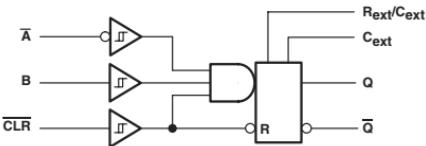
PARAMETER	INPUT	OUTPUT	MAX or MIN	TTL	LS
$t_{W}$			MIN	40	40
$t_{PLH}$	A	Q	MAX	33	33
	B			28	44
$t_{PHL}$	A	$\bar{Q}$	MAX	40	45
	B			36	56
$t_{PLH}$	CLEAR	Q	MAX	27	27
$t_{PHL}$		$\bar{Q}$		40	45

UNIT: NS

## DUAL RETRIGGERABLE MONOSTABLE MULTIVIBRATORS WITH SCHMITT-TRIGGER INPUTS

- Retriggerable for Very Long Output Pulse, Up to 100% Duty Cycle

**Logic Diagram (SN74)**



**FUNCTION TABLE (SN74)**

INPUTS			OUTPUTS	
CLEAR	A (A)	B	Q	$\bar{Q}$
L	X	X	L	H
X	H	X	L <sup>†</sup>	H <sup>†</sup>
X	X	L	L <sup>†</sup>	H <sup>†</sup>
H	L	↑	—	—
H	↓	H	—	—
1	L	H	—	—

See explanation of function table on page

<sup>†</sup> These lines of the functional tables assume that the indicated steady-state conditions at the A and B inputs have been set up long enough to complete any pulse started before the set up.

### ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	TTL	LS	CD74	CD74	AHC	AHCT	LV	LV	UNIT
		HC		HCT				3V	5V	
I <sub>CC</sub>	MAX	66	20	0.16	0.16	0.65	0.975	0.28	0.65	mA
I <sub>OH</sub>	MAX	-0.8	-0.4	-4	-4	-8	-8	-6	-12	mA
I <sub>OL</sub>	MAX	16	8	4	4	8	8	6	12	mA

### TIMING REQUIREMENTS AND SWITCHING CHARACTERISTICS

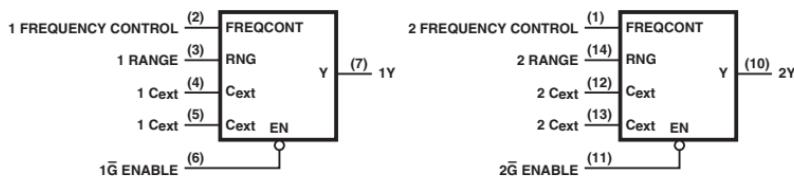
PARAMETER	INPUT	OUTPUT	MAX or MIN	TTL	LS	CD74	CD74	AHC	AHCT	LV	LV
				HC		HCT				3V	5V
t <sub>w</sub>	$\bar{A}$ (A)	Q	MIN	40	40	30	30	5	5	5	5
				33	33	90	90	16	12	27.5	16
t <sub>PLH</sub>	B	Q	MAX	28	44	90	90	16	12	27.5	16
				40	45	96	102	16	12	27.5	16
t <sub>PHL</sub>	$\bar{A}$ (A)	$\bar{Q}$	MAX	36	56	96	102	16	12	27.5	16
				40	45	65	72	13	14	22	13
t <sub>PLH</sub>	B	$\bar{Q}$	MAX	27	27	65	72	13	14	22	13
				40	45	65	72	13	14	22	13

UNIT: NS

## DUAL VOLTAGE-CONTROLLED OSCILLATORS

- Frequency Spectrum: 1Hz to 60MHz
- Typical fmax: 85MHz
- Typical Power Dissipation: 525mW

Block Diagram



## ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	S	UNIT
I <sub>CC</sub>	MAX	150	mA
I <sub>OL</sub>	MAX	-1	mA
I <sub>OL</sub>	MAX	20	mA

## TIMING REQUIREMENTS AND SWITCHING CHARACTERISTICS

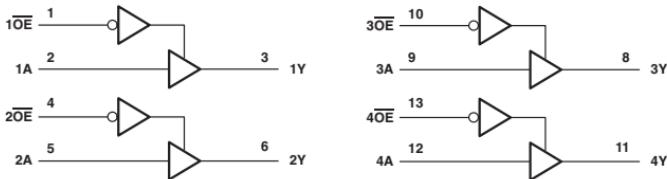
PARAMETER	MAX or MIN	S
f <sub>0</sub>	MIN	60

UNIT: NS

## QUADRUPLE BUS BUFFER GATES WITH 3-STATE OUTPUTS

● Y = A

Logic Diagram (SN74)

FUNCTION TABLE  
(SN74)  
(each buffer)

INPUTS	OUTPUT	
$\overline{OE}$	A	Y
L	H	H
L	L	L
H	X	Z

## ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	TTL	LS	F	SN74 HC	CD74 HC	SN74 HCT	CD74 HCT	SN74 BCT	SN64 BCT	ABT	UNIT
$I_{CC}$	MAX	54	20	40	0.08	0.16	0.08	0.16	49	49	30	mA
$I_{OH}$	MAX	-5.2	-2.6	-15	-6	-6	-6	-6	-15	-15	-32	mA
$I_{OL}$	MAX	16	24	64	6	6	6	6	64	64	60	mA

PARAMETER	MAX or MIN	LVT 3V	LVTH 3V	AHC	AHCT	LV 3V	LV 5V	LV-AT	LVC 3V	ALVC 3V	AUC 1.8V	AUC 2.3V	UNIT
$I_{CC}$	MAX	7	7	0.04	0.02	0.02	0.02	0.02	0.01	0.01	0.01	0.01	mA
$I_{OH}$	MAX	-32	-32	-8	-8	-8	-16	-16	-24	-24	-8	-9	mA
$I_{OL}$	MAX	64	64	8	8	8	16	16	24	24	8	9	mA

## SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	TTL	LS	F	SN74 HC	CD74 HC	SN74 HCT	CD74 HCT	SN74 BCT	SN64 BCT	ABT
$t_{PLH}$	A	Y	MAX	13	15	6.5	30	30	33	38	5.7	6	4.9
$t_{PHL}$			MAX	18	18	8	30	30	33	38	7.7	8	4.9
$t_{PZH}$	$\bar{G}$	Y	MAX	17	20	8.5	30	38	35	38	10.3	11.1	5.9
$t_{PZL}$			MAX	25	25	9	30	38	35	38	11.7	12.8	6.8
$t_{PHZ}$			MAX	8	20	6	30	38	33	42	8.9	9.4	6.2
$t_{PLZ}$			MAX	12	20	6	30	38	33	42	8.6	9.9	6.2

PARAMETER	INPUT	OUTPUT	MAX or MIN	LVT 3V	LVTH 3V	AHC	AHCT	LV 3V	LV 5V	LV-AT	LVC 3V	ALVC 3V	AUC 1.8V	AUC 2.3V
$t_{PLH}$	A	Y	MAX	4.0	3.5	8.5	8.5	13	8.5	10.5	4.8	2.8	2.6	2.1
$t_{PHL}$			MAX	3.9	3.9	8.5	8.5	13	8.5	10.5	4.8	2.8	2.6	2.1
$t_{PZH}$	$\bar{G}$	Y	MAX	4.7	4	8	8	13	8	9.5	5.4	3.5	2.8	2.3
$t_{PZL}$			MAX	4.7	4	8	8	13	8	9.5	5.4	3.5	2.8	2.3
$t_{PHZ}$			MAX	5.1	4.5	10	10	15	10	9	4.6	4	3.4	2.3
$t_{PLZ}$			MAX	4.5	4.5	10	10	15	10	9	4.6	4	3.4	2.3

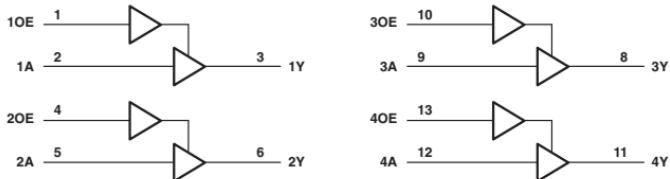
UNIT: NS

■: OBSOLETE or NOT RECOMMENDED NEW DESIGNS

## QUADRUPLE BUS BUFFER GATES WITH 3-STATE OUTPUTS

● Y = A

Logic Diagram (SN74)

FUNCTION TABLE  
(SN74)  
(each buffer)

INPUTS	OUTPUT	
OE	A	Y
H	H	H
H	L	L
L	X	Z

## ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	TTL	LS	F	SN74 HC	CD74 HC	CD74 HCT	SN74 BCT	SN64 BCT	ABT	UNIT
I <sub>CC</sub>	MAX	62	22	48	0.08	0.16	0.16	51	51	30	mA
I <sub>OH</sub>	MAX	-5.2	-2.6	-15	-6	-6	-6	-15	-15	-32	mA
I <sub>OL</sub>	MAX	16	24	64	6	6	6	64	64	64	mA

PARAMETER	MAX or MIN	LVTH 3V	AHC	AHCT	LV 3V	LV 5V	LVC 3V	ALVC 3V	AUC 1.8V	AUC 2.3V	UNIT
I <sub>CC</sub>	MAX	7	0.04	0.02	0.02	0.02	0.01	0.01	0.01	0.01	mA
I <sub>OH</sub>	MAX	-32	-8	-8	-8	-16	-24	-24	-8	-9	mA
I <sub>OL</sub>	MAX	64	8	8	8	16	24	24	8	9	mA

## SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	TTL	LS	F	SN74 HC	CD74 HC	CD74 HCT	SN74 BCT	SN64 BCT	ABT
I <sub>PLH</sub>	A	Y	MAX	13	15	7	30	30	36	6.3	6.3	6.3
I <sub>PHL</sub>			MAX	18	18	8.5	30	30	36	7.4	7.4	5.7
I <sub>PZH</sub>			MAX	18	25	8.5	30	38	38	7.9	7.9	6.5
I <sub>PZL</sub>			MAX	25	35	8.5	30	38	38	10.5	10.5	6.5
I <sub>PZH</sub>			MAX	16	25	7.5	30	38	42	10	10	6.8
I <sub>PZL</sub>			MAX	18	25	8	30	38	42	12.3	12.3	6.7

PARAMETER	INPUT	OUTPUT	MAX or MIN	LVTH 3V	AHC	AHCT	LV 3V	LV 5V	LVC 3V	ALVC 3V	AUC 1.8V	AUC 2.3V
I <sub>PLH</sub>	A	Y	MAX	3.8	8.5	8.5	13	8.5	4.7	3.1	2.6	2.1
I <sub>PHL</sub>			MAX	3.9	8.5	8.5	13	8.5	4.7	3.1	2.6	2.1
I <sub>PZH</sub>			MAX	5.4	8	8	13	8	5.7	3.3	2.7	2.2
I <sub>PZL</sub>			MAX	5.2	8	8	13	8	5.7	3.3	2.7	2.2
I <sub>PZH</sub>			MAX	3.8	10	10	15	10	6	3.7	3.3	2.2
I <sub>PZL</sub>			MAX	5.5	10	10	15	10	6	3.7	3.3	2.2

UNIT: ns

**50- $\Omega$  LINE DRIVERS**

- $Y = \overline{A} + \overline{B}$



ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	TTL	UNIT
$I_{CC}$	MAX	57	mA
$I_{OH}$	MAX	-42.4	mA
$I_{OL}$	MAX	48	mA

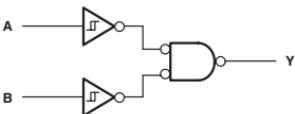
SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	TTL
$t_{PLH}$	A, B	Y	MAX	9
$t_{PHL}$	A, B	Y	MAX	12

UNIT: ns

**QUADRUPLE POSITIVE-NAND GATES WITH SCHMITT TRIGGER INPUTS**

- $Y = \overline{A} \bullet \overline{B}$



ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	TTL	LS	S	SN74 HC	CD74 HC	CD74 HCT	AHC	AHCT	LV 3V	LV 5V	UNIT
$I_{CC}$	MAX	40	14	68	0.02	0.04	0.04	0.02	0.02	0.02	0.02	mA
$I_{OH}$	MAX	-0.8	-0.4	-1	-4	-4	-4	-8	-8	-6	-12	mA
$I_{OL}$	MAX	16	8	20	4	4	4	8	8	6	12	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	TTL	LS	S	SN74 HC	CD74 HC	CD74 HCT	AHC	AHCT
$t_{PLH}$	A, B	Y	MAX	22	22	10.5	31	38	50	11	10
$t_{PHL}$	A, B	Y	MAX	22	22	13	31	38	50	11	8

PARAMETER	INPUT	OUTPUT	MAX or MIN	LV 3V	LV 5V
$t_{PLH}$	A, B	Y	MAX	17.5	11
$t_{PHL}$	A, B	Y	MAX	17.5	11

UNIT: ns

## 13-INPUT POSITIVE-NAND GATES

$$\bullet Y = \overline{A} \cdot \overline{B} \cdot \overline{C} \cdot \overline{D} \cdot \overline{E} \cdot \overline{F} \cdot \overline{G} \cdot \overline{H} \cdot \overline{I} \cdot \overline{J} \cdot \overline{K} \cdot \overline{L} \cdot \overline{M}$$

FUNCTION TABLE

INPUTS A-H	OUTPUT Y
All inputs H	L
One or more inputs L	H

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	S	ALS	SN74 HC	UNIT
I <sub>CC</sub>	MAX	10	0.34	0.02	mA
I <sub>OH</sub>	MAX	-1	-0.4	-4	mA
I <sub>OL</sub>	MAX	20	8	4	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	S	ALS	SN74 HC
I <sub>PLH</sub>	A to M	Y	MAX	6	11	38
I <sub>PHL</sub>	A to M	Y	MAX	7	25	38

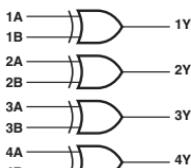
UNIT: ns

## QUADRUPLE 2-INPUT EXCLUSIVE-OR GATES WITH OPEN COLLECTOR OUTPUTS

$$\bullet Y = A \oplus B = \overline{A}B + \overline{A}\overline{B}$$

FUNCTION TABLE

INPUTS	OUTPUT	
A	B	Y
L	L	L
L	H	H
H	L	H
H	H	L



ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	TTL	LS	ALS	AS	UNIT
I <sub>CC</sub>	MAX	50	10	5.9	31	mA
V <sub>OH</sub>	MAX	5.5	5.5	5.5	5.5	V
I <sub>OL</sub>	MAX	16	8	8	20	mA

SWITCHING CHARACTERISTICS

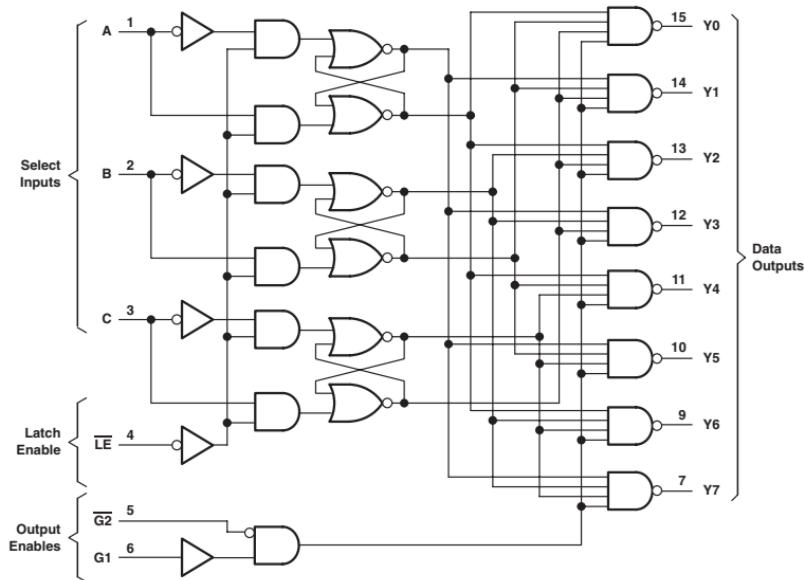
PARAMETER	INPUT	OUTPUT	MAX or MIN	TTL	LS	ALS	AS
I <sub>PLH</sub>	A or B	Y (Other Output = L)	MAX	18	30	50	12.5
I <sub>PHL</sub>	A or B	Y (Other Output = L)	MAX	50	30	15	7.1
I <sub>PLH</sub>	A or B	Y (Other Output = L)	MAX	22	30	50	11.4
I <sub>PHL</sub>	A or B	Y (Other Output = L)	MAX	55	30	15	10.7

UNIT: ns

## 3-LINE TO 8-LINE DECODERS/DEMULTIPLEXERS WITH ADDRESS LATCHES

- Incorporates Two Output Enables To Simplify Cascading

Logic Diagram (SN74ALS)



FUNCTION TABLE (SN74)

INPUTS				OUTPUTS							
ENABLE	SELECT			Y0	Y1	Y2	Y3	Y4	Y5	Y6	Y7
X	X	H	X	X	X	H	H	H	H	H	H
X	L	X	X	X	H	H	H	H	H	H	H
L	H	L	L	L	H	H	H	H	H	H	H
L	H	L	L	H	H	L	H	H	H	H	H
L	H	L	L	H	H	L	H	H	H	H	H
L	H	L	L	H	H	H	L	H	H	H	H
L	H	L	H	L	H	H	H	H	H	L	H
L	H	L	H	H	H	H	H	H	H	H	L
H	H	L	X	X	X	Depends upon the address previously applied while LE was at a logic low.					

## ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	LS	ALS	AS	SN74 HC	CD74 HC	SN74 HCT	CD74 HCT	LVC 3V	UNIT
I <sub>CC</sub>	MAX	18	11	24	0.08	0.16	0.08	0.16	0.01	mA
I <sub>OH</sub>	MAX	-0.4	-0.4	-2	-4	-4	-4	-4	-24	mA
I <sub>OL</sub>	MAX	8	8	20	4	4	4	4	24	mA

## SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	LS	ALS	AS	SN74 HC	CD74 HC	SN74 HCT	CD74 HCT	LVC 3V
I <sub>PLH</sub>	SELECT	Y (CD74: $\bar{Y}$ )	MAX	24	20	12.5	48	54	48	57	-
I <sub>PHL</sub>			MAX	38	20	12.5	48	54	48	57	-
I <sub>PLH</sub>	$\bar{G}_2$	Y (CD74: $\bar{Y}$ )	MAX	21	12	8	36	44	36	56	-
I <sub>PHL</sub>			MAX	27	15	8.5	36	44	36	56	-
I <sub>PLH</sub>	G1	Y (CD74: $\bar{Y}$ )	MAX	21	17	10	36	44	36	53	-
I <sub>PHL</sub>			MAX	27	15	9	36	44	36	53	-
I <sub>PLH</sub>	LE (CD74: LE)	Y (CD74: $\bar{Y}$ )	MAX	27	22	13.5	48	57	52	66	-
I <sub>PHL</sub>			MAX	38	20	14	48	57	52	66	-

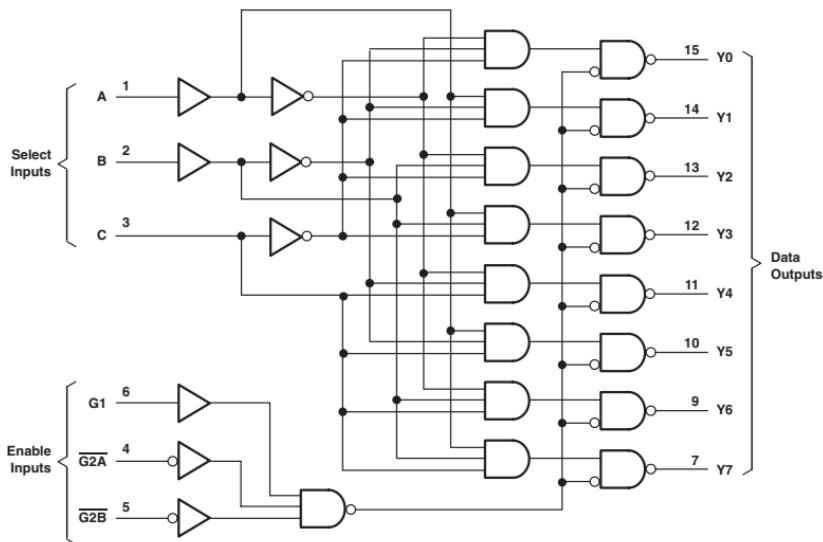
UNIT:ns

LVC:Preview

## 3-LINE TO 8-LINE DECODERS/DEMULITPLEXRS

- 3 Enable Inputs to Simplify Cascading and/or Data Reception
- 74AC11xxx: Product Available in Reduced-Noise Advanced CMOS (11000 Series)
- 74ACT11xxx: Product Available in Reduced-Noise Advanced CMOS (11000 Series)

Logic Diagram (SN74, CD74AC/ACT)



**FUNCTION TABLE (SN74)**

ENABLE INPUTS			SELECT INPUTS			OUTPUTS							
G1	G2A	G2B	C	B	A	Y0	Y1	Y2	Y3	Y4	Y5	Y6	Y7
X	H	X	X	X	X	H	H	H	H	H	H	H	H
X	X	H	X	X	X	H	H	H	H	H	H	H	H
L	X	X	X	X	X	H	H	H	H	H	H	H	H
H	L	L	L	L	L	L	H	H	H	H	H	H	H
H	L	L	L	L	H	H	L	H	H	H	H	H	H
H	L	L	L	H	H	H	H	L	H	H	H	H	H
H	L	L	H	L	L	H	H	H	L	H	H	H	H
H	L	L	H	L	H	H	H	H	H	L	H	H	H
H	L	L	H	H	L	H	H	H	H	H	L	H	H
H	L	L	H	H	H	H	H	H	H	H	H	H	L

**ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS**

PARAMETER	MAX or MIN	LS	S	ALS	AS	F	SN74 HC	CD74 HC	SN74 HCT	CD74 HCT	UNIT
I <sub>CC</sub>	MAX	10	74	10	20	20	0.08	0.16	0.08	0.16	mA
I <sub>OH</sub>	MAX	-0.4	-1	-0.4	-2	-1	-4	-4	-4	-4	mA
I <sub>OL</sub>	MAX	8	20	8	20	20	4	4	4	4	mA

PARAMETER	MAX or MIN	AC 11	CD74 AC	ACT 11	CD74 ACT	AHC	AHCT	LV 3V	LV 5V	LV-AT	LVC 3V	UNIT
I <sub>CC</sub>	MAX	0.04	0.16	0.04	0.16	0.04	0.04	0.02	0.02	0.01	0.01	mA
I <sub>OH</sub>	MAX	-24	-24	-24	-24	-8	-8	-6	-12	-8	-24	mA
I <sub>OL</sub>	MAX	24	24	24	24	8	8	6	12	8	24	mA

**SWITCHING CHARACTERISTICS**

PARAMETER	INPUT	OUTPUT	MAX or MIN	LS	S	ALS	AS	F	SN74 HC	CD74 HC	SN74 HCT	CD74 HCT
I <sub>PLH</sub>	A, B, C	Y (CD74:Ȳ)	MAX	27	12	22	10	8.5	45	45	45	53
I <sub>PHL</sub>			MAX	39	12	18	9.5	9	45	45	45	53
I <sub>PLH</sub>		G2	MAX	26	11	17	7.5	8	39	53	42	53
I <sub>PHL</sub>			MAX	38	11	17	8.5	7.5	39	53	42	53
I <sub>PLH</sub>		G1	MAX	26	11	17	10	9	39	53	42	53
I <sub>PHL</sub>			MAX	38	11	17	10	8.5	39	53	42	53

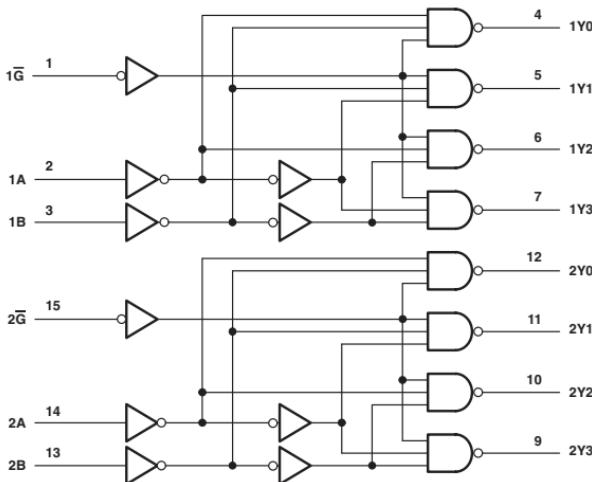
PARAMETER	INPUT	OUTPUT	MAX or MIN	AC 11	CD74 AC	ACT 11	CD74 ACT	AHC	AHCT	LV 3V	LV 5V	LV-AT	LVC 3V
I <sub>PLH</sub>	A, B, C	Y (CD74:Ȳ)	MAX	8.1	11	9.8	12	11.5	13	18	11.5	14	6.7
I <sub>PHL</sub>			MAX	8.8	11	9.7	12	11.5	13	18	11.5	14	6.7
I <sub>PLH</sub>		G2	MAX	8.3	10	8.9	10.5	11.5	12	17	11.5	13	6.5
I <sub>PHL</sub>			MAX	8.3	10	8.9	10.5	11.5	12	17	11.5	13	6.5
I <sub>PLH</sub>		G1	MAX	7.5	11	9.3	11	11.5	11.5	18.5	11.5	12	5.8
I <sub>PHL</sub>			MAX	7.7	11	9.8	11	11.5	11.5	18.5	11.5	12	5.8

UNIT: ns

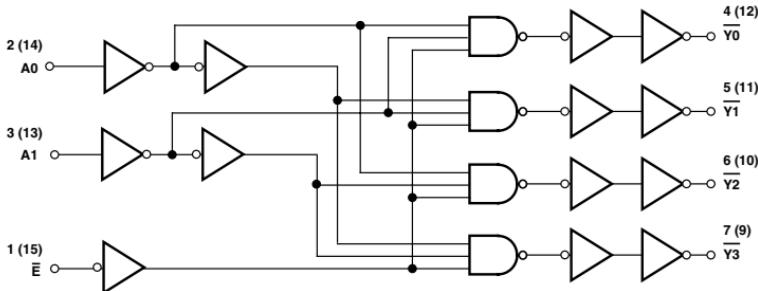
## DUAL 2-LINE TO 4-LINE DECODERS/DEMULTIPLEXERS

- Incorporate Two Enable Inputs to Simplify Cascading and /or Data Reception
- 74ACT11xxx: Product Available in Reduced-Noise Advanced CMOS (11000 Series)

Logic Diagram (SN74, CD74AC/ACT)



Logic Diagram (CD74HC/HCT)



**FUNCTION TABLE (SN74)**

INPUTS		OUTPUTS				
ENABLE $\bar{G}$	SELECT B A	Y0	Y1	Y2	Y3	
H	X X	H	H	H	H	
L	L L	L	H	H	H	
L	L H	H	L	H	H	
L	H L	H	H	L	H	
L	H H	H	H	H	L	

**ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS**

PARAMETER	MAX or MIN	LS	S	ALS	SN74 HC	CD74 HC	SN74 HCT	CD74 HCT	CD74 AC	ACT 11	UNIT
$I_{CC}$	MAX	11	90	13	0.08	0.16	0.08	0.16	0.16	0.08	mA
$I_{OH}$	MAX	-0.4	-1	-0.4	-4	-4	-4	-4	-24	-24	mA
$I_{OL}$	MAX	8	20	8	4	4	4	4	24	24	mA

PARAMETER	MAX or MIN	CD74 ACT	AHC	AHCT	LV 3V	LV 5V	LVC 3V	UNIT
$I_{CC}$	MAX	0.16	0.04	0.02	-	0.02	0.01	mA
$I_{OH}$	MAX	-24	-8	-8	-6	-12	-24	mA
$I_{OL}$	MAX	24	8	8	6	12	24	mA

**SWITCHING CHARACTERISTICS**

PARAMETER	INPUT	OUTPUT	MAX or MIN	LS	S	ALS	SN74 HC	CD74 HC	SN74 HCT	CD74 HCT	CD74 AC	ACT 11
$I_{PLH}$	SELECT	Y (CD74: $\bar{Y}$ )	MAX	29	12	14	44	44	43	51	10.5	8.5
$I_{PHL}$	SELECT	Y (CD74: $\bar{Y}$ )	MAX	38	12	14	44	44	43	51	10.5	8.5
$I_{PLH}$	$\bar{G}$ (CD74: E)	Y (CD74: $\bar{Y}$ )	MAX	24	8	14	44	41	43	51	10.5	7.9
$I_{PHL}$	$\bar{G}$ (CD74: E)	Y (CD74: $\bar{Y}$ )	MAX	32	10	15	44	41	43	51	10.5	7.5

PARAMETER	INPUT	OUTPUT	MAX or MIN	CD74 ACT	AHC	AHCT	LV 3V	LV 5V	LVC 3V
$I_{PLH}$	SELECT	Y (CD74: $\bar{Y}$ )	MAX	11.5	10.5	10.5	16.5	10.5	6.2
$I_{PHL}$	SELECT	Y (CD74: $\bar{Y}$ )	MAX	11.5	10.5	10.5	16.5	10.5	6.2
$I_{PLH}$	$\bar{G}$ (CD74: E)	Y (CD74: $\bar{Y}$ )	MAX	12	9.5	9.5	14.5	9.5	4.7
$I_{PHL}$	$\bar{G}$ (CD74: E)	Y (CD74: $\bar{Y}$ )	MAX	12	9.5	9.5	14.5	9.5	4.7

UNIT: ns

**DUAL 4-INPUT POSITIVE-NAND  
50- $\Omega$  LINE DRIVERS**

●  $Y = \overline{ABCD}$

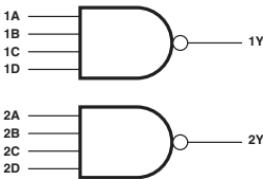
**ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS**

PARAMETER	MAX or MIN	S	UNIT
$I_{CC}$	MAX	44	mA
$I_{OH}$	MAX	-40	mA
$I_{OL}$	MAX	60	mA

**SWITCHING CHARACTERISTICS**

PARAMETER	INPUT	OUTPUT	MAX or MIN	S
$t_{PLH}$	A, B, C, D	Y	MAX	6.5
$t_{PHL}$			MAX	6.5

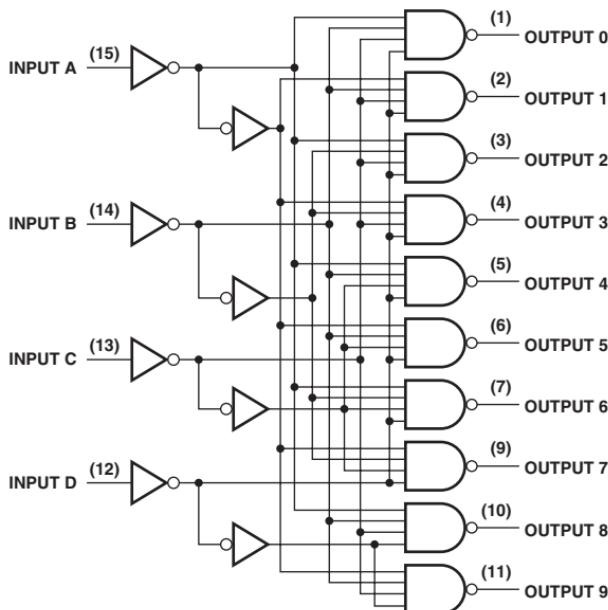
UNIT: ns

**Logic Diagram**


## BCD-TO-DECIMAL DECODERS/DRIVERS

- Sink-Current Capability: 80mA
- Low Power Dissipation (SN74LS): 35mW (typ)

Logic Diagram



FUNCTION TABLE

No.	INPUTS				OUTPUTS									
	D	C	B	A	0	1	2	3	4	5	6	7	8	9
0	L	L	L	L	L	H	H	H	H	H	H	H	H	H
1	L	L	L	H	H	L	H	H	H	H	H	H	H	H
2	L	L	H	L	H	H	L	H	H	H	H	H	H	H
3	L	L	H	H	H	H	H	L	H	H	H	H	H	H
4	L	H	L	L	H	H	H	H	L	H	H	H	H	H
5	L	H	L	H	H	H	H	H	H	L	H	H	H	H
6	L	H	H	L	H	H	H	H	H	H	L	H	H	H
7	L	L	H	H	H	H	H	H	H	H	H	L	H	H
8	H	L	L	L	H	H	H	H	H	H	H	H	L	H
9	H	L	L	H	H	H	H	H	H	H	H	H	H	L
INVALID	H	L	H	L	H	H	H	H	H	H	H	H	H	H
INVALID	H	L	H	H	H	H	H	H	H	H	H	H	H	H
INVALID	H	H	L	L	H	H	H	H	H	H	H	H	H	H
INVALID	H	H	L	H	H	H	H	H	H	H	H	H	H	H
INVALID	H	H	H	L	H	H	H	H	H	H	H	H	H	H
INVALID	H	H	H	H	H	H	H	H	H	H	H	H	H	H

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	TTL	LS	UNIT
I <sub>cc</sub>	MAX	70	13	mA
V <sub>o</sub> (OFF)	MAX	15	15	mA

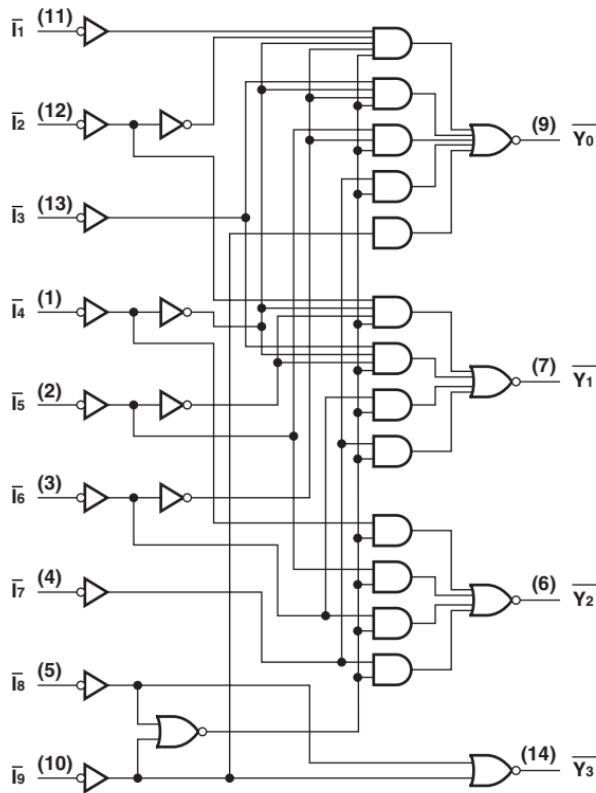
SWITCHING CHARACTERISTICS

PARAMETER	MAX or MIN	TTL	LS
t <sub>PLH</sub>	MAX	50	50
t <sub>PHL</sub>	MAX	50	50

UNIT: ns

## 10-LINE TO 4-LINE BCD PRIORITY ENCODER

Logic Diagram



FUNCTION TABLE

INPUTS								OUTPUTS				
$\overline{I_1}$	$\overline{I_2}$	$\overline{I_3}$	$\overline{I_4}$	$\overline{I_5}$	$\overline{I_6}$	$\overline{I_7}$	$\overline{I_8}$	$\overline{I_9}$	$\overline{V_0}$	$\overline{V_1}$	$\overline{V_2}$	$\overline{V_3}$
H	H	H	H	H	H	H	H	H	H	H	H	H
X	X	X	X	X	X	X	X	L	L	H	H	L
X	X	X	X	X	X	X	L	H	L	H	H	H
X	X	X	X	X	X	L	H	H	H	L	L	L
X	X	X	X	X	L	H	H	H	H	L	L	H
X	X	X	X	L	H	H	H	H	H	L	H	L
X	X	X	X	L	H	H	H	H	H	L	H	H
X	X	X	L	H	H	H	H	H	H	L	H	H
X	X	L	H	H	H	H	H	H	H	H	L	L
X	L	H	H	H	H	H	H	H	H	H	L	H
L	H	H	H	H	H	H	H	H	H	H	L	

## ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	TTL	LS	SN74 HC	CD74 HC	CD74 HCT	UNIT
$I_{CC}$	MAX	70	20	0.08	0.16	0.16	mA
$I_{OH}$	MAX	-0.8	-0.4	-4	-4	-4	mA
$I_{OL}$	MAX	16	8	4	4	4	mA

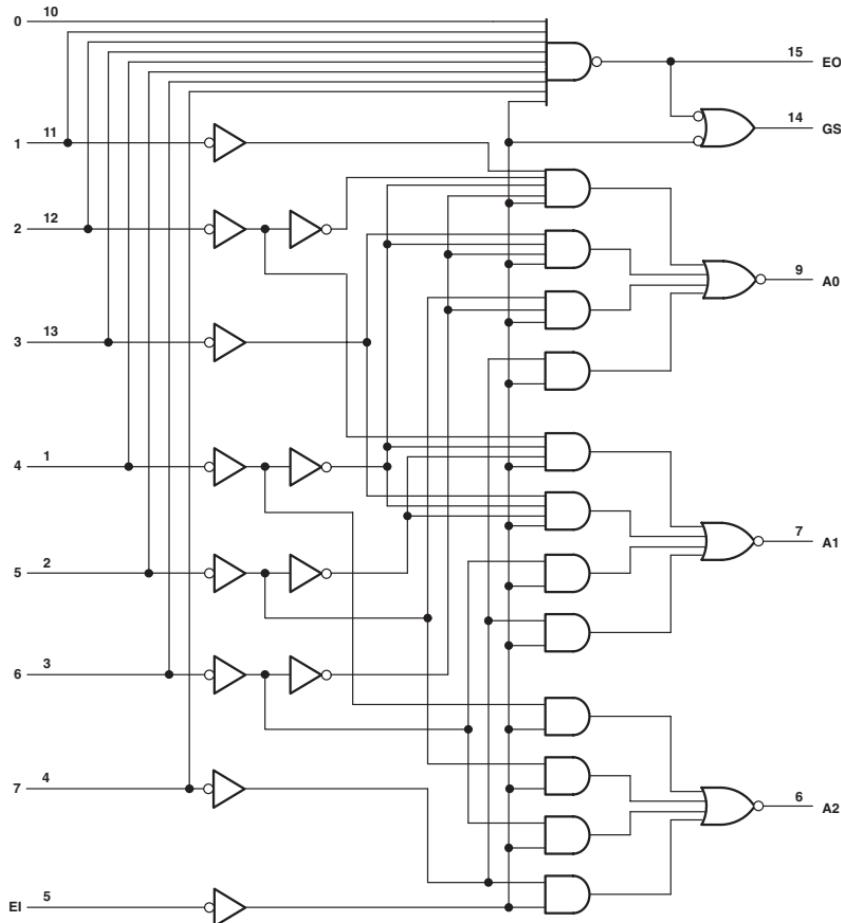
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## SWITCHING CHARACTERISTICS

PARAMETER	MAX or MIN	TTL	LS	SN74 HC	CD74 HC	CD74 HCT
$t_{PLH}$	MAX	19	33	48	48	53
$t_{PHL}$	MAX	19	23	48	48	53

## 8-LINE TO 3-LINE PRIORITY ENCODERS

Logic Diagram (SN74)



FUNCTION TABLE (SN74)

EI	INPUTS							OUTPUTS					
	0	1	2	3	4	5	6	7	A2	A1	A0	GS	EO
H	X	X	X	X	X	X	X	X	H	H	H	H	H
L	H	H	H	H	H	H	H	H	H	H	H	H	L
L	X	X	X	X	X	X	X	L	L	L	L	L	H
L	X	X	X	X	X	X	L	H	L	L	H	L	H
L	X	X	X	X	X	L	H	H	L	H	L	L	H
L	X	X	X	X	L	H	H	H	L	H	H	L	H
L	X	X	X	X	L	H	H	H	L	H	H	L	H
L	X	X	X	L	H	H	H	H	H	L	L	L	H
L	X	X	L	H	H	H	H	H	H	L	H	L	H
L	X	H	H	H	H	H	H	H	H	H	L	L	H
L	L	H	H	H	H	H	H	H	H	H	L	H	H

## ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	TTL	LS	SN74 HC	UNIT
I <sub>CC</sub>	MAX	60	20	0.08	mA
I <sub>OL</sub>	MAX	16	8	4	mA
I <sub>OH</sub>	MAX	-0.8	-0.4	-4	mA

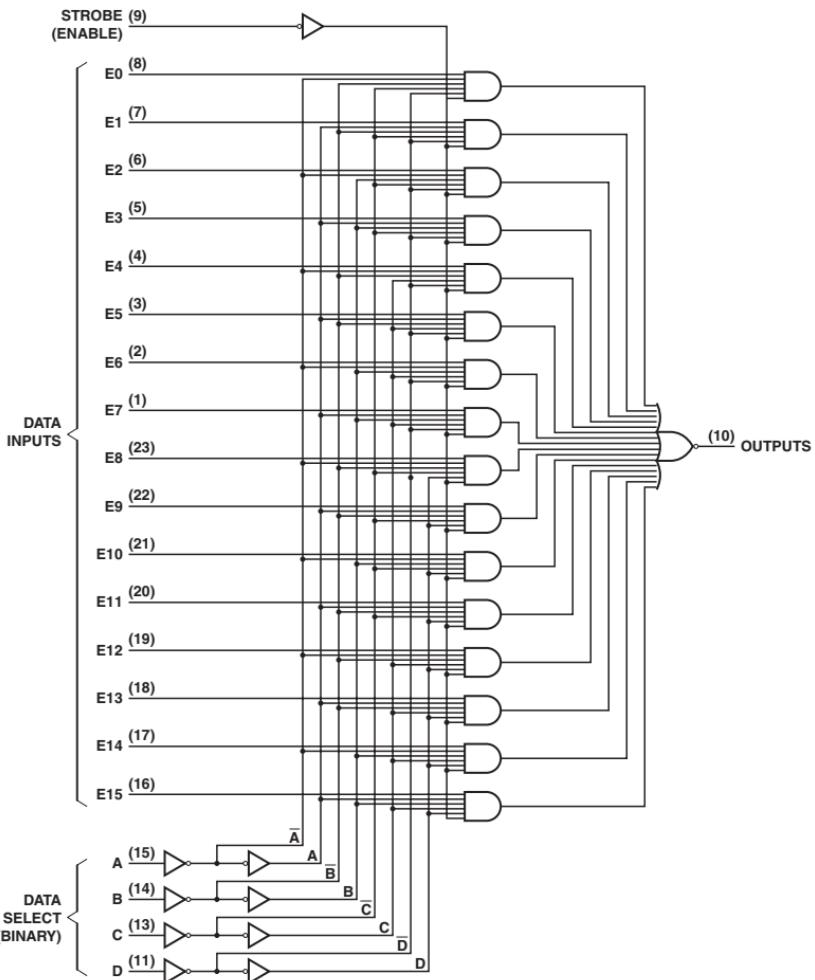
## SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	WAVEFORM	MAX or MIN	TTL	LS	SN74 HC
I <sub>PLH</sub>	1 to 7	A0, A1 or A2	In-phase output	MAX	15	18	45
I <sub>PHL</sub>					14	25	45
I <sub>PLH</sub>	1 to 7	A0, A1 or A2	Out-of-phase output	MAX	19	36	45
I <sub>PHL</sub>					19	29	45
I <sub>PLH</sub>	0 to 7	EO	Out-of-phase output	MAX	10	18	38
I <sub>PHL</sub>					25	40	38
I <sub>PLH</sub>	0 to 7	GS	In-phase output	MAX	30	55	48
I <sub>PHL</sub>					25	21	48
I <sub>PLH</sub>	EI	A0, A1 or A2	In-phase output	MAX	15	25	49
I <sub>PHL</sub>					15	25	49
I <sub>PLH</sub>	EI	GS	In-phase output	MAX	12	17	36
I <sub>PHL</sub>					15	36	36
I <sub>PLH</sub>	EI	EO	In-phase output	MAX	15	21	41
I <sub>PHL</sub>					30	35	41

UNIT: ns

## 16-LINE TO 1-LINE DATA SELECTOR/MULTIPLEXER

Logic Diagram



FUNCTION TABLE

INPUTS				STROBE G	OUTPUT W
SELECT D	C	B	A		
X	X	X	X	H	H
L	L	L	L	L	E0
L	L	L	H	L	E1
L	L	H	L	L	E2
L	L	H	H	L	E3
L	H	L	L	L	E4
L	H	L	H	L	E5
L	H	H	L	L	E6
L	H	H	H	L	E7
H	L	L	L	L	E8
H	L	L	H	L	E9
H	L	H	L	L	E10
H	L	H	H	L	E11
H	H	L	L	L	E12
H	H	L	H	L	E13
H	H	H	L	L	E14
H	H	H	H	L	E15

## NOTES:

H = High Level, L = Low Level, X = irrelevant  
E0, E1 ... E15 = the complement of the level of the respective E input  
D0, D1 ... D7 = the level of the D respective input

## ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	TTL	UNIT
I <sub>CC</sub>	MAX	48	mA
I <sub>OH</sub>	MAX	-0.8	mA
I <sub>OL</sub>	MAX	16	mA

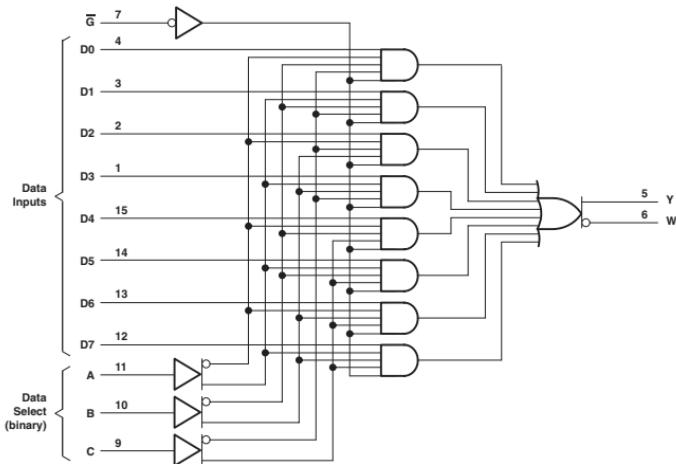
## SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	TTL
I <sub>PLH</sub>	A, B, C or D	W	MAX	35
I <sub>PHL</sub>				33
I <sub>PLH</sub>	Strobe G	W	MAX	24
I <sub>PHL</sub>				30
I <sub>PLH</sub>	E0 thru E15 or E0 thru D7	W	MAX	14
I <sub>PHL</sub>				20

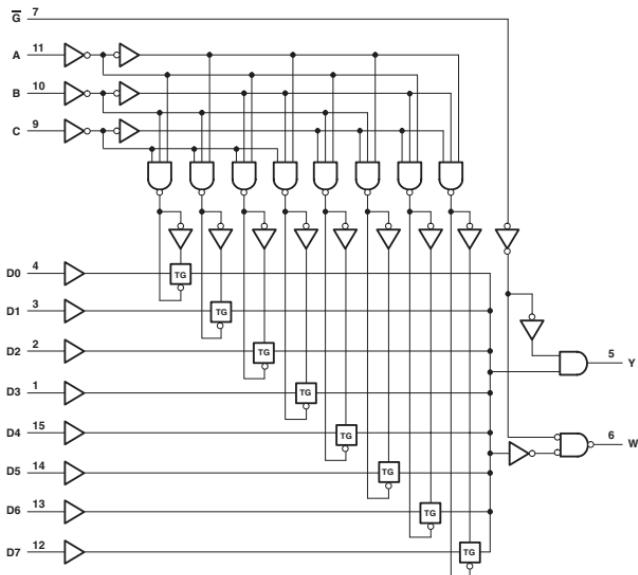
UNIT:ns

## 8-LINE TO 1-LINE DATA SELECTORS/MULTIPLEXERS

Logic Diagram (SN74ALS, AS, F, CD74AC/ACT)



Logic Diagram (SN74HC)



**FUNCTION TABLE (SN74)**

INPUTS			OUTPUTS	
SELECT	C	B	G	Y W
X	X	X	H	L H
L	L	L	L	D0 D0
L	L	H	L	D1 D1
L	H	L	L	D2 D2
L	H	H	L	D3 D3
H	L	L	L	D4 D4
H	L	H	L	D5 D5
H	H	L	L	D6 D6
H	H	H	L	D7 D7

**ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS**

PARAMETER	MAX or MIN	TTL	LS	S	ALS	AS	F	SN74 HC	CD74 HC	CD74 HCT	CD74 AC	CD74 ACT	UNIT
I <sub>CC</sub>	MAX	48	10	70	12	30	21	0.08	0.16	0.16	0.16	0.16	mA
I <sub>OH</sub>	MAX	-0.8	-0.4	-1	-2.6	-15	-1	-6	-4	-4	-24	-24	mA
I <sub>OL</sub>	MAX	16	8	20	24	48	24	6	4	4	24	24	mA

**SWITCHING CHARACTERISTICS**

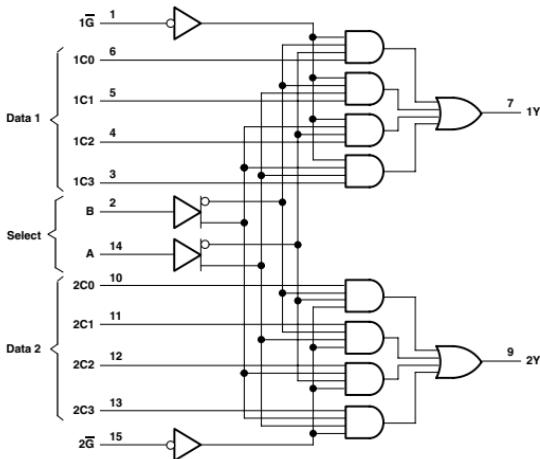
PARAMETER	INPUT	OUTPUT	MAX or MIN	TTL	LS	S	ALS	AS	F	SN74 HC	CD74 HC	CD74 HCT
I <sub>PLH</sub> I <sub>PHL</sub>	A, B or C (CD74HC/HCT: Sn)	Y	MAX	38	43	18	18	14.5	12	63	56	62
				38	30	18	24	15	9	63	56	62
I <sub>PLH</sub> I <sub>PHL</sub>	A, B or C (CD74HC/HCT: Sn)	W (CD74HC: $\bar{Y}$ )	MAX	26	23	15	24	12	9.5	63	62	65
				30	32	13.5	23	12	7.5	63	62	65
I <sub>PLH</sub> I <sub>PHL</sub>	D0 to D7 (CD74HC/HCT: In)	Y	MAX	20	32	16.5	10	10.5	7.5	49	51	57
				27	26	18	15	11	7.5	49	51	57
I <sub>PLH</sub> I <sub>PHL</sub>	D0 to D7 (CD74HC/HCT: In)	W (CD74HC: $\bar{Y}$ )	MAX	14	21	13	15	6.5	7	49	56	54
				14	20	12	15	4.5	5	49	56	54
I <sub>PLH</sub> I <sub>PHL</sub>	$\bar{G}$ (CD74HC/HCT: $\bar{E}$ )	Y	MAX	33	42	12	18	14	10.5	32	42	44
				33	32	12	19	11	7.5	32	42	44
I <sub>PLH</sub> I <sub>PHL</sub>	$\bar{G}$ (CD74HC/HCT: $\bar{E}$ )	W (CD74HC: $\bar{Y}$ )	MAX	21	24	7	19	6	7	32	44	54
				23	30	7	23	10	6	32	44	54

PARAMETER	INPUT	OUTPUT	MAX or MIN	CD74 AC	CD74 ACT
I <sub>PLH</sub> I <sub>PHL</sub>	A, B or C (CD74HC/HCT: Sn)	Y	MAX	18.2	20.2
				18.2	20.2
I <sub>PLH</sub> I <sub>PHL</sub>	A, B or C (CD74HC/HCT: Sn)	W (CD74HC: $\bar{Y}$ )	MAX	19.6	21.6
				19.6	21.6
I <sub>PLH</sub> I <sub>PHL</sub>	D0 to D7 (CD74HC/HCT: In)	Y	MAX	13.5	15.5
				13.5	15.5
I <sub>PLH</sub> I <sub>PHL</sub>	D0 to D7 (CD74HC/HCT: In)	W (CD74HC: $\bar{Y}$ )	MAX	14.9	16.9
				14.9	16.9
I <sub>PLH</sub> I <sub>PHL</sub>	$\bar{G}$ (CD74HC/HCT: $\bar{E}$ )	Y	MAX	12.2	12.1
				12.2	12.1
I <sub>PLH</sub> I <sub>PHL</sub>	$\bar{G}$ (CD74HC/HCT: $\bar{E}$ )	W (CD74HC: $\bar{Y}$ )	MAX	13.5	13.5
				13.5	13.5

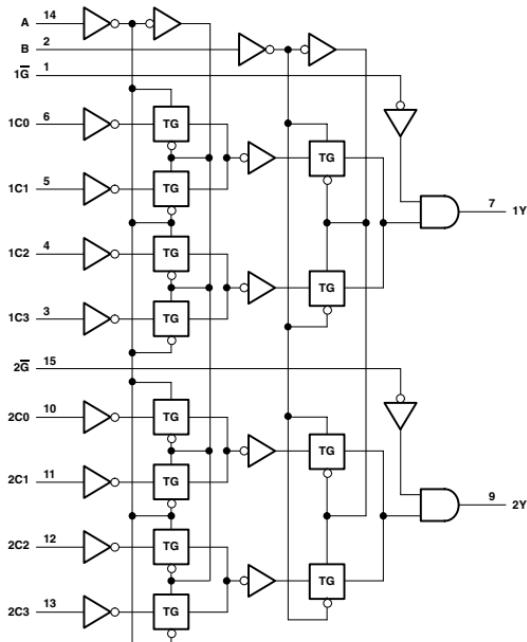
UNIT: ns

## DUAL 4-LINE TO 1-LINE DATA SELECTORS/MULTIPLEXERS

Logic Diagram (SN74ALS, AS, F, LS)



Logic Diagram (SN74HC, HCT, CD74AC, ACT)



FUNCTION TABLE (SN74)

SELECT INPUTS		DATA INPUTS			STROBE	OUTPUTS	
B	A	C0	C1	C2	C3	6	Y
X	X	X	X	X	X	H	L
L	L	L	X	X	X	L	L
L	L	H	X	X	X	L	H
L	H	X	L	X	X	L	L
L	H	H	X	X	X	L	H
H	L	X	X	L	X	L	L
H	L	X	X	H	X	L	H
H	H	X	X	X	X	L	L
H	H	X	X	X	H	L	H

## ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	TTL	LS	S	ALS	AS	F	SN74 HC	CD74 HC	CD74 HCT	CD74 AC	CD74 ACT	UNIT
I <sub>CC</sub>	MAX	60	10	70	14	33	20	0.08	0.16	0.16	0.16	0.16	mA
I <sub>OH</sub>	MAX	-0.8	-0.4	-1	-2.6	-15	-1	-6	-4	-4	-24	-24	mA
I <sub>OL</sub>	MAX	16	8	20	24	48	20	6	4	4	24	24	mA

## SWITCHING CHARACTERISTICS

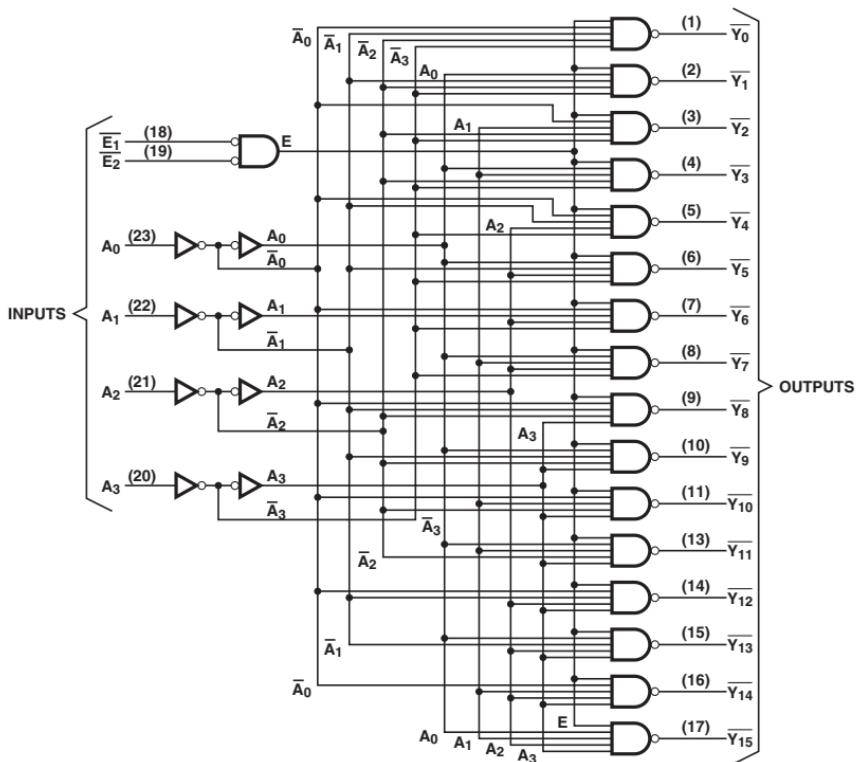
PARAMETER	INPUT	OUTPUT	MAX or MIN	TTL	LS	S	ALS	AS	F	SN74 HC	CD74 HC	CD74 HCT
I <sub>PLH</sub>	DATA	Y	MAX	18	15	9	10	7	8	35	44	51
I <sub>PHL</sub>			MAX	23	26	9	15	8	7.5	35	44	51
I <sub>PLH</sub>	SELECT	Y	MAX	34	29	18	21	12.5	12	38	48	51
I <sub>PHL</sub>			MAX	34	38	18	21	11	10.5	38	48	51
I <sub>PLH</sub>	STROBE	Y	MAX	30	24	15	18	11.5	10.5	24	36	41
I <sub>PHL</sub>			MAX	23	32	13.5	18	9	8	24	36	41

PARAMETER	INPUT	OUTPUT	MAX or MIN	CD74 AC	CD74 ACT
I <sub>PLH</sub>	DATA	Y	MAX	13.3	18
I <sub>PHL</sub>			MAX	13.3	18
I <sub>PLH</sub>	SELECT	Y	MAX	20	22
I <sub>PHL</sub>			MAX	20	22
I <sub>PLH</sub>	STROBE	Y	MAX	11.8	12.6
I <sub>PHL</sub>			MAX	11.8	12.6

UNIT: ns

## 4-LINE TO 16-LINE DECODERS/DEMULTIPLEXERS

Logic Diagram



FUNCTION TABLE

INPUTS					OUTPUTS															
E <sub>1</sub>	E <sub>2</sub>	A <sub>3</sub>	A <sub>2</sub>	A <sub>1</sub>	Y <sub>0</sub>	Y <sub>1</sub>	Y <sub>2</sub>	Y <sub>3</sub>	Y <sub>4</sub>	Y <sub>5</sub>	Y <sub>6</sub>	Y <sub>7</sub>	Y <sub>8</sub>	Y <sub>9</sub>	Y <sub>10</sub>	Y <sub>11</sub>	Y <sub>12</sub>	Y <sub>13</sub>	Y <sub>14</sub>	Y <sub>15</sub>
L	L	H	L	L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	L	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	L	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	L	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	H	L	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	H	L	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H
L	L	L	H	H	L	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H
L	L	H	L	L	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H
L	L	H	L	L	H	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H
L	L	H	L	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H	H
L	L	H	L	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H
L	L	H	H	L	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H
L	L	H	H	L	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H
L	L	H	H	H	L	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H
L	L	H	H	H	L	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H
L	L	H	X	X	X	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
H	L	X	X	X	X	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
H	H	X	X	X	X	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H

## ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	TTL	ALS	SN74 HC	CD74 HC	CD74 HCT	UNIT
I <sub>CC</sub>	MAX	56	23	0.08	0.16	0.16	mA
I <sub>OH</sub>	MAX	-0.8	24	-4	-4	-4	mA
I <sub>OL</sub>	MAX	16	-0.4	4	4	4	mA

## SWITCHING CHARACTERISTICS

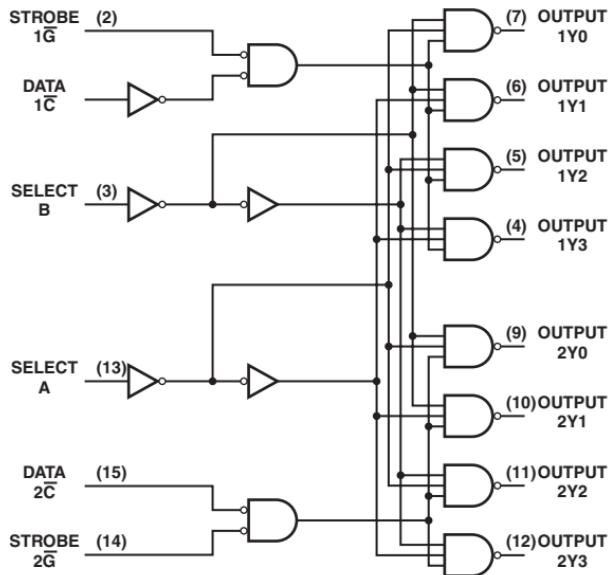
PARAMETER	INPUT	OUTPUT	MAX or MIN	TTL	ALS	SN74 HC	CD74 HC	CD74 HCT
I <sub>PLH</sub>	Adress	0 to 15 (CD74: Y <sub>0</sub> to Y <sub>15</sub> )	MAX	36	12	45	53	53
I <sub>PHL</sub>				33	12	45	53	53
I <sub>PLH</sub>	Enable	0 to 15 (CD74: Y <sub>0</sub> to Y <sub>15</sub> )	MAX	30	12	45	53	51
I <sub>PHL</sub>				27	12	45	53	51

UNIT: ns

## DUAL 2-LINE TO 4-LINE DECODERS/DEMULTIPLEXERS

- Individual Strobes Simplify Cascading for Decoding or Demultiplexing Larger Words
- Outputs: Totem Pole

Logic Diagram



## FUNCTION TABLES

2-LINE TO 4-LINE DECODER OR  
1-LINE TO 4-LINE DEMULTIPLEXER

INPUTS			OUTPUTS					
SELECT	STROBE	DATA	1Y0	1Y1	1Y2	1Y3		
B	A	1G	1C					
X	X	H	X	H	H	H	H	
L	L	L	H	L	H	H	H	
L	H	L	H	H	L	H	H	
H	L	L	H	H	L	H	L	
H	H	L	H	H	H	H	L	
X	X	X	L	H	H	H	H	

INPUTS			OUTPUTS					
SELECT	STROBE	DATA	2Y0	2Y1	2Y2	2Y3		
B	A	2G	2C					
X	X	H	X	H	H	H	H	
L	L	L	L	H	H	H	H	
L	H	L	L	H	L	H	H	
H	L	L	L	H	H	L	H	
H	H	L	L	H	H	H	L	
X	X	X	H	H	H	H	H	

3-LINE TO 8-LINE DECODER OR  
1-LINE TO 8-LINE DEMULTIPLEXER

INPUTS			OUTPUTS							
SELECT	STROBE or DATA	G†	(0)	(1)	(2)	(3)	(4)	(5)	(6)	(7)
C‡	B	A	2Y0	2Y1	2Y2	2Y3	1Y0	1Y1	1Y2	1Y3
X	X	X	H	H	H	H	H	H	H	H
L	L	L	L	H	H	H	H	H	H	H
L	L	H	H	L	H	H	H	H	H	H
L	H	L	L	H	H	L	H	H	H	H
L	H	H	L	H	H	H	L	H	H	H
H	L	L	L	H	H	H	L	H	H	H
H	L	H	L	H	H	H	H	L	H	H
H	H	L	L	H	H	H	H	H	L	H
H	H	H	L	H	H	H	H	H	H	L

† C = inputs 1C and 2C connected together  
‡ G = inputs 1G and 2G connected together

### ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	TTL	LS	ALS	UNIT
I <sub>CC</sub>	MAX	40	10	13	mA
I <sub>OH</sub>	MAX	-0.8	-0.4	-0.4	mA
I <sub>OL</sub>	MAX	16	8	8	mA

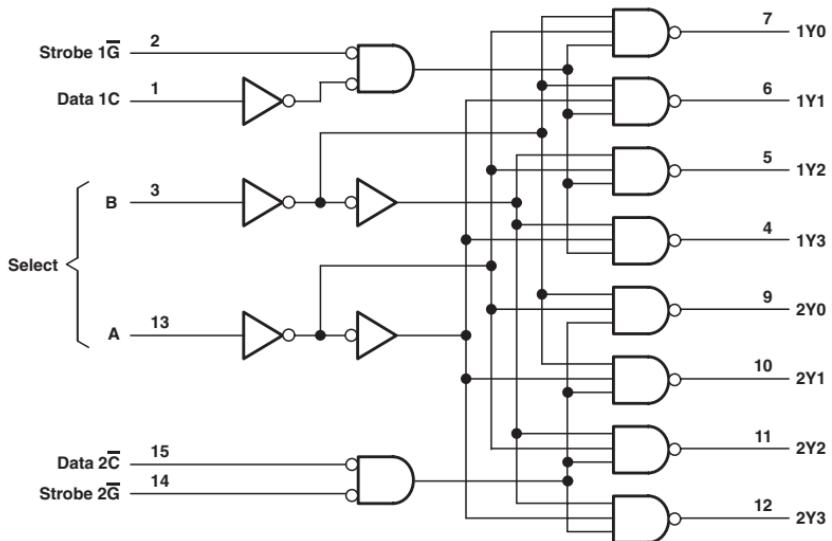
### SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	TTL	LS	ALS
I <sub>PLH</sub>	A or B	Y	MAX	32	26	14
I <sub>PHL</sub>				32	30	12
I <sub>PLH</sub>	1C	Y	MAX	24	27	12
I <sub>PHL</sub>				30	27	14

UNIT: ns

**DUAL 2-LINE TO 4-LINE DECODERS/DEMULITPLEXERS WITH OPEN-COLLECTOR OUTPUTS**

- Individual Strobes Simplify Cascading for Decoding or Demultiplexing Larger Words
- Outputs: Open-Collector

**Logic Diagram**


## FUNCTION TABLES

2-LINE TO 4-LINE DECODER OR  
1-LINE TO 4-LINE DEMULTIPLEXER

INPUTS			OUTPUTS			
SELECT	STROBE	DATA	1Y0	1Y1	1Y2	1Y3
B	A	1G	1C			
X	X	H	X	H	H	H
L	L	L	H	L	H	H
L	H	L	H	L	H	H
H	L	L	H	H	L	H
H	H	L	H	H	H	L
X	X	X	L	H	H	H

INPUTS			OUTPUTS			
SELECT	STROBE	DATA	2Y0	2Y1	2Y2	2Y3
B	A	2G	2C			
X	X	H	X	H	H	H
L	L	L	L	L	H	H
L	H	L	L	H	L	H
H	L	L	L	H	H	L
H	H	L	L	H	H	L
X	X	X	H	H	H	H

3-LINE TO 8-LINE DECODER OR  
1-LINE TO 8-LINE DEMULTIPLEXER

INPUTS			OUTPUTS							
SELECT	STROBE or DATA	Gt	(0)	(1)	(2)	(3)	(4)	(5)	(6)	(7)
C†	B	A	2Y0	2Y1	2Y2	2Y3	1Y0	1Y1	1Y2	1Y3
X	X	X	H	H	H	H	H	H	H	H
L	L	L	L	L	H	H	H	H	H	H
L	L	H	L	H	L	H	H	H	H	H
L	H	L	L	H	L	H	H	H	H	H
L	H	H	L	H	H	L	H	H	H	H
H	L	L	L	H	H	H	L	H	H	H
H	L	H	L	H	H	H	H	L	H	H
H	H	L	L	H	H	H	H	H	L	H
H	H	H	L	H	H	H	H	H	H	L

† C = inputs 1C and 2C connected together

‡ G = inputs 1G and 2G connected together

## ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	TTL	LS	ALS	UNIT
I <sub>CC</sub>	MAX	40	10	9	mA
I <sub>OL</sub>	MAX	16	8	8	mA
V <sub>OH</sub>	MAX	5.5	5.5	5.5	mA

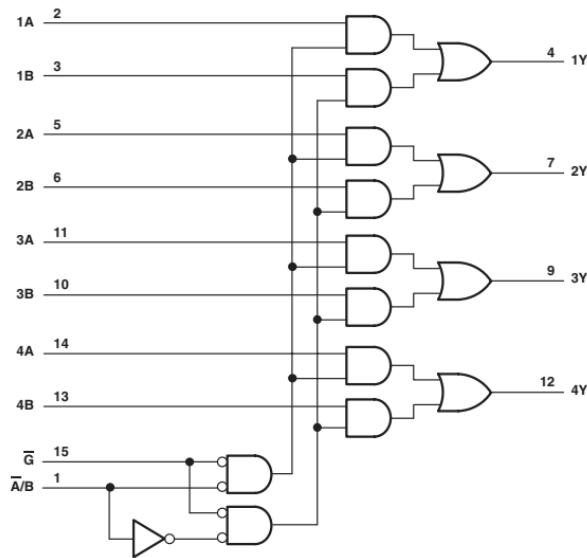
## SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	TTL	LS	ALS
I <sub>PLH</sub>	$\frac{2\bar{C}}{1\bar{G} \text{ or } 2\bar{G}}$	Y	MAX	23	40	38
I <sub>PHL</sub>	A or B	Y	MAX	30	51	22
I <sub>PLH</sub>	A or B	Y	MAX	34	46	55
I <sub>PHL</sub>	1C	Y	MAX	34	51	25
I <sub>PLH</sub>	1C	Y	MAX	27	48	50
I <sub>PHL</sub>	1C	Y	MAX	33	48	23

UNIT: ns

## QUADRUPLE 2-LINE TO 1-LINE DATA SELECTORS/MULTIPLEXERS

Logic Diagram (SN74LV/SN74HC)



FUNCTION TABLE (SN74)

INPUTS			OUTPUT
STROBE	SELECT	A B	
H	X	X X	L
L	L	L X	L
L	L	H X	H
L	H	X L	L
L	H	X H	H

## ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	TTL	LS	S	ALS	AS	F	SN74 HC	CD74 HC	SN74 HCT	UNIT
I <sub>CC</sub>	MAX	48	16	78	11	28	23	0.08	0.16	0.08	mA
I <sub>OH</sub>	MAX	-0.8	-0.4	-1	-0.4	-2	-1	-6	-4	-6	mA
IO <sub>L</sub>	MAX	16	8	20	8	20	20	6	4	6	mA

PARAMETER	MAX or MIN	CD74 HCT	CD74 AC	CD74 ACT	AHC	AHCT	LV 3V	LV 5V	LVC 3V	UNIT
I <sub>CC</sub>	MAX	0.16	0.16	0.16	0.04	0.02	-	0.02	0.01	mA
I <sub>OH</sub>	MAX	-4	-24	-24	-8	-8	-6	-12	-24	mA
IO <sub>L</sub>	MAX	4	24	24	8	8	6	12	24	mA

## SWITCHING CHARACTERISTICS

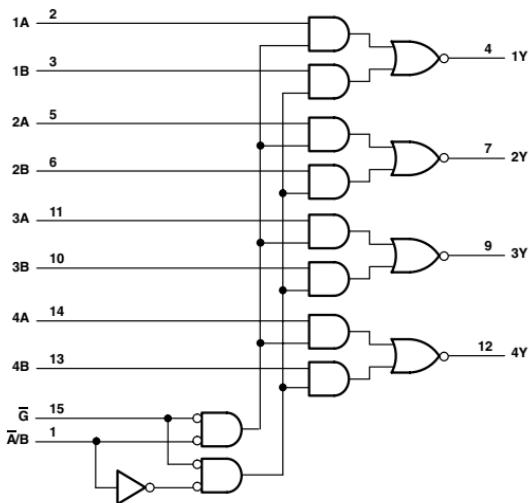
PARAMETER	INPUT	OUTPUT	MAX or MIN	TTL	LS	S	ALS	AS	F	SN74 HC	CD74 HC	SN74 HCT
I <sub>PLH</sub>				14	14	7.5	14	6	6.5	32	38	35
I <sub>PHL</sub>				14	14	6.5	12	5.5	7	32	38	35
I <sub>PLH</sub>				20	20	12.5	20	10.5	11	29	41	33
I <sub>PHL</sub>				21	21	12	13	7.5	7	29	41	33
I <sub>PLH</sub>				23	23	15	24	11	11	31	44	40
I <sub>PHL</sub>				27	27	15	17	10	8	31	44	40
PARAMETER	INPUT	OUTPUT	MAX or MIN	CD74 HCT	CD74 AC	CD74 ACT	AHC	AHCT	LV 3V	LV 5V	LVC 3V	
I <sub>PLH</sub>				38	8.5	9.5	9.5	9.8	15	9.5	5.2	
I <sub>PHL</sub>				38	8.5	9.5	9.5	9.8	15	9.5	5.2	
I <sub>PLH</sub>				41	13.5	13.5	12	12	19.5	12	6.5	
I <sub>PHL</sub>				41	13.5	13.5	12	12	19.5	12	6.5	
I <sub>PLH</sub>				44	14.5	14.5	11.5	12	19	11.5	6.8	
I <sub>PHL</sub>				44	14.5	14.5	11.5	12	19	11.5	6.8	

UNIT: ns

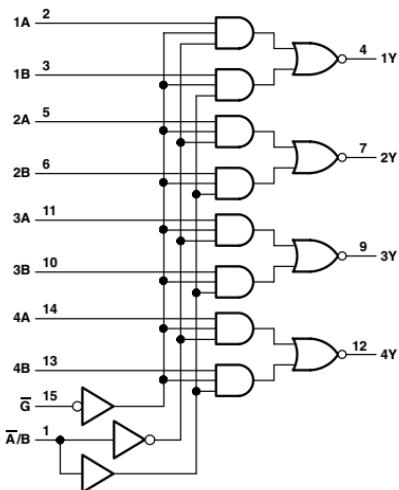
## QUADRUPLE 2-LINE TO 1-LINE DATA SELECTORS/MULTIPLEXERS

- Buffered Inputs and Outputs

Logic Diagram (SN74HC, ALS, LS)



Logic Diagram (SN74AS)



FUNCTION TABLE (SN74)

INPUTS			OUTPUT
STROBE	SELECT	A B	
H	X	X X	H
L	L	L X	H
L	L	H X	L
L	H	X L	H
L	H	X H	L

## ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	LS	S	ALS	AS	F	SN74 HC	CD74 HC	CD74 HCT	UNIT
I <sub>CC</sub>	MAX	11	81	10	22.5	15	0.08	0.16	0.16	mA
I <sub>OH</sub>	MAX	-0.4	-1	-0.4	-2	-1	-6	-4	-4	mA
IOL	MAX	8	20	8	20	20	6	4	4	mA

PARAMETER	MAX or MIN	CD74 AC	CD74 ACT	AHC	AHCT	UNIT
I <sub>CC</sub>	MAX	0.16	0.16	0.04	0.02	mA
I <sub>OH</sub>	MAX	-24	-24	-8	-8	mA
IOL	MAX	24	24	8	8	mA

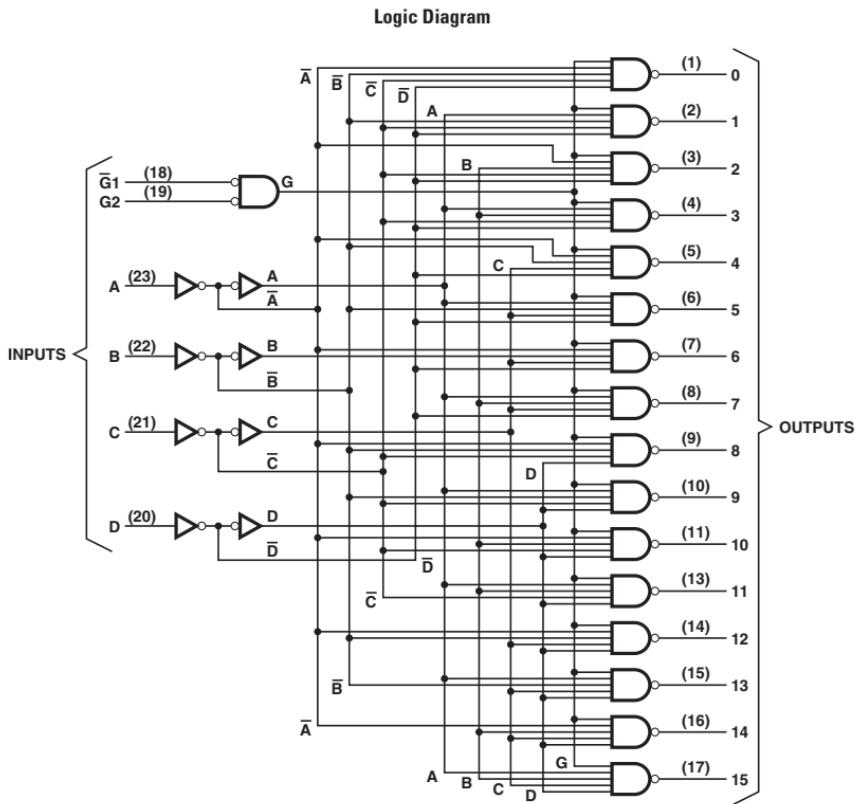
## SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	LS	S	ALS	AS	F	SN74 HC	CD74 HC	CD74 HCT
I <sub>PLH</sub>	DATA	Y	MAX	12	6	15	5	7	32	42	42
				15	6	8	4.5	4.5	32	42	42
I <sub>PHL</sub>	STROBE	Y	MAX	17	11.5	18	6.5	7	29	48	48
				24	12	18	10	6.5	29	48	48
I <sub>PLH</sub>	SELECT	Y	MAX	20	12	18	9.5	9.5	31	45	45
				24	12	18	10.5	7	31	45	45

PARAMETER	INPUT	OUTPUT	MAX or MIN	CD74 AC	CD74 ACT	AHC	AHCT
I <sub>PLH</sub>	DATA	Y	MAX	8	9.2	9.5	9.8
				8	9.2	9.5	9.8
I <sub>PHL</sub>	STROBE	Y	MAX	11.9	12.4	12	12
				11.9	12.4	12	12
I <sub>PLH</sub>	SELECT	Y	MAX	12.9	13.5	11.5	12
				12.9	13.5	11.5	12

UNIT: ns

## 4-LINE TO 16-LINE DECODERS/DEMULTIPLEXERS WITH OPEN-COLLECTOR OUTPUTS



## FUNCTION TABLE

#### ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

ELECTRICAL CHARACTERISTICS AND REQUIREMENTS			
PARAMETER	MAX or MIN	TTL	UNIT
I <sub>CC</sub>	MAX	56	mA
I <sub>OL</sub>	MAX	16	mA

### **SWITCHING CHARACTERISTICS**

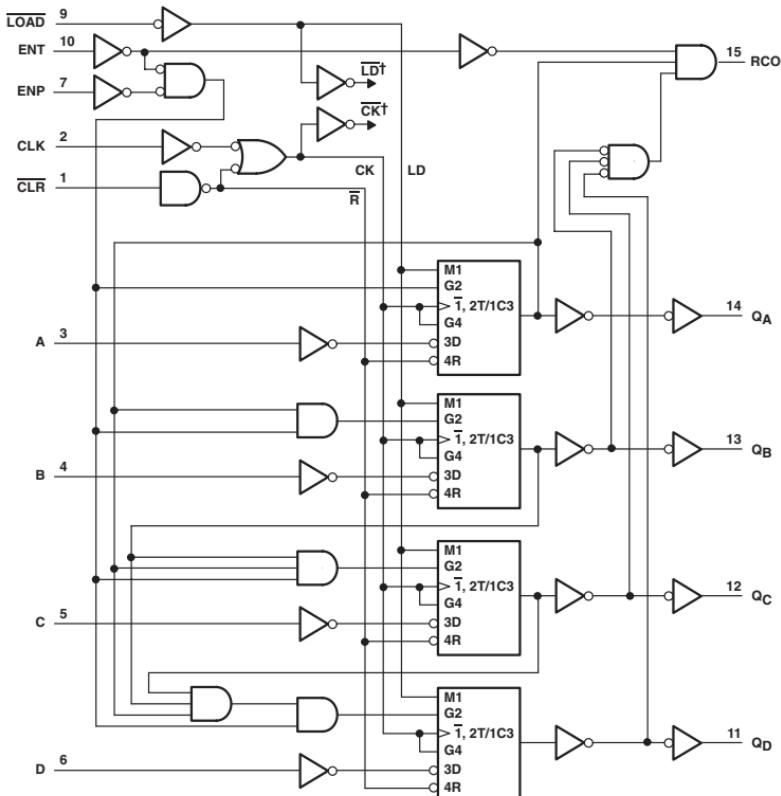
SWITCHING CHARACTERISTICS				
PARAMETER	INPUT	OUTPUT	MAX or MIN	TTL
IPHL	INPUT	ANY	MAX	36
IPHL				36
IPHL	STROBE	ANY	MAX	25
IPHL				36

UNIT: ns

## 4-BIT SYNCHRONOUS BINARY COUNTERS

- Asynchronous Clear Function
- Carry Output for n-Bit Cascading

Logic Diagram (SN74)



† For simplicity, routing of complementary signals  $\overline{LD}$  and  $\overline{CK}$  is not shown on this overall logic diagram. The uses of these signals are shown on the logic diagram of the D/T flip-flops.

FUNCTION TABLE (SN74)

INPUTS					OUTPUTS				FUNCTION
CLR	LOAD	ENP	ENT	CLK	QA	QB	QC	QD	
L	X	X	X	X	L	L	L	L	Reset to "0"
H	L	X	X		A	B	C	D	Preset Data
H	H	X		L					No Change
H	H	L	X						No Change
H	H	H	H						Count up
H	X	X	X						Count
									No Count

## ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	TTL	LS	ALS	AS	F	SN74 HC	CD74 HC	CD74 HCT	CD74 AC	CD74 ACT	LV 3V	LV 5V	UNIT
I <sub>CC</sub>	MAX	101	32	21	53	55	0.08	0.16	0.16	0.08	0.08	-	0.02	mA
I <sub>OH</sub>	MAX	-0.8	-0.4	-0.4	-2	-1	4	-4	-4	-24	-24	-6	-12	mA
I <sub>OL</sub>	MAX	16	8	8	20	20	-4	4	4	24	24	-6	12	mA

## TIMING REQUIREMENTS AND SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	TTL	LS	ALS	AS	F	SN74 HC	CD74 HC	CD74 HCT
fmax			MIN	25	25	40	75	90	25	20	20
t <sub>w</sub>	CLOCK		MIN	25	25	-	-	7	20	24	24
	CLEAR		MIN	20	20	15	8	5	20	30	30
ts <sub>u</sub>	INPUT		MIN	20	20	15	8	5	38	18	15
	ENABLE		MIN	20	20	15	8	11.5	43	15	20
	LOAD		MIN	25	20	15	8	11.5	34	18	18
	CLEAR INACTIVE		MIN	20	25	10	8	-	31	-	-
t <sub>h</sub>			MIN	0	3	0	0	2	0	3	5
t <sub>PLH</sub>	CLOCK	RIPPLE CARRY (CD74HC/HCT: TC)	MAX	35	35	20	16.5	15	54	56	63
t <sub>PLH</sub>			MAX	35	35	20	12.5	15	54	56	63
t <sub>PLH</sub>	CLOCK	ANY Q	MAX	25	24	15	7	9.5	51	56	59
t <sub>PLH</sub>			MAX	29	27	20	13	11	51	56	59
t <sub>PLH</sub>	ENABLE	RIPPLE CARRY (CD74HC/HCT: TC)	MAX	16	14	13	9	8.5	49	36	48
t <sub>PLH</sub>		ANY Q	MAX	16	14	13	8.5	8.5	49	36	48
t <sub>PLH</sub>	CLEAR	RIPPLE CARRY (CD74HC/HCT: TC)	MAX	-	-	23	12.5	11.5	55	63	75

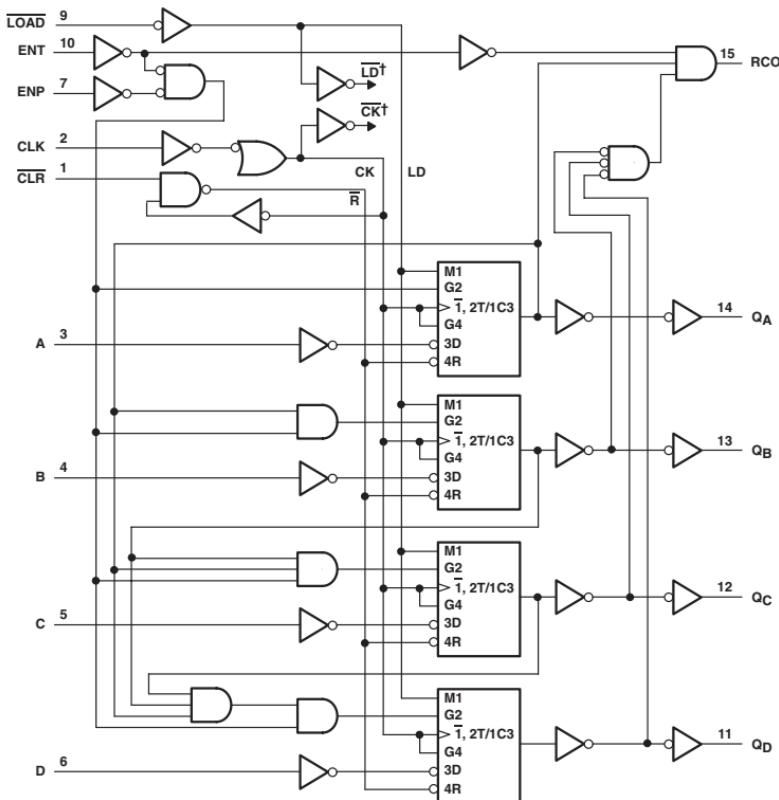
PARAMETER	INPUT	OUTPUT	MAX or MIN	CD74 AC	CD74 ACT	LV 3V	LV 5V
fmax			MIN	90	80	50	85
t <sub>w</sub>	CLOCK		MIN	5.5	6.2	5	5
	CLEAR		MIN	5	6	5	5
ts <sub>u</sub>	INPUT		MIN	5	5	6.5	4.5
	ENABLE		MIN	-	-	9	6
	LOAD		MIN	6	6	9.5	6
	CLEAR INACTIVE		MIN	-	-	2.5	1.5
t <sub>h</sub>			MIN	0	0	1	1
t <sub>PLH</sub>	CLOCK	RIPPLE CARRY (CD74HC/HCT: TC)	MAX	16.7	16.7	23.5	14
t <sub>PLH</sub>			MAX	16.7	16.7	23.5	14
t <sub>PLH</sub>	CLOCK	ANY Q	MAX	16.5	16.5	18.5	11.5
t <sub>PLH</sub>			MAX	16.5	16.5	18.5	11.5
t <sub>PLH</sub>	ENABLE	RIPPLE CARRY (CD74HC/HCT: TC)	MAX	10.3	10.8	18	11.5
t <sub>PLH</sub>		ANY Q	MAX	10.3	10.8	18	11.5
t <sub>PLH</sub>	CLEAR	RIPPLE CARRY (CD74HC/HCT: TC)	MAX	16.5	16.5	19.5	12.5

UNIT fmax : MHz, other : ns

## 4-BIT SYNCHRONOUS BINARY COUNTERS

- Synchronous Clear Function
- Carry Output for n-Bit Cascading

Logic Diagram (SN74LV)



<sup>†</sup> For simplicity, routing of complementary signals  $\overline{LD}$  and  $\overline{CK}$  is not shown on this overall logic diagram. The uses of these signals are shown on the logic diagram of the D/T flip-flops.

FUNCTION TABLE (SN74)

INPUTS					OUTPUTS				FUNCTION	
CLR	LOAD	ENP	ENT	CLK	QA	QB	QC	QD		
L	X	X	X	X	L	L	L	L	Reset to "0"	
H	L	X	X		A	B	C	D	Preset data	
H	H	X	X		No change				No count	
H	H	L	X		No change				No count	
H	H	H	H		Count up				Count	
H	X	X	X		No change				No count	

## ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	TTL	LS	S	ALS	AS	F	SN74 HC	CD74 HC	CD74 HCT	CD74 AC	CD74 ACT	LV 3V	LV 5V	UNIT
I <sub>CC</sub>	MAX	101	32	160	21	53	55	0.08	0.16	0.16	0.16	0.16	-	0.02	mA
I <sub>OH</sub>	MAX	-0.8	-0.4	-1	-0.4	-2	-1	4	-4	-4	-24	-24	-6	-12	mA
I <sub>OL</sub>	MAX	16	8	20	8	20	20	-4	4	4	24	24	-6	12	mA

## TIMING REQUIREMENTS AND SWITCHING CHARACTERISTICS

PARAMETER		INPUT		OUTPUT		MAX or MIN	TTL	LS	S	ALS	AS	F	SN74 HC
fmax						MIN	25	25	40	40	75	90	25
tw	CLOCK					MIN	25	25	10	-	-	7	20
	CLEAR					MIN	20	20	10	12.5	6.7	-	-
tsu	INPUT					MIN	20	20	4	15	8	5	38
	ENABLE					MIN	20	20	12	15	8	11.5	43
	LOAD					MIN	25	20	14	15	8	11.5	34
	CLEAR					MIN	20	20	14	15	12	-	40
th						MIN	0	3	3	0	0	2	0
t <sub>PLH</sub>		CLOCK		ripple carry		MAX	35	35	25	20	16.5	15	54
t <sub>PLHL</sub>						MAX	35	35	25	20	12.5	15	54
t <sub>PLH</sub>		CLOCK		any Q		MAX	25	24	15	15	7	9.5	51
t <sub>PLH</sub>						MAX	29	27	15	20	13	11	51
t <sub>PLH</sub>		ENABLE		ripple carry		MAX	16	14	15	13	9	8.5	49
t <sub>PLHL</sub>						MAX	16	14	15	13	8.5	8.5	49

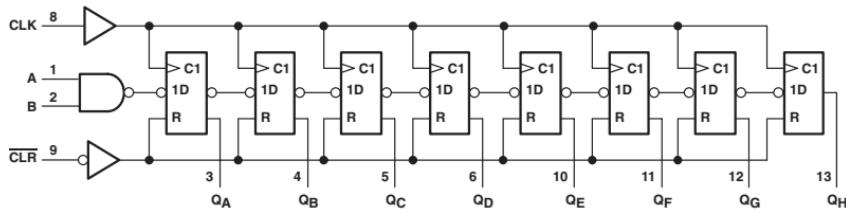
PARAMETER		INPUT		OUTPUT		MAX or MIN	CD74 HC	CD74 HCT	CD74 AC	CD74 ACT	LV 3V	LV 5V
fmax						MIN	20	20	90	80	50	85
tw	CLOCK					MIN	24	24	5.5	6.2	5	5
	CLEAR					MIN	-	-	-	-	-	-
tsu	INPUT					MIN	18	15	5	5	6.5	4.5
	ENABLE					MIN	15	20	5	6	9	6
	LOAD					MIN	18	18	6	7.5	9.5	6
	CLEAR					MIN	20	20	6	7.5	4	3.5
th						MIN	3	5	0	0	1	1
t <sub>PLH</sub>		CLOCK		ripple carry		MAX	56	63	16.7	16.7	23.5	14
t <sub>PLHL</sub>						MAX	56	63	16.7	16.7	23.5	14
t <sub>PLH</sub>		CLOCK		any Q		MAX	56	59	16.5	16.5	18.5	11.5
t <sub>PLH</sub>						MAX	56	59	16.5	16.5	18.5	11.5
t <sub>PLH</sub>		ENABLE		ripple carry		MAX	36	48	10.3	10.8	18	11.5
t <sub>PLHL</sub>						MAX	36	48	10.3	10.8	18	11.5

UNIT fmax : MHz, other : ns

## 8-BIT PARALLEL-OUT SERIAL SHIFT REGISTERS

- AND-Gated (Enable/Disable) Serial Inputs
- Fully Buffered Clock and Serial Inputs

Logic Diagram (SN74)



**FUNCTION TABLE (SN74)**

INPUTS			OUTPUTS				
CLEAR	CLOCK	A B	Q <sub>A</sub>	Q <sub>B</sub>	...	Q <sub>H</sub>	
L	X	X X	L	L	...	L	
H	L	X X	Q <sub>A0</sub>	Q <sub>B0</sub>	...	Q <sub>H0</sub>	
H	↑	H H	H	Q <sub>A1</sub>	...	Q <sub>Gn</sub>	
H	↑	L X	L	Q <sub>A1</sub>	...	Q <sub>Gn</sub>	
H	↑	X L	L	Q <sub>A1</sub>	...	Q <sub>Gn</sub>	

**ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS**

PARAMETER	MAX or MIN	TTL	LS	ALS	SN74 HC	CD74 HC	CD74 HCT	CD74 AC	CD74 ACT	LV 3V	LV 5V	UNIT
I <sub>CC</sub>	MAX	54	27	24	0.08	0.16	0.16	0.16	0.16	-	0.02	mA
I <sub>OH</sub>	MAX	-0.4	-0.4	-0.4	-4	-4	-4	-24	-24	-6	-12	mA
I <sub>OL</sub>	MAX	8	8	8	4	4	4	24	24	6	12	mA

**TIMING REQUIREMENTS AND SWITCHING CHARACTERISTICS**

PARAMETER	INPUT	OUTPUT	MAX or MIN	TTL	LS	ALS	SN74 HC	CD74 HC	CD74 HCT	CD74 AC	CD74 ACT
fmax			MIN	25	25	50	25	20	18	75	70
			MIN	20	20	16	25	18	27	4.5	4.5
			MIN	20	20	10	20	24	27	6.7	7.1
			MIN	20	20	10	20	24	27	6.7	7.1
			MIN	15	15	6	25	18	18	2.5	2.5
			MIN	20	20	8	25	18	18	2.5	2.5
tsu	DATA		MIN	5	5	2	5	4	4	2.5	3
	CLEAR INACTIVE		MAX	42	36	20	51	42	57	13.9	15.8
			MAX	30	27	16	44	51	54	12.5	14.9
th	CLEAR	Q	MAX	37	32	17	44	51	54	12.5	14.9
	CLOCK	Q	MAX								
			MAX								

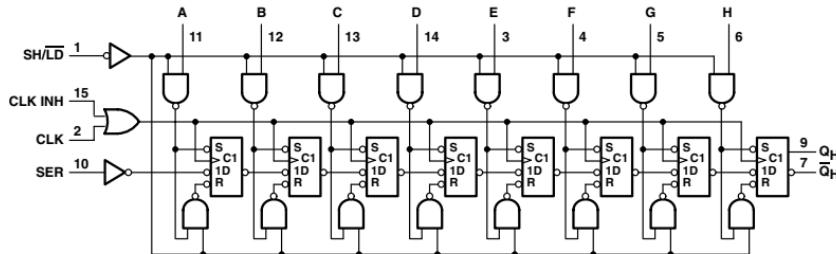
PARAMETER	INPUT	OUTPUT	MAX or MIN	LV 3V	LV 5V
fmax			MIN	45	75
			MIN	5	5
			MIN	5	5
			MIN	5	5
			MIN	6	4.5
			MIN	2.5	2.5
tsu	DATA		MIN	0	1
	CLEAR INACTIVE		MAX	18.5	12.5
			MAX	18.5	12.5
th	CLEAR	Q	MAX	18.5	12.5
	CLOCK	Q	MAX	18.5	12.5
			MAX	18.5	12.5

UNIT fmax : MHz, other : ns

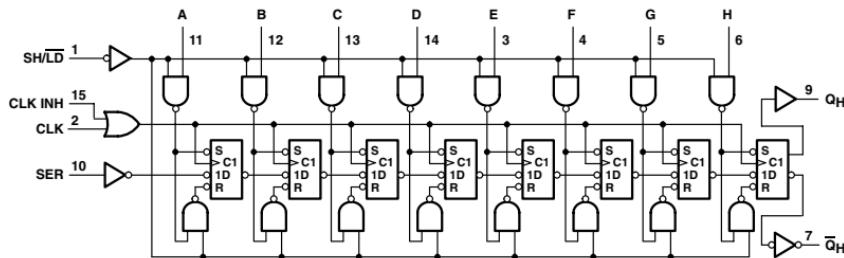
## PARALLEL-LOAD 8-BIT SHIFT REGISTERS

- Complementary Outputs: Serial (QH,  $\bar{Q}_H$ )
- Direct Overriding Load (Data) Inputs
- Parallel-to-Serial Data Conversion

Logic Diagram (SN74LV, ALS, LS)



Logic Diagram (SN74HC)



FUNCTION TABLE (SN74)

SHIFT/ LOAD	CLOCK INHIBIT	INPUTS			INTERNAL OUTPUTS		OUTPUT Q <sub>H</sub>
		CLOCK	SERIAL	PARALLEL A...H	Q <sub>A</sub>	Q <sub>B</sub>	
L	X	X	X	a...h	a	b	h
H	L	L	X	X	Q <sub>A0</sub>	Q <sub>B0</sub>	Q <sub>H0</sub>
H	L	↑	H	X	H	Q <sub>An</sub>	Q <sub>Gn</sub>
H	L	↑	L	X	L	Q <sub>An</sub>	Q <sub>Gn</sub>
H	H	X	X	X	Q <sub>A0</sub>	Q <sub>B0</sub>	Q <sub>H0</sub>

## ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	TTL	LS	ALS	SN74 HC	CD74 HC	CD74 HCT	LV 3V	LV 5V	UNIT
I <sub>CC</sub>	MAX	63	30	24	0.08	0.16	0.16	-	0.02	mA
I <sub>OH</sub>	MAX	-0.8	-0.4	-0.4	-4	-4	-4	-6	-12	mA
I <sub>OL</sub>	MAX	16	8	8	4	4	4	6	12	mA

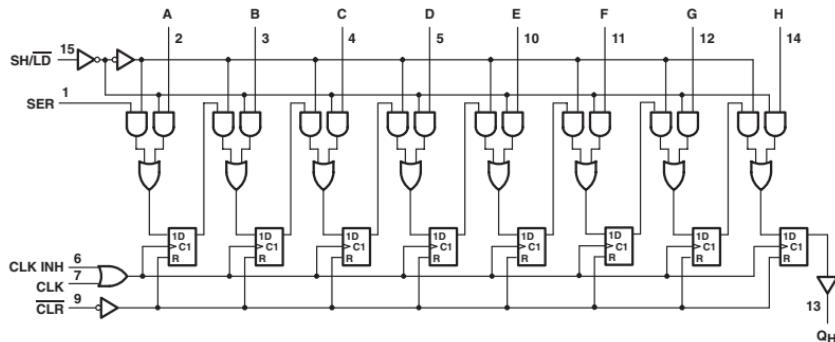
## TIMING REQUIREMENTS AND SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	TTL	LS	ALS	SN74 HC	CD74 HC	CD74 HCT	LV 3V	LV 5V	
fmax			MIN	20	25	45	25	20	18	50	85	
t <sub>w</sub>	CLOCK (CD74: CP)		High	MIN	25	15	11	20	24	27	7	
	Low		MIN	25	25	11	20	24	27	7	4	
t <sub>su</sub>	SH/ $\overline{LD}$ "L" (CD74: PL)		High	MIN	15	25	-	-	-	-	-	
	Low		MIN	15	17	12	20	24	30	9	6	
t <sub>th</sub>	CLK INH (CD74: CE)			MIN	30	30	11	25	24	30	5	
	DATA				10	10	10	25	24	30	8.5	
	SER (CD74: DS)				20	20	10	10	24	30	6	
	SH/ $\overline{LD}$ "H"				45	45	10	20	-	-	6	
UNIT fmax : MHz, other : ns				MIN	0	0	4	5	11	11	0.5	
t <sub>PLH</sub>	CLOCK (CD74: CP)	(Q <sub>H</sub> or $\overline{Q}_H$ (CD74: Q <sub>7</sub> or $\overline{Q}_7$ )	MAX	24	25	13	38	50	60	16.9	13.5	
				31	25	14	38	50	60	16.9	13.5	
t <sub>PLH</sub>	SH/ $\overline{LD}$ (CD74: PL)	(Q <sub>H</sub> or $\overline{Q}_H$ (CD74: Q <sub>7</sub> or $\overline{Q}_7$ )	MAX	31	35	20	38	53	60	22	13.5	
				40	35	22	38	53	60	22	13.5	
t <sub>PLH</sub>	H (CD74: D <sub>7</sub> )	(Q <sub>H</sub> (CD74: Q <sub>7</sub> )	MAX	17	25	13	38	45	53	20	12.5	
				36	30	16	38	45	53	20	12.5	
t <sub>PLH</sub>	H (CD74: D <sub>7</sub> )	$\overline{Q}_H$ (CD74: Q <sub>7</sub> )	MAX	27	30	15	38	45	53	20	12.5	
				27	25	16	38	45	53	20	12.5	

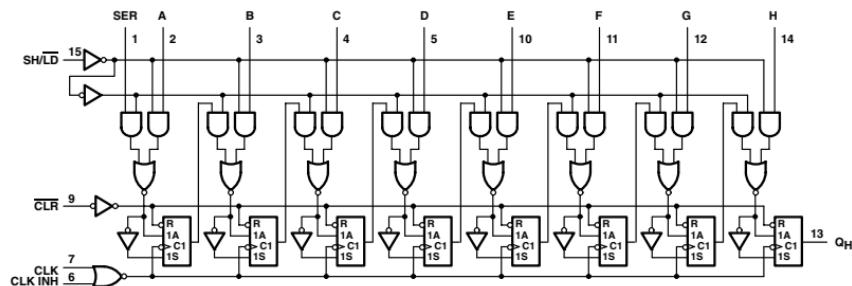
## 8-BIT PARALLEL-LOAD SHIFT REGISTERS

- Synchronous Load
- Direct Overriding Clear
- Parallel-to-Serial Conversion

Logic Diagram (SN74LV, HC)



Logic Diagram (SN74ALS, LS)



FUNCTION TABLE (SN74)

INPUTS						INTERNAL OUTPUTS		OUTPUT
CLEAR	SHIFT/ LOAD	CLOCK INHIBIT	CLOCK	SERIAL	PARALLEL A...H	QA	QB	QH
L	X	X	X	X	X	L	L	L
H	X	L	L	X	X	QA0	QB0	QH0
H	L	L	↑	X	a..h	a	b	h
H	H	L	↑	H	X	H	QAn	QGn
H	H	L	↑	L	X	L	QAn	QGn
H	X	H	↑	X	X	QA0	QB0	QH0

## ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	TTL	LS	ALS	F	SN74 HC	CD74 HC	CD74 HCT	LV 3V	LV 5V	UNIT
Icc	MAX	127	32	24	60	0.08	0.16	0.16	-	0.02	mA
IoH	MAX	-0.8	-0.4	-0.4	-1	-4	-4	-4	-6	-12	mA
IoL	MAX	16	8	8	20	4	4	4	6	12	mA

## TIMING REQUIREMENTS AND SWITCHING CHARACTERISTICS

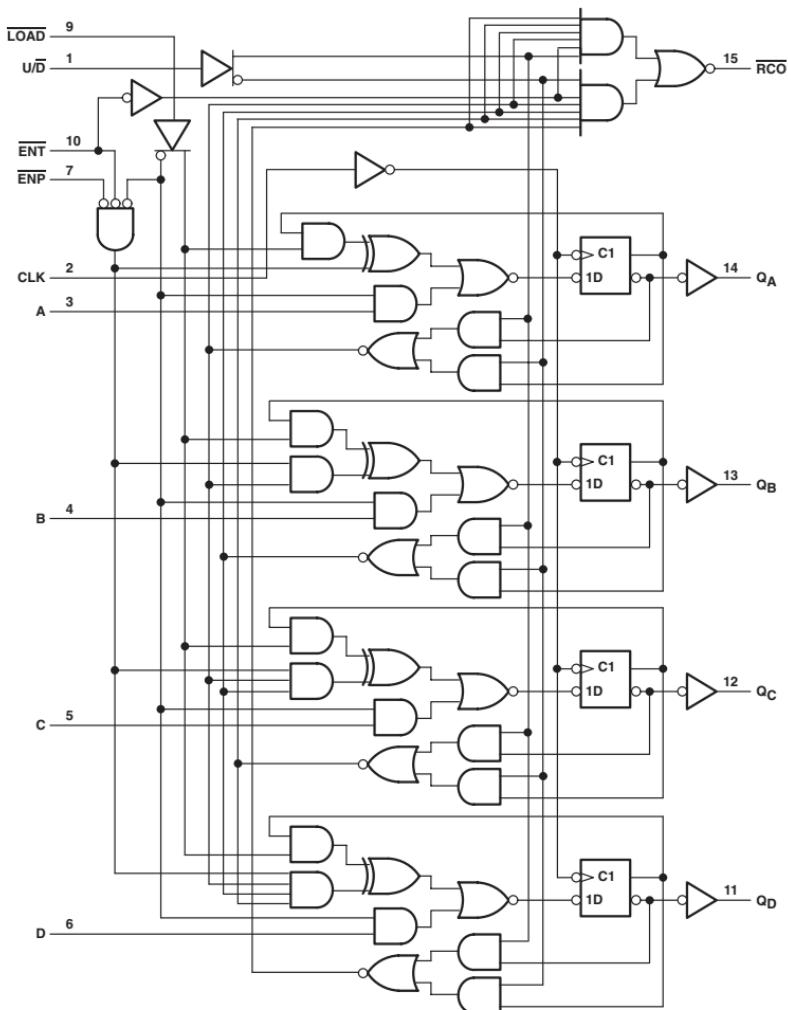
PARAMETER	INPUT	OUTPUT	MAX or MIN	TTL	LS	ALS	F	SN74 HC	CD74 HC	CD74 HCT	LV 3V	LV 5V
fmax			MIN	25	25	45	110	25	20	16	50	85
tw	CLOCK (CD74: CP)  CLEAR (CD74: MR)		MIN	20	20	10	3.5	20	24	30	7	4
				20	25	9	4	25	30	53	7	5
				30	30	16	4	36	44	45	6	4
tsu	Mode Control		MIN	20	20	7	3	20	24	24	6	4.5
	DATA			0	0	3	0	0	1	0	0	1
th			MIN	0	0	3	0	0	1	0	0	1
tpHL	CLEAR	QH	MAX	35	30	14	9.5	30	48	60	18.5	12
	CLOCK	QH		30	25	13	14	38	48	60	21.5	13.5
		QH		26	20	12	9	38	48	60	21.5	13.5

INIT fmax = MHz, other = ns

## SYNCHRONOUS 4-BIT UP/DOWN BINARY COUNTERS

- Fully Synchronous Operation for Counting and Programming
- Internal Carry Look-Ahead Circuitry for Fast Counting
- Carry Output for n-Bit Cascading

Logic Diagram



## ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER		MAX or MIN	LS	S	ALS	AS	F	UNIT
I <sub>CC</sub>		MAX	45	160	25	63	52	mA
I <sub>OH</sub>	RCO	MAX	-0.4	-1	-0.4	-2	-1	mA
	Q	MAX	-1.2	-1	-0.4	-2	-1	mA
I <sub>OL</sub>	RCO	MAX	8	20	8	20	20	mA
	Q	MAX	24	20	8	20	20	mA

## TIMING REQUIREMENTS AND SWITCHING CHARACTERISTICS

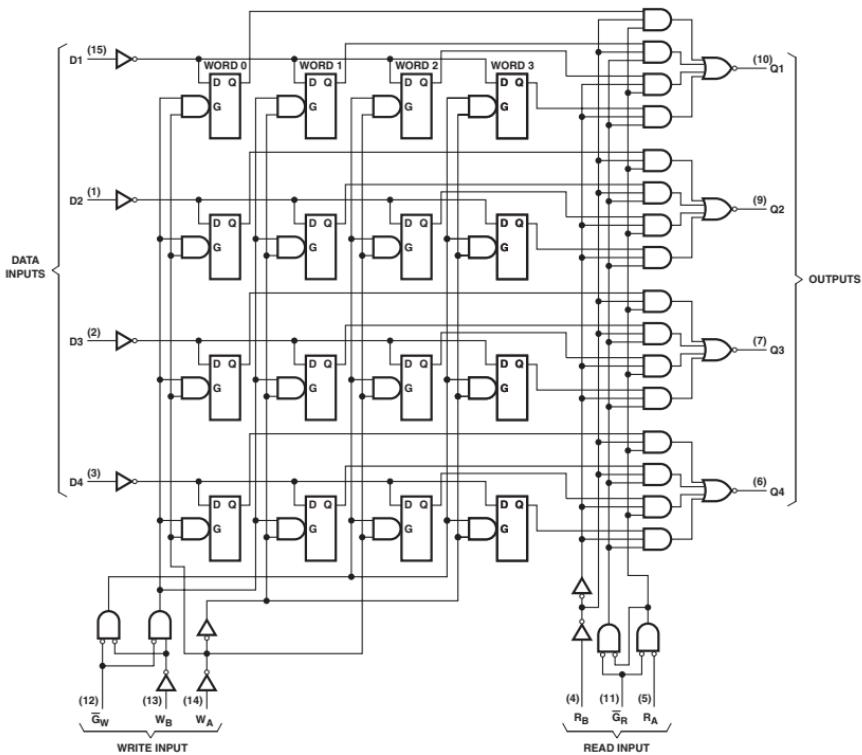
PARAMETER	INPUT	OUTPUT	MAX or MIN	LS	S	ALS	AS	F
f <sub>max</sub>			MIN	20	40	40	75	90
t <sub>PLH</sub>	CLK	RCO	MAX	40	21	20	16.5	17
				25	28	20	13	12.5
t <sub>PLH</sub>	CLK	ANY Q	MAX	25	15	15	13	9.5
				25	15	20	7	13
t <sub>PLH</sub>	ENT	RCO	MAX	25	12	13	9	7
				20	25	16	9	9
t <sub>PLH</sub>	U/D	RCO	MAX	35	15	19	12	12.5
				25	22	19	13	12

UNIT f<sub>max</sub> : MHz, other : ns

## 4-BY-4-REGISTER FILES WITH OPEN-COLLECTOR OUTPUTS

- Separate Read/Write Addressing Permits Simultaneous Reading and Writing
- Fast Access Times: Typically 20ns
- Expandable to 1024 Words of 4 Bits

Logic Diagram



WRITE FUNCTION TABLE

WRITE INPUTS			OUTPUTS			
W <sub>B</sub>	W <sub>A</sub>	W̄ <sub>B</sub>	0	1	2	3
L	L	L	Q = D	Q <sub>O</sub>	Q <sub>O</sub>	Q <sub>O</sub>
L	H	L	Q <sub>O</sub>	Q = D	Q <sub>O</sub>	Q <sub>O</sub>
H	L	L	Q <sub>O</sub>	Q <sub>O</sub>	Q = D	Q <sub>O</sub>
H	H	L	Q <sub>O</sub>	Q <sub>O</sub>	Q <sub>O</sub>	Q = D
X	X	H	Q <sub>O</sub>	Q <sub>O</sub>	Q <sub>O</sub>	Q <sub>O</sub>

READ FUNCTION TABLE

READ INPUTS			OUTPUTS			
R <sub>B</sub>	R <sub>A</sub>	R̄ <sub>B</sub>	Q1	Q2	Q3	Q4
L	L	L	W0B1	W0B2	W0B3	W0B4
L	H	L	W1B1	W1B2	W1B3	W1B4
H	L	L	W2B1	W2B2	W2B3	W2B4
H	H	L	W3B1	W3B2	W3B3	W3B4
X	X	H	H	H	H	H

## ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	TTL	LS	UNIT
I <sub>CC</sub>	MAX	150	40	mA
V <sub>DH</sub>	MAX	5.5	5.5	V
I <sub>OL</sub>	MAX	16	8	mA

## TIMING REQUIREMENTS AND SWITCHING CHARACTERISTICS

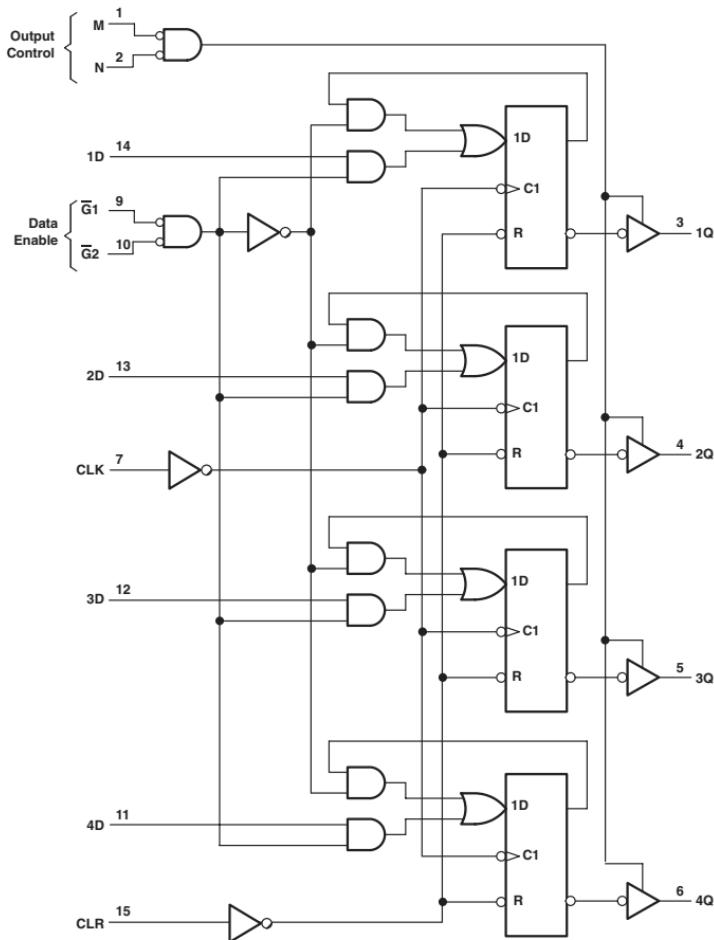
PARAMETER	INPUT	OUTPUT	MAX or MIN	TTL	LS
fmax			MIN		
t <sub>w</sub>			MIN	25	25
t <sub>su</sub>	D		MIN	10	10
	W		MIN	15	15
t <sub>h</sub>	D		MIN	15	15
	W		MIN	5	5
t <sub>PLH</sub>	READ ENABLE	Q	MAX	15	30
t <sub>PLH</sub>				30	30
t <sub>PLH</sub>	READ SELECT	Q	MAX	35	40
t <sub>PLH</sub>				40	40
t <sub>PLH</sub>	WRITE ENABLE	Q	MAX	40	45
t <sub>PLH</sub>				45	40
t <sub>PLH</sub>	DATA	Q	MAX	30	45
t <sub>PLH</sub>				45	35

UNIT fmax : MHz, other : ns

## 4-BIT D-TYPE REGISTERS WITH 3-STATE OUTPUTS

- 3-State Outputs Interface Directly
- Fully Independent Clock Virtually

Logic Diagram (SN74LS)



**FUNCTION TABLE (SN74LS)**

INPUTS				OUTPUT Q	
CLEAR	CLOCK	DATA G1	ENABLE G2	DATA D	Q
H	X	X	X	X	L
L	L	X	X	X	Q <sub>0</sub>
L	↑	H	X	X	Q <sub>0</sub>
L	↑	X	H	X	Q <sub>0</sub>
L	↑	L	L	L	L
L	↑	L	L	H	H

**ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS**

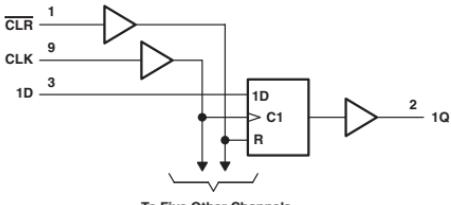
PARAMETER	MAX or MIN	TTL	LS	SN74 HC	CD74 HC	CD74 HCT	UNIT
I <sub>CC</sub>	MAX	72	24	0.08	0.16	0.16	mA
I <sub>OH</sub>	MAX	-5.2	-2.6	-6	-6	-6	mA
I <sub>OL</sub>	MAX	16	24	6	6	6	mA

**TIMING REQUIREMENTS AND SWITCHING CHARACTERISTICS**

PARAMETER	INPUT	OUTPUT	MAX or MIN	TTL	LS	SN74 HC	CD74 HC	CD74 HCT
fmax			MIN	25	25	25	20	13
t <sub>v</sub>			MIN	20	25	20	24	38
t <sub>su</sub>	DATA ENABLE		MIN	17	35	25	18	18
	DATA		MIN	10	17	25	18	27
t <sub>h</sub>	CLR INACTIVE		MIN	10	10	23	-	-
	DATA ENABLE		MIN	2	0	0	0	0
t <sub>PHL</sub>	DATA		MIN	10	3	0	3	0
	CLEAR	Q	MAX	27	35	38	53	66
t <sub>PLH</sub>			MAX	43	25	38	60	60
	CLOCK (CD74: CP)	Q	MAX	31	30	38	60	60
t <sub>PZH</sub>			MAX	30	23	38	45	45
	ENABLE	Q	MAX	30	27	38	45	45
t <sub>PZL</sub>			MAX	14	20	38	45	-
	DISABLE	Q	MAX	20	17	38	45	-

UNIT fmax : MHz, other : ns

- Buffered Clock and Direct Clear Inputs
- Fully Buffered Outputs for Maximum Isolation from External Disturbances



FUNCTION TABLE (SN74)

INPUTS		OUTPUT	
CLEAR	CLOCK	D	Q
L	X	X	L
H	↑	H	H
H	↑	L	L
L	L	X	Q <sub>0</sub>

## ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	TTL	LS	S	ALS	AS	F	SN74 HC	CD74 HC	UNIT
I <sub>CC</sub>	MAX	65	26	144	19	45	55	0.08	0.16	mA
I <sub>OH</sub>	MAX	-0.8	-0.4	-1	-0.4	-2	-1	-4	-4	mA
I <sub>OL</sub>	MAX	16	8	20	8	20	20	4	4	mA

PARAMETER	MAX or MIN	CD74 HCT	CD74 AC	CD74 ACT	AHC	AHCT	LV 3V	LV 5V	UNIT
I <sub>CC</sub>	MAX	0.16	0.16	0.16	0.04	0.04	-	0.02	mA
I <sub>OH</sub>	MAX	-4	-24	-24	-8	-8	-6	-12	mA
I <sub>OL</sub>	MAX	4	24	24	8	8	6	12	mA

## TIMING REQUIREMENTS AND SWITCHING CHARACTERISTICS

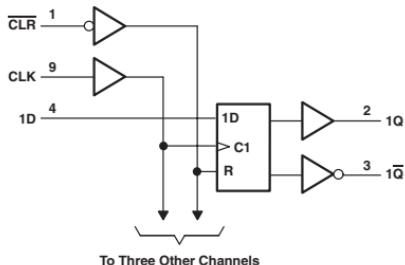
PARAMETER	INPUT	OUTPUT	MAX or MIN	TTL	LS	S	ALS	AS	F	SN74 HC	CD74 HC
t <sub>max</sub>				MIN	25	30	75	50	100	80	25
t <sub>w</sub>	CLR (MR) LOW			MIN	20	20	10	10	5	5	20
	CLK (CP) HIGH			MIN	20	20	7	10	4	4	24
	CLK (CP) LOW			MIN	20	20	7	10	6	6	24
t <sub>su</sub>	DATA INPUT			MIN	20	20	5	10	4	4.5	18
	CLR (MR) INACTIVE			MIN	25	25	5	6	6	5	25
				MIN	5	5	3	0	1	1	5
t <sub>PLH</sub>	CLR (MR)	ANY Q	MAX		25	-	-	18	-	-	45
t <sub>PHL</sub>			MAX		35	35	22	23	14	15	40
t <sub>PLH</sub>	CLK (CP)	ANY Q	MAX		30	30	12	15	8	9	40
t <sub>PHL</sub>			MAX		35	30	17	17	10	11	50

PARAMETER	INPUT	OUTPUT	MAX or MIN	CD74 HCT	CD74 AC	CD74 ACT	AHC	AHCT	LV 3V	LV 5V
t <sub>max</sub>				MIN	17	95	80	80	65	50
t <sub>w</sub>	CLR (MR) LOW			MIN	38	4	4	5	5	5
	CLK (CP) HIGH			MIN	30	5.2	6.2	5	5	5
	CLK (CP) LOW			MIN	30	5.2	6.2	5	5	5
t <sub>su</sub>	DATA INPUT			MIN	24	2	2	4.5	5	4.5
	CLR (MR) INACTIVE			MIN	-	-	-	2.5	3.5	2.5
				MIN	5	3	2.5	0.5	0	0.5
t <sub>PLH</sub>	CLR (MR)	ANY Q	MAX		66	14.5	15.5	-	-	11
t <sub>PHL</sub>			MAX		66	14.5	15.5	11	13	11
t <sub>PLH</sub>	CLK (CP)	ANY Q	MAX		60	13.5	14	10.5	10	16.5
t <sub>PHL</sub>			MAX		60	13.5	14	10.5	10	10.5

UNIT t<sub>max</sub> : MHz, other : ns

## QUADRUPLE D-TYPE FLIP-FLOPS WITH CLEAR

- Complementary Outputs ( $Q$ ,  $\bar{Q}$ )
- Buffered Clock and Direct Clear Inputs
- Asynchronous Clear Function



FUNCTION TABLE (SN74)

INPUTS		OUTPUTS	
CLEAR	CLOCK	D	$Q$ $\bar{Q}$
L	X	X	L H
H	↑	H	H L
H	↑	L	L H
H	L	X	$Q_0$ $\bar{Q}_0$

## ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	TTL	LS	S	ALS	AS	F	SN74 HC	CD74 HC	CD74 HCT	AC 11	CD74 AC	CD74 ACT	UNIT
$I_{CC}$	MAX	45	18	96	14	34	34	0.08	0.16	0.16	0.08	0.16	0.16	mA
$I_{OH}$	MAX	-0.8	-0.4	-1	-0.4	-2	-1	-4	-4	-4	-24	-24	-24	mA
$I_{OL}$	MAX	16	8	20	8	20	20	4	4	4	24	24	24	mA

PARAMETER	MAX or MIN	LV 3V	LV 5V	UNIT
$I_{CC}$	MAX	-	0.02	mA
$I_{OH}$	MAX	-6	-12	mA
$I_{OL}$	MAX	6	12	mA

## TIMING REQUIREMENTS AND SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	TTL	LS	S	ALS	AS	F	SN74 HC	CD74 HC
fmax			MIN	25	30	75	50	100	100	25	20
tw	CLR (MR) LOW			20	20	10	10	5	5	20	24
	CLK (CP) HIGH		MIN	20	20	7	10	4	4	20	24
	CLK (CP) LOW			20	20	7	10	5	5	20	24
	DATA INPUT		MIN	20	20	5	10	3	3	25	24
tsu	CLR (MR) INACTIVE			25	25	5	6	6	5	25	-
			MIN	5	5	3	0	1	1	0	5
	th			25	30	15	18	9	9	38	53
			MAX	35	30	22	23	13	13	38	53
tPLH	CLR (MR)	ANY Q or $\bar{Q}$		30	25	12	15	7.5	7.5	38	53
			MAX	35	25	17	17	10	9.5	38	53
	CLK (CP)	ANY Q or $\bar{Q}$									

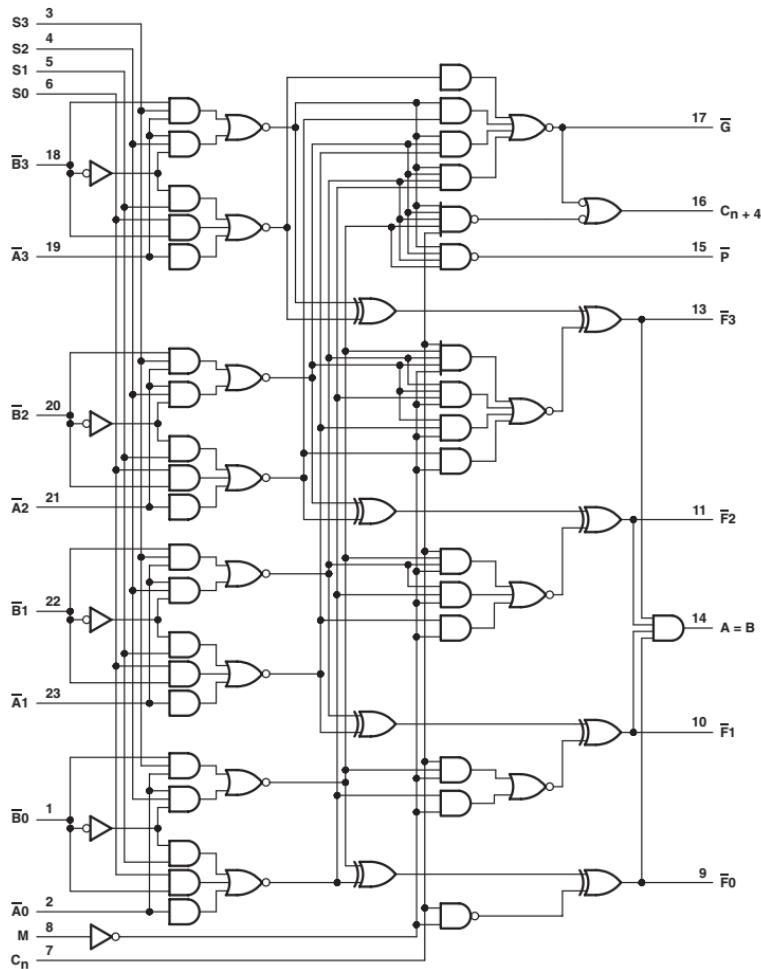
PARAMETER	INPUT	OUTPUT	MAX or MIN	CD74 HCT	AC 11	CD74 AC	CD74 ACT	LV 3V	LV 5V
fmax			MIN	16	125	100	114	45	75
tw	CLR (MR) LOW			30	4	4	4	5	5
	CLK (CP) HIGH		MIN	30	4	5	5	5	5
	CLK (CP) LOW			30	4	5	5	5	5
	DATA INPUT		MIN	30	5.5	2	2	5	4
tsu	CLR (MR) INACTIVE			-	5.5	-	-	5	5
			MIN	5	0.5	2	2	1	1
	th			53	6.8	12.2	13	15.5	9.5
			MAX	53	9.3	12.2	13	15.5	9.5
tPLH	CLR (MR)	ANY Q or $\bar{Q}$		50	6.9	12.2	11.5	17	10.5
			MAX	50	9.3	12.2	11.5	17	10.5
	CLK (CP)	ANY Q or $\bar{Q}$							

UNIT fmax : MHz, other : ns

## ARITHMETIC LOGIC UNITS/FUNCTION GENERATORS

- Full Look-Ahead for High-Speed Operations on Long Words
- Input Clamping Diodes Minimize Transmission-Line Effects

Logic Diagram



FUNCTION TABLE (ACTIVE LOW)

SELECTION	ACTIVE-LOW DATA			
	M = L; ARITHMETIC OPERATIONS			
S3 S2 S1 S0	M = H LOGIC FUNCTION	Cn = L (no carry)	Cn = H (with carry)	
L L L L	F = $\bar{A}$	F = A MINUS 1	F = A	
L L L H	F = AB	F = AB MINUS 1	F = AB	
L L H L	F = A + B	F = AB MINUS 1	F = AB	
L L H H	F = 1	F = MINUS 1 (2's COMP)	F = 0	
L H L L	F = A + B	F = A PLUS (A + $\bar{B}$ )	F = A PLUS (A + $\bar{B}$ ) PLUS 1	
L H L H	F = $\bar{B}$	F = AB PLUS (A + $\bar{B}$ )	F = AB PLUS (A + $\bar{B}$ ) PLUS 1	
L H H L	F = A $\oplus$ B	F = A MINUS B MINUS 1	F = A MINUS B	
L H H H	F = A + B	F = A + $\bar{B}$	F = (A + $\bar{B}$ ) PLUS 1	
H L L L	F = AB	F = A PLUS (A + B)	F = A PLUS (A + B) PLUS 1	
H L L H	F = A $\oplus$ B	F = A PLUS B	F = A PLUS B PLUS 1	
H L H L	F = B	F = AB PLUS (A + B)	F = AB PLUS (A + B) PLUS 1	
H L H H	F = A + B	F = (A + B)	F = (A + B) PLUS 1	
H H L L	F = 0	F = A PLUS A*	F = A PLUS A PLUS 1	
H H L H	F = AB	F = AB PLUS A	F = AB PLUS A PLUS 1	
H H H L	F = AB	F = AB PLUS A	F = AB PLUS A PLUS 1	
H H H H	F = A	F = A	F = A PLUS 1	

\*Each bit is shifted to the next more significant position.

FUNCTION TABLE (ACTIVE HIGH)

SELECTION	ACTIVE-HIGH DATA			
	M = L; ARITHMETIC OPERATIONS			
S3 S2 S1 S0	M = H LOGIC FUNCTION	$\bar{C}_n = H$ (no carry)	$\bar{C}_n = L$ (with carry)	
L L L L	F = A	F = A	F = A	
L L L H	F = A + B	F = A + B	F = A + B	
L L H L	F = AB	F = A + B	F = A + B	
L L H H	F = 0	F = MINUS 1 (2's COMPL)	F = 0	
L H L L	F = AB	F = A PLUS AB	F = A PLUS AB	
L H L H	F = $\bar{B}$	F = (A + B) PLUS AB	F = (A + B) PLUS AB	
L H H L	F = A $\oplus$ B	F = A MINUS B MINUS 1	F = A MINUS B	
L H H H	F = AB	F = AB MINUS 1	F = AB	
H L L L	F = A + B	F = A PLUS AB	F = A PLUS AB	
H L L H	F = $\bar{B}$	F = A PLUS B	F = A PLUS B	
H L H L	F = B	F = AB PLUS (A + B)	F = AB PLUS (A + B) PLUS 1	
H L H H	F = (A + B)	F = (A + B)	F = (A + B) PLUS 1	
H H L L	F = 1	F = A PLUS A PLUS 1	F = A PLUS A PLUS 1	
H H L H	F = A $\oplus$ B	F = (A + B) PLUS A	F = (A + B) PLUS A PLUS 1	
H H H L	F = A	F = (A + B)	F = (A + B) PLUS A	
H H H H	F = A	F = A	F = A	

\*Each bit is shifted to the next more significant position.

## ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER		MAX or MIN	TTL	LS	S	AS	UNIT
I <sub>CC</sub>		MAX	150	37	220	200	mA
I <sub>OH</sub>	All outputs except $A = B$	MAX	-0.8	-0.4	-1	-2	mA
	$\bar{G}$		-	-	-	-3	mA
I <sub>OL</sub>	All outputs except $\bar{G}$	MAX	16	8	20	20	mA
	$\bar{G}$		16	8	20	48	mA

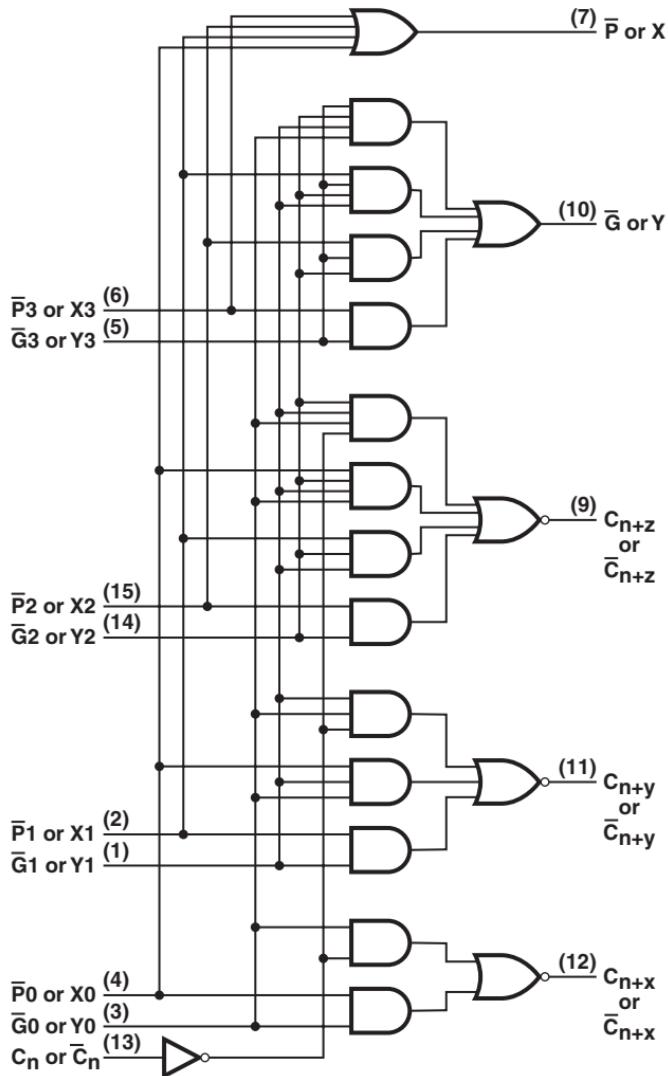
## SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	TTL	LS	S	AS
I <sub>PLH</sub>	$C_n$	$C_n + 4$	MAX	18	27	10.5	9
				19	20	10.5	9
I <sub>PHL</sub>	$\bar{A}, \bar{B}$	$C_n + 4$	MAX	43	38	18.5	12
				41	38	18.5	12
I <sub>PLH</sub>	$C_n$	$\bar{F}$	MAX	19	26	12	9
				18	20	12	9
I <sub>PHL</sub>	$\bar{A}_i, \bar{B}_i$	$\bar{F}_i$	MAX	42	32	16.5	9.5
				32	20	16.5	8

UNIT: ns

## LOOK-AHEAD CARRY GENERATOR

Logic Diagram



## FUNCTION TABLE

<b><math>\bar{G}</math> OUTPUTS</b>						<b><math>\bar{P}</math> OUTPUTS</b>						<b><math>C_{n+x}</math> OUTPUTS</b>					
INPUTS			OUTPUT			INPUTS			OUTPUT			INPUTS			OUTPUT		
$\bar{G}_3$	$\bar{G}_2$	$\bar{G}_1$	$P_3$	$P_2$	$P_1$	$\bar{P}_0$	$\bar{G}$	$\bar{P}_3$	$\bar{P}_2$	$\bar{P}_1$	$\bar{P}_0$	$\bar{P}$	$G_0$	$P_0$	$C_n$	$C_{n+x}$	
L	X	X	X	X	X	X	L	L	L	L	L	L	L	X	X	H	
X	L	X	X	L	X	X	L	All other combinations	X	L	H	H					
X	X	L	X	L	L	X	L	All other combinations	All other combinations	L	L	L					
X	X	X	L	L	L	L	H										
All other combinations							H										

<b><math>C_{n+y}</math> OUTPUTS</b>						<b><math>C_{n+z}</math> OUTPUTS</b>										
INPUTS			OUTPUT			INPUTS			OUTPUT							
$\bar{G}_1$	$\bar{G}_0$	$\bar{P}_1$	$P_0$	$C_n$	$C_{n+y}$	$\bar{G}_2$	$\bar{G}_1$	$\bar{G}_0$	$\bar{P}_2$	$\bar{P}_1$	$\bar{P}_0$	$C_n$	$C_{n+z}$			
L	X	X	X	X	H	L	X	X	X	X	X	H				
X	L	X	X	X	H	X	L	X	X	X	X	H				
X	X	L	L	H	H	X	X	L	L	X	X	H				
All other combinations					L	X	X	L	L	L	H	H				

### ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	TTL	S	AS	UNIT
$I_{CC}$	MAX	72	109	36	mA
$I_{OH}$	MAX	-0.8	-1	-2	mA
$I_{OL}$	MAX	16	20	20	mA

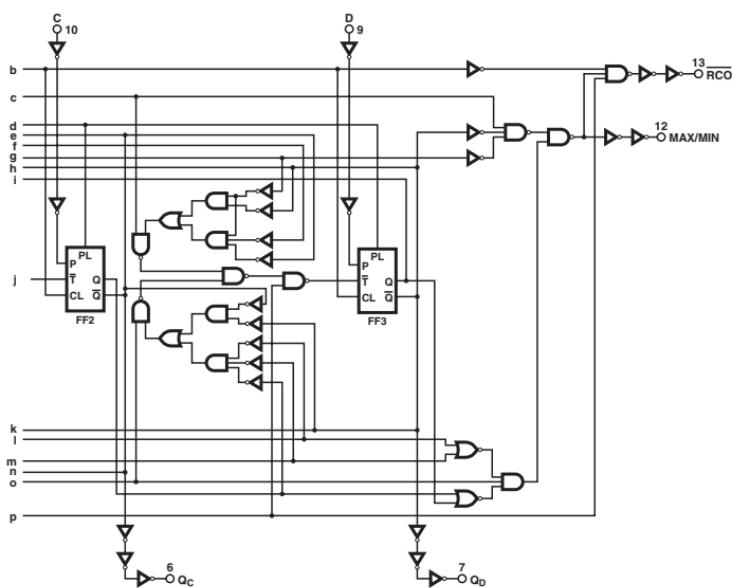
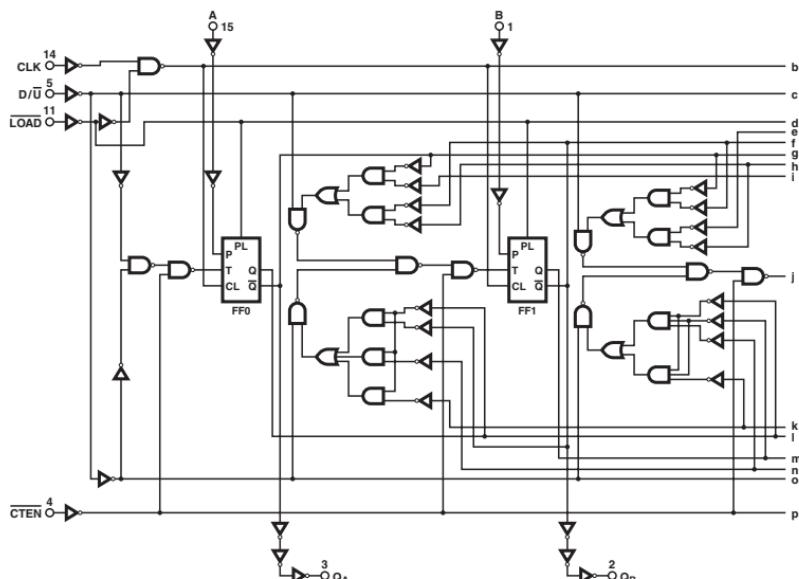
### SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	TTL	S	AS
$t_{PLH}$	$C_n$	$C_n + X, C_n + Y$ or $C_n + Z$	MAX	10	10	10
$t_{PHL}$				10.5	10.5	9.5
$t_{PLH}$	$P$ or $\bar{G}$	$C_n + X, C_n + Y$ or $C_n + Z$	MAX	7	7	10.5
$t_{PHL}$				7	7	6
$t_{PLH}$	$P$ or $\bar{G}$	$\bar{G}$	MAX	7.5	7.5	12
$t_{PHL}$				10.5	10.5	8
$t_{PLH}$	$\bar{P}$	$\bar{P}$	MAX	6.5	6.5	7.5
$t_{PHL}$				10	10	6

UNIT: ns

## SYNCHRONOUS 4-BIT UP/DOWN DECADE AND BINARY COUNTERS

Logic Diagram



FUNCTION TABLE

INPUTS				FUNCTION
LOAD	CTEN	D/ $\bar{U}$	CLK	
H	L	L	↑	Count up
H	L	H	↑	Count down
L	X	X	X	Asynchronous preset
H	H	X	X	No change

D/ $\bar{U}$  or CTEN should be changed only when clock is high.

X = Don't care

↑ Low-to-high clock transition

## ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	TTL	LS	ALS	SN74 HC	CD74 HC	UNIT
I <sub>CC</sub>	MAX	105	35	22	0.08	0.16	mA
I <sub>OL</sub>	MAX	-0.8	-0.4	-0.4	-4	-4	mA
I <sub>OL</sub>	MAX	16	8	8	4	4	mA

## TIMING REQUIREMENTS AND SWITCHING CHARACTERISTICS

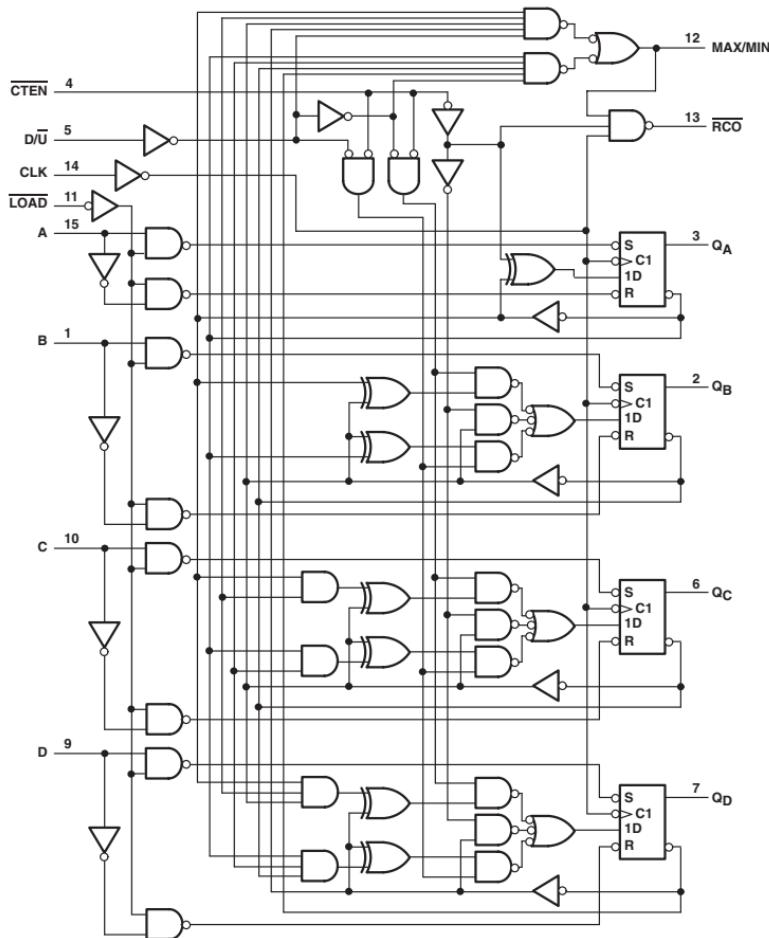
PARAMETER	INPUT	OUTPUT	MAX or MIN	TTL	LS	ALS	SN74 HC	CD74 HC
f <sub>max</sub>			MIN	20	20	25	17	20
t <sub>W</sub>	CLK		MIN	25	25	20	30	30
	LOAD			35	35	20	30	24
t <sub>su</sub>	Data , high or low		MIN	20	20	20	38	18
t <sub>th</sub>	Data hold time		MIN	0	5	5	5	2
t <sub>PLH</sub>	LOAD	Q	MAX	33	33	30	66	59
t <sub>PLHL</sub>				50	50	30	66	59
t <sub>PLH</sub>	DATA	Q	MAX	22	32	21	60	53
t <sub>PLHL</sub>				50	40	21	60	53
t <sub>PLH</sub>	CLK	$\overline{RCO}$	MAX	20	20	20	30	38
t <sub>PLHL</sub>				24	24	20	30	38
t <sub>PLH</sub>	CLK	Q	MAX	24	24	18	48	51
t <sub>PLHL</sub>				36	36	18	48	51
t <sub>PLH</sub>	CLK	MAX/MIN	MAX	42	42	31	63	63
t <sub>PLHL</sub>				52	52	31	63	63
t <sub>PLH</sub>	D/ $\bar{U}$	$\overline{RCO}$	MAX	45	45	37	57	45
t <sub>PLHL</sub>				45	45	28	57	45
t <sub>PLH</sub>	D/ $\bar{U}$	MAX/MIN	MAX	33	33	25	48	50
t <sub>PLHL</sub>				33	33	25	48	50

UNIT f<sub>max</sub> : MHz other : ns

## 4-BIT SYNCHRONOUS UP/DOWN BINARY COUNTERS

- Count Enable Control Input
- Ripple Clock Output for Cascading
- Asynchronously Presentable with Load Control

Logic Diagram (SN74HC)



## ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	TTL	LS	ALS	SN74 HC	CD74 HC	CD74 HCT	UNIT
I <sub>CC</sub>	MAX	105	35	22	0.08	0.16	0.16	mA
I <sub>OH</sub>	MAX	-0.8	-0.4	-0.4	-4	-4	-4	mA
I <sub>OL</sub>	MAX	16	8	8	4	4	4	mA

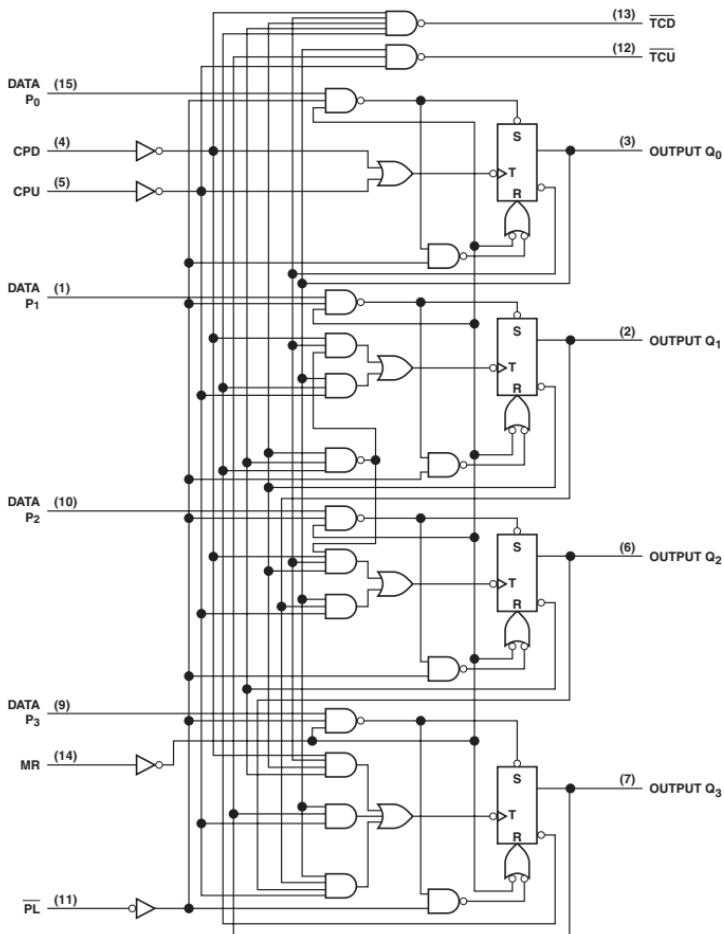
## TIMING REQUIREMENTS AND SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	TTL	LS	ALS	SN74 HC	CD74 HC	CD74 HCT
f <sub>max</sub>			MIN	20	20	30	17	20	20
t <sub>w</sub>	CLK		MIN	25	25	16.5	30	30	30
	LOAD low		MIN	35	35	20	30	24	24
t <sub>su</sub>	DATA		MIN	20	20	20	38	18	18
t <sub>th</sub>	DATA		MIN	0	5	5	5	2	2
t <sub>PLH</sub>			MAX	33	33	30	66	59	60
t <sub>PHL</sub>			MAX	50	50	30	66	59	60
t <sub>PLH</sub>			MAX	22	32	21	60	53	57
t <sub>PHL</sub>	A, B, C, D	QA, QB QC, QD	MAX	50	40	21	60	53	57
t <sub>PLH</sub>			MAX	20	20	20	30	38	53
t <sub>PHL</sub>			MAX	24	24	20	30	38	53
t <sub>PLH</sub>			MAX	24	24	18	48	51	41
t <sub>PHL</sub>			MAX	36	36	18	48	51	41
t <sub>PLH</sub>			MAX	42	42	31	63	63	63
t <sub>PHL</sub>			MAX	52	52	31	63	63	63
t <sub>PLH</sub>	D/̄U	RIPPLE CLK	MAX	45	45	37	57	45	45
t <sub>PHL</sub>			MAX	45	45	28	57	45	45
t <sub>PLH</sub>	D/̄U	MAX or MIN	MAX	33	33	25	48	50	57
t <sub>PHL</sub>			MAX	33	33	25	48	50	57

UNIT f<sub>max</sub> : MHz, other : ns

## PRESETTABLE SYNCHRONOUS 4-BIT UP/DOWN COUNTERS

Logic Diagram



TRUE TABLE

CLOCK UP	CLOCK DOWN	RESET	PARALLEL LOAD	FUNCTION
↑	H	L	H	Count Up
H	↑	L	H	Count Down
X	X	H	X	Reset
X	X	L	L	Load Preset inputs

NOTE: H = High Voltage Level, L = Low Voltage Level, X = Don't Care, ↑ = Transition from Low to High Level

## ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	CD74 HC	UNIT
I <sub>CC</sub>	MAX	0.16	mA
I <sub>OL</sub>	MAX	-4	mA
I <sub>OL</sub>	MAX	4	mA

## TIMING REQUIREMENTS AND SWITCHING CHARACTERISTICS

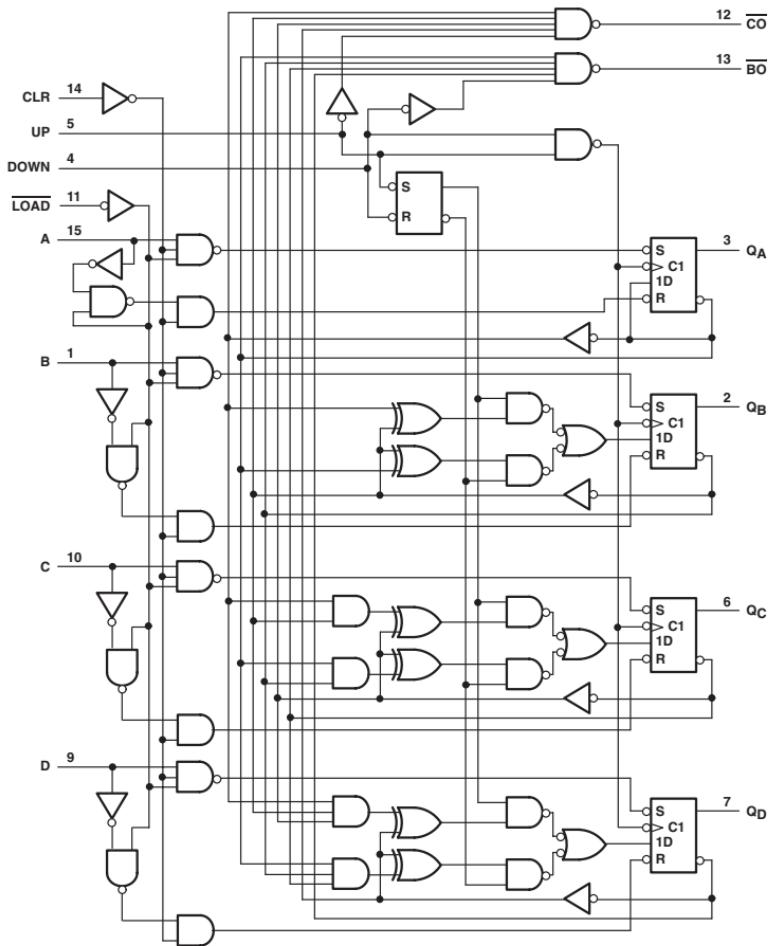
PARAMETER	INPUT	OUTPUT	MAX or MIN	CD74 HC	
t <sub>w</sub>	CPU, CPD		MIN	35	
	PL			24	
	MR			30	
t <sub>su</sub>	P <sub>n</sub> to P <sub>L</sub>		MIN	24	
	P <sub>n</sub> to PL			0	
	CPD to CPU, CPD to CPU			24	
t <sub>phl</sub>	CPU	T <sub>CU</sub>	MAX	38	
				38	
t <sub>phl</sub>	CPD	T <sub>CD</sub>	MAX	38	
				38	
t <sub>phl</sub>	CPU	Q <sub>n</sub>	MAX	65	
				65	
t <sub>phl</sub>	CPD	Q <sub>n</sub>	MAX	65	
				65	
t <sub>phl</sub>	PL	Q <sub>n</sub>	MAX	66	
				66	
t <sub>phl</sub>	MR	Q <sub>n</sub>	MAX	60	

UNIT:ns

## 4-BIT SYNCHRONOUS UP/DOWN COUNTERS (DUAL CLOCK WITH CLEAR)

- Parallel Asynchronous Load for Modulo-N Count Lengths
- Asynchronous Clear

Logic Diagram (SN74)



## ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	TTL	LS	ALS	F	SN74 HC	CD74 HC	CD74 HCT	UNIT
I <sub>CC</sub>	MAX	102	34	22	54	0.08	0.16	0.16	mA
I <sub>OH</sub>	MAX	-0.4	-0.4	-0.4	-1	-4	-4	-4	mA
I <sub>OL</sub>	MAX	16	8	8	20	4	4	4	mA

## TIMING REQUIREMENTS AND SWITCHING CHARACTERISTICS

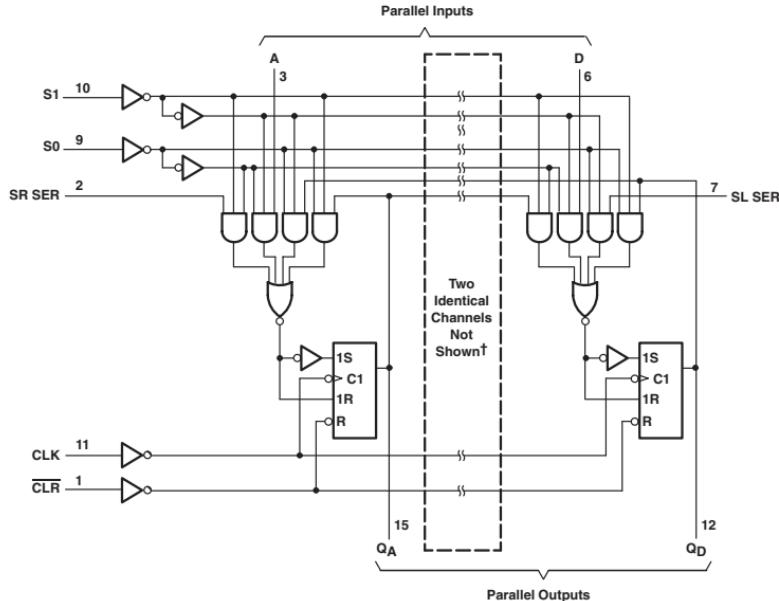
PARAMETER	INPUT	OUTPUT	MAX or MIN	TTL	LS	ALS	F	SN74 HC	CD74 HC	CD74 HCT
fmax	t <sub>w</sub> t <sub>su</sub> t <sub>th</sub>	DATA DATA	MIN	25	25	30	85	17	17	15
			MIN	20	20	20	4	30	30	35
			MIN	20	20	20	3.5	28	22	22
			MIN	0	5	5	2.5	5	0	0
t <sub>PLH</sub>	UP (CD74: CPU)	$\bar{C}_O$	MAX	26	26	16	9	41	38	41
t <sub>PLH</sub>			MAX	24	24	18	9	41	38	41
t <sub>PLH</sub>	DOWN (CD74: CPD)	$\bar{B}_O$	MAX	24	24	16	9	41	38	41
t <sub>PLH</sub>			MAX	24	24	18	9	41	38	41
t <sub>PLH</sub>	UP or DOWN (CD74: CPU or CPD)	ANY Q	MAX	38	38	19	9	63	65	60
t <sub>PLH</sub>			MAX	47	47	17	13	63	65	60
t <sub>PLH</sub>	LOAD (CD74: PL)	ANY Q	MAX	40	40	30	11	65	66	69
t <sub>PLH</sub>			MAX	40	40	28	13	65	66	69
	CLR (CD74: MR)	ANY Q	MAX	35	35	17	12	60	60	65

UNIT fmax : MHz, other : ns

## 4-BIT BIDIRECTIONAL UNIVERSAL SHIFT REGISTERS

- Direct Overriding Clear
- Parallel-to-Serial, Serial-to-Parallel Conversions
- Left or Right Shifts

Logic Diagram (SN74)



† I/O ports not shown: Q<sub>B</sub> (14) and Q<sub>C</sub> (13)

FUNCTION TABLE (SN74)

CLEAR	MODE S1 S0	CLOCK	INPUTS				OUTPUTS			
			SERIAL		PARALLEL		QA	QB	QC	QD
LEFT	RIGHT	A	B	C	D					
L	X X	X	X X	X X	X X X X		L L L L			
H	X X	L	X X	X X	X X X X	Qa0 Qb0 Cc0 Cd0				
H	H H	↑	X X	X X	a b c d	a b c d				
H	L H	↑	X X	H	X X X X	H QAn QBn Ccn				
H	L H	↑	X X	L	X X X X	L QAn QBn Ccn				
H	H L	↑	H	X	X X X X	Qbn Ccn Qd0 H				
H	H L	↑	L	X	X X X X	Qbn Ccn Qd0 L				
H	L L	X	X	X X	X X X X	Qa0 Qb0 Cc0 Cd0				

## ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	TTL	LS	S	AS	SN74 HC	CD74 HC	CD74 HCT	UNIT
Icc	MAX	63	23	135	53	0.1	0.16	0.16	mA
IoH	MAX	-0.8	-0.4	-1	-2	-4	-4	-4	mA
IoL	MAX	16	8	20	20	4	4	4	mA

## TIMING REQUIREMENTS AND SWITCHING CHARACTERISTICS

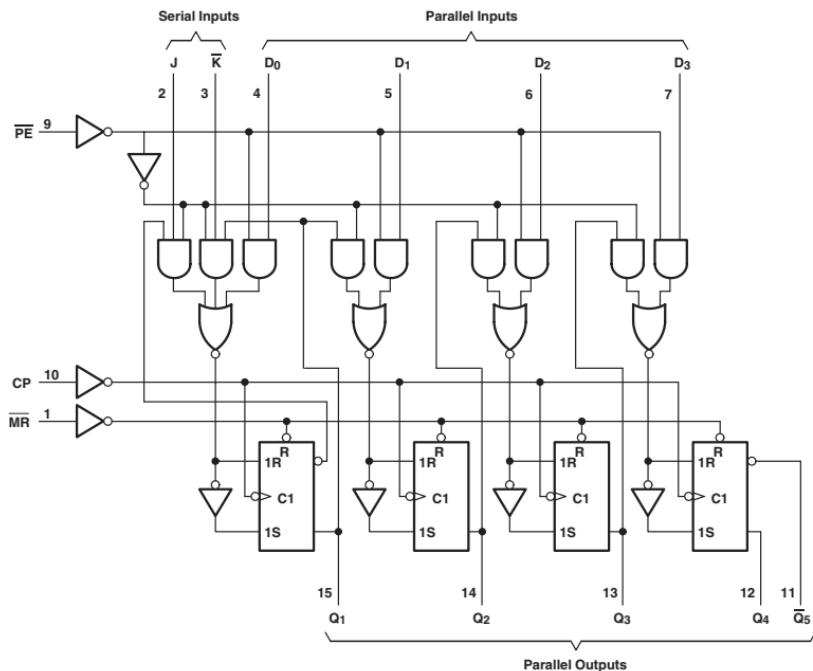
PARAMETER		INPUT	OUTPUT	MAX or MIN	TTL	LS	S	AS	SN74 HC	CD74 HC	CD74 HCT
fmax				MIN	25	25	70	80	25	20	18
t <sub>w</sub>	CLR (MR)			MIN	20	20	12	4.5	20	24	24
	CLK (CP) "H"			MIN	20	20	7	4	20	24	24
	CLK (CP) "L"			MIN	20	20	7	7	20	24	24
tsu	Mode Control			MIN	30	30	11	9.5	25	24	30
	DATA			MIN	20	20	5	4	25	21	21
	CLR (MR) INACTIVE			MIN	25	25	9	6	-	-	-
th				MIN	0	0	3	0.5	0	0	0
t <sub>PHL</sub>	CLEAR (MR)	ANY		MAX	30	30	18.5	12	38	42	60
t <sub>PLH</sub>	CLOCK (CP)	ANY		MAX	22	22	12	7	36	53	56
t <sub>PLH</sub>				MAX	26	26	16.5	7	36	53	56

UNIT fmax : MHz, other : ns

## 4-BIT PARALLEL-ACCESS SHIFT REGISTERS

- Direct Overriding Clear
- Parallel-to-Serial, Serial-to-Parallel Conversions

Logic Diagram



TRUTH TABLE

OPERATING MODES	INPUTS						OUTPUT				
	MR	CP	PE	J	K̄	Dn	Q <sub>0</sub>	Q <sub>1</sub>	Q <sub>2</sub>	Q <sub>3</sub>	Q̄ <sub>3</sub>
Asynchronous Reset	L	X	X	X	X	X	L	L	L	L	H
Shift, Set First Stage	H	↑	h	h	h	X	H	q <sub>0</sub>	q <sub>1</sub>	q <sub>2</sub>	q̄ <sub>2</sub>
Shift, Reset First Stage	H	↑	h	I	I	X	L	q <sub>0</sub>	q <sub>1</sub>	q <sub>2</sub>	q̄ <sub>2</sub>
Shift, Toggle First Stage	H	↑	h	h	I	X	q̄ <sub>0</sub>	q <sub>0</sub>	q <sub>1</sub>	q <sub>2</sub>	q̄ <sub>2</sub>
Shift, Retain First Stage	H	↑	h	I	h	X	q <sub>0</sub>	q <sub>0</sub>	q <sub>1</sub>	q <sub>2</sub>	q̄ <sub>2</sub>
Parallel Load	H	↑	I	X	X	d <sub>n</sub>	d <sub>0</sub>	d <sub>1</sub>	d <sub>2</sub>	d <sub>3</sub>	d̄ <sub>2</sub>

H = High Voltage Level

L = Low Voltage Level,

X = Don't Care

= Transition from Low to High Level

I = Low Voltage Level One Set-up Time Prior to the Low to High Clock Transition

h = Low Voltage Level One Set-up Time prior to the High to Low Clock Transition,

dn (q<sub>n</sub>) = Lower Case Letters Indicate the State of the Referenced Input (or output) One Set-up Time Prior to the Low to High Clock

Transition.

## ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	TTL	LS	S	AS	SN74 HC	CD74 HC	UNIT
I <sub>CC</sub>	MAX	63	21	109	57	0.1	0.16	mA
I <sub>OH</sub>	MAX	-0.8	-0.4	-1	-2	-4	-4	mA
I <sub>OL</sub>	MAX	16	8	20	20	4	4	mA

## TIMING REQUIREMENTS AND SWITCHING CHARACTERISTICS

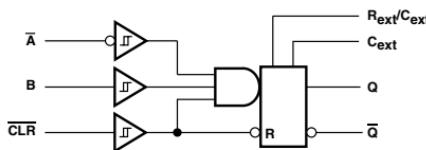
PARAMETER	INPUT	OUTPUT	MAX or MIN	TTL	LS	S	AS	SN74 HC	CD74 HC
fmax			MIN	30	30	70	70	25	20
tw	Clock		MIN	16	16	7	4	20	24
	MR		MIN	12	12	12	7.2	20	24
tsu	PE		MIN	25	25	11	8	25	30
	Serial & Parallel Data		MIN	20	15	5	3.5	25	-
	Clear Inactive Data		MIN	25	25	9	6	25	-
TRELEASE			MAX	10	20	6	-	-	-
th			MIN	0	0	3	1	0	3
t <sub>PHL</sub>	MR		MAX	30	30	18.5	11.5	38	45
t <sub>PLH</sub>		QA, QD	MAX	22	22	12	8.5	36	53
t <sub>PLH</sub>	Clock		MAX	26	26	16.5	10.5	36	53

UNIT fmax : MHz, other : ns

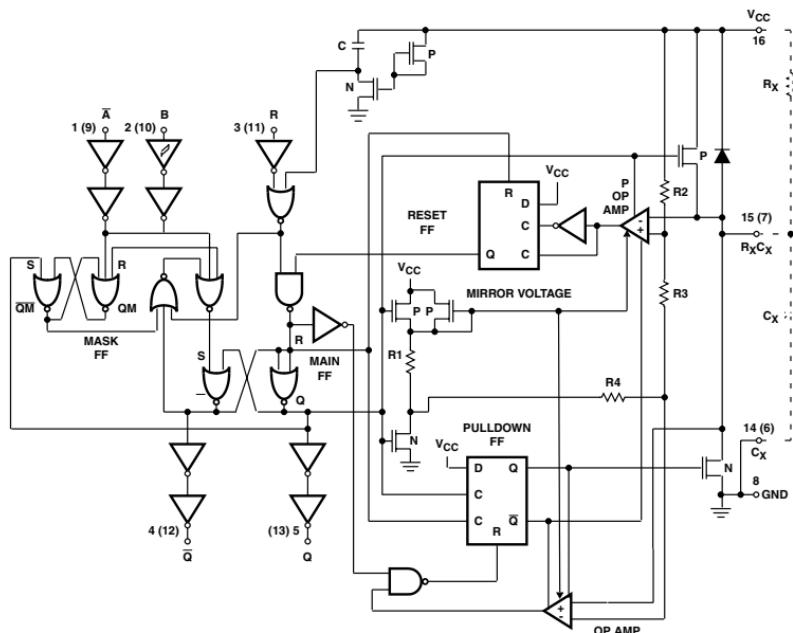
## DUAL MONOSTABLE MULTIVIBRATORS WITH SCHMITT-TRIGGER INPUTS

- Overriding Clear Terminates Outputs Pulse

Logic Diagram (SN74LV)



Logic Diagram (CD74HC/HCT)



**FUNCTION TABLE**  
(each monostable multivibrator)

INPUTS			OUTPUTS	
CLR	A	B	Q	$\bar{Q}$
L	X	X	L	H
X	H	X	L	H
X	X	L	L	H
H	L	↑	↑†	↑†
H	↓	H	↑†	↑†
↑‡	L	H	↑†	↑†

†Pulsed-output patterns are tested during AC switching at 25°C with  $R_{ext} = 2\text{ k}\Omega$ , and  $C_{ext} = 80\text{ pF}$ .

‡This condition is true only if the output of the latch formed by the two NAND gates has been conditioned to the logic 1 state prior to CLR going high. This latch is conditioned by taking either A high or B low while CLR is inactive (high).

#### ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	TTL	LS	CD74 HC	CD74 HCT	LV 3V	LV 5V	UNIT
$I_{CC}$	MAX	80	27	0.16	0.16	0.28	0.65	mA
$I_{OH}$	MAX	-0.8	-0.4	-4	-4	-6	-12	mA
$I_{OL}$	MAX	16	8	4	4	6	12	mA

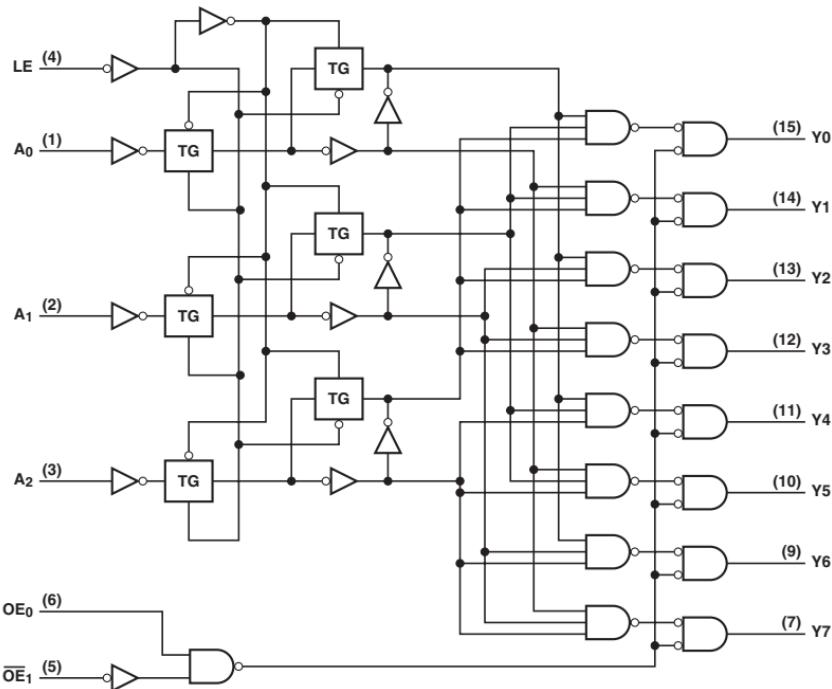
#### SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	TTL	LS	CD74 HC	CD74 HCT	LV 3V	LV 5V
$t_{PLH}$	A (HC, LV: $\bar{A}$ )	Q	MAX	70	70	63	63	27.5	16
	B			55	55	63	63	27.5	16
$t_{PHL}$	A (HC, LV: $\bar{A}$ )	$\bar{Q}$	MAX	80	80	51	51	27.5	16
	B			65	65	51	51	27.5	16
$t_{PHL}$	Clear	Q	MAX	27	55	48	57	22	13
		$\bar{Q}$		40	65	54	56	22	13

UNIT: ns

## 3-LINE TO 8-LINE DECODERS/DEMULTIPLEXERS WITH ADDRESS LATCHES

Logic Diagram



FUNCTION TABLE

INPUTS					OUTPUTS								
LE	OE0	OE1	A2	A1	A0	Y0	Y1	Y2	Y3	Y4	Y5	Y6	Y7
X	X	H	X	X	X	L	L	L	L	L	L	L	L
X	L	X	X	X	X	L	L	L	L	L	L	L	L
L	H	L	L	L	L	H	L	L	L	L	L	L	L
L	H	L	L	L	H	L	H	L	L	L	L	L	L
L	H	L	L	H	L	L	H	L	L	L	L	L	L
L	H	L	L	H	H	L	L	H	L	L	L	L	H
L	H	L	H	L	L	L	L	L	L	L	L	H	L
L	H	L	H	H	H	L	L	L	L	L	L	L	H
H	H	L	X	X	X	Depends upon the address previously applied while LE was at a logic low.							

## ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	SN74 HC	CD74 HC	CD74 HCT	UNIT
Icc	MAX	0.08	0.16	0.16	mA
IoH	MAX	-4	-4	-4	mA
IoL	MAX	4	4	4	mA

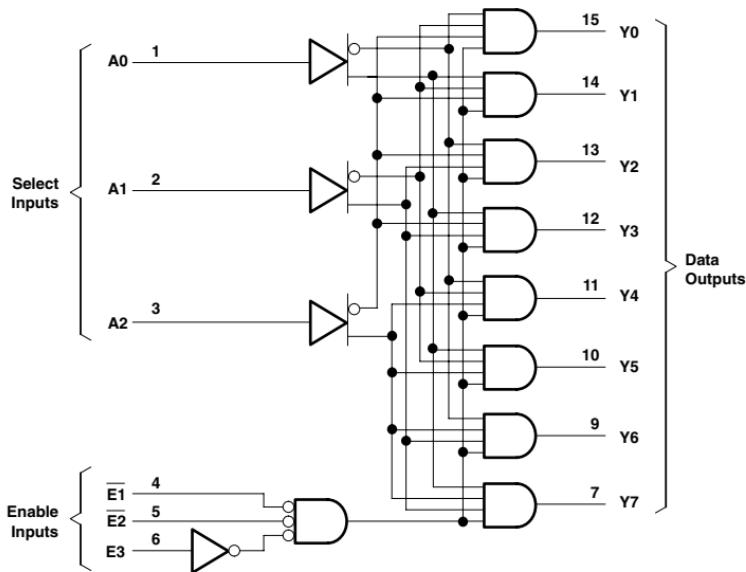
## TIMING REQUIREMENTS AND SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	SN74 HC	CD74 HC	CD74 HCT
t <sub>W</sub>	LE Pulse Width			MIN	20	15
t <sub>su</sub>	An to LE			MIN	19	15
t <sub>h</sub>	An to LE			MIN	5	5
t <sub>PLH</sub>	An	Y	MAX	48	48	57
t <sub>PHL</sub>				48	48	57
t <sub>PLH</sub>	OE <sub>0</sub>	Y	MAX	44	44	60
t <sub>PHL</sub>				44	44	60
t <sub>PLH</sub>	OE <sub>1</sub>	Y	MAX	44	44	53
t <sub>PHL</sub>				44	44	53

UNIT:ns

## 3-LINE TO 8-LINE DECODERS/DEMULTIPLEXERS

Logic Diagram (CD74AC/ACT)



FUNCTION TABLE

INPUTS						OUTPUTS							
ENABLE			ADDRESS			Y0	Y1	Y2	Y3	Y4	Y5	Y6	Y7
E3	E2	E1	A2	A1	A0	Y0	Y1	Y2	Y3	Y4	Y5	Y6	Y7
X	X	H	X	X	X	L	L	L	L	L	L	L	L
L	X	X	X	X	X	L	L	L	L	L	L	L	L
X	H	X	X	X	X	L	L	L	L	L	L	L	L
H	L	L	L	L	L	H	L	L	L	L	L	L	L
H	L	L	L	L	H	L	H	L	L	L	L	L	L
H	L	L	L	H	L	L	L	H	L	L	L	L	L
H	L	L	L	H	H	L	L	L	L	L	H	L	L
H	L	L	H	H	H	L	L	L	H	L	L	L	L
H	L	L	H	H	L	L	L	L	H	L	L	L	L
H	L	L	H	H	L	L	L	L	L	L	H	L	L
H	L	L	H	H	H	L	L	L	L	L	L	H	L
H	L	L	H	H	H	L	L	L	L	L	L	L	H

Note: H = High Voltage Level, L = Low Voltage Level, X = Don't Care

## ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	CD74 HC	CD74 HCT	CD74 AC	CD74 ACT	UNIT
I <sub>CC</sub>	MAX	0.16	0.16	0.16	0.16	mA
I <sub>OH</sub>	MAX	-4	-4	-24	-24	mA
I <sub>OL</sub>	MAX	4	4	24	24	mA

## SWITCHING CHARACTERISTICS

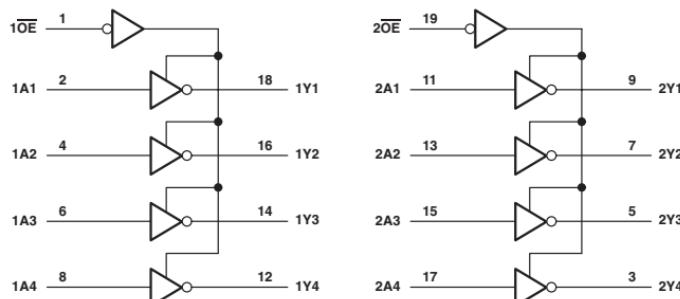
PARAMETER	INPUT	OUTPUT	MAX or MIN	CD74 HC	CD74 HCT	CD74 AC	CD74 ACT
I <sub>PLH</sub>	Address	Y	MAX	45	53	15	15.6
I <sub>PHL</sub>				45	53	15	15.6
I <sub>PLH</sub>	$\overline{E1}, \overline{E2}$ (G2A, G2B)	Y	MAX	60	60	11.9	14.2
I <sub>PHL</sub>				60	60	11.9	14.2
I <sub>PLH</sub>	E3 (G1)	Y	MAX	60	60	16.6	13.6
I <sub>PHL</sub>				60	60	16.6	13.6

UNIT:ns

## OCTAL BUFFERS/DRIVERS WITH 3-STATE OUTPUTS

- 3-State Outputs Drive Bus Lines or Buffer Memory Address Registers
- PNP Inputs Reduce DC Loading
- 74AC11xxx: Product Available in Reduced-Noise Advanced CMOS (11000 Series)
- 74ACT11xxx: Product Available in Reduced-Noise Advanced CMOS (11000 Series)
- CD74AC/ACT240  $T_A: -40$  to  $85^\circ\text{C}$

Logic Diagram (SN74)

FUNCTION TABLE  
(each 4-bit buffer)

INPUTS		OUTPUT Y
OE	A	
L	H	L
L	L	H
H	X	Z

## ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	LS	S	ALS	ALS A-1	AS	F	SN74 HC	CD74 HC	SN74 HCT	CD74 HCT	SN74 BCT	ABT	UNIT
$I_{CH}$	MAX	27	135	11	11	17	29	0.08	0.16	0.08	0.16	31	0.25	mA
$I_{CL}$	MAX	44	150	23	23	75	75	0.08	0.16	0.08	0.16	71	30	mA
$I_{CZ}$	MAX	50	150	25	25	38	63	0.08	0.16	0.08	0.16	9	0.25	mA
$I_{OH}$	MAX	-15	-15	-15	-15	-15	-15	-6	-6	-6	-6	-15	-32	mA
$I_{OL}$	MAX	24	64	24	48	64	64	6	6	6	6	64	64	mA

PARAMETER	MAX or MIN	LVT 3V	LVTH 3V	AC 11	SN74 AC	CD74 AC	ACT 11	SN74 ACT	CD74 ACT	AHC	AHCT	LV 3V	LV 5V	UNIT
$I_{CH}$	MAX	0.19	0.19	0.08	0.04	0.08	0.08	0.04	0.08	0.04	0.04	-	0.02	mA
$I_{CL}$	MAX	5	5	0.08	0.04	0.08	0.08	0.04	0.08	0.04	0.04	-	0.02	mA
$I_{CZ}$	MAX	0.19	0.19	0.08	0.04	0.08	0.08	0.04	0.08	0.04	0.04	-	0.02	mA
$I_{OH}$	MAX	-32	-32	-24	-24	-24	-24	-24	-24	-8	-8	-8	-16	mA
$I_{OL}$	MAX	64	64	24	24	24	24	24	24	8	8	8	16	mA

PARAMETER	MAX or MIN	LVC 3V	LVCZ 3V	AUC 1.8V	AUC 2.3V	AUCH 1.8V	AUCH 2.3V	UNIT
$I_{CH}$	MAX	0.01	0.1	0.02	0.02	0.02	0.02	mA
$I_{CL}$	MAX	0.01	0.1	0.02	0.02	0.02	0.02	mA
$I_{CZ}$	MAX	0.01	0.1	0.02	0.02	0.02	0.02	mA
$I_{OH}$	MAX	-24	-24	-8	-9	-8	-9	mA
$I_{OL}$	MAX	24	24	8	9	8	9	mA

## SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	LS	S	ALS	ALS A-1	AS	F	SN74 HC	CD74 HC	SN74 HCT	CD74 HCT
t <sub>PLH</sub>	A	Y (CD74: $\bar{Y}$ )	MAX	14	7	9	9	6.5	8	25	30	32	33
				18	7	9	9	6.5	5.7	25	30	32	33
t <sub>PHL</sub>	$\bar{OE}$	Y (CD74: $\bar{Y}$ )	MAX	23	10	13	13	6.4	6.1	38	-	44	-
				30	15	18	18	9	10	38	-	44	-
t <sub>PZH</sub>	$\bar{OE}$	Y (CD74: $\bar{Y}$ )	MAX	25	9	10	10	5	6.3	38	-	44	-
				20	15	12	12	9.5	9.5	38	-	44	-

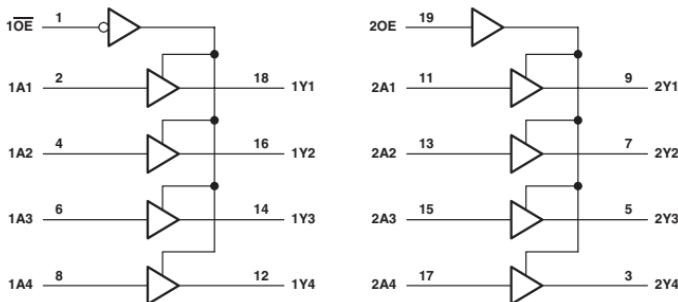
PARAMETER	INPUT	OUTPUT	MAX or MIN	SN74 BCT	ABT	LVT 3V	LVT 3V	AC 11	SN74 AC	CD74 AC	ACT 11	SN74 ACT	CD74 ACT
t <sub>PLH</sub>	A	Y (CD74: $\bar{Y}$ )	MAX	5.6	4.8	3.8	3.8	8.4	7	6.5	10.6	9.5	7.8
				4	4.8	4	4	7.2	6.5	6.5	8.7	8.5	7.8
t <sub>PHL</sub>	$\bar{OE}$	Y (CD74: $\bar{Y}$ )	MAX	8.8	5.2	4.6	4.6	9.2	8	10.9	12.5	9.5	12.2
				10.5	6.2	4.4	4.4	8.7	8.5	10.9	12.3	10.5	12.2
t <sub>PZH</sub>	$\bar{OE}$	Y (CD74: $\bar{Y}$ )	MAX	8.1	6.4	4.4	4.4	6.6	9.5	10.9	10	10.5	12.2
				9.5	5.8	4.3	4.3	7.7	9.5	10.9	10.8	10.5	12.2

PARAMETER	INPUT	OUTPUT	MAX or MIN	AHC	AHCT	LV 3V	LV 5V	LVC 3V	LVCZ 3V	AUC 1.8V	AUC 2.3V	AUCH 1.8V	AUCH 2.3V
t <sub>PLH</sub>	A	Y	MAX	8.5	9.5	12.5	8.5	6.5	6.5	2.1	1.6	2.1	1.6
				8.5	9.5	12.5	8.5	6.5	6.5	2.1	1.6	2.1	1.6
t <sub>PHL</sub>	$\bar{OE}$	Y	MAX	10.5	13	16	10.5	8	8	2.7	2	2.7	2
				10.5	13	16	10.5	8	8	2.7	2	2.7	2
t <sub>PZH</sub>	$\bar{OE}$	Y	MAX	10.5	13	17	15.5	7	7	4	2	4	2
				10.5	13	17	15.5	7	7	4	2	4	2
t <sub>PLZ</sub>	$\bar{OE}$	Y	MAX	10.5	13	17	15.5	7	7	4	2	4	2

UNIT: ns

**OCTAL BUFFERS/DRIVERS WITH 3-STATE OUTPUTS**

- 3-State Outputs Drive Bus Lines or Buffer Memory Address Registers
- PNP Inputs Reduce DC Loading
- CD74AC/ACT241  $T_A: -40$  to  $85^\circ\text{C}$

**Logic Diagram (SN74)****FUNCTION TABLE  
(each buffer)**

INPUTS		OUTPUT
OE	A	Y
L	H	H
L	L	L
H	X	Z

## ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	LS	S	ALS	AS	F	SN74 HC	CD74 HC	CD74 HCT	SN74 BCT	ABT	LVTH 3V	SN74 AC	UNIT
I <sub>CH</sub>	MAX	27	160	18	35	60	0.08	0.16	0.16	43	0.25	0.19	0.04	mA
I <sub>CCL</sub>	MAX	46	180	26	90	90	0.08	0.16	0.16	85	30	5	0.04	mA
I <sub>CCZ</sub>	MAX	54	180	30	56	90	0.08	0.16	0.16	10	0.25	0.19	0.04	mA
I <sub>OH</sub>	MAX	-15	-15	-15	-15	-15	-6	-6	-6	-15	-32	-32	-24	mA
I <sub>OL</sub>	MAX	24	64	24	64	64	6	6	6	64	64	64	24	mA

PARAMETER	MAX or MIN	CD74 AC	SN74 ACT	CD74 ACT	UNIT
I <sub>CH</sub>	MAX	0.16	0.04	0.08	mA
I <sub>CCL</sub>	MAX	0.16	0.04	0.08	mA
I <sub>CCZ</sub>	MAX	0.16	0.04	0.08	mA
I <sub>OH</sub>	MAX	-24	-24	-24	mA
I <sub>OL</sub>	MAX	24	24	24	mA

## SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	LS	S	ALS	AS	F	SN74 HC	CD74 HC	CD74 HCT	SN74 BCT
I <sub>PLH</sub>	A	Y(CD74: $\bar{Y}$ )	MAX	18	9	11	6.2	6.2	29	33	38	4.9
I <sub>PLH</sub>				18	9	10	6.2	6.5	29	33	38	5.9
I <sub>PZH</sub>	$\overline{10E}$	Y(CD74: $\bar{Y}$ )	MAX	23	12	21	9	6.7	38	-	-	8.7
I <sub>PZL</sub>				30	15	21	7.5	8	38	-	-	9.4
I <sub>PLZ</sub>	$\overline{10E}$	Y(CD74: $\bar{Y}$ )	MAX	25	9	10	6	7	38	-	-	8.1
I <sub>PLZ</sub>				20	15	15	9	7	38	-	-	9.9
I <sub>PZH</sub>	20E	Y(CD74: $\bar{Y}$ )	MAX	23	12	21	10.5	6.7	38	-	-	8.7
I <sub>PZL</sub>				30	15	21	8.5	8	38	-	-	9.4
I <sub>PLZ</sub>	20E	Y(CD74: $\bar{Y}$ )	MAX	25	9	10	7	7	38	-	-	8.1
I <sub>PLZ</sub>				20	15	15	12	7	38	-	-	9.9

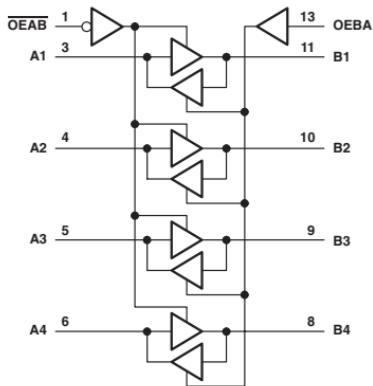
PARAMETER	INPUT	OUTPUT	MAX or MIN	ABT	LVTH 3V	SN74 AC	CD74 AC	SN74 ACT	CD74 ACT
I <sub>PLH</sub>	A	Y(CD74: $\bar{Y}$ )	MAX	4.6	3.5	7.5	7.5	9.5	8.7
I <sub>PLH</sub>				4.6	3.4	7.5	7.5	8.5	8.7
I <sub>PZH</sub>	$\overline{10E}$	Y(CD74: $\bar{Y}$ )	MAX	6.8	4.5	9.5	10.9	9.5	12.2
I <sub>PZL</sub>				6.8	4.4	9.5	10.9	10.5	12.2
I <sub>PLZ</sub>	$\overline{10E}$	Y(CD74: $\bar{Y}$ )	MAX	7.1	4.5	10.5	10.9	10.5	12.2
I <sub>PLZ</sub>				5.9	4.7	10.5	10.9	10.5	12.2
I <sub>PZH</sub>	20E	Y(CD74: $\bar{Y}$ )	MAX	6.8	4.5	9.5	10.9	9.5	12.2
I <sub>PZL</sub>				6.8	4.4	9.5	10.9	10.5	12.2
I <sub>PLZ</sub>	20E	Y(CD74: $\bar{Y}$ )	MAX	7.1	4.5	10.5	10.9	10.5	12.2
I <sub>PLZ</sub>				5.9	4.7	10.5	10.9	10.5	12.2

UNIT: ns

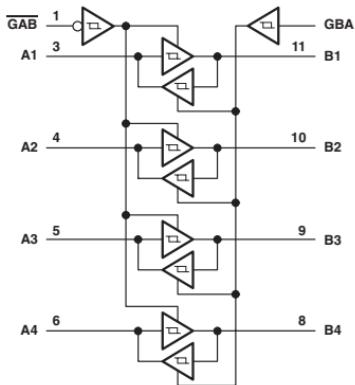
## QUADRUPLE BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

- Two-Way Asynchronous Communication Between Data Buses
- PNP Inputs Reduce DC Loading

Logic Diagram (SN74ALS)



Logic Diagram (SN74LS)



**FUNCTION TABLE (SN74)**

INPUTS		OPERATION	
GAB	GBA		
L	L	A to B	
H	H	B to A	
H	L	Isolation	
L	H	Latch A and B (A = B)	

**ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS**

PARAMETER	MAX or MIN	LS	ALS	AS	SN74 HC	CD74 HC	CD74 HCT	UNIT
I <sub>CH</sub>	MAX	38	25	44	0.08	0.16	0.16	mA
I <sub>CL</sub>	MAX	50	30	74	0.08	0.16	0.16	mA
I <sub>CZ</sub>	MAX	54	32	56	0.08	0.16	0.16	mA
I <sub>OH</sub>	MAX	-15	-15	-	-	-6	-6	mA
I <sub>OL</sub>	MAX	24	24	64	6	6	6	mA

**SWITCHING CHARACTERISTICS**

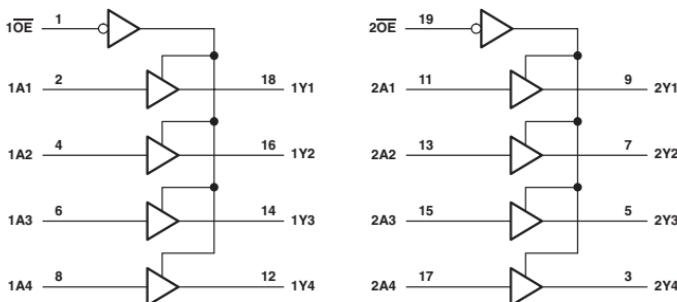
PARAMETER	INPUT	OUTPUT	MAX or MIN	LS	ALS	AS	SN74 HC	CD74 HC	CD74 HCT
t <sub>PLH</sub>	A or B	A or B	MAX	18	11	7.5	25	27	33
t <sub>PHL</sub>	A or B	A or B	MAX	18	11	6.5	25	27	33
t <sub>PZH</sub>	GAB	B	MAX	23	20	9	38	45	51
t <sub>PZL</sub>				30	20	7.5	38	45	51
t <sub>PHZ</sub>	GAB	B	MAX	25	14	6.5	38	45	53
t <sub>PZL</sub>				20	22	9	38	45	53
t <sub>PZH</sub>	GAB	A	MAX	23	20	10.5	38	45	51
t <sub>PZL</sub>				30	20	8.5	38	45	51
t <sub>PHZ</sub>	GAB	A	MAX	25	14	7	38	45	53
t <sub>PZL</sub>				20	22	11	38	45	53

UNIT: ns

## OCTAL BUFFERS/DRIVERS WITH 3-STATE OUTPUTS

- 3-State Outputs Drive Bus Lines or Buffer Memory Address Registers
- PNP Inputs Reduce DC Loading
- 74AC11xxx: Product Available in Reduced-Noise Advanced CMOS (11000 Series)
- 74ACT11xxx: Product Available in Reduced-Noise Advanced CMOS (11000 Series)
- CD74AC/ACT244  $T_A: -40$  to  $85^\circ\text{C}$

Logic Diagram (SN74)

FUNCTION TABLE  
(each buffer)

INPUTS		OUTPUT
OE	A	Y
L	H	H
L	L	L
H	X	Z

## ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	LS	S	ALS	ALS C-1	AS	F	SN74 HC	CD74 HC	SN74 HCT	CD74 HCT	SN74 BCT	SN64 BCT	UNIT
$I_{CH}$	MAX	27	160	17	17	34	60	0.08	0.16	0.08	0.16	40	40	mA
$I_{CL}$	MAX	46	180	24	24	90	90	0.08	0.16	0.08	0.16	80	80	mA
$I_{CZ}$	MAX	54	180	27	27	54	90	0.08	0.16	0.08	0.16	10	10	mA
$I_{OH}$	MAX	-15	-15	-15	-15	-15	-15	-6	-6	-6	-6	-15	-15	mA
$I_{OL}$	MAX	24	64	24	48	64	64	6	6	6	6	64	64	mA

PARAMETER	MAX or MIN	ABT	LVT 3V	LVTH 3V	LVTZ 3V	AC 11	SN74 AC	CD74 AC	ACT 11	SN74 ACT	CD74 ACT	AHC	AHCT	LV 3V	UNIT
$I_{CH}$	MAX	0.25	0.19	0.19	0.225	0.08	0.04	0.08	0.08	0.04	0.08	0.04	0.04	0.04	- mA
$I_{CL}$	MAX	30	5	5	15	0.08	0.04	0.08	0.08	0.04	0.08	0.04	0.04	0.04	- mA
$I_{CZ}$	MAX	0.25	0.19	0.19	0.225	0.08	0.04	0.08	0.08	0.04	0.08	0.04	0.04	0.04	- mA
$I_{OH}$	MAX	-32	-32	-32	-32	-24	-24	-24	-24	-24	-24	-8	-8	-8	mA
$I_{OL}$	MAX	64	64	64	64	24	24	24	24	24	24	8	8	8	mA

PARAMETER	MAX or MIN	LV 5V	LV-AT 3	LVC 3V	LVCH 3V	LVCZ 3V	ALVC 3V	ALVCH 3V	AUC 1.8V	AUC 2.3V	AUCH 1.8V	AUCH 2.3V	UNIT
$I_{CH}$	MAX	0.02	0.02	0.01	0.01	0.1	0.01	0.01	0.02	0.02	0.02	0.02	mA
$I_{CL}$	MAX	0.02	0.02	0.01	0.01	0.1	0.01	0.01	0.02	0.02	0.02	0.02	mA
$I_{CZ}$	MAX	0.02	0.02	0.01	0.01	0.1	0.01	0.01	0.02	0.02	0.02	0.02	mA
$I_{OH}$	MAX	-16	-16	-24	-24	-24	-24	-24	-8	-9	-8	-9	mA
$I_{OL}$	MAX	16	16	24	24	24	24	24	8	9	8	9	mA

## SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	LS	S	ALS	ALS C-1	AS	F	SN74 HC	CD74 HC	SN74 HCT
I <sub>PLH</sub>	A	Y	MAX	18	9	10	10	6.2	6.2	29	33	35
I <sub>PHL</sub>				18	9	10	10	6.2	6.5	29	33	35
I <sub>PZH</sub>	OE	Y	MAX	23	12	20	20	9	6.7	38	-	44
I <sub>PZL</sub>				30	15	20	20	7.5	8	38	-	44
I <sub>PHZ</sub>	OE	Y	MAX	25	9	10	10	6	7	38	-	44
I <sub>PZL</sub>				20	15	13	13	9	7	38	-	44

PARAMETER	INPUT	OUTPUT	MAX or MIN	CD74 HCT	SN74 BCT	SN64 BCT	ABT	LVT 3V	LVT <sub>H</sub> 3V	LVTZ 3V	AC 11	SN74 AC	CD74 AC
I <sub>PLH</sub>	A	Y	MAX	38	5	5.3	4.6	3.5	3.5	4.1	7.3	7.5	7.5
I <sub>PHL</sub>				38	5.5	6	4.6	3.3	3.3	4.1	6.9	7.5	7.5
I <sub>PZH</sub>	OE	Y	MAX	-	8.7	9	5.1	4.5	4.5	5.2	8.5	8	10.9
I <sub>PZL</sub>				-	8.9	9.4	6.1	4.4	4.4	5.2	8.5	8.5	10.9
I <sub>PHZ</sub>	OE	Y	MAX	-	7.7	8	6.6	4.4	4.4	5.6	7.3	9.5	10.9
I <sub>PZL</sub>				-	8.9	9.8	5.7	4.4	4.4	5.1	8.2	9.5	10.9

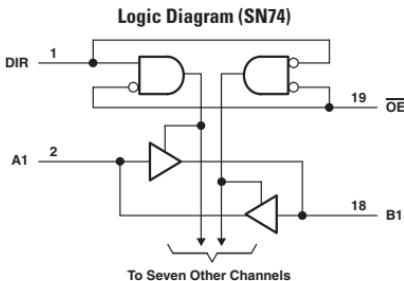
PARAMETER	INPUT	OUTPUT	MAX or MIN	ACT 11	SN74 ACT	CD74 ACT	AHC	AHCT	LV 3V	LV 5V	LV-AT	LVC 3V	LVC <sub>H</sub> 3V
I <sub>PLH</sub>	A	Y	MAX	9.9	10	8.7	8.5	9.5	13.5	8.5	9.5	5.9	5.9
I <sub>PHL</sub>				9.2	10	8.7	8.5	9.5	13.5	8.5	9.5	5.9	5.9
I <sub>PZH</sub>	OE	Y	MAX	12.5	9.5	12.2	10.5	13	16	10.5	13	7.6	7.6
I <sub>PZL</sub>				11.4	10.5	12.2	10.5	13	16	10.5	13	7.6	7.6
I <sub>PHZ</sub>	OE	Y	MAX	10.4	10.5	12.2	10.5	13	18	15.5	13	6.5	5.8
I <sub>PZL</sub>				11.2	10.5	12.2	10.5	13	18	15.5	13	6.5	5.8

PARAMETER	INPUT	OUTPUT	MAX or MIN	LVCZ 3V	ALVC 3V	ALVCH 3V	AUC 1.8V	AUC 2.3V	AUCH 1.8V	AUCH 2.3V
I <sub>PLH</sub>	A	Y	MAX	5.9	2.8	2.8	2.5	1.9	2.5	1.9
I <sub>PHL</sub>				5.9	2.8	2.8	2.5	1.9	2.5	1.9
I <sub>PZH</sub>	OE	Y	MAX	7.6	4.5	4.5	3.1	2.3	3.1	2.3
I <sub>PZL</sub>				7.6	4.5	4.5	3.1	2.3	3.1	2.3
I <sub>PHZ</sub>	OE	Y	MAX	6.5	4.2	4.2	4.2	2.3	4.2	2.3
I <sub>PZL</sub>				6.5	4.2	4.2	4.2	2.3	4.2	2.3

UNIT: ns

## OCTAL BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

- 3-State Outputs Drive Bus Lines Directly
- PNP Inputs Reduce DC Loading on Bus Lines
- 74AC11xxx: Product Available in Reduced-Noise Advanced CMOS (11000 Series)
- 74ACT11xxx: Product Available in Reduced-Noise Advanced CMOS (11000 Series)



FUNCTION TABLE

ENABLE G	DIRECTION CONTROL DIR	OPERATION
L	L	B data to A bus
L	H	A data to B bus
H	X	Isolation

### ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	LS	ALS	ALS A-1	AS	F	SN74 HC	CD74 HC	SN74 HCT	CD74 HCT	SN74 BCT	SN64 BCT	ABT	ABTH	UNIT
I <sub>CCH</sub>	MAX	70	45	45	97	90	0.08	0.16	0.08	0.16	57	57	0.25	0.25	mA
I <sub>CCL</sub>	MAX	90	55	55	143	120	0.08	0.16	0.08	0.16	90	90	30	30	mA
I <sub>CCZ</sub>	MAX	95	58	58	123	110	0.08	0.16	0.08	0.16	15	15	0.25	0.25	mA
I <sub>OH</sub> (A port)	MAX	-15	-15	-15	-15	-3	-6	-4	-6	-4	-3	-3	-32	-32	mA
I <sub>OH</sub> (B port)	MAX	-15	-15	-15	-15	-15	6	-4	-6	-4	-15	-15	-32	-32	mA
I <sub>OL</sub> (A port)	MAX	24	24	48	64	24	-6	4	6	4	24	24	64	64	mA
I <sub>OL</sub> (B port)	MAX	24	24	48	64	64	6	4	6	4	64	64	64	64	mA

PARAMETER	MAX or MIN	LVT 3V	LVTH 3V	LVTR 3V	AC 11	SN74 AC	CD74 AC	ACT 11	SN74 ACT	CD74 ACT	AHC	AHCT	LV 3V	LV 5V	UNIT
I <sub>CCH</sub>	MAX	0.19	0.19	0.19	0.08	0.04	0.16	0.08	0.04	0.16	0.04	0.04	-	0.02	mA
I <sub>CCL</sub>	MAX	5	5	12	0.08	0.04	0.16	0.08	0.04	0.16	0.04	0.04	-	0.02	mA
I <sub>CCZ</sub>	MAX	0.19	0.19	0.19	0.08	0.04	0.16	0.08	0.04	0.16	0.04	0.04	-	0.02	mA
I <sub>OH</sub> (A port)	MAX	-32	-32	-12	-24	-24	-24	-24	-24	-24	-8	-8	-8	-16	mA
I <sub>OH</sub> (B port)	MAX	-32	-32	-32	-24	-24	-24	-24	-24	-24	-8	-8	-8	-16	mA
I <sub>OL</sub> (A port)	MAX	64	64	32	24	24	24	24	24	24	8	8	8	16	mA
I <sub>OL</sub> (B port)	MAX	64	64	32	24	24	24	24	24	24	8	8	8	16	mA

PARAMETER	MAX or MIN	LV-AT	LVC 3V	LVCH 3V	LVCZ 3V	ALVC 3V	ALVCH 3V	AUC 1.8V	AUC 2.3V	AUCH 1.8V	AUCH 2.3V	UNIT
I <sub>CCH</sub>	MAX	0.02	0.01	0.01	0.1	0.01	0.01	0.02	0.02	0.02	0.02	mA
I <sub>CCL</sub>	MAX	0.02	0.01	0.01	0.1	0.01	0.01	0.02	0.02	0.02	0.02	mA
I <sub>CCZ</sub>	MAX	0.02	0.01	0.01	0.1	0.01	0.01	0.02	0.02	0.02	0.02	mA
I <sub>OH</sub> (A port)	MAX	-16	-24	-24	-24	-24	-24	-8	-9	-8	-9	mA
I <sub>OH</sub> (B port)	MAX	-16	-24	-24	-24	-24	-24	-8	-9	-8	-9	mA
I <sub>OL</sub> (A port)	MAX	16	24	24	24	24	24	8	9	8	9	mA
I <sub>OL</sub> (B port)	MAX	16	24	24	24	24	24	8	9	8	9	mA

## SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	LS	ALS	ALS A-1	AS	F	SN74 HC	CD74 HC	SN74 HCT	CD74 HCT	SN74 BCT
tp <sub>LH</sub>	A, B	B, A	MAX	12	10	10	7.5	7	26	33	28	39	7
tp <sub>HL</sub>				12	10	10	7	7	26	33	28	39	7
tp <sub>ZH</sub>	OE	A, B	MAX	40	20	20	9	8	58	45	58	48	10.9
tp <sub>ZL</sub>				40	20	20	8.5	9	58	45	58	48	11.6
tp <sub>HZ</sub>	OE	A, B	MAX	28	10	10	5.5	7.5	50	45	50	45	9.3
tp <sub> LZ</sub>				25	15	15	9.5	7.5	50	45	50	45	9.1

PARAMETER	INPUT	OUTPUT	MAX or MIN	SN64 BCT	ABT	ABTH	LVT 3V	LVTH 3V	AC 11	SN74 AC	CD74 AC	ACT 11	SN74 ACT
tp <sub>LH</sub>	A, B	B, A	MAX	7	3.6	3.6	3.5	3.5	9.5	7	8.5	10	8
tp <sub>HL</sub>				7	3.9	3.9	3.5	3.5	6.9	7	8.5	9.1	9
tp <sub>ZH</sub>	OE	A, B	MAX	10.9	5.6	5.6	5.5	5.5	11.4	9	14	13.2	11
tp <sub>ZL</sub>				11.6	6.2	6.2	5.5	5.5	9.5	9.5	14	12.9	12
tp <sub>HZ</sub>	OE	A, B	MAX	9.3	5.9	5.9	5.9	5.9	9.5	10	14	12.9	11
tp <sub> LZ</sub>				9.1	4.5	4.5	5	5	10.4	10	14	13.9	11

PARAMETER	INPUT	OUTPUT	MAX or MIN	CD74 ACT	AHC	AHCT	LV 3V	LV 5V	LV-AT	LVC 3V	LVCH 3V	LV CZ 3V	ALVC 3V
tp <sub>LH</sub>	A, B	B, A	MAX	10	8.5	9.5	13.5	8.5	9.5	6.3	6.3	6.3	3.4
tp <sub>HL</sub>				10	8.5	9.5	13.5	8.5	9.5	6.3	6.3	6.3	3.4
tp <sub>ZH</sub>	OE	A, B	MAX	14	12	16	19	12	16	8.5	8.5	8.5	5.5
tp <sub>ZL</sub>				14	12	16	19	12	16	8.5	8.5	8.5	5.5
tp <sub>HZ</sub>	OE	A, B	MAX	14.4	11	16.5	22	16	16.5	7.5	7.5	7.5	5.5
tp <sub> LZ</sub>				14.4	11	16.5	22	16	16.5	7.5	7.5	7.5	5.5

PARAMETER	INPUT	OUTPUT	MAX or MIN	ALVCH 3V	AUC 1.8V	AUC 2.3V	AUCH 1.8V	AUCH 2.3V
tp <sub>LH</sub>	A, B	B, A	MAX	3.4	2.2	1.8	2.2	1.8
tp <sub>HL</sub>				3.4	2.2	1.8	2.2	1.8
tp <sub>ZH</sub>	OE	A, B	MAX	5.5	3	2.4	3	2.4
tp <sub>ZL</sub>				5.5	3	2.4	3	2.4
tp <sub>HZ</sub>	OE	A, B	MAX	5.5	4	2.6	4	2.6
tp <sub> LZ</sub>				5.5	4	2.6	4	2.6

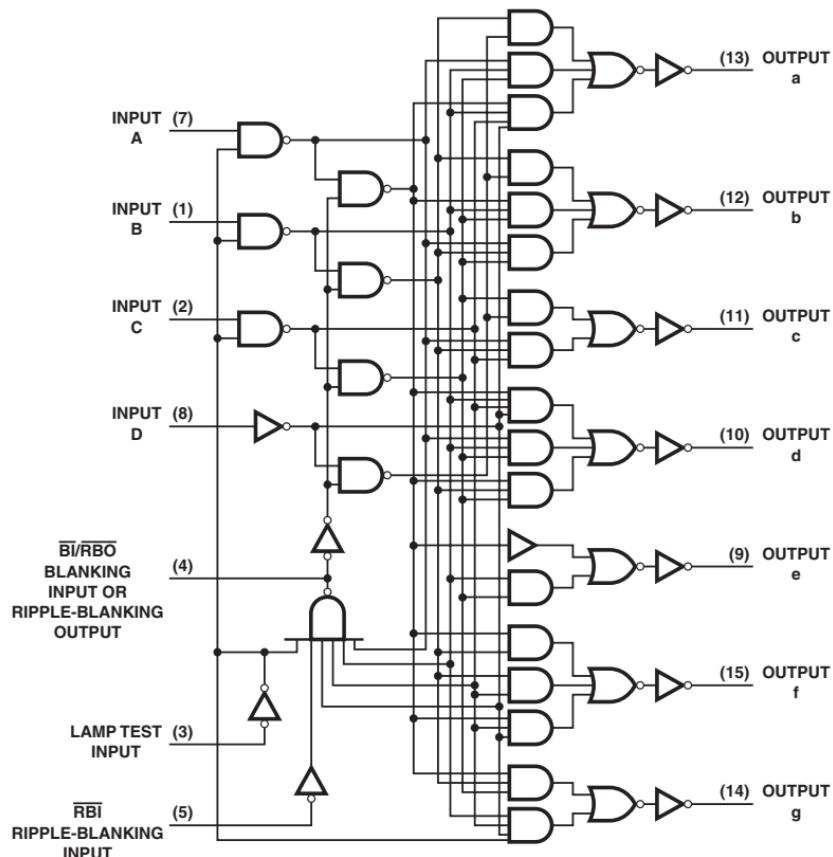
PARAMETER	INPUT	OUTPUT	MAX or MIN	LVTR 3V
tp <sub>LH</sub>	A	B	MAX	4.2
		A		4.4
tp <sub>HL</sub>	A	B	MAX	4.6
		A		4.1
tp <sub>ZH</sub>	OE	B	MAX	5.5
		A		6
tp <sub>ZL</sub>	OE	B	MAX	6.6
		A		6.4
tp <sub>HZ</sub>	OE	B	MAX	6.1
		A		5.8
tp <sub> LZ</sub>	OE	B	MAX	5.2
		A		5.2

UNIT: ns

## BCD-TO-SEVEN-SEGMENT DECODERS/DRIVERS

- Open-Collector Outputs Drive Indicators Directly
- Lamp-Test Provision
- Leading/Trailing Zero Suppression

Logic Diagram



FUNCTION TABLE

DECIMAL OR FUNCTION	INPUTS					BI/RBO	OUTPUTS						
	LT	RBI	D	C	B	A	a	b	c	d	e	f	g
0	H	H	L	L	L	L	H	ON	ON	ON	ON	ON	ON
1	H	X	L	L	L	H	H	OFF	ON	ON	OFF	OFF	OFF
2	H	X	L	L	H	L	H	ON	ON	OFF	ON	OFF	ON
3	H	X	L	H	L	H	H	ON	ON	ON	ON	OFF	ON
4	H	X	L	H	L	L	H	OFF	ON	ON	OFF	OFF	ON
5	H	X	L	H	L	H	H	ON	OFF	ON	ON	ON	ON
6	H	X	L	H	H	L	H	ON	OFF	ON	ON	ON	ON
7	H	X	L	H	H	H	H	ON	ON	ON	OFF	OFF	OFF
8	H	X	H	L	L	L	H	ON	ON	ON	ON	ON	ON
9	H	X	X	H	L	L	H	ON	ON	ON	OFF	ON	ON
10	H	X	X	H	L	H	H	OFF	OFF	ON	ON	OFF	ON
11	H	X	X	H	L	H	H	OFF	ON	ON	OFF	ON	ON
12	H	X	H	H	L	L	H	OFF	ON	OFF	OFF	OFF	ON
13	H	X	H	H	L	H	H	ON	OFF	ON	OFF	ON	ON
14	H	X	H	H	H	L	H	OFF	OFF	ON	ON	ON	ON
15	H	X	H	H	H	H	H	OFF	OFF	OFF	OFF	OFF	OFF
BI	X	X	X	X	X	X	L	OFF	OFF	OFF	OFF	OFF	OFF
RBI	H	L	L	L	L	L	L	OFF	OFF	OFF	OFF	OFF	OFF
LT	L	X	X	X	X	X	H	ON	ON	ON	ON	ON	ON

## ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER		MAX or MIN	TTL	LS	UNIT	
Icc		MAX	103	13	mA	
Vo (off)	a thru g	MAX	15	15	V	
		MAX	40	24	mA	
Io (on)		BI/RBO	MAX	-0.2	-0.05 mA	
Ioh		MAX	8	3.2	mA	
UNIT: ns						

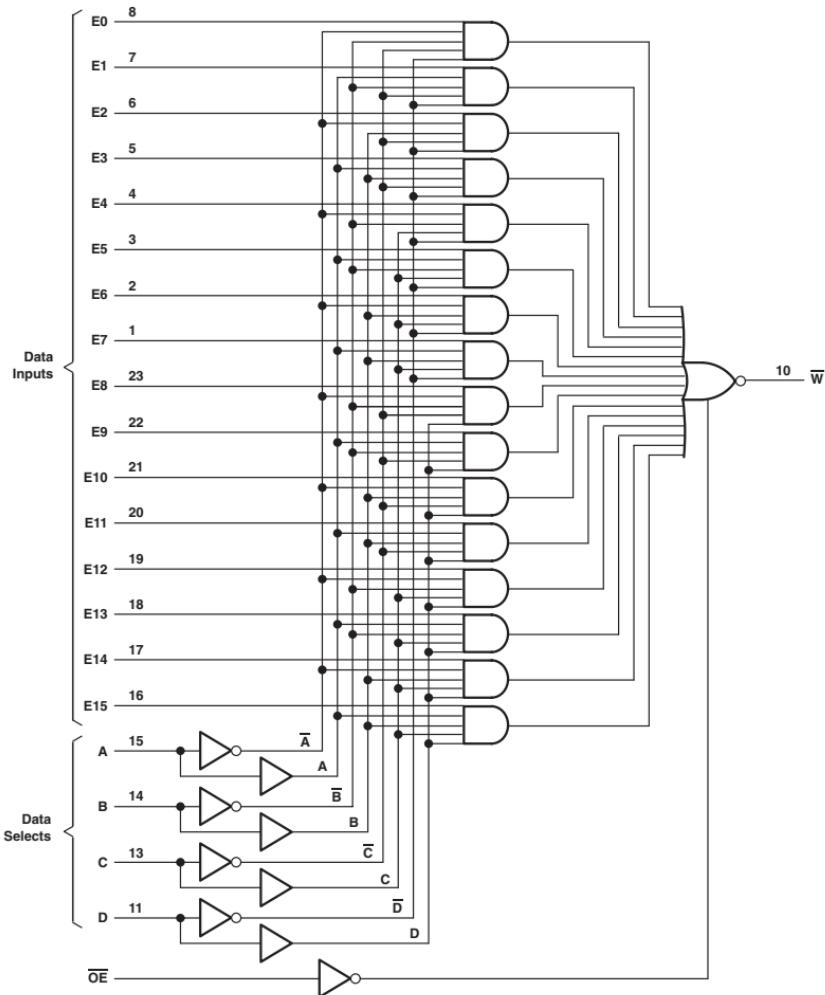
## TIMING REQUIREMENTS AND SWITCHING CHARACTERISTICS

PARAMETER		MAX or MIN	TTL	LS
toff	INPUT A	MIN	100	100
			100	100
ton	INPUT RBI	MIN	100	100
			100	100

UNIT: ns

**1-OF-16 DATA GENERATORS/MULTIPLEXERS WITH 3-STATE OUTPUTS**

- 4-Line to 1-Line Multiplexers That Can Select 1-of-16 Data Inputs
- Applications:
  - Boolean Function Generator
  - Parallel-to-Serial Converter
  - Data Source Selector
- Buffered 3-State Bus Driver Inputs Permit Multiplexing From n Lines to One Line
- 3-State Outputs

**Logic Diagram**

FUNCTION TABLE

INPUTS					OUTPUT	
$\bar{OE}$	A	B	C	D	EI	W
L	L	L	L	L	E0	$\bar{E}0$
L	H	L	L	L	E1	$\bar{E}1$
L	L	H	L	L	E2	$\bar{E}2$
L	H	H	L	L	E3	$\bar{E}3$
L	L	L	H	L	E4	$\bar{E}4$
L	H	L	H	L	E5	$\bar{E}5$
L	L	H	H	L	E6	$\bar{E}6$
L	H	H	H	L	E7	$\bar{E}7$
L	L	L	L	H	E8	$\bar{E}8$
L	H	L	L	H	E9	$\bar{E}9$
L	L	H	L	H	E10	$\bar{E}10$
L	H	H	L	H	E11	$\bar{E}11$
L	L	L	H	H	E12	$\bar{E}12$
L	H	L	H	H	E13	$\bar{E}13$
L	L	H	H	H	E14	$\bar{E}14$
L	H	H	H	H	E15	$\bar{E}15$
H	X	X	X	X	X	Z

## ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	AS	UNIT
$I_{CC}$	MAX	50	mA
$I_{OH}$	MAX	-15	mA
$I_{OL}$	MAX	48	mA

## SWITCHING CHARACTERISTICS

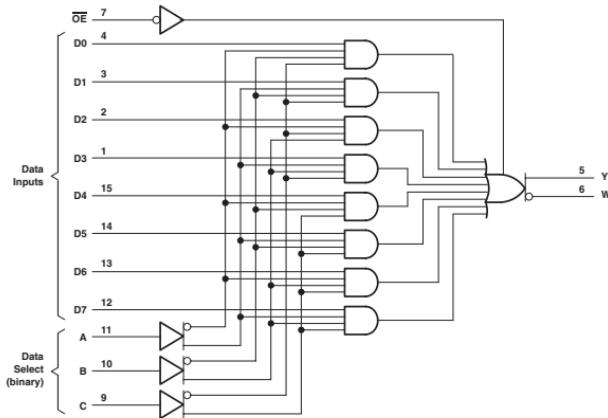
PARAMETER	INPUT	OUTPUT	MAX or MIN	AS
$t_{PLH}$	DATA	$\bar{W}$	MAX	8
		$\bar{W}$	MAX	7
$t_{PHL}$	SELECT	$\bar{W}$	MAX	13
		$\bar{W}$	MAX	10.5
$t_{PZH}$	$\bar{OE}$	$\bar{W}$	MAX	7
		$\bar{W}$	MAX	9
$t_{PZL}$	$\bar{OE}$	$\bar{W}$	MAX	6
		$\bar{W}$	MAX	6.5

UNIT: ns

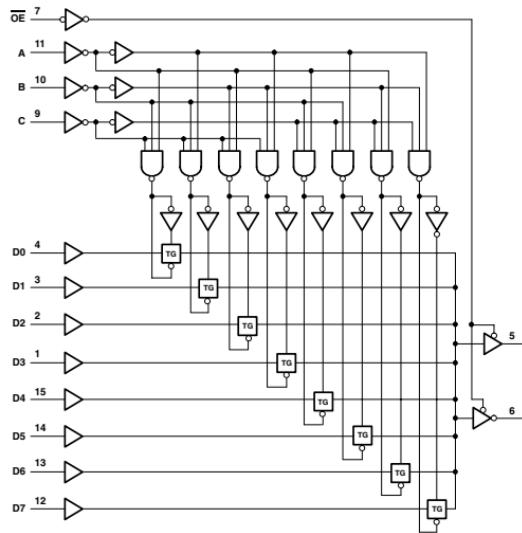
## DATA SELECTORS/MULTIPLEXERS WITH 3-STATE OUTPUTS

- 3-State Version of '151
- 3-State Outputs Interface Directly with System Bus
- Perform Parallel-to-Serial Conversion
- Complementary Outputs Provide True and Inverted Data

Logic Diagram (SN74ALS,F)



Logic Diagram (SN74HC)



**FUNCTION TABLE (SN74)**

INPUTS			OUTPUTS		
SELECT C	B	A	STROBE OE	Y	W
X	X	X	H	Z	Z
L	L	L	L	D0	D0
L	L	H	L	D1	D1
L	H	L	L	D2	D2
L	H	H	L	D3	D3
H	L	L	L	D4	D4
H	L	H	L	D5	D5
H	H	L	L	D6	D6
H	H	H	L	D7	D7

**ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS**

PARAMETER	MAX or MIN	TTL	LS	S	ALS	F	SN74 HC	CD74 HC	CD74 HCT	SN74 AC	CD74 AC	UNIT
I <sub>CC</sub>	MAX	62	12	85	14	24	0.08	0.16	0.16	0.16	0.16	mA
I <sub>OH</sub>	MAX	-5.2	-2.6	-6.5	-2.6	-3	-6	-4	-4	-24	-24	mA
I <sub>OL</sub>	MAX	16	8	20	24	24	6	4	4	24	24	mA

**SWITCHING CHARACTERISTICS**

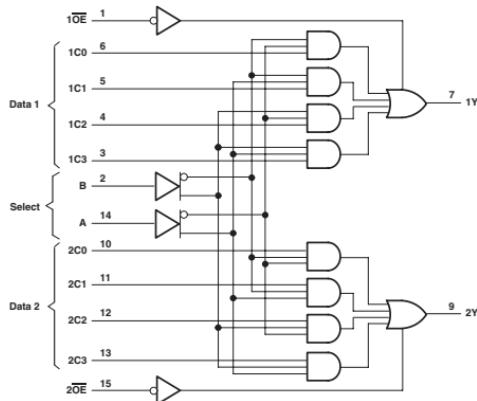
PARAMETER	INPUT	OUTPUT	MAX or MIN	TTL	LS	S	ALS	F	SN74 HC	CD74 HC	CD74 HCT	SN74 AC	CD74 AC
I <sub>PLH</sub> I <sub>PHL</sub>	A, B, C (CD74: S <sub>0</sub> , S <sub>1</sub> , S <sub>2</sub> )	Y	MAX	45	45	18	18	9.5	51	74	63	18.2	18.2
				45	45	19.5	24	7.5	51	74	63	18.2	18.2
I <sub>PLH</sub> I <sub>PHL</sub>	A, B, C (CD74: S <sub>0</sub> , S <sub>1</sub> , S <sub>2</sub> )	W (CD74: $\bar{Y}$ )	MAX	33	33	15	24	12.5	51	74	63	19.6	19.6
				33	33	13.5	23	9	51	74	63	19.6	19.6
I <sub>PLH</sub> I <sub>PHL</sub>	ANY D (CD74: ANYI)	Y	MAX	28	28	12	10	7	49	53	53	13.5	13.5
				28	28	12	15	5	49	53	53	13.5	13.5
I <sub>PLH</sub> I <sub>PHL</sub>	ANY D (CD74: ANYI)	W (CD74: $\bar{Y}$ )	MAX	15	15	7	15	8	49	53	53	14.9	14.9
				15	15	7	15	8	49	53	53	14.9	14.9
I <sub>PZH</sub> I <sub>PZL</sub>	$\bar{G}$	Y	MAX	27	45	19.5	15	7	36	42	45	13.5	13.5
				40	40	21	15	6.5	36	42	45	13.5	13.5
I <sub>PZH</sub> I <sub>PZL</sub>	$\bar{G}$	W (CD74: $\bar{Y}$ )	MAX	27	27	19.5	15	6	36	42	45	13.5	13.5
				40	40	21	15	4.5	36	42	45	13.5	13.5
I <sub>PZH</sub> I <sub>PZL</sub>	$\bar{G}$	Y	MAX	8	45	8.5	10	8.5	49	42	45	13.5	13.5
				23	25	14	10	8	49	42	45	13.5	13.5
I <sub>PZH</sub> I <sub>PZL</sub>	$\bar{G}$	W (CD74: $\bar{Y}$ )	MAX	8	55	8.5	10	5.5	49	42	45	13.5	13.5
				23	25	14	10	4.5	49	42	45	13.5	13.5

UNIT: ns

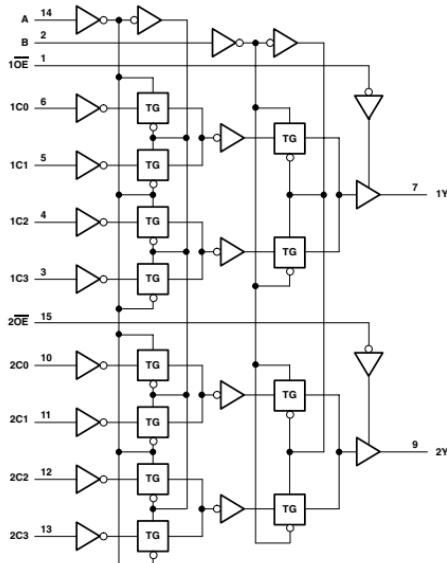
## DUAL 4-LINE TO 1-LINE DATA SELECTORS/MULTIPLEXERS WITH 3-STATE OUTPUTS

- 3-State Version of '153
- Perform Parallel-to-Serial Conversion

Logic Diagram (SN74ALS, AS, F)



Logic Diagram (SN74HC)



FUNCTION TABLE (SN74)

SELECT INPUTS		DATA INPUTS			OUTPUT CONTROL	OUTPUT	
B	A	C0	C1	C2	C3	$\bar{OE}$	Y
X	X	X	X	X	X	H	Z
L	L	L	X	X	X	L	L
L	L	H	X	X	X	L	H
L	H	X	L	X	X	L	L
L	H	H	X	X	X	L	H
H	L	X	X	L	X	L	L
H	L	X	X	H	X	L	H
H	H	X	X	X	L	L	L
H	H	X	X	X	H	L	H

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	LS	ALS	AS	F	SN74 HC	CD74 HC	CD74 HCT	CD74 AC	CD74 ACT	UNIT
$I_{CC}$	MAX	14	14	33	23	0.08	0.16	0.16	0.16	0.16	mA
$I_{OH}$	MAX	-2.6	-2.6	-15	-3	-6	-6	-4	-24	-24	mA
$I_{OL}$	MAX	8	24	48	24	6	6	4	24	24	mA

SWITCHING CHARACTERISTICS

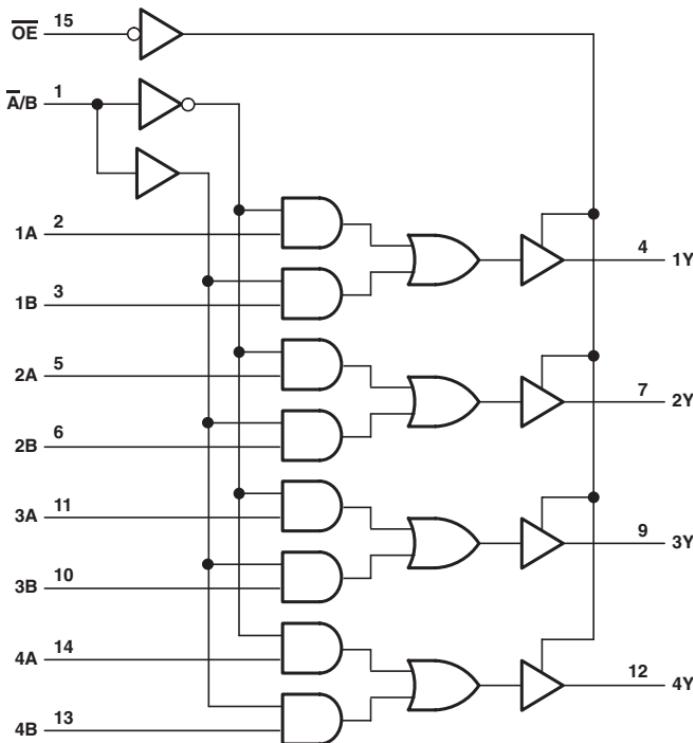
PARAMETER	INPUT	OUTPUT	MAX or MIN	LS	ALS	AS	F	SN74 HC	CD74 HC	CD74 HCT	CD74 AC	CD74 ACT
$t_{PLH}$	DATA	Y	MAX	25	10	7.5	8	35	53	57	13.3	18
				20	14	8	7	35	53	57	13.3	18
$t_{PLH}$	SELECT	Y	MAX	45	21	13.5	13	38	53	60	20	22
				32	21	11.5	10	38	53	60	20	22
$t_{PZH}$	$\bar{OE}$	Y	MAX	28	14	12.5	9	25	33	45	11.5	12.6
				23	16	11.5	9	25	33	45	11.5	12.6
$t_{PHZ}$	$\bar{OE}$	Y	MAX	41	10	6	6	38	45	45	11.5	12.6
				27	14	7	7	38	45	45	11.5	12.6

UNIT: ns

## QUADRUPLE 2-LINE TO 1-LINE DATA SELECTORS/MULTIPLEXERS WITH 3-STATE OUTPUTS

- 3-State Outputs Interface Directly with System Bus
- Provides Bus Interface from Multiple Sources in High-Performance Systems

Logic Diagram (SN74)



**FUNCTION TABLE (SN74)**

INPUTS			OUTPUT Y
OUTPUT CONTROL $\overline{OE}$	SELECT $\overline{A}/B$	A B	
H	X	X X	Z
L	L	L X	L
L	L	H X	H
L	H	X L	L
L	H	X H	H

**ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS**

PARAMETER	MAX or MIN	LS	S	ALS	AS	F	SN74 HC	CD74 HC	SN74 HCT	CD74 HCT	AC 11	CD74 AC	ACT 11	UNIT
I <sub>CC</sub>	MAX	19	87	14	31.9	23	0.08	0.16	0.08	0.16	0.08	0.16	0.08	mA
I <sub>OH</sub>	MAX	-2.6	-6.5	-2.6	-15	-3	-6	-6	-6	-6	-24	-24	-24	mA
I <sub>OL</sub>	MAX	24	20	24	48	24	6	6	6	6	24	24	24	mA

PARAMETER	MAX or MIN	CD74 ACT	LVC 3V	UNIT
I <sub>CC</sub>	MAX	0.16	0.01	mA
I <sub>OH</sub>	MAX	-24	-24	mA
I <sub>OL</sub>	MAX	24	24	mA

**SWITCHING CHARACTERISTICS**

PARAMETER	INPUT	OUTPUT	MAX or MIN	LS	S	ALS	AS	F	SN74 HC	CD74 HC	SN74 HCT	CD74 HCT
t <sub>PLH</sub>	DATA	ANY	MAX	13	7.5	10	5.5	7	25	45	38	50
t <sub>PHL</sub>				15	6.5	12	6	6.5	25	45	38	50
t <sub>PLH</sub>	SELECT	ANY	MAX	21	15	18	11	15	25	53	38	57
t <sub>PHL</sub>				24	15	22	10	9.5	25	53	38	57
t <sub>PZH</sub>	$\overline{OE}$	Y	MAX	30	19.5	16	7.5	8.5	38	45	38	45
t <sub>PZL</sub>				30	21	18	9.5	8.5	38	45	38	45
t <sub>PHZ</sub>	$\overline{OE}$	Y	MAX	30	8.5	10	6.5	7	38	45	38	45
t <sub>PLZ</sub>				25	14	15	7	7	38	45	38	45

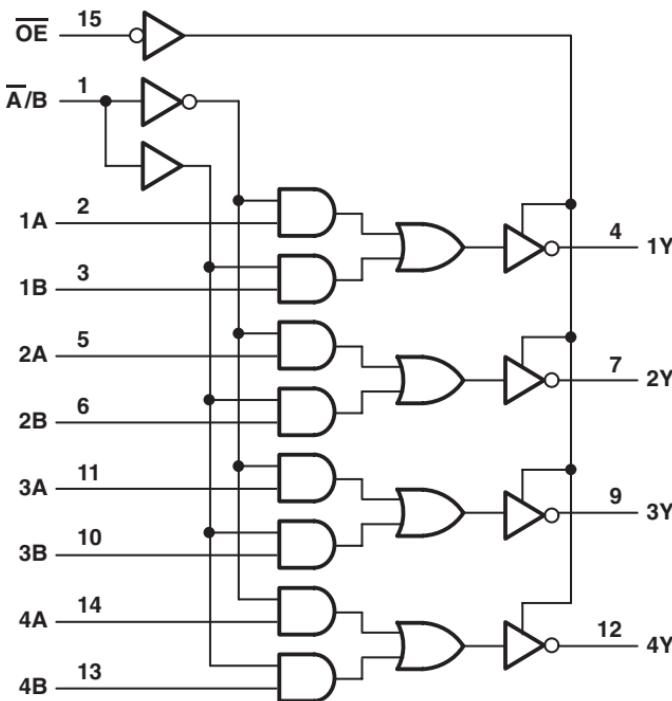
PARAMETER	INPUT	OUTPUT	MAX or MIN	AC 11	CD74 AC	ACT 11	CD74 ACT	LVC 3V
t <sub>PLH</sub>	DATA	ANY	MAX	6.4	9.3	6.9	10.7	4.6
t <sub>PHL</sub>				7.2	9.3	8.7	10.7	4.6
t <sub>PLH</sub>	SELECT	ANY	MAX	7.2	13.4	8.2	15.4	6.4
t <sub>PHL</sub>				7.9	13.4	9.4	15.4	6.4
t <sub>PZH</sub>	$\overline{OE}$	Y	MAX	6.5	14.7	7.3	16.1	5.6
t <sub>PZL</sub>				8.6	14.7	9.6	16.1	5.6
t <sub>PHZ</sub>	$\overline{OE}$	Y	MAX	7.6	14.7	8.4	16.1	4.3
t <sub>PLZ</sub>				7.6	14.7	8.5	16.1	4.3

UNIT: ns

## QUADRUPLE 4-LINE TO 1-LINE DATA SELECTORS/MULTIPLEXERS WITH 3-STATE OUTPUTS

- 3-State Outputs Interface Directly with System Bus
- Provides Bus Interface from Multiple Sources in High-Performance Systems

Logic Diagram (SN74)



FUNCTION TABLE

INPUTS			OUTPUT Y
OUTPUT CONTROL $\bar{OE}$	SELECT $\bar{A}/B$	A B	
H	X	X X	Z
L	L	L X	H
L	L	H X	L
L	H	X L	H
L	H	X H	L

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	LS	S	ALS	AS	F	SN74 HC	CD74 HC	CD74 HCT	CD74 ACT	UNIT
I <sub>CC</sub>	MAX	16	87	13	25.2	23	0.08	0.16	0.16	0.16	mA
I <sub>OH</sub>	MAX	-2.6	-6.5	-2.6	-15	-3	-6	-6	-6	-24	mA
I <sub>OL</sub>	MAX	8	20	24	48	24	6	6	6	24	mA

SWITCHING CHARACTERISTICS

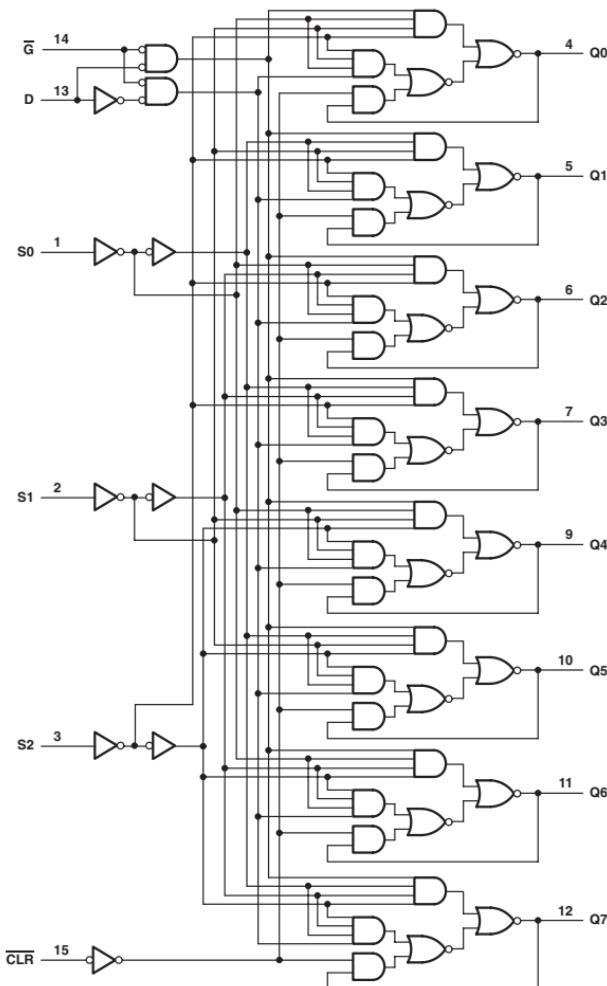
PARAMETER	INPUT	OUTPUT	MAX or MIN	LS	S	ALS	AS	F	SN74 HC	CD74 HC	CD74 HCT	CD74 ACT
I <sub>PZH</sub>	DATA	Y	MAX	12	6	8	5	6	25	24	34	10.7
I <sub>PHL</sub>				17	6	7	4	5.5	25	24	34	10.7
I <sub>PLH</sub>	SELECT	Y	MAX	21	12	25	9.5	9.5	25	35	43	15.4
I <sub>PHL</sub>				24	12	20	10	11	25	35	43	15.4
I <sub>PZL</sub>	G̅	Y	MAX	30	19.5	18	8	8.5	38	35	35	16.1
I <sub>PZL</sub>				30	21	18	10	8.5	38	35	35	16.1
I <sub>PZL</sub>	G̅	Y	MAX	30	8.5	10	6	7	38	38	38	16.1
I <sub>PZL</sub>				25	14	18	6.5	7	38	38	38	16.1

UNIT: ns

## 8-BIT ADDRESSABLE LATCHES

- 8-Bit Parallel-Out Storage Register Performs Serial-to-Parallel Conversion with Storage
- Asynchronous Parallel Clear
- Active-High Decoder
- Enable/Disable Input Simplifies Expansion
- Expandable for n-Bit Applications
- Four Distinct Functional Modes

Logic Diagram (SN74ALS)



**LATCH SELECTION**

SELECT INPUTS	LATCH ADDRESSED		
C	B	A	
L	L	L	0
L	L	H	1
L	H	L	2
L	H	H	3
H	L	L	4
H	L	H	5
H	H	L	6
H	H	H	7

**FUNCTION TABLE (SN74)**

INPUTS	OUTPUT OF ADDRESSED LATCH	EACH OTHER OUTPUT	FUNCTION
CLEAR	G		
H	L	D	Q10
H	H	Q10	Q10
L	L	D	L
L	H	L	L

Addressable latch  
Memory  
8-line demultiplexer  
Clear

**ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS**

PARAMETER	MAX or MIN	TTL	LS	ALS	SN74 HC	CD74 HC	CD74 HCT	UNIT
I <sub>CC</sub>	MAX	90	36	22	0.08	0.16	0.16	mA
I <sub>OH</sub>	MAX	16	8	8	4	4	4	mA
I <sub>OL</sub>	MAX	-0.8	-0.4	-0.4	-4	-4	-4	mA

**TIMING REQUIREMENTS AND SWITCHING CHARACTERISTICS**

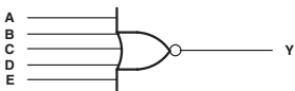
PARAMETER	INPUT	OUTPUT	MAX or MIN	TTL	LS	ALS	SN74	CD74	CD74
							HC	HC	HCT
t <sub>w</sub>	G (CDHC/HCT: LE)		MIN	15	17	15	20	21	27
	CLR (CDHC/HCT: MR)			15	10	10	20	21	27
t <sub>su</sub>	DATA		MIN	15	20	15	19	24	26
	ADDRESS			5	17	15	19	24	26
t <sub>h</sub>	DATA		MIN	0	0	0	5	0	0
	ADDRESS			20	0	0	5	0	0
t <sub>PLH</sub>	CLEAR (CDHC/HCT: MR)	Any Q	MAX	25	18	12	38	47	59
t <sub>PHL</sub>	DATA	Any Q	MAX	24	30	19	33	56	59
t <sub>PLH</sub>				20	20	12	33	-	59
t <sub>PHL</sub>	ADDRESS	Any Q	MAX	28	27	22	50	56	61
t <sub>PLH</sub>				28	20	12	50	-	61
t <sub>PHL</sub>	ENABLE	Any Q	MAX	20	24	20	43	51	57
t <sub>PLH</sub>				20	24	13	43	-	57

UNIT: ns

## DUAL 5-INPUT POSITIVE-NOR GATES

- $Y = \overline{A + B + C + D + E}$

## Logic Diagram



ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	S	F	UNIT
$I_{CC}$	MAX	45	9.5	mA
$I_{OH}$	MAX	-1	-1	mA
$I_{OL}$	MAX	20	20	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	S	F
$t_{PLH}$	A, B, C, D, E	Y	MAX	5.5	6.5
$t_{PHL}$				6	4.5

UNIT: ns

## QUADRUPLE COMPLEMENTARY-OUTPUT ELEMENTS

- $Y = \overline{A}, W = A$
- $Y = AB, W = AB$

## Logic Diagram



ELEMENTS 1 and 4



ELEMENTS 2 and 3

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	TTL	UNIT
$I_{CC}$	MAX	34	mA
$I_{OH}$	MAX	-0.8	mA
$I_{OL}$	MAX	16	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	TTL
$t_{PLH}(W)$	A or B	W	MAX	18
$t_{PHL}(Y)$	A or B	Y	MAX	18
$t_{PLH}(W)$	A or B	W	MAX	18
$t_{PHL}(Y)$	A or B	Y	MAX	18
$t_{PLH}(W)$	A or B	W with respect Y	MAX	$\pm 3$
$t_{PHL}(W)$	A or B	W with respect Y	MAX	$\pm 3$

UNIT: ns

**QUADRUPLE 2-INPUT EXCLUSIVE-NOR GATES  
WITH OPEN-DRAIN OUTPUTS**

- $Y = \overline{A} \oplus \overline{B}$



FUNCTION TABLE

INPUTS		OUTPUT
A	B	Y
L	L	H
L	H	L
H	L	L
H	H	H

## ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	LS	SN74 HC	UNIT
$I_{CC}$	MAX	13	0.02	mA
$V_{OH}$	MAX	5.5	$V_{cc}$	V
$I_{OL}$	MAX	8	4	mA

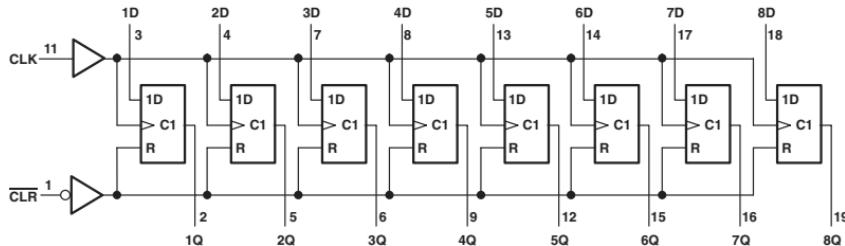
## SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	LS	SN74 HC
$t_{PLH}$	A or B Other INPUT Low	Y	MAX	30	31
$t_{PHL}$	A or B Other INPUT Low	Y	MAX	30	25
$t_{PLH}$	A or B Other INPUT High	Y	MAX	30	31
$t_{PHL}$	A or B Other INPUT High	Y	MAX	30	25

UNIT: ns

**OCTAL D-TYPE FLIP-FLOPS WITH CLEAR**

- Contain Eight Flip-Flops with Single-Rail Outputs
- Buffered Clock and Direct-Clear Inputs

**Logic Diagram (SN74)****FUNCTION TABLE (SN74)**

INPUTS		OUTPUT	
CLEAR	CLOCK	D	Q
L	X	X	L
H	↑	H	H
H	↑	L	L
H	L	X	$Q_0$

## ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	TTL	LS	ALS	SN74 HC	CD74 HC	SN74 HCT	CD74 HCT	ABT	LVTH 3V	CD74 AC	CD74 ACT	UNIT
I <sub>CC</sub>	MAX	94	27	29	0.08	0.16	0.08	0.16	30	5	0.16	0.16	mA
I <sub>OH</sub>	MAX	-0.8	-0.4	-2.6	-4	-4	-4	-4	-32	-32	-24	-24	mA
I <sub>OL</sub>	MAX	16	8	24	4	4	4	4	64	64	24	24	mA

PARAMETER	MAX or MIN	AHC	AHCT	LV 3V	LV 5V	UNIT
I <sub>CC</sub>	MAX	0.04	0.04	-	0.02	mA
I <sub>OH</sub>	MAX	-8	-8	-6	-12	mA
I <sub>OL</sub>	MAX	8	8	6	12	mA

## TIMING REQUIREMENTS AND SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	TTL	LS	ALS	SN74 HC	CD74 HC	SN74 HCT	CD74 HCT	ABT
f <sub>max</sub>			MIN	30	30	35	21	20	16	16	150
t <sub>w</sub>			MIN	16.5	20	14	20	24	25	30	3.3
t <sub>su</sub>	DATA INPUT		MIN	20	20	10	25	18	25	18	2.5
	CLR INACTIVE		MIN	25	25	15	25	-	25	-	2
t <sub>th</sub>			MIN	5	5	0	0	3	0	3	1.2
t <sub>PLH</sub>	CLEAR	ANY Q	MAX	27	27	18	40	45	42	48	7.4
t <sub>PLH</sub>				27	27	12	40	45	42	45	6.5
t <sub>PLH</sub>	CLOCK	ANY Q	MAX	27	27	15	40	45	42	45	7.3

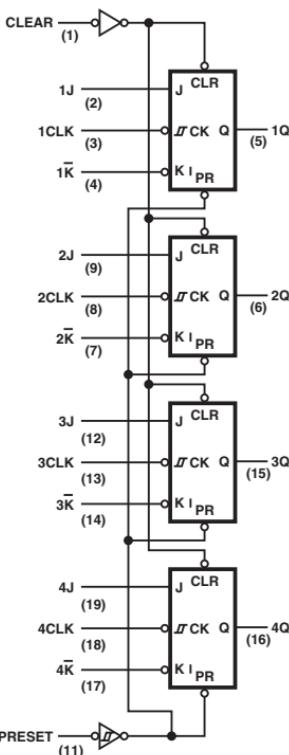
PARAMETER	INPUT	OUTPUT	MAX or MIN	LVTH 3V	CD74 AC	CD74 ACT	AHC	AHCT	LV 3V	LV 5V
f <sub>max</sub>			MIN	150	100	85	70	45	45	70
t <sub>w</sub>			MIN	3.3	5	6	5	6.5	6.5	5
t <sub>su</sub>	DATA INPUT		MIN	2.3	2	2	4.5	5	6.5	4.5
	CLR INACTIVE		MIN	2.3	-	-	2	2.5	2.5	2
t <sub>th</sub>			MIN	0	2	2	1	0	1	1
t <sub>PLH</sub>	CLEAR	ANY Q	MAX	4.3	13.5	13.5	12	12.6	19.5	12
t <sub>PLH</sub>				4.9	13.5	13.5	12.5	9.8	19.5	12.5
t <sub>PLH</sub>	CLOCK	ANY Q	MAX	4.8	13.5	13.5	12.5	11	19.5	12.5

UNIT f<sub>max</sub> : MHz, other : ns

## QUADRUPLE J-K FLIP-FLOPS

- Separate Negative-Edge-Triggered Clocks
- Fully Buffered Outputs

Logic Diagram



FUNCTION TABLE

COMMON INPUTS	INPUTS			OUTPUT	
PRESET	CLEAR	CLOCK	J	K	Q
L	H	X	X	X	H
H	L	X	X	X	L
L	L	X	X	X	Ht
H	H	↓	L	H	Q <sub>0</sub>
H	H	↓	H	H	H
H	H	↓	L	L	L
H	H	↓	H	L	TOGGLE
H	H	H	X	X	Q <sub>0</sub>

† The output levels in this configuration are not guaranteed to meet the minimum levels for  $V_{OH}$ . Furthermore, this configuration is nonstable; that is, it will not persist when either PRE or CLR returns to its inactive (high) level.

## ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	TTL	UNIT
$I_{CC}$	MAX	81	mA
$I_{OH}$	MAX	-0.8	mA
$I_{OL}$	MAX	16	mA

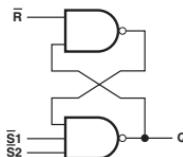
## TIMING REQUIREMENTS AND SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	TTL
fmax			MIN	35
t <sub>w</sub>	CLOCK high		MIN	13.5
	CLOCK low		MIN	15
tsu	J, K		MIN	3
	CLR, PRE		MIN	10
t <sub>h</sub>			MIN	10
t <sub>PLH</sub>	PRESET	Q	MAX	25
t <sub>PHL</sub>	CLEAR	Q	MAX	30
t <sub>PLH</sub>		Q	MAX	30
t <sub>PHL</sub>	CLOCK	Q	MAX	30

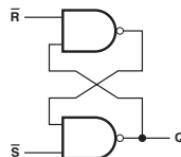
UNIT fmax : MHz, other : ns

QUADRUPLE  $\bar{S}$ - $\bar{R}$  LATCHES

(latches 1 and 3)



(latches 2 and 4)

FUNCTION TABLE  
(each latch)

INPUTS		OUTPUT
$\bar{S}$	$\bar{R}$	Q
H	H	$Q_0$
L	H	H
H	L	L
L	L	H‡

H = high level L = low level

†For latches with double S inputs:

Q<sub>0</sub> = the level of Q before the indicated input conditions were established.‡This configuration is nonstable; that is, it may not persist when the  $\bar{S}$  and  $\bar{R}$  inputs return to their inactive (high) level.

H = both S inputs high

L = one or both  $\bar{S}$  inputs low

## ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	TTL	LS	UNIT
I <sub>CC</sub>	MAX	30	7	mA
I <sub>OH</sub>	MAX	-0.8	-0.4	mA
I <sub>OL</sub>	MAX	16	8	mA

## TIMING REQUIREMENTS AND SWITCHING CHARACTERISTICS

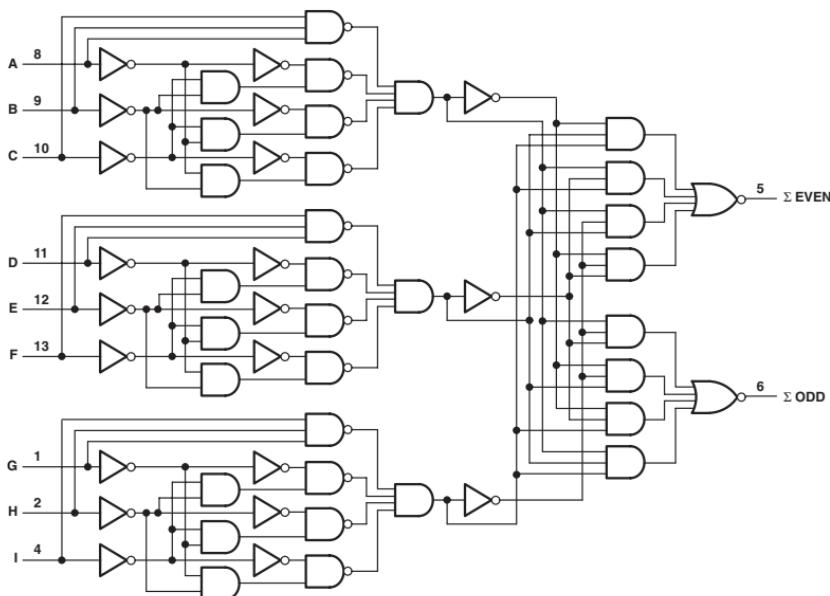
PARAMETER	INPUT	OUTPUT	MAX or MIN	TTL	LS
t <sub>W</sub>			MIN	20	20
t <sub>PLH</sub>	$\bar{S}$	Q	MAX	22	22
t <sub>PHL</sub>			MAX	15	21
t <sub>PHL</sub>	$\bar{R}$		MAX	27	27

UNIT: ns

## 9-BIT PARITY GENERATORS/CHECKERS

- Generate Either Odd or Even Parity for Nine Data Lines
- Cascadable for n-Bit Parity

Logic Diagram (SN74)



**FUNCTION TABLE (SN74)**

NO. OF INPUTS A-I THAT ARE HIGH	OUTPUTS	
	$\Sigma$ EVEN	$\Sigma$ ODD
0, 2, 4, 6, 8	H	L
1, 3, 5, 7, 9	L	H

**ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS**

PARAMETER	MAX or MIN	LS	S	ALS	AS	F	SN74 HC	CD74 HC	CD74 HCT	CD74 AC	CD74 ACT	UNIT
I <sub>CC</sub>	MAX	27	105	16	35	35	0.08	0.16	0.16	0.16	0.16	mA
I <sub>OH</sub>	MAX	-0.4	-1	-2.6	-2	-1	-4	-4	-4	-24	-24	mA
I <sub>OL</sub>	MAX	8	20	24	20	20	4	4	4	24	24	mA

**SWITCHING CHARACTERISTICS**

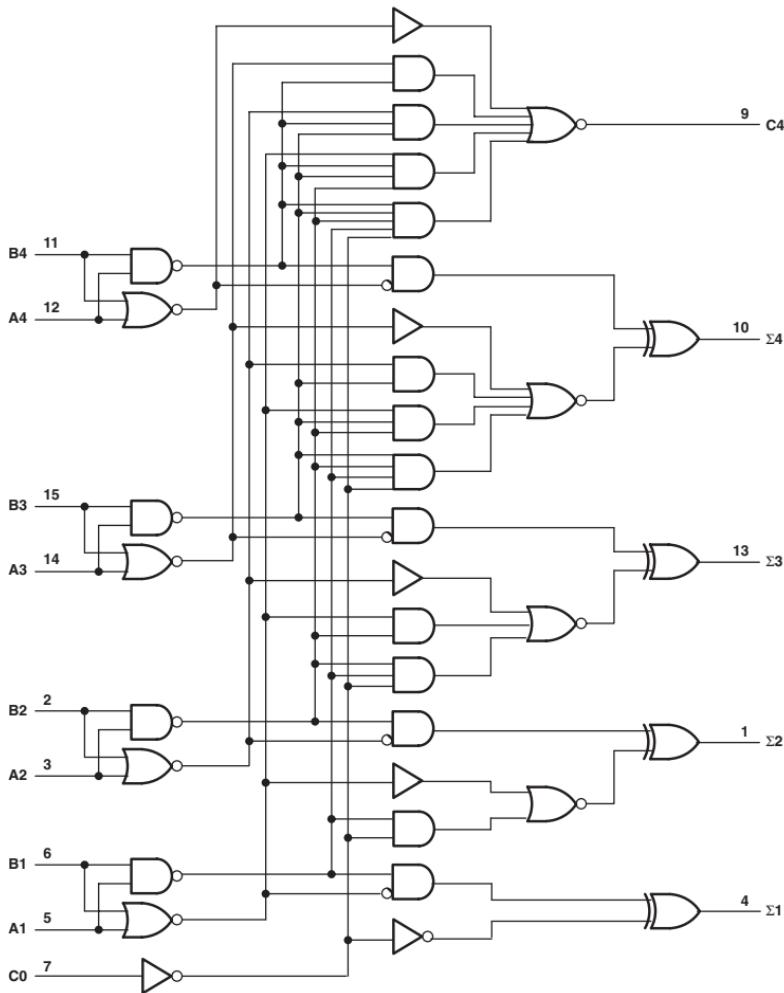
PARAMETER	INPUT	OUTPUT	MAX or MIN	LS	S	ALS	AS	F	SN74 HC	CD74 HC	CD74 HCT	CD74 AC	CD74 ACT
I <sub>PLH</sub>	DATA	$\Sigma$ EVEN (CD74: $\Sigma$ )	MAX	50	21	20	12	10	52	60	63	20	21.6
				45	18	20	11	11	52	60	63	20	21.6
I <sub>PHL</sub>	DATA	$\Sigma$ ODD (CD74: $\Sigma$ O)	MAX	35	21	20	12	10	52	60	68	21	21.6
				50	18	22	11.5	11	52	60	68	21	21.6

UNIT: ns

## 4-BIT BINARY FULL ADDERS WITH FAST CARRY

- Full-Carry Look-Ahead Across the Four Bits

Logic Diagram (SN74)



FUNCTION TABLE (SN74)

INPUTS				OUTPUTS							
				WHEN C0 = L		WHEN C0 = H		WHEN C2 = L		WHEN C2 = H	
A1	B1	A2	B2	$\Sigma_1$	$\Sigma_2$	C2	$\Sigma_1$	$\Sigma_2$	C2		
A3	B3	A4	B4	$\Sigma_3$	$\Sigma_4$	C4	$\Sigma_3$	$\Sigma_4$	C4		
L	L	L	L	L	L	H	H	L	L		
H	L	L	L	H	L	L	H	H	L		
L	H	L	L	H	L	L	H	H	L		
H	H	L	L	H	L	H	H	H	L		
L	L	H	L	H	H	L	L	L	H		
H	L	H	L	H	H	L	L	L	H		
L	H	H	L	H	H	L	H	L	H		
H	H	H	L	L	L	H	H	L	H		
L	L	H	H	L	H	L	H	H	L		
H	L	L	H	H	H	L	L	L	H		
L	H	L	H	H	H	L	L	L	H		
H	H	L	H	H	L	H	H	L	H		
L	L	H	H	H	L	H	H	L	H		
H	L	H	H	H	L	H	H	L	H		
L	H	H	H	H	L	H	H	L	H		
H	H	H	H	H	H	H	H	H	H		

## ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER		MAX or MIN	TTL	LS	S	F	CD74 HC	CD74 HCT	CD74 AC	CD74 ACT	UNIT
I <sub>CC</sub>		MAX	110	39	160	55	0.16	0.16	0.16	0.16	mA
I <sub>OH</sub>	Any OUTPUT except C4	MAX	-0.8	-0.4	-1	-0.5	-1	-4	-4	-24	-24 mA
	C4	MAX	-0.4		-0.5						
I <sub>OL</sub>	Any OUTPUT except C4	MAX	16	8	20	10	20	4	4	24	24 mA
	C4	MAX	8		10		10	8	59	72	17.6

## SWITCHING CHARACTERISTICS

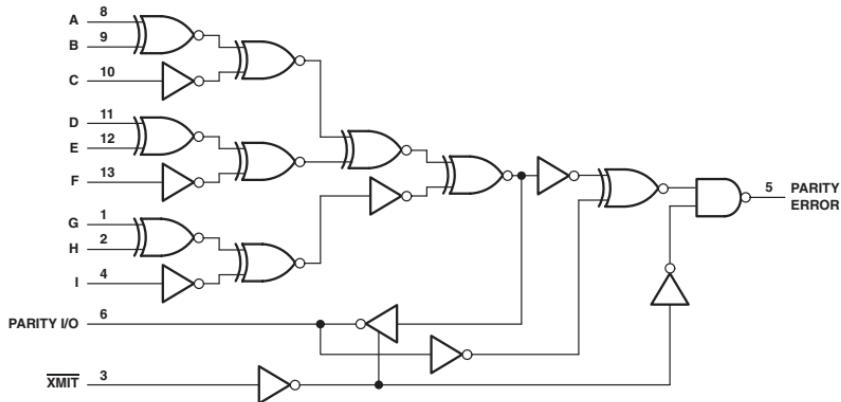
PARAMETER	INPUT	OUTPUT	MAX or MIN	TTL	LS	S	F	CD74 HC	CD74 HCT	CD74 AC	CD74 ACT	
I <sub>PLH</sub>	C0 (CD74:C <sub>n</sub> )	Any $\Sigma$ (CD74:S <sub>j</sub> )	MAX	21	24	18	10.5	69	80	17.6	17.6	
			MAX	21	24	18	10.5	69	80	17.6	17.6	
I <sub>PLH</sub>	An or Bn	$\Sigma n$ (CD74:S <sub>n</sub> )	MAX	24	24	18	10.5	63	74	18.2	18.2	
			MAX	24	24	18	10.5	63	74	18.2	18.2	
I <sub>PLH</sub>	C0 (CD74:C <sub>n</sub> )	C4 (CD74:C <sub>out</sub> )	MAX	14	17	11	8.5	59	69	17.6	17.6	
			MAX	16	22	11	8	59	69	17.6	17.6	
I <sub>PLH</sub>	An or Bn		MAX	14	17	12	8.5	59	72	17.6	17.6	
			MAX	16	17	12	8	59	72	17.6	17.6	

UNIT: ns

## 9-BIT ODD/EVEN PARITY GENERATORS/CHECKERS WITH BUS DRIVER PARITY I/O PORT

- Generate Either Odd or Even Parity for Nine Data Lines
- Cascadable for n-Bit Parity
- Direct Bus Connection for Parity Generation or Checking by Using the Parity I/O Port
- 74AC11xxx: Product Available in Reduced-Noise Advanced CMOS (11000 Series)
- 74ACT11xxx: Product Available in Reduced-Noise Advanced CMOS (11000 Series)

Logic Diagram (SN74AS)



FUNCTION TABLE (SN74AS)

NUMBER OF INPUTS (A-I) THAT ARE HIGH	XMIT	PARITY I/O	PARITY ERROR
0, 2, 4, 6, 8	I	H	H
1, 3, 5, 7, 9	I	L	H
0, 2, 4, 6, 8	h h	h l	H L
1, 3, 5, 7, 9	h h	h l	L H

h = high input level

I = low input level

H = high output level

L = low output level

## ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER		MAX or MIN	AS	AC 11	ACT 11	UNIT
I <sub>CC</sub>		MAX	50	0.08	0.08	mA
I <sub>OH</sub>	Parity error	MAX	-2	-24	-24	mA
	Parity I/O	MAX	-15	-24	-24	mA
I <sub>OL</sub>	Parity error	MAX	20	24	24	mA
	Parity I/O	MAX	48	24	24	mA

## SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	AS	AC 11	ACT 11
I <sub>PZH</sub>	A to I	Parity I/O	MAX	15	9	10.4
I <sub>PHL</sub>				14	107	12
I <sub>PZH</sub>	A to I	Parity error	MAX	16.5	10	11.3
I <sub>PHL</sub>				16.5	12	12.9
I <sub>PZH</sub>	Parity I/O	Parity error	MAX	9	6.2	7.7
I <sub>PHL</sub>				9	7.9	9.1
I <sub>PZH</sub>	XMIT	Parity I/O	MAX	13	5.3	7.3
I <sub>PHL</sub>				16	8.9	11.4
I <sub>PZH</sub>				11.5	6.5	8.5
I <sub>PHL</sub>				10	6.3	7.8

UNIT: ns

## PROGRAMMABLE FREQUENCY DIVIDERS/DIGITAL TIMERS

- Digitally Programmable from  $2^2$  to  $2^{31}$

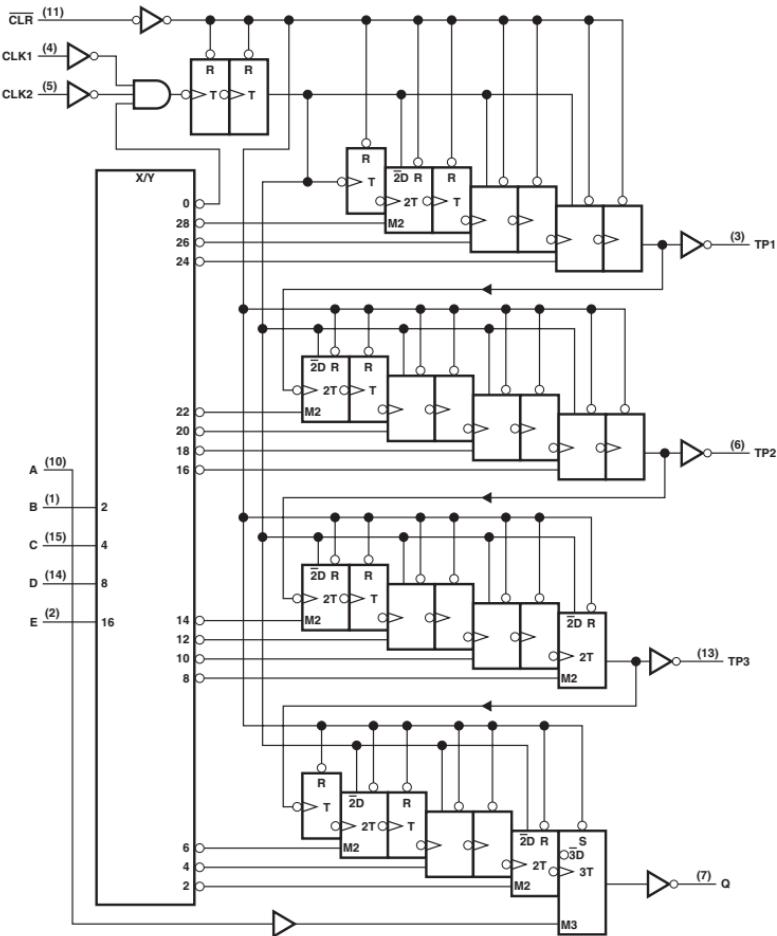
- Easily Expandable

- Applications:

  - Frequency Division

  - Digital Timing

Logic Diagram



**FUNCTION TABLE**

CLEAR	CLK 1	CLK 2	Q OUTPUT MODE
L	X	X	Cleared to L
H	≠	L	Count
H	L	≠	Count
H	H	X	Inhibit
H	X	H	Inhibit

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	LS	UNIT
I <sub>CC</sub>	MAX	75	mA
I <sub>OH</sub> (Q only)	MAX	-1.2	V
I <sub>OL</sub> (Q only)	MAX	24	mA

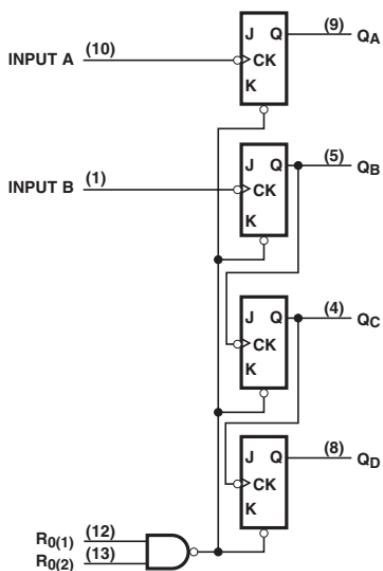
TIMING REQUIREMENTS AND SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	LS
f <sub>max</sub>	CLK		MIN	30
t <sub>PLH</sub>	CLK	Q	MAX	90
t <sub>PHL</sub>	CLK	Q	MAX	120
t <sub>PHI</sub>	CLR	Q̄	MAX	65

UNIT f<sub>max</sub> : MHz, other : ns

## 4-BIT BINARY COUNTERS

Logic Diagram



**COUNT SEQUENCE**

COUNT	OUTPUTS			
	QD	QC	QB	QA
0	L	L	L	L
1	L	L	H	L
2	L	L	L	H
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	L	H	H	L
7	L	H	H	H
8	H	L	L	L
9	H	L	H	H
10	H	L	H	L
11	H	L	H	H
12	H	H	L	L
13	H	H	L	H
14	H	H	H	L
15	H	H	H	H

NOTE: Output QA is connected to input B.

**RESET/COUNT FUNCTION TABLE**

RESET INPUTS		OUTPUTS			
R0(1)	R0(2)	QD	QC	QB	QA
H	H	L	L	L	L
L	X	COUNT		COUNT	
X	L				

**ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS**

PARAMETER	MAX or MIN	TTL	LS	UNIT
Icc	MAX	39	15	mA
IoH	MAX	-0.8	-0.4	mA
Iol	MAX	16	8	mA

**TIMING REQUIREMENTS AND SWITCHING CHARACTERISTICS**

PARAMETER	INPUT	OUTPUT	MAX or MIN	TTL	LS
fmax	A	QA	MIN	32	32
	B	QB	MIN	16	16
tw	A, B		MIN	15	15
				30	30
				15	15
tsu			MIN	25	25
tpLH	A	QA	MAX	16	16
tpHL				18	18
tpLH	A	QB	MAX	70	70
tpHL				70	70
tpLH	B	QB	MAX	16	16
tpHL				21	21
tpLH	B	QC	MAX	32	32
tpHL				35	35
tpLH	B	QD	MAX	51	51
tpHL				51	51

UNIT fmax : MHz, other : ns

## PROGRAMMABLE FREQUENCY DIVIDERS/DIGITAL TIMERS

- Digitally Programmable from  $2^2$  to  $2^{15}$

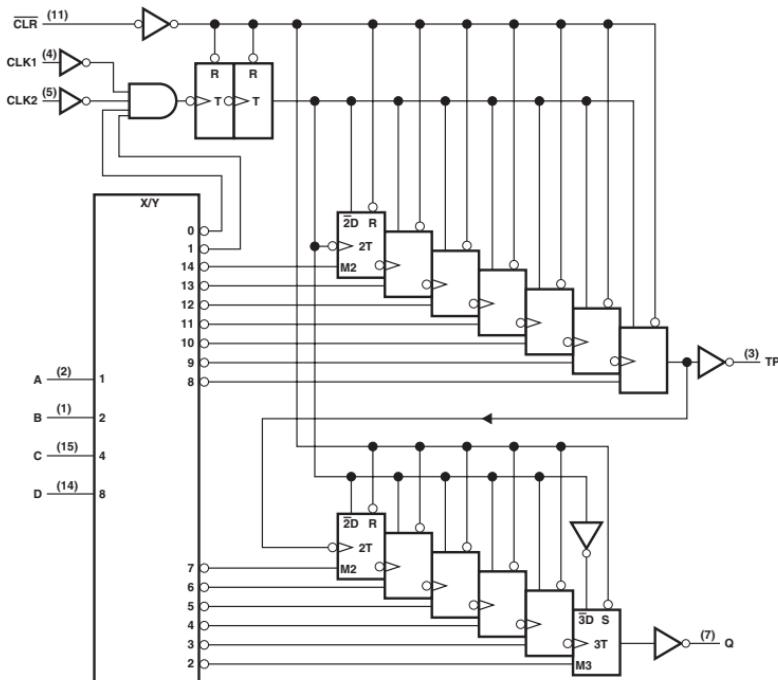
- Easily Expandable

- Applications

  - Frequency Division

  - Digital Timing

Logic Diagram



FUNCTION TABLE

PROGRAMMING INPUTS				FREQUENCY DIVISION			
				Q		TP	
D	C	B	A	BINARY	DECIMAL	BINARY	DECIMAL
L	L	L	L	Inhibit	Inhibit	Inhibit	Inhibit
L	L	L	H	Inhibit	Inhibit	$2^9$	512
L	L	H	L	$2^2$	4	$2^9$	512
L	L	H	H	$2^3$	8	$2^9$	512
L	H	L	L	$2^4$	16	$2^9$	512
L	H	L	H	$2^5$	32	$2^9$	512
L	H	H	L	$2^6$	64	$2^9$	512
L	H	H	H	$2^7$	128	Disabled Low	
H	L	L	L	$2^8$	256	$2^2$	4
H	L	L	H	$2^9$	512	$2^3$	8
H	L	H	L	$2^{10}$	1024	$2^4$	16
H	L	H	H	$2^{11}$	2048	$2^5$	32
H	H	L	L	$2^{12}$	4096	$2^6$	64
H	H	L	H	$2^{13}$	8192	$2^7$	128
H	H	H	L	$2^{14}$	16384	$2^8$	256
H	H	H	H	$2^{15}$	32768	$2^9$	512

## ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	LS	UNIT
I <sub>CC</sub>	MAX	50	mA
I <sub>OH</sub>	MAX	-1.2	V
I <sub>OL</sub>	MAX	24	mA

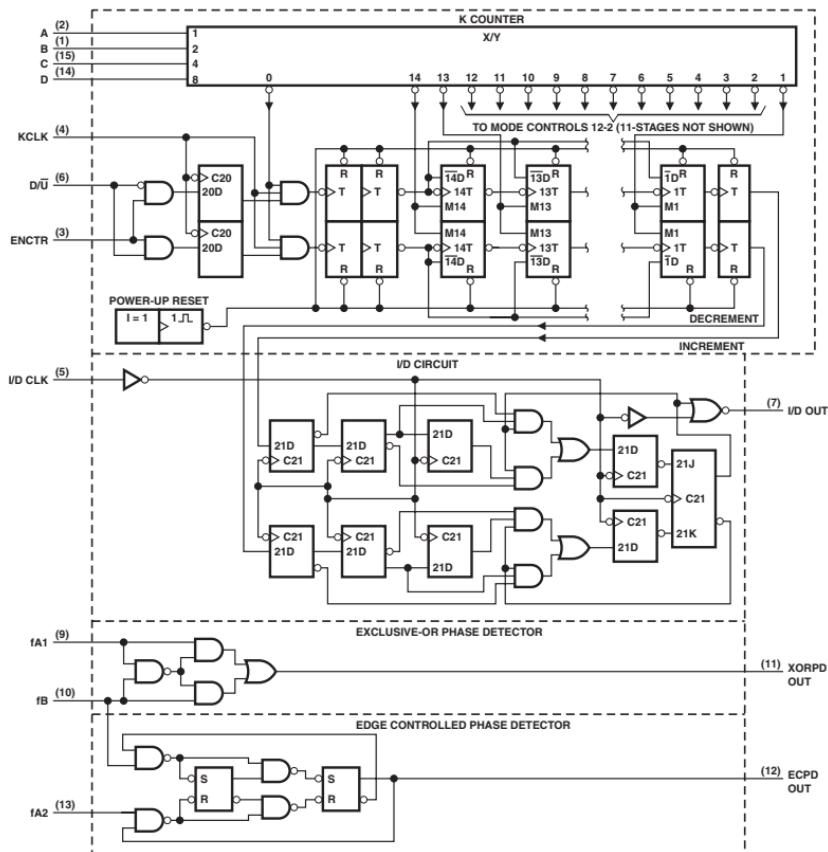
## TIMING REQUIREMENTS AND SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	LS
f <sub>max</sub>	CLK		MIN	30
	CLK 1 or 2		MIN	16
t <sub>w</sub>	CLR		MIN	35
			MAX	90
t <sub>PLH</sub>	CLK 1 or 2	Q	MAX	120
t <sub>PHL</sub>	CLR	Q̄	MAX	65

UNIT f<sub>max</sub>: MHz, other: ns

## DIGITAL PHASE-LOCKED-LOOP FILTERS

Logic Diagram (SN74LS)



## FUNCTION TABLES (SN74LS)

**K COUNTER FUNCTION TABLE  
(DIGITAL CONTROL)**

D	C	B	A	MODULO (K)
L	L	L	L	Inhibited
L	L	L	H	2 <sup>2</sup>
L	L	H	L	2 <sup>4</sup>
L	L	H	H	2 <sup>5</sup>
L	H	L	L	2 <sup>6</sup>
L	H	L	H	2 <sup>7</sup>
L	H	H	L	2 <sup>8</sup>
L	H	H	H	2 <sup>9</sup>
H	L	L	L	2 <sup>10</sup>
H	L	L	H	2 <sup>11</sup>
H	L	H	L	2 <sup>12</sup>
H	L	H	H	2 <sup>13</sup>
H	H	L	L	2 <sup>14</sup>
H	H	L	H	2 <sup>15</sup>
H	H	H	L	2 <sup>16</sup>
H	H	H	H	2 <sup>17</sup>

**EXCLUSIVE OR PHASE DETECTOR**

φA1	φB	XORPD OUT
L	L	L
L	H	H
H	L	H
H	H	L

**EDGE-CONTROLLED PHASE DETECTOR**

φA2	φB	ECPD OUT
H or L	↓	H
↓	H or L	L
H or L	↑	No change
↑	H or L	No change

**ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS**

PARAMETER		MAX or MIN	LS	CD74 HC	CD74 HCT	CD74 ACT	UNIT
ICC		MAX	120	0.16	0.16	0.08	mA
Ioh	I/D OUT	MAX	-1	-	-	-	
	XOR, ECPD	MAX	-0.4	-6	-4	-24	mA
Iol	I/D OUT	MAX	24	4	4	24	mA
	XOR, ECPD	MAX	8				

**TIMING REQUIREMENTS AND SWITCHING CHARACTERISTICS**

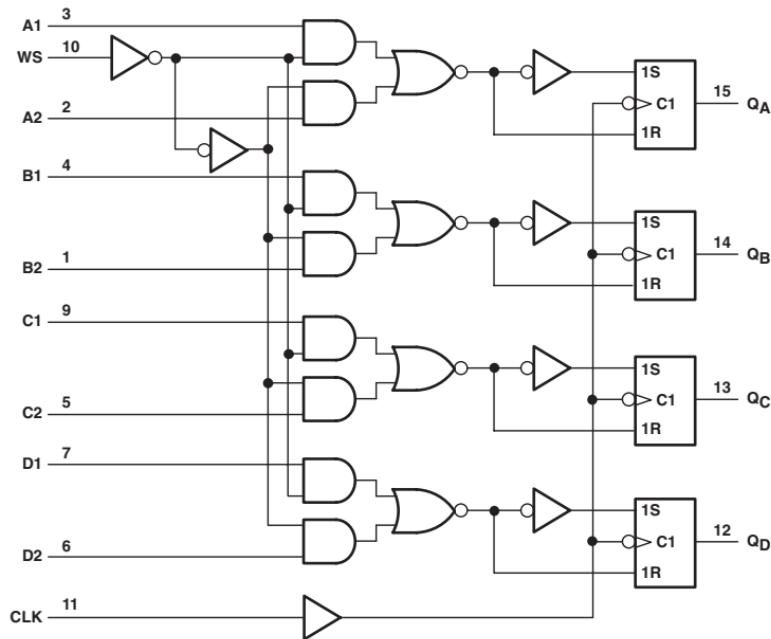
PARAMETER		INPUT		OUTPUT		MAX or MIN	LS	CD74 HC	CD74 HCT	CD74 ACT
fmax		K CLK (K <sub>CP</sub> )		I/D OUT		MIN	32	20	20	45
		I/D CLK (I/D <sub>CP</sub> )		I/D OUT			16	13	13	35
tw	K CLK (K <sub>CP</sub> )					MIN	16	24	24	8
	I/D CLK (I/D <sub>CP</sub> )						33	38	38	9
tsu	Ø/U					MIN	30	30	30	17
	ENCLR (ENCTR)						31	30	30	16
th	Ø/U					MIN	0	0	0	7
	ENCLR (ENCTR)						0	0	0	6
tpLH		I/D CLK ↑		I/D OUT		MAX	25	53	53	24
							35	53	53	24
tpHL		φA1 or φB	other INPUT low	XORPD OUT		MAX	15	45	45	22
			other INPUT high				25	45	45	22
tpHI		φA1 or φB	other INPUT low	XORPD OUT		MAX	25	45	45	22
			other INPUT high				25	45	45	22
tpLH		φB ↓		ECPD OUT		MAX	30	60	60	30
		φA2 ↓		ECPD OUT			30	60	60	30

UNIT fmax : MHz, other : ns

## QUADRUPLE 2-INPUT MULTIPLEXERS WITH STORAGE

- Outputs Storage Register

Logic Diagram



FUNCTION TABLE

INPUTS		OUTPUTS			
WORD SELECT	CLOCK	QA	QB	QC	QD
L	↓	A1	B1	C1	D1
H	↓	A2	B2	C2	D2
X	H	QA <sub>0</sub>	QB <sub>0</sub>	QC <sub>0</sub>	QD <sub>0</sub>

† a1, a2, etc. = the level of steady-state input at A1, A2, etc.  
 QA<sub>0</sub>, QB<sub>0</sub>, etc. = the level of QA, QB, etc. entered  
 on the most recent O transition of CLK

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	TTL	LS	AS	SN74 HC	UNIT
I <sub>CC</sub>	MAX	65	21	36	0.08	mA
I <sub>OL</sub>	MAX	16	8	20	4	mA
I <sub>OH</sub>	MAX	-0.8	-0.4	-2	-4	mA

TIMING REQUIREMENTS AND SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	TTL	LS	AS	SN74 HC
t <sub>w</sub>			MIN	20	20	8	27
t <sub>su</sub>	Data		MIN	15	15	4.5	21
	Word Select		MIN	25	25	13	21
t <sub>h</sub>	Data		MIN	5	5	3.5	0
	Word Select		MIN	0	0	1	0
t <sub>PLH</sub>			MAX	27	27	9	31
t <sub>PHL</sub>	CLK	GA to GD		32	32	11	31

UNIT: ns

## 8-BIT UNIVERSAL SHIFT/STORAGE REGISTERS WITH 3-STATE OUTPUTS

- Multiplexed I/O Ports Provide Improved Bit Density

- Four Modes of Operation:

Hold (Store)

Shift Right

Shift Left

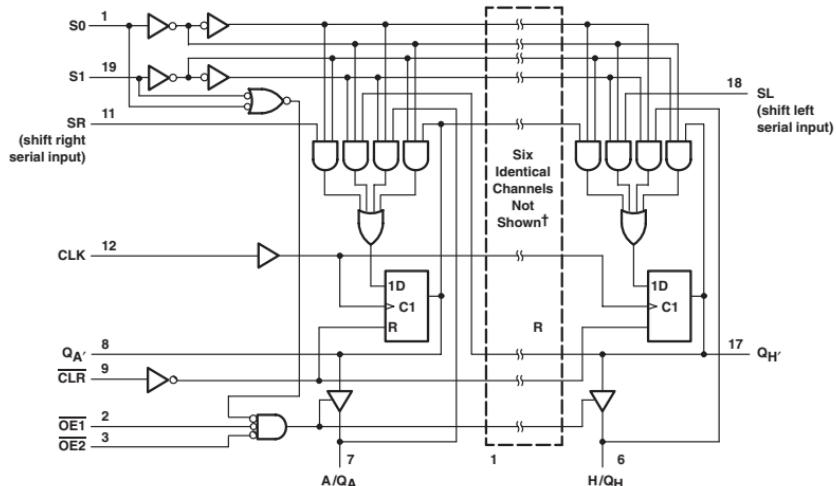
Load Data

- Operate with Outputs Enabled or at High Impedance

- 3-State Outputs Drive Bus Lines Directly

- Can Be Cascaded for n-Bit Word Lengths

Logic Diagram (SN74)



† I/O ports not shown: B/Q<sub>B</sub> (13), C/Q<sub>C</sub> (6), D/Q<sub>D</sub> (14), E/Q<sub>E</sub> (5), F/Q<sub>F</sub> (15), and G/Q<sub>G</sub> (4).

**FUNCTION TABLE (SN74)**

MODE	INPUTS						I/O PORTS								OUTPUTS				
	CLR	S1	S0	OE1†	OE2†	CLK	SL	SR	A/O A	B/Q B	C/O C	D/Q D	E/Q E	F/Q F	G/O G	H/Q H	Q A'	Q H'	
Clear	L	X	L	L	L	X	X	X	L	L	L	L	L	L	L	L	L	L	
	L	L	L	H	X	L	X	X	L	L	L	L	L	L	X	L	L	L	
Hold	H	L	X	L	L	L	X	X	X	Q A0	Q B0	Q C0	Q D0	Q E0	Q F0	Q G0	Q H0	Q A0	Q H0
	H	X	X	L	L	L	L	X	Q A0	Q B0	Q C0	Q D0	Q E0	Q F0	Q G0	Q H0	L	Q A0	Q H0
Shift Right	H	L	H	L	L	↑	X	H	H	Q An	Q Bn	Q Cn	Q Dn	Q En	Q Fn	Q Gn	H	Q Gn	Q Gn
	H	L	H	L	L	↑	X	L	H	Q An	Q Bn	Q Cn	Q Dn	Q En	Q Fn	Q Gn	L	Q Gn	Q Gn
Shift Left	H	H	L	L	L	↑	H	X	Q Bn	Q Cn	Q Dn	Q En	Q Fn	Q Gn	Q Hn	H	Q Bn	H	
	H	H	L	L	L	↑	L	X	Q Bn	Q Cn	Q Dn	Q En	Q Fn	Q Gn	Q Hn	L	Q Bn	L	
Load	H	H	H	X	X	↑	X	X	a	b	c	d	e	f	g	h	a	h	

NOTE: a...h=the level of the steady-state input at inputs A through H, respectively. This data is loaded into the flip-flops while the flip-flop outputs are isolated from the I/O terminals.

† When one or both output-enable inputs are high, the eight I/O terminals are disabled to the high-impedance state; however, sequential operation or clearing of the register is not affected.

**ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS**

PARAMETER		MAX or MIN	LS	S	ALS	F	CD74 HC	CD74 HCT	CD74 AC	CD74 ACT	UNIT
Icc		MAX	53	225	40	95	0.16	0.16	0.16	0.16	mA
Ioh	QA thru QH	MAX	-2.6	-6.5	-2.6	-3	-6	-4	-24	-24	mA
	QA' or QH'		-0.4	-0.5	-0.4	-1	-4	-4	-24	-24	mA
Iol	QA thru QH	MAX	24	20	24	24	6	4	24	24	mA
	QA' or QH'		8	6	8	20	4	4	24	24	mA

**TIMING REQUIREMENTS AND SWITCHING CHARACTERISTICS**

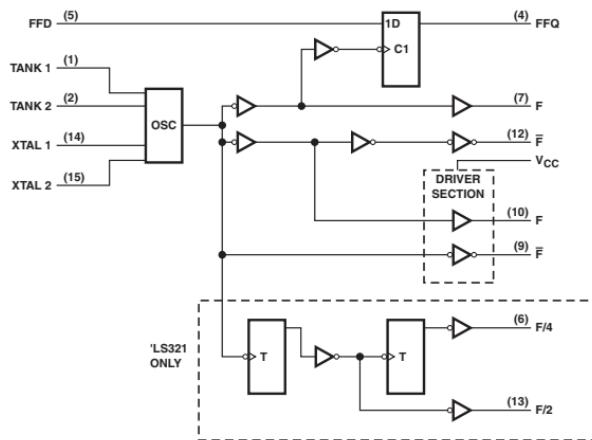
PARAMETER		INPUT	OUTPUT	MAX or MIN	LS	S	ALS	F	CD74 HC	CD74 HCT	CD74 AC	CD74 ACT	
fmax					MIN	20	50	30	70	20	16	95	90
tw	CLK (CP) high				MIN	30	10	16.5	7	24	30	5.2	5.5
	CLK (CP) low				MIN	10	10	16.5	7	24	30	5.2	5.5
	CLR (MR)				MIN	20	10	10	7	15	22	5	5
	DATA "H"				MIN	20	7	16	5.5	36	30	4.5	4.5
tsu	DATA "L"				MIN	20	5	6	5.5	36	30	4.5	4.5
	SELECT				MIN	35	15	20	8.5	36	41	9	9
	CLR (MR) INACTIVE				MIN	20	10	15	7	-	-	-	-
	DATA				MIN	0	5	0	2	0	0	0	0
th	SELECT				MIN	10	5	0	0	0	0	0	0
	IPHL				MAX	33	20	15	10	60	68	12.9	12.9
IPHL	CLK (CD74: CP)		QA or QH' (CD74: Q0 or Q7)		MAX	39	20	18	9.5	60	68	12.9	12.9
	CLK (CD74: CP)				MAX	25	21	13	10	60	68	13.5	14.5
IPHL	IPHL		QA or QH' (CD74: Q0 or Q7)		MAX	39	21	19	12	60	68	13.5	14.5
	CLR				MAX	40	21	22	10.5	60	69	11.2	12.2
IPHL	IPHL		QA thru QH (CD74: I0/0 thru I0/7)		MAX	40	24	22	15	60	69	13.9	18.6
	CLR				MAX	21	18	16	9	47	48	14.9	14.9
IPZL	IPZL		QA thru QH		MAX	30	18	22	11	39	45	14.9	14.9
	IPZL				MAX	20	12	8	7	56	56	14.9	14.9
IPZL	IPZL		QA thru QH		MAX	15	12	15	6.5	47	48	14.9	14.9

UNIT fmax : MHz, other : ns

## CRYSTAL-CONTROLLED OSCILLATORS

- Crystal-Controlled Oscillator Operation from 1MHz to 20MHz
- Complementary Outputs

Logic Diagram



## ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	LS	UNIT
I <sub>CC</sub>	MAX	75	mA
I <sub>OH</sub>	F' or $\bar{F}'$	MAX	-24 mA
	F, $\bar{F}$ , F/2, F/4	MAX	-0.4 mA
I <sub>OL</sub>	F' or $\bar{F}'$	MAX	24 mA
	F, $\bar{F}$ , F/2, F/4	MAX	8 mA

## TIMING REQUIREMENTS AND SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	LS
f <sub>max</sub>		F/2	MIN	10
		F/4	MAX	5
		ANY	MIN	20
t <sub>r</sub>		F', $\bar{F}'$	MAX	14
		ANY	MAX	40
t <sub>f</sub>		F', $\bar{F}'$	MAX	10
		ANY	MAX	20

UNIT f<sub>max</sub> : MHz, other : ns

## 8-BIT UNIVERSAL SHIFT/STORAGE REGISTERS WITH SYNCHRONOUS CLEAR AND 3-STATE OUTPUTS

- Multiplexed I/O Ports Provide Improved Bit Density

- Four Modes of Operation:

Hold (Store)

Shift Right

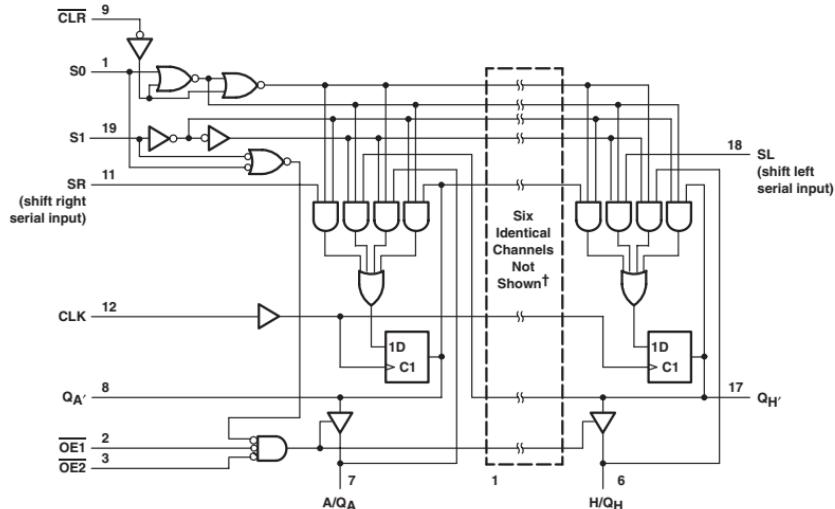
Shift Left

Load Data

- 3-State Outputs Drive Bus Lines Directly

- Can Be Cascaded for n-Bit Word Lengths

Logic Diagram (SN74ALS)



<sup>†</sup>I/O ports not shown: B/Q<sub>B</sub> (13), C/Q<sub>C</sub> (6), D/Q<sub>D</sub> (14), E/Q<sub>E</sub> (5), F/Q<sub>F</sub> (15), and G/Q<sub>G</sub> (4).

FUNCTION TABLE (SN74)

MODE	INPUTS								I/O BORD								OUTPUTS								Q <sub>A'</sub>		Q <sub>H'</sub>								
	CLR	SELECT	OUTPUT CONTROL		CLK	SEREAL		X	X	L	L	L	L	L	L	L	A/Q <sub>A</sub>	B/Q <sub>B</sub>	C/Q <sub>C</sub>	C/Q <sub>D</sub>	C/Q <sub>E</sub>	C/Q <sub>F</sub>	C/Q <sub>G</sub>	H/Q <sub>H</sub>	Q <sub>A'</sub>		Q <sub>H'</sub>								
			S1	S0		OE1†	OE2†	SL	SR	X	X	L	L	L	L	L	X	X	QAO	QAO	QCO	QDO	QE0	QFO	QGO	QHO	QAO	QHO	QAO	QHO					
Clear	L	X	L	L	L	X	L	L	↑	X	X	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L						
Hold	H	L	L	L	L	X	L	L	X	X	X	QAO	QAO	QCO	QDO	QE0	QFO	QGO	QHO	QAO	QHO	QAO	QHO	QAO	QHO	QAO	QHO	QAO	QHO						
Shift Right	H	X	X	L	L	L	L	L	↑	X	H	H	QAn	QBn	QCn	QDn	QEn	QFn	QGn	H	QGn	QAn	QBn	QCn	QDn	QE	QFn	QGn	QAn	QBn	QCn	QDn	QE	QFn	QGn
Shift Left	H	L	H	L	L	↑	X	L	X	L	X	QBn	QCh	QCn	QDn	QE	QFn	QGn	QHn	H	QGn	QBn	QCh	QCn	QDn	QE	QFn	QGn	QBn	QCh	QCn	QDn	QE	QFn	QGn
Load	H	H	H	X	X	↑	X	X	a	b	c	d	e	f	g	h	a	b	c	d	e	f	g	h	a	b	c	d	e	f	g	h			

† a ...h=the level of the steady-state input at inputs A through H, respectively. This data is loaded into the flip-flops while the flip-flop outputs are isolated from the I/O terminals.

## ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER		MAX or MIN	LS	ALS	CD74 AC	CD74 ACT	UNIT
I <sub>CC</sub>		MAX	225	40	0.16	0.16	mA
I <sub>OH</sub>	Q <sub>A'</sub> or Q <sub>H'</sub>	MAX	-0.5	-0.4	-24	-24	mA
	Q <sub>A</sub> thru Q <sub>H</sub>		-6.5	-2.6	-24	-24	mA
I <sub>OL</sub>	Q <sub>A'</sub> or Q <sub>H'</sub>	MAX	6	8	24	24	mA
	Q <sub>A</sub> thru Q <sub>H</sub>		20	24	24	24	mA

## TIMING REQUIREMENTS AND SWITCHING CHARACTERISTICS

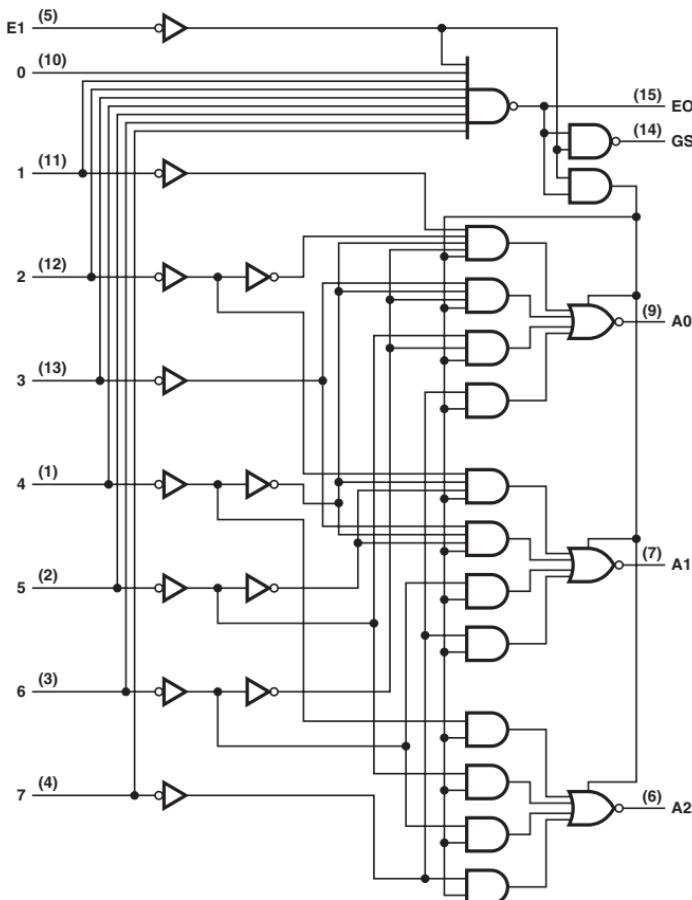
PARAMETER		INPUT	OUTPUT	MAX or MIN	LS	ALS	CD74 AC	CD74 ACT
fmax				MIN	25	17	95	90
t <sub>WV</sub>	CLK		Q <sub>A'</sub> or Q <sub>B'</sub>	MAX	30	16.5	5.2	5.5
	CLR				20	-	5	5
t <sub>su</sub>	DATA H			MIN	20	16	4.5	4.5
	DATA L				20	6	4.5	4.5
t <sub>h</sub>	SELECT			MIN	-	20	9	9
	CLR				-	20	5.5	5.5
t <sub>PLH</sub>	SELECT			MIN	-	0	0	0
	DATA				0	0	0	0
t <sub>PLH</sub>		CLK	Q <sub>A'</sub> or Q <sub>B'</sub>	MAX	33	15	12.9	12.9
t <sub>PHL</sub>		CLK	Q <sub>A</sub> thru Q <sub>H</sub>	MAX	39	18	12.9	12.9
t <sub>PLH</sub>		CLK	Q <sub>A</sub> thru Q <sub>H</sub>	MAX	25	13	13.5	14.5
t <sub>PHL</sub>					39	19	13.5	14.5
t <sub>PZH</sub>		OE1†	Q <sub>A</sub> thru Q <sub>H</sub>	MAX	21	16	14.9	14.9
t <sub>PZL</sub>		OE1†	Q <sub>A</sub> thru Q <sub>H</sub>	MAX	30	22	14.9	14.9
t <sub>PZH</sub>		OE1†	Q <sub>A</sub> thru Q <sub>H</sub>	MAX	20	8	14.9	14.9
t <sub>PZL</sub>		OE2†	Q <sub>A</sub> thru Q <sub>H</sub>	MAX	15	15	14.9	14.9
t <sub>PZH</sub>		OE2†	Q <sub>A</sub> thru Q <sub>H</sub>	MAX	21	16	14.9	14.9
t <sub>PZL</sub>		OE2†	Q <sub>A</sub> thru Q <sub>H</sub>	MAX	30	22	14.9	14.9
t <sub>PZH</sub>		OE2†	Q <sub>A</sub> thru Q <sub>H</sub>	MAX	20	8	14.9	14.9
t <sub>PZL</sub>		OE2†	Q <sub>A</sub> thru Q <sub>H</sub>	MAX	15	15	14.9	14.9

UNIT fmax : MHz, other : ns

## 8-LINE TO 3-LINE PRIORITY ENCODERS WITH 3-STATE OUTPUTS

- 3-State Outputs Drive Bus Lines Directly
- Encodes 8 Data Lines to 3-Line Binary (Octal)

Logic Diagram



FUNCTION TABLE

E1	INPUTS							OUTPUTS					
	0	1	2	3	4	5	6	7	A2	A1	A0	GS	E0
H	X	X	X	X	X	X	X	X	Z	Z	Z	H	H
H	H	H	H	H	H	H	H	H	Z	Z	Z	H	L
L	X	X	X	X	X	X	X	L	L	L	L	L	H
L	X	X	X	X	X	X	L	H	L	L	H	L	H
L	X	X	X	X	X	L	H	H	L	H	L	L	H
L	X	X	X	X	L	H	H	H	L	H	H	L	H
L	X	X	X	X	L	H	H	H	H	L	H	L	H
L	X	X	X	L	H	H	H	H	H	L	L	L	H
L	X	X	X	L	H	H	H	H	H	L	L	L	H
L	X	X	L	H	H	H	H	H	H	L	H	L	H
L	X	X	L	H	H	H	H	H	H	L	H	L	H
L	X	L	H	H	H	H	H	H	H	H	L	L	H
L	L	H	H	H	H	H	H	H	H	H	L	H	H

## ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER		MAX or MIN	LS	UNIT
Icc		MAX	25	mA
IoH	A0, A1, A2	MAX	-2.6	mA
	E0, ES	MAX	-0.4	mA
Iol		MAX	24	mA
		MAX	8	mA

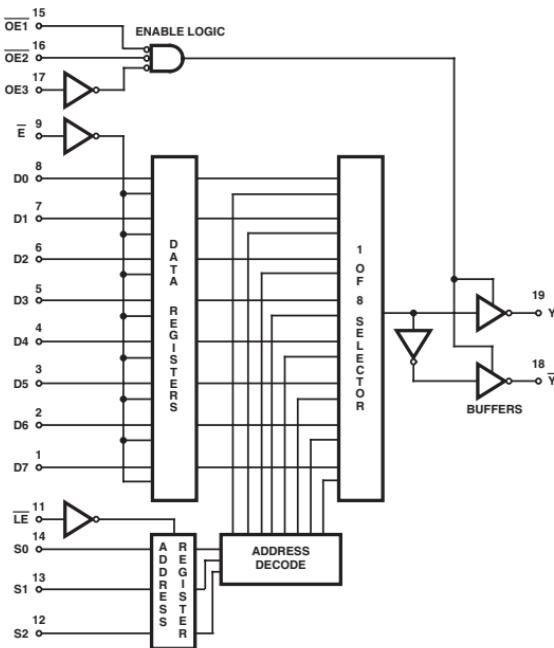
## SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	LS
tPLH	1 to 7	A0, A1, A2	MAX	35
			MAX	35
tPHL	0 to 7	E0	MAX	18
			MAX	40
tPLH	0 to 7	GS	MAX	55
			MAX	21

UNIT: ns

**8-LINE TO 1-LINE DATA SELECTORS/MULTIPLEXERS/TRANSPARENT/REGISTERS  
WITH 3-STATE OUTPUTS**

**Logic Diagram  
(CD74)**



FUNCTION TABLE (SN74)

INPUTS			OUTPUT ENABLES		OUTPUTS			
S2	S1	S0	DC	G1	G2	G3	W	Y
X	X	X	X	X	X	X	Z	Z
X	X	X	X	X	X	X	Z	Z
X	X	X	X	X	X	X	Z	Z
L	L	L	L	L	L	H	D0	D0
L	L	L	H	L	L	H	D0n	D0n
L	L	H	L	L	L	H	D1	D1
L	L	H	H	L	L	H	D1n	D1n
L	H	L	L	L	L	H	D2	D2
L	H	L	H	L	L	H	D2n	D2n
L	H	H	L	L	L	H	D3	D3
L	H	H	H	L	L	H	D3n	D3n
H	L	L	L	L	L	H	D4	D4
H	L	L	H	L	L	H	D4n	D4n
H	L	H	L	L	L	H	D5	D5
H	L	H	H	L	L	H	D5n	D5n
H	H	L	L	L	L	H	D6	D6
H	H	L	H	L	L	H	D6n	D6n
H	H	H	L	L	H	H	D7	D7
H	H	H	H	L	H	H	D7n	D7n

## NOTES:

H = High Voltage Level (Steady State); L = Low Voltage Level (Steady State); X = Don't Care; Z = High Impedance State (Off State); D0n ... D7n = the level of steady-state inputs D0 through D7, respectively, before the most recent low-to-high transition of data control.

† This column shows the input address setup with  $\overline{LE}$  low.

TRUTH TABLE (CD74)

INPUTS			SELECT (NOTE 3)			ENABLE DATA			OUTPUT ENABLES			OUTPUTS	
S2	S1	S0	E	OE1	OE2	OE3	Y	Y					
X	X	X	X	X	X	X	Z	Z					
X	X	X	X	X	X	X	Z	Z					
X	X	X	X	X	X	X	Z	Z					
L	L	L	L	L	L	L	L	L					
L	L	L	H	L	L	H	D0	D0					
L	L	H	L	L	L	H	D0n	D0n					
L	L	H	L	L	L	H	D1	D1					
L	H	L	L	L	L	H	D1n	D1n					
L	H	L	H	L	L	H	D2	D2					
L	H	L	H	L	L	H	D2n	D2n					
L	H	H	L	L	L	H	D3	D3					
L	H	H	H	L	L	H	D3n	D3n					
L	H	H	L	L	L	H	D4	D4					
L	H	H	H	L	L	H	D4n	D4n					
H	L	L	L	L	L	H	D5	D5					
H	L	H	L	L	L	H	D5n	D5n					
H	H	L	L	L	L	H	D6	D6					
H	H	L	H	L	L	H	D6n	D6n					
H	H	H	L	L	H	H	D7	D7					
H	H	H	H	L	H	H	D7n	D7n					

H = High Voltage Level (Steady State); L = Low Voltage Level (Steady State); X = Don't Care; Z = High Impedance State (Off State); D0n ... D7n = the level of steady-state inputs D0 through D7, respectively, before the most recent low-to-high transition of data control.

## NOTE:

1. This column shows the input address setup with  $\overline{LE}$  low.

## ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	LS	SN74 HC	CD74 HC	CD74 HCT	UNIT
I <sub>CC</sub>	MAX	46	0.08	0.16	0.16	mA
I <sub>OH</sub>	MAX	-2.6	-6	-6	-4	mA
I <sub>OL</sub>	MAX	24	6	6	4	mA

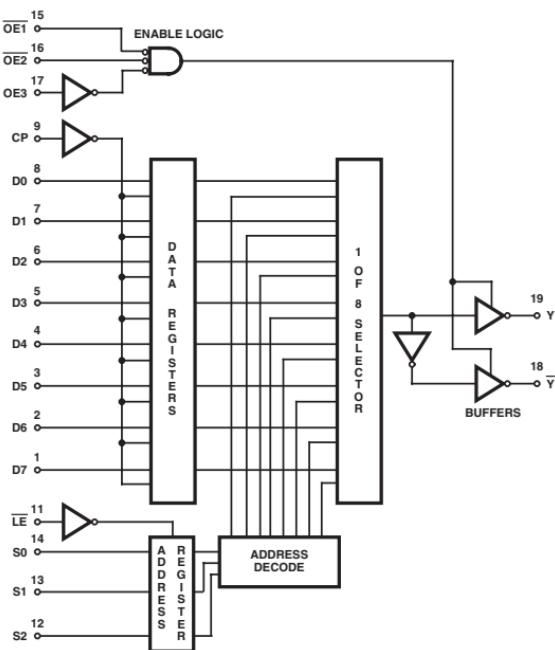
## TIMING REQUIREMENTS AND SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	LS	SN74 HC	CD74 HC	CD74 HCT
$t_{au}$			MAX	15	19	15	15
				15	5	14	14
$t_{th}$	D0 thru D7	Y	MAX	36	59	63	71
				35	59	63	71
$t_{PLH}$	D0 thru D7	W (CD74: $\bar{Y}$ )	MAX	27	59	63	71
				44	59	63	71
$t_{PHL}$	$\overline{DC}$ (CD74: $\bar{E}$ )	Y	MAX	42	68	75	81
				39	68	75	81
$t_{PLH}$	$\overline{DC}$ (CD74: $\bar{E}$ )	W (CD74: $\bar{Y}$ )	MAX	33	68	75	81
				50	68	75	81

UNIT: ns

## 8-INPUT MULTIPLEXER/REGISTER, 3-STATE

**Logic Diagram  
(CD74)**



FUNCTION TABLE (SN74)

INPUTS			OUTPUTS				
SELECT†	CLK	OUTPUT ENABLES	G1	G2	G3	W	Y
X	X	X	H	X	X	Z	Z
X	X	X	X	H	X	Z	Z
X	X	X	X	X	L	Z	Z
L	L	L	↑	L	L	H	D0 D0
L	L	L	H or L	L	L	H	D0n D0n
L	L	H	↑	L	L	H	D1 D1
L	L	H	H or L	L	L	H	D1n D1n
L	H	L	↑	L	L	H	D2 D2
L	H	L	H or L	L	L	H	D2n D2n
L	H	H	↑	L	L	H	D3 D3
L	H	H	H or L	L	L	H	D3n D3n
H	L	L	↑	L	L	H	D4 D4
H	L	H	H or L	L	L	H	D4n D4n
H	L	H	↑	L	L	H	D5 D5
H	L	H	H or L	L	L	H	D5n D5n
H	H	L	↑	L	L	H	D6 D6
H	H	L	H or L	L	L	H	D6n D6n
H	H	H	↑	L	L	H	D7 D7
H	H	H	H or L	L	L	H	D7n D7n

## NOTES:

H = High Voltage Level (Steady State); L = Low Voltage Level (Steady State); ↑ = Transition from Low to High Level; X = Don't Care; Z = High-Impedance State (Off State); D0n ... D7n = the level of steady-state inputs D0 through D7, respectively, before the most recent low-to-high transition of data control.

† This column shows the input address setup with LE low.

TRUTH TABLE (CD74)

INPUTS				OUTPUTS		
SELECT (NOTE 3)			CLOCK	OUTPUT ENABLES		
S2	S1	S0	CP	OE1	OE2	OE3
X	X	X	X	H	X	X
X	X	X	X	X	H	X
X	X	X	X	X	X	L
L	L	L	↑	L	L	H
L	L	H or L	L	L	H	D0
L	L	H	↑	L	H	D1
L	L	H	H or L	L	H	D1n
L	H	L	↑	L	H	D2
L	H	L	H or L	L	H	D2n
L	H	H	↑	L	H	D3
L	H	H	H or L	L	H	D3n
H	L	L	↑	L	H	D4
H	L	H	H or L	L	H	D4n
H	L	H	↑	L	H	D5
H	L	H	H or L	L	H	D5n
H	H	L	↑	L	H	D6
H	H	L	H or L	L	H	D6n
H	H	H	↑	L	H	D7
H	H	H	H or L	L	H	D7n
H	H	H	↑	L	H	D8
H	H	H	H or L	L	H	D8n
H	H	H	↑	L	H	D9
H	H	H	H or L	L	H	D9n
H	L	L	↑	L	H	D10
H	L	L	H or L	L	H	D10n
H	L	H	↑	L	H	D11
H	L	H	H or L	L	H	D11n
H	H	L	↑	L	H	D12
H	H	L	H or L	L	H	D12n
H	H	H	↑	L	H	D13
H	H	H	H or L	L	H	D13n
H	L	L	↑	L	H	D14
H	L	L	H or L	L	H	D14n
H	L	H	↑	L	H	D15
H	L	H	H or L	L	H	D15n
H	H	L	↑	L	H	D16
H	H	L	H or L	L	H	D16n
H	H	H	↑	L	H	D17
H	H	H	H or L	L	H	D17n

H = High Voltage Level (Steady State); L = Low Voltage Level (Steady State); ↑ = Transition from Low to High Level; X = Don't Care; Z = High-Impedance State (Off State); D0n ... D7n = the level of steady-state inputs D0 through D7, respectively, before the most recent low-to-high transition of data control.

## NOTE:

- This column shows the input address setup with LE low.

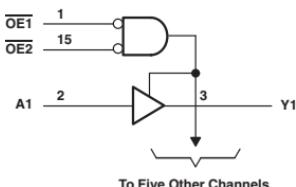
## ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	LS	SN74 HC	CD74 HCT	UNIT
I <sub>CC</sub>	MAX	46	0.08	0.16	mA
I <sub>OH</sub>	MAX	-2.6	-6	-4	mA
IOL	MAX	24	6	4	mA

## TIMING REQUIREMENTS AND SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	LS	SN74 HC	CD74 HCT
t <sub>su</sub>	D0 thru D7		MIN	15	19	11
t <sub>th</sub>	D0 thru D7		MIN	0	5	14
t <sub>PLH</sub>	CLK	Y	MAX	27	64	77
t <sub>PLH</sub>	CLK	W (CD74 : $\bar{Y}$ )	MAX	50	64	77
t <sub>PLH</sub>	S0, S1, S2	Y	MAX	36	64	77
t <sub>PLH</sub>	S0, S1, S2	W (CD74 : $\bar{Y}$ )	MAX	27	64	77
t <sub>PLH</sub>	S0, S1, S2	Y	MAX	45	71	89
t <sub>PLH</sub>	S0, S1, S2	W (CD74 : $\bar{Y}$ )	MAX	48	71	89
t <sub>PLH</sub>	S0, S1, S2	Y	MAX	54	71	89
t <sub>PLH</sub>	S0, S1, S2	W (CD74 : $\bar{Y}$ )	MAX	45	71	89

UNIT: ns

**HEX BUFFERS AND LINE DRIVERS  
WITH 3-STATE OUTPUTS**

**FUNCTION TABLE (SN74)**  
(each buffer/driver)

INPUTS			OUTPUT
$\overline{OE1}$	$\overline{OE2}$	A	Y
H	X	X	Z
X	H	X	Z
L	L	H	H
L	L	L	L

**ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS**

PARAMETER	MAX or MIN	TTL	LS	SN74 HC	CD74 HC	CD74 HCT	UNIT
$I_{CC}$	MAX	85	24	0.08	0.16	0.16	mA
$I_{OH}$	MAX	-5.2	-2.6	-6	-6	-4	mA
$I_{OL}$	MAX	32	24	6	6	4	mA

**SWITCHING CHARACTERISTICS**

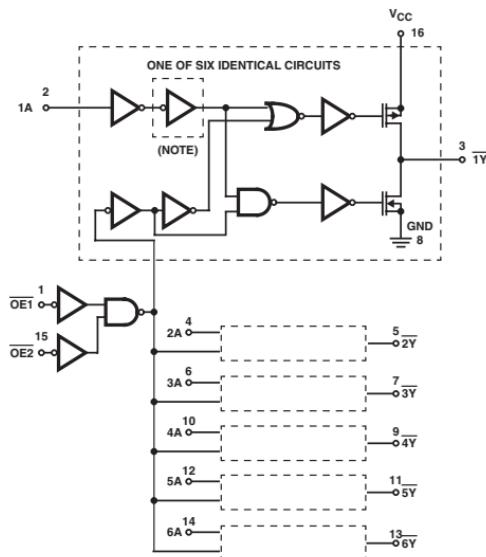
PARAMETER	INPUT	OUTPUT	MAX or MIN	TTL	LS	SN74 HC	CD74 HC	CD74 HCT
$t_{PLH}$	A	Y	MAX	16	15	24	32	38
			MAX	22	18	24	32	38
$t_{PHL}$	$\bar{G}$ (CD74: $\overline{OE}$ )	Y	MAX	35	35	48	45	53
			MAX	37	45	48	45	53
$t_{PZH}$	$\bar{G}$ (CD74: $\overline{OE}$ )	Y	MAX	11	32	48	45	53
			MAX	27	35	48	45	53

UNIT: ns

## HEX BUFFERS AND LINE DRIVERS WITH 3-STATE OUTPUTS

Logic Diagram

(CD74HC)



NOTE: Inverter not included in HC/HCT365.

FIGURE 1. LOGIC DIAGRAM FOR THE HC/HCT365 AND HC366 (OUTPUTS FOR HC/HCT365 ARE COMPLEMENTS OF THOSE SHOWN, i.e., 1Y, 2Y, ETC.)

## FUNCTION TABLE (CD74)

INPUTS		OUTPUT Y
OE1	OE2	A
L	L	L
L	L	H
X	H	X
H	X	X
		Z
		Z

## NOTES:

H = High Voltage Level

L = Low Voltage Level

X = Don't Care

Z = High Impedance (OFF) State

## ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

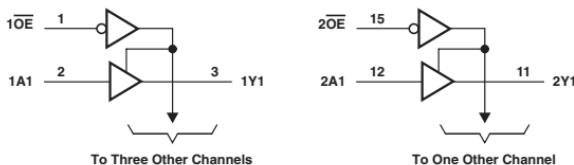
PARAMETER	MAX or MIN	TTL	LS	SN74 HC	CD74 HC	UNIT
I <sub>CC</sub>	MAX	77	21	0.08	160	mA
I <sub>OH</sub>	MAX	-5.2	-2.6	-6	-6	mA
I <sub>OL</sub>	MAX	32	24	6	6	mA

## SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	TTL	LS	SN74 HC	CD74 HC
$t_{PLH}$	A	$\bar{Y}$	MAX	17	15	24	33
		(CD74 : $\bar{Y}$ )	MAX	16	18	24	33
$t_{PHL}$		$\bar{Y}$	MAX	35	35	48	45
		(CD74 : $\bar{Y}$ )	MAX	37	45	48	45
$t_{PZH}$	$\bar{G}$ (CD74 : $\bar{OE}$ )	$\bar{Y}$	MAX	11	32	48	45
		(CD74 : $\bar{Y}$ )	MAX	27	35	48	45
UNIT:ns							

## HEX BUFFERS AND LINE DRIVERS WITH 3-STATE OUTPUTS

Logic Diagram (SN74)

FUNCTION TABLE (SN74)  
(each buffer/driver)

INPUTS		OUTPUT
OE	A	Y
L	H	H
L	L	L
H	X	Z

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	TTL	LS	SN74 HC	CD74 HC	CD74 HCT	AHC	AHCT	LV 3V	LV 5V	UNIT
I <sub>CC</sub>	MAX	85	24	0.08	0.16	0.16	0.04	0.04	-	0.02	mA
I <sub>OH</sub>	MAX	-5.2	-2.6	-6	-6	-4	-8	-8	-8	-16	mA
I <sub>OL</sub>	MAX	32	24	6	6	4	8	8	8	16	mA

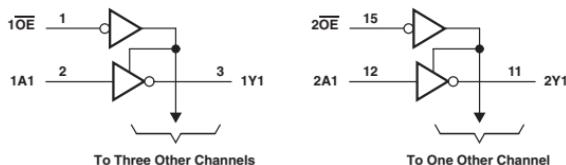
SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	TTL	LS	SN74 HC	CD74 HC	CD74 HCT	AHC	AHCT	LV 3V	LV 5V
t <sub>PLH</sub>	A	Y	MAX	16	16	24	32	38	9	6.5	13.5	9
t <sub>PHL</sub>			MAX	22	22	24	32	38	9	6.5	13.5	9
t <sub>PZH</sub>	$\overline{OE}$	Y	MAX	35	35	48	45	53	10.5	9.5	16	10.5
t <sub>PZL</sub>			MAX	47	40	48	45	53	10.5	8.5	16	10.5
t <sub>PHZ</sub>	$\overline{OE}$	Y	MAX	11	30	48	45	53	10.5	9.5	15.5	10.5
t <sub>PZL</sub>			MAX	27	35	48	45	53	10.5	8.5	15.5	10.5

UNIT: ns

## HEX INVERTING BUFFERS AND LINE DRIVERS WITH 3-STATE OUTPUTS

Logic Diagram (SN74)

FUNCTION TABLE (SN74)  
(each buffer/driver)

INPUTS	OUTPUT	
$\overline{OE}$	A	Y
H	X	Z
L	H	L
L	L	H

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	TTL	LS	SN74 HC	CD74 HC	CD74 HCT	UNIT
$I_{CC}$	MAX	77	21	0.08	0.16	0.16	mA
$I_{OH}$	MAX	-5.2	-2.6	-6	-6	-4	mA
$I_O$	MAX	32	24	6	6	4	mA

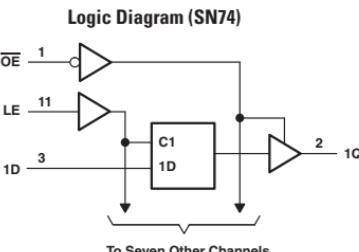
SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	TTL	LS	SN74 HC	CD74 HC	CD74 HCT
$t_{PLH}$	A	Y	MAX	17	15	24	32	45
			MAX	16	18	24	32	45
$t_{PHL}$	$\overline{OE}$	Y	MAX	35	35	48	45	53
			MAX	37	45	48	45	53
$t_{PZH}$	$\overline{OE}$	Y	MAX	11	32	48	45	53
			MAX	27	35	48	45	53

UNIT: ns

## OCTAL TRANSPARENT D-TYPE LATCHES WITH 3-STATE OUTPUTS

- 3-State Bus-Driving True Outputs
- Buffered Control Inputs
- 74AC11xxx: Product Available in Reduced-Noise Advanced CMOS (11000 Series)
- 74ACT11xxx: Product Available in Reduced-Noise Advanced CMOS (11000 Series)



**FUNCTION TABLE (SN74)**

OUTPUT CONTROL	INPUTS		OUTPUT Q
	LE	D	
L	H	H	H
L	H	L	L
L	L	X	Q0
H	X	X	Z

**ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS**

PARAMETER	MAX or MIN	LS	S	ALS	AS	F	SN74 HC	CD74 HC	SN74 HCT	CD74 HCT	SN74 BCT	ABT	LVTH 3V	UNIT
I <sub>CC</sub>	MAX	40	190	27	100	55	0.08	0.16	0.08	0.16	60	30	5	mA
I <sub>OH</sub>	MAX	-2.6	-6.5	-2.6	-15	-3	-6	-6	-6	-6	-15	-32	-32	mA
I <sub>OL</sub>	MAX	24	20	24	48	24	6	6	6	6	64	64	64	mA

PARAMETER	MAX or MIN	AC 11	SN74 AC	CD74 AC	ACT 11	SN74 ACT	CD74 ACT	AHC	AHCT	LV 3V	LV 5V	LV-AT	LVC 3V	ALVCH 3V	UNIT
I <sub>CC</sub>	MAX	0.08	0.04	0.16	0.08	0.04	0.16	0.04	0.04	-	0.02	0.02	0.01	0.02	mA
I <sub>OH</sub>	MAX	-24	-24	-24	-24	-24	-24	-8	-8	-8	-16	-16	-24	-24	mA
I <sub>OL</sub>	MAX	24	24	24	24	24	24	8	8	8	16	16	24	24	mA

## TIMING REQUIREMENTS AND SWITCHING CHARACTERISTICS

PARAMETER		INPUT	OUTPUT	MAX or MIN	LS	S	ALS	AS	F	SN74 HC	CD74 HC	SN74 HCT	CD74 HCT	SN74 BCT	ABT
tw	High			MIN	15	6	10	4.5	6	20	24	25	24	7.5	3.3
	Low			MIN	15	7.3	-	-	-	-	-	-	-	-	-
	tsu			MIN	5	0	10	2	2	13	15	13	20	2	1.9
	th			MIN	20	10	7	3	3	12	5	10	15	5.5	1
tpUH	D	Q		MAX	18	12	12	6	8	38	45	44	48	9.3	5.9
tpHL				MAX	18	12	16	6	6	38	45	44	48	9.5	6.2
tpUH	LE	Q		MAX	30	14	22	11.5	13	44	53	44	53	9.3	6.6
tpHL				MAX	30	18	23	7.5	8	44	53	44	53	8.8	7.2
tpZH	$\overline{OE}$	Q		MAX	28	15	18	6.5	12	38	45	44	53	11.8	5.2
tpZL				MAX	36	18	20	9.5	8.5	38	45	44	53	12	6.7
tpHZ	$\overline{OE}$	Q		MAX	25	9	10	6.5	7.5	38	45	44	53	7	6.9
tpLZ				MAX	20	12	12	7	6	38	45	44	53	7.4	6.5

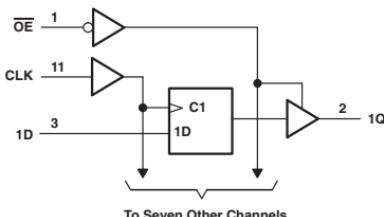
PARAMETER		INPUT	OUTPUT	MAX or MIN	LVTH 3V	AC 11	SN74 AC	CD74 AC	ACT 11	SN74 ACT	CD74 ACT	AHC	AHCT	LV 3V	LV 5V
tw	High			MIN	3	4	4.5	4	5	8	4	5	6.5	5	5
	Low			MIN	-	-	-	4	-	-	4	-	-	-	-
	tsu			MIN	1.1	3.5	4.5	2	3.5	8	2	4	1.5	4	4
	th			MIN	1.4	2	1	3	3.5	1	3	1	3.5	1	1
tpUH	D	Q		MAX	3.9	10.3	10.5	8.5	11.8	11.5	10.4	10.5	10.5	17	10.5
tpHL				MAX	3.9	8.4	10.5	8.5	10	11.5	10.4	10.5	10.5	17	10.5
tpUH	LE	Q		MAX	4.2	11.3	10.5	12	13	11.5	12.5	10.5	14.5	16.5	10.5
tpHL				MAX	4.2	10.2	10.5	12	12.2	11.5	12.5	10.5	14.5	16.5	10.5
tpZH	$\overline{OE}$	Q		MAX	4.8	10.8	9.5	10.5	12.5	10.5	13.5	11.5	13.5	17	11.5
tpZL				MAX	4.8	9.7	9.5	10.5	12	10.5	13.5	11.5	13.5	17	11.5
tpHZ	$\overline{OE}$	Q		MAX	4.6	11.1	12.5	11.5	12.2	12.5	12.5	10.5	12	15	10.5
tpLZ				MAX	4.5	8.7	10	11.5	10.1	10	12.5	10.5	12	15	10.5

PARAMETER		INPUT	OUTPUT	MAX or MIN	LV-AT	LVC 3V	ALVCH 3V
tw	High			MIN	8.5	3.3	3.3
	Low			MIN	-	-	-
	tsu			MIN	1.5	2	0.5
	th			MIN	3.5	1.5	1.2
tpUH	D	Q		MAX	11	6.8	3.6
tpHL				MAX	11	6.8	3.6
tpUH	LE	Q		MAX	15	7.6	3.3
tpHL				MAX	15	7.6	3.3
tpZH	$\overline{OE}$	Q		MAX	14	7.7	4.8
tpZL				MAX	14	7.7	4.8
tpHZ	$\overline{OE}$	Q		MAX	12.5	7	4.4
tpLZ				MAX	12.5	7	4.4

UNIT fmax : MHz, other : ns

**OCTAL EDGE-TRIGGERED D-TYPE FLIP-FLOPS  
WITH 3-STATE OUTPUTS**

- Buffered Control Inputs
- 74AC11xxx: Product Available in Reduced-Noise Advanced CMOS (11000 Series)
- 74ACT11xxx: Product Available in Reduced-Noise Advanced CMOS (11000 Series)

**Logic Diagram (SN74)****FUNCTION TABLE (SN74)**

OUTPUT CONTROL	INPUTS		OUTPUT Q
	CLK	D	
L	↑	H	H
L	↑	L	L
L	L	X	Q0
H	X	X	Z

**ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS**

PARAMETER	MAX or MIN	LS	S	ALS	AS	F	SN74 HC	CD74 HC	SN74 HCT	CD74 HCT	SN74 BCT	ABT	LVTH 3V	UNIT
I <sub>CC</sub>	MAX	40	160	31	128	86	0.08	0.16	0.08	0.16	60	30	5	mA
I <sub>OH</sub>	MAX	-2.6	-6.5	-2.6	-15	-3	-6	-6	-6	-6	-15	-32	-32	mA
I <sub>OL</sub>	MAX	24	20	24	48	24	6	6	6	6	64	64	64	mA

PARAMETER	MAX or MIN	AC 11	SN74 AC	CD74 AC	ACT 11	SN74 ACT	CD74 ACT	AHC	AHCT	LV 3V	LV 5V	LVC 3V	ALVCH 3V	UNIT
I <sub>CC</sub>	MAX	0.08	0.04	0.16	0.08	0.04	0.16	0.04	0.04	-	0.02	0.01	0.01	mA
I <sub>OH</sub>	MAX	-24	-24	-24	-24	-24	-24	-8	-8	-8	-16	-24	-24	mA
I <sub>OL</sub>	MAX	24	24	24	24	24	24	8	8	8	16	24	24	mA

## TIMING REQUIREMENTS AND SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	LS	S	ALS	AS	F	SN74 HC	CD74 HC	SN74 HCT	CD74 HCT	SN74 BCT	ABT	
fmax	t <sub>W</sub> High		MIN	35	75	35	125	70	24	20	25	20	70	150	
			MIN	15	6	14	4	7	20	24	20	24	7	3.3	
			MIN	15	7.3	14	3	6	20	24	20	24	-	3.3	
	t <sub>SU</sub> t <sub>H</sub>		MIN	20	5	10	2	2	25	18	25	18	6.5	1.9	
			MIN	0	2	0	2	2	5	5	10	5	0	2.1	
			MAX	28	15	12	8	10	45	50	45	50	10.6	6.2	
t <sub>PLH</sub>	CLK (CD74: CP)	Q	MAX	28	17	16	9	10	45	50	45	50	10	7.1	
t <sub>PHL</sub>			MAX	26	15	17	6	12.5	38	45	38	45	12.3	5.2	
t <sub>PZH</sub>			MAX	28	18	18	10	8.5	38	45	38	45	12.7	6.7	
t <sub>PZL</sub>			MAX	28	9	10	6	8	38	41	38	42	6.8	6.7	
t <sub>PHZ</sub>			MAX	28	9	10	6	8	38	41	38	42	6.8	6.7	
t <sub>PZL</sub>			MAX	20	12	18	6	6.5	38	41	38	42	6.8	6.5	

PARAMETER	INPUT	OUTPUT	MAX or MIN	LVT <sub>3V</sub>	AC 11	SN74 AC	CD74 AC	ACT 11	SN74 ACT	CD74 ACT	AHC	AHCT	LV 3V	LV 5V	
fmax	t <sub>W</sub> High		MIN	150	95	100	12.5	55	90	110	75	75	50	75	
			MIN	3.3	5	4.5	4	9	5	4.5	5	6.5	5.5	5	
			MIN	3.3	5	4.5	4	9	5	4.5	5	6.5	5.5	5	
	t <sub>SU</sub> t <sub>H</sub>		MIN	1.5	2.5	4.5	2	3	5.5	2	3	2.5	4.5	3	
			MIN	0.8	3.5	1.5	2	5.5	1.5	3	2	2.5	2	2	
			MAX	4.5	10.2	10.5	10.8	12.4	11.5	11.2	11.5	11.5	18.5	11.5	
t <sub>PLH</sub>	CLK (CD74: CP)	Q	MAX	4.2	10.1	10	10.8	13	11	11.2	11.5	11.5	18.5	11.5	
t <sub>PHL</sub>			MAX	4.7	9.1	9.5	14.5	12.3	10.5	14.5	11	12.5	16.5	11	
t <sub>PZH</sub>			MAX	4.7	9.4	9.5	14.5	12.3	10.5	14.5	11	12.5	16.5	11	
t <sub>PZL</sub>			MAX	4.6	11.2	12.5	14.5	13.2	12.5	14.5	10	12	16	10	
t <sub>PHZ</sub>			MAX	4.5	9.2	10	14.5	10.8	10	14.5	10	12	16	10	
t <sub>PZL</sub>			MAX	4.5	9.2	10	14.5	10.8	10	14.5	10	12	16	10	

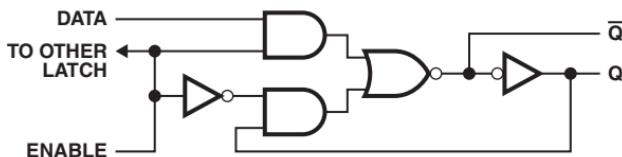
PARAMETER	INPUT	OUTPUT	MAX or MIN	LVC 3V	ALVCH 3V	
fmax	t <sub>W</sub> High		MIN	100	150	
			MIN	3.3	3.3	
			MIN	3.3	3.3	
	t <sub>SU</sub> t <sub>H</sub>		MIN	2	1.8	
			MIN	1.5	0.5	
			MAX	7	3.6	
t <sub>PLH</sub>	CLK	Q	MAX	7	3.6	
t <sub>PHL</sub>			MAX	7.5	5.2	
t <sub>PZH</sub>			MAX	7.5	5.2	
t <sub>PZL</sub>			MAX	6.5	4.5	
t <sub>PHZ</sub>			MAX	6.5	4.5	
t <sub>PZL</sub>			MAX	6.5	4.5	

UNIT fmax : MHz, other : ns

## 4-BIT BISTABLE LATCHES

- Complementary Outputs ( $Q$ ,  $\bar{Q}$ )

Logic Diagram



FUNCTION TABLE

INPUTS		OUTPUTS	
D	C	Q	$\bar{Q}$
L	H	L	H
H	H	H	L
X	L	$Q_0$	$Q_0$

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	LS	SN74 HC	UNIT
$I_{CC}$	MAX	12	0.04	mA
$I_{OH}$	MAX	-0.4	-4	mA
$I_{OL}$	MAX	8	4	mA

TIMING REQUIREMENTS AND SWITCHING CHARACTERISTICS

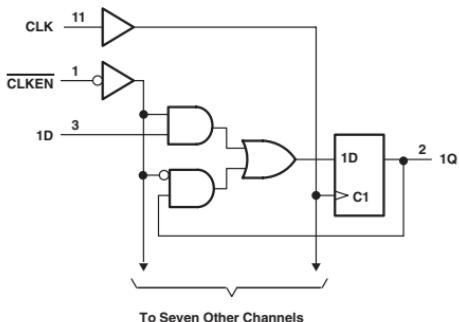
PARAMETER	INPUT	OUTPUT	MAX or MIN	LS	SN74 HC
$t_{PLH}$	D	$Q$	MIN	20	20
$t_{PHL}$			MIN	20	25
$t_{PHL}$			MIN	0	5
$t_{PLH}$	D	$\bar{Q}$	MAX	27	30
$t_{PHL}$			MAX	17	30
$t_{PLH}$	C	$Q$	MAX	20	30
$t_{PHL}$			MAX	15	30
$t_{PLH}$	C	$\bar{Q}$	MAX	27	33
$t_{PHL}$			MAX	25	33
$t_{PLH}$	$\bar{Q}$	$Q$	MAX	30	33
$t_{PHL}$			MAX	15	33

UNIT: ns

## OCTAL D-TYPE FLIP-FLOPS WITH CLOCK ENABLE

- Individual Data Input to Each Flip-Flop
- 74ACT11xxx: Product Available in Reduced-Noise Advanced CMOS (11000 Series)

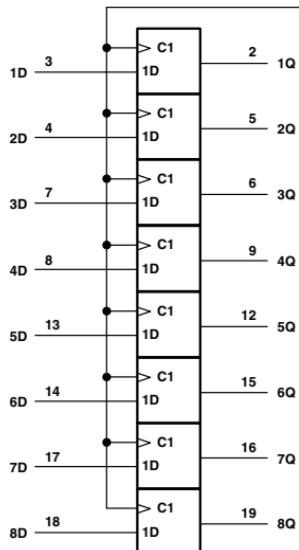
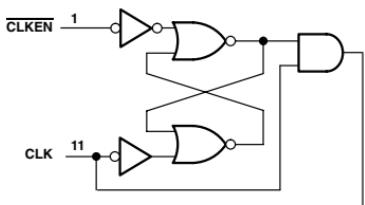
Logic Diagram (SN74ABT)



FUNCTION TABLE (SN74)

INPUTS			OUTPUTS	
CLKEN	CLOCK	DATA	Q	$\bar{Q}$
H	X	X	Q <sub>0</sub>	$\bar{Q}_0$
	↑	H	H	L
L	↑	L	L	H
X	L	X	Q <sub>0</sub>	$\bar{Q}_0$

Logic Diagram (SN74HC)



## ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	LS	F	SN74 HC	CD74 HC	SN74 HCT	CD74 HCT	ABT	AC 11	UNIT
I <sub>CC</sub>	MAX	28	90	0.08	0.16	0.08	0.16	30	0.08	mA
I <sub>OH</sub>	MAX	-0.4	-1	-4	-4	-4	-4	-32	-24	mA
I <sub>OL</sub>	MAX	8	20	4	4	4	4	64	24	mA

## TIMING REQUIREMENTS AND SWITCHING CHARACTERISTICS

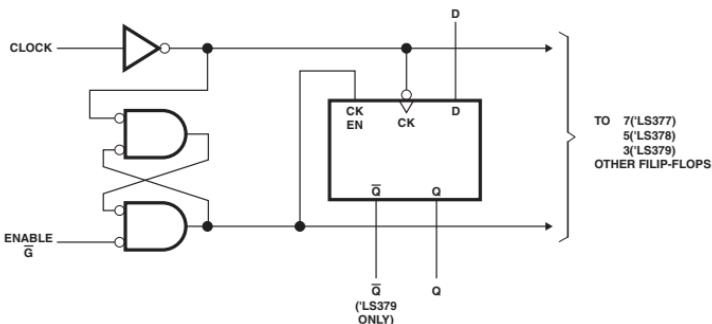
PARAMETER		INPUT	OUTPUT	MAX or MIN	LS	F	SN74 HC	CD74 HC	SN74 HCT	CD74 HCT	ABT	AC 11
f <sub>max</sub>				MIN	30	110	20	20	17	16	150	100
t <sub>w</sub>				MIN	20	5	25	24	25	30	3.3	5
t <sub>su</sub>		DATA		MIN	20	2	25	18	15	18	2.5	4
*CLKEN ACTIVE				MIN	25	2.5	25	-	15	-	3	6
*CLKEN INACTIVE				MIN	10	4.5	25	18	15	18	3	6
t <sub>th</sub>				MIN	5	1	5	5	5	5	1.8	0
t <sub>PLH</sub>		CLK (CD74: CP)	Q	MAX	27	10	40	53	45	57	6.5	11.3
t <sub>PHL</sub>				MAX	27	10.5	40	53	45	57	7.3	12.9

UNIT: f<sub>max</sub> : MHz, other : ns

\*CD74: E

## HEX D-TYPE FLIP-FLOPS WITH CLOCK ENABLE

Logic Diagram



FUNCTION TABLE

INPUTS			OUTPUTS	
G	CLOCK	DATA	Q	$\bar{Q}$
H	X	X	$Q_0$	$\bar{Q}_0$
L	↑	H	H	L
L	↑	L	L	H
X	L	X	$Q_0$	$\bar{Q}_0$

## ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	LS	F	SN74 HC	UNIT
$I_{CC}$	MAX	22	45	0.08	mA
$I_{OH}$	MAX	-0.4	-1	-4	mA
$I_{OL}$	MAX	8	20	4	mA

## TIMING REQUIREMENTS AND SWITCHING CHARACTERISTICS

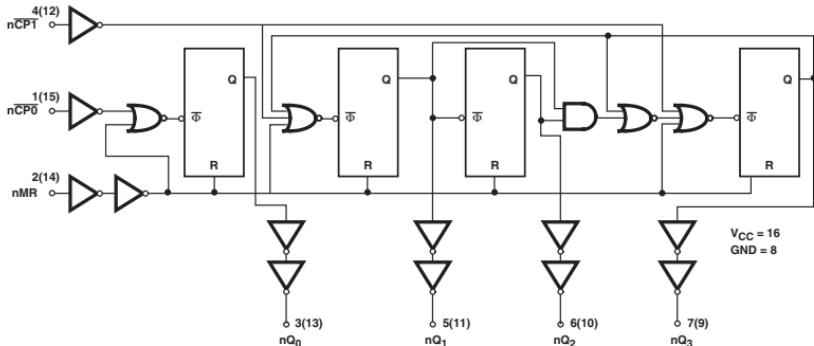
PARAMETER	INPUT	OUTPUT	MAX or MIN	LS	F	SN74 HC
$t_{max}$			MIN	30	110	20
$t_w$	CLK H		MIN	20	4	25
	CLK L		MIN	20	6	25
$t_{su}$	DATA		MIN	20	5	25
	$\bar{G}$ ACTIVE		MIN	25	3.5	25
$t_h$	$\bar{G}$ INACTIVE		MIN	10	5	25
			MIN	5↑	0	5
$t_{PLH}$	CLK	Q	MAX	27	6.7	40
			MAX	27	6.1	40

UNIT  $t_{max}$  : MHz, other : ns

## DUAL 4-BIT DECADE COUNTERS

- Individual Clock for A and B Flip-Flops Provide Dual + 2 and + 5 Counters
- All Have Direct Clear for Each 4-Bit Counter
- Typical maximum Count Frequency: 35MHz
- Buffered Outputs Reduce Possibility of Collector Commutation

Logic Diagram (CD74)



## FUNCTION TABLE (CD74)

## BCD COUNT SEQUENCE FOR 1/2

COUNT	OUTPUTS			
	Q <sub>3</sub>	Q <sub>2</sub>	Q <sub>1</sub>	Q <sub>0</sub>
0	L	L	L	L
1	L	L	H	L
2	L	L	H	L
3	L	H	H	H
4	L	H	L	L
5	L	H	L	H
6	L	H	H	L
7	L	H	H	H
8	H	L	L	L
9	H	L	L	H

## BI-QUINARY COUNT SEQUENCE FOR 1/2

COUNT	OUTPUTS			
	Q <sub>0</sub>	Q <sub>1</sub>	Q <sub>2</sub>	Q <sub>3</sub>
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	H	L	L	L
6	H	L	L	H
7	H	L	H	L
8	H	L	H	H
9	H	H	L	L

## ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	TTL	LS	SN74 HC	CD74 HC	CD74 HCT	UNIT
I <sub>CC</sub>	MAX	69	26	0.08	0.16	0.16	mA
I <sub>OH</sub>	MAX	-0.8	-0.4	-4	-4	-4	mA
I <sub>OL</sub>	MAX	16	8	4	4	4	mA

## TIMING REQUIREMENTS AND SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	TTL	LS	SN74 HC	CD74 HC	CD74 HCT
f <sub>max</sub>	nCKA (CD74: n $\bar{CP}_0$ )	nQA (CD74: n $Q_P_0$ )	MIN	25	25	25	20	18
	nCKB (CD74: n $\bar{CP}_1$ )	nQB (CD74: n $Q_P_1$ )	MIN	20	12.5	25	20	18
nV <sub>TH</sub>	nCKA (CD74: n $\bar{CP}_0$ )	MIN	20	20	20	24	29	
nV <sub>TH</sub>	nCKB (CD74: n $\bar{CP}_1$ )	MIN	25	40	20	24	29	
*CLR H		MIN	20	20	20	15	20	
t <sub>SU</sub>		MIN	25	25	5	-	-	
t <sub>PLH</sub>	nCKA (CD74: n $\bar{CP}_0$ )	nQA (CD74: n $Q_0$ )	MAX	20	20	30	53	60
t <sub>PLH</sub>	nCKB (CD74: n $\bar{CP}_1$ )	nQA (CD74: n $Q_1$ )	MAX	20	20	30	53	60
t <sub>PLH</sub>	nCKA (CD74: n $\bar{CP}_0$ )	nQC (CD74: n $Q_2$ )	MAX	60	60	72	-	126
t <sub>PLH</sub>	nCKB (CD74: n $\bar{CP}_1$ )	nQC (CD74: n $Q_2$ )	MAX	60	60	72	-	126
t <sub>PLH</sub>	nCKA (CD74: n $\bar{CP}_0$ )	nQB (CD74: n $Q_3$ )	MAX	21	21	33	56	65
t <sub>PLH</sub>	nCKB (CD74: n $\bar{CP}_1$ )	nQB (CD74: n $Q_3$ )	MAX	21	21	33	56	65
t <sub>PLH</sub>	nCKA (CD74: n $\bar{CP}_0$ )	nQC (CD74: n $Q_3$ )	MAX	39	39	46	74	83
t <sub>PLH</sub>	nCKB (CD74: n $\bar{CP}_1$ )	nQC (CD74: n $Q_3$ )	MAX	39	39	46	74	83
t <sub>PLH</sub>	nCKA (CD74: n $\bar{CP}_0$ )	nQD (CD74: n $Q_3$ )	MAX	21	21	33	54	63
t <sub>PLH</sub>	nCKB (CD74: n $\bar{CP}_1$ )	nQD (CD74: n $Q_3$ )	MAX	21	21	33	54	63
*CLR		Q	MAX	39	39	41	57	63

UNIT f<sub>max</sub> : MHz, other : ns

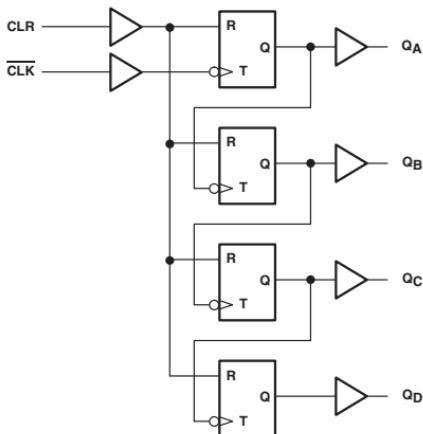
\*CD74: MR

**DUAL 4-BIT BINARY COUNTERS**

- Dual 4-Bit Binary Counter with Individual Clock
- All Have Direct Clear for Each 4-Bit Counter
- Typical maximum Count Frequency: 35MHz
- Buffered Outputs Reduce Possibility of Collector Commutation

**FUNCTION TABLE (SN74)**

COUNT	INPUTS			
	Q <sub>D</sub>	Q <sub>C</sub>	Q <sub>B</sub>	Q <sub>A</sub>
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	L	H	H	L
7	L	H	H	H
8	H	L	L	L
9	H	L	L	H
10	H	L	H	L
11	H	L	H	H
12	H	H	L	L
13	H	H	L	H
14	H	H	H	L
15	H	H	H	H

**Logic Diagram (SN74)****ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS**

PARAMETER	MAX or MIN	TTL	LS	SN74 HC	CD74 HC	CD74 HCT	LV 3V	LV 5V	UNIT
I <sub>CC</sub>	MAX	64	26	0.08	0.16	0.16	-	0.02	mA
I <sub>OH</sub>	MAX	-0.8	-0.4	-4	-4	-4	-6	-12	mA
I <sub>OL</sub>	MAX	16	8	4	4	4	6	12	mA

**TIMING REQUIREMENTS AND SWITCHING CHARACTERISTICS**

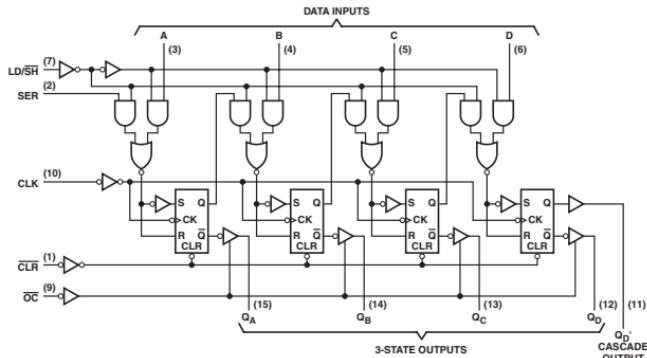
PARAMETER	INPUT	OUTPUT	MAX or MIN	TTL	LS	SN74 HC	CD74 HC	CD74 HCT	LV 3V	LV 5V
fmax			MIN	25	25	25	20	18	35	75
t <sub>W</sub>	CLK	A	MIN	20	20	20	24	29	5	5
		B	MIN	25	40	20	24	29	5	5
	CLR H		MIN	20	20	20	24	24	5	5
t <sub>SU</sub>			MIN	25	25	5	-	-	5	4
t <sub>PLH</sub>	CLKA (CD74:nCP)	QA	MAX	20	20	30	59	48	19	12
			MAX	20	20	30	59	48	19	12
t <sub>PHL</sub>	CLKB (CD74:nCP)	QD	MAX	60	60	72	86	93	26.5	16.5
			MAX	60	60	72	86	93	26.5	16.5
t <sub>PLH</sub>	CLR	Q	MAX	39	39	41	41	48	18	11.5

UNIT fmax : MHz, other : ns

## CASCADABLE SHIFT REGISTERS

- 3-State Outputs
- Parallel-In, Parallel-Out Registers
- Low Power Dissipation: 75mW Typical (Enable)

Logic Diagram



FUNCTION TABLE

CLEAR	LOAD/SHIFT CONTROL	INPUTS		3-STATE OUTPUTS				CASCADE OUTPUT QD
		CLOCK	SERIAL	A	B	C	D	
L	X	X	X	X X X X	X X X X	X X X X	X X X X	L L L L
H	H	H	X	X X X X	a b c d	X X X X	X X X X	Q <sub>A0</sub> Q <sub>B0</sub> Q <sub>C0</sub> Q <sub>D0</sub>
H	H	↓	X	a b c d	X X X X	X X X X	X X X X	Q <sub>b</sub> Q <sub>c</sub> Q <sub>d</sub>
H	L	L	H	X X X X	X X X X	X X X X	X X X X	Q <sub>A0</sub> Q <sub>Bn</sub> Q <sub>Cn</sub> Q <sub>Dn</sub>
H	L	↓	H	X X X X	X X X X	X X X X	X X X X	Q <sub>b</sub> Q <sub>An</sub> Q <sub>Bn</sub> Q <sub>Cn</sub>
H	L	↓	L	X X X X	X X X X	X X X X	X X X X	Q <sub>A0</sub> Q <sub>Bn</sub> Q <sub>Cn</sub> Q <sub>Dn</sub>

## ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER		MAX or MIN	LS	UNIT
Icc		MAX	34	mA
Ioh	QA, QB, QC, QD	MAX	-2.6	mA
	QD'	MAX	-0.4	mA
Iol	QA, QB, QC, QD	MAX	24	mA
	QD'	MAX	8	mA

## TIMING REQUIREMENTS AND SWITCHING CHARACTERISTICS

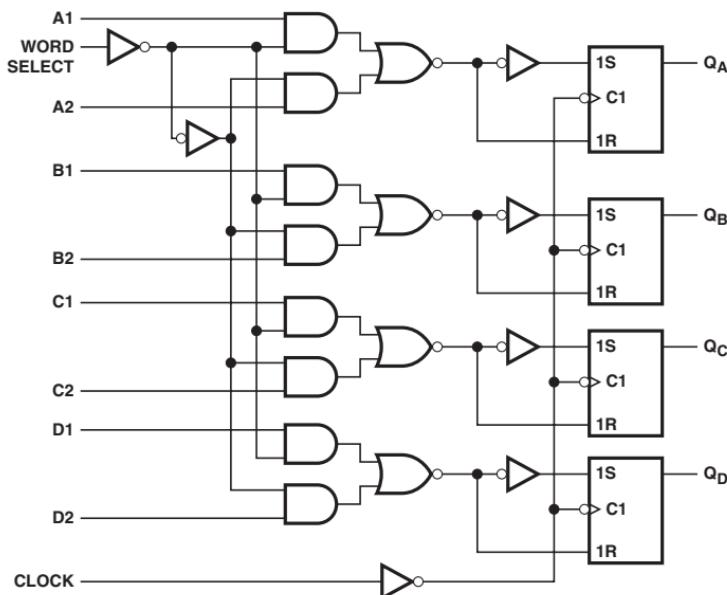
PARAMETER	INPUT	OUTPUT	MAX or MIN	LS
fmax	LD/S#		MIN	30
t <sub>w</sub>			MIN	16
t <sub>su</sub>			MIN	40
t <sub>th</sub>			MIN	20
t <sub>th</sub>			MIN	10
t <sub>PLH</sub>	CLK	Q	MAX	30
t <sub>PHL</sub>			MAX	30

UNIT fmax : MHz, other : ns

## QUADRUPLE 2-INPUT MULTIPLEXERS WITH STORAGE

- Single-Rail Outputs ( $Q$ ,  $\bar{Q}$ )
- Select One of Two 4-Bit Data Sources and Stores Data Synchronously with System Clock

Logic Diagram



FUNCTION TABLE

INPUTS		OUTPUTS			
WORD SELECT	CLOCK	Q <sub>A</sub>	Q <sub>B</sub>	Q <sub>C</sub>	Q <sub>D</sub>
L	↑	A <sub>1</sub>	B <sub>1</sub>	C <sub>1</sub>	D <sub>1</sub>
H	↑	A <sub>2</sub>	B <sub>2</sub>	C <sub>2</sub>	D <sub>2</sub>
X	L	Q <sub>A0</sub>	Q <sub>B0</sub>	Q <sub>C0</sub>	Q <sub>D0</sub>

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	LS	UNIT
I <sub>CC</sub>	MAX	13	mA
I <sub>OH</sub>	MAX	-0.4	mA
I <sub>OL</sub>	MAX	8	mA

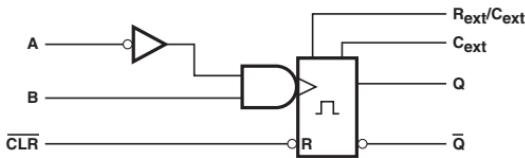
TIMING REQUIREMENTS AND SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	LS	
t <sub>W</sub>			MIN	20	
t <sub>su</sub>	DATA WORD SELECT		MIN	25	
t <sub>h</sub>			MIN	45	
t <sub>PLH</sub>	CLK	Q	MIN	0	
t <sub>PHL</sub>			MIN	0	
UNIT: ns			MAX	27	
			MAX	32	

## RETRIGGERABLE MONOSTABLE MULTIVIBRATORS

- Will Not Trigger from Clear

Logic Diagram (SN74LS)



FUNCTION TABLE (SN74LS)

INPUTS			OUTPUTS	
CLR	A	B	Q	$\bar{Q}$
L	X	X	L	H
X	H	X	L	H
X	X	L	L	H
H	L	↑	[T]	[T]
H	↓	H	[T]	[T]

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	LS	CD74 HC	CD74 HCT	UNIT
$I_{CC}$	MAX	20	0.16	0.16	mA
$I_{OH}$	MAX	-0.4	-4	-4	mA
$I_{OL}$	MAX	8	4	4	mA

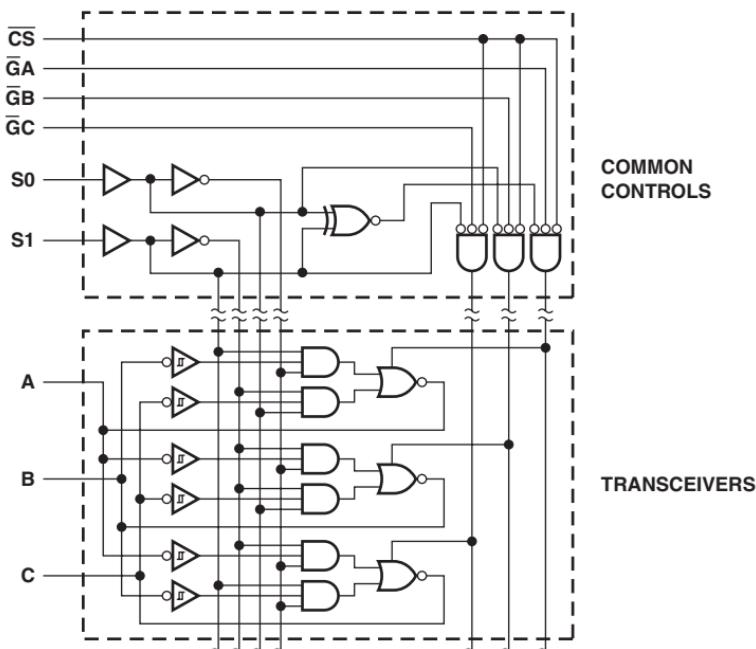
TIMING REQUIREMENTS AND SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	LS	CD74 HC	CD74 HCT
$t_W$			MIN	40	30	30
$t_{PLH}$	A (CD74: $\bar{A}$ )	Q	MAX	33	90	90
				44	90	90
$t_{PHL}$	A (CD74: $\bar{A}$ )	$\bar{Q}$	MAX	45	96	102
				56	96	102
$t_{PLH}$	CLR (CD74: $\bar{R}$ )	Q	MAX	27	65	72
		$\bar{Q}$	MAX	45	65	72

UNIT: ns

## QUADRUPLE TRIDIRECTIONAL BUS TRANSCEIVERS

Logic Diagram



FUNCTION TABLE

CS	S1	S0	GA	GB	GĀ	INPUTS		TRANSFERS		BUSES
						X	X	X	X	
H	X	X	X	X	X					None
X	H	H	X	X	X					None
X	X	X	H	H	H					None
X	L	L	X	H	H					None
X	L	H	H	X	H					None
X	H	L	H	H	X					None
L	L	L	X	L	L			A → B, A → C		
L	L	H	L	X	L			B → C, B → A		
L	H	L	L	L	X			C → A, C → B		
L	L	L	X	L	H			A → B		
L	L	H	H	X	L			B → C		
L	H	L	L	H	X			C → A		
L	L	L	X	H	L			A → C		
L	L	H	L	X	H			B → A		
L	H	L	H	L	X			C → B		

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	LS	UNIT
I <sub>CC</sub>	MAX	95	mA
I <sub>OH</sub>	MAX	-15	mA
I <sub>OL</sub>	MAX	24	mA

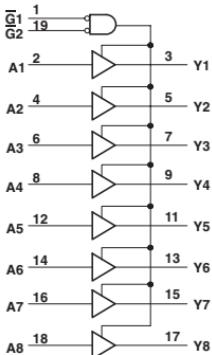
SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	LS
t <sub>PLH</sub>	A	B or C	MAX	14
	B	A or C		
	C	A or B		
t <sub>PHL</sub>	A	B or C	MAX	20
	B	A or C		
	C	A or B		
t <sub>PZL</sub>	Any Ḡ		MAX	33
	S <sub>0</sub> , S <sub>1</sub>			
	GĀ			
t <sub>PZH</sub>	Ḡ, S, CS	A, B, C	MAX	42
	Ḡ, S, CS̄	A, B, C		
t <sub>PZL</sub>	Ḡ, S, CS	A, B, C	MAX	36
t <sub>PZH</sub>	Ḡ, S, CS̄	A, B, C	MAX	32
t <sub>PZL</sub>	Ḡ, S, CS	A, B, C	MAX	35
t <sub>PZH</sub>	Ḡ, S, CS̄	A, B, C	MAX	25

UNIT: ns

: OBSOLETED or NOT RECOMMENDED NEW DESIGNS

## OCTAL BUFFERS WITH 3-STATE OUTPUTS



ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	LS	ALS	UNIT
I <sub>CC</sub>	MAX	37	33	mA
I <sub>OH</sub>	MAX	-2.6	-15	mA
I <sub>OL</sub>	MAX	24	24	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	LS	ALS
t <sub>PLH</sub>	A	Y	MAX	15	13
t <sub>PHL</sub>				18	12
t <sub>PZH</sub>	$\bar{G}$	Y	MAX	40	23
t <sub>PZL</sub>				45	25
t <sub>PHZ</sub>	$\bar{G}$	Y	MAX	40	10
t <sub>PZL</sub>				45	18

UNIT: ns

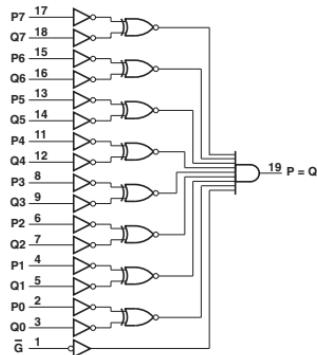
† These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

## OCTAL BINARY/BCD IDENTITY COMPARATORS WITH ENABLE

- Open-Collector Outputs
- 20-k $\Omega$  Pullup Resistors on Q Inputs

FUNCTION TABLE

INPUTS		OUTPUT
DATA P, Q	ENABLE G	P = Q
P = Q	L	H
P > Q	L	L
P < Q	L	L
X	H	L



ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	ALS	UNIT
I <sub>CC</sub>	MAX	17	mA
I <sub>OL</sub>	MAX	24	mA
V <sub>DH</sub>	MAX	5.5	V

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	ALS
t <sub>PLH</sub>	P or Q	P = Q	MAX	33
t <sub>PHL</sub>				15
t <sub>PZH</sub>	$\bar{G}$	P = Q	MAX	33
t <sub>PZL</sub>				15

UNIT: ns

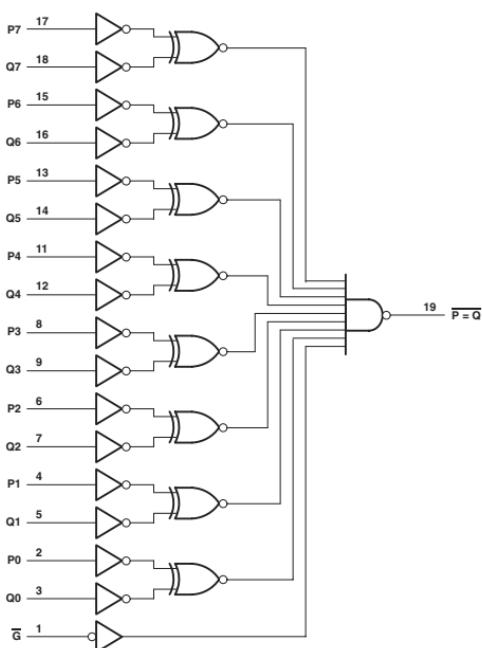
## OCTAL BINARY/BCD IDENTITY COMPARATORS WITH ENABLE

- 20-k $\Omega$  Pullup Resistors on Q Inputs
- 74AC11xxx: Product Available in Reduced-Noise Advanced CMOS (11000 Series)

FUNCTION TABLE

INPUTS		OUTPUT
DATA P, Q	ENABLE G	$\overline{P} = \overline{Q}$
P = Q	L	L
P > Q	L	H
P < Q	L	H
X	H	H

Logic Diagram



## ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	ALS	F	AC 11	UNIT
I <sub>CC</sub>	MAX	19	32	8	mA
I <sub>OH</sub>	MAX	-2.6	-1	-24	mA
I <sub>OL</sub>	MAX	24	20	24	mA

## SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	ALS	F	AC 11
t <sub>PLH</sub>	P or Q	$\overline{P} = \overline{Q}$	MAX	12	8.7	12.6
				20	10.3	11.3
t <sub>PHL</sub>	$\overline{OE}$	$\overline{P} = \overline{Q}$	MAX	12	6.4	7.4
				22	10.4	7.8

UNIT: ns

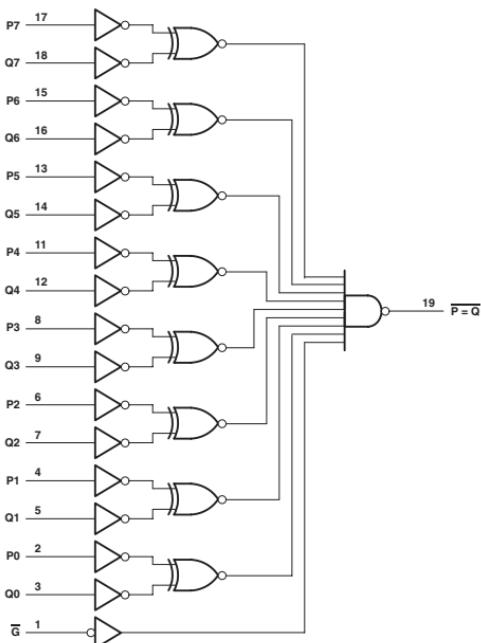
## 8-BIT IDENTITY COMPARATORS WITH OPEN-COLLECTOR OUTPUTS

- 74AC11xxx: Product Available in Reduced-Noise Advanced CMOS (11000 Series)

FUNCTION TABLE

INPUTS		OUTPUT
DATA P, Q	ENABLE G	$\overline{P} = \overline{Q}$
P = Q	L	L
P > Q	L	H
P < Q	L	H
X	H	H

Logic Diagram



## ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	ALS	F	AC 11	UNIT
I <sub>CC</sub>	MAX	19	32	0.08	mA
I <sub>OH</sub>	MAX	-2.6	-1	-24	mA
I <sub>OL</sub>	MAX	24	20	24	mA

## SWITCHING CHARACTERISTICS

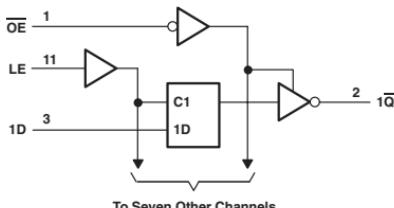
PARAMETER	INPUT	OUTPUT	MAX or MIN	ALS	F	AC 11
t <sub>PLH</sub>	P or Q	$\overline{P} = \overline{Q}$	MAX	12	11	13
t <sub>PHL</sub>				20	11	11.4
t <sub>PLH</sub>	$\overline{G}$	$\overline{P} = \overline{Q}$	MAX	12	7.5	7.9
t <sub>PHL</sub>				22	10	8.1

UNIT: ns

## OCTAL TRANSPARENT D-TYPE LATCHES WITH 3-STATE OUTPUTS

- 3-State Bus-Driving Inverting Outputs
- Functionally Equivalent to '373, Except for Having Inverted Outputs
- 74AC11xxx: Product Available in Reduced-Noise Advanced CMOS (11000 Series)
- 74ACT11xxx: Product Available in Reduced-Noise Advanced CMOS (11000 Series)

Logic Diagram (SN74)



FUNCTION TABLE (SN74)

INPUTS			OUTPUT
$\overline{OE}$	ENABLE	LE	$\bar{Q}$
L	H	H	L
L	H	L	H
L	L	X	$\bar{Q}_0$
H	X	X	Z

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	ALS	AS	SN74 HC	CD74 HC	SN74 HCT	CD74 HCT	ABT	AC 11	SN74 AC	ACT 11	SN74 ACT	UNIT
$I_{CC}$	MAX	28	110	0.08	0.16	0.08	0.16	30	0.08	0.04	0.08	0.04	mA
$I_{OH}$	MAX	-2.6	-15	-6	-6	-6	-6	-32	-24	-24	-24	-24	mA
$I_{OL}$	MAX	24	48	6	6	6	6	64	24	24	24	24	mA

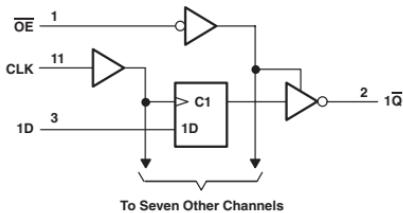
TIMING REQUIREMENTS AND SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN		ALS	AS	SN74 HC	CD74 HC	SN74 HCT	CD74 HCT	ABT	AC 11	SN74 AC	ACT 11	SN74 ACT
			MIN	MAX											
$t_{w}$					15	2	20	24	25	24	3.3	4	5	5	6
$t_{su}$					15	2	13	15	13	15	2.1	3.5	4.5	3.5	4
$t_{th}$					7	3	5	11	5	12	2.1	2	1	3.5	2.5
$t_{PLH}$	D	$\bar{Q}$	MAX	19	7.5	38	50	44	51	6.4	9.8	11	11.3	11.5	
$t_{PHL}$				13	7	38	50	44	51	6.6	8	10.5	9.5	11	
$t_{PLH}$	LE (CD74: LE)	$\bar{Q}$	MAX	23	9	44	53	44	57	7.3	11.3	11.5	13	11.5	
$t_{PHL}$				18	8	44	53	44	57	7.3	10.3	11	12.2	11.5	
$t_{ZH}$	$\overline{OE}$	$\bar{Q}$	MAX	17	6.5	38	45	44	53	5.7	10.8	10.5	12.5	11	
$t_{ZL}$				18	9.5	38	45	44	53	6.7	9.7	10.5	12	11	
$t_{HZ}$	$\overline{OE}$	$\bar{Q}$	MAX	10	6.5	38	45	44	45	6.9	11.4	11	12.8	11	
$t_{HL}$				16	7	38	45	44	45	6.5	8.9	11	10.3	11	

UNIT: ns

## OCTAL EDGE-TRIGGERED D-TYPE FLIP-FLOPS WITH 3-STATE OUTPUTS

- 3-State Bus-Driving Inverting Outputs
- '534 Have Inverted Outputs, But Otherwise Are Functionally Equivalent to '374
- 74AC11xxx: Product Available in Reduced-Noise Advanced CMOS (11000 Series)
- 74ACT11xxx: Product Available in Reduced-Noise Advanced CMOS (11000 Series)



FUNCTION TABLE (SN74)

INPUTS	OUTPUT		
OE	CLK	D	Q̄
L	↑	H	L
L	↑	L	H
L	H or L	X	Q̄ <sub>0</sub>
H	X	X	Z

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	ALS	AS	SN74 HC	CD74 HC	SN74 HCT	CD74 HCT	ABT	AC 11	SN74 AC	CD74 AC	ACT 11	SN74 ACT	UNIT
I <sub>CC</sub>	MAX	31	128	0.08	0.16	0.08	0.16	30	0.08	0.04	0.16	0.08	0.04	mA
I <sub>OH</sub>	MAX	-2.6	-15	-6	-6	-6	-6	-32	-24	-24	-24	-24	-24	mA
I <sub>OL</sub>	MAX	24	48	6	6	6	6	64	24	24	24	24	24	mA

TIMING REQUIREMENTS AND SWITCHING CHARACTERISTICS

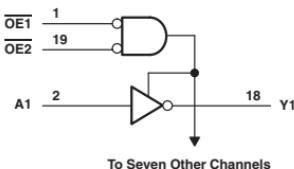
PARAMETER	INPUT	OUTPUT	MAX or MIN	ALS	AS	SN74 HC	CD74 HC	SN74 HCT	CD74 HCT	ABT	AC 11	SN74 AC	CD74 AC
f <sub>max</sub>			MIN	35	125	25	20	25	16	125	75	140	125
t <sub>w</sub>	CLK 'H'		MIN	14	4	20	24	20	30	3.5	6.5	4	4
	CLK 'L'		MIN	14	3	20	24	20	30	3.5	6.5	4	4
t <sub>su</sub>			MIN	10	2	25	18	25	30	1.6	3.5	4	2
t <sub>th</sub>			MIN	0	2	5	5	5	5	2	4.5	1.5	2
t <sub>PLH</sub>	CLK (CD74: CP)	Q̄	MAX	12	8	45	50	45	53	6.7	11.7	12	11.3
t <sub>PLH</sub>			MAX	16	9	45	50	45	53	7.6	12.1	11	11.3
t <sub>PZH</sub>	OE	Q̄	MAX	17	6	38	45	37	53	5	10.4	11.5	14.5
t <sub>PZL</sub>	OE	Q̄	MAX	18	10	38	45	37	53	6.8	10.4	11.5	14.5
t <sub>PHZ</sub>	OE	Q̄	MAX	10	6	38	45	37	45	7.3	11.6	12.5	14.5
t <sub>PZL</sub>	OE	Q̄	MAX	14	6	38	45	37	45	6.5	9.2	11	14.5

PARAMETER	INPUT	OUTPUT	MAX or MIN	ACT 11	SN74 ACT
f <sub>max</sub>			MIN	55	120
t <sub>w</sub>	CLK 'H'		MIN	9	3.5
	CLK 'L'		MIN	9	3.5
t <sub>su</sub>			MIN	3	4
				5.5	1.5
t <sub>th</sub>			MIN	14.5	12.5
t <sub>PLH</sub>	CLK (CD74: CP)	Q̄	MAX	15	12
t <sub>PLH</sub>			MAX	13.3	12.5
t <sub>PZH</sub>	OE	Q̄	MAX	13.5	11.5
t <sub>PZL</sub>	OE	Q̄	MAX	13.5	13.5
t <sub>PHZ</sub>	OE	Q̄	MAX	12	10.5
t <sub>PZL</sub>	OE	Q̄	MAX		

UNIT f<sub>max</sub> : MHz, other : ns

## OCTAL BUFFERS/DRIVERS WITH 3-STATE OUTPUTS

- 3-State Outputs Drive Bus Lines or Buffer Memory Address Registers
- P-N-P Inputs Reduce D-C Loading
- Schmitt-Triggered Inputs (SN74LS540)



FUNCTION TABLE (SN74)  
(each buffer/driver)

INPUTS			OUTPUT Y
OE1	OE2	A	
L	L	L	H
L	L	H	L
H	X	X	Z
X	H	X	Z

### ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	LS	ALS	ALS-1	SN74 HC	CD74 HC	SN74 HCT	CD74 HCT	SN74 BCT	ABT	LVTH 3V	CD74 AC	CD74 ACT	AHC	UNIT
I <sub>CC</sub>	MAX	52	22	22	0.08	0.16	0.08	0.16	71	30	5	0.16	0.16	0.04	mA
I <sub>OH</sub>	MAX	-15	-15	-15	-6	-6	-6	-6	-15	-32	-32	-24	-24	-8	mA
I <sub>OL</sub>	MAX	24	24	48	6	6	6	6	64	64	64	24	24	8	mA

PARAMETER	MAX or MIN	AHCT	LV 3V	LV 5V	LVC 3V	UNIT
I <sub>CC</sub>	MAX	0.04	-	0.02	0.01	mA
I <sub>OH</sub>	MAX	-8	-8	-16	-24	mA
I <sub>OL</sub>	MAX	8	8	16	24	mA

### SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	LS	ALS	ALS-1	SN74 HC	CD74 HC	SN74 HCT	CD74 HCT	SN74 BCT	ABT
I <sub>PLH</sub>	A	Y (CD74: $\bar{Y}$ )	MAX	15	12	12	25	33	25	36	6.9	4.8
				15	9	9	25	33	25	36	4	4.8
I <sub>PZH</sub>	$\bar{OE}$	Y (CD74: $\bar{Y}$ )	MAX	25	15	15	38	-	38	-	10.1	5.9
				38	20	20	38	-	38	-	11.3	6.4
I <sub>PHZ</sub>	$\bar{OE}$	Y (CD74: $\bar{Y}$ )	MAX	25	10	10	38	48	38	53	9	7.3
				18	12	12	38	48	38	53	8.5	6.2

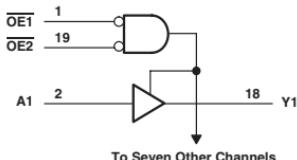
PARAMETER	INPUT	OUTPUT	MAX or MIN	LVTH 3V	CD74 AC	CD74 ACT	AHC	AHCT	LV 3V	LV 5V	LVC 3V
I <sub>PLH</sub>	A	Y (CD74: $\bar{Y}$ )	MAX	3.8	68	7.2	8	10	12	8	5.3
				3.8	68	7.2	8	10	12	8	5.3
I <sub>PZH</sub>	$\bar{OE}$	Y (CD74: $\bar{Y}$ )	MAX	5.2	12	13.4	10.5	12	16	10.5	6.6
				5.3	12	13.4	10.5	12	16	10.5	6.6
I <sub>PHZ</sub>	$\bar{OE}$	Y (CD74: $\bar{Y}$ )	MAX	5.6	12	13.4	10	12	17.5	10	7.4
				5	12	13.4	10	12	17.5	10	7.4

UNIT: ns

## OCTAL BUFFERS/DRIVERS WITH 3-STATE OUTPUTS

- 3-State Outputs Drive Bus Lines or Buffer Memory Address Registers
- P-N-P Inputs Reduce D-C Loading
- Schmitt-Triggered Inputs (SN74LS541)

Logic Diagram (SN74)

FUNCTION TABLE (SN74)  
(each buffer/driver)

INPUTS			OUTPUT
OE1	OE2	A	Y
L	L	L	L
L	L	H	H
H	X	X	Z
X	H	X	Z

### ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	LS	ALS	ALS-1	F	SN74 HC	CD74 HC	SN74 HCT	CD74 HCT	SN74 BCT	ABT	LVTH 3V	CD74 AC	UNIT
I <sub>CC</sub>	MAX	55	25	25	75	0.08	0.16	0.08	0.16	72	30	5	0.16	mA
I <sub>OH</sub>	MAX	-15	-15	-15	-15	-6	-6	-6	-6	-15	-32	-32	-24	mA
I <sub>OL</sub>	MAX	24	24	48	64	6	6	6	6	64	64	64	24	mA

PARAMETER	MAX or MIN	CD74 ACT	AHC	AHCT	LV 3V	LV 5V	LV-AT	LVC 3V	UNIT
I <sub>CC</sub>	MAX	0.16	0.04	0.04	-	0.02	0.02	0.01	mA
I <sub>OH</sub>	MAX	-24	-8	-8	-8	-16	-16	-24	mA
I <sub>OL</sub>	MAX	24	8	8	8	16	16	24	mA

### SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	LS	ALS	ALS-1	F	SN74 HC	CD74 HC	SN74 HCT	CD74 HCT	SN74 BCT	CD74 AC
I <sub>PLH</sub>	A	Y	MAX	15	14	14	6	29	35	29	42	6	
				18	10	10	6	29	35	29	42	8.2	
I <sub>PZH</sub>	$\overline{OE}$	Y	MAX	32	15	15	9.5	38	-	38	-	10.7	
				38	20	20	9.5	38	-	38	-	11.5	
I <sub>PLZ</sub>	$\overline{OE}$	Y	MAX	29	10	10	6.5	38	48	38	53	8.6	
				18	12	12	6	38	48	38	53	8.6	

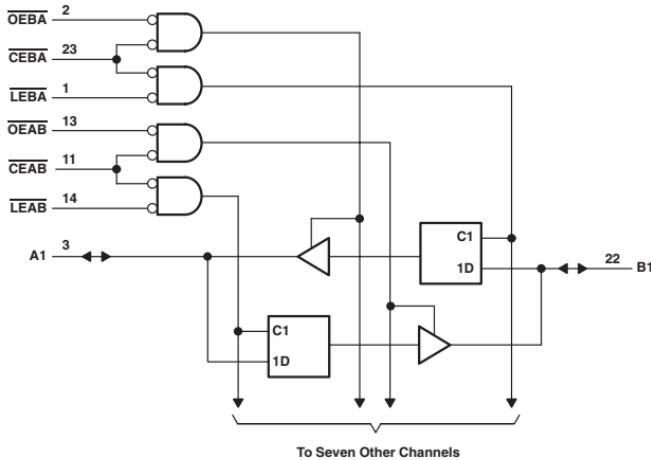
PARAMETER	INPUT	OUTPUT	MAX or MIN	ABT	LVTH 3V	CD74 AC	CD74 ACT	AHC	AHCT	LV 3V	LV 5V	LV-AT	LVC 3V
I <sub>PLH</sub>	A	Y	MAX	3.6	3.5	7.8	8.2	8	9.5	12	8	9	5.1
				3.9	3.5	7.8	8.2	8	9.5	12	8	9	5.1
I <sub>PZH</sub>	$\overline{OE}$	Y	MAX	4	5.2	12	13.4	10.5	12	16	10.5	14	7
				5.9	5.3	12	13.4	10.5	12	16	10.5	14	7
I <sub>PLZ</sub>	$\overline{OE}$	Y	MAX	5.8	5.6	12	13.4	10	12	17.5	10	13.5	7
				4.4	5	12	13.4	10	12	17.5	10	13.5	7

UNIT: ns

## OCTAL REGISTERED TRANSCEIVERS WITH 3-STATE OUTPUTS

- Back-to-Back Registers for Storage
- 3-State True Outputs
- 74ACT11xxx: Product Available in Reduced-Noise Advanced CMOS (11000 Series)

Logic Diagram



**FUNCTION TABLE<sup>†</sup>**

INPUTS				OUTPUT B
CEAB	LEAB	OEAB	A	
H	X	X	X	Z
X	X	H	X	Z
L	H	L	X	B <sub>0</sub> <sup>‡</sup>
L	L	L	L	L
L	L	L	H	H

<sup>†</sup> A-to-B data flow is shown; B-to-A flow control is the same except that it uses CEBA, LEBA, and OEBA.

<sup>‡</sup> Output level before the indicated steady-state input conditions were established

**ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS**

PARAMETER		MAX or MIN		F	SN74 BCT	ABT	LVT 3V	LVTH 3V	ACT 11	LVC 3V	UNIT
I <sub>CH</sub>		MAX	100	8	0.25	0.19	0.19	0.08	0.01	mA	
I <sub>CCL</sub>		MAX	125	71	30	12	5	0.08	0.01	mA	
I <sub>CC2</sub>		MAX	125	15	0.25	0.19	0.19	0.08	0.01	mA	
I <sub>OH</sub>	A	MAX	-3	-15	-32	-32	-32	-24	-24	mA	
	B	MAX	-15	-15	-32	-32	-32	-24	-24	mA	
I <sub>OL</sub>	A	MAX	24	64	64	64	64	24	24	mA	
	B	MAX	64	64	64	64	64	24	24	mA	

**TIMING REQUIREMENTS AND SWITCHING CHARACTERISTICS**

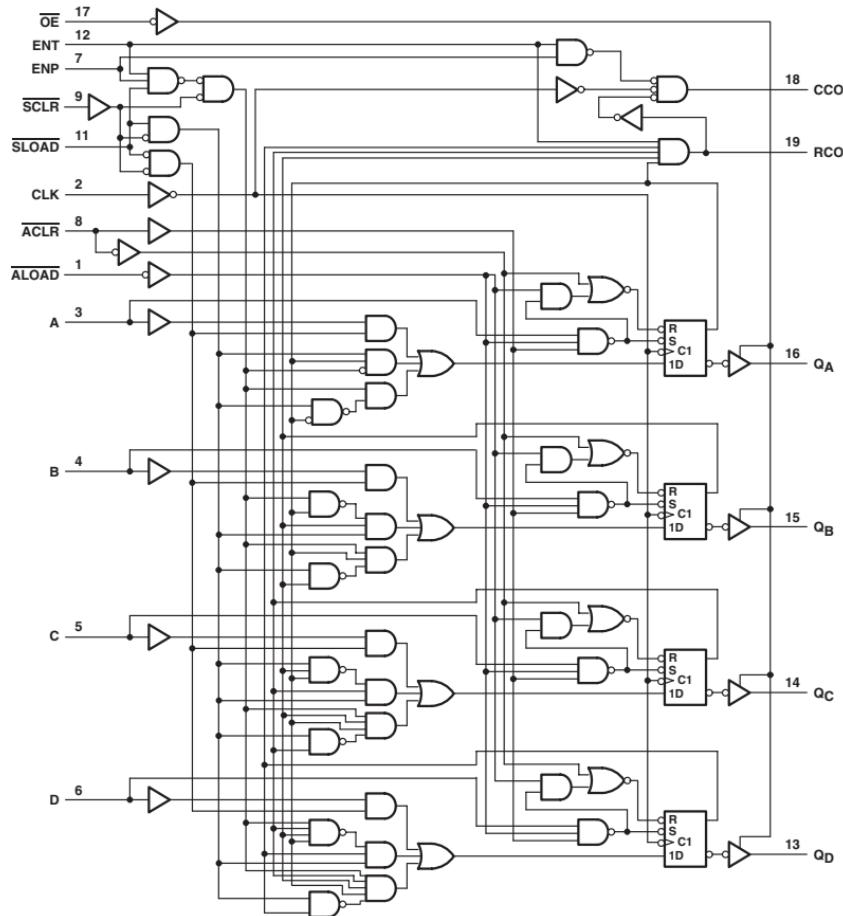
PARAMETER		INPUT	OUTPUT	MAX or MIN	F	SN74 BCT	ABT	LVT 3V	LVTH 3V	ACT 11	LVC 3V
t <sub>w</sub>				MIN	5	7	3.5	3.3	3.3	4	3.3
tsu	L <sub>E</sub> ↑ before 'H'				3.5	4.5	3.5	0	0.4	2.5	1.6
	L <sub>E</sub> ↑ before 'L'				3.5	4.5	3	0.8	1	2.5	1.6
	C <sub>E</sub> ↑ before 'H'				-	-	3.5	0	0.2	3	1.6
	C <sub>E</sub> ↑ before 'L'				-	-	3	0.9	0.7	3	1.6
th	L <sub>E</sub> ↓ after 'H'				3.5	1.5	0.5	1.7	1.5	2	2.1
	L <sub>E</sub> ↓ after 'L'				3.5	1.5	0.5	1.7	1.3	2	2.1
	C <sub>E</sub> ↓ after 'H'				-	-	0.5	1.8	1.6	1.5	2.1
	C <sub>E</sub> ↓ after 'L'				-	-	0.5	1.8	1.4	1.5	2.1
t <sub>PLH</sub>	A or B	B or A		MAX	8.5	8.8	6.9	4.7	3.7	10.2	7
t <sub>PLH</sub>					7.5	9.6	6.9	4.6	3.7	12.1	7
t <sub>PLH</sub>					12.5	12.9	6.6	5.9	4.7	11.2	8.5
t <sub>PHL</sub>	LEBA	A		MAX	12.5	12.7	7.1	5.7	4.7	13.2	8.5
t <sub>PLH</sub>	LEAB	B		MAX	12.5	12.9	6.6	5.9	4.7	11.2	8.5
t <sub>PHL</sub>					12.5	12.7	7.1	5.7	4.7	13.2	8.5
t <sub>PZH</sub>	OE	A or B		MAX	10	10.7	6.4	5.8	4.9	11.5	7.7
t <sub>PZL</sub>	OE	A or B		MAX	12	12.3	7.5	6.4	4.9	15.3	7.7
t <sub>PZH</sub>	OE	A or B		MAX	9	8.1	8.4	6.5	5.3	10.4	7
t <sub>PZL</sub>	OE	A or B		MAX	8.5	7.2	8	5.8	5.3	10.5	7
t <sub>PZH</sub>	CE	A or B		MAX	10	12	6.4	6	5.3	12.2	8
t <sub>PZL</sub>	CE	A or B		MAX	12	13.5	7.5	6.7	5.3	16	8
t <sub>PZH</sub>	CE	A or B		MAX	9	8.5	8.4	6.4	5.4	11	7
t <sub>PZL</sub>	CE	A or B		MAX	8.5	7.6	8	5.4	5.4	11.1	7

UNIT: ns

## SYNCHRONOUS 4-BIT COUNTERS WITH 3-STATE OUTPUTS

- 3-State Outputs
- Choice of Asynchronous or Synchronous Clearing and Loading
- Internal Look-Ahead Circuitry for Fast Cascading

Logic Diagram



FUNCTION TABLE

INPUTS							OPERATION	
OE	ACLK	ALOAD	SCLR	SLOAD	ENT	ENP	CLK	
H	X	X	X	X	X	X	X	Q outputs disabled
L	L	X	X	X	X	X	X	Asynchronous clear
L	H	L	X	X	X	X	X	Asynchronous load
L	H	H	L	X	X	X	↑	Synchronous clear
L	H	H	H	L	X	X	↑	Synchronous load
L	H	H	H	H	H	H	↑	Count
L	H	H	H	H	L	X	X	Inhibit counting
L	H	H	H	H	X	L	X	Inhibit counting

## ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER		MAX or MIN	ALS	UNIT
Icc		MAX	36	mA
Ioh	OUTPUT Q	MAX	-2.6	mA
	CCO & RCO	MAX	-0.4	mA
Iol		MAX	24	mA
		CCO & RCO	MAX	8 mA

## TIMING REQUIREMENTS AND SWITCHING CHARACTERISTICS

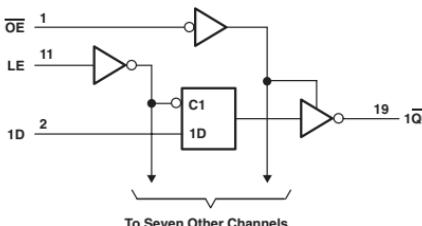
PARAMETER		INPUT	OUTPUT	MAX or MIN	ALS
fmax				MIN	30
tw	CLK "H"			MIN	16.5
	CLK "L"				16.5
tsu	ENP or ENT	H			20
		L			20
	A, B, C, D				20
	SCLR	L		MIN	15
		H			30
	SLOAD	L			15
		H			30
th				MIN	0
tPLH		CLK	Q	MAX	12
tPLH					18
tPLH		CLK	RCO	MAX	29
tPLH					24
tPLH		ALOAD	Q	MAX	35
tPLH					23
tPLH		ALOAD	CCO	MAX	55
tPLH					33
tPLH		ENT	RCO	MAX	16
tPLH					14
tPLH		ACLK	Q	MAX	22

UNIT fmax : MHz, other : ns

## OCTAL D-TYPE TRANSPARENT LATCHES WITH 3-STATE OUTPUTS

- 3-State Buffer-Type Outputs Drive Bus Lines Directly
- Bus-Structured Pinout

### Logic Diagram (SN74)



FUNCTION TABLE (SN74)

INPUTS			OUTPUT
$\overline{OE}$	ENABLE LE	D	$\overline{Q}$
L	H	H	L
L	H	L	H
L	L	X	$Q_0$
H	X	X	Z

### ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	ALS	SN74 HC	CD74 HC	SN74 HCT	CD74 HCT	SN74 AC	CD74 AC	SN74 ACT	UNIT
$I_{CC}$	MAX	29	0.08	0.16	0.08	0.16	0.08	0.16	0.04	mA
$I_{OH}$	MAX	-2.6	-6	-6	-6	-6	-24	-24	-24	mA
$I_{OL}$	MAX	24	6	6	6	6	24	24	24	mA

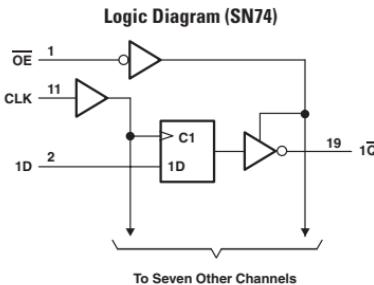
### TIMING REQUIREMENTS AND SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	ALS	SN74 HC	CD74 HC	SN74 HCT	CD74 HCT	SN74 AC	CD74 AC	SN74 ACT	
$t_{W}$				MIN	15	20	24	25	24	5	4	3
					10	13	15	13	15	2.5	2	4.5
					10	5	4	10	5	2	3	0
$t_{PLH}$	D	$\overline{Q}$	MAX		18	44	45	44	45	11.5	10.5	12.5
					14	44	45	44	45	11	10.5	11
$t_{PHL}$	LE (CD74: $\overline{LE}$ )	$\overline{Q}$	MAX		22	44	50	44	53	11	12	11.5
					21	44	50	44	53	9.5	12	10.5
$t_{PZH}$	$\overline{OE}$	$\overline{Q}$	MAX		18	38	45	44	53	10	10.5	10
					18	38	45	44	53	9.5	10.5	9.5
$t_{PZL}$	$\overline{OE}$	$\overline{Q}$	MAX		10	38	45	44	53	12	11.5	11.5
					15	38	45	44	53	9	11.5	8.5

UNIT: ns

## OCTAL D-TYPE EDGE-TRIGGERED FLIP-FLOPS WITH 3-STATE OUTPUTS

- 3-State Buffer-Type Inverting Outputs Drive Bus Lines Directly
- Bus-Structured Pinout



**FUNCTION TABLE (SN74)**

INPUTS			OUTPUT
$\overline{OE}$	CLK	D	Q
L	↑	H	L
L	↑	L	H
L	L	X	$\overline{Q}_0$
H	X	X	Z

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	ALS	SN74 HC	CD74 HC	SN74 HCT	CD74 HCT	SN74 AC	SN74 ACT	UNIT
$I_{CC}$	MAX	30	0.08	0.16	0.08	0.16	0.04	0.04	mA
$I_{OH}$	MAX	-2.6	-6	-6	-6	-6	-24	-24	mA
$I_{OL}$	MAX	24	6	6	6	6	24	24	mA

TIMING REQUIREMENTS AND SWITCHING CHARACTERISTICS

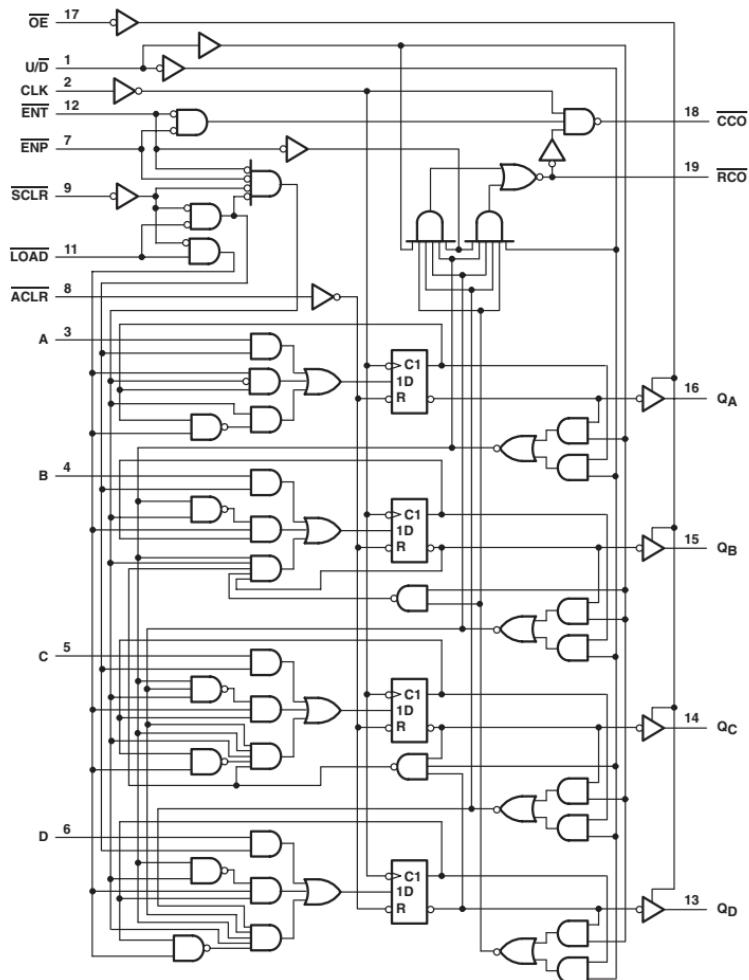
PARAMETER	INPUT	OUTPUT	MAX or MIN	ALS	SN74 HC	CD74 HC	SN74 HCT	CD74 HCT	SN74 AC	SN74 ACT
$f_{max}$			MIN	30	25	20	25	16	85	75
$t_{w}$	CLK 'H'		MIN	14	20	24	20	30	5	3.5
	CLK 'L'			14	20	24	20	30	5	3.5
$t_{su}$	CLK ↑		MIN	15	25	18	25	30	2.5	3
$t_{th}$	CLK ↑			0	5	5	5	3	2	1
$t_{PLH}$	CLK	$\bar{Q}$	MAX	14	45	50	45	53	11.5	11.5
$t_{PHL}$				14	45	50	45	53	10.5	10.5
$t_{PZH}$	$\overline{OE}$	$\bar{Q}$	MAX	18	38	45	38	53	9.5	9.5
$t_{PZL}$				18	38	45	38	53	9.5	9.5
$t_{PHZ}$	$\overline{OE}$	$\bar{Q}$	MAX	10	38	41	38	45	11.5	11.5
$t_{PZT}$				15	38	41	38	45	9	8.5

UNIT  $f_{max}$  : MHz, other : ns

## SYNCHRONOUS 4-BIT UP/DOWN BINARY COUNTERS WITH 3-STATE OUTPUTS

- 3-State Q Outputs Drive Bus Lines Directly
- Fully Synchronous Clear, Count, and Load
- Asynchronous Clear Is Also Provided
- Fully Cascadable

Logic Diagram



FUNCTION TABLE

INPUTS							OPERATION
OE	ACLR	SCLR	LOAD	ENT	ENP	UD	
H	X	X	X	X	X	X	Q outputs disabled
L	L	X	X	X	X	X	Asynchronous clear
L	H	L	X	X	X	↑	Synchronous clear
L	H	H	L	X	X	↑	Load
L	H	H	H	L	L	↑	Count up
L	H	H	H	H	L	↓	Count down
L	H	H	H	H	X	X	Inhibit count
L	H	H	H	X	H	X	Inhibit count

## ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER		MAX or MIN	ALS	UNIT
Icc		MAX	32	mA
Ioh	OUTPUT Q	MAX	-2.6	mA
	CCO & RCO		-0.4	mA
Iol	OUTPUT Q	MAX	24	mA
	CCO & RCO		8	mA

## TIMING REQUIREMENTS AND SWITCHING CHARACTERISTICS

PARAMETER		INPUT	OUTPUT	MAX or MIN	ALS
fmax		CLK 'H' CLK 'L'		MIN	30
tw	ACLR, LOAD			MIN	15
	ENP, ENT			MIN	16.5
tsu	DATA at A, B, C, D			MIN	16.5
	High			MIN	20
	Low			MIN	30
	SCLR			MIN	20
	High			MIN	15
	Low			MIN	30
	LOAD			MIN	15
	High			MIN	30
	Low			MIN	30
	UD			MIN	10
	ACLR			MIN	0
th		CLK	ANY Q	MAX	13
tpLH				MAX	16
tpHL		CLK	RCO	MAX	28
tpHL				MAX	19
tpLH		ENT	RCO	MAX	15
tpHL				MAX	13
tpHL		ACLR	Q	MAX	20
tpZL				MAX	18
tpZH		OE	Q	MAX	24
tpHZ				MAX	10
tpLZ		OE	Q	MAX	13

UNIT fmax : MHz, other : ns

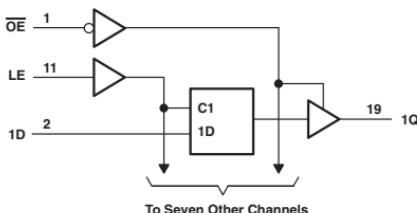
## OCTAL TRANSPARENT D-TYPE LATCHES WITH 3-STATE OUTPUTS

- 3-State Buffer-Type Outputs Drive Bus Lines Directly
- Bus-Structured Pinout

FUNCTION TABLE (SN74)

INPUTS			OUTPUT Q
OE	ENABLE	D	
L	H	H	H
L	H	L	L
L	L	X	Q <sub>0</sub>
H	X	X	Z

Logic Diagram (SN74)



ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	ALS	AS	F	SN74 HC	CD74 HC	SN74 HCT	CD74 HCT	SN74 BCT	ABT	LVT 3V	LVTH 3V	SN74 AC	CD74 AC	UNIT
I <sub>CC</sub>	MAX	27	106	55	0.08	0.16	0.08	0.16	62	30	12	5	0.04	0.16	mA
I <sub>OH</sub>	MAX	-2.6	-15	-3	-6	-6	-6	-6	-15	-32	-32	-32	-24	-24	mA
I <sub>OL</sub>	MAX	24	48	24	6	6	6	6	64	64	64	64	24	24	mA

PARAMETER	MAX or MIN	SN74 ACT	CD74 ACT	AHC	AHCT	LV 3V	LV 5V	LV-AT	LVC 3V	UNIT
I <sub>CC</sub>	MAX	0.04	0.16	0.04	0.04	-	0.02	0.02	0.01	mA
I <sub>OH</sub>	MAX	-24	-24	-8	-8	-8	-16	-16	-24	mA
I <sub>OL</sub>	MAX	24	24	8	8	8	16	16	24	mA

## TIMING REQUIREMENTS AND SWITCHING CHARACTERISTICS

PARAMETER		INPUT	OUTPUT	MAX or MIN	ALS	AS	F	SN74 HC	CD74 HC	SN74 HCT	CD74 HCT	SN74 BCT
tw	LE	LE ↓	LE ↓	MIN	10	4.5	6	20	24	25	24	4
tsu	LE ↓				10	2	2	13	15	13	20	1
th	LE ↓				7	3	3	5	12	5	15	4
tpLH	D	Q	MAX	MAX	14	8	8	44	53	44	53	8.4
tpHL					14	7	6	44	53	44	53	9.6
tpLH	LE	Q	MAX	MAX	20	13	13	44	53	44	53	8.1
tpHL					19	7.5	8	44	53	44	53	7.8
tpZH	$\overline{OE}$	Q	MAX	MAX	18	6.5	12	38	45	44	53	10.4
tpZL					18	9.5	8.5	38	45	44	53	11
tpHZ	$\overline{OE}$	Q	MAX	MAX	10	6.5	7.5	38	45	44	53	6
tpLZ					15	7	6	38	45	44	53	6

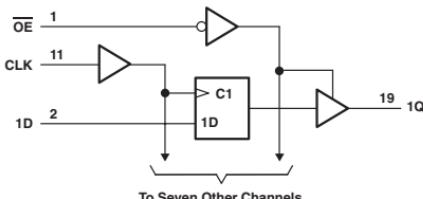
PARAMETER		INPUT	OUTPUT	MAX or MIN	ABT	LVT 3V	LVTH 3V	SN74 AC	CD74 AC	SN74 ACT	CD74 ACT	AHC
tw	LE	LE ↓	LE ↓	MIN	3.3	3.3	3	5	4	4	4	5
tsu	LE ↓				1.9	0.7	0.7	3.5	2	3.5	2	3.5
th	LE ↓				1.8	1.6	1.5	2	3	0	3	1.5
tpLH	D	Q	MAX	MAX	5.9	4.2	3.9	11.5	8.5	12	10.4	10
tpHL					6.2	4.3	3.9	11	8.5	12	10.4	10
tpLH	LE (CD74AC/ACT: LE)	Q	MAX	MAX	6.6	5.6	4.2	11	12	12	12.5	11
tpHL					7.2	6.5	4.2	10	12	10.5	12.5	11
tpZH	$\overline{OE}$	Q	MAX	MAX	5.2	5.1	5.1	10	10.5	11	13.5	11
tpZL					6.7	5.5	5.1	9.5	10.5	10.5	13.5	11
tpHZ	$\overline{OE}$	Q	MAX	MAX	7.1	5.7	4.9	12	11.5	12.5	12.5	11
tpLZ					6.5	4.6	4.6	9	11.5	9.5	12.5	11

PARAMETER		INPUT	OUTPUT	MAX or MIN	AHCT	LV 3V	LV 5V	LV-AT	LVC 3V
tw	LE	LE ↓	LE ↓	MIN	5	5	5	8.5	3.3
tsu	LE ↓				3.5	3.5	3.5	1.5	2
th	LE ↓				1.5	1.5	1.5	3.5	1.5
tpLH	D	Q	MAX	MAX	7.5	16.5	10	10.5	6.9
tpHL					10	16.5	10	10.5	6.9
tpLH	LE (CD74AC/ACT: LE)	Q	MAX	MAX	8.5	17.5	11	14.5	7.7
tpHL					10	17.5	11	14.5	7.7
tpZH	$\overline{OE}$	Q	MAX	MAX	8	17	11	13.5	7.5
tpZL					11	17	11	13.5	7.5
tpHZ	$\overline{OE}$	Q	MAX	MAX	12	16.5	11	12	6.5
tpLZ					10.5	16.5	11	12	6.5

UNIT: ns

**OCTAL EDGE-TRIGGERED D-TYPE FLIP-FLOPS  
WITH 3-STATE OUTPUTS**

- 3-State Buffer-Type Noninverting Outputs Drive Bus Lines Directly
- Bus-Structured Pinout



FUNCTION TABLE (SN74)

INPUTS		OUTPUT	
OE	CLK	D	Q
L	↑	H	H
L	↑	L	L
L	L	X	$Q_0$
H	X	X	Z

## ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	ALS	AS	F	SN74 HC	CD74 HC	SN74 HCT	CD74 HCT	SN74 BCT	ABT	LVT 3V	LVTH 3V	SN74 AC	UNIT
$I_{CC}$	MAX	28	134	86	0.08	0.16	0.08	0.16	62	30	12	5	0.04	mA
$I_{OH}$	MAX	-2.6	-15	-3	-6	-6	-6	-6	-15	-32	-32	-32	-24	mA
$I_{OL}$	MAX	24	48	24	6	6	6	6	64	64	64	64	24	mA

PARAMETER	MAX or MIN	CD74 AC	SN74 ACT	CD74 ACT	AHC	AHCT	LV 3V	LV 5V	LVC 3V	UNIT
$I_{CC}$	MAX	0.16	0.04	0.16	0.04	0.04	-	0.02	0.01	mA
$I_{OH}$	MAX	-24	-24	-24	-8	-8	-8	-16	-24	mA
$I_{OL}$	MAX	24	24	24	8	8	8	16	24	mA

## TIMING REQUIREMENTS AND SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	ALS	AS	F	SN74 HC	CD74 HC	SN74 HCT	CD74 HCT	SN74 BCT
fmax			MIN	35	125	100	24	20	24	20	77
t <sub>w</sub>			MIN	14	5.5	7	20	24	20	24	6.5
t <sub>su</sub>			MIN	15	5.5	2	25	18	25	18	6
t <sub>th</sub>			MIN	0	0	2	5	5	5	5	0
t <sub>PLH</sub>	CLK (CD74: CP)	Q	MAX	14	8	10	45	50	45	50	10
t <sub>PHL</sub>			MAX	14	9	10	45	50	45	50	8.9
t <sub>PZH</sub>			MAX	18	6	12.5	38	45	38	45	10.4
t <sub>PZL</sub>			MAX	18	10	8.5	38	45	38	45	10.9
t <sub>PHZ</sub>	$\overline{OE}$	Q	MAX	10	6	8	38	41	38	42	7.5
t <sub>PZL</sub>			MAX	12	6	6.5	38	41	38	42	6.4

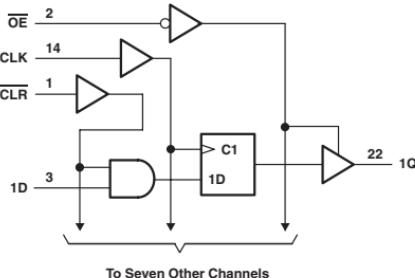
PARAMETER	INPUT	OUTPUT	MAX or MIN	ABT	LVT 3V	LVT 3V	SN74 AC	CD74 AC	SN74 ACT	CD74 ACT	AHC
fmax			MIN	150	150	150	85	125	85	110	75
t <sub>w</sub>			MIN	3.3	3.3	3.3	5	4	4	4.5	5
t <sub>su</sub>			MIN	1.5	2	2	2	2	2.5	2	3
t <sub>th</sub>			MIN	1.8	0.3	0.3	1.5	2	1	3	1.5
t <sub>PLH</sub>	CLK (CD74: CP)	Q	MAX	6.8	5.4	4.5	11	10.8	12	11.2	12
t <sub>PHL</sub>			MAX	7.1	5.9	4.5	9.5	10.8	11	11.2	12
t <sub>PZH</sub>			MAX	5.1	4.8	4.8	9	14.5	10	14.5	12.5
t <sub>PZL</sub>			MAX	6.7	5.1	4.8	9	14.5	10	14.5	12.5
t <sub>PHZ</sub>	$\overline{OE}$	Q	MAX	7	5.5	4.8	10.5	14.5	11.5	14.5	11.5
t <sub>PZL</sub>			MAX	6.5	4.5	4.4	8.5	14.5	9	14.5	11.5

PARAMETER	INPUT	OUTPUT	MAX or MIN	AHCT	LV 3V	LV 5V	LVC 3V
fmax			MIN	75	45	75	150
t <sub>w</sub>			MIN	5.5	5	5	3.3
t <sub>su</sub>			MIN	3.5	3.5	3.5	2
t <sub>th</sub>			MIN	1.5	1.5	1.5	1.5
t <sub>PLH</sub>	CLK (CD74: CP)	Q	MAX	12	19	12	7
t <sub>PHL</sub>			MAX	12	19	12	7
t <sub>PZH</sub>			MAX	12.5	18.5	12.5	7.5
t <sub>PZL</sub>			MAX	12.5	18.5	12.5	7.5
t <sub>PHZ</sub>	$\overline{OE}$	Q	MAX	11.5	17	11.5	6.4
t <sub>PZL</sub>			MAX	11.5	17	11.5	6.4

UNIT fmax : MHz, other : ns

## OCTAL D-TYPE EDGE-TRIGGERED FLIP-FLOPS WITH 3-STATE OUTPUTS

- 3-State Buffer-Type Noninverting Outputs Drive Bus Lines Directly
- Bus-Structured Pinout
- Synchronous Clear



FUNCTION TABLE

INPUTS				OUTPUT
OE	CLR	CLK	D	Q
L	L	↑	X	L
L	H	↑	H	H
L	H	↑	L	L
L	H	L	X	Q <sub>0</sub>
H	X	X	X	Z

## ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	ALS	AS	UNIT
I <sub>CC</sub>	MAX	30	142	mA
I <sub>OH</sub>	MAX	-2.6	-15	mA
I <sub>OL</sub>	MAX	24	48	mA

## TIMING REQUIREMENTS AND SWITCHING CHARACTERISTICS

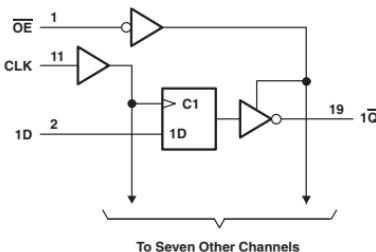
PARAMETER	INPUT	OUTPUT	MAX or MIN	ALS	AS
fmax			MIN	30	90
t <sub>w</sub>	CLK   H CLK   L			16.5	5.5 5.5
t <sub>su</sub>	DATA CLR   L		MIN	15	5.5 6.5
t <sub>th</sub>	DATA CLR			0	3 0
t <sub>PHL</sub>		CLK	MAX	14	8
t <sub>PHL</sub>		Q		14	9
t <sub>PZH</sub>		Q	MAX	18	6
t <sub>PZL</sub>		Q		18	10
t <sub>PHZ</sub>		Q	MAX	10	6
t <sub>PZL</sub>		Q		13	6

UNIT fmax : MHz, other : ns

## OCTAL D-TYPE EDGE-TRIGGERED FLIP-FLOPS WITH 3-STATE OUTPUTS

- 3-State Buffer-Type Inverting Outputs Drive Bus Lines Directly
- Bus-Structured Pinout
- Functionally Equivalent to '576, Except for Having Inverted Outputs

Logic Diagram



FUNCTION TABLE

INPUTS			OUTPUT
OE	CLK	D	Q
L	↑	H	L
L	↑	L	H
L	L	X	Q̄₀
H	X	X	Z

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	ALS	AS	UNIT
I <sub>CC</sub>	MAX	30	135	mA
I <sub>OH</sub>	MAX	-2.6	-15	mA
I <sub>OL</sub>	MAX	24	48	mA

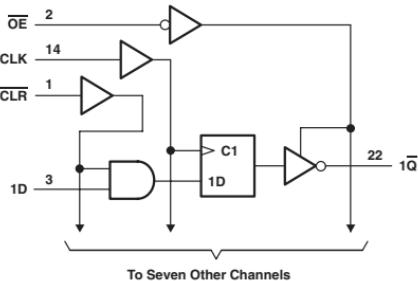
TIMING REQUIREMENTS AND SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	ALS	AS
f <sub>max</sub>			MIN	30	125
t <sub>w</sub>	H			16.5	4
	L				2
t <sub>su</sub>	DATA		MIN	15	2
t <sub>th</sub>	DATA			0	2
t <sub>pLH</sub>			MAX	14	8
t <sub>pHL</sub>				14	9
t <sub>pZH</sub>		Q̄	MAX	18	6
t <sub>pZL</sub>		Q̄		18	10
t <sub>pHZ</sub>		Q̄	MAX	10	6
t <sub>pLZ</sub>		Q̄		15	6

UNIT f<sub>max</sub> : MHz, other : ns

**OCTAL D-TYPE EDGE-TRIGGERED FLIP-FLOPS  
WITH 3-STATE OUTPUTS**

- 3-State Buffer-Type Inverting Outputs Drive Bus Lines Directly
- Bus-Structured Pinout
- Synchronous Clear



FUNCTION TABLE

INPUTS				OUTPUT
OE	CLR	CLK	D	$\bar{Q}$
L	L	↑	X	H
L	H	↑	H	L
L	H	↑	L	H
L	H	L	X	$\bar{Q}_0$
H	X	X	X	Z

## ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	ALS	AS	UNIT
$I_{CC}$	MAX	30	142	mA
$I_{OH}$	MAX	-2.6	-15	mA
$I_{OL}$	MAX	24	48	mA

## TIMING REQUIREMENTS AND SWITCHING CHARACTERISTICS

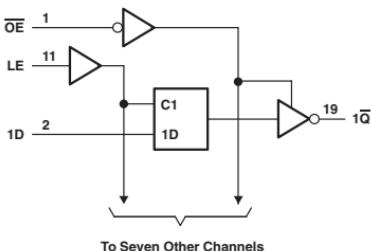
PARAMETER	INPUT	OUTPUT	MAX or MIN	ALS	AS
$t_{max}$			MIN	30	125
$t_w$				16.5	4
$t_{su}$	DATA		MIN	15	2
$t_h$	CLR			0	2
$t_{PLH}$	CLK	$\bar{Q}$	MAX	14	8
$t_{PHL}$				14	9
$t_{PZH}$	$\bar{OE}$	$\bar{Q}$	MAX	18	6
$t_{PZL}$				18	10
$t_{PHZ}$	$\bar{OE}$	$\bar{Q}$	MAX	10	6
$t_{PLZ}$				15	6

UNIT  $t_{max}$  : MHz, other : ns

## OCTAL D-TYPE TRANSPARENT LATCHES WITH 3-STATE OUTPUTS

- 3-State Buffer-Type Outputs Drive Bus Lines Directly
- Inverting-Logic Outputs
- Bus-Structured Pinout

Logic Diagram



FUNCTION TABLE

INPUTS			OUTPUT
ENABLE			Q
OE	LE	D	
L	H	H	L
L	H	L	H
L	L	X	$\bar{Q}_0$
H	X	X	Z

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	ALS	AS	UNIT
I <sub>CC</sub>	MAX	29	115	mA
I <sub>OH</sub>	MAX	-2.6	-15	mA
I <sub>OL</sub>	MAX	24	48	mA

TIMING REQUIREMENTS AND SWITCHING CHARACTERISTICS

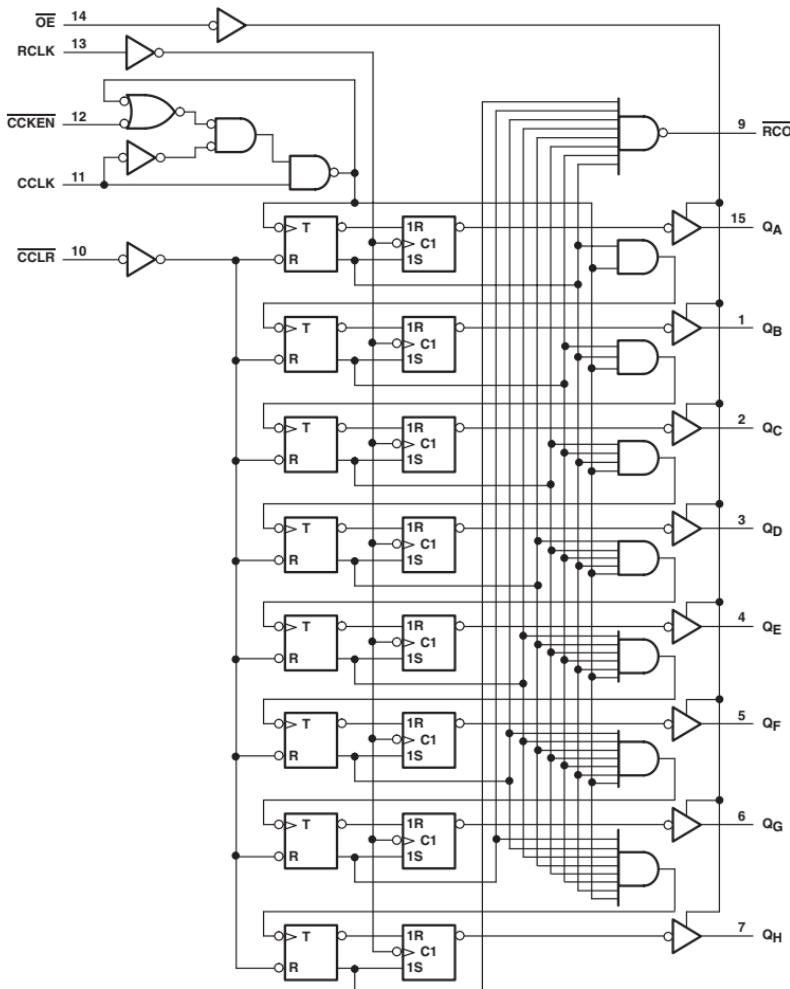
PARAMETER	INPUT	OUTPUT	MAX or MIN	ALS	AS
t <sub>w</sub>	C ↓		MIN	15	2
t <sub>su</sub>				10	2
t <sub>th</sub>				10	3
t <sub>PLH</sub>	D	$\bar{Q}$	MAX	18	7.5
t <sub>PHL</sub>				14	7
t <sub>PLH</sub>	LE	$\bar{Q}$	MAX	22	9
t <sub>PHL</sub>				21	8
t <sub>PZH</sub>	$\bar{OE}$	$\bar{Q}$	MAX	18	6.5
t <sub>PZL</sub>				18	9.5
t <sub>PHZ</sub>	$\bar{OE}$	$\bar{Q}$	MAX	10	6.5
t <sub>PLZ</sub>				15	7

UNIT: ns

## 8-BIT BINARY COUNTERS WITH 3-STATE OUTPUT REGISTERS

- Parallel Register Outputs
- Counter Has Direct Clear
- 3-State Outputs
- Guaranteed Counter Frequency: DC to 20MHz

Logic Diagram



## ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER		MAX or MIN	LS	SN74 HC	UNIT
I <sub>CC</sub>		MAX	65	0.08	mA
	RCO	MAX	-1	-4	mA
I <sub>OH</sub>	Q	MAX	-2.6	-6	mA
	RCO	MAX	16	4	mA
I <sub>OL</sub>	Q	MAX	24	6	mA

## TIMING REQUIREMENTS AND SWITCHING CHARACTERISTICS

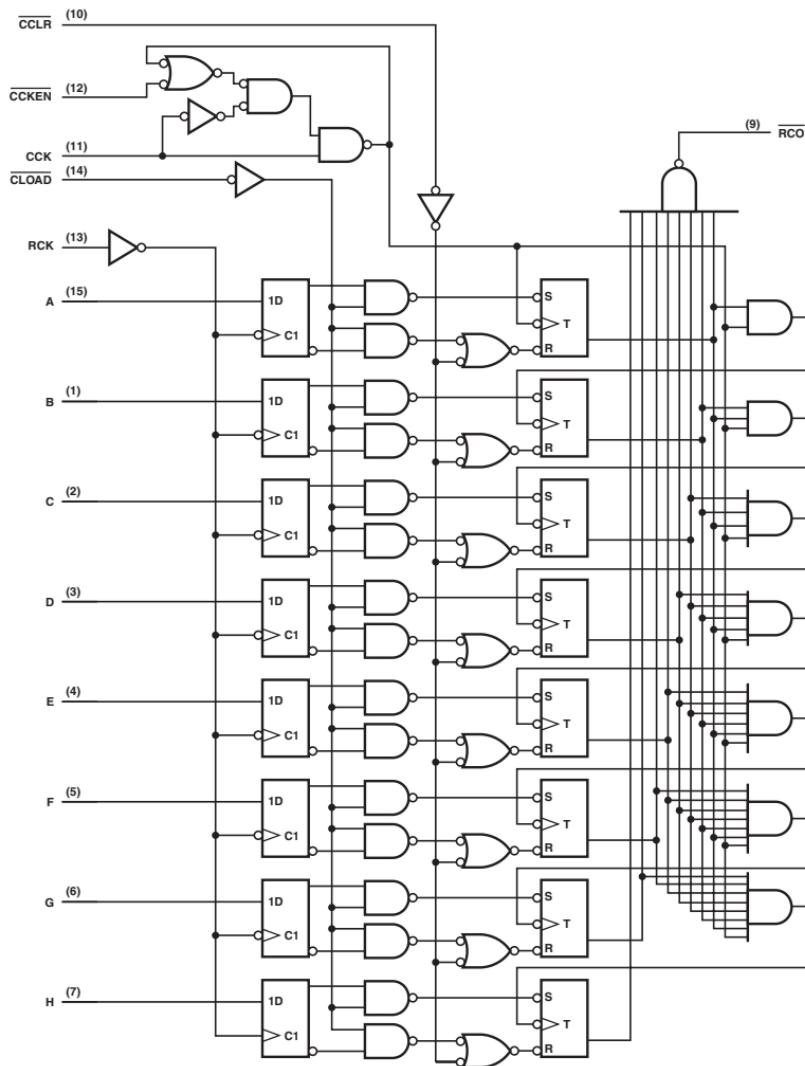
PARAMETER		INPUT	OUTPUT	MAX or MIN	LS	SN74 HC
f <sub>max</sub>		CCK	RCO	MIN	20	13
t <sub>w</sub>	CCK			MIN	25	31
	CCLR				20	25
	RCK			MIN	20	31
	CCLR ↑ before CCK ↑				20	25
t <sub>su</sub>	CCK ↑ before RCK ↑			MIN	40	25
	t <sub>PLH</sub>	CCK ↑	RCO	MAX	22	45
	t <sub>PHL</sub>	CCLR ↓	RCO	MAX	30	45
t <sub>PLH</sub>	CCLR ↓			MAX	45	39
	RCK ↑				18	42
	RCK ↑			MAX	33	42
	Q					
t <sub>PZH</sub>	OE ↓	Q		MAX	38	37
	OE ↓	Q			45	37
	OE ↓	Q	MAX	MAX	30	37
	OE ↓	Q			38	37

UNIT f<sub>max</sub> : MHz, other : ns

## 8-BIT BINARY COUNTERS WITH INPUT REGISTERS

- Parallel Register Inputs
- Counter Has Directly Overriding Load and Clear
- Accurate Counter Frequency: DC to 20MHz

Logic Diagram



## ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	LS	UNIT
I <sub>CC</sub>	MAX	60	mA
I <sub>OH</sub>	MAX	-1	mA
I <sub>OL</sub>	MAX	16	mA

## TIMING REQUIREMENTS AND SWITCHING CHARACTERISTICS

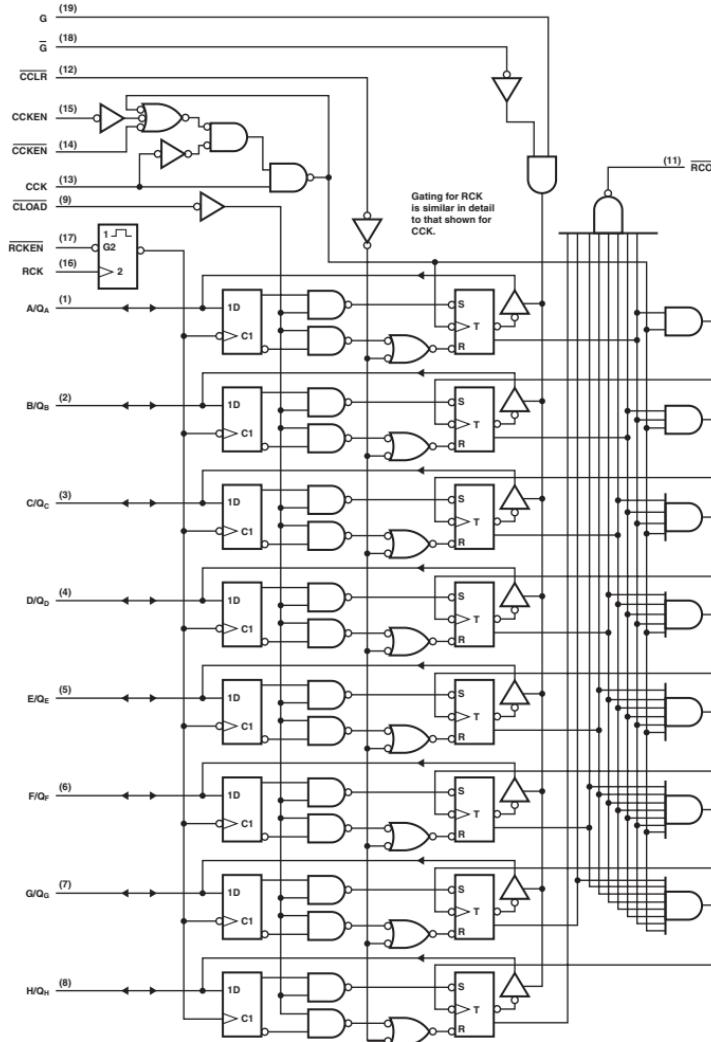
PARAMETER	INPUT	OUTPUT	MAX or MIN	LS
f <sub>max</sub>	CCK	$\overline{RCO}$	MIN	20
t <sub>w</sub>	CCK	$\overline{RCO}$	MIN	25
	$\overline{CCLR}$			20
	RCK			20
	$\overline{CLOAD}$			40
t <sub>su</sub>	$\overline{CCLR} \uparrow$ before CCK $\uparrow$	$\overline{RCO}$	MIN	20
	$\overline{CLOAD} \uparrow$ before CCK $\uparrow$			20
	RCK $\uparrow$ before $\overline{CLOAD} \uparrow$			30
	A to H before RCK			20
			MIN	0
t <sub>PLH</sub>	CCK $\uparrow$	$\overline{RCO}$	MAX	23
t <sub>PHL</sub>				30
t <sub>PLH</sub>	$\overline{CLOAD} \downarrow$	$\overline{RCO}$	MAX	47
t <sub>PHL</sub>				17
t <sub>PLH</sub>	$\overline{CCLR} \downarrow$	$\overline{RCO}$	MAX	45
t <sub>PLH</sub>				53
t <sub>PHL</sub>	RCK $\uparrow$	$\overline{RCO Q}$	MAX	45

UNIT f<sub>max</sub> : MHz, other : ns

## 8-BIT BINARY COUNTERS WITH INPUT REGISTERS

- Parallel 3-State I/O: Register Inputs/Counter Outputs
  - Counter Has Directly Overriding Load and Clear
  - Accurate Counter Frequency: DC to 20MHz
  - 74ACT11xxx: Product Available in Reduced-Noise Advanced CMOS (11000 Series)

## Logic Diagram



## ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	LS	ACT 11	UNIT
$I_{CC}$	MAX	85	0.08	mA
	$\bar{RCO}$	MAX	-1	-24 mA
$I_{OH}$	$Q$	MAX	-2.6	-24 mA
	$\bar{RCO}$	MAX	16	24 mA
$I_{OL}$	$Q$	MAX	24	24 mA

## TIMING REQUIREMENTS AND SWITCHING CHARACTERISTICS

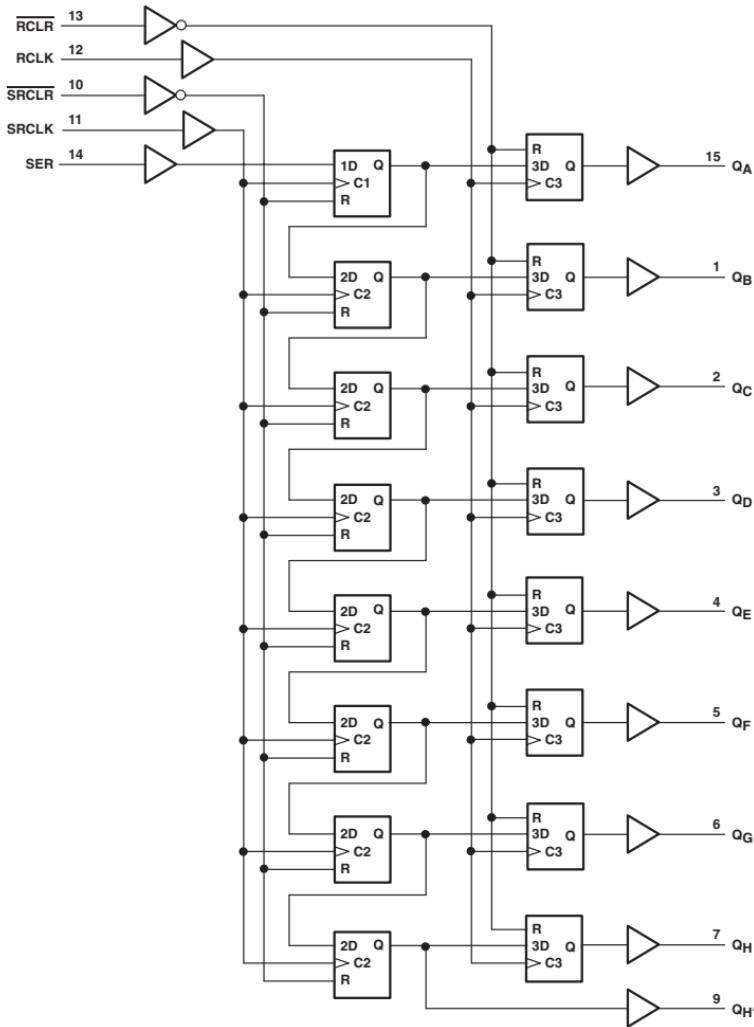
PARAMETER	INPUT	OUTPUT	MAX or MIN	LS	ACT 11
$t_{max}$	CCK	$\bar{RCO}$	MIN	20	52
$t_{W}$	CCK		MIN	25	9.6
	$\bar{CCLR}$			20	7.6
	RCK			20	5.8
	$\bar{CLOAD}$			40	6.2
$t_{SU}$	$\bar{CCLR} \uparrow$ before CCK $\uparrow$		MIN	20	1.2
	$\bar{CLOAD} \uparrow$ before CCK $\uparrow$			20	5.1
	RCK $\uparrow$ before $\bar{CLOAD} \uparrow$			30	7.4
	A to H before RCK			20	2.4
			MIN	0	0.8
$t_{PHL}$	CCK $\uparrow$	Q	MAX	21	15.1
$t_{PLH}$				39	15
$t_{PLH}$	$\bar{CLOAD} \downarrow$	Q	MAX	51	19.1
$t_{PHL}$				42	21.7
$t_{PHL}$	$\bar{CCLR} \downarrow$	Q	MAX	38	16

UNIT fmax : MHz, other : ns

## 8-BIT SHIFT REGISTERS WITH OUTPUT REGISTERS

- 8-Bit Serial-In, Parallel-Out Shift Registers with Storage
- Independent Direct Overriding Clears on Shift and Storage Registers
- Independent Clocks for Shift and Storage Registers
- Guaranteed Shift Frequency: DC to 20MHz

Logic Diagram



FUNCTION TABLE

INPUTS					FUNCTION					
SER	SRCLK	SRCLR	RCLK	RCLR						
X	X	L	X	X	Shift register is cleared.					
L	↑	H	X	X	First stage of shift register goes low. Other stages store the data of previous stage, respectively.					
H	↑	H	X	X	First stage of shift register goes high. Other stages store the data of previous stage, respectively.					
L	↓	H	X	X	Shift register state is not changed.					
X	X	X	X	L	Storage register is cleared.					
X	X	X	↑	H	Shift register data is stored in the storage register.					
X	X	X	↓	H	Storage register state is not changed.					

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER		MAX or MIN	LS	SN74 HC	AHC	AHCT	LV 3V	LV 5V	UNIT
Icc	MAX	65	0.08	0.04	0.02	-	0.02	mA	
	QH'	MAX	-1	-4	-4	-4	-6	-12	mA
Ioh	Q	MAX	-2.6	-6	-8	-8	-6	-12	mA
	QH'	MAX	16	4	4	4	6	12	mA
Iol	QA to QH	MAX	24	6	8	8	6	12	mA

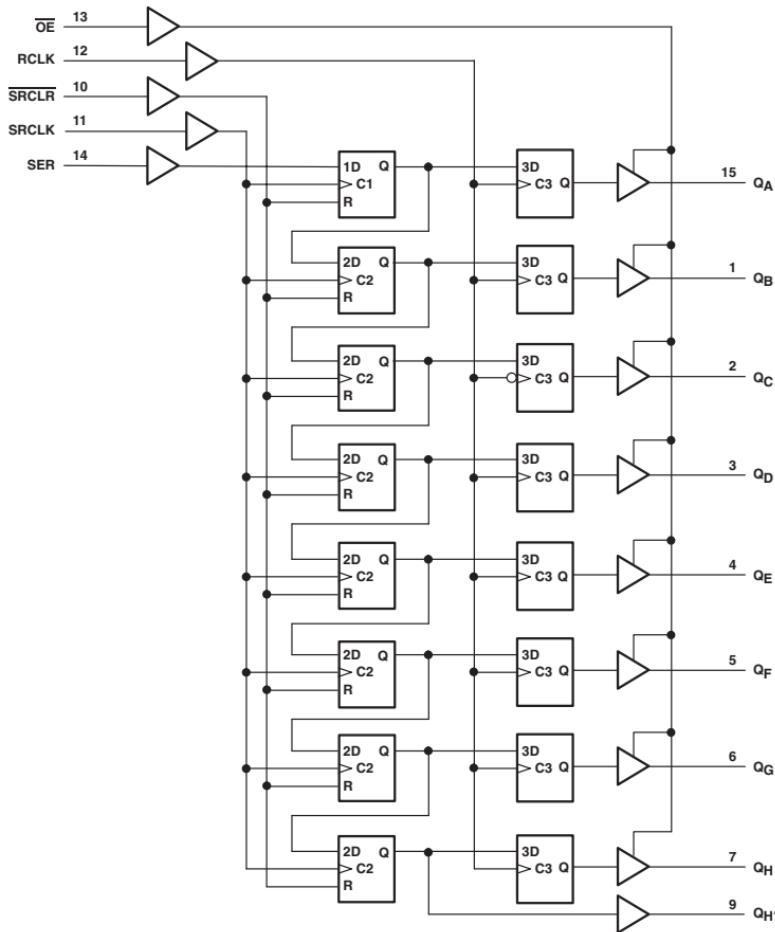
TIMING REQUIREMENTS AND SWITCHING CHARACTERISTICS

PARAMETER		INPUT	OUTPUT	MAX or MIN	LS	SN74 HC	AHC	AHCT	LV 3V	LV 5V
tw	SRCK				MIN	25	20	5	5.5	5.5
	RCK					20	20	5	5.5	5
tsu	SRCLR ↑ to SRCK ↑				MIN	20	10	3.3	3.3	4.8
	SER to SRCK ↑					20	22	3	3	3.5
	SRCK ↑ to RCK ↑					40	22	5	5	5
	SRCLR ↓ to RCK ↑					40	13	5	9	5
	RCLR ↑ to RCK ↑					20	5	3.7	3.8	5.3
	QA to QH					0	5	2	2	1.5
th					MIN	18	37	9.1	9.1	12.4
tpHL		SRCK ↑	QH'	MAX		23	37	10.1	10.1	13.9
tpHL		RCK ↑	QA to QH	MAX		18	37	8.3	8.3	11.1
tpHL		SRCLR ↓	QH'	MAX		30	37	9.7	9.7	13.1
tpHL		RCLR ↓	QA to QH	MAX		33	37	10.1	10.1	10.1
tpHL						57	31	10.7	10.7	14.4
UNIT: ns										

## 8-BIT SHIFT REGISTERS WITH 3-STATE OUTPUT REGISTERS

- 8-Bit Serial-In, Parallel-Out Shift Registers with Storage
- 3-State Outputs
- Shift Register Has Direct Clear
- Accurate Shift Frequency: DC to 20MHz

Logic Diagram



FUNCTION TABLE

INPUTS					FUNCTION					
SER	SRCLK	SRCLR	RCLK	OE						
X	X	X	X	H	Outputs Q <sub>A</sub> -Q <sub>H</sub> are disabled.					
X	X	X	X	L	Outputs Q <sub>A</sub> -Q <sub>H</sub> are enabled.					
X	X	L	X	X	Shift register is cleared.					
L	↑	H	X	X	First stage of the shift register goes low. Other stages store the data of previous stage, respectively.					
H	↑	H	X	X	First stage of the shift register goes high. Other stages store the data of previous stage, respectively.					
X	↓	H	X	X	Shift-register state is not changed.					
X	X	X	↑	X	Shift-register data is stored in the storage register.					
X	X	X	↓	X	Storage-register state is not changed.					

## ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER		MAX or MIN	LS	SN74 HC	CD74 HC	AHC	AHCT	LV 3V	LV 5V	UNIT
I <sub>CC</sub>	MAX	65	0.08	0.16	0.04	0.04	-	0.02	mA	
	QH'	MAX	-1	-4	-4	-8	-8	-8	-16	mA
	QA to QH	MAX	-26	-6	-6	-8	-8	-8	-16	mA
	QH'	MAX	16	4	4	8	8	8	16	mA
I <sub>OL</sub>	QA to QH	MAX	24	6	6	8	8	8	16	mA

## TIMING REQUIREMENTS AND SWITCHING CHARACTERISTICS

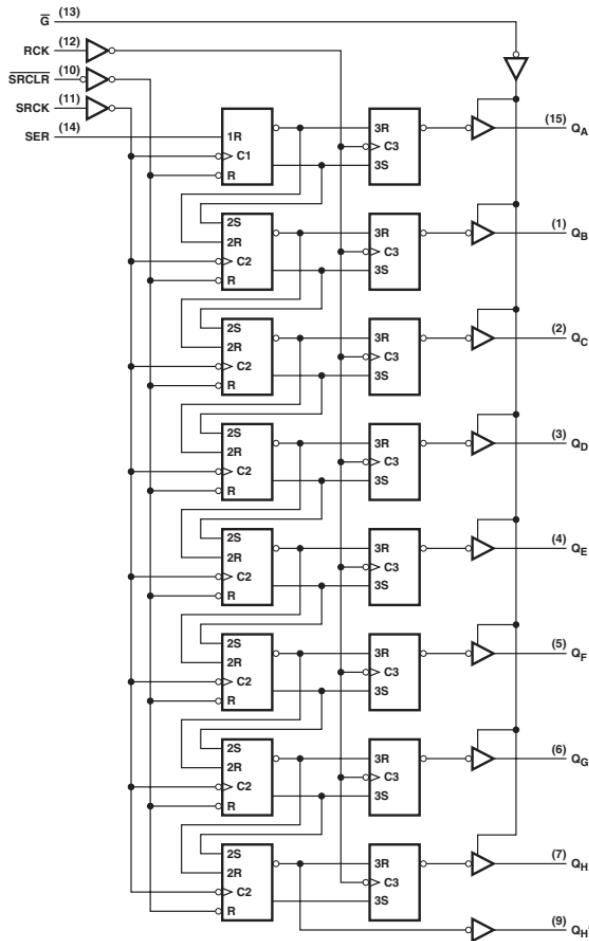
PARAMETER		INPUT	OUTPUT	MAX or MIN	LS	SN74 HC	CD74 HC	AHC	AHCT	LV 3V	LV 5V
t <sub>w</sub>	SRCK			MIN	25	20	20	5	5.5	5.5	5
	RCK				20	20	20	5	5.5	5.5	5
t <sub>su</sub>	SRCLR ↑ to SRCK ↑			MIN	20	12	12	2.5	3.8	3	2.5
	SER to SRCK ↑				20	25	25	3	3	3.5	3
	SRCK ↑ to RCK ↑				40	19	19	5	5	8.5	5
	SRCLR ↓ to RCK ↑				40	13	13	5	5	9	5
					MIN	0	0	0	2	2	1.5
t <sub>th</sub>	IPHL	SRCK ↑	QH'	MAX	18	40	48	11.4	11.4	18.5	11.4
	IPHL				25	40	48	11.4	11.4	18.5	11.4
t <sub>phl</sub>	IPHL	RCK ↑	QA to QH	MAX	18	37	45	10.5	10.5	17	10.5
	IPHL				35	37	45	10.5	10.5	17	10.5
t <sub>phl</sub>	IPHL	SRCLR ↓	QH'	MAX	35	44	44	11.1	11.1	17.2	11.1

UNIT: ns

## 8-BIT SHIFT REGISTERS WITH OUTPUT LATCHES

- 8-Bit Serial-In, Parallel-Out Shift Registers with Storage
- Open-Collector Parallel Outputs
- Shift Register Has Direct Clear
- Accurate Shift Frequency: DC to 20MHz

Logic Diagram



## ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER		MAX or MIN	LS	UNIT
I <sub>CC</sub>		MAX	55	mA
I <sub>OH</sub>	QH'	MAX	16	mA
	Q	MAX	24	mA
I <sub>OL</sub>	QH'	MAX	-1	mA
V <sub>OH</sub>	QA to QH	MAX	5.5	V

## TIMING REQUIREMENTS AND SWITCHING CHARACTERISTICS

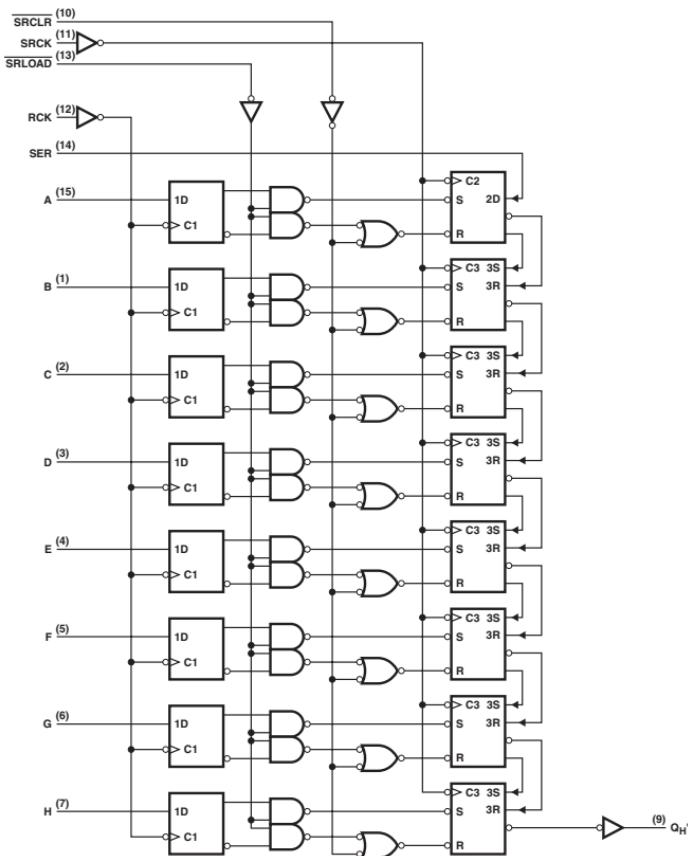
PARAMETER	INPUT	OUTPUT	MAX or MIN	LS
t <sub>W</sub>	SRCK RCK		MIN	25 20
t <sub>SU</sub>	SRCLR ↑ to SRCK ↑			20
	SER to SRCK ↑			20
	SRCK ↑ to RCK ↑			40
	SRCLR ↓ to RCK ↑			40
t <sub>H</sub>			MIN	0
t <sub>PLH</sub>	SRCK ↑	QH'	MAX	21
t <sub>PLH</sub>				30
t <sub>PLH</sub>	RCK ↑	QA to QH	MAX	42
t <sub>PLH</sub>	SRCLR ↓	QH'	MAX	35

UNIT: ns

## SERIAL-OUT SHIFT REGISTERS WITH INPUT LATCHES

- 8-Bit Parallel Storage Registers Inputs
- Shift Register Has Direct Overriding Load and Clear
- Accurate Shift Frequency: DC to 20MHz

Logic Diagram (SN74LS)



## ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	LS	CD74 HC	CD74 HCT	UNIT
I <sub>CC</sub>	MAX	53	0.16	0.16	mA
I <sub>OH</sub>	MAX	-1	-4	-4	mA
I <sub>OL</sub>	MAX	16	4	4	mA

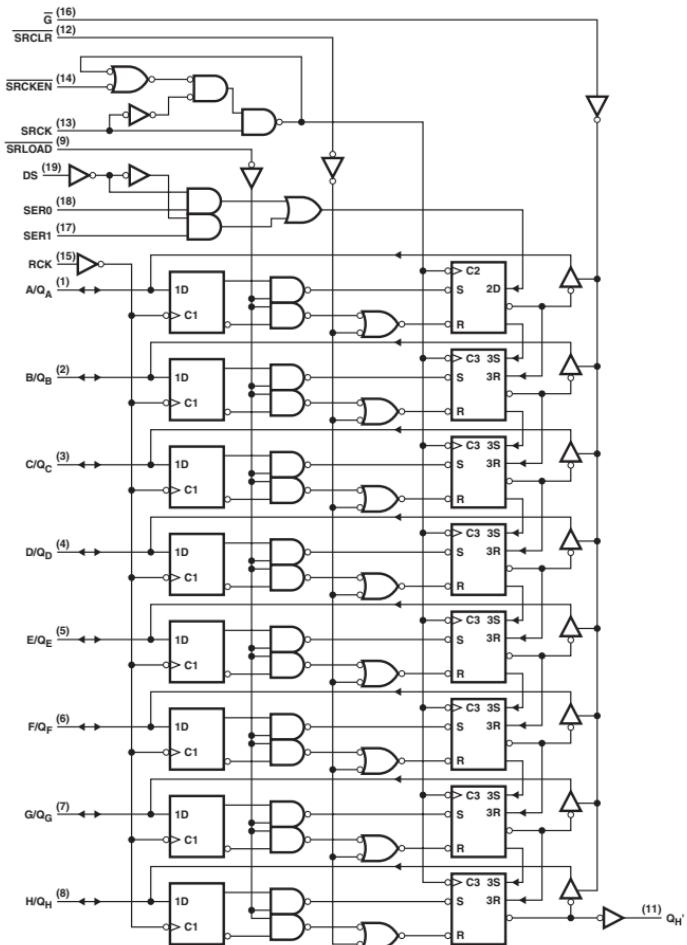
## TIMING REQUIREMENTS AND SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	LS	CD74 HC	CD74 HCT
f <sub>max</sub>	SRCK	Q	MIN	20	-	-
	SRCK	QH'	MIN	20	-	-
	SH <sub>CP</sub>		MIN	-	20	16
t <sub>w</sub>	SRCK high		MIN	15	-	-
	SRCK low		MIN	35	-	-
	RCK		MIN	20	-	-
	SRCLR		MIN	20	-	-
	SRLOAD		MIN	40	-	-
	SH <sub>CP</sub>		MIN	-	20	30
	ST <sub>CP</sub>		MIN	-	15	20
	MR		MIN	-	20	27
	PL		MIN	-	18	24
t <sub>su</sub>	Data before RCK ↑		MIN	20	-	-
	SRCLR inactive before SRCK ↑		MIN	25	-	-
	SRLOAD inactive before SRCK ↑		MIN	30	-	-
	RCK ↑ before SRLOAD ↑		MIN	40	-	-
	SER before SRCK ↑		MIN	20	-	-
	ST <sub>CP</sub> to SH <sub>CP</sub>		MIN	-	30	36
	D <sub>s</sub> to SH <sub>CP</sub>		MIN	-	15	15
	D <sub>n</sub> to ST <sub>CP</sub>		MIN	-	15	15
	LS597 only			0	-	-
t <sub>h</sub>	ST <sub>CP</sub> to SH <sub>CP</sub>		MIN	-	0	0
	D <sub>s</sub> to SH <sub>CP</sub>			-	3	3
	D <sub>n</sub> to ST <sub>CP</sub>			-	3	3
	SRCK ↑	QH'		MAX	23	-
t <sub>PLH</sub>	SRCK ↑	QH'			23	-
t <sub>PLH</sub>	SRLOAD ↓	QH'	MAX		57	-
t <sub>PLH</sub>	SRLOAD ↓	QH'			44	-
t <sub>PLH</sub>	RCK ↑	QH'	MAX		36	-
t <sub>PLH</sub>	RCK ↑	QH'			60	-
t <sub>PLH</sub>	RCK ↑	QH'	MAX		48	-
t <sub>PLH</sub>	SH <sub>CP</sub>	Q7	MAX		-	53
t <sub>PLH</sub>	SH <sub>CP</sub>	Q7			-	57
t <sub>PLH</sub>	PL	Q7	MAX		-	60
t <sub>PLH</sub>	PL	Q7			-	72
t <sub>PLH</sub>	ST <sub>CP</sub>	Q7	MAX		-	60
t <sub>PLH</sub>	ST <sub>CP</sub>	Q7			-	72
t <sub>PLH</sub>	MR	Q7	MAX		-	84
t <sub>PLH</sub>	MR	Q7			-	72
t <sub>PLH</sub>	MR	Q7	MAX		-	53
t <sub>PLH</sub>	MR	Q7			-	66

UNIT f<sub>max</sub> : MHz, other : ns

## 8-BIT SHIFT REGISTERS WITH INPUT LATCHES

Logic Diagram



## ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	LS	UNIT
I <sub>CC</sub>	MAX	85	mA
I <sub>OH</sub>	MAX	-2.6	mA
I <sub>OL</sub>	MAX	24	mA

## TIMING REQUIREMENTS AND SWITCHING CHARACTERISTICS

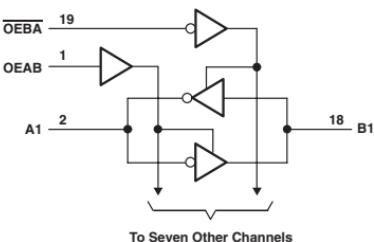
PARAMETER	INPUT	OUTPUT	MAX or MIN	LS
f <sub>max</sub>	SRCK	Q	MIN	20
	SRCK	QHB	MIN	20
t <sub>w</sub>	SRCK high		MIN	15
	SRCK low		MIN	35
	RCK		MIN	20
	SRCLR		MIN	20
	SRLOAD		MIN	40
	Data before RCK ↑		MIN	20
t <sub>su</sub>	DS before RCK ↑		MIN	30
	SRCKEN low before SRCK ↑		MIN	20
	SRCLR inactive before SRCK ↑		MIN	25
	SRLOAD inactive before SRCK ↑		MIN	30
	RCK ↑ before SRLOAD ↑		MIN	40
	SER before SRCK ↑		MIN	20
t <sub>h</sub>			MIN	0
t <sub>PLH</sub>	SRCK ↑	QHB	MAX	17
				23
t <sub>PHL</sub>	SRLOAD ↓	QHB	MAX	42
				39
t <sub>PLH</sub>	SRCLR ↓	QHB	MAX	27
				48
t <sub>PLH</sub>	RCK ↑	QHB	MAX	36
				18
t <sub>PLH</sub>	SHCP	Q7	MAX	28

UNIT f<sub>max</sub> : MHz, other : ns

## OCTAL BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

- Local Bus-Latch Capability
- 3-State Inverting Outputs
- 74ACT11xxx: Product Available in Reduced-Noise Advanced CMOS (11000 Series)
- 74ACT11xxx: Product Available in Reduced-Noise Advanced CMOS (11000 Series)

Logic Diagram



FUNCTION TABLE

ENABLE INPUTS		OPERATION
OEBA	OEAB	
L	L	B data to Abus
H	H	Ā data to B bus
H	L	Isolation
L	H	B data to Abus Ā data to B bus

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	LS	ALS	ALS-1	AS	SN74 HC	SN74 BCT	ABT	AC 11	ACT 11	UNIT
I <sub>CCZ</sub>	MAX	95	47	47	77	0.08	10	0.25	0.08	0.008	mA
I <sub>CCL</sub>	MAX	90	44	44	122	0.08	84	30	0.08	0.008	mA
I <sub>OH</sub> (A port)	MAX	-15	-15	-15	-15	-6	-3	-32	-24	-24	mA
I <sub>OH</sub> (B port)	MAX	-15	-15	-15	-15	-6	-15	-32	-24	-24	mA
I <sub>OL</sub> (A port)	MAX	24	24	48	64	6	24	64	24	24	mA
I <sub>OL</sub> (B port)	MAX	24	24	48	64	6	64	64	24	24	mA

SWITCHING CHARACTERISTICS

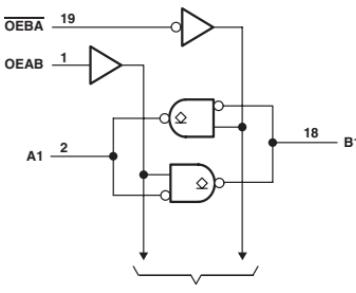
PARAMETER	INPUT	OUTPUT	MAX or MIN	LS	ALS	ALS-1	AS	SN74 HC	SN74 BCT	ABT	AC 11	ACT 11
I <sub>PLH</sub>	A	B	MAX	10	10	10	7	26	5.8	4.8	7.4	9.4
				15	10	10	6	26	3.6	4.8	7.1	8.6
I <sub>PHL</sub>	B	A	MAX	10	10	10	7	26	6.9	4.8	7.4	9.4
				15	10	10	6	26	3.9	4.8	7.1	8.6
I <sub>PZH</sub>	OEBA	A	MAX	40	17	17	8	53	10.6	5.5	8.9	10.3
				40	25	25	9	53	11.1	7.1	8.5	10.1
I <sub>PHZ</sub>	OEBA	A	MAX	25	12	12	6	38	10	7	8.1	10.4
				25	18	18	12	38	7.8	5.8	8.7	10.9
I <sub>PZL</sub>	OEAB	B	MAX	40	18	18	8	53	7.4	6.8	8.8	11.3
				40	25	25	9	53	9	6.4	8.8	11
I <sub>PHZ</sub>	OEAB	B	MAX	25	12	12	6	38	8.1	6.5	8.2	9.4
				25	18	18	13	38	5.9	5.6	8.6	9.6

UNIT: ns

## OCTAL BUS TRANSCEIVERS

- Local Bus-Latch Capability
- Open-Collector True Outputs
- Schmitt-Triggered Inputs (SN74LS621)

Logic Diagram



FUNCTION TABLE

ENABLE INPUTS		OPERATION
OEBA	OEAB	
L	L	B data to Abus
H	H	A data to B bus
H	L	Isolation
L	H	B data to Abus A data to B bus

## ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	LS	ALS	ALS A-1	AS	UNIT
I <sub>CC</sub>	MAX	90	48	48	189	mA
V <sub>DH</sub>	MAX	5.5	5.5	5.5	5.5	V
I <sub>OL</sub>	MAX	24	24	48	64	mA

## SWITCHING CHARACTERISTICS

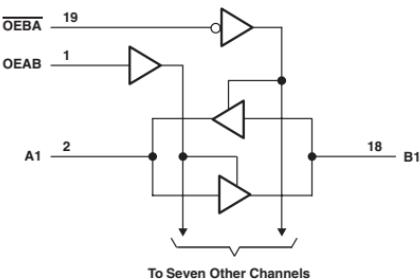
PARAMETER	INPUT	OUTPUT	MAX or MIN	LS	ALS	ALS A-1	AS
I <sub>PLH</sub>	A	B	MAX	25	33	33	24
I <sub>PHL</sub>				25	20	20	21
I <sub>PLH</sub>	B	A	MAX	25	33	33	7.5
I <sub>PHL</sub>				25	20	20	7.5
I <sub>PLH</sub>	OEBA	A	MAX	40	39	39	21
I <sub>PHL</sub>				50	35	35	9
I <sub>PLH</sub>	OEAB	B	MAX	40	39	39	22
I <sub>PHL</sub>				50	35	35	10

UNIT: ns

## OCTAL BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

- Local Bus-Latch Capability
- 3-State True Outputs
- Schmitt-Triggered Inputs (SN74LS623)
- 74AC11xx: Product Available in Reduced-Noise Advanced CMOS (11000 Series)
- 74ACT11xx: Product Available in Reduced-Noise Advanced CMOS (11000 Series)

## Logic Diagram (SN74)



### FUNCTION TABLE (SN74)

ENABLE INPUTS		OPERATION	
OEBA	OEAB		
L	L	B data to Abus	
H	H	A data to B bus	
H	L	Isolation	
L	H	B data to Abus	A data to B bus

### ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	LS	ALS	AS	F	SN74 HC	SN74 HCT	SN74 BCT	ABT	AC 11	ACT 11	CD74 AC	CD74 ACT	UNIT
I <sub>CCZ</sub>	MAX	95	55	116	130	0.08	0.08	11	0.25	0.08	0.04	0.16	0.16	mA
I <sub>CCL</sub>	MAX	90	50	189	140	0.08	0.08	92	30	0.08	0.04	0.16	0.16	mA
I <sub>OH</sub> (A port)	MAX	-15	-15	-15	-3	-6	-6	-3	-32	-24	-24	-24	-24	mA
I <sub>OH</sub> (B port)	MAX	-15	-15	-15	-15	-6	-6	-15	-32	-24	-24	-24	-24	mA
I <sub>OL</sub> (A port)	MAX	24	24	64	24	6	6	24	64	24	24	24	24	mA
I <sub>OL</sub> (B port)	MAX	24	24	64	64	6	6	64	64	24	24	24	24	mA

### SWITCHING CHARACTERISTICS

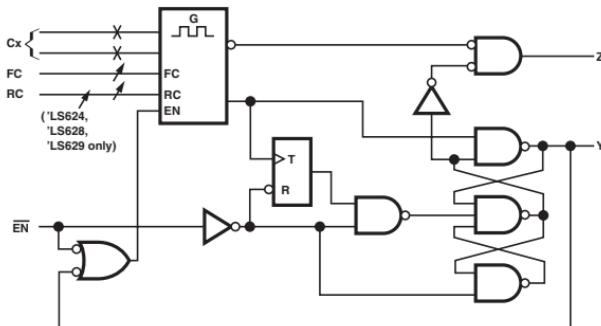
PARAMETER	INPUT	OUTPUT	MAX or MIN	LS	ALS	AS	F	SN74 HC	SN74 HCT	SN74 BCT	ABT	AC 11	ACT 11	CD74 AC	CD74 ACT
I <sub>PLH</sub>	A	B	MAX	15	13	9	6.5	26	28	5.2	4.6	7.8	8.5	9.6	10.6
				15	11	8	7.5	26	28	7.4	4.6	7.1	7.9	9.6	10.6
I <sub>PHL</sub>	B	A	MAX	15	13	9	6.5	26	28	6.7	4.6	7.8	8.5	9.6	10.6
				15	11	8.5	7.5	26	28	8	4.6	7.1	7.9	9.6	10.6
I <sub>PZH</sub>	OEBA	A	MAX	40	22	11	12	53	53	10.6	7.5	9	9.7	13.4	14.4
				40	22	10	10	53	53	10.7	7.5	9.1	10	13.4	14.4
I <sub>PZL</sub>	OEBA	A	MAX	25	16	7.5	7.5	38	38	9.8	7.5	8.3	10.9	13.4	14.4
				25	19	11.5	7	38	38	7.8	7.5	8.8	11.5	13.4	14.4
I <sub>PZH</sub>	OEAB	B	MAX	40	22	11.5	11.5	53	53	7.6	7.5	9.2	10.7	13.4	14.4
				40	22	11	9.5	53	53	8.9	7.5	9.4	10.9	13.4	14.4
I <sub>PZL</sub>	OEAB	B	MAX	25	16	7	10	38	38	7.7	7.5	8.3	9.5	13.4	14.4
				25	19	9	10	38	38	7.1	7.5	8.8	10	13.4	14.4

UNIT: ns

## VOLTAGE-CONTROLLED OSCILLATORS

- This Voltage Oscillators (VCOs) is Improved Versions of The Original VCO Family: SN74124, 324, 325, 326, 327
- Separate Supply Voltage Pins for Isolation of Frequency Control Inputs and Oscillators from Outputs Circuitry
- Highly Stable Operation over Specified Temperature and / or Supply Voltage Ranges

**Logic Diagram**



### ELECTRICAL CHARACTERISTICS AND RECOMMENDED OP

PARAMETER	MAX or MIN	LS	UNIT
I <sub>cc</sub>	MAX	35	mA
I <sub>OL</sub>	MAX	24	mA
I <sub>OH</sub>	MAX	-1.2	mA

### TIMING REQUIREMENTS AND SWITCHING CHARACTERIST

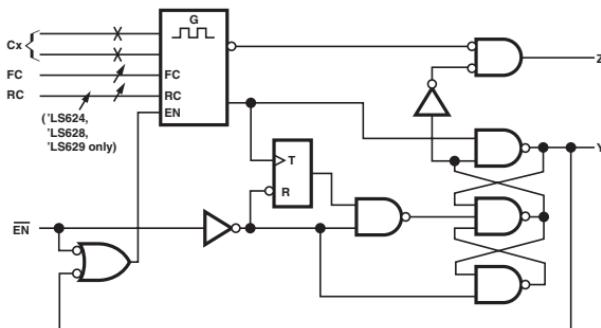
PARAMETER	MAX or MIN	LS
f <sub>o</sub>	MAX	25

UNIT: MHz

## VOLTAGE-CONTROLLED OSCILLATORS

- This Voltage Oscillators (VCOs) is Improved Versions of The Original VCO Family: SN74124, 324, 325, 326, 327
- Separate Supply Voltage Pins for Isolation of Frequency Control Inputs and Oscillators from Outputs Circuitry
- Highly Stable Operation over Specified Temperature and / or Supply Voltage Ranges
- Two External Pins Can Offer More Precise Temperature Compensation

**Logic Diagram**



### ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	LS	UNIT
I <sub>CC</sub>	MAX	35	mA
I <sub>OH</sub>	MAX	-1.2	mA
I <sub>OL</sub>	MAX	24	mA

### TIMING REQUIREMENTS AND SWITCHING CHARACTERISTIC

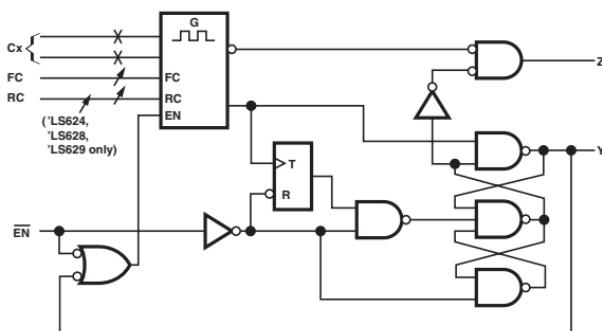
PARAMETER	MAX or MIN	LS
f <sub>o</sub>	MAX	25

UNIT: MHz

## DUAL VOLTAGE-CONTROLLED OSCILLATORS

- This Voltage Oscillators (VCOs) is Improved Versions of The Original VCO Family: SN74124, 324, 325, 326, 327
- Separate Supply Voltage Pins for Isolation of Frequency Control Inputs and Oscillators from Outputs Circuitry
- Highly Stable Operation over Specified Temperature and / or Supply Voltage Ranges

Logic Diagram



## ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	LS	UNIT
I <sub>cc</sub>	MAX	55	mA
I <sub>oh</sub>	MAX	-1.2	mA
I <sub>ol</sub>	MAX	24	mA

## TIMING REQUIREMENTS AND SWITCHING CHARACTERISTICS

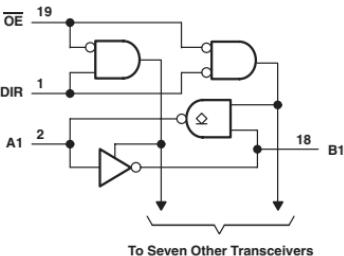
PARAMETER	MAX or MIN	LS
f <sub>o</sub>	MAX	25

UNIT: MHz

## OCTAL BUS TRANSCEIVERS

- Bidirectional Bus Transceivers
- Inverting Logic
- Outputs A-Bus: Open-Collector 3-State
- Schmitt-Triggered Inputs (SN74LS638)

Logic Diagram



FUNCTION TABLE

CONTROL INPUTS		OPERATION			
OE	DIR				
L	L	B data to A bus			
L	H	A data to B bus			
H	X	Isolation			

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	LS	ALS	ALS A-1	AS	UNIT
I <sub>CCZ</sub>	MAX	95	30	30	61	mA
I <sub>CCL</sub>	MAX	90	41	41	122	mA
I <sub>OH</sub> (B)	MAX	-15	-15	-15	-15	mA
V <sub>OH</sub> (A)	MAX	5.5	5.5	5.5	5.5	V
I <sub>OL</sub>	MAX	24	24	48	64	mA

SWITCHING CHARACTERISTICS

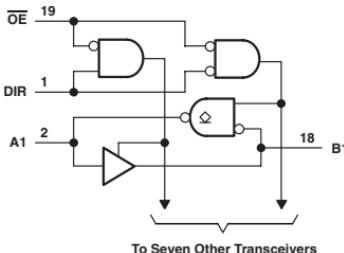
PARAMETER	INPUT	OUTPUT	MAX or MIN	LS	ALS	ALS A-1	AS
t <sub>PLH</sub>	A	B	MAX	10	12	12	7
				15	12	12	6.5
t <sub>PHL</sub>	B	A	MAX	25	25	25	20
				25	30	30	7
t <sub>PLH</sub>	OE	A	MAX	40	25	25	19
				60	45	45	9
t <sub>PZH</sub>	OE	B	MAX	40	20	20	8
				40	22	22	10
t <sub>PZL</sub>	OE	B	MAX	25	10	10	7
				25	15	15	10

UNIT: ns

## OCTAL BUS TRANSCEIVERS

- Bidirectional Bus Tranceivers
- True Logic
- Outputs A-Bus: Open-Collector 3-State
- Schmitt-Triggered Inputs (SN74LS638)

## Logic Diagram



FUNCTION TABLE

CONTROL INPUTS		OPERATION	
OE	DIR		
L	L	B data to A bus	
L	H	A data to B bus	
H	X	Isolation	

## ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	LS	ALS	ALS A-1	AS	UNIT
I <sub>CC2</sub>	MAX	95	54	54	100	mA
I <sub>CC1</sub>	MAX	90	50	50	154	mA
I <sub>OH</sub> (B)	MAX	-15	-15	-15	-15	mA
V <sub>OH</sub> (A)	MAX	5.5	5.5	5.5	5.5	V
I <sub>OL</sub>	MAX	24	24	48	64	mA

## SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	LS	ALS	ALS A-1	AS
t <sub>PLH</sub>	A	B	MAX	15	12	12	9.5
t <sub>PHL</sub>				15	12	12	9
t <sub>PLH</sub>	B	A	MAX	25	30	30	22
t <sub>PHL</sub>				25	22	22	9
t <sub>PLH</sub>	$\overline{OE}$	A	MAX	40	30	30	21.5
t <sub>PHL</sub>				50	35	35	11.5
t <sub>PZH</sub>	$\overline{OE}$	B	MAX	40	21	21	10.5
t <sub>PZL</sub>				40	25	25	10.5
t <sub>PHZ</sub>	$\overline{OE}$	B	MAX	25	10	10	7
t <sub>PZL</sub>				25	16	16	10.5

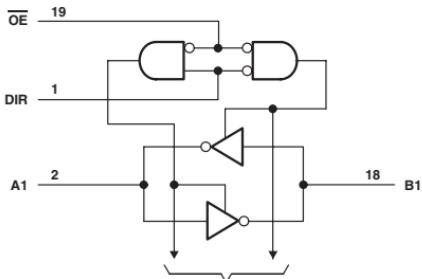
UNIT: ns

## OCTAL BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

- Bidirectional Bus Transceivers
- Inverting Logic
- 3-State Outputs
- Schmitt-Triggered Inputs (SN74LS640, 640-1)
- 74ACT11xxx: Product Available in Reduced-Noise Advanced CMOS (11000 Series)

FUNCTION TABLE (SN74)

CONTROL INPUTS		OPERATION	
OE	DIR		
L	L	$\bar{B}$ data to A bus	
L	H	$\bar{A}$ data to B bus	
H	X	Isolation	



### ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	LS	LS-1	ALS	ALS B-1	AS	SN74 HC	CD74 HC	SN74 HCT	CD74 HCT	SN74 BCT	ABT	ACT 11	UNIT
I <sub>CCZ</sub>	MAX	95	95	50	50	80	0.08	0.16	0.08	0.16	11	0.25	0.08	mA
I <sub>CCL</sub>	MAX	90	90	55	55	123	0.08	0.16	0.08	0.16	94	30	0.08	mA
I <sub>OH</sub> (A port)	MAX	-15	-15	-15	-15	-15	-6	-6	-6	-6	-3	-32	-24	mA
I <sub>OH</sub> (B port)	MAX	-15	-15	-15	-15	-15	-6	-6	-6	-6	-15	-32	-24	mA
I <sub>OL</sub> (A port)	MAX	24	48	24	48	64	6	6	6	6	24	64	24	mA
I <sub>OL</sub> (B port)	MAX	24	48	24	48	64	6	6	6	6	64	64	24	mA

### SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	LS	LS-1	ALS	ALS B-1	AS	SN74 HC	CD74 HC	SN74 HCT
t <sub>PLH</sub>	A	B	MAX	10	10	11	11	7	26	27	28
				15	15	10	10	6	26	27	28
t <sub>PHL</sub>	B	A	MAX	10	10	11	11	7	26	27	28
				15	15	10	10	6	26	27	28
t <sub>PZH</sub>	OE	A	MAX	40	40	21	21	8	58	45	58
				40	40	24	24	10	58	45	58
t <sub>PZL</sub>	OE	A	MAX	25	25	10	10	8	38	45	50
				25	25	15	15	13	38	45	50
t <sub>PZH</sub>	OE	B	MAX	40	40	21	21	8	58	45	58
				40	40	24	24	10	58	45	58
t <sub>PZL</sub>	OE	B	MAX	25	25	10	10	8	38	45	50
				25	25	15	15	13	38	45	50

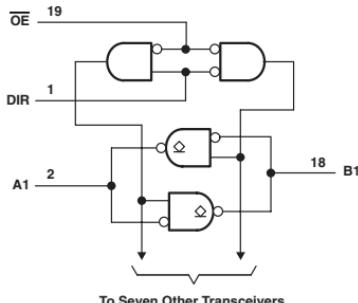
PARAMETER	INPUT	OUTPUT	MAX or MIN	CD74 HCT	SN74 BCT	ABT	ACT 11
t <sub>PLH</sub>	A	B	MAX	33	6.5	4.9	10.5
				33	3.7	4.9	9.5
t <sub>PHL</sub>	B	A	MAX	33	6.5	4.9	10.5
				33	3.7	4.9	9.5
t <sub>PZH</sub>	OE	A	MAX	45	10.2	5.8	13.4
				45	10.7	7.3	13.6
t <sub>PZL</sub>	OE	A	MAX	45	10.2	6.8	13.9
				45	7.8	5.5	14.2
t <sub>PZH</sub>	OE	B	MAX	45	10.2	5.8	13.4
				45	10.7	7.3	13.6
t <sub>PZL</sub>	OE	B	MAX	45	10.2	6.8	13.9
				45	7.8	5.5	14.2

UNIT: ns

## OCTAL BUS TRANSCEIVERS

- Bidirectional Bus Transceivers
- True Logic
- 3-State Outputs
- Schmitt-Triggered Inputs (SN74LS641)

## Logic Diagram



FUNCTION TABLE

CONTROL INPUTS		OPERATION	
$\bar{G}$	DIR		
L	L	B data to A bus	
L	H	A data to B bus	
H	X	Isolation	

## ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	LS	LS-1	ALS	ALS A-1	AS	UNIT
$I_{CC2}$	MAX	95	95	-	-	-	mA
$I_{CCL}$	MAX	90	90	47	47	136	mA
$V_{OH}$	MAX	5.5	5.5	5.5	5.5	5.5	V
$I_{OL}$	MAX	24	48	24	48	64	mA

## SWITCHING CHARACTERISTICS

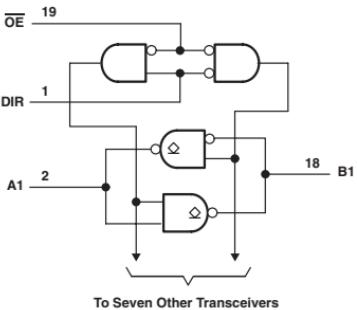
PARAMETER	INPUT	OUTPUT	MAX or MIN	LS	LS-1	ALS	ALS A-1	AS
$t_{PLH}$	A	B	MAX	25	25	25	25	21
				25	25	18	18	7.5
$t_{PHL}$	B	A	MAX	25	25	25	25	21
				25	25	18	18	7.5
$t_{PLH}$	$\bar{OE}$	A,B	MAX	40	40	30	30	21
				50	50	30	30	9
$t_{PHL}$	DIR	A,B	MAX	40	40	32	32	22
				50	50	32	32	10

UNIT: ns

## OCTAL BUS TRANSCEIVERS WITH OPEN-COLLECTOR OUTPUTS

- Bidirectional Bus Tranceivers
- Inverting Logic
- 3-State Outputs
- Schmitt-Triggered Inputs (SN74LS642)

Logic Diagram



FUNCTION TABLE

CONTROL INPUTS		OPERATION	
OE	DIR		
L	L	$\bar{B}$ data to A bus	
L	H	A data to B bus	
H	X	Isolation	

### ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	LS	LS-1	ALS	ALS A-1	AS	UNIT
$I_{CCZ}$	MAX	95	95	-	-	-	mA
$I_{CCL}$	MAX	90	90	28	28	104	mA
$V_{OH}$	MAX	5.5	5.5	5.5	5.5	5.5	V
$I_{OL}$	MAX	24	48	24	48	64	mA

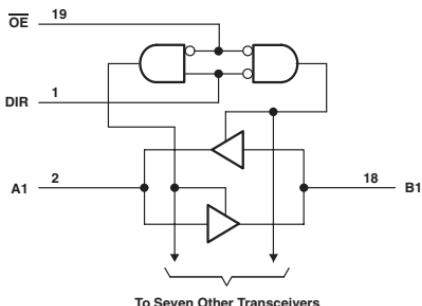
### SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	LS	LS-1	ALS	ALS A-1	AS
$t_{PLH}$	A	B	MAX	25	25	30	30	24
				25	25	22	22	7.5
$t_{PHL}$	B	A	MAX	25	25	30	30	24
				25	25	22	22	7.5
$t_{PLH}$	$\bar{OE}, \bar{DIR}$	A	MAX	40	40	30	30	23.5
				60	60	38	38	11.5
$t_{PHL}$	$\bar{OE}, \bar{DIR}$	B	MAX	40	40	30	30	23.5
				60	60	38	38	11.5

UNIT: ns

## OCTAL BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

- Bidirectional Bus Tranceivers
- True Logic
- 3-State Outputs
- Schmitt-Triggered Inputs (SN74LS645, 645-1)



### FUNCTION TABLE

CONTROL INPUTS		OPERATION
OE	DIR	
L	L	B data to A bus
L	H	$\bar{A}$ data to B bus
H	X	Isolation

### ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	LS	LS-1	ALS	ALS A-1	AS	SN74 HC	SN74 HCT	UNIT
I <sub>CCZ</sub>	MAX	95	95	58	58	123	0.08	0.08	mA
I <sub>CCL</sub>	MAX	90	90	55	55	149	0.08	0.08	mA
I <sub>OH</sub>	MAX	-15	-15	-15	-15	-15	-6	-6	mA
I <sub>OL</sub>	MAX	24	48	24	48	64	6	6	mA

### SWITCHING CHARACTERISTICS

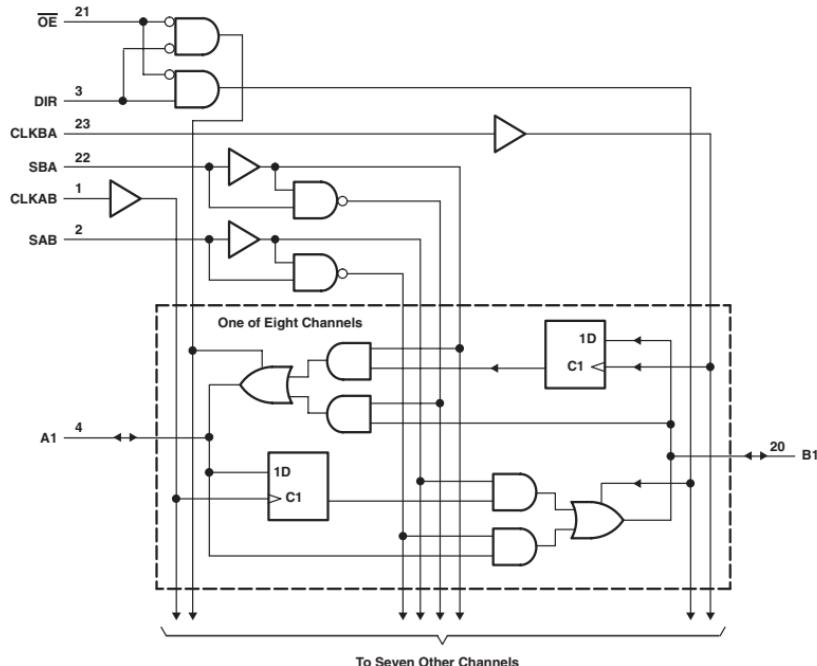
PARAMETER	INPUT	OUTPUT	MAX or MIN	LS	LS-1	ALS	ALS A-1	AS	SN74 HC	SN74 HCT
I <sub>PLH</sub>	A	B	MAX	15	15	10	10	9.5	26	28
I <sub>PLH</sub>				15	15	10	10	9	26	28
I <sub>PLH</sub>	B	A	MAX	15	15	10	10	9.5	26	28
I <sub>PLH</sub>				15	15	10	10	9	26	28
I <sub>PZH</sub>	$\overline{OE}$	A	MAX	40	40	20	20	11	58	58
I <sub>PZH</sub>				40	40	20	20	10	58	58
I <sub>PZH</sub>	$\overline{OE}$	A	MAX	25	25	10	10	7	50	50
I <sub>PZH</sub>				25	25	15	15	12	50	50
I <sub>PZL</sub>	$\overline{OE}$	B	MAX	40	40	20	20	11	58	58
I <sub>PZL</sub>				40	40	20	20	10	58	58
I <sub>PZH</sub>	$\overline{OE}$	B	MAX	25	25	10	10	7	50	50
I <sub>PZH</sub>				25	25	15	15	12	50	50

UNIT: ns

## OCTAL BUS TRANSCEIVERS AND REGISTERS WITH 3-STATE OUTPUTS

- Bidirectional Bus Tranceivers
- Independent Registers for A and B Buses
- Multiplexed Real-Time and Stored Data
- True Data Paths
- 3-State Outputs
- 74AC11xxx: Product Available in Reduced-Noise Advanced CMOS (11000 Series)
- 74ACT11xxx: Product Available in Reduced-Noise Advanced CMOS (11000 Series)

Logic Diagram (SN74)



## ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	LS	ALS	ALS A-1	AS	SN74 HC	CD74 HC	SN74 HCT	CD74 HCT	SN74 BCT	ABT	ABT Ver.A	UNIT
I <sub>CC</sub>	MAX	165	88	88	211	0.08	0.16	0.08	0.16	67	30	30	mA
I <sub>OH</sub>	MAX	-15	-15	-15	-15	-6	-6	-6	-6	-15	-32	-32	mA
I <sub>OL</sub>	MAX	24	24	48	48	6	6	6	6	64	64	64	mA

PARAMETER	MAX or MIN	LVTH 3V	AC 11	CD74 AC	ACT 11	CD74 ACT	LVC 3V	UNIT
I <sub>CC</sub>	MAX	5	0.08	0.08	0.08	0.08	0.01	mA
I <sub>OH</sub>	MAX	-32	-24	-24	-24	-24	-24	mA
I <sub>OL</sub>	MAX	64	24	24	24	24	24	mA

FUNCTION TABLE (SN74)

INPUTS						DATA I/O†		OPERATION OR FUNCTION						
OE	DIR	CLKAB	CLKBA	SAB	SBA	A1-A8	B1-B8							
H	X	H to L	H to L	X	X	Input	Input	Isolation Store A and B data						
H	X	T	T	X	X	Input	Input	Real-time B data to A bus Stored B data to A bus						
L	L	X	X	X	L	Output	Input	Real-time A data to B bus Stored A data to B bus						
L	H	X	X	L	X	Input	Output	Real-time A data to B bus Stored A data to B bus						
L	H	H to L	X	H	X	Input	Output							

† The data output functions can be enabled or disabled by various signals at OE and DIR. Data input functions are always enabled; i.e., data at the bus terminals is stored on every low-to-high transition of the clock inputs.

## TIMING REQUIREMENTS AND SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	LS	ALS	ALS A-1	AS	SN74 HC	CD74 HC	SN74 HCT	CD74 HCT	SN74 BCT
t <sub>max</sub>			MIN	-	40	40	90	27	20	27	17	83
t <sub>w</sub>	CLKBA,CLKAB "H"		MIN	15	12.5	12.5	5	19	24	19	38	6
	CLKBA,CLKAB "L"		MIN	30	12.5	12.5	6	19	24	19	38	6
	DATA		MIN	30	-	-	-	-	-	-	-	-
t <sub>su</sub>	CLKBA,CLKAB "H"		MIN	15	10	10	6	25	-	25	18	6
	CLKBA,CLKAB "L"		MIN	15	10	10	6	25	-	25	18	6
	CLKBA,CLKAB		MIN	0	0	0	0	5	11	5	5	0.5
t <sub>plh</sub>	CLOCK	A,B	MAX	25	30	30	8.5	45	66	45	66	11.2
				35	17	17	9	45	66	45	66	10.6
	A,B	B,A	MAX	18	20	20	9	34	41	34	56	9.5
t <sub>phl</sub>	SAB,SBA (sorted data high)	A,B	MAX	20	12	12	7	34	41	34	56	10.5
				40	25	25	11	48	51	48	69	13.8
	A,B		MAX	35	20	20	9	48	51	48	69	9.1
t <sub>plh</sub>	SAB,SBA (sorted data low)	A,B	MAX	50	35	35	11	48	51	48	69	12
				25	20	20	9	48	51	48	69	12.9
	OE	A,B	MAX	55	17	17	9	61	53	61	68	13.2
t <sub>plz</sub>	OE	A,B	MAX	65	20	20	14	61	53	61	68	14.4
				35	10	10	9	61	53	61	53	10.9
	DIR	A,B	MAX	35	16	16	9	61	53	61	53	10.5
t <sub>pzh</sub>	DIR	A,B	MAX	45	30	30	16	61	53	61	-	13.1
				60	25	25	18	61	53	61	-	14.6
	DIR	A,B	MAX	30	10	10	10	61	53	61	-	12.6
t <sub>pzl</sub>	DIR	A,B	MAX	30	16	16	10	61	53	61	-	11.8
				30	16	16	10	61	53	61	-	

PARAMETER	INPUT	OUTPUT	MAX or MIN	ABT	ABT Ver.A	LVTH 3V	AC 11	CD74 AC	ACT 11	CD74 ACT	LVC 3V
t <sub>max</sub>			MIN	125	125	150	100	125	105	110	150
t <sub>w</sub>	CLKBA,CLKAB "H"		MIN	4	4	3.3	5	4	4.8	4.5	3.3
	CLKBA,CLKAB "L"		MIN	4	4	3.3	5	4	4.8	4.5	3.3
	DATA		MIN	-	-	-	-	-	-	-	-
t <sub>su</sub>	CLKBA,CLKAB "H"		MIN	3.5	3	1.2	4.5	2.5	4.5	2.5	1.5
	CLKBA,CLKAB "L"		MIN	3	3	1.6	4.5	2.5	4.5	2.5	1.5
	CLKBA,CLKAB		MIN	0	0	0.8	1	2	2.5	2	1.7
t <sub>plh</sub>	CLOCK	A,B	MAX	7.8	5.6	4.7	11	13.5	13.5	15.5	8.4
				8.4	5.6	4.7	12.2	13.5	14.9	15.5	8.4
	A,B	B,A	MAX	6.9	4.8	3.5	8.8	11	11.5	12.5	7.4
t <sub>phl</sub>	SAB,SBA (sorted data high)	A,B	MAX	7.1	6.5	4.9	9.4	12	11.5	14.5	8.6
				7.9	5.9	4.9	10.7	12	13.5	14.5	8.6
	SAB,SBA (sorted data low)	A,B	MAX	7.1	6.5	4.9	9.9	12	12.4	14.5	8.6
t <sub>pzh</sub>	OE	A,B	MAX	6.3	6.3	5.2	12	13.5	14.4	15.5	8.2
				8.8	8.8	5.2	13.1	13.5	15.3	15.5	8.2
	DIR	A,B	MAX	8.3	5	5.5	8.9	13.5	11.6	15.5	7.5
t <sub>pzl</sub>	OE	A,B	MAX	7.5	4.5	5.5	8.3	13.5	10.6	15.5	7.5
				9.5	9.5	5.2	13.7	13.5	16.5	15.5	8.3
	DIR	A,B	MAX	7.7	5.7	5.6	8.7	13.5	11.3	15.5	7.9
t <sub>flz</sub>	DIR	A,B	MAX	8.2	6	5.6	8.1	13.5	10.3	15.5	7.9
				8.2	6	5.6	8.1	13.5	10.3	15.5	7.9

UNIT fmax : MHz other : ns

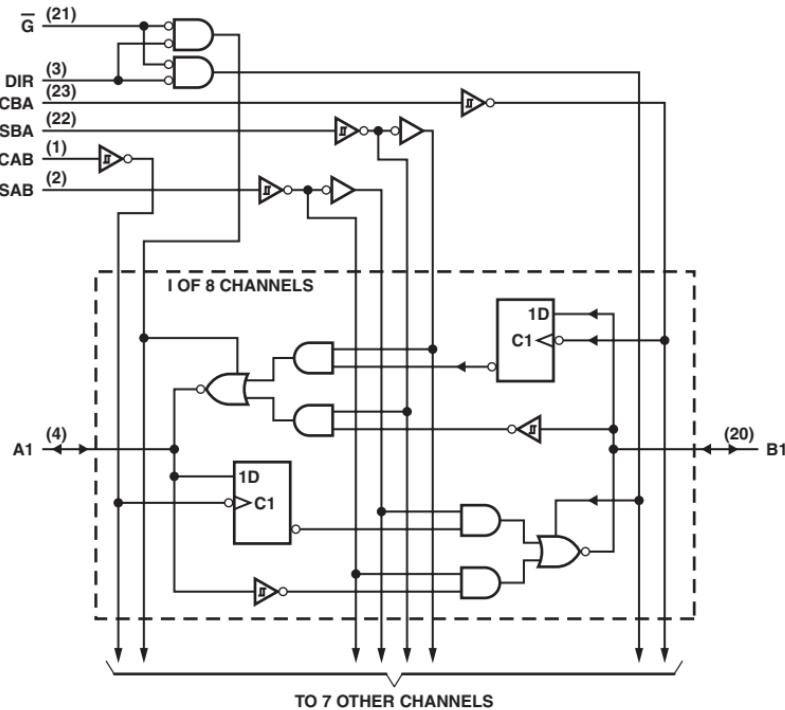
## CD74HC: NOT RECOMMENDED FOR NEW DESIGNS

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters. See [www.ti.com/sc/logic](http://www.ti.com/sc/logic) for the most current data sheets.

## OCTAL BUS TRANSCEIVERS AND REGISTERS

- Bidirectional Bus Tranceivers
- Independent Registers for A and B Buses
- Multiplexed Real-Time and Stored Data
- True Data Paths
- Open-Collector Outputs

Logic Diagram



FUNCTION TABLE

INPUTS					DATA I/O†		OPERATION OR FUNCTION	
<b>G</b>	<b>DIR</b>	<b>CAB</b>	<b>CBA</b>	<b>SAB</b>	<b>SBA</b>	<b>A1-A8</b>	<b>B1-B8</b>	
H	X	H to L	H to L	X	X	Input	Input	Isolation
H	X	↑	↑	X	X	Input	Input	Store A and B data
L	L	X	X	X	L	Output	Input	Real-time B data to A bus
L	L	X	H to L	X	H	Output	Input	Stored B data to A bus
L	H	X	X	L	X	Input	Output	Real-time A data to B bus
L	H	H to L	X	H	X	Input	Output	Stored A data to B bus

† The data output functions can be enabled or disabled by various signals at OE and DIR. Data input functions are always enabled; i.e., data at the bus terminals is stored on every low-to-high transition of the clock inputs.

## ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	LS	UNIT
I <sub>CC</sub>	MAX	150	mA
V <sub>OH</sub>	MAX	5.5	V
I <sub>OL</sub>	MAX	24	mA

## TIMING REQUIREMENTS AND SWITCHING CHARACTERISTICS

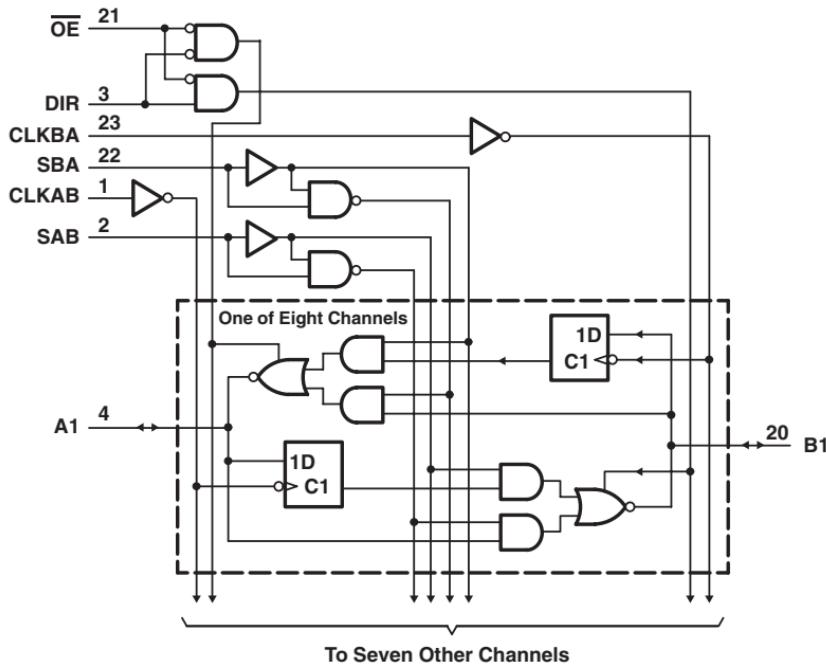
PARAMETER	INPUT	OUTPUT	MAX or MIN	LS
t <sub>W</sub>			MIN	30
t <sub>SW</sub>		A,B	MIN	15
t <sub>B</sub>		A,B	MIN	0
t <sub>PLH</sub>	CLOCK	A,B	MAX	35
t <sub>PHL</sub>			MAX	45
t <sub>PLH</sub>	A,B	B,A	MAX	26
t <sub>PHL</sub>			MAX	27
t <sub>PLH</sub>	SAB,SBA (With Bus Input High)	A,B	MAX	50
t <sub>PHL</sub>			MAX	45
t <sub>PLH</sub>	SAB,SBA (With Bus Input Low)	A,B	MAX	60
t <sub>PHL</sub>			MAX	30
t <sub>PLH</sub>	G	A,B	MAX	40
t <sub>PHL</sub>			MAX	50
t <sub>PLH</sub>	DIR	A,B	MAX	35
t <sub>PHL</sub>			MAX	40

UNIT: ns

## OCTAL BUS TRANSCEIVERS AND REGISTERS

- Bidirectional Bus Tranceivers
- Independent Registers for A and B Buses
- Multiplexed Real-Time and Stored Data
- Inverting Data Paths
- 3-State Outputs

Logic Diagram



FUNCTION TABLE

INPUTS				DATA I/O†			OPERATION OR FUNCTION	
OE	DIR	CLKAB	CLKBA	SAB	SBA	A1-A8	B1-B8	
H	X	H to L	H to L	X	X	Input	Input	Isolation
H	X	T	T	X	X	Input	Input	Store A and B data
L	L	X	X	X	L	Output	Input	Real-time B data to A bus
L	L	X	H to L	X	H	Output	Input	Stored B data to A bus
L	H	X	X	L	X	Input	Output	Real-time A data to B bus
L	H	H to L	X	H	X	Input	Output	Stored A data to B bus

† The data output functions can be enabled or disabled by various signals at OE and DIR. Data input functions are always enabled; i.e., data at the bus terminals is stored on every low-to-high transition of the clock inputs.

## ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	LS	ALS	AS	SN74 HC	SN74 HCT	UNIT
I <sub>CC</sub>	MAX	180	88	195	0.08	0.08	mA
I <sub>OH</sub>	MAX	-15	-15	-15	-6	-6	mA
I <sub>OL</sub>	MAX	24	24	48	6	6	mA

## TIMING REQUIREMENTS AND SWITCHING CHARACTERISTICS

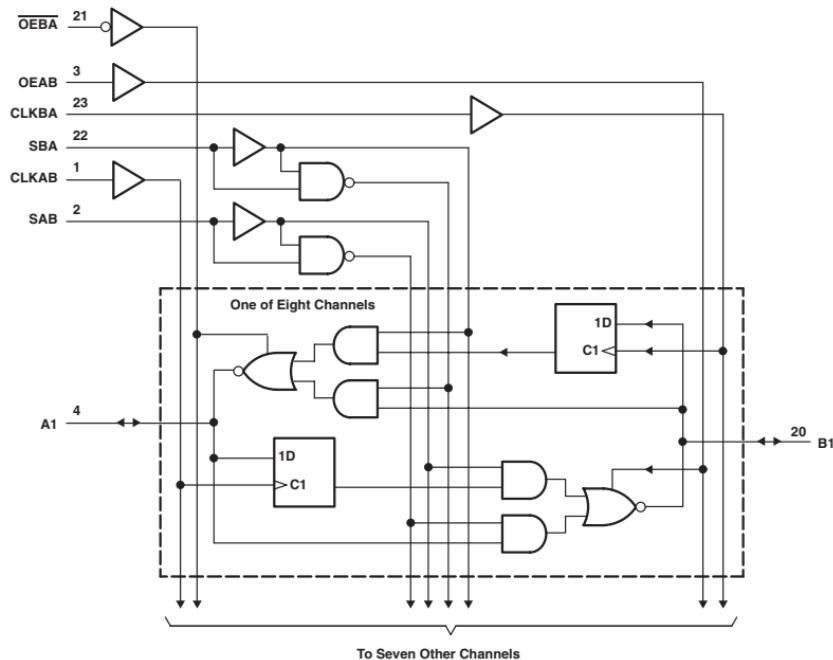
PARAMETER	INPUT	OUTPUT	MAX or MIN	LS	ALS	AS	SN74 HC	SN74 HCT
f <sub>max</sub>			MIN	-	40	90	27	27
t <sub>w</sub>	CLKAB, CLKBA "H"		MIN	15	12.5	5	19	19
	CLKAB, CLKBA "L"		MIN	30	12.5	6	19	19
DATA			MIN	30	-	-	-	-
t <sub>su</sub>	CLKAB, CLKBA		MIN	15	10	6	25	25
t <sub>th</sub>	CLKAB, CLKBA		MIN	0	0	0	5	5
t <sub>PLH</sub>	CLOCK	A,B	MAX	25	33	8.5	45	45
t <sub>PHL</sub>				40	20	9	45	45
t <sub>PLH</sub>	A,B	B,A	MAX	18	17	8	34	34
t <sub>PHL</sub>				25	10	7	34	34
t <sub>PLH</sub>	SAB,SBA (With Bus Input High)	A,B	MAX	55	25	11	48	48
t <sub>PHL</sub>				40	21	9	48	48
t <sub>PLH</sub>	SAB,SBA (With Bus Input Low)	A,B	MAX	40	39	11	48	48
t <sub>PHL</sub>				40	22	9	48	48
t <sub>ZH</sub>	OE	A,B	MAX	50	22	9	61	61
t <sub>ZL</sub>				55	22	15	61	61
t <sub>ZH</sub>	OE	A,B	MAX	45	10	9	61	61
t <sub>ZL</sub>				35	15	9	61	61
t <sub>ZH</sub>	DIR	A,B	MAX	40	27	16	61	61
t <sub>ZL</sub>				45	19	18	61	61
t <sub>ZH</sub>	DIR	A,B	MAX	35	14	10	61	61
t <sub>ZL</sub>				30	15	10	61	61

UNIT f<sub>max</sub> : MHz other : ns

## OCTAL BUS TRANSCEIVERS AND REGISTERS WITH 3-STATE OUTPUTS

- Bus Tranceivers / Registers
- Independent Registers and Enables for A and B Buses
- Multiplexed Real-Time and Stored Data
- Inverting Data Paths
- 3-State Outputs

Logic Diagram (SN74)



FUNCTION TABLE (SN74)

INPUTS						DATA I/O				OPERATION OR FUNCTION		
OEAB	OEBA	CLKAB	CLKBA	SAB	SBA	A1-A8		B1-B8				
L	H	H to L	H to L	X	X	Input	Input	Isolation				
L	H	↑	↑	X	X	Input	Input	Store A and B data				
X	H	↑	H to L	X	X	Input	Input	Store A, hold B				
H	H	↑	↑	X	X	Unspecified	Output	Store A in both registers				
L	X	H to L	↑	X	X	Unspecified	Output	Hold A, store B				
L	L	↑	↑	X	X	Output	Output	Store B in both registers				
L	L	X	X	X	L	Output	Input	Real-time B data to A bus				
L	L	X	X	H	X	Output	Input	Stored B data to A bus				
H	H	X	X	L	X	Input	Input	Real-time A data to B bus				
H	H	H to L	X	H	X	Input	Input	Stored A data to B bus				
H	L	H to L	H to L	H	H	Output	Output	Stored A data to B bus and stored B data to A bus				

## ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	LS	ALS	ALS A-1	AS	SN74 HC	SN74 HCT	SN74 BCT	ABT	CD74 ACT	UNIT
I <sub>CC</sub>	MAX	165	82	82	195	0.08	0.08	62	30	160	mA
I <sub>OH</sub>	MAX	-15	-15	-15	-15	-6	-6	-15	-32	-24	mA
I <sub>OL</sub>	MAX	24	24	48	48	6	6	64	64	24	mA

## TIMING REQUIREMENTS AND SWITCHING CHARACTERISTICS

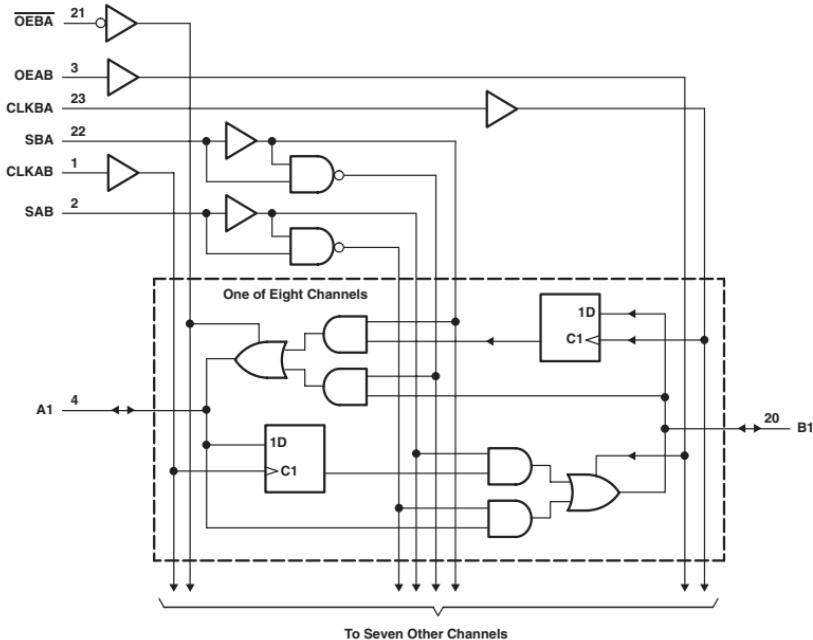
PARAMETER	INPUT	OUTPUT	MAX or MIN	LS	ALS	ALS A-1	AS	SN74 HC	SN74 HCT	SN74 BCT	ABT	CD74 ACT
t <sub>max</sub>			MIN	-	40	40	90	27	20	85	125	110
t <sub>w</sub>	CLKBA, CLKAB "H"		MIN	15	12.5	12.5	5	19	25	4.8	4	4.5
	CLKBA, CLKAB "L"		MIN	15	12.5	12.5	6	19	25	7	4	4.5
	DATA		MIN	15	-	-	-	-	-	-	-	-
t <sub>su</sub>	A,B		MIN	15	10	10	6	25	19	6	3	2.5
t <sub>th</sub>	A,B		MIN	0	0	0	0	5	5	1	0	2
t <sub>pLH</sub>	CLOCK	A,B	MAX	24	32	32	8.5	45	45	11.7	5.6	15.5
t <sub>pHL</sub>				35	17	17	9	45	45	11.8	5.6	15.5
t <sub>pLH</sub>	A,B	B,A	MAX	18	18	18	9	34	34	12.6	6.2	12.5
t <sub>pHL</sub>				30	10	10	7	34	34	9.8	5.4	12.5
t <sub>pLH</sub>	SAB,SBA (With Bus Input High)	A,B	MAX	47	38	38	11	48	48	9.8	6.5	15.5
t <sub>pHL</sub>				33	21	21	9	48	48	15.5	5.9	15.5
t <sub>pLH</sub>	SAB,SBA (With Bus Input Low)	A,B	MAX	35	25	25	11	48	48	14.6	6.5	15.5
t <sub>pHL</sub>				30	21	21	9	48	48	12.8	5.9	15.5
t <sub>pZH</sub>	OEBA	A	MAX	44	20	20	10	61	61	12	5.8	15.5
t <sub>pZL</sub>				60	18	18	16	61	61	13.1	8.5	15.5
t <sub>pHZ</sub>	OEBA	A	MAX	38	9	9	9	61	61	10.2	5	15.5
t <sub>pZL</sub>				30	12	12	9	61	61	9.6	4.1	15.5
t <sub>pZH</sub>	OEAB	B	MAX	29	22	22	11	61	61	8.3	6.5	15.5
t <sub>pZL</sub>				40	21	21	16	61	61	9.7	7.4	15.5
t <sub>pHZ</sub>	OEAB	B	MAX	38	12	12	10	61	61	15	5.5	15.5
t <sub>pZL</sub>				30	14	14	11	61	61	12.3	5.1	15.5

UNIT t<sub>max</sub> : MHz other : ns

## OCTAL BUS TRANSCEIVERS AND REGISTERS

- Bus Tranceivers / Registers
- Independent Registers and Enables for A and B Buses
- Multiplexed Real-Time and Stored Data
- True Data Paths
- 3-State Outputs
- 74AC11xxx: Product Available in Reduced-Noise Advanced CMOS (11000 Series)
- 74ACT11xxx: Product Available in Reduced-Noise Advanced CMOS (11000 Series)

**Logic Diagram (SN74)**



**FUNCTION TABLE (SN74)**

INPUTS		DATA I/O				OPERATION OR FUNCTION		
OEAB	OEBA	CLKAB	CLKBA	SAB	SBA	A1-A8	B1-B8	
L	H	H to L	H to L	X	X	Input	Input	Isolation Store A and B data
L	H	↑	↑	X	X	Input	Input	Store A, hold B Store A in both registers
X	H	↑	H to L	X	X	Input	Unspecified Output	Hold A, store B Store B in both registers
H	H	↑	↑	X	X	Unspecified Output	Input Input	Real-time B data to A bus Stored B data to A bus
L	X	H to L	↑	X	X	Output	Input	Real-time A data to B bus Stored A data to B bus
L	L	X	H to L	X	H	Output	Output	Real-time A data to B bus Stored A data to B bus
H	H	X	X	L	X	Input	Output	Stored A data to B bus and stored B data to A bus
H	L	H to L	H to L	H	H	Output	Output	

## ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	LS	ALS	ALS A-1	AS	SN74 HC	CD74 HC	SN74 HCT	CD74 HCT	SN74 BCT	ABT	UNIT
I <sub>CC</sub>	MAX	180	88	88	211	0.08	0.16	0.08	0.16	69	30	mA
I <sub>OH</sub>	MAX	-15	-15	-15	-15	-6	-6	-6	-6	-15	-32	mA
I <sub>OL</sub>	MAX	24	24	48	48	6	6	6	6	64	64	mA

PARAMETER	MAX or MIN	ABT Ver.A	LVTH 3V	AC 11	CD74 AC	ACT 11	CD74 ACT	LVC 3V	UNIT
I <sub>CC</sub>	MAX	30	5	0.08	0.16	0.08	0.16	0.01	mA
I <sub>OH</sub>	MAX	-32	-32	-24	-24	-24	-24	-24	mA
I <sub>OL</sub>	MAX	64	64	24	24	24	24	24	mA

## TIMING REQUIREMENTS AND SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	LS	ALS	ALS A-1	AS	SN74 HC	CD74 HC	SN74 HCT	CD74 HCT	SN74 BCT
t <sub>max</sub>			MIN	-	40	40	90	27	20	20	17	77
t <sub>tr</sub>	CLKBA, CLKAB "H"		MIN	15	12.5	12.5	5	19	24	25	38	6.5
	CLKBA, CLKAB "L"		MIN	15	12.5	12.5	6	19	24	25	38	6.5
	DATA		MIN	15	-	-	-	-	-	-	-	-
t <sub>su</sub>	A,B High		MIN	15	10	10	6	25	18	19	18	5
	A,B Low		MIN	15	10	10	6	25	18	19	18	5
t <sub>th</sub>	A,B		MIN	0	0	0	0	5	11	5	5	1
t <sub>PLH</sub>	CLOCK	A,B	MAX	25	30	30	8.5	45	66	45	66	10.5
t <sub>PLHL</sub>			MAX	36	17	17	9	45	66	45	66	9.9
t <sub>PLH</sub>	A,B	B,A	MAX	18	18	18	9	34	41	34	56	8.9
t <sub>PLHL</sub>			MAX	20	12	12	7	34	41	34	56	9.8
t <sub>PLH</sub>	SAB,SBA (With Bus Input High)	A,B	MAX	35	35	35	11	48	51	48	69	13.1
t <sub>PLHL</sub>			MAX	32	20	20	9	48	51	48	69	8.5
t <sub>PLH</sub>	SAB,SBA (With Bus Input Low)	A,B	MAX	50	25	25	11	48	51	48	69	11.3
t <sub>PLHL</sub>			MAX	23	20	20	9	48	51	48	69	12.5
t <sub>ZH</sub>	OEBA	A	MAX	45	17	17	10	61	53	61	68	10.6
t <sub>ZL</sub>			MAX	54	18	18	16	61	53	61	68	12
t <sub>PZH</sub>	OEBA	A	MAX	38	10	10	9	61	53	61	53	10
t <sub>PZL</sub>			MAX	30	16	16	9	61	53	61	53	9.5
t <sub>ZH</sub>	OEAB	B	MAX	30	22	22	11	61	53	61	68	8.1
t <sub>ZL</sub>			MAX	38	18	18	16	61	53	61	68	9.3
t <sub>PZH</sub>	OEAB	B	MAX	38	10	10	10	61	53	61	53	11.6
t <sub>PZL</sub>			MAX	30	16	16	11	61	53	61	53	11.3

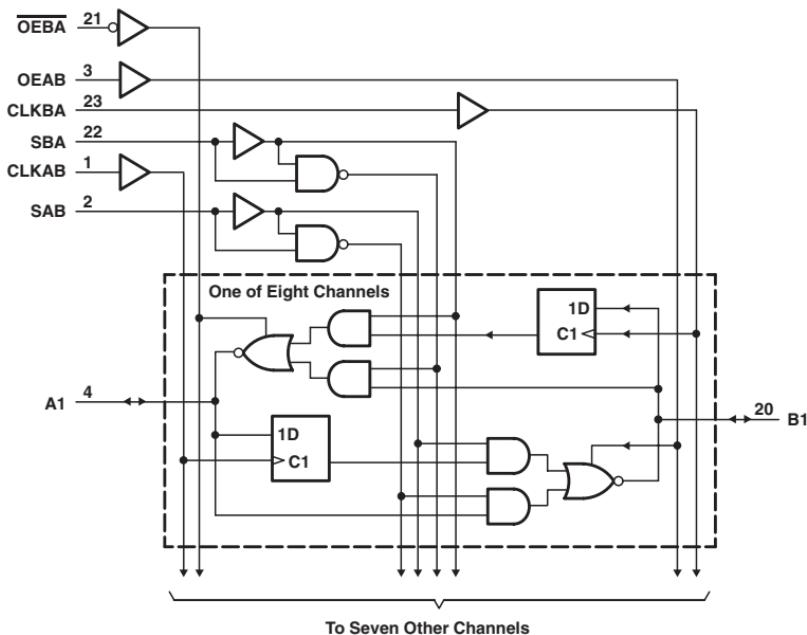
PARAMETER	INPUT	OUTPUT	MAX or MIN	ABT	ABT Ver.A	LVTH 3V	AC 11	CD74 AC	ACT 11	CD74 ACT	LVC 3V
t <sub>max</sub>			MIN	125	125	150	105	125	105	110	100
t <sub>tr</sub>	CLKBA, CLKAB "H"		MIN	4	4	3.3	4.8	4	4.8	4.5	3.3
	CLKBA, CLKAB "L"		MIN	4	4	3.3	4.8	4	4.8	4.5	3.3
	DATA		MIN	-	-	-	-	-	-	-	-
t <sub>su</sub>	A,B High		MIN	3.5	3	1.2	4.5	2.5	4	2.5	1.9
	A,B Low		MIN	3.5	3	1.6	4.5	2.5	4	2.5	1.9
t <sub>th</sub>	A,B		MIN	0	0	0.8	1	2	2.5	2	1.7
t <sub>PLH</sub>	CLOCK	A,B	MAX	7.8	5.6	4.7	10.7	13.5	13.1	15.5	8
t <sub>PLHL</sub>			MAX	8.4	5.6	4.7	12	13.5	14.4	15.5	8
t <sub>PLH</sub>	A,B	B,A	MAX	6.7	4.8	3.5	8.6	11	11.1	12.5	7.4
t <sub>PLHL</sub>			MAX	6.7	5.4	3.5	9.6	11	11.6	12.5	7.4
t <sub>ZH</sub>	SAB,SBA (With Bus Input High)	A,B	MAX	6.9	6.5	4.9	9.1	12	11	14.5	8.7
t <sub>ZL</sub>			MAX	7.7	5.9	4.9	10.7	12	13.3	14.5	8.7
t <sub>PZH</sub>	SAB,SBA (With Bus Input Low)	A,B	MAX	6.9	6.5	4.9	9.9	12	12.2	14.5	8.7
t <sub>PZL</sub>			MAX	7.7	5.9	4.9	10.9	12	12.6	14.5	8.7
t <sub>ZH</sub>	OEBA	A	MAX	5.8	5.8	5.2	10.9	13.5	12.6	15.5	7.4
t <sub>ZL</sub>			MAX	8.5	8.5	5.2	12.2	13.5	13.8	15.5	7.4
t <sub>PZH</sub>	OEBA	A	MAX	8.2	5	5.5	7.6	13.5	9.9	15.5	7.5
t <sub>PZL</sub>			MAX	6.8	4.1	5.5	7.1	13.5	9.3	15.5	7.5
t <sub>ZH</sub>	OEAB	B	MAX	6.5	6.5	4.7	11.3	13.5	15.2	15.5	7.1
t <sub>ZL</sub>			MAX	7.4	7.4	4.7	12.3	13.5	16.1	15.5	7.1
t <sub>PZH</sub>	OEAB	B	MAX	6.9	5.5	5.6	7.6	13.5	10.3	15.5	7.4
t <sub>PZL</sub>			MAX	6.2	5.1	5.6	7.2	13.5	9.3	15.5	7.4

UNIT fmax : MHz other : ns

## OCTAL BUS TRANSCEIVERS AND REGISTERS

- Bus Tranceivers / Registers
  - Independent Registers and Enables for A and B Buses
  - Multiplexed Real-Time and Stored Data
  - Inverting Data Paths
  - Outputs
- A Bus: Open-Collector  
B Bus: 3-State

Logic Diagram



FUNCTION TABLE

INPUTS						DATA VOL		OPERATION OR FUNCTION
OEAB	OEBA	CLKAB	CLKBA	SAB	SBA	A1-A8	B1-B8	
L	H	H or L	H or L	X	X	Input	Input	Isolation Store A and B data
L	H	↑	↑	X	X	Input	Unspecified‡	Store A, hold B Store A in both registers
X	H	↑	H or L	X	X	Input	Output	Hold A, store B Store B in both registers
H	H	↑	↑	X‡	X	Unspecified‡	Input	Real-time B data to A bus Stored B data to A bus
L	X	H or L	↑	X	X	Output	Input	Real-time A data to B bus Stored A data to B bus
L	L	↑	↑	X	X‡	Input	Output	Stored A data to B bus and stored B data to A bus
L	L	X	X	X	L	Output	Input	
L	L	X	H or L	X	H			
H	H	X	X	L	X			
H	H	H or L	X	H	X			
H	L	H or L	H or L	H	H	Output	Output	

## NOTES:

† The data output functions can be enabled or disabled by a variety of level combinations at GAB or GBA. Data input functions always are enabled; i.e., data at the bus terminals is stored on every low-to-high transition on the clock inputs.

‡ Select control = L: clocks can occur simultaneously.

Select control = H: clock must be staggered to load both registers.

## ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	LS	ALS	UNIT
I <sub>CC</sub>	MAX	165	88	mA
I <sub>OH</sub>	MAX	-15	-15	mA
I <sub>OL</sub>	MAX	24	24	mA

## TIMING REQUIREMENTS AND SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	LS	ALS
t <sub>w</sub>	CLK "H"		MIN	15	14.5
	CLK "L"		MIN	30	14.5
	DATA		MIN	30	-
t <sub>su</sub>	A, B		MIN	15	10
t <sub>th</sub>	A, B		MIN	0	0
t <sub>PLH</sub>	CLKBA	A	MAX	38	64
t <sub>PHL</sub>				39	22
t <sub>PLH</sub>	CLKAB	B	MAX	23	30
t <sub>PHL</sub>				36	17
t <sub>PLH</sub>	A	B	MAX	18	18
t <sub>PHL</sub>				30	15
t <sub>PLH</sub>	B	A	MAX	32	56
t <sub>PHL</sub>				24	15
t <sub>PLH</sub>	SBA (B "H")	A	MAX	57	62
t <sub>PHL</sub>				39	25
t <sub>PLH</sub>	SBA (B "L")	A	MAX	51	62
t <sub>PHL</sub>				35	25
t <sub>PLH</sub>	SAB	B	MAX	48	35
t <sub>PHL</sub>				33	22
t <sub>PLH</sub>	SAB (A "H")	B	MAX	36	25
t <sub>PHL</sub>				30	22
t <sub>PLH</sub>	SAB (A "L")	B	MAX	35	30
t <sub>PHL</sub>				35	24
t <sub>ZH</sub>	OEAB	B	MAX	29	22
t <sub>ZL</sub>				38	22
t <sub>PZ</sub>	OEAB	B	MAX	39	14
t <sub>PLZ</sub>				29	16

UNIT:ns

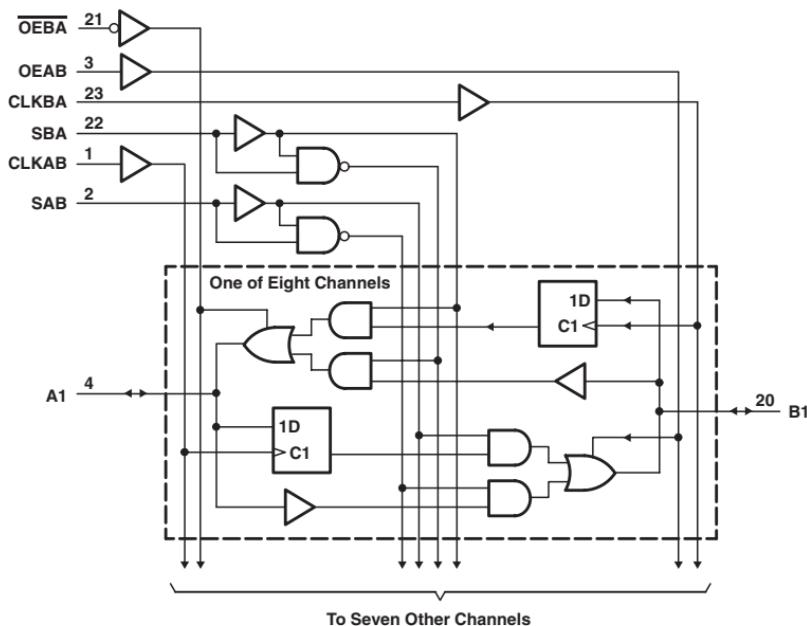
## OCTAL BUS TRANSCEIVERS AND REGISTERS

- Bus Tranceivers / Registers
- Independent Registers and Enables for A and B Buses
- Multiplexed Real-Time and Stored Data
- True Data Paths
- Outputs

A Bus: Open-Collector

B Bus: 3-State

Logic Diagram



FUNCTION TABLE								
INPUTS				DATA I/O		OPERATION OR FUNCTION		
OEAB	OEBA	CLKAB	CLKBA	SAB	SBA	A1-A8	B1-B8	
L	H	H to L	H to L	X	X	Input	Input	Isolation Store A and B data
L	H	↑	↑	X	X	Input	Input	Store A, hold B Store A in both registers
X	H	↑	H to L	X	X	Unspecified	Output	Store A, hold B Store B in both registers
L	X	H to L	↑	X	X	Unspecified	Output	Hold A, store B Store B in both registers
L	L	X	X	X	L	Output	Input	Real-time B data to A bus Stored B data to A bus
L	L	X	H to L	X	H	Output	Input	Real-time A data to B bus Stored A data to B bus
H	H	X	X	L	X	Input	Output	Real-time A data to B bus Stored A data to B bus
H	H	H to L	X	H	X	Input	Output	Real-time B data to A bus Stored B data to A bus
H	L	H to L	H to L	H	H	Output	Output	Stored A data to B bus and stored B data to A bus

#### ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	LS	ALS	UNIT
I <sub>CC</sub>	MAX	180	88	mA
I <sub>OH</sub>	MAX	-15	-15	mA
I <sub>OL</sub>	MAX	24	24	mA

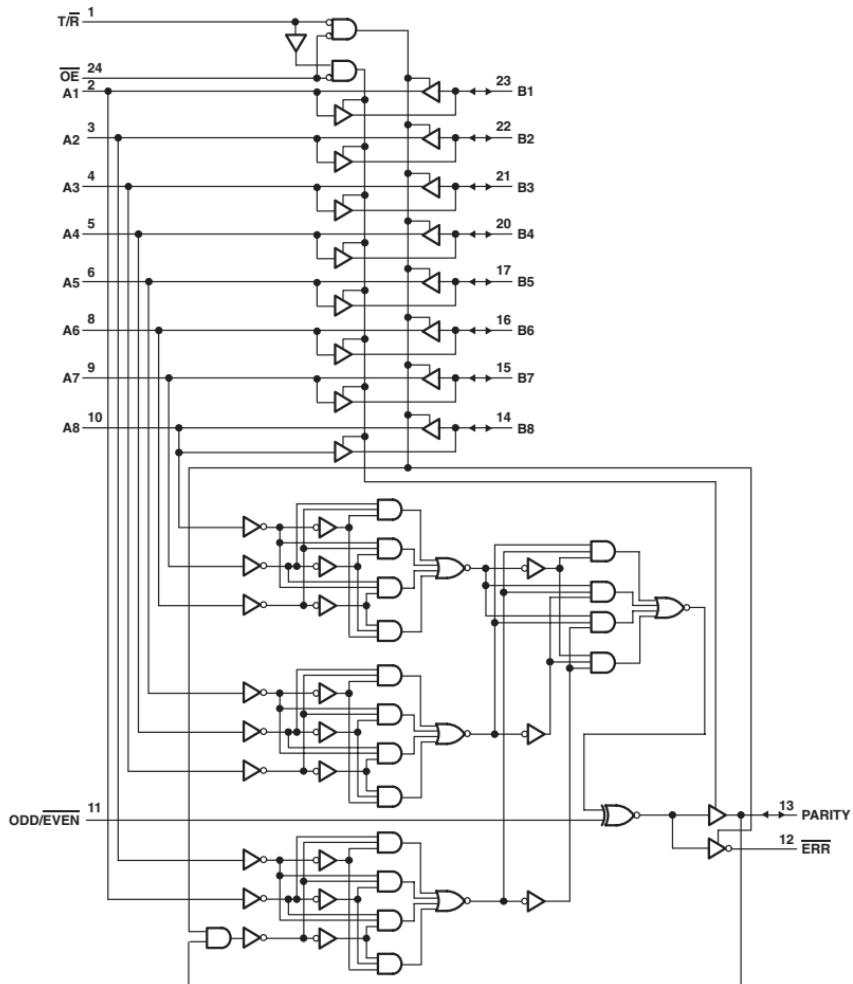
#### TIMING REQUIREMENTS AND SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	LS	ALS
t <sub>w</sub>	CLKBA, CLKAB "H"		MIN	15	14.5
	CLKBA, CLKAB "L"		MIN	30	14.5
	DATA		MIN	30	-
t <sub>tu</sub>	A,B		MIN	15	10
t <sub>th</sub>	A,B		MIN	0	0
t <sub>PLH</sub>	CLKBA	A	MAX	33	64
t <sub>PHL</sub>				36	22
t <sub>PLH</sub>	CLKAB	B	MAX	21	30
t <sub>PHL</sub>				33	17
t <sub>PLH</sub>	A	B	MAX	18	18
t <sub>PHL</sub>				30	15
t <sub>PLH</sub>	B	A	MAX	27	56
t <sub>PHL</sub>				21	21
t <sub>PLH</sub>	SBA (B "H")	A	MAX	48	62
t <sub>PHL</sub>				32	25
t <sub>PLH</sub>	SBA (B "L")	A	MAX	54	62
t <sub>PHL</sub>				29	25
t <sub>PLH</sub>	SAB (A "H")	B	MAX	35	25
t <sub>PHL</sub>				27	22
t <sub>PLH</sub>	SAB (A "L")	B	MAX	45	35
t <sub>PHL</sub>				21	22
t <sub>ZH</sub>	OEBA	A	MAX	35	30
t <sub>ZL</sub>				53	24
t <sub>PHZ</sub>	OEAB	B	MAX	29	22
t <sub>PZL</sub>				33	22
t <sub>PLZ</sub>	OEAB	B	MAX	39	14
t <sub>PLZ</sub>				29	16

UNIT: ns

**OCTAL BUS TRANSCEIVERS WITH PARITY GENERATORS/CHECKERS AND 3-STATE OUTPUTS**

- Combines SN74F245 and SN74F280B Functions in One Package
- 3-State Outputs
- 74ACT11xxx: Product Available in Reduced-Noise Advanced CMOS (11000 Series)

**Logic Diagram**

## ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	F	SN74 BCT	ABT	ACT 11	UNIT
I <sub>CH</sub>	MAX	125	2	0.25	0.08	mA
I <sub>CL</sub>	MAX	150	90	40	0.08	mA
I <sub>CZ</sub>	MAX	145	1	0.25	0.08	mA
I <sub>OH</sub> A1-A9	MAX	-3	-3	-32	-24	mA
I <sub>OH</sub> B1-B9, PARITY, <u>ERR</u>	MAX	-12	-15	-32	-24	mA
I <sub>OL</sub> A1-A8	MAX	24	24	64	24	mA
I <sub>OL</sub> B1-B8, PARITY, <u>ERR</u>	MAX	64	64	64	24	mA

## SWITCHING CHARACTERISTICS

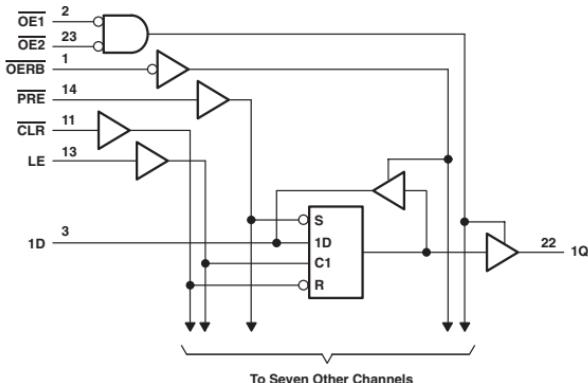
PARAMETER	INPUT	OUTPUT	MAX or MIN	F	SN74 BCT	ABT	ACT 11
I <sub>PLH</sub>	A,B	B,A	MAX	8	6.6	4.6	9.4
I <sub>PLH</sub>			MAX	8	9	4.3	9.4
I <sub>PLH</sub>	A	PARITY	MAX	16	15.4	8.1	14.4
I <sub>PLH</sub>			MAX	16	15.9	7.7	15
I <sub>PLH</sub>	ODD/EVEN	PARITY, <u>ERR</u>	MAX	12	7.1	4.9	10.7
I <sub>PLH</sub>			MAX	12.5	9	4.9	11.3
I <sub>PLH</sub>	B	<u>ERR</u>	MAX	22.5	15.3	7.9	23.6
I <sub>PLH</sub>			MAX	22.5	15.5	7.8	24.6
I <sub>PLH</sub>	PARITY	<u>ERR</u>	MAX	16.5	13.2	7.7	14.6
I <sub>PLH</sub>			MAX	17	13.9	7.5	14.7
I <sub>PZH</sub>	OE	A, B, PARITY	MAX	9	9.1	6.5	12.1
I <sub>PZH</sub>			MAX	11	16.3	6.5	13.8
I <sub>PZH</sub>	OE	<u>ERR</u>	MAX	9	9.1	6.6	12.1
I <sub>PZH</sub>			MAX	11	16.3	9.2	13.8
I <sub>PZL</sub>	OE	A, B, PARITY, ERR	MAX	8	9.1	6.2	12.1
I <sub>PZL</sub>			MAX	6.5	8	7.8	11.6

UNIT: ns

## 8-BIT D-TYPE TRANSPARENT READ-BACK LATCHES WITH 3-STATE OUTPUTS

- 3-State I/O-Type Read-Back Inputs
- True Outputs
- Bus-Structured Pinout

Logic Diagram

ELECTRICAL CHARACTERISTICS AND  
RECOMMENDED OPERATING CONDITIONS

PARAMETER		MAX or MIN	ALS	UNIT
$I_{CC}$		MAX	73	mA
	Q	MAX	-2.6	mA
$I_{OH}$	D	MAX	-0.4	mA
	Q	MAX	24	mA
$I_{OL}$	D	MAX	8	mA

## TIMING REQUIREMENTS AND SWITCHING CHARACTERISTICS

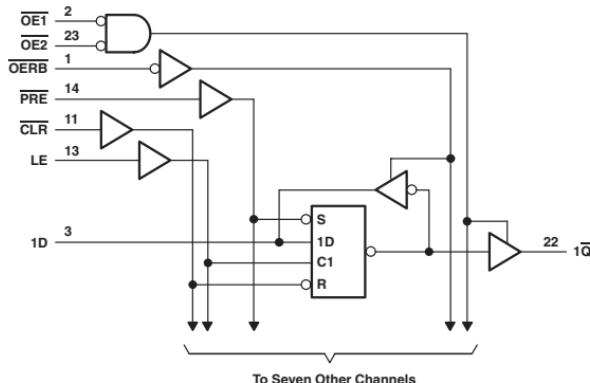
PARAMETER	INPUT	OUTPUT	MAX or MIN	ALS
$t_{\text{tw}}$	LE "H"		MIN	10
	$\overline{\text{CLR}}$ "L"		MIN	10
	$\overline{\text{PRE}}$ "L"		MIN	10
	DATA (LE)		MIN	10
	DATA (OERB)		MIN	10
	DATA (LE)		MIN	5
	$\overline{\text{DPL}}$		MAX	14
$t_{\text{PHL}}$	D	Q	MAX	18
$t_{\text{PHL}}$	LE	Q	MAX	21
$t_{\text{PHL}}$	$\overline{\text{CLR}}$	Q	MAX	29
$t_{\text{PHL}}$	$\overline{\text{PRE}}$	D	MAX	32
$t_{\text{PHL}}$	PRE	Q	MAX	22
$t_{\text{PHL}}$	PRE	D	MAX	28
$t_{\text{en}}$	$\overline{\text{OERB}}$	D	MAX	21
$t_{\text{dis}}$			MAX	14
$t_{\text{en}}$	$\overline{\text{OE1}}, \overline{\text{OE2}}$	Q	MAX	21
$t_{\text{dis}}$			MAX	14

UNIT: ns

## 8-BIT D-TYPE TRANSPARENT READ-BACK LATCHES WITH 3-STATE OUTPUTS

- 3-State I/O-Type Read-Back Inputs
- Inverted Outputs
- Bus-Structured Pinout

Logic Diagram

ELECTRICAL CHARACTERISTICS AND  
RECOMMENDED OPERATING CONDITIONS

PARAMETER		MAX or MIN	ALS	UNIT
I <sub>CC</sub>		MAX	79	mA
	Q	MAX	-2.6	mA
I <sub>OH</sub>	D	MAX	-0.4	mA
	Q	MAX	24	mA
I <sub>OL</sub>	D	MAX	8	mA

## TIMING REQUIREMENTS AND SWITCHING CHARACTERISTICS

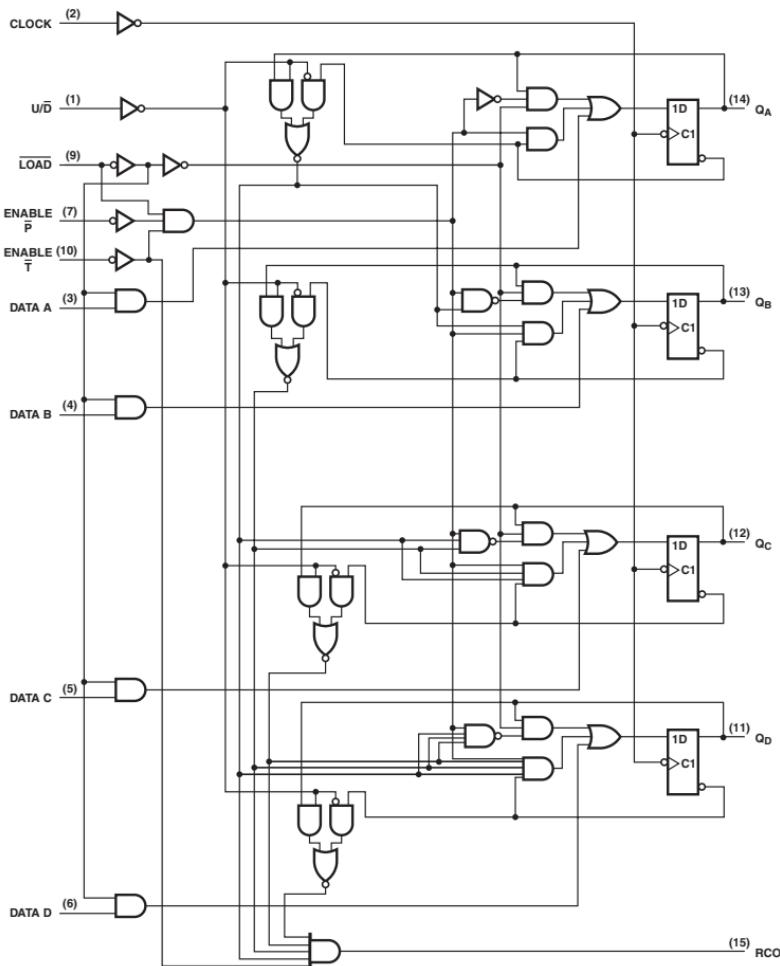
PARAMETER	INPUT	OUTPUT	MAX or MIN	ALS
t <sub>w</sub>	LE "H"		MIN	10
	CLR "L"		MIN	10
	PRE "L"		MIN	10
	DATA (LE)		MIN	10
	DATA (OE <sub>B</sub> )		MIN	10
	DATA (LE)		MIN	5
t <sub>plh</sub>	D	Q̄	MAX	20
				15
t <sub>phl</sub>	LE	Q̄	MAX	28
				22
t <sub>phl</sub>	CLR	Q̄	MAX	24
		D	MAX	26
t <sub>plh</sub>	PRE	Q̄	MAX	25
		D	MAX	28
t <sub>en</sub>	OE <sub>B</sub>	D	MAX	21
t <sub>dis</sub>				14
t <sub>en</sub>	OE <sub>1</sub> , OE <sub>2</sub>	Q̄	MAX	21
t <sub>dis</sub>				14

UNIT: ns

## SYNCHRONOUS 4-BIT UP/DOWN COUNTERS

- Fully Synchronous Operation for Counting and Programming
- Internal Look-Ahead for Fast Counting
- Carry Output for n-Bit Cascading

Logic Diagram



## ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	LS	UNIT
I <sub>CC</sub>	MAX	34	mA
I <sub>OH</sub>	MAX	-0.4	mA
I <sub>OL</sub>	MAX	8	mA

## TIMING REQUIREMENTS AND SWITCHING CHARACTERISTICS

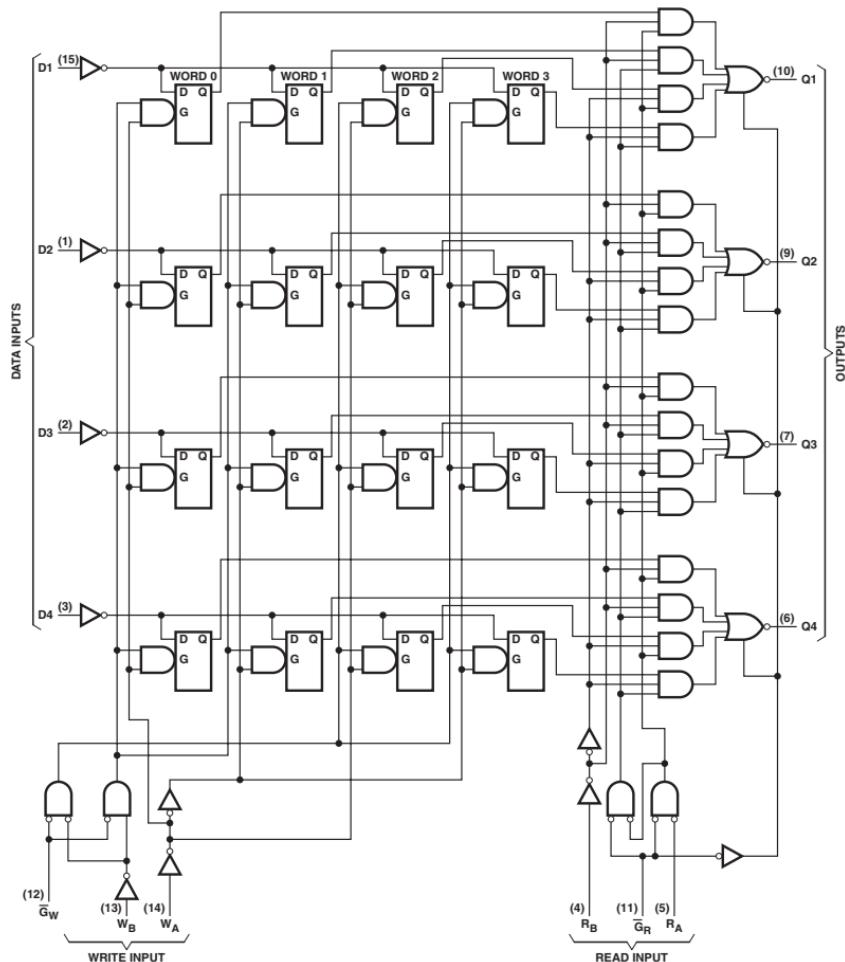
PARAMETER	INPUT	OUTPUT	MAX or MIN	LS
f <sub>max</sub>			MIN	25
t <sub>tr</sub>			MIN	20
t <sub>su</sub>	A,B,C,D		MIN	25
	ENP,ENT		MIN	40
	LOAD		MIN	30
	U/D		MIN	45
	t <sub>th</sub>		MIN	0
t <sub>PLH</sub>	CLOCK	$\overline{RCO}$	MAX	40
t <sub>PHL</sub>				60
t <sub>PLH</sub>	CLOCK	Q	MAX	27
t <sub>PHL</sub>				27
t <sub>PLH</sub>	ENT	$\overline{RCO}$	MAX	17
t <sub>PHL</sub>				45
t <sub>PLH</sub>	U/D	$\overline{RCO}$	MAX	35
t <sub>PHL</sub>				40

UNIT fmax : MHz other : ns

## 4-BY-4 REGISTER FILES WITH 3-STATE OUTPUTS

- Separate Read / Write Addressing Permits Simultaneous Reading and Writing
- Organized as 4 Words of 4 Bits
- Expandable to 512 Words of n-Bits
- 3-State Outputs

Logic Diagram (SN74LS)



**FUNCTION TABLE (SN74)**

WRITE INPUTS			WORD			
W <sub>B</sub>	W <sub>A</sub>	Q̄ <sub>W</sub>	0	1	2	3
L	L	L	Q = D	Q <sub>0</sub>	Q <sub>0</sub>	Q <sub>0</sub>
L	H	L	Q <sub>0</sub>	Q = D	Q <sub>0</sub>	Q <sub>0</sub>
H	L	L	Q <sub>0</sub>	Q <sub>0</sub>	Q = D	Q <sub>0</sub>
H	H	L	Q <sub>0</sub>	Q <sub>0</sub>	Q <sub>0</sub>	Q = D
X	X	H	Q <sub>0</sub>	Q <sub>0</sub>	Q <sub>0</sub>	Q <sub>0</sub>

READ INPUTS			OUTPUTS			
R <sub>B</sub>	R <sub>A</sub>	Q̄ <sub>R</sub>	Q1	Q2	Q3	Q4
L	L	L	W0B1	W0B2	W0B3	W0B4
L	H	L	W1B1	W1B2	W1B3	W1B4
H	L	L	W2B1	W2B2	W2B3	W2B4
H	H	L	W3B1	W3B2	W3B3	W3B4
X	X	H	Z	Z	Z	Z

**ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS**

PARAMETER	MAX or MIN	LS	CD74 HC	CD74 HCT	UNIT
I <sub>CC</sub>	MAX	50	0.16	0.16	mA
I <sub>OH</sub>	MAX	-2.6	-6	-6	mA
I <sub>OL</sub>	MAX	8	6	6	mA

**TIMING REQUIREMENTS AND SWITCHING CHARACTERISTICS**

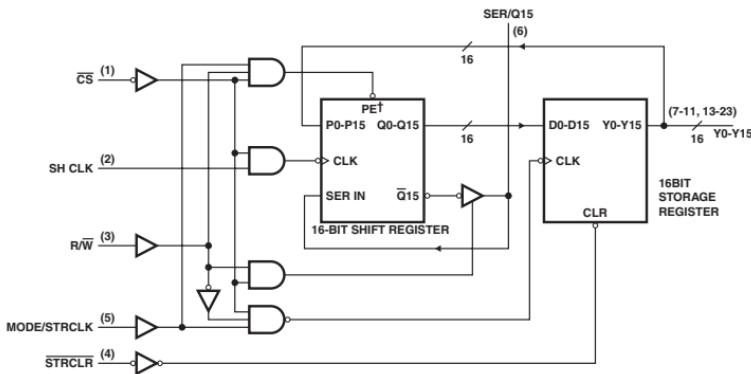
PARAMETER	INPUT	OUTPUT	MAX or MIN	LS	CD74 HC	CD74 HCT
t <sub>w</sub>	Width of write-enable or read-enable pulse		MIN	25	24	30
t <sub>su</sub>	Data input with respect to write enable		MIN	10	18	18
	Write select with respect to write enable			15	18	27
t <sub>h</sub>	Data input with respect to write enable		MIN	15	5	5
	Write select with respect to write enable			5	5	5
t <sub>lat</sub>			MIN	25	30	38
t <sub>PPLH</sub>	Read Select	Q	MAX	40	59	53
				45	59	53
t <sub>PHL</sub>	Write Enable	Q	MAX	45	75	75
				50	75	75
t <sub>PLH</sub>	Data	Q	MAX	45	75	75
				40	75	75
t <sub>PZH</sub>	Read Enable	Q	MAX	35	45	57
				40	45	57
t <sub>PZL</sub>	Read Disable	Q	MAX	50	45	53
				35	45	53

UNIT : ns

## 16-BIT SHIFT REGISTERS

- 16-Bit Serial-In, Serial-Out Shift Register with 16-Bit Parallel-Out Storage Register
- Performs Serial-to-Parallel Conversion

Logic Diagram



† When PE is active, data synchronously parallel loaded into the shift registers form the 16 P inputs and no shifting takes place.

FUNCTION TABLE

CS	R/W	INPUTS		MODE/ STRCLK	SHIFT REGISTER FUNCTIONS					STORAGE REGISTER FUNCTIONS	
		SH CLK	STRCLR		SHIFT	READ FROM SERIAL INPUT	WRITE INTO SERIAL INPUT	PARALLEL LOAD	CLEAR	LOAD	
H	X	X	X	X	Z	NO	NO	NO	NO	NO	
X	X	X	L	X					YES		
L	L	↓	X	X	Z	YES	NO	YES	NO		
L	H	X	X	X	Q15	YES	YES	NO	NO		NO
L	H	↓	X	L	Q14n	YES	YES	NO	NO		NO
L	H	↓	L	X	L	NO	YES		YES	YES;	NO
L	H	↓	H	X	Y15n	NO	YES		YES	NO	NO
L	L	X	H	↑	Z	NO	NO		NO	NO	YES

## ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER		MAX or MIN	LS	UNIT
Icc		MAX	80	mA
Ioh	SER/Q15	MAX	-2.6	mA
	Y0-Y15	MAX	-0.4	mA
Iol	SER/Q15	MAX	24	mA
	Y0-Y15	MAX	8	mA

## TIMING REQUIREMENTS AND SWITCHING CHARACTERISTICS

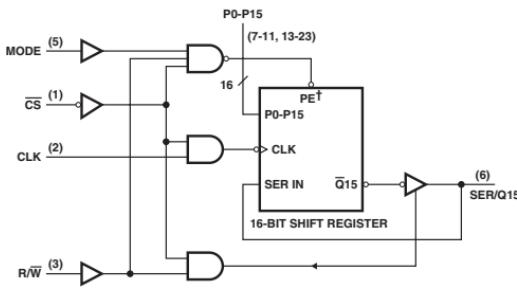
PARAMETER		INPUT	OUTPUT	MAX or MIN	LS
fmax				MIN	20
t <sub>w</sub>	CLK			MIN	20
	CLR			MIN	20
t <sub>su</sub>	SER/Q15			MIN	20
	Y0-Y15			MIN	20
t <sub>th</sub>	Mode			MIN	35
	R/W, CS			MIN	35
t <sub>plh</sub>	SER/Q15			MIN	0
	Y0-Y15			MIN	0
t <sub>phl</sub>	Mode			MIN	0
t <sub>plh</sub>	STRCLR	Y0-Y15		MAX	40
t <sub>phl</sub>	MODE/ STRCLK	Y0-Y15		MAX	45
					45
t <sub>plh</sub>	SH CLK	SER/Q15		MAX	33
					40

UNIT fmax : MHz other : ns

## 16-BIT SHIFT REGISTERS

- 16-Bit Parallel-In, Serial-Out Shift Register
- Performs Parallel-to-Serial Conversion

Logic Diagram



† When PE is active, data synchronously parallel loaded into the shift registers form the 16 P inputs and no shifting takes place.

FUNCTION TABLE

INPUTS				SER/ Q15	OPERATION
CS	R/W	MODE	CLK		
H	X	X	X	Z	Do nothing
L	L	X	↓	Z	Shift and write (serial load)
L	H	L	↓	Q14n	Shift and read
L	H	H	↓	P15	parallel load

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER		MAX or MIN	LS	UNIT
ICC		MAX	40	mA
I <sub>OH</sub>	SER/Q15	MAX	-2.6	mA
	P0-P15	MAX	-0.4	mA
I <sub>OL</sub>	SER/Q15	MAX	24	mA
	P0-P15	MAX	8	mA

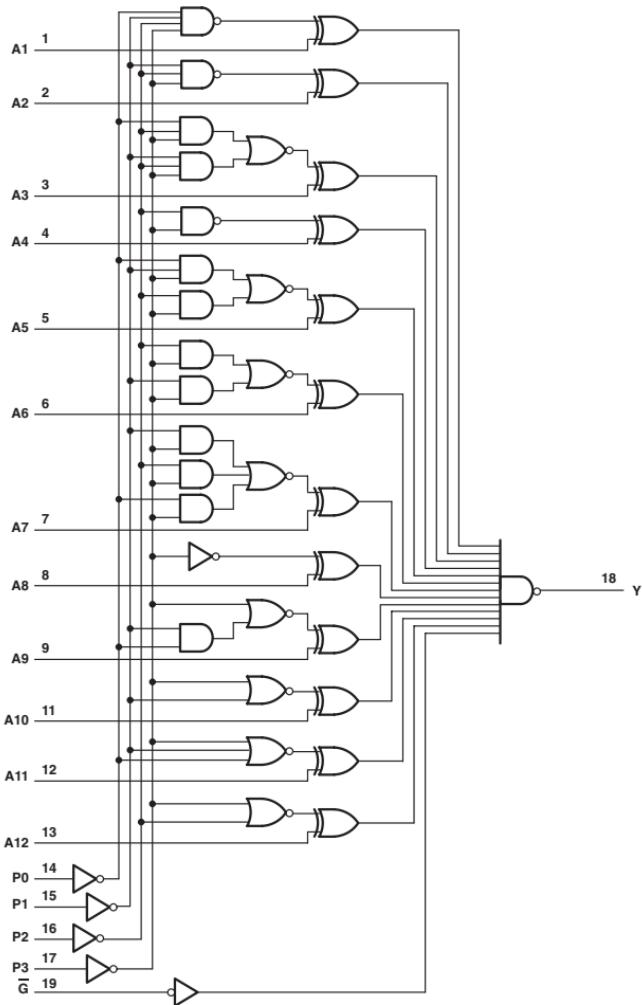
TIMING REQUIREMENTS AND SWITCHING CHARACTERISTICS

PARAMETER		INPUT	OUTPUT	MAX or MIN	LS
t <sub>max</sub>				MIN	20
t <sub>w</sub>	CLK			MIN	20
	CLR				20
t <sub>su</sub>	SER/Q15			MIN	20
	P0-P15				20
t <sub>h</sub>	Mode				35
	R/W, CS				35
t <sub>PLH</sub>	SER/Q15			MIN	0
	P0-P15				0
t <sub>PHL</sub>	Mode			MIN	0
					33
t <sub>ZH</sub>		CLK	SER/Q15	MAX	40
t <sub>ZL</sub>		CS, R/W	SER/Q15	MAX	45
t <sub>HZ</sub>		CS, R/W	SER/Q15	MAX	45
t <sub>LZ</sub>		CS, R/W	SER/Q15	MAX	40

UNIT fmax : MHz other : ns

**12-BIT ADDRESS COMPARATOR**

- 12-Bit Address Comparator with Enable

**Logic Diagram**

FUNCTION TABLE

<b>G</b>	INPUTS												<b>OUTPUT</b>				
	P3	P2	P1	P0	A1	A2	A3	A4	A5	A6	A7	A8	A9	A10	A11	A12	Y
L	L	L	L	L	H	H	H	H	H	H	H	H	H	H	H	L	
L	L	L	L	H	L	H	H	H	H	H	H	H	H	H	H	L	
L	L	L	H	L	L	L	H	H	H	H	H	H	H	H	H	L	
L	L	L	H	H	L	L	H	H	H	H	H	H	H	H	H	L	
L	L	H	L	L	L	L	H	H	H	H	H	H	H	H	H	L	
L	L	H	L	H	L	L	L	L	H	H	H	H	H	H	H	L	
L	L	H	H	L	L	L	L	L	L	H	H	H	H	H	H	L	
L	L	H	H	H	L	L	L	L	L	H	H	H	H	H	H	L	
L	H	L	L	L	L	L	L	L	L	L	L	H	H	H	H	L	
L	H	L	L	H	L	L	L	L	L	L	L	L	H	H	H	L	
L	H	L	H	L	L	L	L	L	L	L	L	L	L	H	H	L	
L	H	H	L	L	L	L	L	L	L	L	L	H	H	H	H	L	
L	H	H	L	H	L	L	L	L	L	L	L	L	H	H	H	L	
L	H	H	H	L	L	L	L	L	L	L	L	L	L	L	L	L	
L					All other combinations												H
H					Any combination												H

## ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	ALS	SN74 HC	UNIT
I <sub>CC</sub>	MAX	28	0.08	mA
I <sub>OH</sub>	MAX	-2.6	-4	mA
I <sub>OL</sub>	MAX	24	4	mA

## SWITCHING CHARACTERISTICS

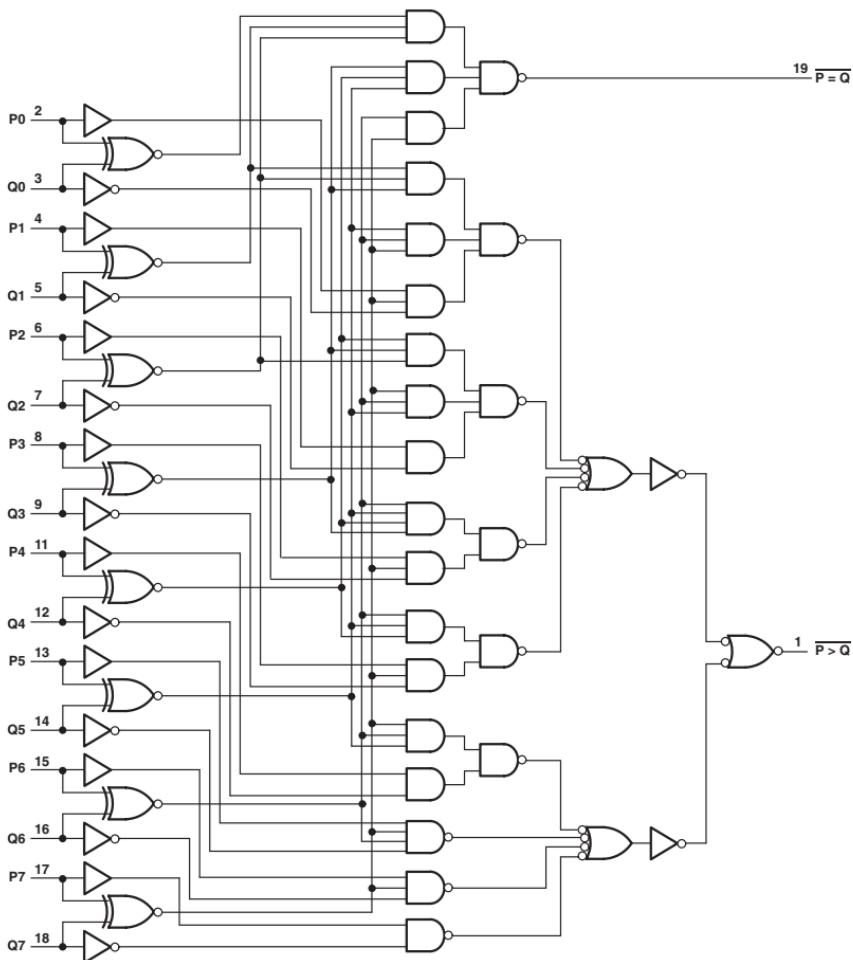
PARAMETER	INPUT	OUTPUT	MAX or MIN	ALS	SN74 HC
I <sub>PLH</sub>	Any P	Y	MAX	25	375
I <sub>PHL</sub>				35	375
I <sub>PLH</sub>	Any A	Y	MAX	22	78
I <sub>PHL</sub>				30	78
I <sub>PLH</sub>	G	Y	MAX	13	31
I <sub>PHL</sub>				25	31

UNIT: ns

## 8-BIT MAGNITUDE COMPARATORS

- Totem-Pole Outputs
- Hysteresis at P and Q Inputs
- 20k $\Omega$  Pullup Resistors on the Q Inputs

Logic Diagram



FUNCTION TABLE

DATA INPUT P, Q	OUTPUTS	
	P=Q	$\overline{P}=\overline{Q}$
P=Q	L	H
P>Q	H	L
P<Q	H	H

## ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	LS	SN74 HC	UNIT
I <sub>CC</sub>	MAX	70	0.11	mA
I <sub>OH</sub>	MAX	-0.4	-4	mA
I <sub>OL</sub>	MAX	24	4	mA

## SWITCHING CHARACTERISTICS

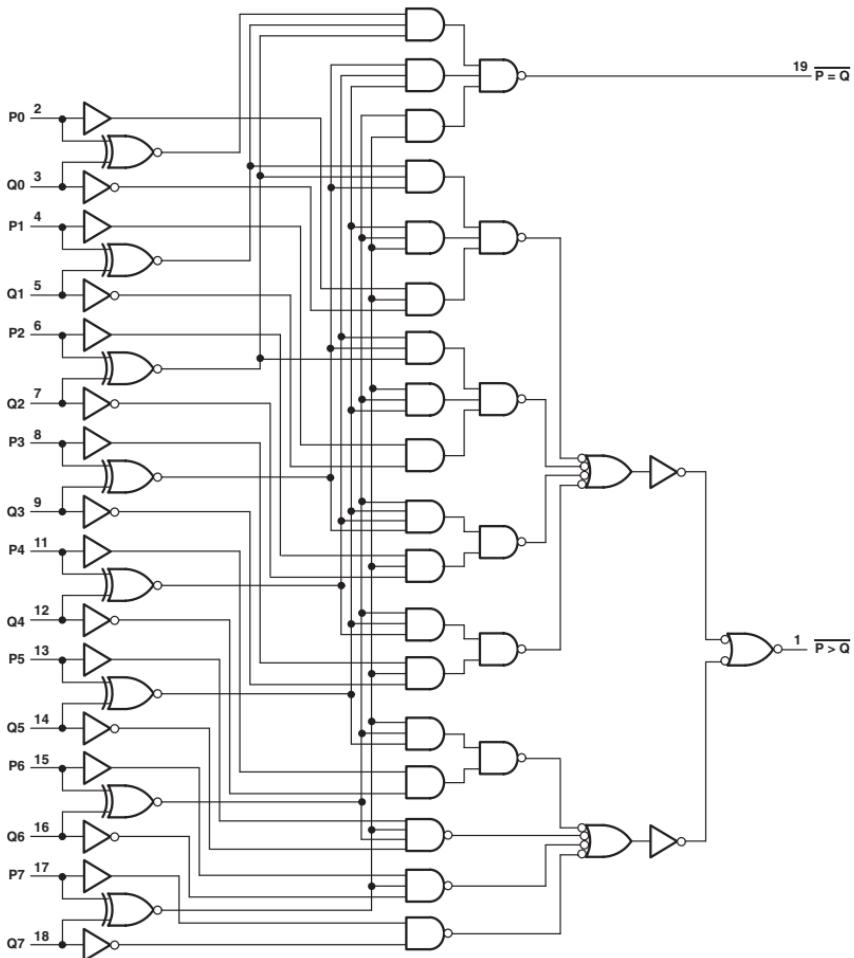
PARAMETER	INPUT	OUTPUT	MAX or MIN	LS	SN74 HC
t <sub>PLH</sub>	P	$\overline{P} = \overline{Q}$	MAX	25	69
				25	69
t <sub>PHL</sub>	Q	$\overline{P} = \overline{Q}$	MAX	25	69
				25	69
t <sub>PLH</sub>	P	$\overline{P} > \overline{Q}$	MAX	30	69
				30	69
t <sub>PHL</sub>	Q	$\overline{P} > \overline{Q}$	MAX	30	69
				30	69

UNIT: ns

## 8-BIT MAGNITUDE COMPARATORS

- Totem-Pole Outputs
- Hysteresis at P and Q Inputs

Logic Diagram



FUNCTION TABLE

DATA INPUT P, Q	OUTPUTS	
	$\bar{P} = \bar{Q}$	$\bar{P} > \bar{Q}$
$P = Q$	L	H
$P > Q$	H	L
$P < Q$	H	H

## ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	LS	SN74 HC	UNIT
$I_{CC}$	MAX	65	0.08	mA
$I_{OH}$	MAX	-0.4	-4	mA
$I_{OL}$	MAX	24	4	mA

## SWITCHING CHARACTERISTICS

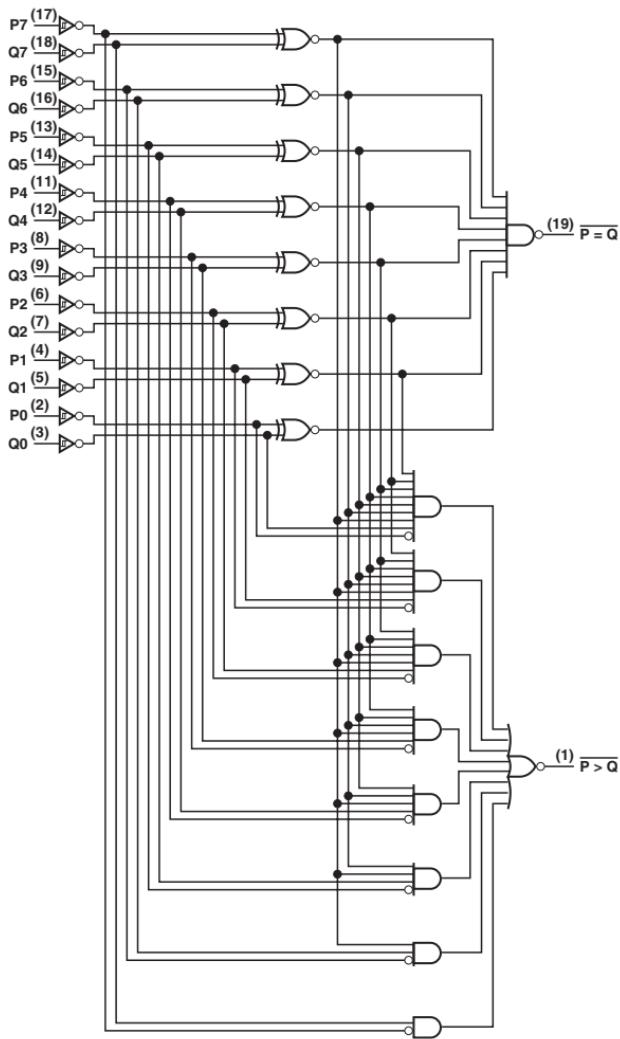
PARAMETER	INPUT	OUTPUT	MAX or MIN	LS	SN74 HC
$t_{PLH}$	P	$\bar{P} = \bar{Q}$	MAX	25	69
				25	69
$t_{PHL}$	Q	$\bar{P} = \bar{Q}$	MAX	25	69
				25	69
$t_{PLH}$	P	$\bar{P} > \bar{Q}$	MAX	30	69
				30	69
$t_{PHL}$	Q	$\bar{P} > \bar{Q}$	MAX	30	69
				30	69

UNIT: ns

## 8-BIT MAGNITUDE/IDENTITY COMPARATORS

- Totem-Pole Outputs
- Hysteresis at P and Q Inputs

Logic Diagram



FUNCTION TABLE

DATA	INPUTS		OUTPUTS	
	ENABLE		$\bar{P}=\bar{Q}$	$\bar{P}>\bar{Q}$
P, Q	$\bar{G}_1$	$\bar{G}_2$		
P=Q	L	L	L	H
P>Q	L	L	H	L
P<Q	L	L	H	H
X	H	H	H	H

## ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	LS	UNIT
$I_{CC}$	MAX	75	mA
$I_{OH}$	MAX	-0.4	mA
$I_{OL}$	MAX	24	mA

## SWITCHING CHARACTERISTICS

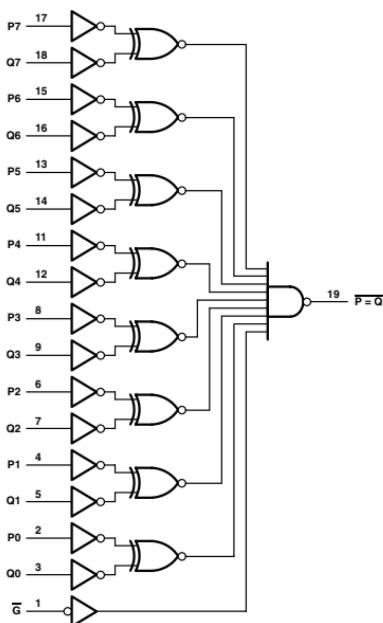
PARAMETER	INPUT	OUTPUT	MAX or MIN	LS
$t_{PLH}$	P	$\bar{P} = \bar{Q}$	MAX	25
				30
$t_{PHL}$	Q	$\bar{P} = \bar{Q}$	MAX	25
				30
$t_{PLH}$	$\bar{G}_1$	$\bar{P} = \bar{Q}$	MAX	20
				30
$t_{PHL}$	P	$\bar{P} > \bar{Q}$	MAX	30
				30
$t_{PLH}$	Q	$\bar{P} > \bar{Q}$	MAX	30
				30
$t_{PLH}$	$\bar{G}_2$	$\bar{P} > \bar{Q}$	MAX	30
				25

UNIT: ns

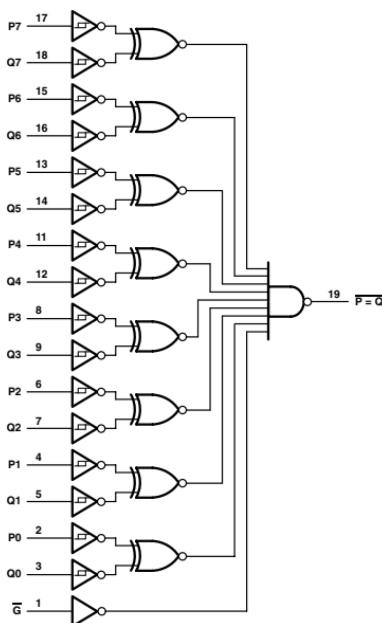
## 8-BIT IDENTITY COMPARATORS

- Totem-Pole Outputs
- Hysteresis at P and Q Inputs

**Logic Diagram  
(SN74ALS)**



**(SN74LS)**



FUNCTION TABLE

INPUTS		OUTPUT
DATA	ENABLE	$\bar{P} = Q$
P, Q	$\bar{G}$	
P=Q	L	L
P>Q	L	H
P<Q	L	H
X	H	H

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	LS	ALS	SN74 HC	CD74 HC	CD74 HCT	UNIT
$I_{CC}$	MAX	65	19	0.08	0.16	0.16	mA
$I_{OH}$	MAX	-0.4	-2.6	-4	-4	-4	mA
$I_{OL}$	MAX	24	24	4	4	4	mA

SWITCHING CHARACTERISTICS

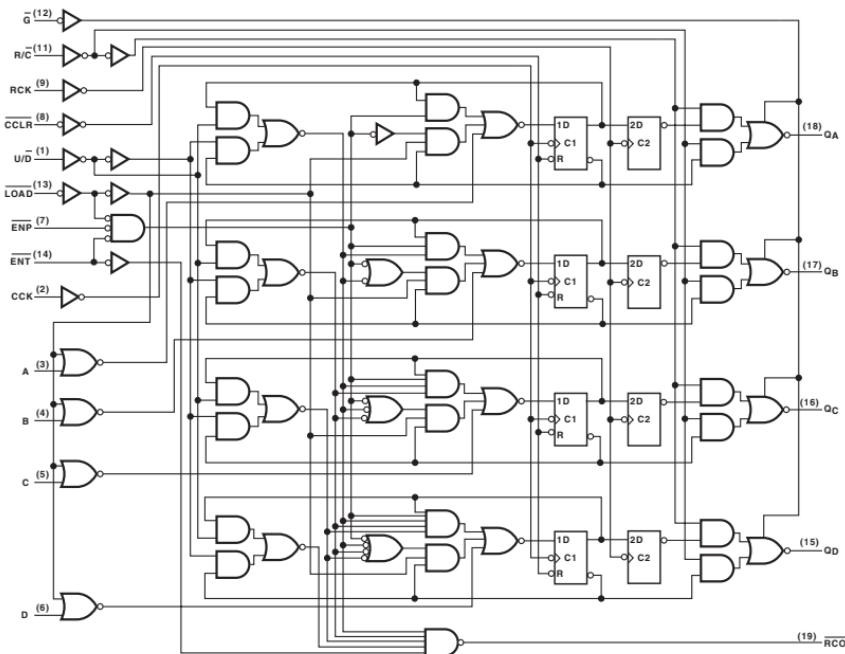
PARAMETER	INPUT	OUTPUT	MAX or MIN	LS	ALS	SN74 HC	CD74 HC	CD74 HCT
$t_{PLH}$	$P$ (CD74: A)	$\bar{P} = \bar{Q}$ (CD74: Y)	MAX	18	12	53	51	51
$t_{PHL}$				23	20	53	51	51
$t_{PLH}$	$Q$ (CD74: B)	$\bar{P} = \bar{Q}$ (CD74: Y)	MAX	18	12	53	51	51
$t_{PHL}$				23	20	53	51	51
$t_{PLH}$	$\bar{G}$ (CD74: E)	$\bar{P} = \bar{Q}$ (CD74: Y)	MAX	18	12	30	36	36
$t_{PHL}$				20	22	30	36	36

UNIT: ns

## SYNCHRONOUS UP/DOWN COUNTERS WITH OUTPUT REGISTERS AND MULTIPLEXED 3-STATE OUTPUTS

- Multiplexed Outputs for Counter or Latched Data
- 3-State Outputs Drive Bus Lines Directly
- Binary Counter, Direct Clear

Logic Diagram



## ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER		MAX or MIN	LS	UNIT
$I_{CC}$		MAX	70	mA
$I_{OH}$	Q	MAX	-2.6	mA
	RCO		-0.4	mA
$I_{OL}$	Q	MAX	24	mA
	RCO		8	mA

## TIMING REQUIREMENTS AND SWITCHING CHARACTERISTICS

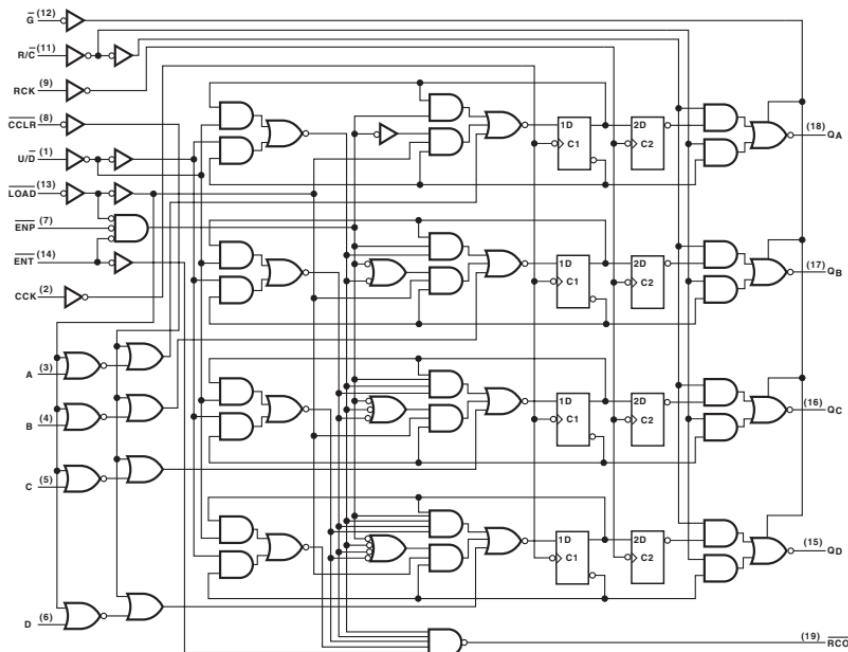
PARAMETER		INPUT	OUTPUT	MAX or MIN	LS
$t_{W}$	CCK			MIN	25
	RCK				25
$t_{SU}$	A thru D			MIN	30
	$\overline{ENT}$ , $\overline{ENP}$				30
$t_{D}$	U/D			MIN	35
					0
$t_{PLH}$		CCK $\uparrow$	$\overline{RCO}$	MAX	40
$t_{PHL}$					40
$t_{PLH}$		$\overline{ENT}$	$\overline{RCO}$	MAX	20
$t_{PHL}$					20
$t_{PLH}$		CCK $\downarrow$	Q	MAX	20
$t_{PHL}$					25
$t_{PLH}$		$RCK \downarrow$	Q	MAX	20
$t_{PHL}$					25
$t_{PLH}$		$\overline{CCLR} \downarrow$	Q	MAX	40
$t_{PLH}$		R / $\overline{C}$	Q	MAX	25
$t_{PHL}$					25

UNIT: ns

## SYNCHRONOUS UP/DOWN COUNTERS WITH OUTPUT REGISTERS AND MULTIPLEXED 3-STATE OUTPUTS

- Multiplexed Outputs for Counter or Latched Data
- 3-State Outputs Drive Bus Lines Directly
- Binary Counter, Synchronous Clear

**Logic Diagram**



## ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER		MAX or MIN	LS	UNIT
I <sub>CC</sub>		MAX	70	mA
I <sub>OH</sub>	Q	MAX	-2.6	mA
	RCO	MAX	-0.4	mA
I <sub>OL</sub>		MAX	24	mA
I <sub>OL</sub>	Q	MAX	8	mA
	RCO	MAX	8	mA

## TIMING REQUIREMENTS AND SWITCHING CHARACTERISTICS

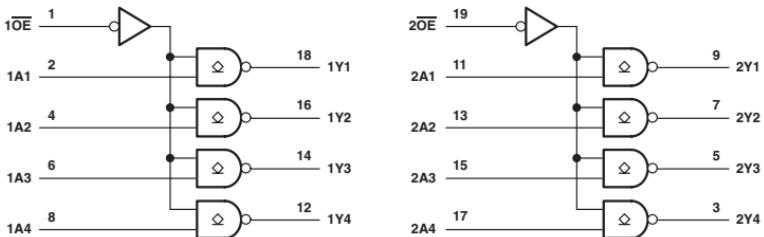
PARAMETER		INPUT	OUTPUT	MAX or MIN	LS
<i>t</i> <sub>W</sub>	CCK			MIN	25
	RCK				25
	A thru D				30
	<u>ENT</u> , <u>ENP</u>			MIN	30
	<u>U/D</u>				35
	<u>CCLR</u>				30
	<u>t</u> <sub>H</sub>			MIN	0
	<u>t</u> <sub>PLH</sub>	CCK ↑	RCO	MAX	40
	<u>t</u> <sub>PHL</sub>				40
	<u>t</u> <sub>PLH</sub>	ENT	RCO	MAX	20
<u>t</u> <sub>PLH</sub>	CCK ↑	Q	MAX		20
					25
	RCK ↑	Q	MAX		20
					25
	R/C	Q	MAX		25

UNIT: ns

## OCTAL BUFFER/DRIVER WITH OPEN-COLLECTOR OUTPUTS

- Eliminate the Need for 3-State Overlap Protection
- pnp Inputs Reduce dc Loading
- Open-Collector Versions of SN74AS240A

Logic Diagram



## ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	AS	SN74 BCT	UNIT
I <sub>CC</sub>	MAX	80	86	mA
V <sub>OH</sub>	MAX	5.5	5.5	V
I <sub>OL</sub>	MAX	64	64	mA

## SWITCHING CHARACTERISTICS

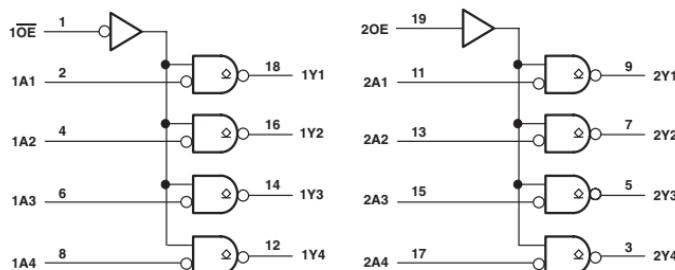
PARAMETER	INPUT	OUTPUT	MAX or MIN	AS	SN74 BCT
t <sub>PLH</sub>	A	Y	MAX	19	11.3
t <sub>PHL</sub>				6	4.2
t <sub>PLH</sub>	OE	Y	MAX	19.5	16.5
t <sub>PHL</sub>				7.5	10.3

UNIT:ns

## OCTAL BUFFER/DRIVER WITH OPEN-COLLECTOR OUTPUTS

- Eliminate the Need for 3-State Overlap Protection
- pnp Inputs Reduce dc Loading
- Open-Collector Versions of SN74AS241

Logic Diagram



## ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	AS	SN74 BCT	SN64 BCT	UNIT
I <sub>CC</sub>	MAX	95	77	77	mA
V <sub>OH</sub>	MAX	5.5	5.5	5.5	V
I <sub>OL</sub>	MAX	64	64	64	mA

## SWITCHING CHARACTERISTICS

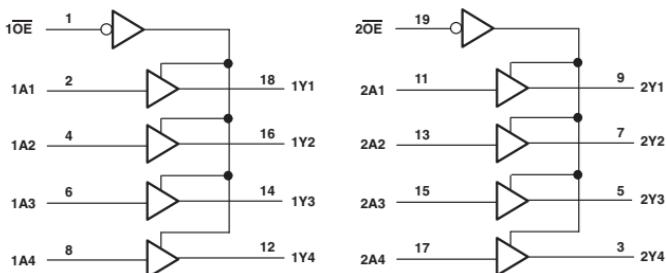
PARAMETER	INPUT	OUTPUT	MAX or MIN	AS	SN74 BCT	SN64 BCT
t <sub>PLH</sub>	A	Y	MAX	18.5	10.1	10.1
t <sub>PHL</sub>				6	6.6	6.6
t <sub>PLH</sub>	1OE	1Y	MAX	20	19.7	19.7
t <sub>PHL</sub>				7	6.9	6.9
t <sub>PLH</sub>	2OE	2Y	MAX	21	18	18
t <sub>PHL</sub>				7.5	8.5	8.5

UNIT:ns

## OCTAL BUFFERS/DRIVERS WITH OPEN-COLLECTOR OUTPUTS

- Open-Collector Outputs Drive Bus Lines or Buffer Memory Address Registers
- pnp Inputs Reduce dc Loading
- Open-Collector Versions of SN74ALS244 and SN74AS244

Logic Diagram



## ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	ALS	AS	SN74 BCT	UNIT
$I_{CC}$	MAX	19	94	76	mA
$V_{OH}$	MAX	5.5	5.5	5.5	V
$I_{OL}$	MAX	24	64	64	mA

## SWITCHING CHARACTERISTICS

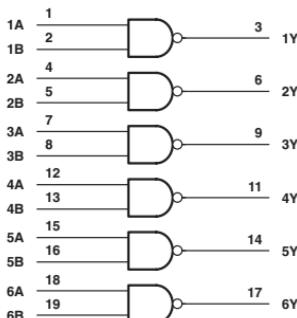
PARAMETER	INPUT	OUTPUT	MAX or MIN	ALS	AS	SN74 BCT
$t_{PLH}$	A	Y	MAX	15	18.5	10
$t_{PHL}$				12	6	7.2
$t_{PLH}$	$\overline{OE}$	Y	MAX	16	18.5	17.5
$t_{PHL}$				13	7	9.9

UNIT:ns

## HEX 2-INPUT NAND DRIVERS

- $Y = \overline{A \cdot B}$
- High Capacitive-Drive Capability

Logic Diagram



FUNCTION TABLE

INPUTS		OUTPUT
A	B	Y
H	H	L
L	X	H
X	L	H

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	ALS	AS	SN74 HC	UNIT
I <sub>CC</sub>	MAX	12	27	0.08	mA
I <sub>OH</sub>	MAX	-15	-48	-6	mA
I <sub>OL</sub>	MAX	24	48	6	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	ALS	AS	SN74 HC
t <sub>PLH</sub>	A, B	Y	MAX	7	4	25
t <sub>PHL</sub>			MAX	8	4	25

UNIT:ns

## 805

### HEX 2-INPUT NOR DRIVERS

- $Y = \overline{A} + \overline{B}$
- High Capacitive-Drive Capability

**FUNCTION TABLE**

INPUTS	OUTPUT	
A	B	Y
H	X	L
X	H	L
L	L	H

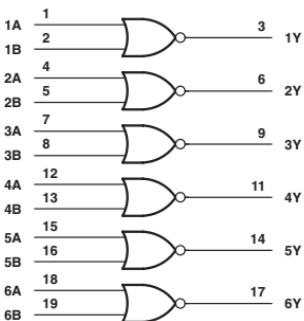
ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	ALS	AS	SN74 HC	UNIT
$I_{CC}$	MAX	14	32	0.08	mA
$I_{OH}$	MAX	-15	-48	-6	mA
$I_{OL}$	MAX	24	48	6	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	ALS	AS	SN74 HC
$t_{PLH}$	A, B	Y	MAX	7	4.3	24
$t_{PHL}$			MAX	8	4.3	24

UNIT:ns

**Logic Diagram**

## 808

### HEX 2-INPUT AND DRIVERS

- $Y = A + B$
- High Capacitive-Drive Capability

**FUNCTION TABLE**

INPUTS	OUTPUT	
A	B	Y
H	H	H
L	X	L
X	L	L

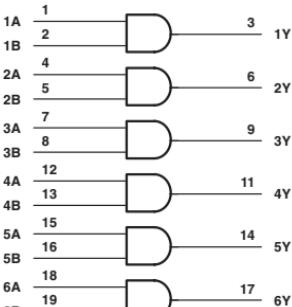
ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	AS	SN74 HC	UNIT
$I_{CC}$	MAX	33	0.08	mA
$I_{OH}$	MAX	-48	-6	mA
$I_{OL}$	MAX	48	6	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	AS	SN74 HC
$t_{PLH}$	A, B	Y	MAX	6	25
$t_{PHL}$			MAX	6	25

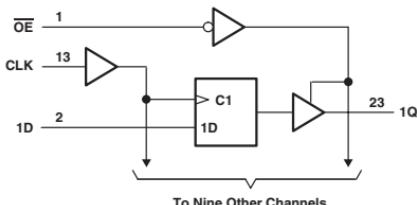
UNIT:ns

**Logic Diagram**

## 10-BIT BUS-INTERFACE FLIP FLOPS WITH 3-STATE OUTPUTS

- Outputs Have Undershoot-Protection Circuitry
- Power-Up High-Impedance State

Logic Diagram



FUNCTION TABLE

INPUTS			OUTPUT
OE	CLK	D	Q
L	↑	H	H
L	↑	L	L
L	L	X	Q <sub>0</sub>
H	X	X	Z

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	AS	ABT	LVC 3V	UNIT
I <sub>CC</sub>	MAX	113	38	0.01	mA
I <sub>OH</sub>	MAX	-24	-32	-24	mA
I <sub>OL</sub>	MAX	48	64	24	mA

TIMING REQUIREMENTS AND SWITCHING CHARACTERISTICS

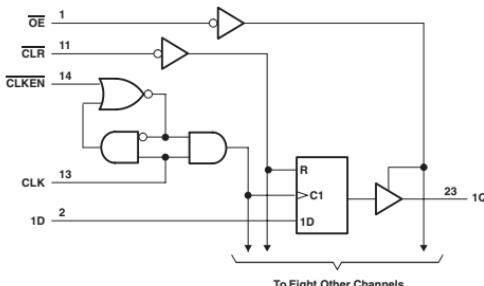
PARAMETER	INPUT	OUTPUT	MAX or MIN	AS	ABT	LVC 3V
t <sub>w</sub>	High		MIN	8	2.9	3.3
	Low		MIN	8	3.8	3.3
t <sub>tr</sub>			MIN	6	2.1	1.9
			MIN	0	1.3	1.5
t <sub>PLH</sub>	CLK	Q	MAX	7.5	6.2	7.3
t <sub>PHL</sub>				13	6.7	7.3
t <sub>PZH</sub>	$\overline{OE}$	Q	MAX	11	5.8	7.6
t <sub>PZL</sub>				12	6.3	7.6
t <sub>PHZ</sub>	$\overline{OE}$	Q	MAX	8	6.7	6.2
t <sub>PLZ</sub>				8	6.5	6.2

UNIT: ns

## 9-BIT BUS-INTERFACE FLIP-FLOPS WITH 3-STATE OUTPUTS

- Functionally Equivalent to AMD's AM29823 and AM29824
- Outputs Have Undershoot-Protection Circuitry
- Power-Up High-Impedance State

Logic Diagram



FUNCTION TABLE

INPUTS					OUTPUT
$\overline{OE}$	$\overline{CLR}$	$\overline{CLKEN}$	$CLK$	$D$	$Q$
L	L	X	X	X	L
L	H	L	$\uparrow$	H	H
L	H	L	$\uparrow$	L	L
L	H	H	X	X	$Q_0$
H	X	X	X	X	Z

## ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	AS	ABT	LVC 3V	UNIT
$I_{CC}$	MAX	103	38	0.01	mA
$I_{OH}$	MAX	-24	-32	-24	mA
$I_{OL}$	MAX	48	64	24	mA

## TIMING REQUIREMENTS AND SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	AS	ABT	LVC 3V
$t_{w}$	$\overline{CLR}$ 'L'		MIN	6.5	5.5	3.3
	$\overline{CLK}$ 'H'			8	2.9	3.3
	$\overline{CLK}$ 'L'			8	3.8	3.3
$t_{su}$	$\overline{CLR}$ inactive		MIN	8	2.5	1
	DATA			6	2.1	1.3
	$\overline{CLKEN}$ 'H'			7.5	2	-
$t_h$	$\overline{CLKEN}$ 'L'		MIN	7.5	3.3	1.8
	DATA			-	1.3	2
	$\overline{CLKEN}$ 'H'			-	1	-
$t_{ph}$	$\overline{CLKEN}$ 'L'		MIN	0	2	1.3
	CLK			7.5	6.8	6
	$\overline{CLR}$			13	6.7	8
$t_{phl}$	$\overline{CLKEN}$		MAX	15.5	7.1	7.9
	Q			11	6	7.2
	$\overline{OE}$			12	6.5	7.2
$t_{pz}$	$\overline{OE}$		MAX	8	7.5	6
	Q			8	6.9	6

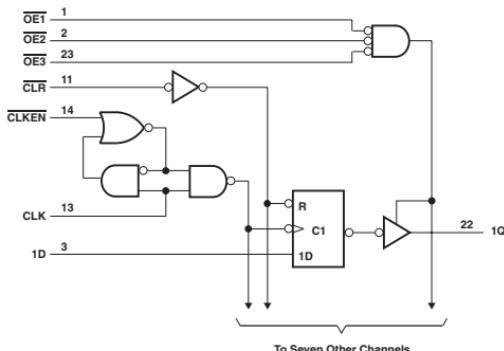
UNIT: ns

■: OBSOLETED or NOT RECOMMENDED NEW DESIGNS

## 8-BIT BUS-INTERFACE FLIP-FLOPS WITH 3-STATE OUTPUTS

- Improved  $I_{OH}$  Specifications (Max: -24mA)
- Outputs Have Undershoot-Protection Circuitry
- Power-Up High-Impedance State

Logic Diagram



FUNCTION TABLE

INPUTS				OUTPUT
OE	CLR	CLKEN	CLK	Q
L	L	X	X	L
L	H	L	↑	H
L	H	L	↑	L
L	H	H	X	X
H	X	X	X	Z

## ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	AS	UNIT
$I_{CC}$	MAX	95	mA
$I_{OH}$	MAX	-24	mA
$I_{OL}$	MAX	48	mA

## TIMING REQUIREMENTS AND SWITCHING CHARACTERISTICS

PARAMETER		INPUT	OUTPUT	MAX or MIN	AS
$t_{W}$	CLR "L"			MIN	4
	CLK "H"				8
	CLK "L"				8
	CLR			MIN	8
	DATA				6
	CLKEN				6
$t_b$				MIN	0
$t_{PLH}$		CLK	Q	MAX	7.5
$t_{PHL}$					13
$t_{PHL}$		CLR	Q	MAX	15.5
$t_{PZH}$		$\overline{OE}$	Q	MAX	11
$t_{PZL}$					12
$t_{PHZ}$		$\overline{OE}$	Q	MAX	8
$t_{PLZ}$					8

UNIT: ns

## 10-BIT BUFFERS/DRIVERS WITH 3-STATE OUTPUTS

- 3-State Outputs Drive Bus Lines or Buffer Memory Address Registers
- 74AC11xxx: Product Available in Reduced-Noise Advanced CMOS (11000 Series)
- 74ACT11xxx: Product Available in Reduced-Noise Advanced CMOS (11000 Series)

FUNCTION TABLE

INPUTS	OUTPUT		
OE1	OE2	A	Y
L	L	H	H
L	L	L	L
X	H	X	Z
H	X	X	Z

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	ABT	AC 11	ACT 11	LVC 3V	UNIT
ICC	MAX	40	0.08	0.08	0.01	mA
IOH	MAX	-32	-24	-24	-24	mA
IOL	MAX	64	24	24	24	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	ABT	AC 11	ACT 11	LVC 3V
t <sub>PLH</sub>	A	Y	MAX	4.8	8.7	9.2	6.7
t <sub>PHL</sub>				4.7	9.7	11.2	6.7
t <sub>PZH</sub>	OE	Y	MAX	5.9	9.7	11.3	7.3
t <sub>PZL</sub>				6.9	13	14	7.3
t <sub>PHZ</sub>	OE	Y	MAX	6.8	9.1	12	6.7
t <sub>PZL</sub>				6.9	8.8	11.6	6.7

UNIT: ns

## 10-BIT BUFFERS/DRIVERS WITH 3-STATE OUTPUTS

- 3-State Outputs Drive Bus Lines or Buffer Memory Address Registers
- 74AC11xxx: Product Available in Reduced-Noise Advanced CMOS (11000 Series)
- 74ACT11xxx: Product Available in Reduced-Noise Advanced CMOS (11000 Series)

FUNCTION TABLE

INPUTS	OUTPUT		
OE1	OE2	A	Y
L	L	H	L
L	L	L	H
H	X	X	Z
X	H	X	Z

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	AC 11	ACT 11	LVC 3V	UNIT
ICC	MAX	0.08	0.08	0.01	mA
IOH	MAX	-24	-24	-24	mA
IOL	MAX	24	24	24	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	AC 11	ACT 11	LVC 3V
t <sub>PLH</sub>	A	Y	MAX	9.5	10.2	6.7
t <sub>PHL</sub>				10.4	11.7	6.7
t <sub>PZH</sub>	OE	Y	MAX	10.7	12.1	7.3
t <sub>PZL</sub>				13.2	14.7	7.3
t <sub>PHZ</sub>	OE	Y	MAX	9.6	12.3	6.7
t <sub>PZL</sub>				9.2	11.7	6.7

UNIT: ns

## HEX 2-INPUT OR DRIVERS

- $Y = A + B$
- High Capacitive-Drive Capability

FUNCTION TABLE

INPUTS	OUTPUT	
A	B	Y
H	X	H
X	H	H
L	L	L

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

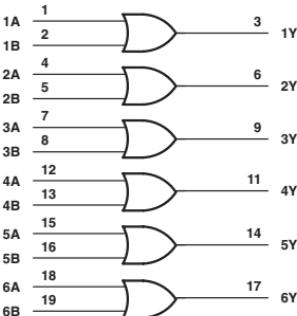
PARAMETER	MAX or MIN	ALS	AS	SN74 HC	UNIT
$I_{CC}$	MAX	16	36	0.08	mA
$I_{OH}$	MAX	-15	-48	-6	mA
$I_{OL}$	MAX	24	48	6	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	ALS	AS	SN74 HC
$t_{PLH}$	A, B	Y	MAX	9	6.3	25
$t_{PHL}$			MAX	8	6.3	25

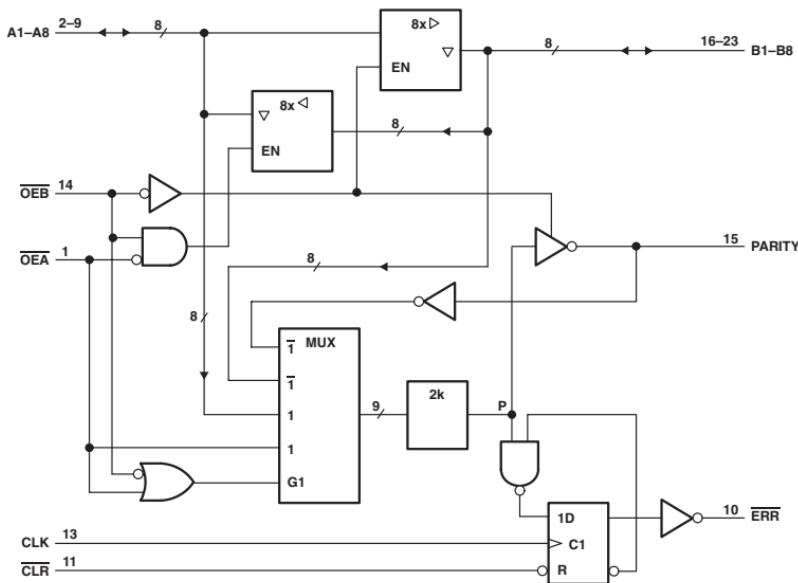
UNIT: ns

## Logic Diagram



## 8-BIT TO 9-BIT PARITY BUS TRANSCEIVERS

Logic Diagram



FUNCTION TABLE

INPUTS						OUTPUTS AND I/O				FUNCTION
OEB	OE <sub>A</sub>	CLR	CLK	A <sub>I</sub> Σ OF H's	B <sub>I</sub> Σ OF H's	A	B	PARITY	ERR	
L	H	X	X	Odd Even	NA	NA	A	L H	NA	A data to B bus and generate parity
H	L	H	↑	NA	Odd Even	B	NA	NA	H L	B data to A bus and check parity
X	X	L	X	X	X	X	NA	NA	H	Check error flag register
H	H	H	↑	H No ↑ L No ↑ H ↑ H ↑	X	Z	Z	Z	H H H L	Isolation
L	L	X	X	Odd Even	NA	NA	A	H L	NA	A data to B bus and generate inverted parity

INPUTS	INTERNAL TO DEVICE	OUTPUT PRE-STATE	OUTPUT	FUNCTION
CLR	CLK	POINT P	ERR <sub>n-1†</sub>	ERR
H	↑	H	H	H
H	↑	X	L	H
H	↑	L	X	L
L	X	X	X	Clear

† The state of ERR before any changes at CLR, CLK, or point P

## ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	ABT	UNIT
I <sub>CC</sub>	MAX	38	mA
I <sub>OH</sub>	MAX	-32	mA
I <sub>OL</sub>	MAX	64	mA

## SWITCHING CHARACTERISTICS

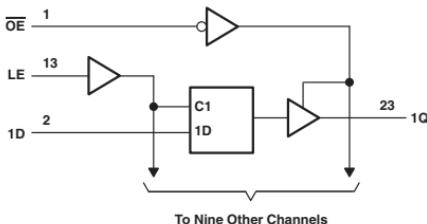
PARAMETER	INPUT	OUTPUT	MAX or MIN	ABT
I <sub>PLH</sub>	A or B	B or A	MAX	5.3
I <sub>PHL</sub>				5.3
I <sub>PLH</sub>	A	PARITY	MAX	11.2
I <sub>PHL</sub>				11
I <sub>PZH</sub>	OE	PARITY	MAX	10.5
I <sub>PZL</sub>				10
I <sub>PLH</sub>	CLR	ERR	MAX	5.2
I <sub>PHL</sub>				6.2
I <sub>PZH</sub>	OE	A,B, or PARITY	MAX	6.5
I <sub>PZL</sub>				6.5
I <sub>PHZ</sub>	OE	A,B, or PARITY	MAX	7.9
I <sub>PLZ</sub>				8.1

UNIT: ns

## 10-BIT BUS-INTERFACE D-TYPE LATCHES WITH 3-STATE OUTPUTS

- 3-State Buffer-Type Outputs Drive Bus Lines Directly
- Bus-Structured Pinout
- Provide Extra Bus-Driving Latches Necessary for Wider Address/Data Paths or Buses with Parity
- Power-Up High-Impedance State

Logic Diagram



FUNCTION TABLE

INPUTS			OUTPUT	
OE	LE	D	Q	
L	H	H	L	
L	H	L	H	
L	L	X	Q <sub>0</sub>	
H	X	X	Z	

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	ALS	AS	ABT	LVC 3V	UNIT
I <sub>CC</sub>	MAX	62	94	38	0.01	mA
I <sub>OH</sub>	MAX	-2.6	-24	-32	-24	mA
I <sub>OL</sub>	MAX	24	48	64	24	mA

TIMING REQUIREMENTS AND SWITCHING CHARACTERISTICS

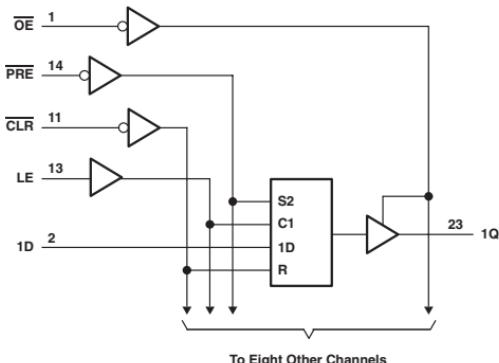
PARAMETER	INPUT	OUTPUT	MAX or MIN	ALS	AS	ABT	LVC 3V
t <sub>w</sub>	High	Q	MAX	20	4	3.3	3.3
t <sub>su</sub>				10	2.5	2.5	2.1
t <sub>sl</sub>				10	2.5	1.5	2.1
t <sub>h</sub>				5	2.5	1.5	1
t <sub>PZH</sub>	D	Q	MAX	13	6.5	6.2	6.7
t <sub>PHL</sub>				13	10.5	6.2	6.7
t <sub>PLH</sub>	LE	Q	MAX	21	12	6.5	7.6
t <sub>PLH</sub>				26	12	6.7	7.6
t <sub>PZL</sub>	OE	Q	MAX	12	14	5.3	7.2
t <sub>PZL</sub>				12	16	6.3	7.2
t <sub>PHZ</sub>	OE	Q	MAX	10	8	7.1	5.9
t <sub>PLZ</sub>				12	8	6.5	5.9

UNIT: ns

## 9-BIT BUS-INTERFACE D-TYPE LATCHES WITH 3-STATE OUTPUTS

- 3-State Buffer-Type Outputs Drive Bus Lines Directly
- Bus-Structured Pinout
- Provides Extra Bus-Driving Latches Necessary for Wider Address/Data Paths or Buses with Parity
- Power-Up High-Impedance State

Logic Diagram



FUNCTION TABLE

INPUTS					OUTPUT
PRE	CLR	OE	LE	D	
L	H	L	X	X	H
H	L	L	X	X	L
L	L	L	X	X	H
H	H	L	H	L	L
H	H	L	H	H	H
H	H	L	L	X	Q <sub>0</sub>
X	X	H	X	X	Z

## ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

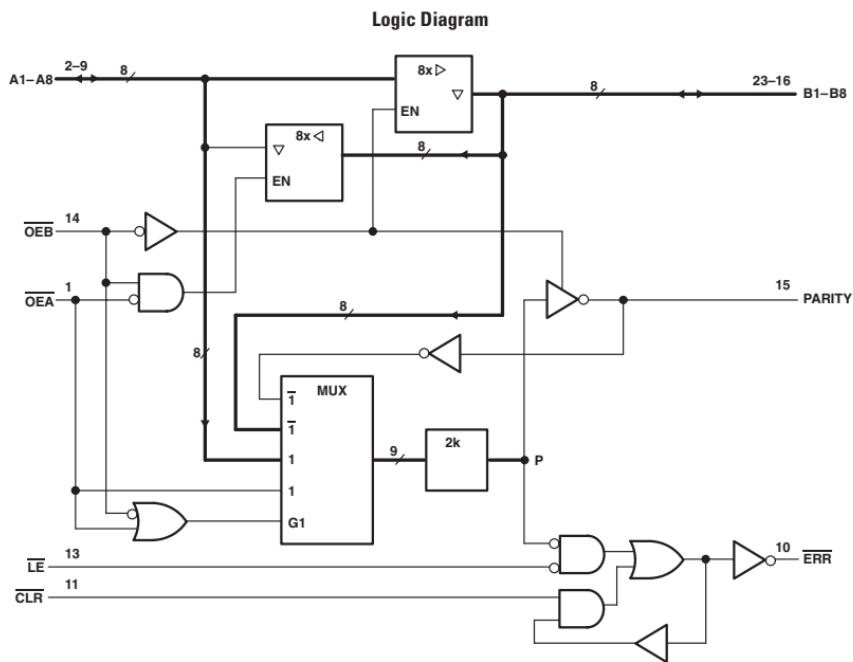
PARAMETER	MAX or MIN	ALS	AS	ABT	UNIT
I <sub>CC</sub>	MAX	67	92	34	mA
I <sub>OH</sub>	MAX	-2.6	-24	-32	mA
I <sub>OL</sub>	MAX	24	48	64	mA

## TIMING REQUIREMENTS AND SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	ALS	AS	ABT
t <sub>w</sub>	CLR "L"		MIN	35	4	5.5
	PRE "L"			35	4	4.5
	LE "H"			20	4	-
	LE "L"			-	4	3.4
t <sub>su</sub>	LE "L"		MIN	10	2.5	2.5
	LE "H"			10	2.5	3
	PRE inactive			-	15	1.6
	CLR inactive			-	14	2
t <sub>h</sub>	LE "L"		MIN	5	2.5	1
	LE "H"			5	2.5	1.5
t <sub>PLH</sub>	D	Q	MAX	13	6.5	6.7
t <sub>PHL</sub>				18	9	7.2
t <sub>PLH</sub>	LE	Q	MAX	21	12	7.2
t <sub>PHL</sub>				26	12	6.9
t <sub>PLH</sub>	CLR	Q	MAX	-	-	7.1
t <sub>PHL</sub>				23	13	8
t <sub>PLH</sub>	PRE	Q	MAX	22	10	7.4
t <sub>PHL</sub>				-	-	7.2
t <sub>PZH</sub>	OE	Q	MAX	12	10.5	5.7
t <sub>PZL</sub>				14	13.5	6.5
t <sub>PZH</sub>	OE	Q	MAX	10	8	6.8
t <sub>PZL</sub>				12	8	5.9

UNIT: ns

## 8-BIT TO 9-BIT PARITY BUS TRANSCEIVERS



FUNCTION TABLE

INPUTS						OUTPUT AND I/Os				FUNCTION
OEB	OE <sub>A</sub>	CLR	LE	A <sub>I</sub> Σ OF H	B <sub>I</sub> Σ OF H	A	B	PARITY	ERR‡	
L	H	X	X	Odd Even	NA	NA	A	L	NA	A data to B bus and generate parity
H	L	H	L	NA	Odd Even	B	NA	NA	H L	B data to A bus and check parity
H	L	H	H	X	X	X	NA	NA	NC	Store error flag
X	X	L	H	X	X	X	NA	NA	H	Clear error flag register
H	H	H	X						NC	
H	H	H	L	L Odd H Even	X	Z	Z	Z	H L	Isolation§ (parity check)
L	L	X	X	Odd Even	NA	NA	A	H L	NA	A data to B bus and generate inverted parity

NA = not applicable, NC = no change, X = don't care

† Summation of high-level inputs includes PARITY along with Bi inputs.

‡ Output states shown assume ERR was previously high.

§ In this mode, ERR (when clocked) shows inverted parity of the A bus.

ERROR-FLAG FUNCTION TABLE

INPUTS	INTERNAL TO DEVICE	OUTPUT PRE-STATE	OUTPUT ERR	FUNCTION
CLR LE	POINT P	ERR <sub>n-1</sub> †		
L L	L H	X	L H	Pass
H L	L X H	X L H	L L H	Sample
L H	X	X	H	Clear
H H	X H	L H	L H	Store

† The state of ERR before changes at CLR, LE, or point P

## ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	ABT	UNIT
I <sub>CC</sub>	MAX	38	mA
I <sub>OH</sub>	MAX	-32	mA
I <sub>OL</sub>	MAX	64	mA

## SWITCHING CHARACTERISTICS

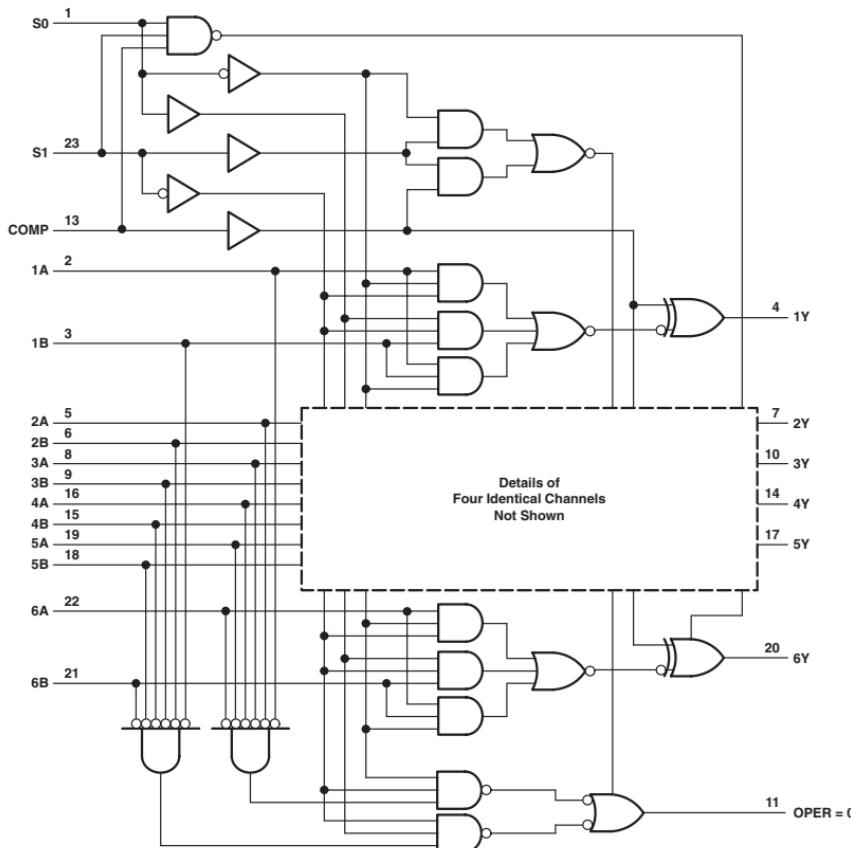
PARAMETER	INPUT	OUTPUT	MAX or MIN	ABT
I <sub>PLH</sub>	A or B	B or A	MAX	5.3
I <sub>PHL</sub>				5.3
I <sub>PLH</sub>	A	PARITY	MAX	11.2
I <sub>PHL</sub>				11
I <sub>PLH</sub>	OE	PARITY	MAX	10.5
I <sub>PHL</sub>				10
I <sub>PLH</sub>	CLR	ERR	MAX	6.2
I <sub>PHL</sub>				6
I <sub>PLH</sub>	LE	ERR	MAX	6.6
I <sub>PHL</sub>				6
I <sub>PLH</sub>	B or RARITY	ERR	MAX	11.7
I <sub>PHL</sub>				12.8
I <sub>PZH</sub>	OE	A or B or PARITY	MAX	6.7
I <sub>PZL</sub>				6.7
I <sub>PHZ</sub>	OE	A or B or PARITY	MAX	7.9
I <sub>PZL</sub>				8.1

UNIT: ns

## HEX 2-TO-1 UNIVERSAL MULTIPLEXERS WITH 3-STATE OUTPUTS

- Select True or Complementary Data
- Perform AND/NAND (Masking) of A or B Operand
- Cascadable to Expand Number of Operands
- Detect Zeros on A or B Operands
- 3-State Outputs Interface Directly with System Bus

Logic Diagram



FUNCTION TABLE

INPUTS			OUTPUTS	
COMP	S1	S0	Y	OPER = 0
L	L	L	A	H = all A inputs L
L	L	H	B	H = all B inputs L
L	H	L	<u>A+B</u>	Z
L	H	H	<u>L</u>	L
H	L	L	<u>A</u>	H = all A inputs L
H	L	H	<u>B</u>	H = all B inputs L
H	H	L	<u>A+B</u>	Z
H	H	H	Z	Z

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER		MAX or MIN	ALS	AS	UNIT
I <sub>CCZ</sub>		MAX	36	135	mA
I <sub>CCL</sub>		MAX	33	175	mA
I <sub>OH</sub>	Y	MAX	-2.6	-15	mA
	OPER = 0	MAX	-2.6	-2	mA
I <sub>OL</sub>	Y	MAX	24	48	mA
	OPER = 0	MAX	24	20	mA

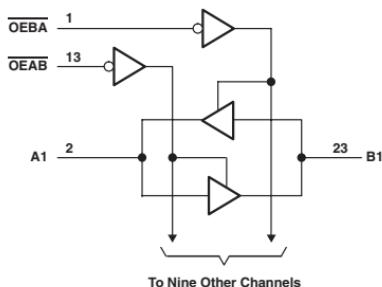
TIMING REQUIREMENTS AND SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	ALS	AS
t <sub>pd</sub>	A or B (COMP = "H")	Y inverting	MAX	14	12
t <sub>pd</sub>	A or B (COMP = "L")	Y non-inverting	MAX	14	10
t <sub>pd</sub>	S0 or S1	Y		33	13
t <sub>pd</sub>	COMP	Y		18	13
t <sub>pd</sub>	A or B	OPER = 0		37	14
t <sub>pd</sub>	S0 to S1	OPER = 0		23	18
t <sub>en</sub>	S0 to S1	Y	MAX	35	12
t <sub>dis</sub>				23	11
t <sub>en</sub>	COMP	Y	MAX	24	12
t <sub>dis</sub>				21	9
t <sub>en</sub>	S0	OPER = 0	MAX	20	12
t <sub>dis</sub>				27	9
t <sub>en</sub>	S1	OPER = 0	MAX	25	12
t <sub>dis</sub>				19	9
t <sub>en</sub>	COMP	OPER = 0	MAX	25	13
t <sub>dis</sub>				20	9

UNIT: ns

## 10-BIT TRANSCEIVERS WITH 3-STATE OUTPUTS

Logic Diagram



FUNCTION TABLE

INPUTS	OPERATION
OEAB OEBA	
L H	A data to B bus
H L	B data to A bus
H H	Isolation
L L	Latch A and B (A = B)

## ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	ABT	LVC 3V	UNIT
$I_{CC}$	MAX	38	0.01	mA
$I_{OH}$	MAX	-32	-24	mA
$I_{OL}$	MAX	64	24	mA

## SWITCHING CHARACTERISTICS

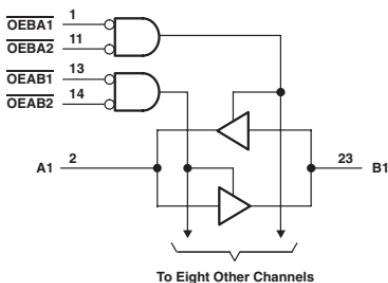
PARAMETER	INPUT	OUTPUT	MAX or MIN	ABT	LVC 3V
$t_{PLH}$	A or B	B or A	MAX	5.2 4.9	6.4 6.4
$t_{PHL}$				5.9 6.9	7 7
$t_{PZH}$	$\overline{OEAB}$ or $\overline{OEBA}$	B or A	MAX	7.5	5.9
$t_{PZL}$				7.1	5.9
$t_{PHZ}$	$\overline{OEAB}$ or $\overline{OEBA}$	B or A	MAX		
$t_{PLZ}$					

UNIT: ns

## 9-BIT BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

## ● 3-State Outputs

Logic Diagram



FUNCTION TABLE

INPUTS				OPERATION
OEAB1	OEAB2	OEBA1	OEBA2	
L	L	L	L	Latch A and B
L	L	H	X	A to B
L	L	X	H	
H	X	L	L	B to A
X	H	L	L	
H	X	H	X	
H	X	X	H	
X	H	X	H	
X	H	H	X	Isolation

## ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	ABT	LVC 3V	UNIT
Icc	MAX	38	0.01	mA
IoH	MAX	-32	-24	mA
IoL	MAX	64	24	mA

## SWITCHING CHARACTERISTICS

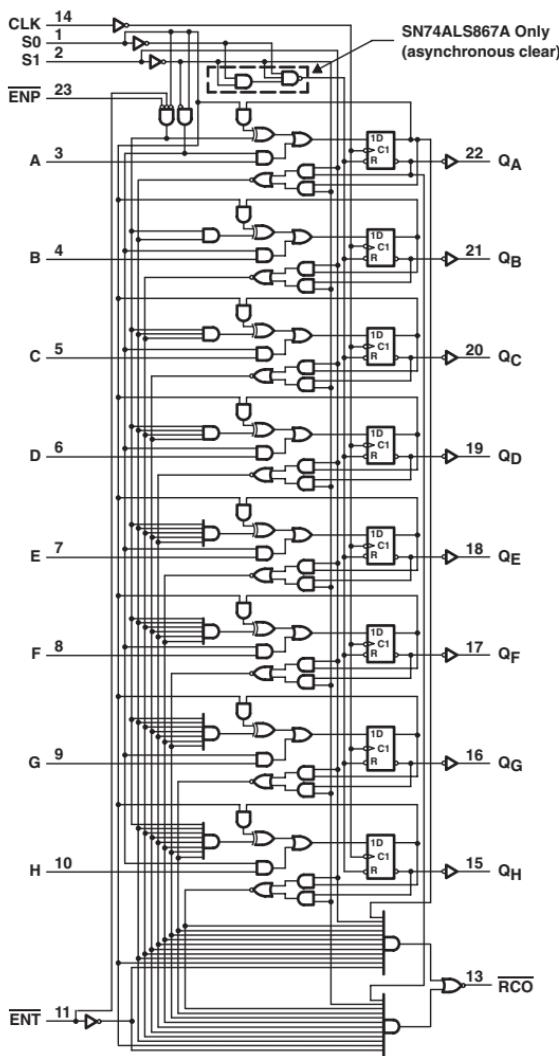
PARAMETER	INPUT	OUTPUT	MAX or MIN	ABT	LVC 3V
tPLH	A or B	B or A	MAX	5.7	6.1
tPHL				3.9	6.1
tPZH	OE	A or B	MAX	5.5	7.2
tPZL				5.4	7.2
tPHZ	OE	A or B	MAX	6.7	6.3
tPLZ				6.9	6.3

UNIT: ns

## SYNCHRONOUS 8-BIT UP/DOWN COUNTERS

- Fully Programmable with Synchronous Counting and Loading
- Asynchronous Clear
- Ripple-Carry Output for n-Bit Cascading

Logic Diagram



**FUNCTION TABLE**

S1	S0	FUNCTION
L	L	Clear
L	H	Count down
H	L	Load
H	H	Count up

**ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS**

PARAMETER	MAX or MIN	ALS	AS	UNIT
I <sub>CC</sub>	MAX	45	195	mA
I <sub>OH</sub>	MAX	-0.4	-2	mA
I <sub>OL</sub>	MAX	8	20	mA

**TIMING REQUIREMENTS AND SWITCHING CHARACTERISTICS**

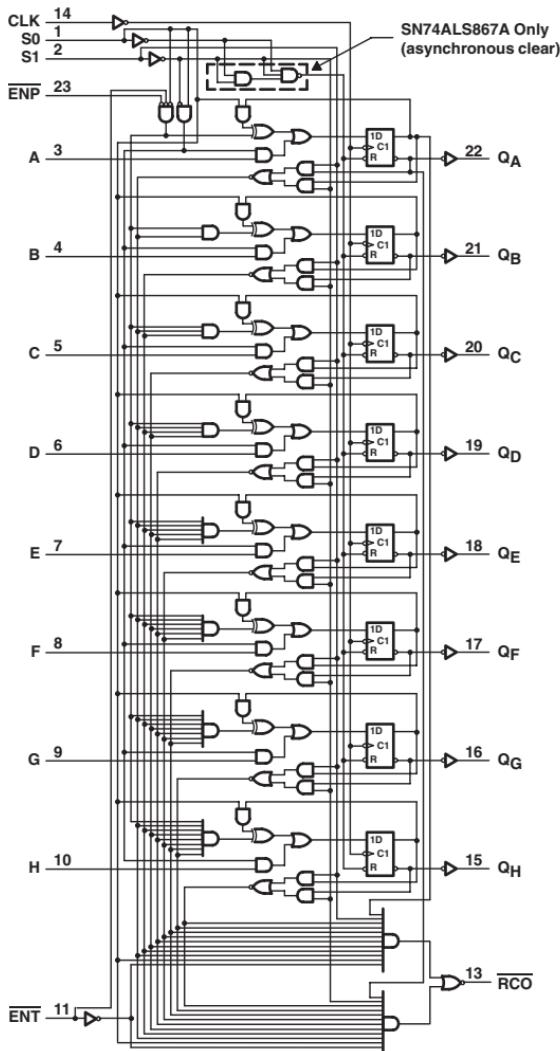
PARAMETER	INPUT	OUTPUT	MAX or MIN	ALS	AS
t <sub>max</sub>			MIN	35	50
t <sub>w</sub>	CLK (clock)		MIN	14	10
	S0 and S1 (clear)			10	10
t <sub>tu</sub>	Data input A-H			10	4
	ENP or ENT			15	8
	S0 low and S1 high (load)			12	10
	S0 and S1 low (clear)			-	10
	S0 high and S1 low (count down)			12	40
	S0 and S1 high (count up)			12	40
t <sub>th</sub>	S0 high after S1 ↑ or S1 high after S0 ↑		MIN	3	-
	Data input A-H			0	0
t <sub>PLH</sub>	CLK	<u>RCO</u>	MAX	14	22
t <sub>PHL</sub>				14	16
t <sub>PLH</sub>	CLK	Any Q	MAX	16	11
t <sub>PHL</sub>				16	15
t <sub>PLH</sub>	ENT	<u>RCO</u>	MAX	14	10
t <sub>PHL</sub>				9	17
t <sub>PLH</sub>	ENP	<u>RCO</u>	MAX	-	14
t <sub>PHL</sub>				-	17
t <sub>PLH</sub>	S0, S1 (clear mode)	Any Q	MAX	26	-
t <sub>PHL</sub>	S0 or S1 (count up/down)	<u>RCO</u>	MAX	16	-
t <sub>PLH</sub>				16	-
t <sub>PHL</sub>	S0 or S1 (clear mode)	<u>RCO</u>	MAX	16	21

 UNIT t<sub>max</sub> : MHz other : ns

## SYNCHRONOUS 8-BIT UP/DOWN COUNTERS

- Fully Programmable with Synchronous Counting and Loading
- Synchronous Clear
- Ripple-Carry Output for n-Bit Cascading

Logic Diagram



**FUNCTION TABLE**

S1	S0	FUNCTION
L	L	Clear
L	H	Count down
H	L	Load
H	H	Count up

## ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	ALS	AS	UNIT
I <sub>CC</sub>	MAX	45	195	mA
I <sub>OH</sub>	MAX	-0.4	-2	mA
I <sub>OL</sub>	MAX	8	20	mA

## TIMING REQUIREMENTS AND SWITCHING CHARACTERISTICS

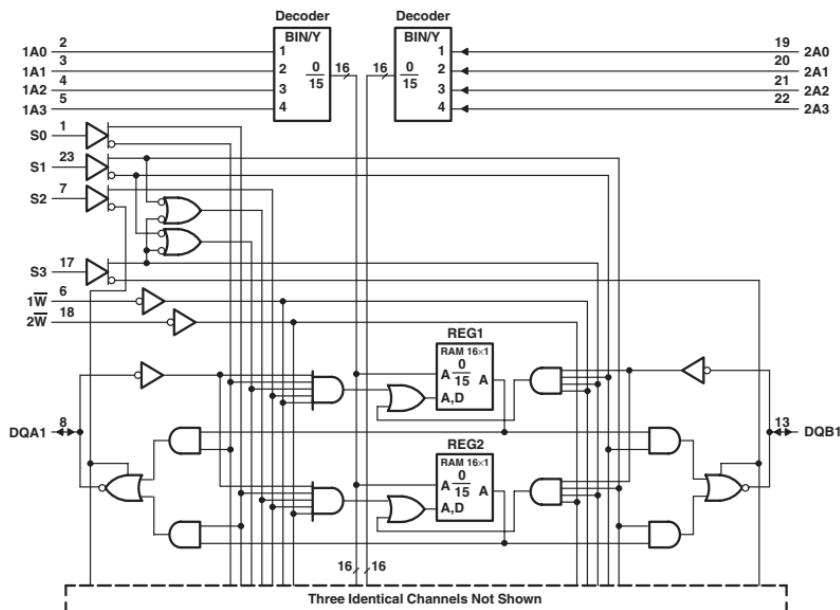
PARAMETER	INPUT	OUTPUT	MAX or MIN	ALS	AS
t <sub>max</sub>			MIN	35	45
t <sub>w</sub>			MIN	14	11
t <sub>su</sub>	Data input A-H		MIN	10	5
	ENP or ENT			15	9
	S0 low and S1 high (load)			13	11
	S0 and S1 low (clear)			13	11
	S0 high and S1 low (count down)			13	50
	S0 and S1 high (count up)			13	50
t <sub>f</sub>	S0 high after S1↑ or S1 high after S0↑		MIN	3	-
	Data input A-H			0	0
t <sub>PLH</sub>	CLK	R <sub>CO</sub>	MAX	14	35
t <sub>PHL</sub>	CLK	Any Q	MAX	14	18
t <sub>PLH</sub>	ENT	R <sub>CO</sub>	MAX	16	11
t <sub>PHL</sub>	ENP	R <sub>CO</sub>	MAX	16	15
t <sub>PLH</sub>	S1 (count up/down)	R <sub>CO</sub>	MAX	14	15
t <sub>PHL</sub>	S0 (clear/load)	R <sub>CO</sub>	MAX	9	17
t <sub>PLH</sub>				-	19
t <sub>PHL</sub>				-	18
t <sub>PLH</sub>				15	-
t <sub>PHL</sub>				15	-
t <sub>PLH</sub>				16	-
t <sub>PHL</sub>				12	-

UNIT t<sub>max</sub> : MHz other : ns

## DUAL 16-BY 4-BIT REGISTER FILES

- 3-State Buffer-Type Outputs Drive Bus Lines Directly
- Each Register File Has Individual Write-Enable Controls and Address Lines

Logic Diagram



FUNCTION TABLE

FILE SELECT		INPUT/OUTPUT			
S0	S1	FILE SEL	S2	S3	I/O SEL
L	L	1R to A, 1R to B	L	L	A out B A out, B out
H	L	2R to A, 1R to B			
L	H	1R to A, 2R to B			
H	H	2R to A, 2R to B			
L	L	A to 1R, 1R to B	H	L	A in B A in, B out
H	L	A to 2R, 1R to B			
L	H	A to 1R, 2R to B			
H	H	A to 2R, 2R to B			
L	L	1R to A, B to 1R	L	H	A out B A out, B in
H	L	2R to A, B to 1R			
L	H	1R to A, B to 2R			
H	H	2R to A, B to 2R			
L	L	B to 1R	H	H	A in Bin A in, B
H	L	A to 2R, B to 1R			
L	H	A to 1R, B to 2R			
H	H	B to 2R			

## ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	ALS	AS	UNIT
I <sub>CC</sub>	MAX	110	190	mA
I <sub>OL</sub>	MAX	24	48	mA
I <sub>OH</sub>	MAX	-2.6	-15	mA

## TIMING REQUIREMENTS AND SWITCHING CHARACTERISTICS

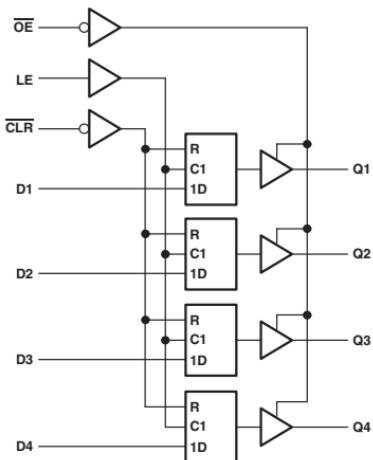
PARAMETER	INPUT	OUTPUT	MAX or MIN	ALS	AS	
t <sub>w</sub>	write		MIN	12	12	
t <sub>su</sub>	Address before write ↓		MIN	5	5	
	Data before write ↑			15	15	
	Select before write ↓			12	12	
	Address before write ↓			0	0	
t <sub>th</sub>	Data before write ↑		MIN	0	0	
	Select before write ↓			12	12	
	Any A	Any DQ		19	15	
t <sub>ts(A)</sub>	S0	Any DQA	MAX	15	13	
	S1	Any DQB		15	13	
t <sub>tds</sub>	S2	Any DQA	MAX	14	11	
	S3	Any DQB		14	11	
t <sub>ten</sub>	S2	Any DQA	MAX	17	12	
	S3	Any DQB		17	12	
t <sub>tpd</sub>	W	Any DQ	MAX	23	19	
	DA	DQB		26	22	
	DQB	DQA		26	22	

UNIT: ns

## DUAL 4-BIT D-TYPE LATCHES WITH 3-STATE OUTPUTS

- 3-State Buffer-Type Outputs Drive Bus Lines Directly
- Bus-Structured Pinout
- Asynchronous Clear

Logic Diagram



FUNCTION TABLE

INPUTS				OUTPUT
$\overline{OE}$	CLR	ENABLE	D	
LE				
L	L	X	X	L
L	H	H	H	H
L	H	H	L	L
L	H	L	X	$Q_0$
H	X	X	X	Z

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	ALS	AS	UNIT
$I_{CC}$	MAX	31	129	mA
$I_{OH}$	MAX	-2.6	-15	mA
$I_{OL}$	MAX	24	48	mA

TIMING REQUIREMENTS AND SWITCHING CHARACTERISTICS

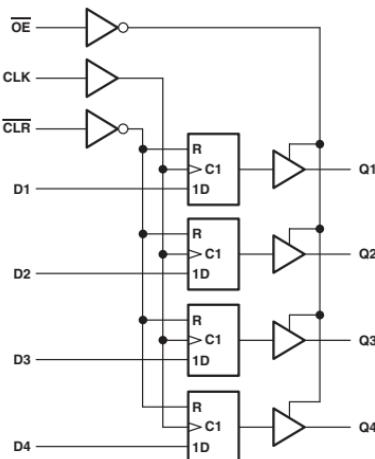
PARAMETER	INPUT	OUTPUT	MAX or MIN	ALS	AS
$t_{w}$	$\overline{CLR}$ low $\overline{LE}$ high		MIN	15	5
$t_{su}$				10	5
$t_h$				10	2
$t_{PLH}$				7	4.5
$t_{PHL}$	D	Q	MAX	14	9.5
$t_{PLH}$				14	7.5
$t_{PHL}$	LE	Q	MAX	22	13
$t_{PHL}$				21	7.5
$t_{PHL}$	$\overline{CLR}$	Q	MAX	20	9
$t_{PZH}$	$\overline{OE}$	Q	MAX	18	6.5
$t_{PZL}$				18	10.5
$t_{PHZ}$				10	7.5
$t_{PLZ}$	$\overline{OE}$	Q	MAX	15	7.5

UNIT: ns

## DUAL 4-BIT D-TYPE EDGE-TRIGGERED FLIP-FLOPS WITH 3-STATE OUTPUTS

- 3-State Buffer-Type Outputs Drive Bus Lines Directly
- Bus-Structured Pinout
- Asynchronous Clear

Logic Diagram



FUNCTION TABLE

INPUTS				OUTPUTS	
<u>OE</u>	<u>CLR</u>	CLK	D		
L	L	X	X	L	
L	H	↑	H	H	
L	H	↑	L	L	
L	H	L	X	Q <sub>0</sub>	
H	X	X	X	Z	

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX OR MIN	ALS	AS	UNIT
I <sub>CC</sub>	MAX	32	160	mA
I <sub>OH</sub>	MAX	-2.6	-15	mA
I <sub>OL</sub>	MAX	24	48	mA

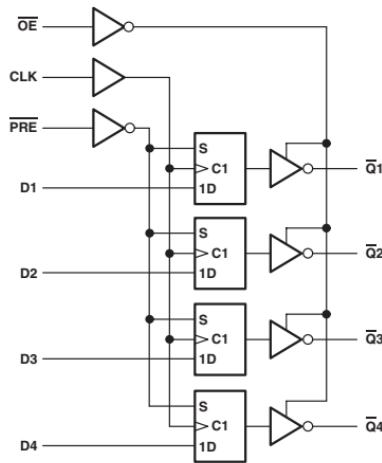
TIMING REQUIREMENTS AND SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX OR MIN	ALS	AS
t <sub>max</sub>			MIN	30	125
t <sub>w</sub>	PRE or CLR low		MIN	10	2
	CLK 'H'			16.5	3
	CLK 'L'		16.5	4	
t <sub>su</sub>	Data		MIN	15	2
	PRE or CLR inactive		MIN	10	4
t <sub>h</sub>			MIN	0	1
t <sub>PLH</sub>	CLK	Q	MAX	14	8.5
t <sub>PHL</sub>			MAX	14	10.5
t <sub>PLH</sub>	CLR	Q	MAX	17	9.5
t <sub>PZH</sub>			MAX	18	7
t <sub>PZL</sub>			MAX	18	10.5
t <sub>PHZ</sub>	OE	Q	MAX	10	6
t <sub>PZL</sub>	OE	Q	MAX	12	7.5

UNIT f<sub>max</sub> : MHz other : ns

**DUAL 4-BIT D-TYPE EDGE-TRIGGERED FLIP-FLOPS WITH 3-STATE OUTPUTS**

- 3-State Buffer-Type Outputs Drive Bus Lines Directly
- Bus-Structured Pinout
- Asynchronous Clear

**Logic Diagram**

**FUNCTION TABLE**  
(each flip-flop)

INPUTS				OUTPUT
OE	PRE	CLK	D	Q
L	L	X	X	L
L	H	↑	H	L
L	H	↑	L	H
L	H	L	X	$\bar{Q}_0$
H	X	X	X	Z

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	ALS	AS	UNIT
I <sub>CC</sub>	MAX	31	160	mA
I <sub>OH</sub>	MAX	-2.6	-15	mA
I <sub>OL</sub>	MAX	24	48	mA

TIMING REQUIREMENTS AND SWITCHING CHARACTERISTICS

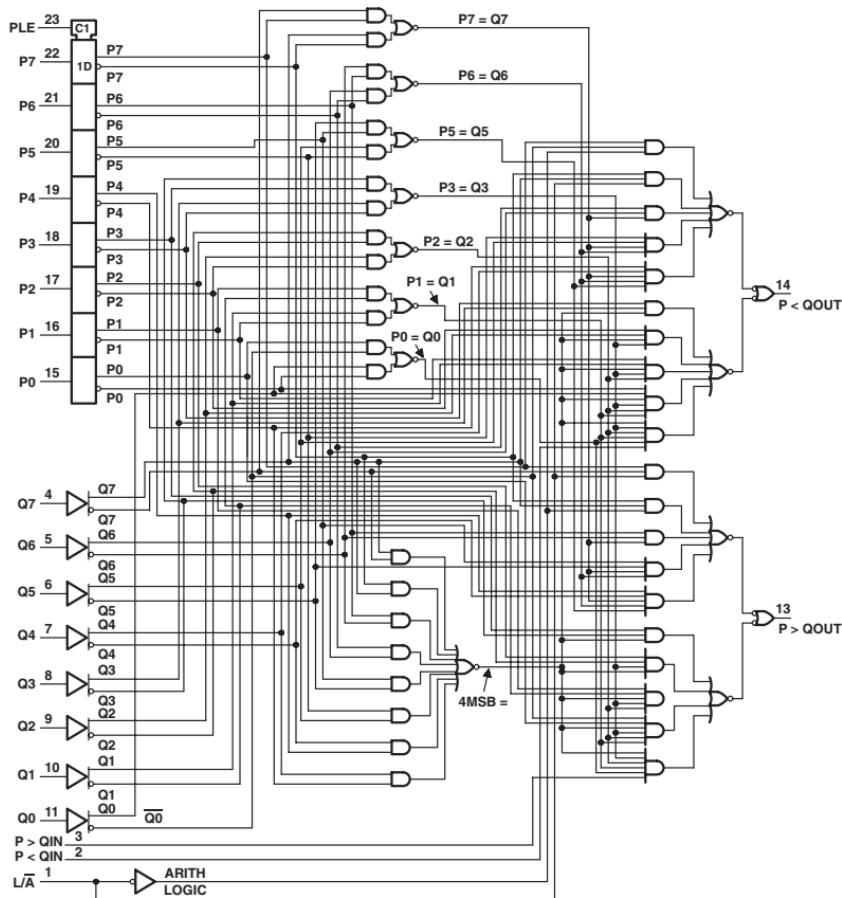
PARAMETER		INPUT	OUTPUT	MAX or MIN	ALS	AS		
$t_{max}$	PRE "L"			MIN	30	80		
	CLK "H"				10	4.5		
	CLK "L"			MIN	16.5	6.2		
	Data				16.5	6.2		
	PRE inactive			MIN	15	4.5		
	$t_h$				10	5		
$t_{PLH}$		CLK	$\bar{Q}$	MIN	0	2		
$t_{PHL}$				MAX	14	8.5		
$t_{PHL}$		$\bar{PRE}$	$\bar{Q}$	MAX	14	10.5		
$t_{PZH}$		$\bar{OE}$	$\bar{Q}$	MAX	19	9.5		
$t_{PZL}$				MAX	18	7		
$t_{PHZ}$		$\bar{OE}$	$\bar{Q}$	MAX	18	11		
$t_{PLZ}$				MAX	10	7		
$t_{PZL}$				MAX	13	7		

UNIT  $t_{max}$  : MHz, other : ns

## 8-BIT MAGNITUDE COMPARATORS

- SN54AS885 Latchable P-Input Ports with Power-Up Clear
- Choice of Logical or Arithmetic (Two's Complement) Comparison
- Data and PLE Inputs Utilize pnp Input Transistors to Reduce dc Loading Effects
- Cascadable to n Bits While Maintaining High Performance

Logic Diagram



FUNCTION TABLE

COMPARISON	INPUTS			OUTPUTS		
	L/A	DATA P0-P7, Q0-Q7	P > QIN	P < QIN	P > QOUT	P < QOUT
Logical	H	P > Q	X	X	H	L
Logical	H	P < Q	X	X	L	H
Logical†	H	P = Q	H or L	H or L	H or L	H or L
Arithmetic	L	P AG Q	X	X	H	L
Arithmetic	L	Q AG P	X	X	L	H
Arithmetic†	L	P = Q	H or L	H or L	H or L	H or L

† In these cases, P > QOUT follows P > QIN and P < QOUT follows P < QIN.

AG = arithmetically greater than

## ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	AS	UNIT
Icc	MAX	210	mA
IoH	MAX	-2	mA
IoL	MAX	20	mA

## TIMING REQUIREMENTS AND SWITCHING CHARACTERISTICS

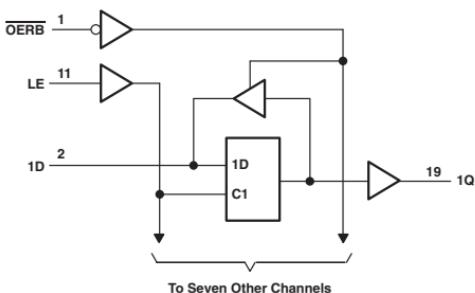
PARAMETER	INPUT	OUTPUT	MAX or MIN	AS
t <sub>tr</sub>	Data before PLE ↓		MIN	2
t <sub>th</sub>	Data after PLE ↓			4
t <sub>PLH</sub>		P < QOUT, P > QOUT	MAX	13
t <sub>PHL</sub>	L / A			13
t <sub>PLH</sub>	P < QIN, P > QIN	P < QOUT, P > QOUT	MAX	8
t <sub>PHL</sub>				8
t <sub>PLH</sub>	Any P or Q data input	P < QOUT, P > QOUT	MAX	17.5
t <sub>PHL</sub>				15

UNIT: ns

## 8-BIT D-TYPE TRANSPARENT READ-BACK LATCH

- 3-State I/O-Type Read-Back Inputs
- True Logic Outputs
- Bus-Structured Pinout

Logic Diagram



## ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER		MAX or MIN	ALS	UNIT
<u>I<sub>CC</sub></u>		MAX	70	mA
<u>I<sub>OH</sub></u>	<u>Q</u>	MAX	-2.6	mA
	D		-0.4	mA
<u>I<sub>OL</sub></u>	<u>Q</u>	MAX	24	mA
	D		8	mA

## TIMING REQUIREMENTS AND SWITCHING CHARACTERISTICS

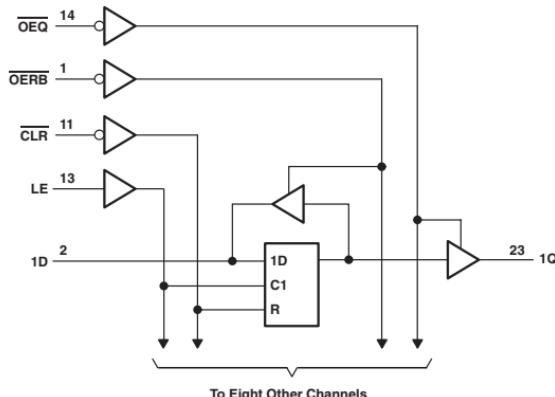
PARAMETER	INPUT	OUTPUT	MAX or MIN	ALS
<u>t<sub>w</sub></u>	LE high		MIN	10
<u>t<sub>su</sub></u>	Data before LE ↓		MIN	10
	Data before OERB			10
	Data after LE ↓		MIN	5
<u>t<sub>PLH</sub></u>	D	Q	MAX	17
<u>t<sub>PHL</sub></u>				24
<u>t<sub>PLH</sub></u>	LE	Q	MAX	26
<u>t<sub>PHL</sub></u>				26
<u>t<sub>en</sub></u>	<u>OERB</u>	D	MAX	21
<u>t<sub>dis</sub></u>			MAX	19

UNIT: ns

## 9-BIT D-TYPE TRANSPARENT READ-BACK LATCH WITH 3-STATE OUTPUTS

- 3-State I/O-Type Read-Back Inputs
- True Logic Outputs
- Bus-Structured Pinout
- Designed with Nine Bits for Parity Applications

Logic Diagram



## ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER		MAX or MIN	ALS	UNIT
Icc		MAX	80	mA
Ioh	Q	MAX	-2.6	mA
	D		-0.4	mA
Iol	Q	MAX	24	mA
	D		8	mA

## TIMING REQUIREMENTS AND SWITCHING CHARACTERISTICS

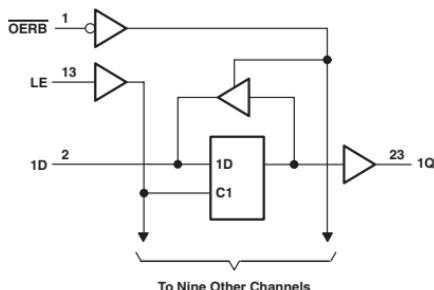
PARAMETER	INPUT	OUTPUT	MAX or MIN	ALS
t <sub>tr</sub>	C "H"		MIN	10
	CLR "L"			10
t <sub>tsu</sub>	Data before LE ↓		MIN	10
	Data before OERB ↓			10
t <sub>th</sub>	Data after LE ↓		MIN	5
t <sub>PLH</sub>	D	Q	MAX	14
t <sub>PLH</sub>				16
t <sub>PLH</sub>	LE	Q	MAX	20
t <sub>PLH</sub>				25
t <sub>PHL</sub>	CLR	Q	MAX	20
t <sub>PHL</sub>				26
t <sub>ton</sub>	OERB	D	MAX	21
t <sub>dis</sub>				14
t <sub>ten</sub>	OEQ	Q	MAX	18
t <sub>dis</sub>				14

UNIT:ns

## 10-BIT D-TYPE TRANSPARENT READ-BACK LATCH

- 3-State I/O-Type Read-Back Inputs
- True Logic Outputs
- Bus-Structured Pinout

Logic Diagram



## ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER		MAX or MIN	ALS	UNIT
$I_{CC}$		MAX	82	mA
$I_{OH}$	Q	MAX	-2.6	mA
	D		-0.4	mA
$I_{OL}$	Q	MAX	24	mA
	D		8	mA

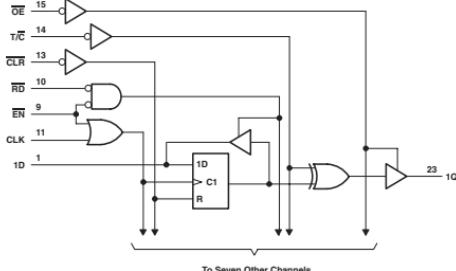
## TIMING REQUIREMENTS AND SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	ALS
$t_w$		C 'H'	MIN	10
$t_{SU}$		Data before LE ↓	MIN	10
		Data before OERB ↓		10
$t_h$		Data after LE ↓	MIN	5
$t_{PLH}$	D	Q	MAX	14
$t_{PHL}$				18
$t_{PLH}$	LE	Q	MAX	21
$t_{PHL}$				27
$t_{en}$	OERB	D	MAX	21
$t_{dis}$				16

UNIT:ns

## 8-BIT D-TYPE EDGE-TRIGGERED READ-BACK LATCHES

- 3-State I/O-Type Read-Back Inputs
- True Logic Outputs
- T/C Determines True or Complementary Data at Q Outputs



### ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER		MAX or MIN	ALS	ALS-1	UNIT
I <sub>CC</sub>		MAX	85	85	mA
I <sub>OL</sub>	Q	MAX	24	48	mA
	D		8	8	mA
I <sub>OH</sub>	Q	MAX	-2.6	-2.6	mA
	D		-0.4	-0.4	mA

### TIMING REQUIREMENTS AND SWITCHING CHARACTERISTICS

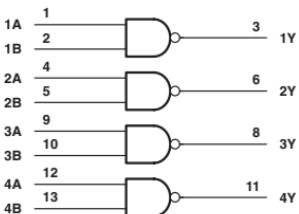
PARAMETER	INPUT	OUTPUT	MAX or MIN	ALS	ALS-1
t <sub>W</sub>	CLR low		MIN	10	10
	CLK low			14.5	14.5
	CLK high			14.5	14.5
t <sub>su</sub>	Data before CLK ↑		MIN	15	15
	EN low before CLK ↑			10	10
	CLK high before EN ↑ * <sup>1</sup>			15	15
	CLR high (inactive) before CLK ↑			10	10
t <sub>h</sub>	Data after CLK ↑		MIN	0	0
	EN low after CLK ↑			5	5
	RD high after CLK ↑ * <sup>2</sup>			5	5
t <sub>PLH</sub>	CLK (T/C = H or L)	Q	MAX	28	28
t <sub>PHL</sub>				28	28
t <sub>PLH</sub>	CLR (T/C = L)	Q	MAX	27	27
t <sub>PHL</sub>	CLR (T/C = H)	Q	MAX	23	23
t <sub>PLH</sub>	T / C	Q	MAX	23	23
t <sub>PHL</sub>				23	23
t <sub>PLH</sub>	CLR	D	MAX	30	30
t <sub>PLS</sub> * <sup>3</sup>	RD	D	MAX	16	16
t <sub>PLS</sub> * <sup>4</sup>				19	19
t <sub>PLS</sub> * <sup>3</sup>	EN	D	MAX	16	16
t <sub>PLS</sub> * <sup>4</sup>				19	19
t <sub>PLS</sub> * <sup>3</sup>	OE	Q	MAX	15	15
t <sub>PLS</sub> * <sup>4</sup>				10	10

UNIT: ns

## 1000

### QUADRUPLE 2-INPUT POSITIVE-NAND BUFFERS/DRIVERS

- Buffer Version of SN74ALS00A
- Driver Version of SN74AS00
- High Capacitive-Drive Capability

**Logic Diagram****FUNCTION TABLE**

INPUTS	OUTPUT	
A	B	Y
H	H	L
L	X	H
X	L	H

**ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS**

PARAMETER	MAX or MIN	ALS	AS	UNIT
$I_{CC}$	MAX	7.8	19	mA
$I_{OH}$	MAX	-2.6	-48	mA
$I_{OL}$	MAX	24	48	mA

**SWITCHING CHARACTERISTICS**

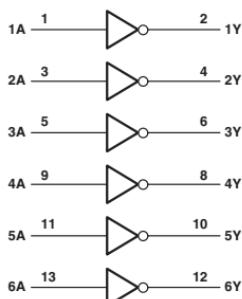
PARAMETER	INPUT	OUTPUT	MAX or MIN	ALS	AS
$t_{PLH}$	A or B	Y	MAX	8	4
$t_{PHL}$				7	4

UNIT: ns

## 1004

### HEX INVERTING DRIVERS

- Driver Version of SN74ALS04B and SN74AS04
- High Capacitive-Drive Capability

**Logic Diagram****FUNCTION TABLE**

INPUT	OUTPUT
A	Y
H	L
L	H

**ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS**

PARAMETER	MAX or MIN	ALS	AS	UNIT
$I_{CC}$	MAX	12	27	mA
$I_{OH}$	MAX	-15	-48	mA
$I_{OL}$	MAX	24	48	mA

**SWITCHING CHARACTERISTICS**

PARAMETER	INPUT	OUTPUT	MAX or MIN	ALS	AS
$t_{PLH}$	A or B	Y	MAX	7	4
$t_{PHL}$				6	4

UNIT: ns

## 1005

### HEX INVERTING BUFFERS WITH OPEN-COLLECTOR OUTPUTS

- Buffer Version of SN74ALS05A

**FUNCTION TABLE**

INPUT A	OUTPUT Y
H	L
L	H

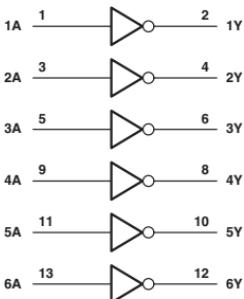
ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	ALS	UNIT
I <sub>CC</sub>	MAX	12	mA
V <sub>DH</sub>	MAX	5.5	V
I <sub>OL</sub>	MAX	24	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	ALS
t <sub>PLH</sub>	A	Y	MAX	30
t <sub>PHL</sub>				10

UNIT: ns

**Logic Diagram**

## 1008

### QUADRUPLE 2-INPUT POSITIVE-AND BUFFER/DRIVER

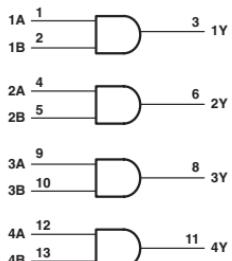
- Buffer Version of SN74ALS08
- Driver Version of SN74AS08

**FUNCTION TABLE**

INPUTS A B	OUTPUT Y
H H	H
L X	L
X L	L

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	ALS	AS	UNIT
I <sub>CC</sub>	MAX	9.3	22	mA
I <sub>OH</sub>	MAX	-2.6	-48	mA
I <sub>OL</sub>	MAX	24	48	mA

**Logic Diagram**

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	ALS	AS
t <sub>PLH</sub>	A or B	Y	MAX	9	6
t <sub>PHL</sub>				9	6

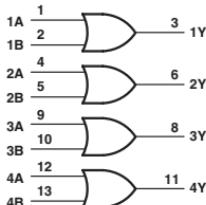
UNIT: ns

## 1032

### QUADRUPLE 2-INPUT POSITIVE-OR BUFFERS/DRIVERS

- $Y = A + B$
- Driver Version of SN74AS32
- High Capacitive-Drive Capability

### Logic Diagram



**FUNCTION TABLE**  
(each gate)

INPUTS	OUTPUT	
A	B	Y
H	X	H
X	H	H
L	L	L

ELECTRICAL CHARACTERISTICS AND  
RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	ALS	AS	UNIT
$I_{CC}$	MAX	10.6	24	mA
$I_{OH}$	MAX	-2.6	-48	mA
$I_{OL}$	MAX	24	48	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	ALS	AS
$t_{PLH}$	A or B	Y	MAX	9	6.3
$t_{PHL}$	A or B	Y	MAX	12	6.3

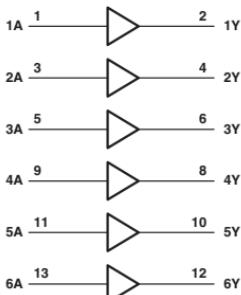
UNIT: ns

## 1034

### HEX DRIVERS

- SN74AS1034A Offer High Capacitive-Drive Capability
- Noninverting Drivers

### Logic Diagram



**FUNCTION TABLE**

INPUT	OUTPUT
A	Y
H	H
L	L

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	ALS	AS	UNIT
$I_{CC}$	MAX	14	35	mA
$I_{OH}$	MAX	-15	-48	mA
$I_{OL}$	MAX	24	48	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	ALS	AS
$t_{PLH}$	A	Y	MAX	8	6
$t_{PHL}$				8	6

UNIT: ns

## 1035

### HEX NONINVERTING BUFFERS WITH OPEN-COLLECTOR OUTPUTS

- Noninverting Buffers with Open-Collector Outputs

**FUNCTION TABLE**

INPUT A	OUTPUT Y
H	H
L	L

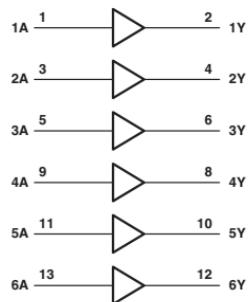
ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	ALS	UNIT
I <sub>CC</sub>	MAX	14	mA
V <sub>DH</sub>	MAX	5.5	V
I <sub>OL</sub>	MAX	24	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	ALS
I <sub>PLH</sub>	A	Y	MAX	30
I <sub>PHL</sub>				12

UNIT: ns

**Logic Diagram**

## 1240

### OCTAL BUFFER AND LINE DRIVER WITH 3-STATE OUTPUTS

- Low-Power Versions of SN74ALS240A
- 3-State Outputs Drive Bus Lines or Buffer Memory Address Registers
- 3-State Outputs Drive Bus Lines or Buffer Memory Address Registers

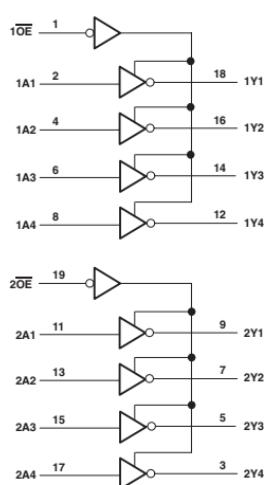
ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	ALS	UNIT
I <sub>CZ</sub>	MAX	13	mA
I <sub>CL</sub>	MAX	14	mA
I <sub>OH</sub>	MAX	-15	mA
I <sub>OL</sub>	MAX	16	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	ALS
I <sub>PLH</sub>	A	Y	MAX	13
I <sub>PHL</sub>				13
I <sub>PZH</sub>	OE	Y	MAX	20
I <sub>PZL</sub>				22
I <sub>PHZ</sub>	OE	Y	MAX	10
I <sub>PZL</sub>				13

UNIT: ns

**Logic Diagram**

## 1244

### OCTAL BUFFERS AND DRIVERS WITH 3-STATE OUTPUTS

- 3-State Outputs Drive Bus Lines or Buffer Memory Address Registers
- pnp Inputs Reduce dc Loading
- Low-Power Versions of SN74ALS244 Series

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

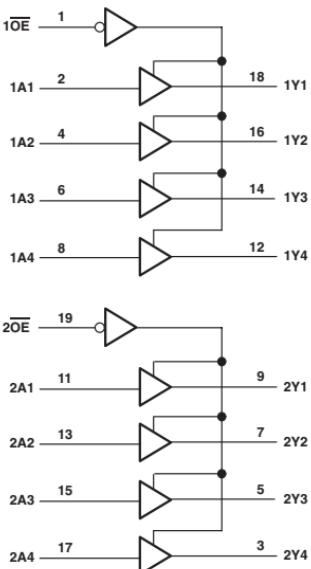
PARAMETER	MAX or MIN	ALS	UNIT
$I_{CC2}$	MAX	20	mA
$I_{CLL}$	MAX	17	mA
$I_{OH}$	MAX	-15	mA
$I_{OL}$	MAX	16	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	ALS
$t_{PLH}$	A	Y	MAX	14
$t_{PHL}$				14
$t_{PZH}$	$\overline{OE}$	Y	MAX	22
$t_{PZL}$	$\overline{OE}$	Y	MAX	22
$t_{PHZ}$	$\overline{OE}$	Y	MAX	13
$t_{PLZ}$	$\overline{OE}$	Y	MAX	16

UNIT: ns

### Logic Diagram



## 1245

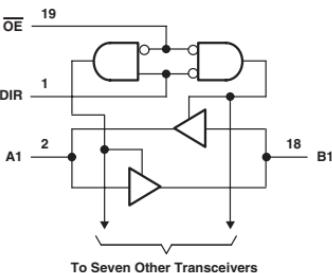
### OCTAL BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

- Low-Power Versions of 4ALS245 Series

FUNCTION TABLE

CONTROL INPUTS		OPERATION
OE	DIR	
L	L	B data to A bus
L	H	A data to B bus
H	X	Isolation

### Logic Diagram



ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	ALS	UNIT
$I_{CC2}$	MAX	36	mA
$I_{CLL}$	MAX	33	mA
$I_{OH}$	MAX	-15	mA
$I_{OL}$	MAX	16	mA

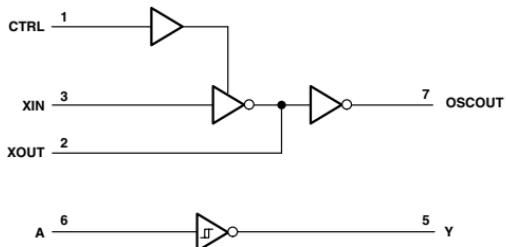
SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	ALS
$t_{PLH}$	A or B	B or A	MAX	13
$t_{PHL}$				13
$t_{PZH}$	$\overline{OE}$	A or B	MAX	25
$t_{PZL}$	$\overline{OE}$	A or B	MAX	25
$t_{PHZ}$	$\overline{OE}$	A or B	MAX	12
$t_{PLZ}$	$\overline{OE}$	A or B	MAX	18

UNIT: ns

## **OSCILLATOR DRIVER FOR CRYSTAL OSCILLATOR OR CERAMIC RESONATOR**

## Logic Diagram



## FUNCTION TABLES

FUNCTION TABLES			
INPUTS		OUTPUTS	
CTRL	XIN	XOUT	OSCOUT
H	L	H	L
H	H	L	H
L	X	L	H

INPUT A	OUTPUT Y
L	H
H	L

#### ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC CHARGING CONDITIONS						
PARAMETER	MAX OR MIN	LVC 1.8V	LVC 2.5V	LVC 3V	LVC 5V	UNIT
Icc	MAX	0.01	0.01	0.01	0.01	mA
iOH (OSCOUT, XOUT, Y outputs)	MAX	-4	-8	-24	-32	mA
iIH (OSCOUT, XOUT, Y outputs)	MAX	4	8	24	32	mA
iOL (XOUT)	MAX	2	-	-	-	mA

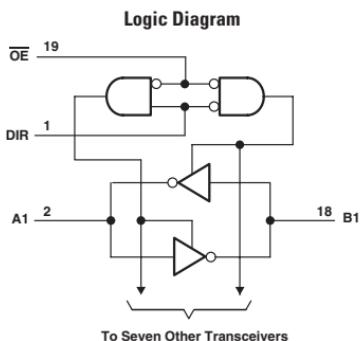
## SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	LVC 1.8V	LVC 2.5V	LVC 3V	LVC 5V
IPHL	A	Y	MAX	17.3	7.4	6.4	5.3
IPHL				17.3	7.4	6.4	5.3
IPHL	XIN	XOUT	MAX	15.8	5.8	5.4	4.6
IPHL				15.8	5.8	5.4	4.6
IPHL	XIN	OSCOUT	MAX	25.7	7.1	7.8	6.7
IPHL				25.7	7.1	7.8	6.7
IPHL	CTRL	XOUT	MAX	24.5	12	12.7	11.2
IPHL				24.5	12	12.7	11.2

UNIT-1

## OCTAL BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

- Lower-Power Versions of SN74ALS640B
- Inverting Logic
- 3-State Outputs



FUNCTION TABLE

CONTROL INPUTS		OPERATION	
OE	DIR		
L	L	$\bar{B}$ data to A bus	
L	H	$\bar{A}$ data to B bus	
H	X	Isolation	

## ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	ALS	UNIT
$I_{CC}$	MAX	32	mA
$I_{OH}$	MAX	-15	mA
$I_{OL}$	MAX	16	mA

## SWITCHING CHARACTERISTICS

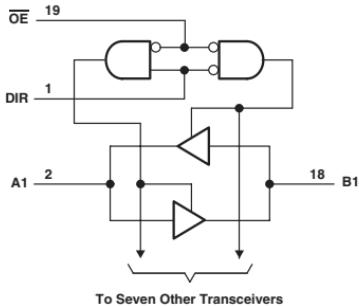
PARAMETER	INPUT	OUTPUT	MAX or MIN	ALS
$t_{PLH}$	A or B	B or A	MAX	15
$t_{PHL}$				10
$t_{PZH}$	$\bar{OE}$	A or B	MAX	20
$t_{PZL}$				22
$t_{PHZ}$	$\bar{OE}$	A or B	MAX	10
$t_{PLZ}$				13

UNIT: ns

## OCTAL BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

- Lower-Power Versions of SN74ALS645A
- 3-State Outputs

Logic Diagram



To Seven Other Transceivers

FUNCTION TABLE

CONTROL INPUTS		OPERATION	
OE	DIR		
L	L	B data to A bus	
L	H	A data to B bus	
H	X	Isolation	

## ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	ALS	UNIT
I <sub>CC</sub>	MAX	38	mA
I <sub>OH</sub>	MAX	-15	mA
I <sub>OL</sub>	MAX	16	mA

## SWITCHING CHARACTERISTICS

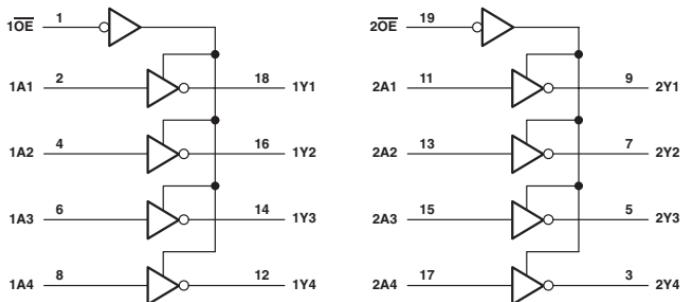
PARAMETER	INPUT	OUTPUT	MAX or MIN	ALS
t <sub>PLH</sub>	A or B	B or A	MAX	13
t <sub>PHL</sub>				13
t <sub>PZH</sub>	OE	A or B	MAX	25
t <sub>PZL</sub>				25
t <sub>PHZ</sub>	OE	A or B	MAX	12
t <sub>PZL</sub>				18

UNIT: ns

## OCTAL BUFFERS AND LINE/MOS DRIVERS WITH 3-STATE OUTPUTS

- I/O Ports Have 25- $\Omega$  Series Resistors, So No External Resistors Are Required (SN74ALS2240, SN74ABT2240A)
- Output Ports Have Equivalent 33- $\Omega$  Series Resistors, So No External Resistors Are Required (SN74BCT2240)

Logic Diagram



## ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	ALS	SN74 BCT	ABT	UNIT
$I_{CC2}$	MAX	20	8	0.25	mA
$I_{CLL}$	MAX	23	76	30	mA
$I_{OH}$	MAX	-15	-12	-32	mA
$I_{OL}$	MAX	15	12	12	mA

## SWITCHING CHARACTERISTICS

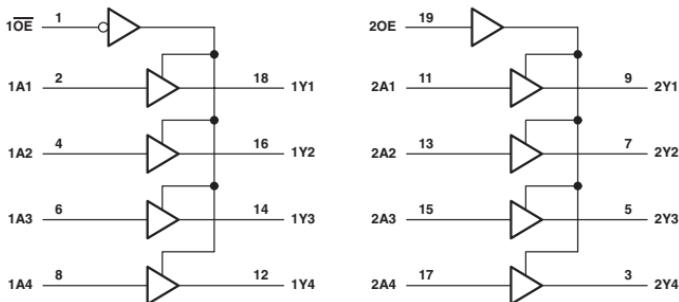
PARAMETER	INPUT	OUTPUT	MAX or MIN	ALS	SN74	ABT
					BCT	ABT
$t_{PLH}$	A	Y	MAX	10	5.7	4.8
				10	4.4	5.4
$t_{PHL}$	$\bar{OE}$	Y	MAX	17	9.3	5.2
				20	12.4	6.8
$t_{PZH}$	$\bar{OE}$	Y	MAX	10	8.7	6.4
				15	10.6	6.2

UNIT: ns

## OCTAL BUFFERS AND LINE/MOS DRIVERS WITH 3-STATE OUTPUTS

- Output Ports Have Equivalent  $25\text{-}\Omega$  Series Resistors, So No External Resistors Are Required (SN74ABT2241A)
- Output Ports Have Equivalent  $33\text{-}\Omega$  Series Resistors, So No External Resistors Are Required (SN74BCT2241)

Logic Diagram



## ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	SN74 BCT	ABT	UNIT
I <sub>CC2</sub>	MAX	9	0.25	mA
I <sub>CCL</sub>	MAX	76	30	mA
I <sub>OH</sub>	MAX	-12	-32	mA
I <sub>OL</sub>	MAX	12	12	mA

## SWITCHING CHARACTERISTICS

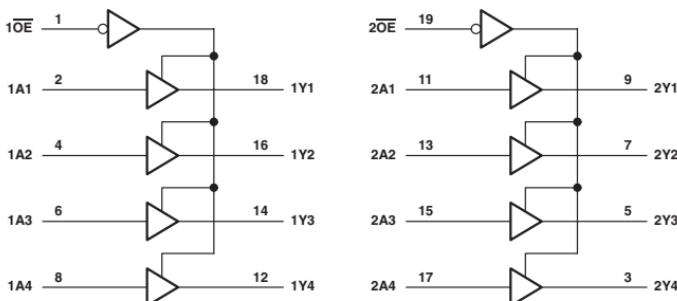
PARAMETER	INPUT	OUTPUT	MAX or MIN	SN74 BCT	ABT
t <sub>PLH</sub>	A	Y	MAX	4.9	4.7
t <sub>PHL</sub>				6.9	5.6
t <sub>PZH</sub>	1OE	Y	MAX	8.9	5.8
t <sub>PZL</sub>				10.3	8.4
t <sub>PHZ</sub>	1OE	Y	MAX	8.7	6.6
t <sub>PLZ</sub>				11.3	6.4
t <sub>PZH</sub>	2OE	Y	MAX	8.9	5.8
t <sub>PZL</sub>				10.3	8.4
t <sub>PHZ</sub>	2OE	Y	MAX	8.7	6.6
t <sub>PLZ</sub>				11.3	6.4

UNIT: ns

## OCTAL BUFFERS AND LINE/MOS DRIVERS WITH 3-STATE OUTPUTS

- Output Ports Have Equivalent 25- $\Omega$  Series Resistors, So No External Resistors Are Required (SN74ABT2244A)
- Output Ports Have Equivalent 33- $\Omega$  Series Resistors, So No External Resistors Are Required (SN74BCT2244)
- Output Ports Have Equivalent 26- $\Omega$  Series Resistors, So No External Resistors Are Required (SN74LVC2244A)

Logic Diagram



FUNCTION TABLE

INPUTS	OUTPUT	
OE	A	Y
H	X	Z
L	L	L
L	H	H

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	ALS	SN74 BCT	ABT	LVC 3V	UNIT
$I_{CC2}$	MAX	23	10	0.25	0.01	mA
$I_{CCL}$	MAX	22	77	30	0.01	mA
$I_{OH}$	MAX	-15	-12	-32	-12	mA
$I_{OL}$	MAX	15	12	12	12	mA

SWITCHING CHARACTERISTICS

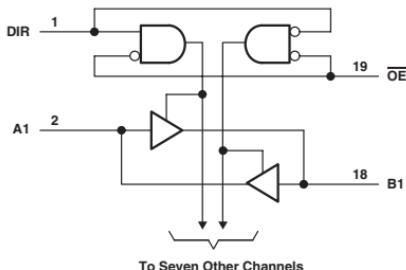
PARAMETER	INPUT	OUTPUT	MAX or MIN	ALS	SN74 BCT	ABT	LVC 3V
$t_{PLH}$	A	Y	MAX	16	4.9	4.7	5.5
$t_{PHL}$				17	6.7	5.6	5.5
$t_{PZH}$	$\overline{OE}$	Y	MAX	17	8.7	5.5	7.1
$t_{PZL}$	$\overline{OE}$	Y	MAX	14	10.4	8.3	7.1
$t_{PHZ}$	$\overline{OE}$	Y	MAX	9	7.8	6.6	6.8
$t_{PLZ}$	$\overline{OE}$	Y	MAX	9	9.8	5.8	6.8

UNIT: ns

## OCTAL TRANSCEIVER AND LINE/MOS DRIVERS WITH 3-STATE OUTPUTS

- B Port Has Equivalent 33- $\Omega$  Series Resistors, So No External Resistors Are Required (SN74BCT2245)
- B-Port Outputs Have Equivalent 25- $\Omega$  Series Resistors, So No External Resistors Are Required (SN74ABT2245)
- Outputs Have Equivalent 25- $\Omega$  Series Resistors, So No External Resistors Are Required (SN74ABTR2245)
- All Outputs Have Equivalent 26- $\Omega$  Series Resistors, So No External Resistors Are Required (SN74LVCR2245)
- B-Port Outputs Have Equivalent 22- $\Omega$  Series Resistors, So No External Resistors Are Required (SN74LVTH2245)

Logic Diagram



FUNCTION TABLE

INPUTS		OPERATION	
OE	DIR		
L	L	B	data to A bus
L	H	A	data to B bus
H	X		Isolation

## ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	SN74 BCT	ABT	ABTR	LVTH 3V	LVCR 3V	UNIT
I <sub>CC2</sub>	MAX	15	0.25	0.25	0.19	0.01	mA
I <sub>CC1</sub>	MAX	100	32	32	5	0.01	mA
I <sub>OH</sub> (A port)	MAX	-3	-32	-12	-32	-12	mA
I <sub>OH</sub> (B port)	MAX	-12	-12	-12	-12	-12	mA
I <sub>OL</sub> (A port)	MAX	24	64	12	64	12	mA
I <sub>OL</sub> (B port)	MAX	12	12	12	12	12	mA

## SWITCHING CHARACTERISTICS

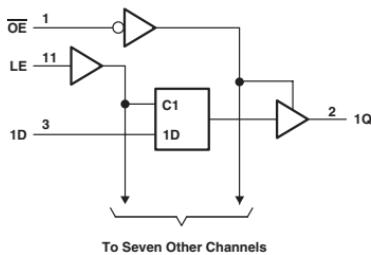
PARAMETER	INPUT	OUTPUT	MAX or MIN	SN74 BCT	ABT	ABTR	LVTH 3V	LVCR 3V
I <sub>PLH</sub>	A	B	MAX	5.8	3.8	3.8	4.4	6.3
I <sub>PLH</sub>				7.8	4.5	4.5	4.4	6.3
I <sub>PLH</sub>	B	A	MAX	7	3.6	3.8	3.5	6.3
I <sub>PLH</sub>				7.7	4	4.5	3.5	6.3
I <sub>ZH</sub>	$\overline{OE}$	B	MAX	9.9	6.1	6.1	6.2	8.2
I <sub>ZH</sub>				12.2	6.3	6.3	6.2	8.2
I <sub>PHZ</sub>	$\overline{OE}$	B	MAX	8.2	5.3	5.3	5.9	7.8
I <sub>PHZ</sub>				9.2	4.8	4.8	5.4	7.8
I <sub>ZH</sub>	$\overline{OE}$	A	MAX	11.1	5.5	6.1	5.5	8.2
I <sub>ZH</sub>				11.4	5.7	6.3	5.5	8.2
I <sub>PHZ</sub>	$\overline{OE}$	A	MAX	9.4	5.6	5.3	5.9	7.8
I <sub>PHZ</sub>				7.6	4.5	4.8	5	7.8

UNIT: ns

25- $\Omega$  OCTAL TRANSPARENT D-TYPE LATCH WITH 3-STATE OUTPUTS

- 3-State True Outputs with 25- $\Omega$  Sink Resistors
- Full Parallel Access for Loading
- Buffered Control Inputs

Logic Diagram



To Seven Other Channels

FUNCTION TABLE  
(each latch)

INPUTS			OUTPUT
OE	LE	D	Q
L	H	H	H
L	H	L	L
L	L	X	Q <sub>0</sub>
H	X	X	Z

## ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	F	UNIT
I <sub>CC</sub>	MAX	66	mA
I <sub>OH</sub>	MAX	-3	mA
I <sub>OL</sub>	MAX	12	mA

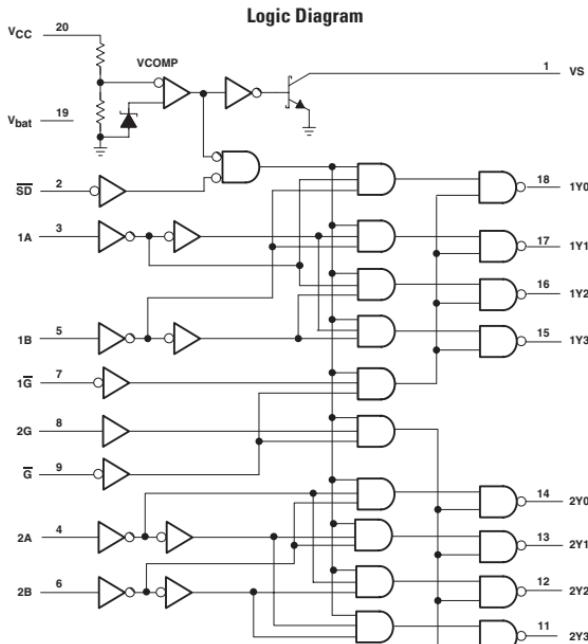
## TIMING REQUIREMENTS AND SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	F
t <sub>w</sub>	LE high		MIN	6
t <sub>su</sub>	Data before LE ↓		MIN	2
t <sub>th</sub>	Data after LE ↓		MIN	6
t <sub>PLH</sub>	D	Q	MAX	9
t <sub>PHL</sub>				7
t <sub>PLH</sub>	LE	Q	MAX	13
t <sub>PHL</sub>				8
t <sub>PZH</sub>	OE	Q	MAX	12
t <sub>PZL</sub>				9.5
t <sub>PHZ</sub>	OE	Q	MAX	7.5
t <sub>PZL</sub>				6

UNIT:ns

## MEMORY DECODER WITH ON-CHIP SUPPLY VOLTAGE MONITOR

- Built-In Supply-Voltage Monitor for  $V_{CC}$
- Separate Enable Inputs for Easy Cascading

**FUNCTION TABLE**

INPUTS			OUTPUTS					
CONTROL	1G	SD	1B	1A	1Y0	1Y1	1Y2	1Y3
H	X	X	X	X	H	H	H	H
X	H	X	X	X	H	H	H	H
X	X	L	X	X	H	H	H	H
L	L	H	L	L	L	H	H	H
L	L	H	L	H	H	L	H	H
L	L	H	H	L	H	H	L	L
L	L	H	H	H	H	H	H	L

**ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS**

PARAMETER	MAX or MIN	SN74 BCT	UNIT
$I_{CC}$	MAX	3	mA
$I_{OL}$ (Output low)	MAX	3	mA
$I_{OH}$	MAX	-0.4	mA
$I_{OL}$ (Y Output)	MAX	8	mA
$I_{OL}$ (I/S Output)	MAX	20	mA

**SWITCHING CHARACTERISTICS**

PARAMETER	INPUT	OUTPUT	MAX or MIN	SN74 BCT
$t_{PLH}$		Any Y	MAX	12
$t_{PHL}$		Any Y	MAX	12
$t_{PLH}$	Any $\overline{G}$	Any Y	MAX	10
$t_{PHL}$		Any Y	MAX	11
$t_{PLH}$	$\overline{SD}$	Any Y	MAX	12
$t_{PHL}$		Any Y	MAX	12
$t_{PLH}$	$V_{CC}$	Any Y	MAX	250
$t_{PHL}$		Any Y	MAX	250
$t_{PLH}$	$V_{CC}$	VS	MAX	250
$t_{PHL}$		VS	MAX	250

INITIAL

## 2541

### OCTAL LINE DRIVER/MOS DRIVER WITH 3-STATE OUTPUTS

- Outputs Have 25- $\Omega$  Series Resistor So No External Resistors Are Required

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

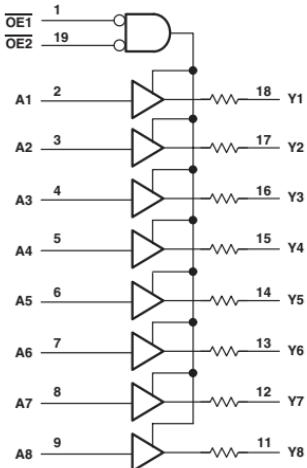
PARAMETER	MAX or MIN	ALS	UNIT
$I_{CCZ}$	MAX	22	mA
$I_{CCL}$	MAX	25	mA
$I_{OH}$	MAX	-0.4	mA
$I_{OL}$	MAX	12	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	ALS
$t_{PLH}$	A	Y	MAX	15
$t_{PHL}$				12
$t_{PZH}$	$\overline{OE}$	Y	MAX	15
$t_{PZL}$	$\overline{OE}$	Y	MAX	20
$t_{PHZ}$	$\overline{OE}$	Y	MAX	10
$t_{PLZ}$	$\overline{OE}$	Y	MAX	12

UNIT: ns

### Logic Diagram

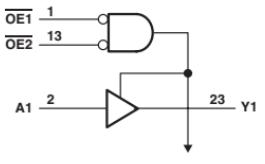
All output resistors are 25  $\Omega$ .

## 2827

### 10-BIT BUFFERS/DRIVERS WITH 3-STATE OUTPUTS

- Output Ports Have Equivalent 25- $\Omega$  Series Resistors, So No External Resistors Are Required (SN74ABT2827)
- Output Ports Have Equivalent 25- $\Omega$  Resistors; No External Resistors Are Required (SN74BCT2827C)

### Logic Diagram



To Nine Other Channels

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	SN74 BCT	ABT	UNIT
$I_{CCZ}$	MAX	6	0.25	mA
$I_{CCL}$	MAX	40	40	mA
$I_{OH}$	MAX	-1	-12	mA
$I_{OL}$	MAX	12	12	mA

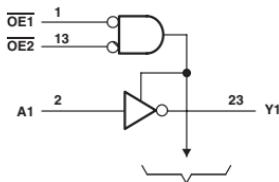
SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	SN74 BCT	ABT
$t_{PLH}$	A	Y	MAX	6	5.5
$t_{PHL}$				7.8	5.1
$t_{PZH}$	$\overline{OE}$	Y	MAX	10.7	6.7
$t_{PZL}$	$\overline{OE}$	Y	MAX	12.9	7.8
$t_{PHZ}$	$\overline{OE}$	Y	MAX	13	7.2
$t_{PLZ}$	$\overline{OE}$	Y	MAX	10	7.5

UNIT: ns

## 10-BIT BUS/MOS MEMORY DRIVERS WITH 3-STATE INVERTING

- Output Ports Have Equivalent 33- $\Omega$  Series Resistors, So No External Resistors Are Required (SN74BCT2828)



To Nine Other Channels

### ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	SN74 BCT	UNIT
I <sub>CZ</sub>	MAX	6	mA
I <sub>CCL</sub>	MAX	40	mA
I <sub>OH</sub>	MAX	-1	mA
I <sub>OL</sub>	MAX	12	mA

### SWITCHING CHARACTERISTICS

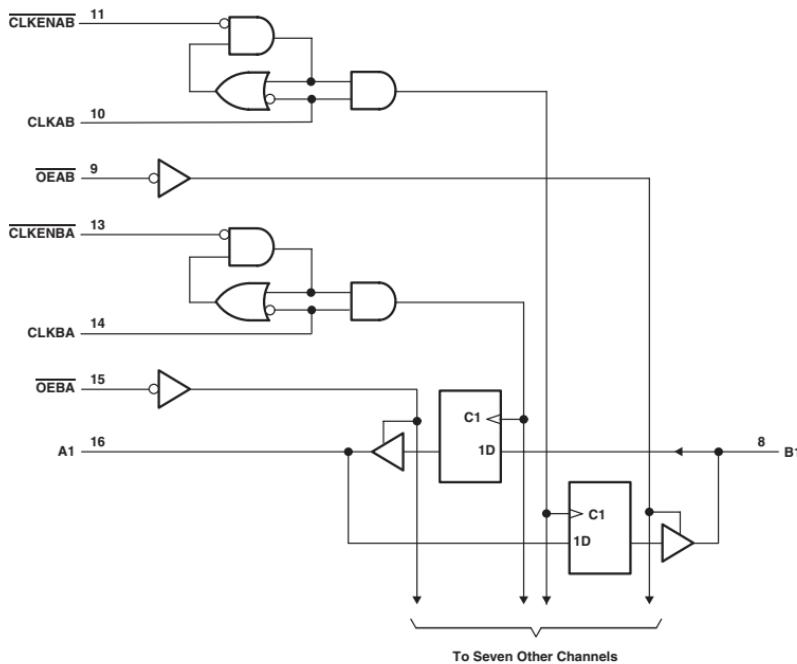
PARAMETER	INPUT	OUTPUT	MAX or MIN	SN74 BCT
t <sub>PLH</sub>	A	Y	MAX	6.6
t <sub>PHL</sub>				5
t <sub>PZH</sub>	OE	Y	MAX	9
t <sub>PZL</sub>				11.5
t <sub>PHZ</sub>	OE	Y	MAX	10.8
t <sub>PZL</sub>				8.7

UNIT: ns

## OCTAL BUS TRANSCEIVERS AND REGISTERS WITH 3-STATE OUTPUTS

- Two 8-Bit Back-to-Back Registers Store Data Flowing in Both Directions
- Noninverting Outputs
- 3-State Outputs

Logic Diagram



FUNCTION TABLE†

INPUTS				OUTPUT B
CLKENAB	CLKAB	OEAB	A	
H	X	L	X	B <sub>0</sub>
X	H or L	L	X	B <sub>0</sub>
L	↑	L	L	L
L	↑	L	H	H
X	X	H	X	Z

† A-to-B data flow is shown; B-to-A data flow is similar but uses CLKENBA, CLKBA, and OEBA.

‡ Level of B before the indicated steady-state input conditions were established

## ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER		MAX or MIN	SN74 BCT	ABT	LVTH 3V	LVC 3V	UNIT
I <sub>CC</sub>		MAX	55	35	5	0.01	mA
I <sub>OH</sub>	A	MAX	-3	-32	-32	-24	mA
	B		-15	-32	-32	-24	mA
I <sub>OL</sub>	A	MAX	24	64	64	24	mA
	B		64	64	64	24	mA

## TIMING REQUIREMENTS AND SWITCHING CHARACTERISTICS

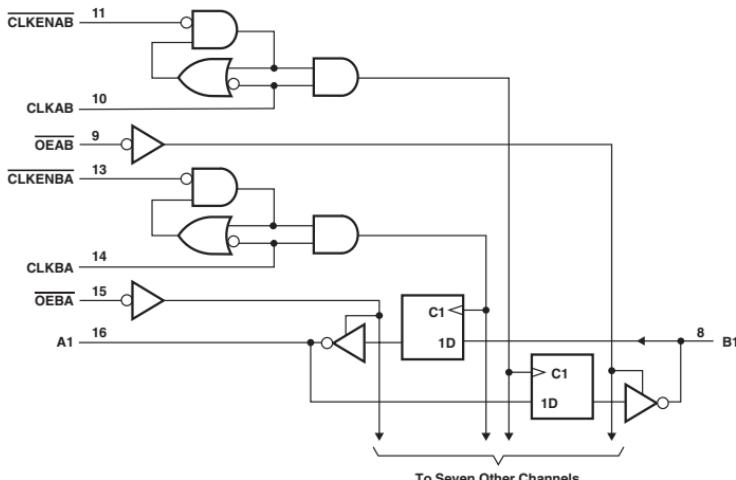
PARAMETER	INPUT	OUTPUT	MAX or MIN	SN74 BCT	ABT	LVTH 3V	LVC 3V	
t <sub>max</sub>			MIN	125	150	150	150	
t <sub>w</sub>	CLK "H"		MIN	4	3.3	3.3	3.3	
	CLK "L"			4	3.3	3.3	3.3	
t <sub>su</sub>	A or B before CLK High		MIN	2.5	2.5	1.5	1.3	
	A or B before CLK Low			2.5	2.5	1.5	-	
	CLKENAB or CLKENB̄ High			2	3	1.5	1.1	
	CLKENAB or CLKENB̄ Low			2	3	1.9	-	
t <sub>b</sub>	A or B after CLK		MIN	1.5	1.5	1	1.1	
	CLKENAB or CLKENB̄			2.5	2	1.2	1.1	
t <sub>PLH</sub>	CLKBA	A,B	MAX	9	5.9	4.6	8.2	
				10.5	6.3	4.6	8.2	
t <sub>PHL</sub>	CLKAB	A,B	MAX	8.2	5.6	4.6	7.8	
				12.9	6.6	4.6	7.8	
t <sub>PZH</sub>	OEBA	A,B	MAX	8.4	6.4	5.4	7.8	
				7	6.2	5.1	7.8	

UNIT f<sub>max</sub> : MHz other : ns

## OCTAL BUS TRANSCEIVER AND REGISTER WITH 3-STATE OUTPUTS

- Two 8-Bit, Back-to-Back Registers Store Data Flowing in Both Directions
- Inverting Outputs
- 3-State Outputs

Logic Diagram



FUNCTION TABLE†

INPUTS				OUTPUT B
OEAB	CLKAB	OEAB	A	
H	↑	L	X	A <sub>0</sub>
L	↑	L	L	H
L	↑	L	H	L
X	X	H	X	Z

† A-to-B data flow is shown; B-to-A data flow is similar but uses CEBA, CLKBA, and OEBA.

‡ Level of B before the indicated steady-state input conditions were established

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	SN74 BCT	UNIT
I <sub>cc</sub>	MAX	55	mA
I <sub>OH</sub>	MAX	-3	mA
		-15	mA
I <sub>OL</sub>	MAX	24	mA
		64	mA

TIMING REQUIREMENTS AND SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	SN74 BCT
f <sub>max</sub>			MIN	110
t <sub>tw</sub>		CLK "H"	MIN	4.5
		CLK "L"		4.5
t <sub>su</sub>		A or B High		2.5
		A or B Low		2.5
		CLKENAB or CLKENBA High	MIN	2
		CLKENAB or CLKENBA Low		2
t <sub>h</sub>		A or B	MIN	1.5
		CLKENAB or CLKENBA		2
t <sub>PLH</sub>	CLKBA	A,B	MAX	9.5
t <sub>PHL</sub>	CLKAB	A,B	MAX	10.2
t <sub>PZH</sub>	OEBA	A,B	MAX	8.8
t <sub>PZL</sub>	OEAB	A,B	MAX	14
t <sub>PHZ</sub>	OEBA	A,B	MAX	9.1
t <sub>PZ</sub>	OEAB	A,B	MAX	7.6

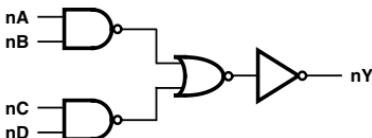
UNIT f<sub>max</sub> : MHz other : ns

# 4002

## DUAL 4-INPUT POSITIVE-NOR GATES

●  $Y = \overline{A + B + C + D}$

**Logic Diagram**



**FUNCTION TABLE**

A	B	C	D	OUTPUT
L	L	L	L	H
H	X	X	X	L
X	H	X	X	L
X	X	H	X	L
X	X	X	H	L

NOTES:

H = High Voltage Level

L = Low Voltage Level

X = Irrelevant

**ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS**

PARAMETER	MAX or MIN	SN74		UNIT
		HC	CD74	
I <sub>CC</sub>	MAX	0.02	0.04	mA
I <sub>OH</sub>	MAX	-4	-4	mA
I <sub>OL</sub>	MAX	4	4	mA

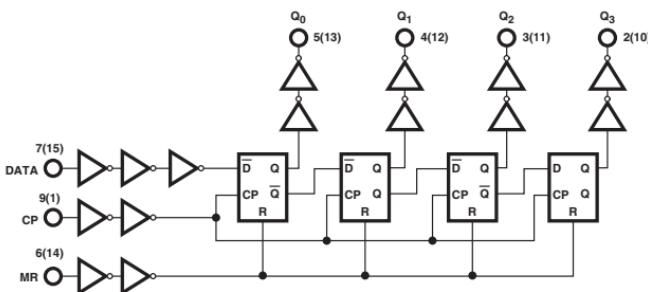
**SWITCHING CHARACTERISTICS**

PARAMETER	INPUT	OUTPUT	MAX or MIN	SN74	CD74
				HC	HC
I <sub>PLH</sub>	A, B, C, D	Y	MAX	28	30
I <sub>PHL</sub>			MAX	28	30

UNIT:ns

## DUAL 4-STAGE STATIC SHIFT REGISTER

Logic Diagram



## FUNCTION TABLE

INPUTS			OUTPUT			
CP	D	R	Q <sub>0</sub>	Q <sub>1</sub>	Q <sub>2</sub>	
↑	I	L	L	q'0	q'1	q'2
↑	h	L	H	q'0	q'1	q'2
↓	X	L	q'0	q'1	q'2	
X	X	H	L	L	L	

## NOTES:

H = High Voltage Level  
 h = High Voltage Level One Set-up Time Prior to the Low to High Clock Transition  
 L = Low Voltage Level  
 I = Low Voltage Level One Set-up Time Prior to the Low to High Clock Transition  
 X = Don't Care  
 ↑ = Low to High Clock Transition  
 ↓ = High to Low Clock Transition  
 q'n = Lower case letters indicate the state of the referenced output one set-up time prior to the Low to High clock transition.

## ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	CD74 HC	UNIT
I <sub>CC</sub>	MAX	0.16	mA
I <sub>OH</sub>	MAX	4	mA
I <sub>OL</sub>	MAX	4	mA

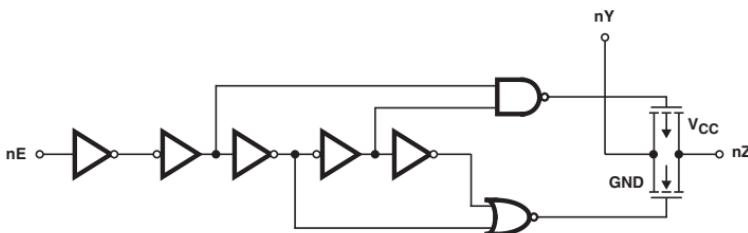
## TIMING REQUIREMENTS AND SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	CD74 HC
t <sub>max</sub>			MIN	20
t <sub>W</sub>	Clock		MIN	24
	MR			45
t <sub>SUL</sub>	Data-In to CP		MIN	18
t <sub>SUH</sub>			MIN	18
t <sub>H</sub>	Data-In to CP		MIN	0
t <sub>PLH</sub>	Clock	Q <sub>n</sub>	MAX	54
t <sub>PHL</sub>			MAX	54
t <sub>PLH</sub>	MR	Q <sub>n</sub> (Clock High)	MAX	83
t <sub>PHL</sub>			MAX	83
t <sub>PLH</sub>	MR	Q <sub>n</sub> (Clock Low)	MAX	98
t <sub>PHL</sub>			MAX	98

UNIT f<sub>max</sub> : MHz other : ns

## QUAD BILATERAL SWITCH

Logic Diagram



## FUNCTION TABLE

INPUT nE	SWITCH
L	OFF
H	ON

## NOTES:

H = High Level Voltage  
L = Low Level Voltage

## ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

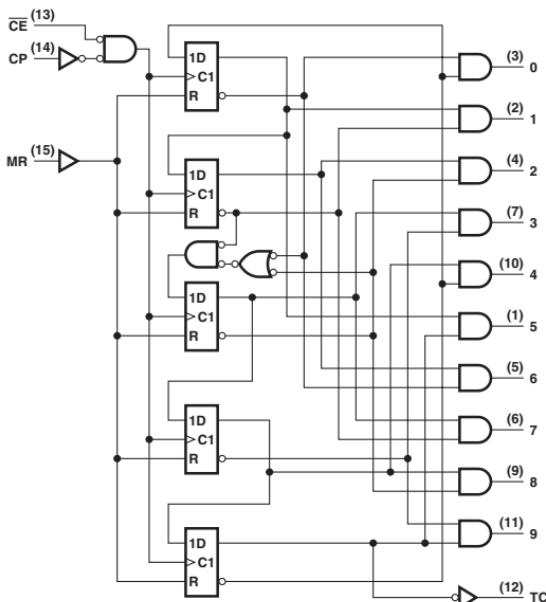
PARAMETER	MAX or MIN	CD74 HC	UNIT
I <sub>CC</sub>	MAX	0.04	mA
R <sub>ON</sub>	MAX	480	Ω

## SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	CD74 HC
I <sub>PLH</sub>	Switch In	Switch Out	MAX	18
I <sub>PHL</sub>			MAX	18
I <sub>PZH</sub>	En	Z	MAX	57
I <sub>PZL</sub>			MAX	57
I <sub>PHZ</sub>	En	Z	MAX	44
I <sub>PZL</sub>			MAX	44

UNIT: ns

Logic Diagram



FUNCTION TABLE

CP	INPUTS	OUTPUT STATE†	
	CE	MR	
L	X	L	No Change
X	H	L	No Change
X	X	H	"0" = H, "1"- "9" = L
↑	L	L	Increments Counter
↓	X	L	No Change
X	↑	L	No Change
H	↓	L	Increments Counter

## NOTES:

H = High Level

L = Low Level

↑ = High to Low Transition

↓ = Low to High Transition

X = Don't Care

† If n &lt; 5 TC = H, Otherwise = L

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	SN74 HC	CD74 HC	UNIT
I <sub>CC</sub>	MAX	0.08	0.16	mA
I <sub>OH</sub>	MAX	-4	-4	mA
I <sub>OL</sub>	MAX	4	4	mA

TIMING REQUIREMENTS AND SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	SN74	CD74
				HC	HC
f <sub>max</sub>			MIN	25	20
t <sub>tr</sub>	CP		MIN	20	24
				20	24
t <sub>ts</sub>	CE to CP		MIN	13	22
				13	-
t <sub>th</sub>	CE to CP		MIN	5	0
t <sub>PLH</sub>	CP	0 to 9	MAX	58	69
				58	69
t <sub>PHL</sub>	CE	0 to 9	MAX	63	75
				63	75
t <sub>PHL</sub>	MR	0 to 9	MAX	58	69
				58	69
t <sub>PHL</sub>	MR	TC	MAX	-	69
				58	69

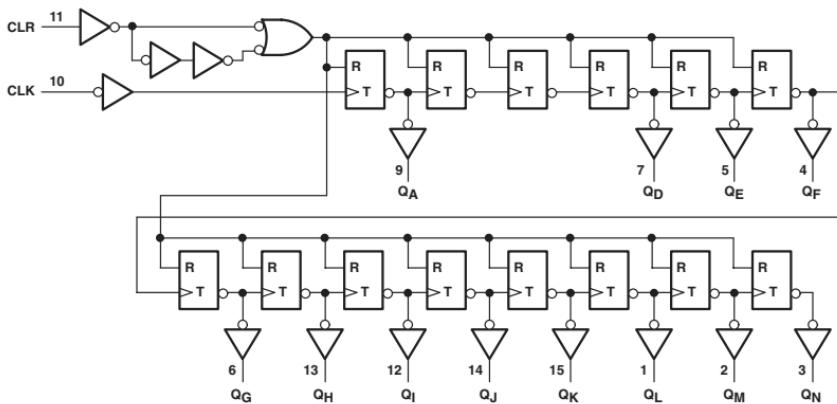
UNIT f<sub>max</sub> : MHz, other : ns

■ OBSOLETE or NOT RECOMMENDED NEW DESIGNS

## 14-STAGE BINARY COUNTERS

- Same Pinouts as CMOS4020
- $V_{CC}$ : 2V to 6V

Logic Diagram (SN74HC)



FUNCTION TABLE (SN74)

CLK	CLR	OUTPUT
↑	L	No Change
↓	L	Advance to Next State
X	H	All Outputs Are Low

NOTE: H = High Voltage Level, L = Low Voltage Level,  
 X = Don't Care, = ↑ Transition from Low to High Level,  
 ↓ = Transition from High to Low.

## ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	SN74 HC	CD74 HC	CD74 HCT	UNIT
$I_{CC}$	MAX	0.08	0.16	0.16	mA
$I_{OH}$	MAX	-4	-4	-4	mA
$I_{OL}$	MAX	4	4	4	mA

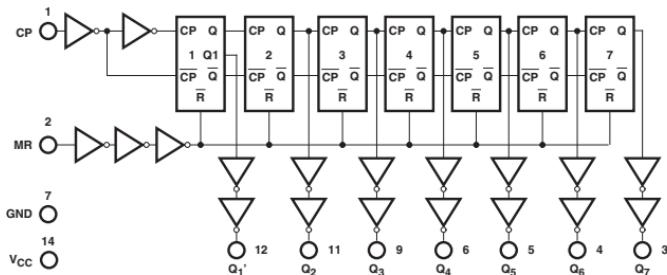
## TIMING REQUIREMENTS AND SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	SN74 HC	CD74 HC	CD74 HCT
$t_{max}$	CLK (CD74: CP) CLR high	CLR inactive before CLK ↓	MIN	22	20	16
			MIN	23	24	30
			MIN	18	24	30
$t_{tu}$	CLK (CD74: CP)	Q <sub>A</sub> (CD74: Q <sub>i</sub> )	MIN	15	-	-
$t_{PLH}$	CLK (CD74: CP)		MAX	38	42	60
$t_{PHL}$	CLR (CD74: CP)	Any	MAX	38	42	60
$t_{PLH}$	CLR (CD74: CP)	Any	MAX	35	51	60

UNIT  $t_{max}$  : MHz other : ns

## 7-STAGE BINARY COUNTERS

Logic Diagram



FUNCTION TABLE (SN74)

CLK	CLR	OUTPUT
$\uparrow$	L	No Change
$\downarrow$	L	Advance to Next State
X	H	All Outputs Are Low

NOTE: H = High Voltage Level, L = Low Voltage Level.

X = Don't Care,  $\uparrow$  = Transition from Low to High Level. $\downarrow$  = Transition from High to Low.

## ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	SN74 HC	CD74 HC	CD74 HCT	UNIT
$I_{CC}$	MAX	0.08	0.16	0.16	mA
$I_{OH}$	MAX	-4	-4	-4	mA
$I_{OL}$	MAX	4	4	4	mA

## TIMING REQUIREMENTS AND SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	SN74 HC	CD74 HC	CD74 HCT
$t_{max}$			MIN	22	20	16
$t_w$	CP (CLK)		MIN	23	24	30
	MR (CLR H)		MIN	20	24	30
$t_{su}$	CLR low before CLK		MIN	20	-	-
$t_{PLH}$	CP (CLK)	Q1 (QA)	MAX	30	42	60
$t_{PHL}$			MAX	30	42	60
$t_{PLH}$	MR (CLR)	any Q	MAX	-	51	60
$t_{PHL}$			MAX	33	51	60

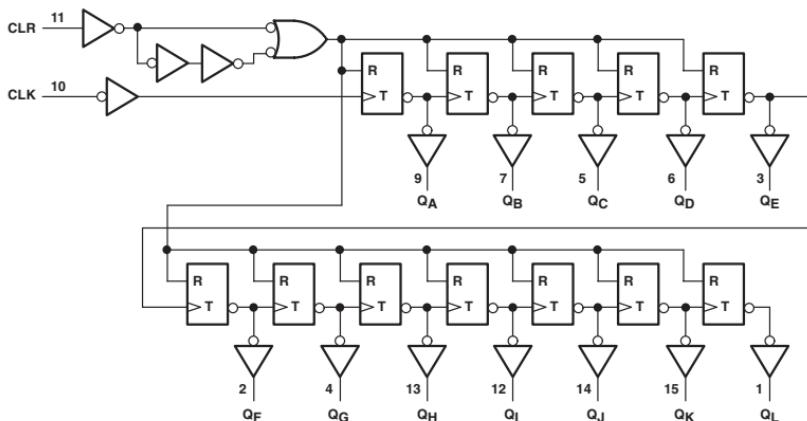
UNIT  $t_{max}$ : MHz, other : ns

# 4040

## 12-STAGE BINARY COUNTERS

- Same Pinouts as CMOS4040
- $V_{CC}$ : 2V to 6V

Logic Diagram (SN74HC)



FUNCTION TABLE

CLK	CLR	OUTPUT
↑	L	No Change
↓	L	Advance to Next State
X	H	All Outputs Are Low

NOTE: H = High Voltage Level, L = Low Voltage Level,  
X = Don't Care, ↑ = Transition from Low to High Level,  
↓ = Transition from High to Low.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

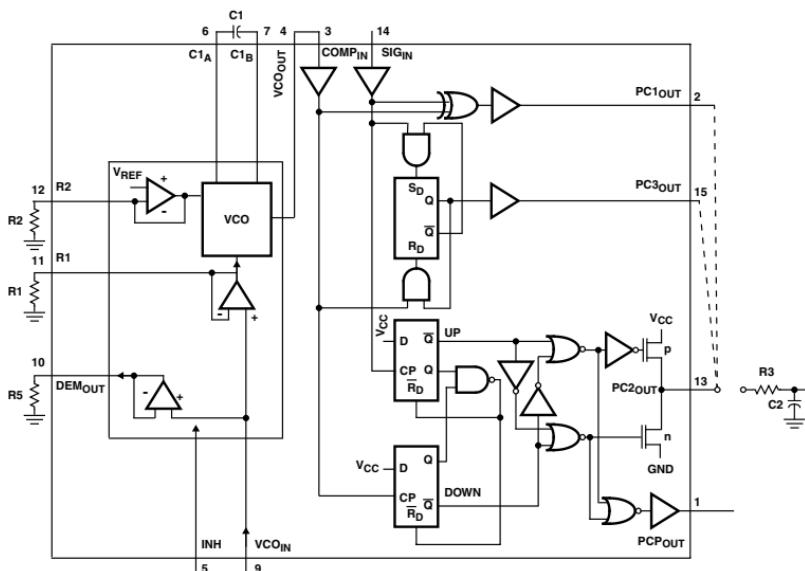
PARAMETER	MAX or MIN	SN74 HC	CD74 HC	CD74 HCT	LV 3V	LV 5V	UNIT
$I_{CC}$	MAX	0.08	0.16	0.16	-	0.02	mA
$I_{OH}$	MAX	-4	-4	-4	-6	-12	mA
$I_{OL}$	MAX	4	4	4	6	12	mA

TIMING REQUIREMENTS AND SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	SN74 HC	CD74 HC	CD74 HCT	LV 3V	LV 5V
$t_{max}$			MIN	22	20	16	50	80
			MIN	23	24	30	5	5
			MIN	18	24	30	5	5
$t_{w}$	CLK (CP)	CLR(MR) high	MIN	15	-	-	5	5
			MAX	38	42	60	17.5	10.5
$t_{wU}$	CLK (CP)	QA (Q1)	MAX	38	42	60	17.5	10.5
			MAX	35	51	60	18.5	12
UNIT $t_{max}$ : MHz other : ns								

## PHASE-LOCKED-LOOP WITH VCO

Logic Diagram



Pin Descriptions

PIN NUMBER	SYMBOL	NAME AND FUNCTION
1	$PCP_{OUT}$	Phase Comparator Pulse Output
2	$PC1_{OUT}$	Phase Comparator 1 Output
3	COMPIN	Comparator Input
4	$VCO_{OUT}$	VCO Output
5	INH	Inhibit Input
6	$C1_A$	Capacitor C1 Connection A
7	$C1_B$	Capacitor C1 Connection B
8	GND	Ground (0V)
9	$VCO_{IN}$	VCO Input
10	$DEM_{OUT}$	Demodulator Output
11	$R_1$	Resistor R1 Connection
12	$R_2$	Resistor R2 Connection
13	$PC2_{OUT}$	Phase Comparator 2 Output
14	SIGIN	Signal Input
15	$PC3_{OUT}$	Phase Comparator 3 Output
16	$V_{CC}$	Positive Supply Voltage

## ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	CD74 HC	CD74 HCT	UNIT
I <sub>CC</sub>	MAX	0.16	0.16	mA
I <sub>OH</sub>	MAX	-4	-4	mA
I <sub>OL</sub>	MAX	4	4	mA

## SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	CD74 HC	CD74 HCT
t <sub>PLH</sub>	SIG <sub>IN</sub>	PC1OUT	MAX	60	68
	COMPIN			60	68
t <sub>PHL</sub>	SIG <sub>IN</sub>	PCP <sub>OUT</sub>	MAX	90	102
	COMPIN			90	102
t <sub>PLH</sub>	SIG <sub>IN</sub>	PC3OUT	MAX	74	87
	COMPIN			74	87
t <sub>T1H</sub>	A	Y	MAX	22	22
t <sub>T1L</sub>				22	22
t <sub>PZH</sub>	SIG <sub>IN</sub>	PC2OUT	MAX	80	90
	COMPIN			80	90
t <sub>PZL</sub>	SIG <sub>IN</sub>	PC2OUT	MAX	95	102
	COMPIN			95	102

UNIT:ns

## 4049

### HEX INVERTING BUFFERS

Logic Diagram



ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	CD74 HC	UNIT
$I_{CC}$	MAX	0.04	mA
$I_{OH}$	MAX	-4	mA
$I_{OL}$	MAX	4	mA

SWITCHING CHARACTERISTICS

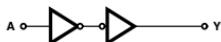
PARAMETER	INPUT	OUTPUT	MAX or MIN	CD74 HC
$t_{PLH}$	nA	nY	MAX	26
$t_{PHL}$				26

UNIT:ns

## 4050

### HEX NON-INVERTING BUFFERS

Logic Diagram



ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	CD74 HC	UNIT
$I_{CC}$	MAX	0.04	mA
$I_{OH}$	MAX	-4	mA
$I_{OL}$	MAX	4	mA

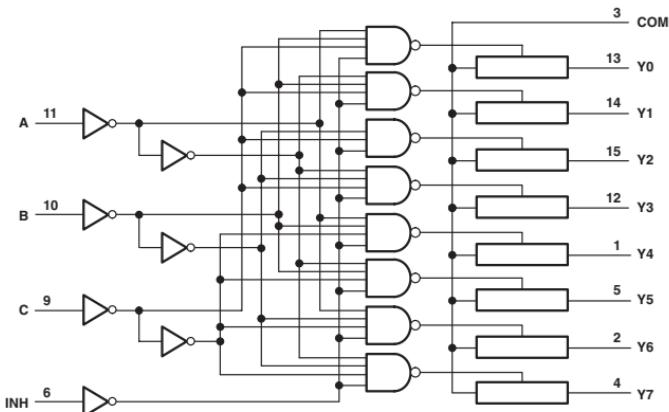
SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	CD74 HC
$t_{PLH}$	nA	nY	MAX	26
$t_{PHL}$				26

UNIT:ns

## 8-CHANNEL ANALOG MULTIPLEXERS / DEMULTIPLEXERS

Logic Diagram (SN74LV)

FUNCTION TABLE  
(SN74)

INPUTS			ON CHANNEL
INH	C	B	A
L	L	L	L
L	L	L	H
L	L	H	L
L	L	H	H
L	H	L	L
L	H	L	H
L	H	H	L
L	H	H	H
H	X	X	X

## ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	CD74 HC	CD74 HCT	LV 3V	LV 5V	UNIT
I <sub>CC</sub>	MAX	0.16	0.16	-	0.02	mA
R <sub>ON</sub>	MAX	180	180	190	100	Ω

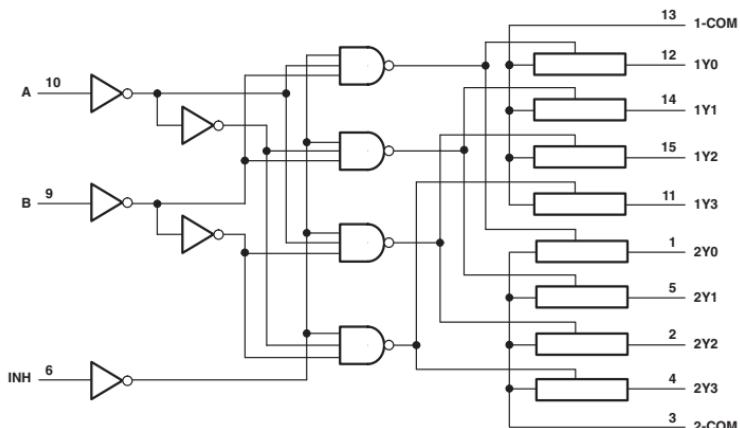
## SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	CD74 HC	CD74 HCT	LV 3V	LV 5V
I <sub>PLH</sub>	COM or Y <sub>n</sub> (An)	Y <sub>n</sub> (An) or COM	MAX	18	18	12	8
I <sub>PHL</sub>				18	18	12	8
I <sub>PZH</sub>	INH	COM or Y <sub>n</sub> (An)	MAX	68	83	25	18
I <sub>PZL</sub>				68	83	25	18
I <sub>PHZ</sub>	INH	COM or Y <sub>n</sub> (An)	MAX	68	68	25	18
I <sub>PLZ</sub>				68	68	25	18

UNIT: ns

## DUAL 4-CHANNEL ANALOG MULTIPLEXERS / DEMULTIPLEXERS

Logic Diagram (SN74LV)

FUNCTION TABLE  
(SN74)

INPUTS			ON CHANNEL
INH	B	A	
L	L	L	1Y0, 2Y0
L	L	H	1Y1, 2Y1
L	H	L	1Y2, 2Y2
L	H	H	1Y3, 2Y3
H	X	X	None

## ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

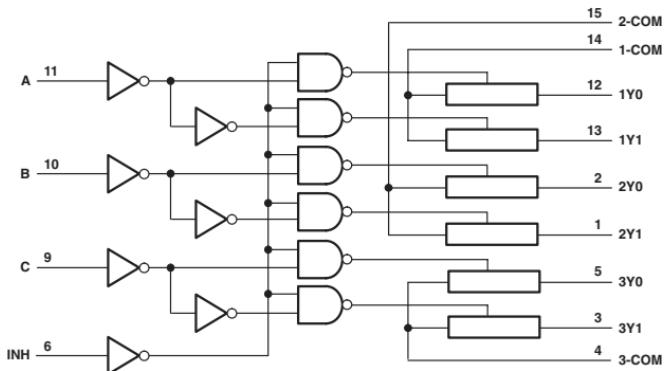
PARAMETER	MAX or MIN	CD74 HC	CD74 HCT	LV 3V	LV 5V	UNIT
$I_{CC}$	MAX	0.16	0.16	-	0.02	mA
$R_{ON}$	MAX	180	180	190	100	$\Omega$

## SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	CD74 HC	CD74 HCT	LV 3V	LV 5V
$t_{PLH}$	COM or $Y_n$ (An)	$Y_n$ (An) or COM	MAX	18	18	12	8
				18	18	12	8
$t_{PHL}$	INH	COM or $Y_n$ (An)	MAX	98	105	25	18
				98	105	25	18
$t_{PZH}$	INH	COM or $Y_n$ (An)	MAX	75	75	25	18
				75	75	25	18
UNIT: ns							

## TRIPLE 2-CHANNEL ANALOG MULTIPLEXERS/DEMULITPLEXERS

Logic Diagram (SN74LV)

FUNCTION TABLE  
(SN74)

INPUTS			ON CHANNEL
INH	C	B	A
L	L	L	L
L	L	L	H
L	L	H	L
L	L	H	H
L	H	L	L
L	H	L	H
L	H	H	L
L	H	H	H
H	X	X	X

Legend: L = Low, H = High, X = Don't care, None = No connection.

## ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	CD74 HC	CD74 HCT	LV 3V	LV 5V	UNIT
I <sub>CC</sub>	MAX	0.16	0.16	-	0.02	mA
R <sub>ON</sub>	MAX	180	180	190	100	Ω

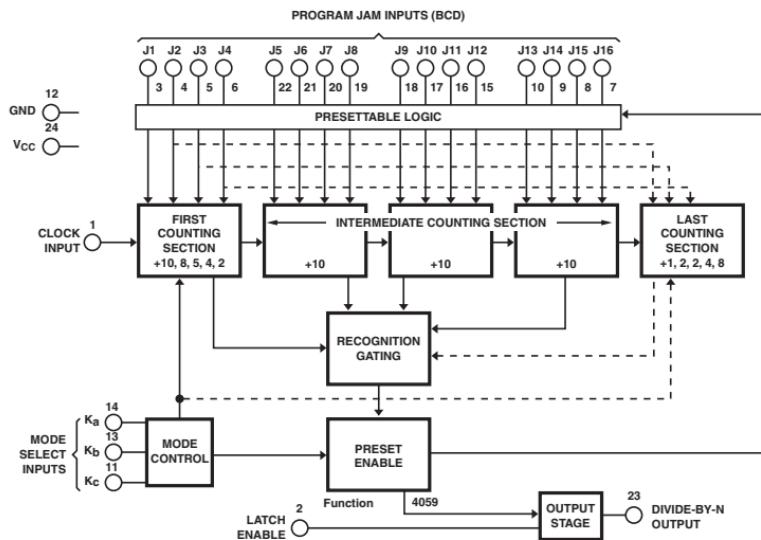
## SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	CD74 HC	CD74 HCT	LV 3V	LV 5V
I <sub>PLH</sub>	COM or Y <sub>n</sub> (A <sub>n</sub> , B <sub>n</sub> , C <sub>n</sub> )	Y <sub>n</sub> (A <sub>n</sub> , B <sub>n</sub> , C <sub>n</sub> ) or COM	MAX	18	18	12	8
I <sub>PHL</sub>				18	18	12	8
I <sub>PZH</sub>	INH	COM or Y <sub>n</sub> (A <sub>n</sub> , B <sub>n</sub> , C <sub>n</sub> )	MAX	66	72	25	18
I <sub>ZL</sub>				66	72	25	18
I <sub>PZ</sub>	INH	COM or Y <sub>n</sub> (A <sub>n</sub> , B <sub>n</sub> , C <sub>n</sub> )	MAX	63	66	25	18
I <sub>LZ</sub>				63	66	25	18

UNIT: ns

## CMOS PROGRAMMABLE DIVIDE-BY-N COUNTER

## Function Diagram



FUNCTION TABLE

MODE	SELECT	INPUT
K <sub>a</sub>	K <sub>b</sub>	K <sub>c</sub>
H	H	H
L	H	H
H	L	H
L	L	H
H	H	L
X	L	L

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	CD74 HC	UNIT
I <sub>CC</sub>	MAX	0.16	mA
I <sub>OH</sub>	MAX	-4	mA
I <sub>OL</sub>	MAX	4	mA

TIMING REQUIREMENTS AND SWITCHING CHARACTERISTICS

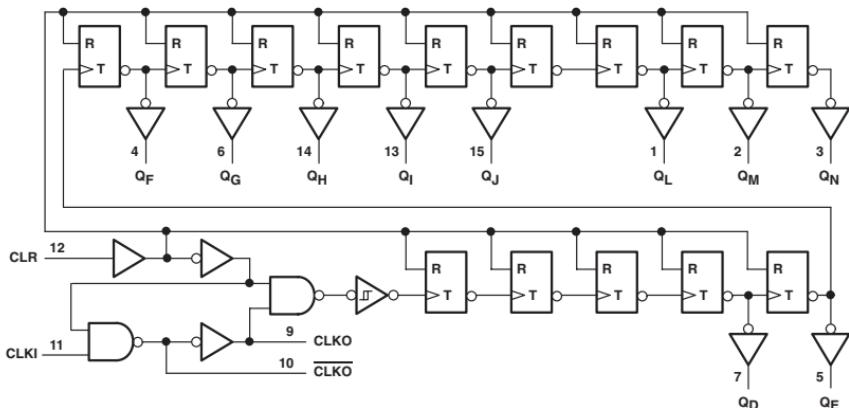
PARAMETER	INPUT	OUTPUT	MAX or MIN	CD74 HC
t <sub>max</sub>	CP		MIN	18
t <sub>w</sub>	CP		MIN	27
t <sub>su</sub>	K <sub>b</sub> , K <sub>c</sub> to CP		MIN	22
t <sub>PLH</sub>	CP	Q	MAX	60
t <sub>PHL</sub>	CP	Q	MIN	60
t <sub>PLH</sub>	LE	Q	MAX	53
t <sub>PHL</sub>	LE	Q	MIN	53

UNIT f<sub>max</sub> : MHz other : ns

## ASYNCHRONOUS 14-STAGE BINARY COUNTERS AND OSCILLATORS

- Same Pinouts as CMOS4060
- Allow Design of Either RC or Crystal Oscillator Circuits
- $V_{CC}$ : 2V to 6V

Logic Diagram (SN74HC)



FUNCTION TABLE (SN74)

INPUTS		OUTPUTS		
CLKI	CLR	$Q_D$ to $Q_N$	CLKO	$\overline{CLKO}$
$\uparrow$	L	No Change	$\uparrow$	$\downarrow$
$\downarrow$	L	Advance to Next State	$\downarrow$	$\uparrow$
X	H	All Outputs are Low	L	H

## ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	SN74 HC	CD74 HC	CD74 HCT	UNIT
$I_{CC}$	MAX	0.08	0.16	0.16	mA
$I_{OH}$	MAX	-4	-4	-4	mA
$I_{OL}$	MAX	4	4	4	mA

## TIMING REQUIREMENTS AND SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	SN74 HC	CD74 HC	CD74 HCT
$t_{max}$			MIN	22	20	20
$t_{tr}$	CLKI ( $\phi_1$ )		MIN	23	24	24
	CLR high (MR)			23	24	38
$t_{tu}$	CLR inactive before CLK $\downarrow$		MIN	40	-	-
$t_{PLH}$	CLKI ( $\phi_1$ )	$Q_D$ (Q4)	MAX	123	90	100
$t_{PHL}$	CLKI ( $\phi_1$ )	$Q_D$ (Q4)	MAX	123	90	100
$t_{PHL}$	CLR (MR)	Any	MAX	35	53	66

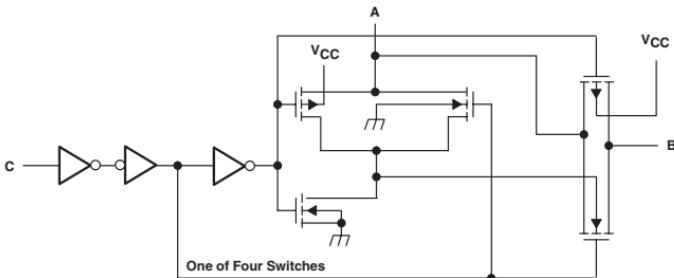
UNIT  $t_{max}$  : MHz other : ns

4066

## QUADRUPLE BILATERAL SWITCHES

- Same Pinouts as CMOS4016, 4066
  - Low On-State Impedance:  $50\text{-}\Omega$  TYP at  $V_{CC} = 6V$
  - Individual Switch Controls
  - Extremely Low Input Current
  - High On-Off Output Voltage Ratio
  - Low Crosstalk Between Switches

## Logic Diagram (SN74)



## FUNCTION TABLE (SN74)

FUNCTION TABLE (CH 4)	
INPUT (C)	SWITCH
L	OFF
H	ON

**NOTE:**

H = High Level

L = Low Level

## ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	SN74 HC	CD74 HC	CD74 HCT	AHC	LV 3V	LV 5V	UNIT
$I_{CC}$	MAX	0.02	0.04	0.04	0.02	-	0.02	mA
$R_{ON}$	MAX	106	128	128	100	190	100	$\Omega$

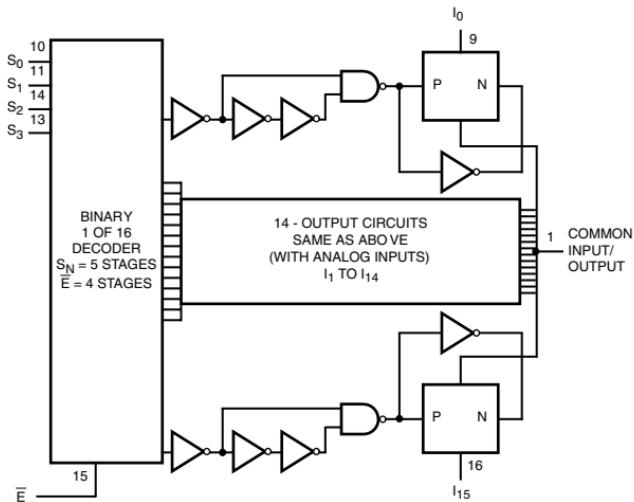
## SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	SN74 HC	CD74 HC	CD74 HCT	AHC	LV 3V	LV 5V
tPLH	A or B (Y or Z)	B or A (Z or Y)	MAX	15	18	18	8	12	8
				15	18	18	8	12	8
tPZH	C (E)	A or B (Y or Z)	MAX	45	30	36	16	22	16
				45	30	36	16	22	16
tPHZ	C (E)	A or B (Y or Z)	MAX	50	45	53	16	22	16
				50	45	53	16	22	16

UNIT-1

## 16-CHANNEL ANALOG MULTIPLEXER/DEMULTIPLEXER

Function Diagram



FUNCTION TABLE

<b>S0</b>	<b>S1</b>	<b>S2</b>	<b>S3</b>	<b>E</b>	<b>SELECTED CHANNEL</b>
X	X	X	X	X	None
0	0	0	0	0	0
1	0	0	0	0	1
0	1	0	0	0	2
1	1	0	0	0	3
0	0	1	0	0	4
1	0	1	0	0	5
0	1	1	0	0	6
1	1	1	0	0	7
0	0	0	1	0	8
1	0	0	1	0	9
0	1	0	1	0	10
1	1	0	1	0	11
0	0	1	1	0	12
1	0	1	1	0	13
0	1	1	1	0	14
1	1	1	1	0	15

NOTES:

H = High Level

L = Low Level

X = Don't Care

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	CD74 HC	CD74 HCT	UNIT
$I_{CC}$	MAX	0.16	0.16	mA
$R_{ON}$	MAX	240	240	$\Omega$

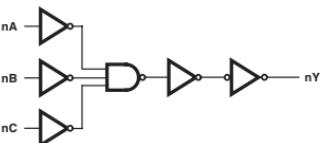
SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	CD74 HC	CD74 HCT
$t_{PLH}$	Switch In	COMON I/O	MAX	22	22
$t_{PHL}$			MAX	22	22
$t_{PZH}$	$\bar{E}$	COMON I/O	MAX	83	90
$t_{PZL}$			MAX	83	90
$t_{PZH}$	$\bar{E}$	COMON I/O	MAX	83	83
$t_{PZL}$			MAX	83	83
$t_{PHZ}$	Sn	COMON I/O	MAX	90	90
$t_{PZL}$			MAX	90	90
$t_{PHZ}$	Sn	COMON I/O	MAX	87	87
$t_{PZL}$			MAX	87	87

UNIT: ns

# 4075

## Logic Diagram



### TRIPLE 3-INPUT OR GATES

- $\bullet \quad Y = A + B + C$

**FUNCTION TABLE**

INPUTS			OUTPUT
A	B	C	Y
L	L	L	L
H	X	X	H
X	H	X	H
X	X	H	H

**NOTES:**

H = High Voltage Level

L = Low Voltage Level

X = Don't Care

**ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS**

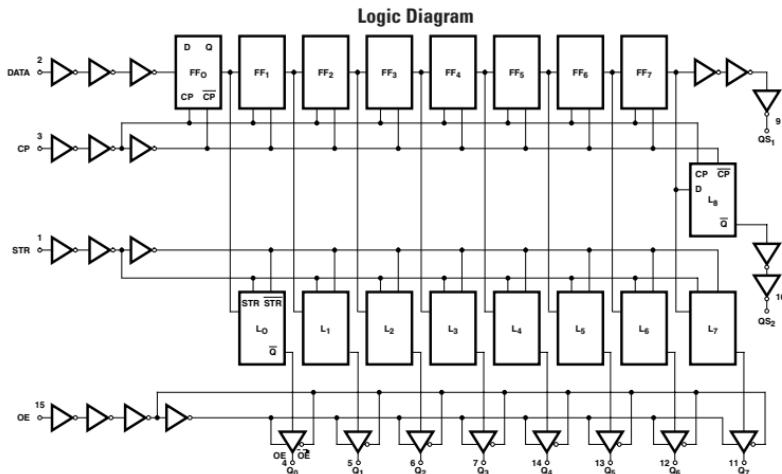
PARAMETER	MAX or MIN	SN74 HC	CD74 HC	CD74 HCT	UNIT
$I_{CC}$	MAX	0.02	0.04	0.04	mA
$I_{OH}$	MAX	-4	-4	-4	mA
$I_{OL}$	MAX	4	4	4	mA

**SWITCHING CHARACTERISTICS**

PARAMETER	INPUT	OUTPUT	MAX or MIN	SN74 HC	CD74 HC	CD74 HCT
$t_{PLH}$	A, B or C	Y	MAX	25	30	36
$t_{PHL}$	A, B or C	Y	MAX	25	30	36

UNIT:ns

## 8-STAGE SHIFT AND STORE BUS REGISTER, THREE-STATE

**FUNCTION TABLE**

INPUTS			PARALLEL OUTPUT		SERIAL OUTPUT		
CP	OE	STR	D	Q <sub>0</sub>	Q <sub>n</sub>	QS <sub>1</sub> †	QS <sub>2</sub>
↑	L	X	X	Z	Z	Q' <sub>6</sub>	NC
↓	L	X	X	Z	Z	NC	Q' <sub>7</sub>
↑	H	L	X	NC	NC	Q' <sub>6</sub>	NC
↑	H	H	L	L	Q <sub>n-1</sub>	Q' <sub>6</sub>	NC
↑	H	H	H	H	Q <sub>n-1</sub>	Q' <sub>6</sub>	NC
↓	H	H	H	NC	NC	NC	Q' <sub>7</sub>

NOTES:

† H = High Voltage Level, L = Low Voltage Level, X = Don't Care, NC = No charge, Z = High Impedance Off-state.

↑ = Transition from Low to High Level, ↓ = Transition from High Low.

‡ At the positive clock edge the information in the seventh register stage is transferred to the eighth register stage and QS<sub>1</sub> output.**ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS**

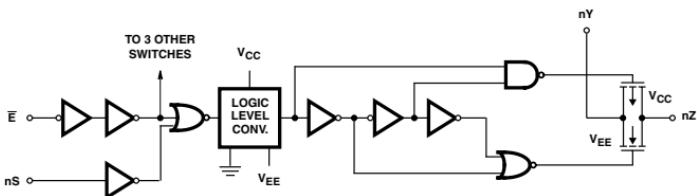
PARAMETER	MAX or MIN	CD74 HC	CD74 HCT	UNIT
I <sub>CC</sub>	MAX	0.16	0.16	mA
I <sub>OL</sub>	MAX	4	4	mA
I <sub>OH</sub>	MAX	-4	-4	mA

**TIMING REQUIREMENTS AND SWITCHING CHARACTERISTICS**

PARAMETER	INPUT	OUTPUT	MAX or MIN	CD74 HC	CD74 HCT
t <sub>W</sub>		CP	MIN	24	24
t <sub>W</sub> H		STR	MIN	24	24
t <sub>SU</sub>	Data		MIN	15	15
	STR			30	30
t <sub>H</sub>	Data		MIN	3	4
	STR			0	0
t <sub>PLH</sub>	CP	QS <sub>1</sub>	MAX	45	-
t <sub>PHL</sub>				45	-
t <sub>PLH</sub>	CP	QS <sub>2</sub>	MAX	41	-
t <sub>PHL</sub>				41	-
t <sub>PLH</sub>	CP	Q <sub>n</sub>	MAX	59	-
t <sub>PHL</sub>				59	-
t <sub>PLH</sub>	STR	Q <sub>n</sub>	MAX	54	-
t <sub>PHL</sub>				54	-
t <sub>PZH</sub>	OE	Q <sub>n</sub>	MAX	53	-
t <sub>PZL</sub>				53	-
t <sub>PZL</sub>	OE	Q <sub>n</sub>	MAX	38	-
t <sub>PZH</sub>				38	-
			UNIT:ns		

## QUAD ANALOG SWITCH WITH LEVEL TRANSLATION

Logic Diagram



FUNCTION TABLE

INPUTS		SWITCH
E	S	
L	L	OFF
L	H	ON
H	X	OFF

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	CD74 HC	CD74 HCT	UNIT
I <sub>CC</sub>	MAX	0.32	0.32	mA
R <sub>ON</sub>	MAX	270	270	Ω

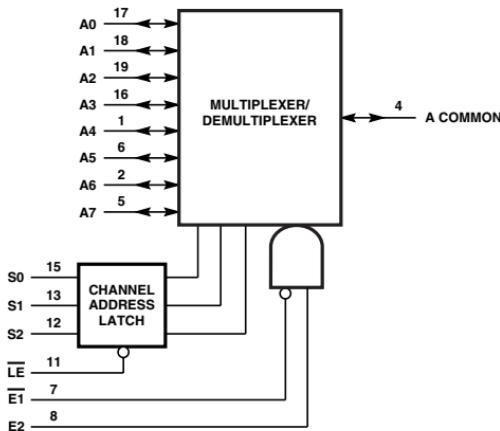
SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	CD74 HC	CD74 HCT
t <sub>PLH</sub>	Switch in	Switch out	MAX	18	18
t <sub>PHL</sub>				18	18
t <sub>PZH</sub>	E	Z	MAX	62	66
t <sub>PZL</sub>				62	85
t <sub>PZL</sub>	nS	Z	MAX	62	75
t <sub>PHZ</sub>				62	-
t <sub>PZH</sub>	nS	Z	MAX	53	60
t <sub>PZL</sub>				53	75
t <sub>PZL</sub>	nS	Z	MAX	53	-
t <sub>PHZ</sub>				53	66

UNIT:ns

## ANALOG MULTIPLEXERS/DEMULITPLEXERS WITH LATCH

## Logic Diagram



## FUNCTION TABLE

E1	E2	S2	S1	S0	INPUTS		"ON"† LE = H
					1	0	
L	H	L	L	L	A0		
L	H	L	L	H	A1		
L	H	L	H	L	A2		
L	H	L	H	H	A3		
L	H	H	L	L	A4		
L	H	H	L	H	A5		
L	H	H	H	L	A6		
L	H	H	H	H	A7		
H	L	X	X	X	None		

NOTES:

† When LE is low S0-S2 data are latched and switches cannot change state.

H = High Voltage Level, L = Low Voltage Level, X = Don't Care

## ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	CD74 HC	CD74 HCT	UNIT
IC <sub>C</sub>	MAX	0.32	0.32	mA
R <sub>ON</sub>	MAX	240	240	Ω

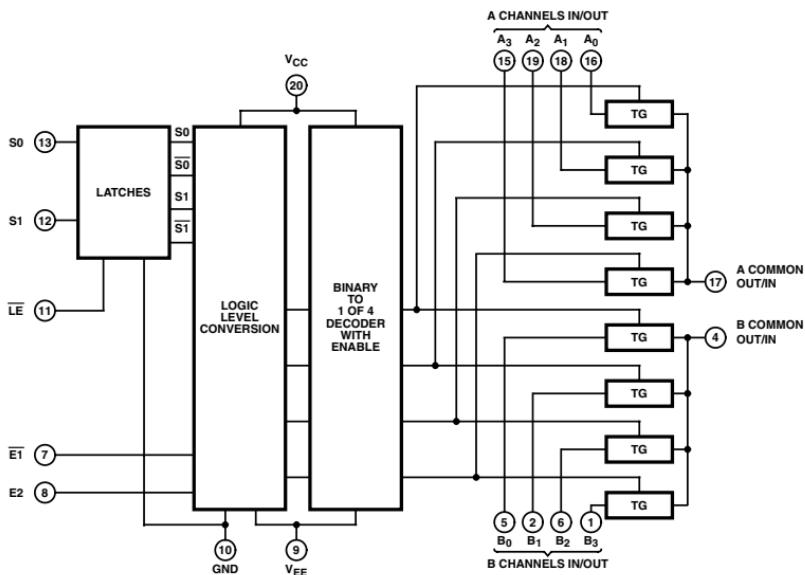
## TIMING REQUIREMENTS AND SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	CD74 HC	CD74 HCT
t <sub>W</sub>	LE		MIN	30	28
t <sub>su</sub>	S <sub>n</sub> to LE		MAX	18	18
t <sub>H</sub>	S <sub>n</sub> to LE		MIN	5	5
t <sub>PLH</sub>	Switch In	Switch Out	MAX	11	11
t <sub>PHL</sub>				11	11
t <sub>PZH</sub>	E <sub>1</sub> , E <sub>2</sub> , LE	V <sub>os</sub>	MAX	90	113
t <sub>PZL</sub>				90	113
t <sub>PZH</sub>	S <sub>n</sub>	V <sub>os</sub>	MAX	90	113
t <sub>PZL</sub>				90	113
t <sub>PLZ</sub>	E <sub>1</sub>	V <sub>os</sub>	MAX	75	83
t <sub>PHZ</sub>				75	83
t <sub>PLZ</sub>	E <sub>2</sub>	V <sub>os</sub>	MAX	75	90
t <sub>PHZ</sub>				75	90
t <sub>PLZ</sub>	LE	V <sub>os</sub>	MAX	83	90
t <sub>PHZ</sub>				83	90
t <sub>PLZ</sub>	S <sub>n</sub>	V <sub>os</sub>	MAX	83	98
t <sub>PHZ</sub>				83	98

UNIT:ns

## ANALOG MULTIPLEXERS/DEMULTIPLEXERS WITH LATCH

Function Diagram



## FUNCTION TABLE

INPUTS				"ON"† SWITCHES $\bar{E}_1 = H$
$\bar{E}_1$	$E_2$	$S_1$	$S_0$	
L	H	L	L	$A_0, B_0$
L	H	L	H	$A_1, B_1$
L	H	H	L	$A_2, B_2$
L	H	H	H	$A_3, B_3$
H	L	X	X	None

## NOTES:

† When  $\bar{E}_1$  is low  $S_0-S_2$  data are latched and switches cannot change state.  
H = High Voltage Level, L = Low Voltage Level, X = Don't Care

## ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	CD74 HC	UNIT
$I_{CC}$	MAX	0.32	mA
$R_{ON}$	MAX	240	$\Omega$

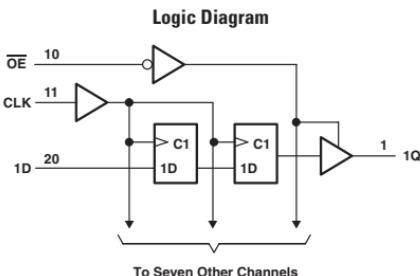
## TIMING REQUIREMENTS AND SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	CD74 HC
$t_{W}$	$\bar{E}_1$		MIN	30
$t_{SU}$	$S_n$ to $\bar{E}_1$		MIN	-
$t_H$	$S_n$ to $\bar{E}_1$		MIN	5
$t_{PLH}$	Switch In	Switch Out	MAX	11
$t_{PHL}$			MAX	11
$t_{ZH}$	$\bar{E}_1, E_2, \bar{L}_E$	$V_{OS}$	MAX	105
$t_{ZL}$			MAX	105
$t_{ZH}$	$S_n$	$V_{OS}$	MAX	113
$t_{ZL}$			MAX	113
$t_{PLZ}$	$\bar{E}_1, E_2, \bar{L}_E$	$V_{OS}$	MAX	83
$t_{PHZ}$			MAX	83

UNIT: ns

**OCTAL EDGE-TRIGGERED D-TYPE  
DUAL-RANK FLIP-FLOP WITH  
3-STATE OUTPUTS**

- 3-State Outputs Drive Bus Lines Directly



FUNCTION TABLE

INPUTS			OUTPUT
OE	CLK	D	Q
L	↑	H	H
L	↑	L	L
L	L	X	Q <sub>O</sub>
H	X	X	Z

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

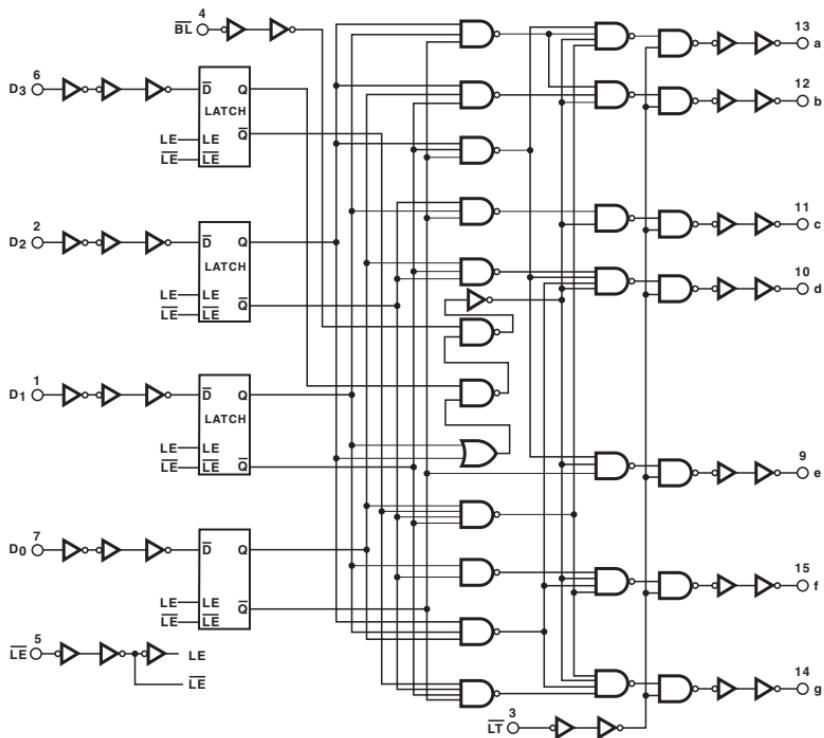
PARAMETER	MAX or MIN	AS	UNIT
I <sub>CC</sub>	MAX	150	mA
I <sub>OH</sub>	MAX	-15	mA
I <sub>OL</sub>	MAX	48	mA

TIMING REQUIREMENTS AND SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	AS
t <sub>max</sub>			MIN	125
t <sub>w</sub>			MIN	4
t <sub>su</sub>			MIN	4
t <sub>h</sub>			MIN	1
t <sub>PLH</sub>			MAX	8
t <sub>PHL</sub>	CLK	Q	MAX	8
t <sub>PZH</sub>			MAX	6
t <sub>PZL</sub>	OE	Q	MAX	8
t <sub>PHZ</sub>			MAX	6.5
t <sub>PZL</sub>	OE	Q	MAX	7

UNIT f<sub>max</sub> : MHz other : ns

Logic Diagram



FUNCTION TABLE

$\overline{LE}$	$\overline{BL}$	$\overline{LT}$	D <sub>3</sub>	D <sub>2</sub>	D <sub>1</sub>	D <sub>0</sub>	a	b	c	d	e	f	g	Display
X	X	L	X	X	X	X	H	H	H	H	H	H	H	8
X	L	H	X	X	X	X	L	L	L	L	L	L	L	Blank
L	H	H	L	L	L	L	H	H	H	H	H	L	L	0
L	H	H	L	L	L	L	H	H	L	L	L	L	L	1
L	H	H	L	L	H	L	H	H	L	L	L	H	L	2
L	H	H	L	L	H	L	H	H	H	L	L	H	H	3
L	H	H	L	H	H	L	H	H	H	L	L	H	H	4
L	H	H	L	H	L	L	H	H	L	L	H	H	H	5
L	H	H	L	H	L	L	L	H	H	H	L	H	H	6
L	H	H	L	H	H	H	H	H	L	L	L	L	L	7
L	H	H	H	L	L	L	H	H	H	H	H	H	H	8
L	H	H	H	L	L	L	H	H	L	L	H	H	H	9
L	H	H	H	L	H	L	L	L	L	L	L	L	L	Blank
L	H	H	H	H	L	L	L	L	L	L	L	L	L	Blank
L	H	H	H	H	L	L	L	L	L	L	L	L	L	Blank
L	H	H	H	H	H	L	L	L	L	L	L	L	L	Blank
L	H	H	H	H	H	L	L	L	L	L	L	L	L	Blank
H	H	H	X	X	X	X	†	†	†	†	†	†	†	†

X = Don't care

† Depends on BCD code previously applied when  $\overline{LE} = L$ 

NOTES: Display is blank for all illegal input codes (BCD &gt; HLLH).

## ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	CD74 HC	CD74 HCT	UNIT
I <sub>cc</sub>	MAX	0.16	0.16	mA
I <sub>oh</sub>	MAX	-7.4	-4	mA
I <sub>ol</sub>	MAX	4	4	mA

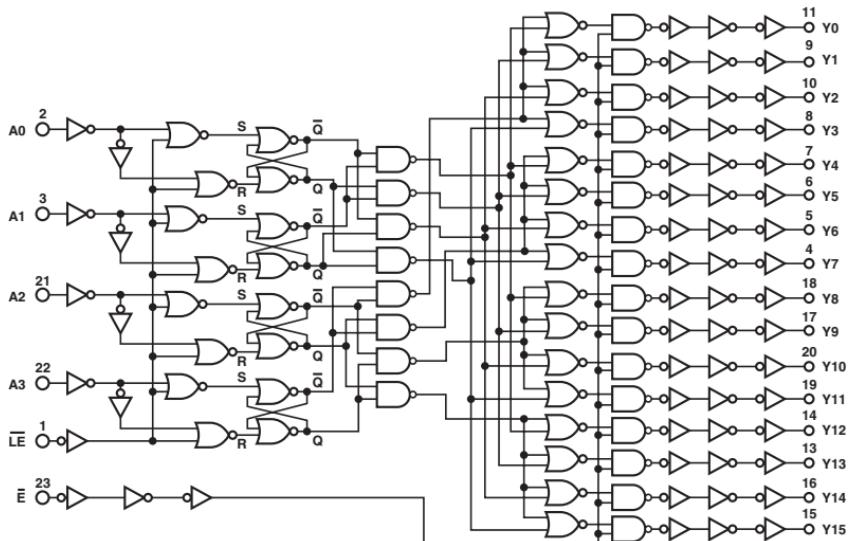
## TIMING REQUIREMENTS AND SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT		MAX or MIN	CD74 HC	CD74 HCT
		Latch Enable				
t <sub>W</sub>		Dn to $\overline{LE}$		MIN	24	24
t <sub>WU</sub>		Dn to $\overline{LE}$		MIN	18	24
t <sub>H</sub>		Dn to $\overline{LE}$		MIN	3	5
t <sub>PLH</sub>	Dn	a to g		MAX	90	90
t <sub>PHL</sub>				MAX	90	90
t <sub>PLH</sub>	$\overline{LE}$	a to g		MAX	81	81
t <sub>PHL</sub>				MAX	81	81
t <sub>PLH</sub>	$\overline{BL}$	a to g		MAX	66	66
t <sub>PHL</sub>				MAX	66	66
t <sub>PLH</sub>	$\overline{LT}$	a to g		MAX	48	50
t <sub>PHL</sub>				MAX	48	50

UNIT:ns

## 4-LINE TO 16-LINE DECODERS/DEMULTIPLEXERS WITH INPUT LATCHES

Logic Diagram

FUNCTION TABLE  
( $\bar{E} = H$ )

E	DECODER INPUTS				ADDRESSED OUTPUT H
	A3	A2	A1	A0	
L	L	L	L	L	Y0
L	L	L	H		Y1
L	L	H	L		Y2
L	L	H	H		Y3
L	L	H	L		Y4
L	L	H	H		Y5
L	L	H	L		Y6
L	L	H	H		Y7
L	H	L	L		Y8
L	H	L	H		Y9
L	H	L	L		Y10
L	H	L	H		Y11
L	H	H	L		Y12
L	H	H	L		Y13
L	H	H	H		Y14
L	H	H	H		Y15
H	X	X	X	X	All outputs = L

H = high, L = low, X = don't care

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	SN74 HC	CD74 HC	CD74 HCT	UNIT
$I_{CC}$	MAX	0.08	0.16	0.16	mA
$I_{OH}$	MAX	-4	-4	-4	mA
$I_{OL}$	MAX	4	4	4	mA

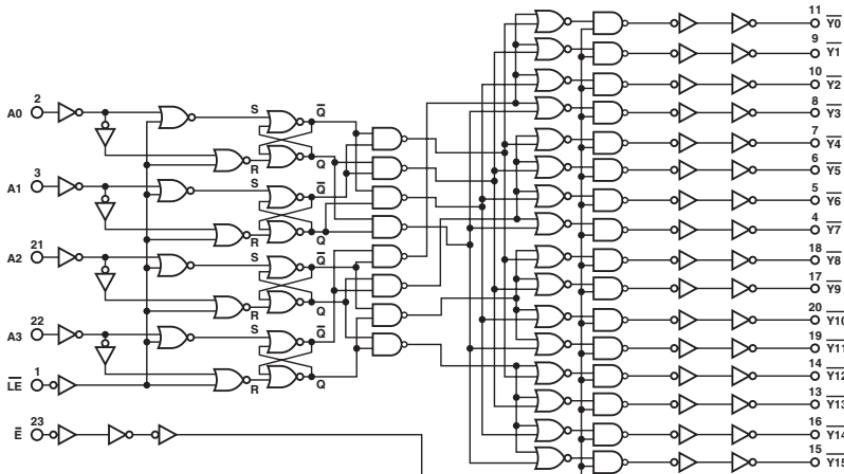
TIMING REQUIREMENTS AND SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	SN74 HC	CD74 HC	CD74 HCT
$t_{AV}$	$\bar{E}$ (LE)		MIN	20	22	45
$t_{SU}$	$\bar{E}$ (LE)		MIN	25	30	30
$t_h$	$\bar{E}$ (LE)		MIN	5	0	5
$t_{PLH}$	A0, 1, 2, 3 (A, B, C, D)	Y	MAX	58	83	83
$t_{PHL}$		Y	MAX	58	83	83
$t_{PLH}$	$\bar{E}$ (LE)	Y	MAX	58	68	75
$t_{PHL}$		Y	MAX	58	68	75
$t_{PLH}$	$\bar{E}$ (G)	Y	MAX	44	53	60
$t_{PHL}$		Y	MAX	44	53	60

UNIT:ns

## 4-LINE TO 16-LINE DECODERS/DEMULTIPLEXERS WITH INPUT LATCHES

Logic Diagram

FUNCTION TABLE  
( $\bar{L}E = H$ )

E	DECODER INPUTS				ADDRESSED OUTPUT L
	A3	A2	A1	A0	
L	L	L	L	L	Y0
L	L	L	H		Y1
L	L	H	L		Y2
L	L	L	H		Y3
L	L	H	L		Y4
L	L	H	H		Y5
L	L	H	H	L	Y6
L	L	H	H	H	Y7
L	H	L	L		Y8
L	H	L	L	H	Y9
L	H	L	H	L	Y10
L	H	L	H	H	Y11
L	H	H	L	L	Y12
L	H	H	L	H	Y13
L	H	H	H	L	Y14
L	H	H	H	H	Y15
H	X	X	X	X	All outputs = H

H = high, L = low, X = don't care

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

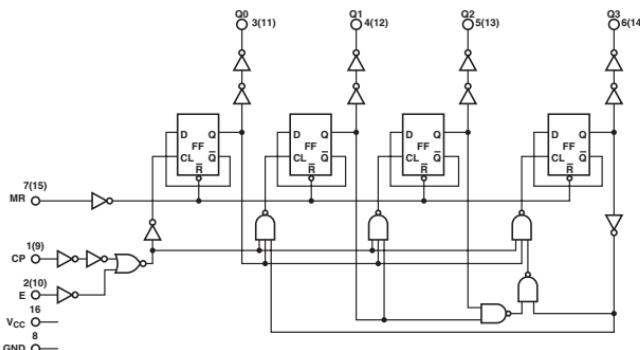
PARAMETER	MAX or MIN	SN74HC	CD74HC	CD74HCT	UNIT
I <sub>CC</sub>	MAX	0.08	0.16	0.16	mA
I <sub>OH</sub>	MAX	-4	-4	-4	mA
I <sub>OL</sub>	MAX	4	4	4	mA

TIMING REQUIREMENTS AND SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	SN74HC	CD74HC	CD74HCT
t <sub>rw</sub>	LE (LE)		MIN	20	22	45
t <sub>tsu</sub>	LE (LE)		MIN	25	30	30
t <sub>th</sub>	LE (LE)		MIN	5	0	5
t <sub>PLH</sub>	A0, 1, 2, 3 (A, B, C, D)	CD74HCT:Y (Ȳ)	MAX	58	83	83
t <sub>PLH</sub>	(LE)	CD74HCT:Y (Ȳ)	MAX	58	68	75
t <sub>PLH</sub>	Ē (Ḡ)	CD74HCT:Y (Ȳ)	MAX	58	68	75
t <sub>PLH</sub>	Ē (Ḡ)	CD74HCT:Y (Ȳ)	MAX	44	53	60
			UNIT:ns	44	53	60

## DUAL SYNCHRONOUS COUNTERS

Logic Diagram



FUNCTION TABLE

INPUTS			OUTPUT STATE
CP	E	MR	
↑	H	L	Increment Counter
L	↓	L	Increment Counter
↓	X	L	No Change
H	↑	L	No Change
↑	L	L	No Change
H	↓	L	No Change
L	X	H	Q <sub>0</sub> thru Q <sub>3</sub> = L

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	CD74 HC	UNIT
I <sub>CC</sub>	MAX	0.16	mA
I <sub>OH</sub>	MAX	-4	mA
I <sub>OL</sub>	MAX	4	mA

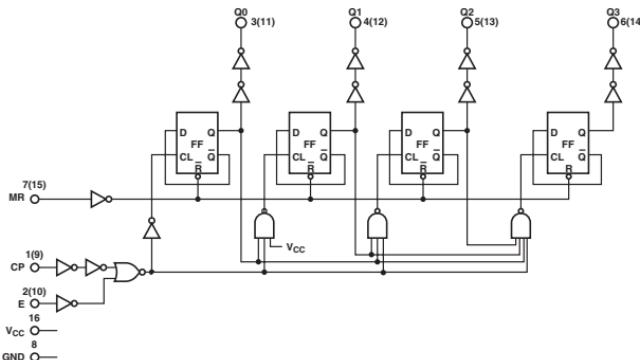
TIMING REQUIREMENTS AND SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	CD74 HC
f <sub>max</sub>				MIN 20
t <sub>w</sub>	CP			MIN 24
	MR			30
t <sub>su</sub>	Enable to CP			MIN 24
	CP to Enable			24
t <sub>PLH</sub>	CP		MAX 72	
t <sub>PHL</sub>	Enable		MAX 72	
t <sub>PLH</sub>	MR		MAX 45	
t <sub>PHL</sub>			MAX 45	

UNIT f<sub>max</sub> : MHz other : ns

## DUAL SYNCHRONOUS COUNTERS

Logic Diagram



## FUNCTION TABLE

INPUTS			OUTPUT STATE
CP	E	MR	
↑	H	L	Increment Counter
L	↓	L	Increment Counter
↓	X	L	No Change
X	↑	L	No Change
↑	L	L	No Change
H	↓	L	No Change
X	X	H	Q <sub>0</sub> thru Q <sub>3</sub> = L

## ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

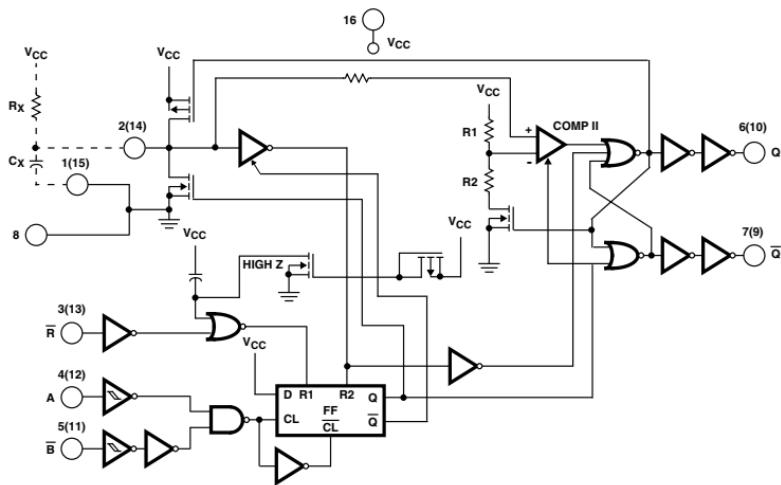
PARAMETER	MAX or MIN	CD74 HC	CD74 HCT	UNIT
I <sub>CC</sub>	MAX	0.16	0.16	mA
I <sub>OH</sub>	MAX	-4	-4	mA
I <sub>OL</sub>	MAX	4	4	mA

## TIMING REQUIREMENTS AND SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	CD74 HC	CD74 HCT
f <sub>max</sub>				MIN	20 17
t <sub>w</sub>	CP			MIN	24 30
	MR			MIN	30 30
t <sub>su</sub>	Enable to CP			MIN	24 24
	CP to Enable			MIN	24 -
t <sub>PLH</sub>	CP		MAX	72 80	
t <sub>PHL</sub>	CP		MAX	72 80	
t <sub>PLH</sub>	Enable		MAX	72 83	
t <sub>PHL</sub>	Enable		MAX	72 83	
t <sub>PLH</sub>	MR		MAX	45 53	
t <sub>PHL</sub>	MR		MAX	45 53	

UNIT f<sub>max</sub>: MHz other : ns

Logic Diagram



### FUNCTION TABLE

INPUTS			OUTPUTS	
$\bar{R}$	A	$\bar{B}$	E	$\bar{Q}$
L	X	X	L	H
X	H	X	L	H
X	X	L	L	H
H	L	$\downarrow$	$\square$	$\square$
H	$\uparrow$	H	$\square$	$\square$

H = High Level, L = Low Level,  $\uparrow$  = Transition from Low to High,  
 $\downarrow$  = Transition from High to Low,  $\square$  = One High Level Pulse,  
 $\square$  = One Low Level Pulse, X = Irrelevant.

### ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	CD74 HC	CD74 HCT	UNIT
$I_{CC}$	MAX	0.16	0.16	mA
$I_{OH}$	MAX	-4	-4	mA
$I_{OL}$	MAX	4	4	mA

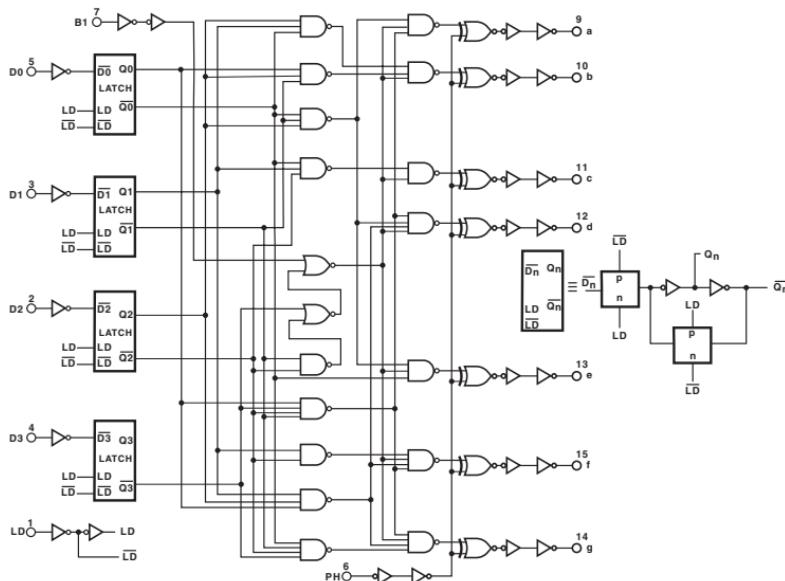
### TIMING REQUIREMENTS AND SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	CD74 HC	CD74 HCT	
$t_{WH}$	$A, \bar{B}$		MIN	24	24	
$t_{WL}$	$A, \bar{B}$			24	24	
$t_{WL}$	$\bar{R}$			24	30	
$t_{PLH}$	$\bar{A}, B$	Q	MAX	75	83	
$t_{PHL}$		$\bar{Q}$		75	83	
$t_{PLH}$	$\bar{R}$	Q	MAX	75	75	
$t_{PHL}$		$\bar{Q}$		75	60	

UNIT:ns

## BCD-TO-7 SEGMENT LATCH/DECODER/DRIVERS

Logic Diagram



FUNCTION TABLE

LD	B1	PH	D3	D2	D1	D0	a	b	c	d	e	f	g	Display
X	H	L	X	X	X	X	L	L	L	L	L	L	L	Blank
H	L	L	L	L	L	L	H	H	H	H	H	H	L	0
H	L	L	L	L	L	H	L	H	H	L	L	L	L	1
H	L	L	L	L	H	L	H	H	H	L	L	H	L	2
H	L	L	L	H	L	H	H	H	H	L	L	H	H	3
H	L	L	L	H	H	H	H	H	H	L	L	H	H	4
H	L	L	L	H	L	L	L	H	H	L	L	H	H	5
H	L	L	L	H	H	L	H	L	H	H	L	H	H	6
H	L	L	L	H	H	H	H	L	H	H	L	L	L	7
H	L	L	L	H	H	H	H	H	L	L	L	L	L	8
H	L	L	L	H	H	H	H	H	H	H	L	H	H	9
H	L	L	H	L	L	H	H	H	H	H	L	H	H	Blank
H	L	L	H	L	H	L	L	L	L	L	L	L	L	Blank
H	L	L	H	L	H	L	L	L	L	L	L	L	L	Blank
H	L	L	H	H	L	H	L	L	L	L	L	L	L	Blank
H	L	L	H	H	H	L	L	L	L	L	L	L	L	Blank
H	L	L	H	H	H	H	L	L	L	L	L	L	L	Blank
L	L	L	X	X	X	X	NOTE							NOTE
as above			N	as above			inverse above							as above

## NOTE:

Depends open the BCD code previously applied when LE = High

## ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	CD74 HC	CD74 HCT	UNIT
I <sub>CC</sub>	MAX	0.16	0.16	mA
I <sub>OH</sub>	MAX	-1	-4	mA
I <sub>OL</sub>	MAX	1	4	mA

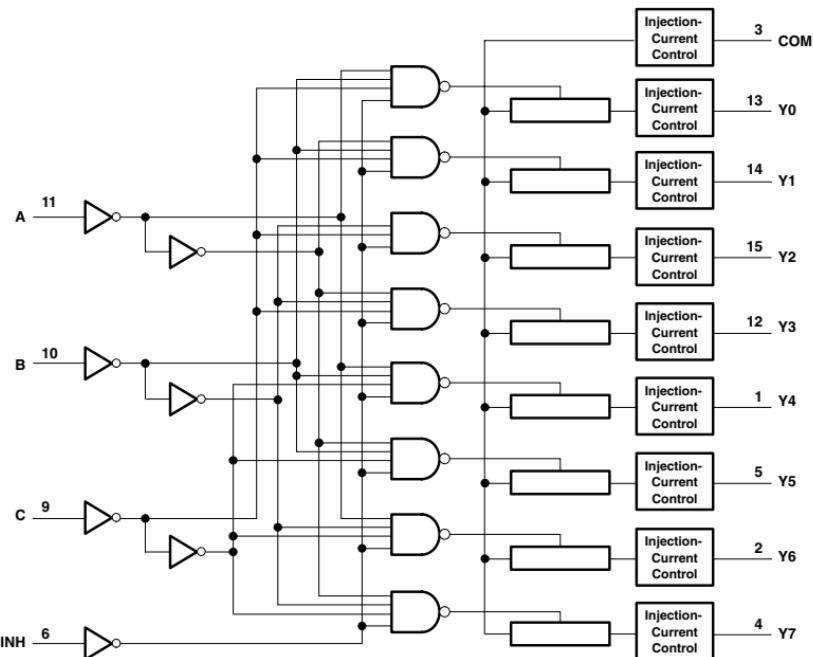
## TIMING REQUIREMENTS AND SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	CD74 HC	CD74 HCT
t <sub>W</sub>	Latch Disable		MIN	15	15
t <sub>su</sub>	Dn to LD		MIN	18	18
t <sub>h</sub>	Dn to LD		MIN	9	12
t <sub>PLH</sub>	Dn	a - g	MAX	102	120
t <sub>PHL</sub>			MAX	102	120
t <sub>PLH</sub>	LD	a - g	MAX	111	116
t <sub>PHL</sub>			MAX	111	116
t <sub>PLH</sub>	BI	a - g	MAX	80	99
t <sub>PHL</sub>			MAX	80	99
t <sub>PLH</sub>	PH	a - g	MAX	60	99
t <sub>PHL</sub>			MAX	60	99

UNIT:ns

**8-CHANNEL ANALOG MULTIPLEXER/DEMULTIPLEXER WITH INJECTION-CURRENT EFFECT CONTROL**

Logic Diagram


**ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS**

PARAMETER	MAX or MIN	SN74 HC	UNIT
I <sub>CC</sub>	MAX	0.01	mA
R <sub>ON</sub>	MAX	250	Ω

**SWITCHING CHARACTERISTICS**

PARAMETER	INPUT	OUTPUT	MAX or MIN	SN74 HC
T <sub>PLH</sub>	COM or Y <sub>n</sub>	Y <sub>n</sub> or COM	MAX	12.5
T <sub>PHL</sub>				12.5
T <sub>PLH</sub>	INH	COM or Y <sub>n</sub>	MAX	15
T <sub>PHL</sub>				15
T <sub>PLH</sub>	INH	COM or Y <sub>n</sub>	MAX	90
T <sub>PHL</sub>				90
T <sub>PLH</sub>	INH	COM or Y <sub>n</sub>	MAX	90
T <sub>PHL</sub>				90

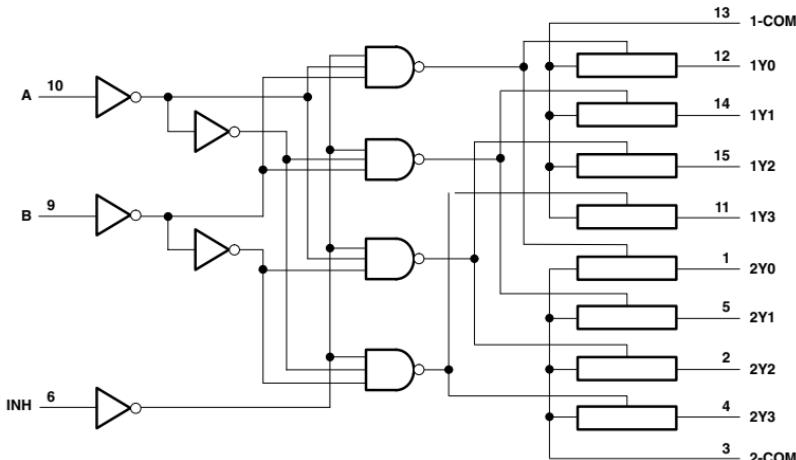
UNIT: ns

FUNCTION TABLE

INPUTS				ON CHANNEL
INH	C	B	A	
L	L	L	L	Y0
L	L	L	H	Y1
L	L	H	L	Y2
L	L	H	H	Y3
L	H	L	L	Y4
L	H	L	H	Y5
L	H	H	L	Y6
L	H	H	H	Y7
H	X	X	X	None

**DUAL 4-TO-1 CHANNEL ANALOG MULTIPLEXER/DEMULTIPLEXER WITH INJECTION-CURRENT EFFECT CONTROL**

- Low Crosstalk Between Switches
- Pin Compatible with SN74HC4052

**Logic Diagram**

**ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS**

PARAMETER	MAX or MIN	SN74 HC	UNIT
I <sub>CC</sub>	MAX	0.01	mA
R <sub>ON</sub>	MAX	270	Ω

**FUNCTION TABLE**

INPUTS			ON CHANNEL
INH	B	A	
L	L	L	1Y0, 2Y0
L	L	H	1Y1, 2Y1
L	H	L	1Y2, 2Y2
L	H	H	1Y3, 2Y3
H	X	X	None

**SWITCHING CHARACTERISTICS**

PARAMETER	INPUT	OUTPUT	MAX or MIN	SN74 HC
t <sub>PLH</sub>	COM or Y <sub>n</sub>	Y <sub>n</sub> or COM	MAX	12.5
t <sub>PHL</sub>				12.5
t <sub>PLH</sub>	Channel Select	COM or Y <sub>n</sub>	MAX	15
t <sub>PHL</sub>				15
t <sub>PLH</sub>	INH	COM or Y <sub>n</sub>	MAX	45
t <sub>PHL</sub>				45
t <sub>PLH</sub>	INH	COM or Y <sub>n</sub>	MAX	90
t <sub>PHL</sub>				90

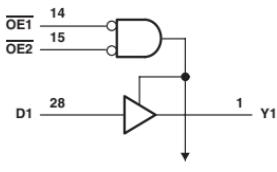
UNIT: ns

# 5400

## 11-BIT LINE/MEMORY DRIVERS WITH 3-STATE OUTPUTS

- Output Ports Have Equivalent 25- $\Omega$  Series Resistors,  
So No External Resistors Are Required  
(SN74ABT5400A)

Logic Diagram



FUNCTION TABLE

INPUTS		INPUT	Y
$\overline{OE1}$	$\overline{OE2}$	D	
L	L	L	L
L	L	H	H
H	X	X	Z
X	H	X	Z

ELECTRICAL CHARACTERISTICS AND  
RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	ABT	UNIT
$I_{CC}$	MAX	45	mA
$I_{OH}$	MAX	-12	mA
$I_{OL}$	MAX	12	mA

SWITCHING CHARACTERISTICS

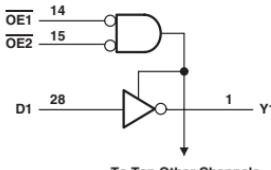
PARAMETER	INPUT	OUTPUT	MAX or MIN	ABT
$t_{PLH}$		Y	MAX	6.2
$t_{PHL}$	D			5.6
$t_{PZH}$		Y	MAX	8.7
$t_{PZL}$	$\overline{OE}$			7.5
$t_{PHZ}$		Y	MAX	5.2
$t_{PZL}$	$\overline{OE}$			6.9

# 5401

## 11-BIT LINE/MEMORY DRIVERS WITH 3-STATE OUTPUTS

- Output Ports Have Equivalent 25- $\Omega$  Series Resistors,  
So No External Resistors Are Required  
(SN74ABT5401)

Logic Diagram



FUNCTION TABLE

INPUTS		OUTPUT	Y
$\overline{OE1}$	$\overline{OE2}$	D	
L	L	L	H
L	L	H	L
H	X	X	Z
X	H	X	Z

ELECTRICAL CHARACTERISTICS AND  
RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	ABT	UNIT
$I_{CC}$	MAX	45	mA
$I_{OH}$	MAX	-12	mA
$I_{OL}$	MAX	12	mA

SWITCHING CHARACTERISTICS

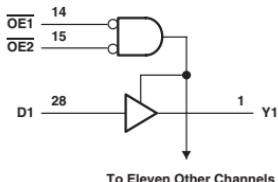
PARAMETER	INPUT	OUTPUT	MAX or MIN	ABT
$t_{PLH}$		Y	MAX	6.9
$t_{PHL}$	D			5.7
$t_{PZH}$		Y	MAX	8.5
$t_{PZL}$	$\overline{OE}$			6.8
$t_{PHZ}$		Y	MAX	5.2
$t_{PZL}$	$\overline{OE}$			6.9

UNIT: ns

## 5402

### 12-BIT LINE/MEMORY DRIVERS WITH 3-STATE OUTPUTS

- Output Ports Have Equivalent 25- $\Omega$  Series Resistors, So No External Resistors Are Required (SN74ABT5402A)

**Logic Diagram****FUNCTION TABLE**

INPUTS	OUTPUT		
OE1	OE2	D	Y
L	L	L	L
L	L	H	H
H	X	X	Z
X	H	X	Z

**ELECTRICAL CHARACTERISTICS AND  
RECOMMENDED OPERATING CONDITIONS**

PARAMETER	MAX or MIN	ABT	UNIT
$I_{CC}$	MAX	48	mA
$I_{OH}$	MAX	-12	mA
$I_{OL}$	MAX	12	mA

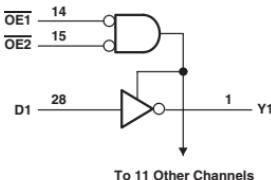
**SWITCHING CHARACTERISTICS**

PARAMETER	INPUT	OUTPUT	MAX or MIN	ABT
$t_{PLH}$	$D$	$Y$	MAX	6.2
$t_{PHL}$				5.6
$t_{PZH}$	$\overline{OE}$	$Y$	MAX	8.7
$t_{PZL}$				7.5
$t_{PHZ}$	$\overline{OE}$	$Y$	MAX	5.2
$t_{PLZ}$				6.9

## 5403

### 12-BIT LINE/MEMORY DRIVERS WITH 3-STATE OUTPUTS

- Output Ports Have Equivalent 25- $\Omega$  Series Resistors, So No External Resistors Are Required (SN74ABT5403)

**Logic Diagram****FUNCTION TABLE**

INPUTS	OUTPUT		
OE1	OE2	D	Y
L	L	L	H
L	L	H	L
H	X	X	Z
X	H	X	Z

**ELECTRICAL CHARACTERISTICS AND  
RECOMMENDED OPERATING CONDITIONS**

PARAMETER	MAX or MIN	ABT	UNIT
$I_{CC}$	MAX	45	mA
$I_{OH}$	MAX	-12	mA
$I_{OL}$	MAX	12	mA

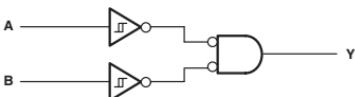
**SWITCHING CHARACTERISTICS**

PARAMETER	INPUT	OUTPUT	MAX or MIN	ABT
$t_{PLH}$	$D$	$Y$	MAX	6.9
$t_{PHL}$				5.7
$t_{PZH}$	$\overline{OE}$	$Y$	MAX	8.5
$t_{PZL}$				6.8
$t_{PHZ}$	$\overline{OE}$	$Y$	MAX	5.2
$t_{PLZ}$				6.9

## 7001

### QUADRUPLE POSITIVE-AND GATES WITH SCHMITT-TRIGGER INPUTS

- Same Pinouts as SN74HC08
- $V_{CC}$ : 2V to 6V
- Schmitt-Triggered Inputs
- $Y = A \bullet B$

**Logic Diagram**

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	SN74 HC	UNIT
$I_{CC}$	MAX	0.02	mA
$I_{OH}$	MAX	-4	mA
$I_{OL}$	MAX	4	mA

SWITCHING CHARACTERISTICS

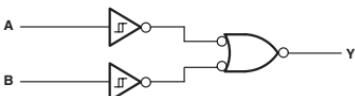
PARAMETER	INPUT	OUTPUT	MAX or MIN	SN74 HC
$t_{PLH}$	A or B	Y	MAX	33
$t_{PHL}$				33

UNIT: ns

## 7002

### QUADRUPLE POSITIVE-NOR GATES WITH SCHMITT-TRIGGER INPUTS

- Same Pinouts as SN74HC36
- $V_{CC}$ : 2V to 6V
- Schmitt-Triggered Inputs
- $Y = \overline{A} + \overline{B}$

**Logic Diagram**

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	SN74 HC	UNIT
$I_{CC}$	MAX	0.02	mA
$I_{OH}$	MAX	-4	mA
$I_{OL}$	MAX	4	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	SN74 HC
$t_{PLH}$	A or B	Y	MAX	33
$t_{PHL}$				33

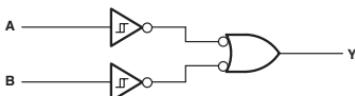
UNIT: ns

# 7032

## QUADRUPLE POSITIVE-OR GATES WITH SCHMITT-TRIGGER INPUTS

- Same Pinouts as SN74HC32
- $V_{CC}$ : 2V to 6V
- Schmitt-Triggered Inputs
- $Y = A + B$

Logic Diagram



### ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	SN74 HC	UNIT
$I_{CC}$	MAX	0.02	mA
$I_{OH}$	MAX	-4	mA
$I_{OL}$	MAX	4	mA

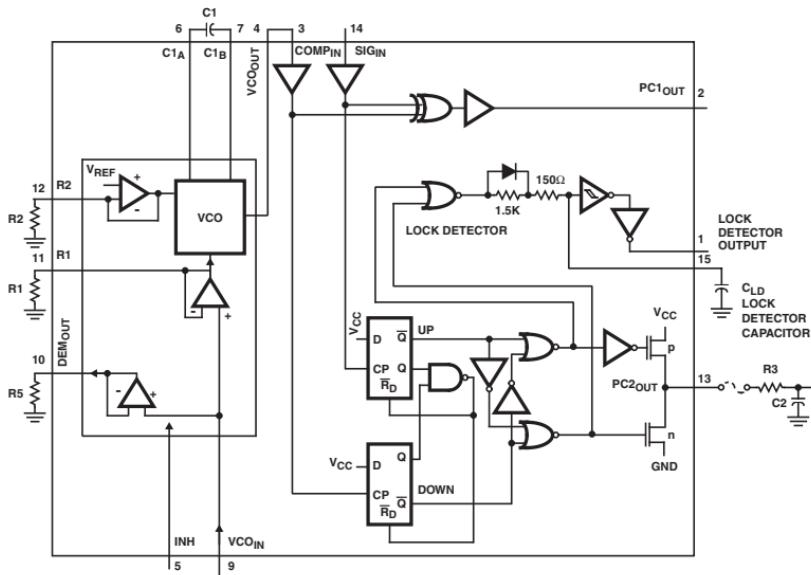
### SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	SN74 HC
$t_{PLH}$	A or B	Y	MAX	33
$t_{PHL}$				33

UNIT: ns

## PHASE-LOCKED LOOP WITH VCO AND LOCK DETECTOR

Logic Diagram



## ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	CD74 HC	CD74 HCT	UNIT
$I_{CC}$	MAX	0.16	0.16	mA
$I_{OH}$	MAX	-4	-4	mA
$I_{OL}$	MAX	4	4	mA

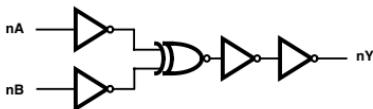
## SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	CD74 HC	CD74 HCT
$t_{PLH}$	SIGIN, COMPIN	PC1OUT	MAX	60	68
$t_{PHL}$	SIGIN, COMPIN	PC1OUT		60	68
$t_{PZH}$	SIGIN, COMPIN	PC2OUT	MAX	84	90
$t_{PZL}$	SIGIN, COMPIN	PC2OUT		84	90
$t_{PHZ}$	SIGIN, COMPIN	PC2OUT	MAX	98	105
$t_{PZL}$	SIGIN, COMPIN	PC2OUT		98	105

UNIT:ns

## QUAD 2-INPUT EXCLUSIVE-NOR GATES

$$\bullet \quad Y = \overline{A \oplus B}$$



FUNCTION TABLE

INPUTS	OUTPUT	
A	B	Y
L	L	H
L	H	L
H	L	L
H	H	H

NOTES:

H = High Voltage Level

L = Low Voltage Level

## ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	SN74 HC	CD74 HC	UNIT
I <sub>CC</sub>	MAX	0.02	0.04	mA
I <sub>OH</sub>	MAX	-4	-4	V
I <sub>OL</sub>	MAX	4	4	V

## SWITCHING CHARACTERISTICS

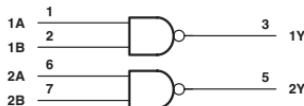
PARAMETER	INPUT	OUTPUT	MAX or MIN	SN74 HC	CD74 HC
t <sub>PLH</sub>	A or B	Y	MAX	25	35
t <sub>PHL</sub>		Y	MAX	25	35

UNIT: ns

## 8003

## Logic Diagram

## DUAL 2-INPUT POSITIVE-NAND GATES



## ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

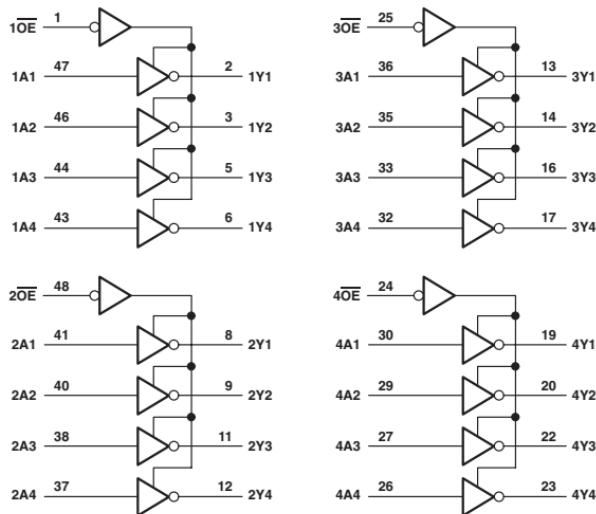
PARAMETER	MAX or MIN	ALS	AS	UNIT
I <sub>CC</sub>	MAX	1.5	8.7	mA
I <sub>OH</sub>	MAX	-0.4	-2	mA
I <sub>OL</sub>	MAX	8	20	mA

## SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	ALS	AS
t <sub>PLH</sub>	A or B	Y	MAX	11	4.5
t <sub>PHL</sub>				8	4

UNIT: ns

Logic Diagram



**FUNCTION TABLE**  
(each 4-bit buffer)

INPUTS	OUTPUT	
OE	A	Y
L	H	L
L	L	H
H	X	Z

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	ABT	LVT 3V	LVTH 3V	ALVTH 3V	AC	ACT	AHC	AHCT	LVCH 3V	LVCZ 3V	ALVCH 3V	UNIT
I <sub>CC</sub>	MAX	34	5	5	5	0.08	0.08	0.04	0.04	0.02	0.1	0.04	mA
I <sub>OH</sub>	MAX	-32	-32	-32	-32	-24	-24	-8	-8	-24	-24	-24	mA
I <sub>OL</sub>	MAX	64	64	64	64	24	24	8	8	24	24	24	mA

PARAMETER	MAX or MIN	AUC 1.8V	AUC 2.3V	UNIT
I <sub>CC</sub>	MAX	0.02	0.02	mA
I <sub>OH</sub>	MAX	-8	-9	mA
I <sub>OL</sub>	MAX	8	9	mA

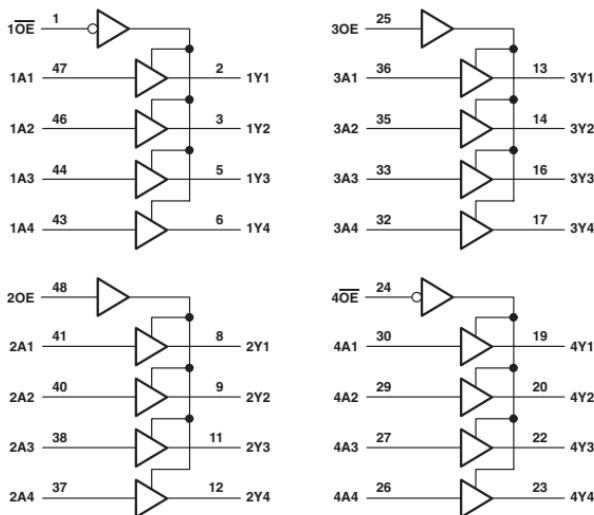
SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	ABT	LVT 3V	LVTH 3V	ALVTH 3V	AC	ACT	AHC	AHCT
t <sub>PLH</sub>				4.7	3.5	3.5	3.3	5.8	8.5	8.5	10.5
t <sub>PHL</sub>	A	Y	MAX	4.8	3.5	3.5	3.2	7.1	10.2	8.5	10.5
t <sub>PZH</sub>				5.3	4	4	3.7	6.6	9.4	10.5	13
t <sub>PZL</sub>	OE	Y	MAX	7.1	4.4	4.4	3.1	8.1	11.4	10.5	13
t <sub>PHZ</sub>	OE	Y	MAX	6.1	4.5	4.5	5	8.1	12	10.5	13
t <sub>PZL</sub>	OE	Y	MAX	5.6	4.2	4.2	4.1	7.3	10.7	10.5	13

PARAMETER	INPUT	OUTPUT	MAX or MIN	LVCH 3V	LVCZ 3V	ALVCH 3V	AUC 1.8V	AUC 2.3V
t <sub>PLH</sub>				4.2	4.2	3.9	2.0	1.6
t <sub>PHL</sub>	A	Y	MAX	4.2	4.2	3.9	2.0	1.6
t <sub>PZH</sub>				4.7	4.7	5	2.5	2
t <sub>PZL</sub>	OE	Y	MAX	4.7	4.7	5	2.5	2
t <sub>PHZ</sub>	OE	Y	MAX	5.9	5.9	4.4	4.5	2.3
t <sub>PZL</sub>	OE	Y	MAX	5.9	5.9	4.4	4.5	2.3

UNIT: ns

Logic Diagram



**FUNCTION TABLE**

INPUTS		OUTPUTS	
1OE, 4OE		1A, 4A	
L	H	L	
L	L	H	
H	X	Z	

INPUTS		OUTPUTS	
2OE, 3OE		2A, 3A	
H	H	H	
H	L	L	
L	X	Z	

**ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS**

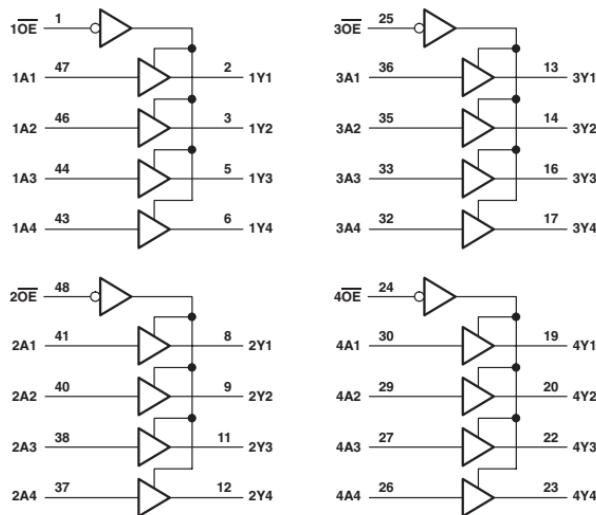
PARAMETER	MAX or MIN	ABT	LVTH 3V	ACT	UNIT
I <sub>CC</sub>	MAX	34	5	0.08	mA
I <sub>OH</sub>	MAX	-32	-32	-24	mA
I <sub>OL</sub>	MAX	64	64	24	mA

**SWITCHING CHARACTERISTICS**

PARAMETER	INPUT	OUTPUT	MAX or MIN	ABT	LVTH 3V	ACT
t <sub>PLH</sub>	A	Y	MAX	3.7	3.5	9.5
t <sub>PHL</sub>				4.5	3.5	9.1
t <sub>PZH</sub>	OE or OE	Y	MAX	5	4.5	9.4
t <sub>PZL</sub>				6.9	4.5	10.5
t <sub>PHZ</sub>	OE or OE	Y	MAX	6.2	5.3	11.6
t <sub>PZL</sub>				5.6	4.9	10.7

UNIT: ns

Logic Diagram



**FUNCTION TABLE**  
(each buffer)

INPUTS	OUTPUT	
OE	A	Y
L	H	H
L	L	L
H	X	Z

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	ABT	ABTH	LVT 3V	LVTH 3V	ALB 3V	ALVTH 3V	AC	ACT	AHC	AHCT	LVC 3V	UNIT
I <sub>CC</sub>	MAX	32	32	5	5	5.6	5	0.08	0.08	0.04	0.04	0.02	mA
I <sub>OH</sub>	MAX	-32	-32	-32	-32	-25	-32	-24	-24	-8	-8	-24	mA
I <sub>OL</sub>	MAX	64	64	64	64	25	64	24	24	8	8	24	mA

PARAMETER	MAX or MIN	LVCH 3V	LVCZ 3V	ALVC 3V	ALVCH 3V	AVC 3V	AUC 1.8V	AUC 2.3V	AUCH 1.8V	AUCH 2.3V	UNIT
I <sub>CC</sub>	MAX	0.02	0.1	0.04	0.04	0.04	0.02	0.02	0.02	0.02	mA
I <sub>OH</sub>	MAX	-24	-24	-24	-24	-12	-8	-9	-8	-9	mA
I <sub>OL</sub>	MAX	24	24	24	24	12	8	9	8	9	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	ABT	ABTH	LVT 3V	LVTH 3V	ALB 3V	ALVTH 3V	AC	ACT
t <sub>PLH</sub>			MAX	3.5	3.5	3.2	3.2	2	2.4	7.1	9.4
t <sub>PHL</sub>	A	Y	MAX	4.1	4.1	3.2	3.2	2	2.5	7.9	9.5
t <sub>PZH</sub>			MAX	4.8	4.8	4	4	4.7	3.8	7.5	8.9
t <sub>PZL</sub>	OE	Y	MAX	4.8	4.8	4	4	4.7	2.9	9	10.3
t <sub>PHZ</sub>			MAX	4.8	4.8	4.5	4.5	4.2	4.2	8.4	11.3
t <sub>PZL</sub>	OE	Y	MAX	4.1	4.1	4.2	4.2	3.6	7.6	10.3	

PARAMETER	INPUT	OUTPUT	MAX or MIN	AHC	AHCT	LVC 3V	LVCH 3V	LVCZ 3V	ALVC 3V	ALVCH 3V	AVC 3V
t <sub>PLH</sub>			MAX	8.5	10.5	4.1	4.1	3	3	3	1.7
t <sub>PHL</sub>	A	Y	MAX	8.5	10.5	4.1	4.1	3	3	3	1.7
t <sub>PZH</sub>			MAX	10.5	13	4.6	4.6	4.6	4.4	4.4	3.5
t <sub>PZL</sub>	OE	Y	MAX	10.5	13	4.6	4.6	4.6	4.4	4.4	3.5
t <sub>PHZ</sub>			MAX	10.5	13	5.8	5.8	5.8	4.1	4.1	3.5
t <sub>PZL</sub>	OE	Y	MAX	10.5	13	5.8	5.8	5.8	4.1	4.1	3.5

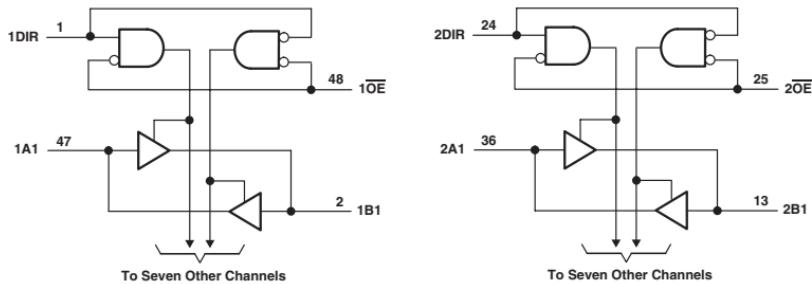
PARAMETER	INPUT	OUTPUT	MAX or MIN	AUC 1.8V	AUC 2.3V	AUCH 1.8V	AUCH 2.3V
t <sub>PLH</sub>			MAX	1.8	1.8	1.8	1.8
t <sub>PHL</sub>	A	Y	MAX	1.8	1.8	1.8	1.8
t <sub>PZH</sub>			MAX	2.5	1.9	2.5	1.9
t <sub>PZL</sub>	OE	Y	MAX	2.5	1.9	2.5	1.9
t <sub>PHZ</sub>			MAX	4.0	2	4.0	2
t <sub>PZL</sub>	OE	Y	MAX	4.0	2	4.0	2

UNIT: ns

**16245**

**16-BIT BUS TRANSCEIVER WITH 3-STATE OUTPUTS**

**Logic Diagram**



**FUNCTION TABLE**  
(each 8-bit section)

INPUTS		OPERATION
OE	DIR	
L	L	B data to A bus
L	H	A data to B bus
H	X	Isolation

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	ABT	ABTH	LVT 3V	LVTH 3V	ALB 3V	ALVTH 3V	ALVT HR 3V	AC	ACT	AHCT	UNIT
I <sub>CC</sub>	MAX	32	32	5	5	5.6	5	5	0.08	0.08	0.04	mA
I <sub>OH</sub>	MAX	-32	-32	-32	-32	-25	-32	-12	-24	-24	-8	mA
I <sub>OL</sub>	MAX	64	64	64	64	25	64	12	24	24	8	mA

PARAMETER	MAX or MIN	LVC 3V	LVCH 3V	LVCHR 3V	LVCR 3V	LVCZ 3V	ALVCH 3V	ALVC HR 3V	AVC 3V	AUC 1.8V	AUC 2.3V	UNIT
I <sub>CC</sub>	MAX	0.02	0.02	0.02	0.02	0.06	0.04	0.04	0.04	0.02	0.02	mA
I <sub>OH</sub>	MAX	-24	-24	-12	-12	-24	-24	-12	-12	-8	-9	mA
I <sub>OL</sub>	MAX	24	24	12	12	24	24	12	12	8	9	mA

SWITCHING CHARACTERISTICS

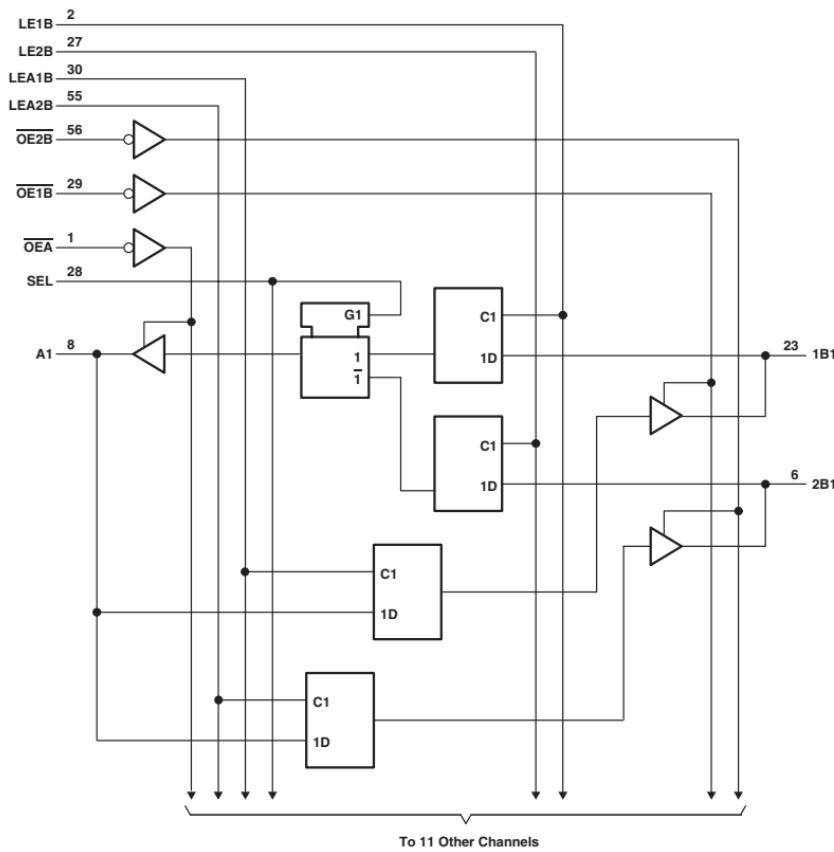
PARAMETER	INPUT	OUTPUT	MAX or MIN	ABT	ABTH	LVT 3V	LVTH 3V	ALB 3V	ALVTH 3V	ALVT HR 3V	AC
I <sub>PLH</sub>	A or B	B or A	MAX	3.9	3.9	3.3	3.3	2	3.1	3.7	7.9
I <sub>PHL</sub>				4.2	4.2	3.3	3.3	2	2.9	3.9	8.9
I <sub>PZH</sub>	OE	B or A	MAX	6.3	6.3	4.5	4.5	6	4.2	5.2	8.6
I <sub>PZL</sub>				6.4	6.4	4.6	4.6	6	3.5	4	10.7
I <sub>PHZ</sub>	OE	B or A	MAX	6.3	6.3	5.1	5.1	4.2	5.3	5.1	9.8
I <sub>PZL</sub>				5.2	5.2	5.1	5.1	4.2	5	4.8	8.7

PARAMETER	INPUT	OUTPUT	MAX or MIN	ACT	AHCT	LVC 3V	LVCH 3V	LVCHR 3V	LVCR 3V	LVCZ 3V	ALVCH 3V
I <sub>PLH</sub>	A or B	B or A	MAX	10.5	10.5	4	4	4.8	4.8	4	3
I <sub>PHL</sub>				10.2	10.5	4	4	4.8	4.8	4	3
I <sub>PZH</sub>	OE	B or A	MAX	10	15	5.5	5.5	6.3	6.3	5.6	4.4
I <sub>PZL</sub>				11.6	15	5.5	5.5	6.3	6.3	5.6	4.4
I <sub>PHZ</sub>	OE	B or A	MAX	12.6	15	6.6	6.6	7.4	7.4	6.6	4.1
I <sub>PZL</sub>				11.8	15	6.6	6.6	7.4	7.4	6.6	4.1

PARAMETER	INPUT	OUTPUT	MAX or MIN	ALVC HR 3V	AVC 3V	AUC 1.8V	AUC 2.3V
I <sub>PLH</sub>	A or B	B or A	MAX	4.2	1.7	2	1.9
I <sub>PHL</sub>				4.2	1.7	2	1.9
I <sub>PZH</sub>	OE	B or A	MAX	5.6	3.7	3.1	2.6
I <sub>PZL</sub>				5.6	3.7	3.1	2.6
I <sub>PHZ</sub>	OE	B or A	MAX	5.5	3.9	4.8	2.9
I <sub>PZL</sub>				5.5	3.9	4.8	2.9

UNIT: ns

Logic Diagram



**FUNCTION TABLE**
**B TO A ( $\bar{OE}_B = H$ )**

INPUTS						OUTPUT
1B	2B	SEL	LE1B	LE2B	$\bar{OE}_A$	A
H	X	H	H	X	L	H
L	X	H	H	X	L	L
X	X	H	L	X	L	$A_0$
X	H	L	X	H	L	H
X	L	L	X	H	L	L
X	X	L	X	L	L	$A_0$
X	X	X	X	X	H	Z

**A TO B ( $\bar{OE}_A = H$ )**

INPUTS					OUTPUTS	
1B	LEA1B	LEA2B	OE1B	OE2B	1B	2B
H	H	H	L	L	H	H
L	H	H	L	L	L	L
H	H	L	L	L	H	$2B_0$
L	H	L	L	L	$2B_0$	H
H	L	H	L	L	$1B_0$	H
L	L	H	L	L	$1B_0$	L
X	L	L	L	L	$1B_0$	$2B_0$
X	X	X	H	H	Z	Z
X	X	X	L	H	Active	Z
X	X	X	H	L	Z	Active
X	X	X	L	L	Active	Active

**ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS**

PARAMETER	MAX or MIN	ABTH	ALVCH 3V	UNIT
$I_{CC}$	MAX	63	0.04	mA
$I_{OH}$	MAX	-32	-24	mA
$I_{OL}$	MAX	64	24	mA

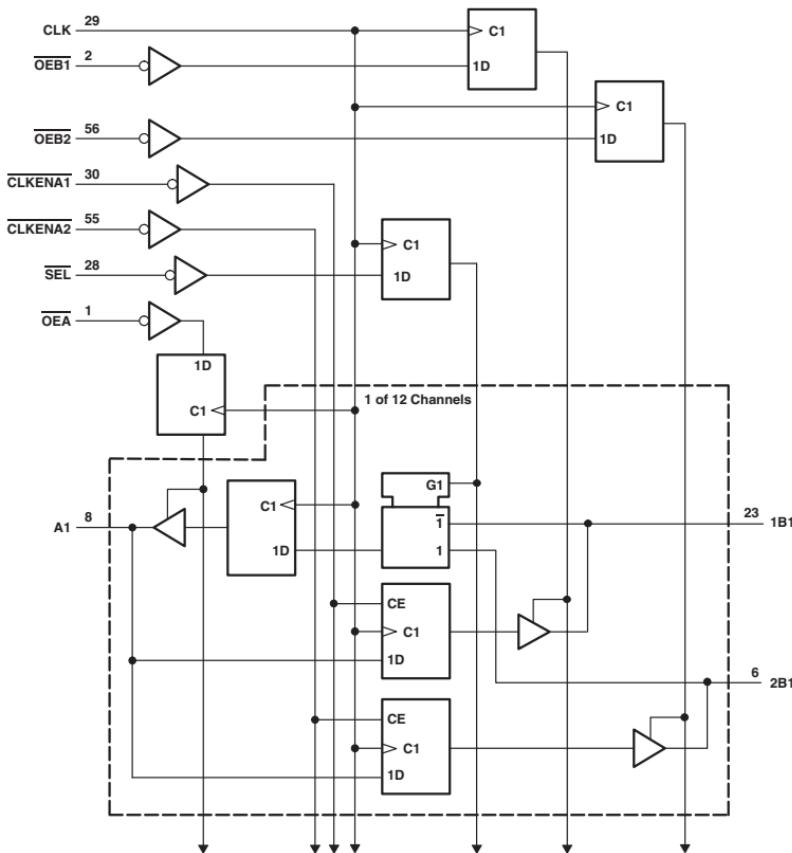
**TIMING REQUIREMENTS AND SWITCHING CHARACTERISTICS**

PARAMETER	INPUT	OUTPUT	MAX or MIN	ABTH	ALVCH 3V
$t_{\text{Pulse}}$ Pulse duration, LE1B, LE2B, LEA1B, or LEA2B high			MIN	3.3	3.3
$t_{\text{Setup}}$ Setup time, data before LE1B, LE2B, LEA1B, or LEA2B ↓			MIN	1.5	1.1
$t_h$ Hold time, data after LE1B, LE2B, LEA1B, or LEA2B ↓			MIN	1	1.5
$t_{PLH}$	A or B	B or A	MAX	5.6	4.3
$t_{PHL}$				5.9	4.3
$t_{PLH}$	LE	A or B	MAX	5.8	4.4
$t_{PHL}$				5.3	4.4
$t_{PLH}$	SEL (B1)	A	MAX	5.3	5.6
	SEL (B2)			6	5.6
$t_{PHL}$	SEL (B1)	A	MAX	4.4	5.6
	SEL (B2)			5.9	5.6
$t_{PZH}$	$\bar{OE}$	A or B	MAX	5.7	5.4
$t_{PZL}$				5.8	5.4
$t_{PHZ}$	$\bar{OE}$	A or B	MAX	6.4	4.6
$t_{PZL}$				4.8	4.6

UNIT: ns

## 12-BIT TO 24-BIT REGISTERED BUS TRANSCEIVER WITH 3-STATE OUTPUTS

Logic Diagram



**FUNCTION TABLE**
**OUTPUT ENABLE**

INPUTS			OUTPUTS	
CLK	OE <sub>A</sub>	OE <sub>B</sub>	A	1B,2B
↑	H	H	Z	Z
↑	H	L	Z	Active
↑	L	H	Active	Z
↑	L	L	Active	Active

**A-TO-B STORAGE (OE<sub>B</sub> = L)**

INPUTS			OUTPUTS	
CLKEN <sub>A1</sub>	CLKEN <sub>A2</sub>	CLK	A	1B 2B
H	H	X	X	1B↑† 2B↑†
L	X	↑	L	L X
L	X	↑	H	H X
X	L	↑	L	X L
X	L	↑	H	X H

† Output level before the indicated steady-state input conditions were established

**B-TO-A STORAGE (OE<sub>A</sub> = L)**

INPUTS			OUTPUT	
CLK	SEL	1B 2B	A	
X	H	X X	X	A <sub>0t</sub>
X	L	X X	X	A <sub>0t</sub>
↑	H	H X	X	L
↑	H	L X	X	H
↑	L	X L	L	L
↑	L	X H	H	H

† Output level before the indicated steady-state input conditions were established

**ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS**

PARAMETER	MAX or MIN	ALVCH 3V	ALVCHR 3V	AVC 3V	UNIT
I <sub>CC</sub>	MAX	0.04	0.04	0.04	mA
I <sub>OH</sub>	MAX	-24	-12	-12	mA
I <sub>OL</sub>	MAX	24	12	12	mA

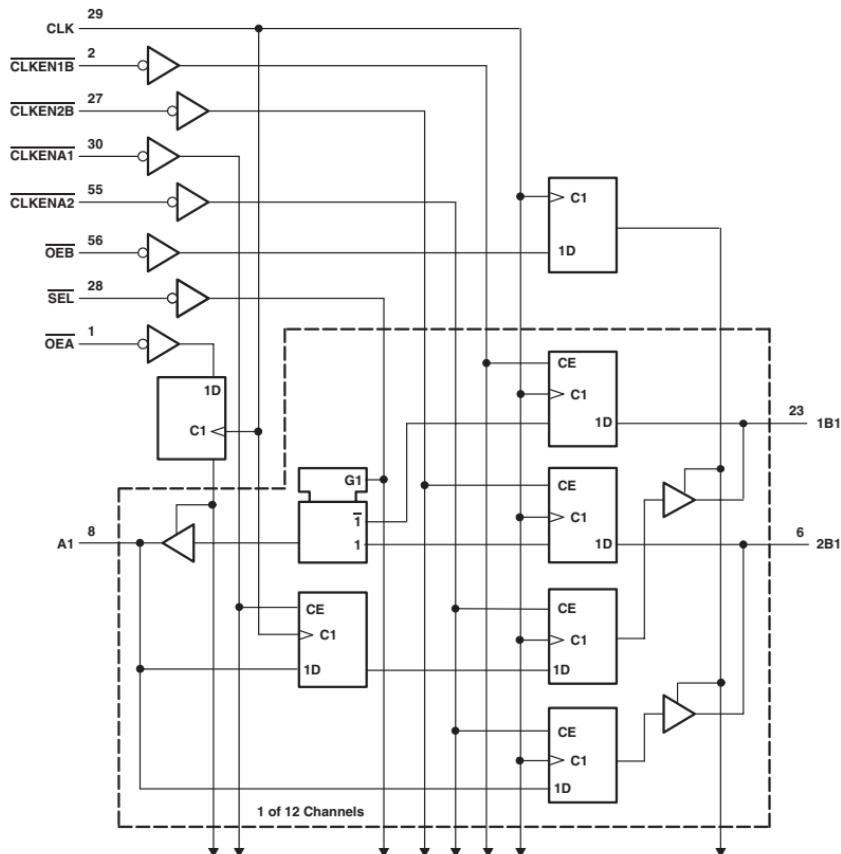
**TIMING REQUIREMENTS AND SWITCHING CHARACTERISTICS**

PARAMETER	INPUT	OUTPUT	MAX or MIN	ALVCH 3V	ALVCHR 3V	AVC 3V
f <sub>max</sub>			MIN	135	135	175
t <sub>w</sub> Pulse duration, CLK high or low			MIN	3.3	3.3	3.5
t <sub>su</sub> Setup time	A data before CLK↑		MIN	1.7	1	1.9
	B data before CLK↑		MIN	1.8	1.1	1.9
	SEL before CLK↑		MIN	1.3	1.3	1.3
	CLKEN <sub>A1</sub> or CLKEN <sub>A2</sub> before CLK↑		MIN	0.9	0.8	1.1
	OE before CLK↑		MIN	1.3	1.2	1.1
t <sub>h</sub> Hold time	A data after CLK↑		MIN	0.6	1.2	1
	B data after CLK↑		MIN	0.6	1	0.7
	SEL after CLK↑		MIN	0.7	1.7	0.4
	CLKEN <sub>A1</sub> or CLKEN <sub>A2</sub> after CLK↑		MIN	1.1	1.6	1
	OE after CLK↑		MIN	0.8	1.2	0.3
t <sub>pd</sub>	CLK	B	MAX	6.2	5.8	3
		A		5	5.2	2.7
t <sub>en</sub>	CLK	B	MAX	6.1	5.8	3.8
		A		5.9	5.3	3.4
t <sub>dis</sub>	CLK	B	MAX	6.1	6	3.7
		A		5.6	6	3.4

UNIT f<sub>max</sub> : MHz other : ns

## 12-BIT TO 24-BIT REGISTERED BUS EXCHANGER WITH 3-STATE OUTPUTS

## Logic Diagram



## FUNCTION TABLE

### OUTPUT ENABLE

INPUTS			OUTPUTS	
CLK	OE <sub>A</sub>	OE <sub>B</sub>	A	1B,2B
↑	H	H	Z	Z
↑	H	L	Z	Active
↑	L	H	Active	Z
↑	L	L	Active	Active

### A-TO-B STORAGE (OE<sub>B</sub> = L)

INPUTS			OUTPUTS	
CLKENA1	CLKENA2	CLK	A	1B 2B
L	H	↑	L	L↑ 2B0‡
L	H	↑	H	H↑ 2B0‡
L	L	↑	L	L↑ L
L	L	↑	H	H↑ H
H	L	↑	L	1B0‡ L
H	L	↑	H	1B0‡ H
H	H	X	X	1B0‡ 2B0†

† Two CLK edges are needed to propagate data.

‡ Output level before the indicated steady-state input conditions were established

### B-TO-A STORAGE (OE<sub>A</sub> = L)

INPUTS					OUTPUT
CLKEN1B	CLKEN2B	CLK	SEL	1B	2B
H	X	X	H	X	X A0‡
X	H	X	L	X	X A0‡
L	X	↑	H	H	X L
L	X	↑	H	L	X H
X	L	↑	L	X	L L
X	L	↑	L	X	H H

‡ Output level before the indicated steady-state input conditions were established

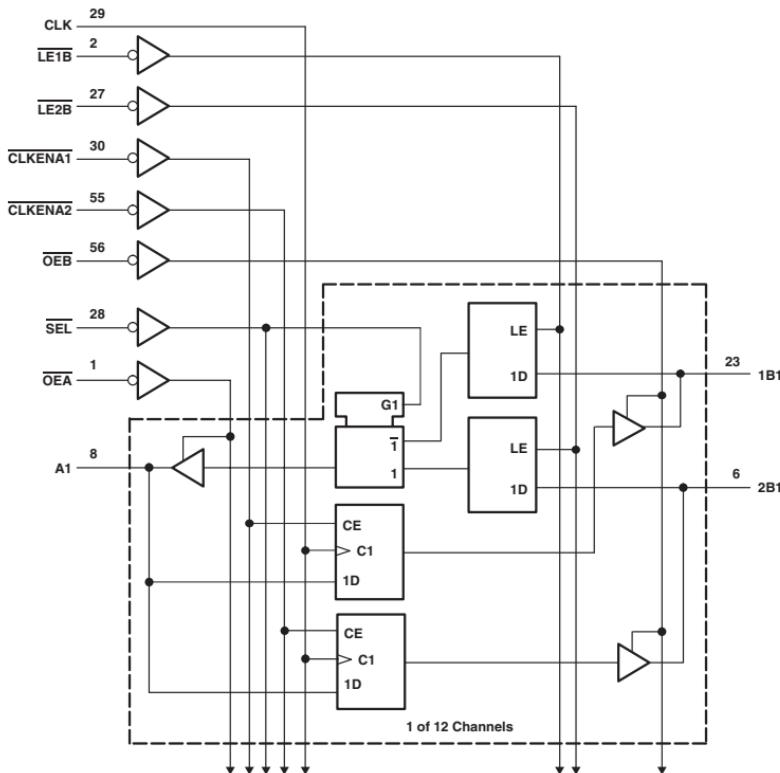
## ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	ALVCH 3V	UNIT
I <sub>CC</sub>	MAX	0.04	mA
I <sub>OH</sub>	MAX	-24	mA
I <sub>OL</sub>	MAX	24	mA

## TIMING REQUIREMENTS AND SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	ALVCH 3V
f <sub>max</sub>			MIN	150
t <sub>w</sub>	Pulse duration, CLK high or low		MIN	3.3
t <sub>su</sub>	A data before CLK ↑		MIN	3.1
	B data before CLK ↑		MIN	0.9
	CLKENA1 or CLKENA2 before CLK ↑		MIN	2.7
	CLKEN1B or CLKEN2B before CLK ↑		MIN	2.6
t <sub>sh</sub>	OE before CLK ↑		MIN	3.2
	A data after CLK ↑		MIN	0.2
	B data after CLK ↑		MIN	1.7
	CLKENA1 or CLKENA2 after CLK ↑		MIN	0.3
t <sub>th</sub>	CLKEN1B or CLKEN2B after CLK ↑		MIN	0.6
	OE after CLK ↑		MIN	0.1
	CLK	A or B	MAX	5.1
	SEL	A	MAX	5.5
t <sub>an</sub>	CLK	A or B	MAX	6
t <sub>dis</sub>	CLK	A or B	MAX	5.8
UNIT fmax : MHz other : ns				

Logic Diagram



## FUNCTION TABLE

### OUTPUT ENABLE

INPUTS		OUTPUTS	
OEA	OEB	A	1B, 2B
H	X	Z	Z
L	L	Z	Active
L	H	Active	Z
L	L	Active	Active

### A-TO-B STORAGE (OEB = L)

INPUTS			OUTPUTS	
CLKENA1	CLKENA2	CLK	A	1B 2B
H	H	X	X	1B <sub>0†</sub> 2B <sub>0†</sub>
L	X	↑	L	L X
L	X	↑	H	H X
X	L	↑	L	X L
X	L	↑	H	A <sub>0</sub> H

### B-TO-A STORAGE (OEA = L)

INPUTS			OUTPUTA
LE	SEL	1B 2B	
H	X	X X	A <sub>0†</sub>
H	X	X X	A <sub>0†</sub>
L	H	L X	L
L	H	H X	H
L	L	X L	L
L	L	X H	H

† Output level before the indicated steady-state input conditions were established

### ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

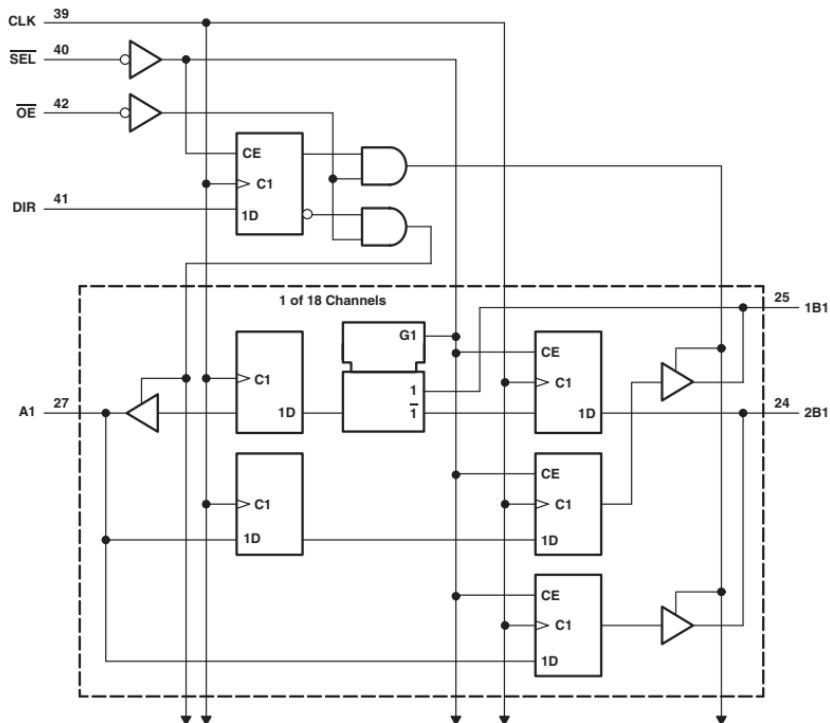
PARAMETER	MAX or MIN	ALVCH 3V	UNIT
I <sub>CC</sub>	MAX	0.04	mA
I <sub>OH</sub>	MAX	-24	mA
I <sub>OL</sub>	MAX	24	mA

### TIMING REQUIREMENTS AND SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	ALVCH 3V
f <sub>max</sub>			MIN	130
t <sub>tr</sub>	Pulse duration, CLK high or low		MIN	3.3
t <sub>su</sub>	A before CLK ↑		MIN	1.7
	B before LE		MIN	1.3
	CLKEN before CLK ↑		MIN	1
t <sub>th</sub>	A after CLK ↑		MIN	0.7
	B after LE		MIN	1.1
	CLKEN after CLK ↑		MIN	0.9
t <sub>pd</sub>	CLK	B	MAX	4.3
	B			4
	LE		MAX	4.8
	SEL			5.2
t <sub>on</sub>	OEB or OEA	B or A	MAX	5.1
t <sub>dis</sub>	OEB or OEA	B or A	MAX	4.2

UNIT f<sub>max</sub> : MHz other : ns

Logic Diagram



### FUNCTION TABLE

A-TO-B STORAGE ( $\overline{OE} = L$ ,  $DIR = H$ )

INPUTS			OUTPUTS	
SEL	CLK	A	1B	2B
H	X	X	1B <sub>0†</sub>	2B <sub>0†</sub>
↑	↑	L	L <sub>‡</sub>	X
L	↑	H	H <sub>†</sub>	X

† Output level before the indicated steady-state input conditions were established.

‡ Two CLK edges are needed to propagate the data.

B-TO-A STORAGE ( $\overline{OE} = L$ ,  $DIR = L$ )

INPUTS			OUTPUT
CLK	SEL	1B	2B
↑	H	X	L
↑	H	X	H <sub>§</sub>
↑	L	L	X
↑	L	H	L

§ Two CLK edges are needed to propagate the data. The data is loaded in the first register when SEL is low and propagates to the second register when SEL is high.

### OUTPUT ENABLE

INPUTS			OUTPUTS	
CLK	OE	DIR	A	1B, 2B
↑	H	X	Z	Z
↑	L	L	Z	Active
↑	L	H	Active	Z

### ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	ALVCH 3V	UNIT
I <sub>CC</sub>	MAX	0.04	mA
I <sub>OH</sub>	MAX	-24	mA
I <sub>OL</sub>	MAX	24	mA

### TIMING REQUIREMENTS AND SWITCHING CHARACTERISTICS

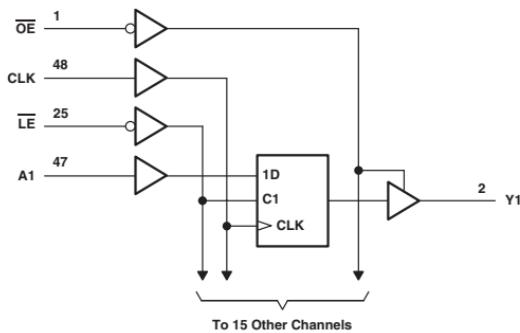
PARAMETER	INPUT	OUTPUT	MAX or MIN	ALVCH 3V
f <sub>max</sub>			MIN	150
t <sub>w</sub> Pulse duration, CLK high or low			MIN	3.3
t <sub>su</sub> Setup time	A data before CLK ↑		MIN	2
	B data before CLK ↑		MIN	1.8
	DIR before CLK ↑		MIN	1.7
	SEL before CLK ↑		MIN	1.8
t <sub>h</sub> Hold time	A data after CLK ↑		MIN	0.7
	B data after CLK ↑		MIN	0.6
	DIR after CLK ↑		MIN	0.5
	SEL after CLK ↑		MIN	0.8
t <sub>pd</sub>	CLK	A	MAX	5
		B		5.3
t <sub>en</sub>	OE	A	MAX	5.7
		B		7.4
t <sub>dis</sub>	OE	A	MAX	5.7
		B		6.4

UNIT f<sub>max</sub> : MHz other : ns

**16334**

**16-BIT UNIVERSAL BUS DRIVER WITH 3-STATE OUTPUTS**

**Logic Diagram**



FUNCTION TABLE

INPUTS				OUTPUT
OE	LE	CLK	A	Y
H	X	X	X	Z
L	L	X	L	L
L	L	X	H	H
L	H	↑	L	L
L	H	↑	H	H
L	H	L or H	X	Y <sub>0†</sub>

† Output level before the indicated steady-state input conditions were established

## ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	ALVC 3V	ALVCH 3V	AVC 3V	UNIT
I <sub>CC</sub>	MAX	0.04	0.04	0.04	mA
I <sub>OH</sub>	MAX	-24	-24	-12	mA
I <sub>OL</sub>	MAX	24	24	12	mA

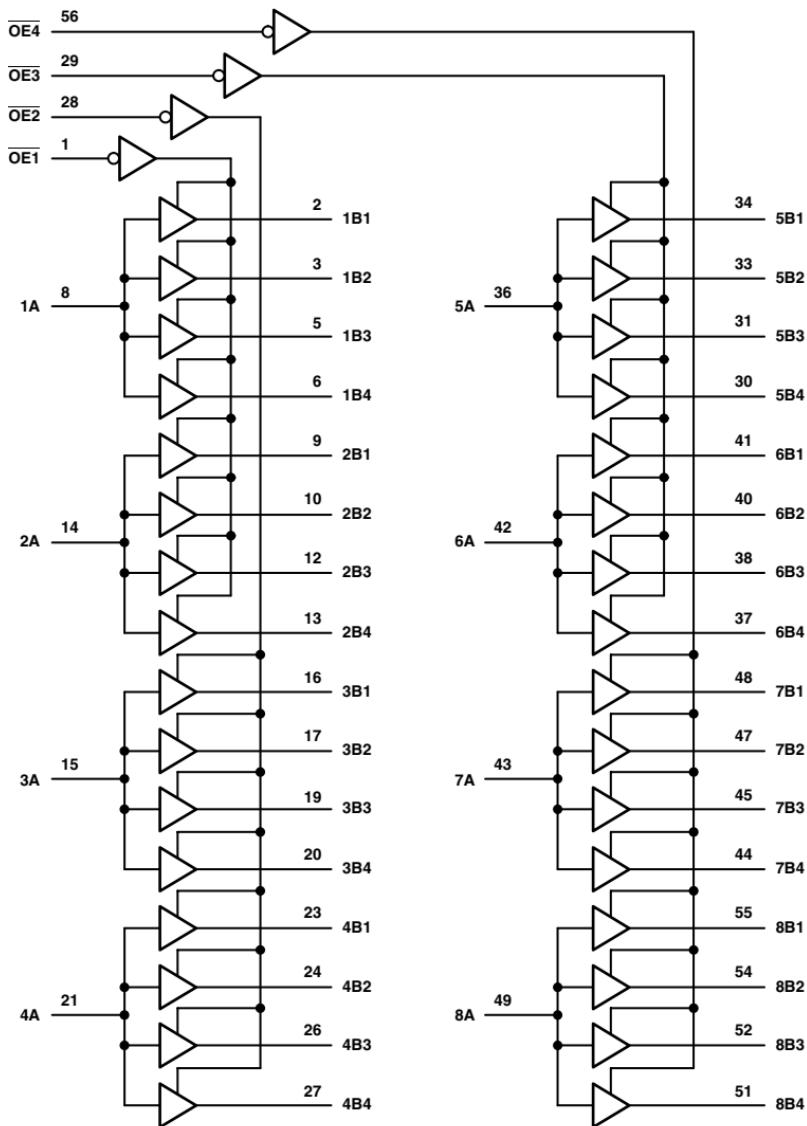
## TIMING REQUIREMENTS AND SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	ALVC 3V	ALVCH 3V	AVC 3V
f <sub>max</sub>			MIN	150	150	150
t <sub>w</sub> Pulse duration	LE low			3.3	3.3	3.3
	CLK high or low		MIN	3.3	3.3	3.3
t <sub>uw</sub> Setup time	Data before CLK ↑		MIN	1.5	1.5	0.7
	Data before LE ↑ CLK high		MIN	1.3	1.3	0.9
	Data before LE ↑ CLK low		MIN	1.2	1.2	1
t <sub>th</sub> Hold time	Data after CLK ↑		MIN	0.9	0.9	0.7
	Data after LE ↑ CLK high		MIN	1.1	1.1	1.5
	Data after LE ↑ CLK low		MIN	1.1	1.1	1.3
t <sub>pd</sub>	A		MAX	3.3	3.3	2.5
	LE	Y		4.4	4.4	4
	CLK		MAX	4.1	4.1	3.1
t <sub>on</sub>	OE	Y		4.6	4.6	6.2
t <sub>dis</sub>	OE	Y	MAX	4.4	4.4	5.3

UNIT f<sub>max</sub> : MHz other : ns

## 1-BIT TO 4-BIT ADDRESS DRIVER WITH 3-STATE OUTPUTS

Logic Diagram



**FUNCTION TABLE**

INPUTS		OUTPUT
OE	A	Bn
L	H	H
L	L	L
H	H	Z

**ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS**

PARAMETER	MAX or MIN	ALVCH 3V	UNIT
I <sub>CC</sub>	MAX	0.04	mA
I <sub>OH</sub>	MAX	-24	mA
I <sub>OL</sub>	MAX	24	mA

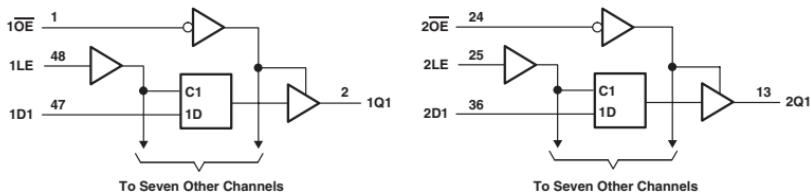
**SWITCHING CHARACTERISTICS**

PARAMETER	INPUT	OUTPUT	MAX or MIN	ALVCH 3V
t <sub>PLH</sub>				4
t <sub>PHL</sub>	A	B	MAX	4
t <sub>PZH</sub>				5.1
t <sub>PZL</sub>	OE	B	MAX	5.1
t <sub>PHZ</sub>	OE	B	MAX	4
t <sub>PLZ</sub>				4

UNIT: ns

## 16-BIT TRANSPARENT LATCHES WITH 3-STATE OUTPUTS

Logic Diagram



**FUNCTION TABLE**  
(each latch)

INPUTS			OUTPUT Q
OE	LE	D	
L	H	H	H
L	H	L	L
L	L	X	Q <sub>O</sub>
H	X	X	Z

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	ABT	LVTH 3V	ALVTH 3V	AC	ACT	AHC	AHCT	LVC 3V	LVC ver.A 3V	LVCH 3V	ALVCH 3V	UNIT
I <sub>CC</sub>	MAX	85	5	5	0.08	0.08	0.04	0.04	0.04	0.02	0.02	0.04	mA
I <sub>OH</sub>	MAX	-32	-32	-32	-24	-24	-8	-8	-24	-24	-24	-24	mA
I <sub>OL</sub>	MAX	64	64	64	24	24	8	8	24	24	24	24	mA

PARAMETER	MAX or MIN	AVC 3V	AUC 1.8V	AUC 2.3V	UNIT
I <sub>CC</sub>	MAX	0.04	0.02	0.02	mA
I <sub>OH</sub>	MAX	-12	-8	-9	mA
I <sub>OL</sub>	MAX	12	8	9	mA

TIMING REQUIREMENTS AND SWITCHING CHARACTERISTICS

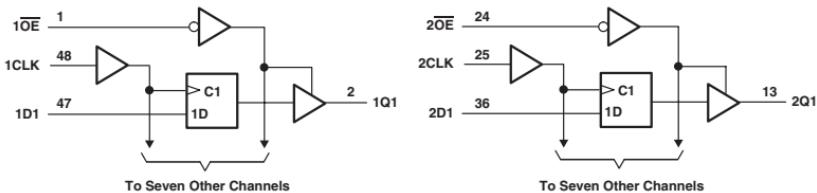
PARAMETER	INPUT	OUTPUT	MAX or MIN	ABT	LVTH 3V	ALVTH 3V	AC	ACT	AHC	AHCT
t <sub>W</sub> Pulse duration, LE high or low			MIN	3.3	3	1.5	4	1	5	6.5
t <sub>WS</sub> Setup time	Data before LE ↓, data high		MIN	1.5	1	1.4	1.5	1	4	1.5
	Data before LE ↓, data low		MIN	1.5	1	0.9	1.5	1	4	1.5
t <sub>th</sub> Hold time	Data after LE ↓, data high		MIN	1	1	0.9	2.4	5	1	3.5
	Data after LE ↓, data low		MIN	1	1	1.4	2.4	5	1	3.5
t <sub>PLH</sub>	D	Q	MAX	6.3	3.8	3.1	9.7	11.1	10.5	10.5
t <sub>PHL</sub>				6.2	3.6	3.3	10.1	12.3	10.5	10.5
t <sub>PLH</sub>	LE	Q	MAX	6.7	4.3	3.3	11.9	12.8	10.5	10.5
t <sub>PHL</sub>				6.1	4	3.5	10.9	12.2	10.5	10.5
t <sub>PZH</sub>	OE	Q	MAX	6.1	4.3	4	10.8	12.1	11.5	11.5
t <sub>PZL</sub>				5.6	4.3	3.4	12.8	14.2	11.5	11.5
t <sub>PHZ</sub>	OE	Q	MAX	8.1	5	4.9	8.8	10.7	11.5	12
t <sub>PZL</sub>				6.5	4.7	4.5	8.1	9.4	11.5	12

PARAMETER	INPUT	OUTPUT	MAX or MIN	LVC 3V	LVC ver.A 3V	LVCH 3V	ALVCH 3V	AVC 3V	AUC 1.8V	AUC 2.3V
t <sub>W</sub> Pulse duration, LE high or low			MIN	4	3.3	3.3	3.3	1.8	2.1	1.7
t <sub>WS</sub> Setup time	Data before LE ↓, data high		MIN	2	1.7	1.7	1.1	0.8	0.4	0.4
	Data before LE ↓, data low		MIN	2	1.7	1.7	1.1	0.8	0.4	0.4
t <sub>th</sub> Hold time	Data after LE ↓, data high		MIN	2	1.2	1.2	1.4	1	0.7	0.6
	Data after LE ↓, data low		MIN	2	1.2	1.2	1.4	1	0.7	0.6
t <sub>PLH</sub>	D	Q	MAX	7	4.2	4.2	3.6	2.8	2.4	1.9
t <sub>PHL</sub>				7	4.2	4.2	3.6	2.8	2.4	1.9
t <sub>PLH</sub>	LE	Q	MAX	8	4.6	4.6	3.9	3.2	2.8	2.1
t <sub>PHL</sub>				8	4.6	4.6	3.9	3.2	2.8	2.1
t <sub>PZH</sub>	OE	Q	MAX	8	4.7	4.7	4.7	3.4	2.9	2.2
t <sub>PZL</sub>				8	4.7	4.7	4.7	3.4	2.9	2.2
t <sub>PHZ</sub>	OE	Q	MAX	7	5.9	5.9	4.1	3.9	4.6	2.5
t <sub>PZL</sub>				7	5.9	5.9	4.1	3.9	4.6	2.5

UNIT: ns

AUC: Preview

Logic Diagram



**FUNCTION TABLE**  
(each flip-flop)

INPUTS	OUTPUT		
OE	CLK	D	Q
L ↑	H		H
L ↑	L		L
L H or L X	X		Q <sub>O</sub>
H X	X		Z

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	ABT	LVTH 3V	ALVTH 3V	AC	ACT	AHC	AHCT	LVC 3V	LVC ver.A 3V	LVCH 3V	ALVCH 3V	UNIT
I <sub>CC</sub>	MAX	72	5	5	0.08	0.08	0.04	0.04	0.04	0.02	0.02	0.04	mA
I <sub>OH</sub>	MAX	-32	-32	-32	-24	-24	-8	-8	-24	-24	-24	-24	mA
I <sub>OL</sub>	MAX	64	64	64	24	24	8	8	24	24	24	24	mA

PARAMETER	MAX or MIN	AVC 3V	AUC 1.8V	AUC 2.3V	AUCH 1.8V	AUCH 2.3V	UNIT
I <sub>CC</sub>	MAX	0.04	0.02	0.02	0.02	0.02	mA
I <sub>OH</sub>	MAX	-12	-8	-9	-8	-9	mA
I <sub>OL</sub>	MAX	12	8	9	8	9	mA

TIMING REQUIREMENTS AND SWITCHING CHARACTERISTICS

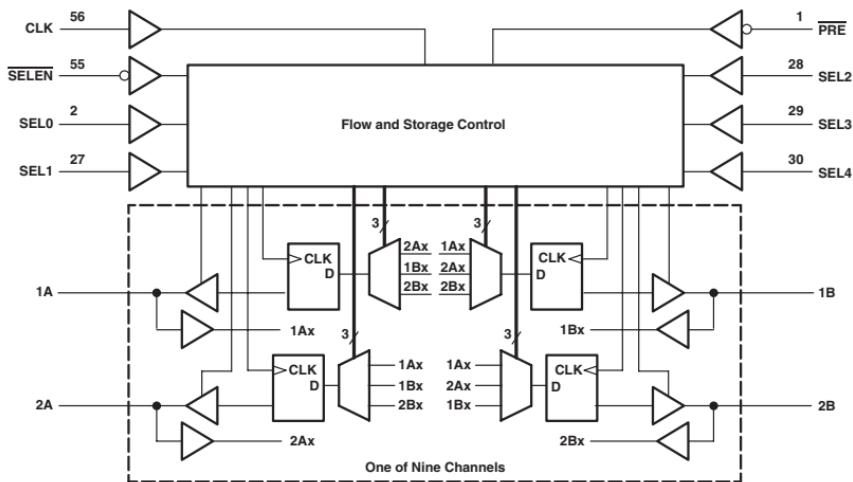
PARAMETER	INPUT	OUTPUT	MAX or MIN	ABT	LVTH 3V	ALVTH 3V	AC	ACT	AHC	AHCT	LVC 3V
f <sub>max</sub>			MIN	150	160	250	100	65	110	110	100
t <sub>w</sub> Pulse duration	CLK high		MIN	3.3	3	1.5	5	7.5	5	6.5	4
	CLK low			3.3	3	1.5	5	4.5	5	6.5	4
t <sub>su</sub> Setup time	Data before CLK ↑ , data high		MIN	1.1	1.8	1	5	4.5	3	2.5	2
	Data before CLK ↑ , data low			1.1	1.8	1.5	5	4.5	3	2.5	2
t <sub>h</sub> Hold time	Data after CLK ↑ , data high		MIN	1.3	0.8	0.5	0	6.5	2	2.5	1.5
	Data after CLK ↑ , data low			1.3	0.8	1	0	6.5	2	2.5	1.5
t <sub>PLH</sub>	CLK	Q	MAX	6.2	4.5	3.2	10.8	12.4	11.5	11.5	7.5
t <sub>PHL</sub>			MAX	5.9	4	3.2	10.6	12.2	11.5	11.5	7.5
t <sub>PZH</sub>	OE	Q	MAX	5.6	4.5	3.8	10.2	11.9	11.5	11.5	7.5
t <sub>PZL</sub>			MAX	5.3	4.4	3.3	12.1	13.4	11.5	11.5	7.5
t <sub>PHZ</sub>	OE	Q	MAX	8.2	5	4.6	8.2	10.4	11.5	12	7
t <sub>PZL</sub>			MAX	6.6	4.6	4.2	7.9	9.8	11.5	12	7

PARAMETER	INPUT	OUTPUT	MAX or MIN	LVC ver.A 3V	LVCH 3V	ALVCH 3V	AVC 3V	AUC 1.8V	AUC 2.3V	AUCH 1.8V	AUCH 2.3V
f <sub>max</sub>			MIN	150	150	150	200	250	250	250	250
t <sub>w</sub> Pulse duration	CLK high		MIN	3.3	3.3	3.3	2.5	1.9	1.9	1.9	1.9
	CLK low			3.3	3.3	3.3	2.5	1.9	1.9	1.9	1.9
t <sub>su</sub> Setup time	Data before CLK ↑ , data high		MIN	1.9	1.9	1.9	1.4	0.6	0.6	0.6	0.6
	Data before CLK ↑ , data low			1.9	1.9	1.9	1.4	0.6	0.6	0.6	0.6
t <sub>h</sub> Hold time	Data after CLK ↑ , data high		MIN	1.9	1.1	0.5	1.1	0.4	0.4	0.4	0.4
	Data after CLK ↑ , data low			1.9	1.1	0.5	1.1	0.4	0.4	0.4	0.4
t <sub>PLH</sub>	CLK	Q	MAX	4.5	4.5	4.2	3.3	2.8	2.2	2.8	2.2
t <sub>PHL</sub>			MAX	4.5	4.5	4.2	3.3	2.8	2.2	2.8	2.2
t <sub>PZH</sub>	OE	Q	MAX	4.6	4.6	4.8	3.4	2.9	2.2	2.9	2.2
t <sub>PZL</sub>			MAX	4.6	4.6	4.8	3.4	2.9	2.2	2.9	2.2
t <sub>PHZ</sub>	OE	Q	MAX	5.5	5.5	4.3	3.9	4.5	2.2	4.5	2.2
t <sub>PZL</sub>			MAX	5.5	5.5	4.3	3.9	4.5	2.2	4.5	2.2

UNIT f<sub>max</sub> : MHz other : ns

## 9-BIT, 4-PORT UNIVERSAL BUS EXCHANGER WITH 3-STATE OUTPUTS

Logic Diagram



**FUNCTION TABLE**

INPUTS		OUTPUT RECEIVE PORT
CLK	SEND PORT	
X	X	B <sub>0</sub> †
X	L	L
X	H	H
↑	L	L
↑	H	H
H	X	B <sub>0</sub> †
L	X	B <sub>0</sub> †

† Output level before the indicated steady-state input conditions were established

**DATA-FLOW CONTROL**

INPUTS								DATA FLOW
PRE	SELEN	CLK	SEL0	SEL1	SEL2	SEL3	SEL4	
H	X	X	X	X	X	X	X	All outputs disabled
L	H	↑	X	X	X	X	X	No change
L	L	↑	0	0	0	0	0	None, all I/Os off
L	L	↑	0	0	0	0	1	Not used
L	L	↑	0	0	0	1	0	Not used
L	L	↑	0	0	0	1	1	Not used
L	L	↑	0	0	1	0	0	Not used
L	L	↑	0	0	1	0	1	Not used
L	L	↑	0	0	1	1	0	Not used
L	L	↑	0	0	1	1	1	Not used
L	L	↑	0	1	0	0	0	2A to 1A and 1B to 2B
L	L	↑	0	1	0	0	1	2A to 1A
L	L	↑	0	1	0	1	0	2B to 1B
L	L	↑	0	1	0	1	1	2A to 1A and 2B to 1B
L	L	↑	0	1	1	0	0	1A to 2A and 1B to 2B
L	L	↑	0	1	1	0	1	1A to 2A
L	L	↑	0	1	1	1	0	1B to 2B
L	L	↑	0	1	1	1	1	1A to 2A and 2B to 1B
L	L	↑	1	0	0	0	0	1A to 1B and 2B to 2A
L	L	↑	1	0	0	0	1	1A to 1B
L	L	↑	1	0	0	1	0	2A to 2B
L	L	↑	1	0	0	1	1	1A to 1B and 2A to 2B
L	L	↑	1	0	1	0	0	1B to 1A
L	L	↑	1	0	1	1	0	2B to 2A
L	L	↑	1	0	1	1	1	1B to 1A and 2B to 2A
L	L	↑	1	1	0	0	0	2B to 1A
L	L	↑	1	1	0	1	1	2B to 1A and 1B to 2A
L	L	↑	1	1	1	0	0	1A to 2B and 1B to 2A
L	L	↑	1	1	1	0	1	1A to 2B
L	L	↑	1	1	1	1	0	2A to 1B
L	L	↑	1	1	1	1	1	1A to 2B and 2A to 1B

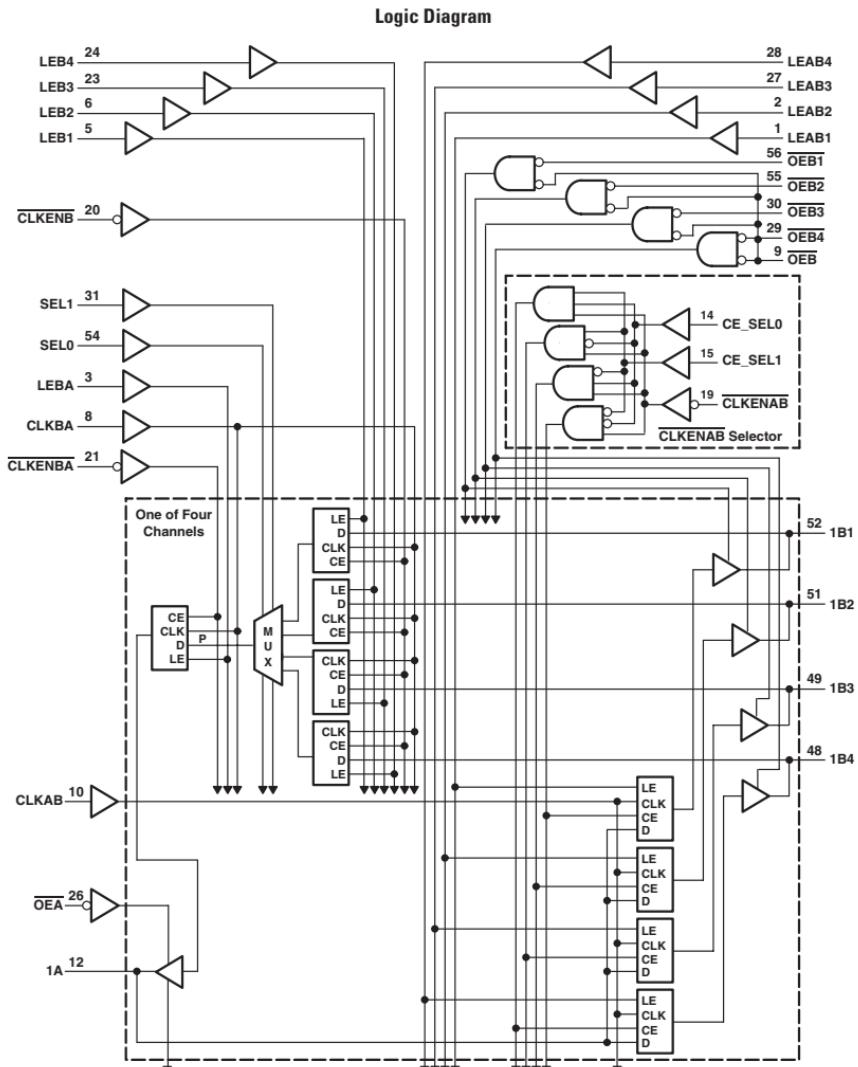
**ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS**

PARAMETER	MAX or MIN	ALVCH 3V	ALVC HR 3V	UNIT
I <sub>CC</sub>	MAX	0.04	0.04	mA
I <sub>OH</sub>	MAX	-24	-12	mA
I <sub>OL</sub>	MAX	24	12	mA

**TIMING REQUIREMENTS AND SWITCHING CHARACTERISTICS**

PARAMETER	INPUT	OUTPUT	MAX or MIN	ALVCH 3V	ALVC HR 3V
t <sub>max</sub>			MIN	120	120
t <sub>w</sub>	Pulse duration, CLK high or low		MIN	3	3
t <sub>su</sub>	A or B data before CLK ↑ SEL before CLK ↑ SELEN before CLK ↑ PRE before CLK ↑		MIN	1.4	1.4
t <sub>th</sub>	A or B data after CLK ↑ SEL after CLK ↑ SELEN after CLK ↑		MIN	3.5	3.5
t <sub>pd</sub>	CLK	A or B	MAX	5.1	6.2
t <sub>ten</sub>	CLK	A or B	MAX	5.7	6.8
t <sub>dis</sub>	CLK PRE	A or B	MAX	5.7	6.1
				6.1	6.4

UNIT f<sub>max</sub> : MHz other : ns



**FUNCTION TABLE**
**A-TO-B OUTPUT ENABLE**

INPUTS	OUTPUT
OEB	OEBn
H	Z
H	L
L	H
L	L

Active

 $t_n = 1, 2, 3, 4$ 
**A-TO-B OUTPUT ENABLE  
(assuming OEB = L, OEBn = L) ‡**

INPUTS									OUTPUTS			
CLKENAB	CE_SEL1	CE_SELO	CLKAB	LEAB1	LEAB2	LEAB3	LEAB4	B1	B2	B3	B4	
X	X	X	H or L	H	L	L	L	A	A0	A0	A0	
X	X	X	H or L	H	H	H	L	A	A	A	A	
L	X	X	L	L	L	L	L	A0	A0	A0	A0	
L	X	X	L	L	L	L	L	A	A0	A0	A0	
L	L	L	H	↑	L	L	L	A0	A	A0	A0	
L	H	L	H	↑	L	L	L	A0	A0	A	A0	
L	H	H	H	↑	L	L	L	A0	A0	A0	A0	
H	X	X	↑	L	L	L	L	A0	A0	A0	A0	

**B-TO-A STORAGE  
(after point P)**

INPUTS									P
CLKENB	CLKBA	LEB1	LEB2	LEB3	LEB4	SEL1	SEL0		P
X	X	H	L	L	L	L	L	B1	
X	X	L	H	L	L	H	L	B2	
X	X	L	L	H	L	H	L	B3	
X	X	L	L	L	H	H	L	B4	
						L	L	B1	
						L	H	B2	
L	↑	L	L	L	L	H	L	B3	
L	L	L	L	L	L	H	H	B4	
						L	L	B1 <sub>0†</sub>	
						L	H	B2 <sub>0†</sub>	
						H	L	B3 <sub>0†</sub>	
						H	H	B4 <sub>0†</sub>	

 $†$  Output level before the indicated steady-state input conditions were established

**B-TO-A STORAGE  
(after point P)**

INPUTS					OUTPUT
CLKENBA	CLKBA	LEBA	OEA	B	A
X	X	X	H	X	Z
X	X	H	L	L	L
X	X	H	L	H	H
H	X	L	L	X	A0†
L	↑	L	L	L	L
L	↑	L	L	H	H
L	L	L	L	X	A0†

**ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS**

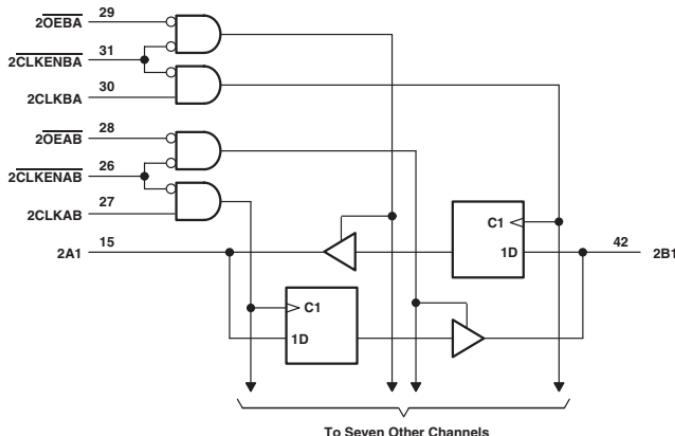
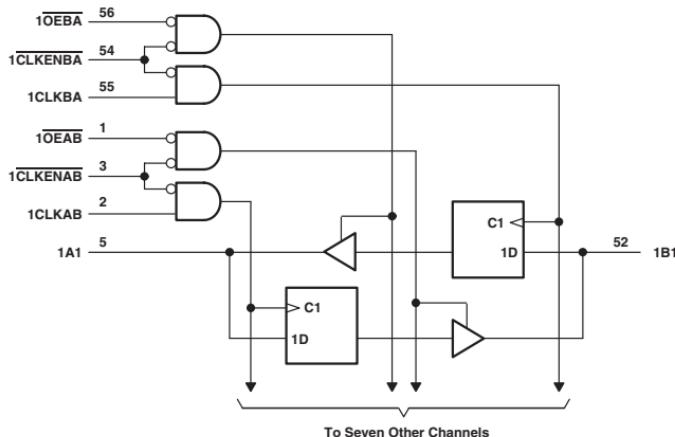
PARAMETER	MAX or MIN	ABTH	UNIT
I <sub>CC</sub>	MAX	32	mA
I <sub>OH</sub>	MAX	-32	mA
I <sub>OL</sub>	MAX	64	mA

**TIMING REQUIREMENTS AND SWITCHING CHARACTERISTICS**

PARAMETER		MAX or MIN	ABTH	PARAMETER	INPUT	OUTPUT	MAX or MIN	ABTH
<i>f</i> <sub>max</sub>		MIN	160	<i>t<sub>PLH</sub></i>	B	A	MAX	6.5
CLKAB high or low		MIN	3.8	<i>t<sub>PHL</sub></i>				6.5
CLKBA high or low		MIN	4.5	<i>t<sub>PZH</sub></i>	OEA	A	MAX	5.6
CLKENAB		MIN	2.2	<i>t<sub>PZL</sub></i>				5.2
LEAB1, 2, 3 or 4 high		MIN	2.1	<i>t<sub>PHZ</sub></i>	OEA	A	MAX	5.9
LEBA high		MIN	2.4	<i>t<sub>PLZ</sub></i>				6.5
LEB1, 2, 3 or 4 high		MIN	2.4	<i>t<sub>PLH</sub></i>	A	B	MAX	5.7
<i>t<sub>su</sub></i> Setup time		MIN	3.2	<i>t<sub>PHL</sub></i>	CE_SEL0/1	MIN	3.2	5.7
Before CLKAB ↑		MIN	3.2	<i>t<sub>PZH</sub></i>	CLKENAB	MIN	3.2	6.4
Before CLKBA ↑		MIN	2.3	<i>t<sub>PZL</sub></i>	CLKENBA	MIN	2.5	6.3
Before LEAB1, 2, 3, or 4 ↓ A bus		MIN	3.6	<i>t<sub>PHZ</sub></i>	LEB1, 2, 3 or 4	MIN	4.3	7
Before LEAB1, 2, 3, or 4 ↓ A bus		MIN	3.8	<i>t<sub>PLZ</sub></i>	SEL0/1	MIN	4.5	6.1
Before CLKBA ↑		MIN	2.3	<i>t<sub>PHL</sub></i>	CE_SEL0/1	MIN	3.2	5.8
Before LEAB1, 2, 3 or 4 ↓ B bus		MIN	3.2	<i>t<sub>PZH</sub></i>	CLKENAB	MIN	3.2	5.6
Before CLKBA ↑		MIN	4	<i>t<sub>PZL</sub></i>	CLKENBA	MIN	1	6.1
Before LEAB1, 2, 3 or 4 ↓ B bus		MIN	4.4	<i>t<sub>PHZ</sub></i>	LEB1, 2, 3, 4	MIN	0	5.3
Before CLKBA ↑		MIN	4.3	<i>t<sub>PLZ</sub></i>	SEL0/1	MIN	1.5	7.4
<i>t<sub>th</sub></i> Hold time		MIN	0.5	<i>t<sub>PHL</sub></i>	CLKAB	B	MAX	7.7
after CLKAB ↑		MIN	1.1	<i>t<sub>PHL</sub></i>	LEBA	A	MAX	6.2
after CLKBA ↑		MIN	0.5	<i>t<sub>PZH</sub></i>	LEAB1, 2, 3, 4	B	MAX	5.9
after LEAB1, 2, 3, or 4 ↓ A bus		MIN	1.2	<i>t<sub>PZH</sub></i>	SEL0/1	MIN	0	5.6
after LEAB1, 2, 3, or 4 ↓ A bus		MIN	1.3	<i>t<sub>PLH</sub></i>	LEB1, 2, 3, 4	A	MAX	5.3
after CLKBA ↑		MIN	1	<i>t<sub>PLH</sub></i>	SEL0/1	MIN	1.5	5.8
after LEAB1, 2, 3 or 4 ↓ B bus		MIN	1.5	<i>t<sub>PLH</sub></i>	SEL	A	MAX	7.2
after CLKBA ↑		MIN	0.4	<i>t<sub>PLH</sub></i>				6.8
after LEAB1, 2, 3 or 4 ↓ B bus		MIN	0.1	<i>t<sub>PLH</sub></i>				7.5
after CLKBA ↑		MIN	0.1	<i>t<sub>PLH</sub></i>				6.9

UNIT f<sub>max</sub> : MHz other : ns

Logic Diagram



FUNCTION TABLE

INPUTS			OUTPUT
CLKENAB	CLKAB	OEAB	B
H	X	X	X
X	X	H	X
L	L	L	X
L	↑	L	L
L	↑	L	H

† A-to-B data flow is shown; B-to-A flow is similar but uses CLKENBA, CLKBA, and OEBA.

‡ Output level before the indicated steady-state input conditions were established.

## ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

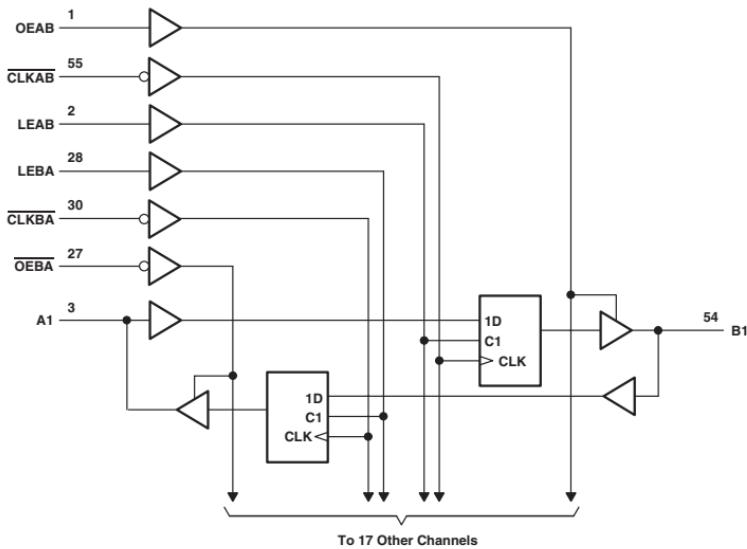
PARAMETER	MAX or MIN	ABT	ACT	UNIT
I <sub>CC</sub>	MAX	35	0.08	mA
I <sub>OH</sub>	MAX	-32	-24	mA
I <sub>OL</sub>	MAX	64	24	mA

## TIMING REQUIREMENTS AND SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	ABT	ACT
f <sub>max</sub>			MIN	150	55
t <sub>w</sub> Pulse duration, CLKAB or CLKBA high			MIN	3.3	4
t <sub>w</sub> Pulse duration, CLKAB or CLKBA low				3.3	8.5
t <sub>su</sub> Setup time, data before CLKAB ↑ or CLKBA ↑			MIN	4	6
t <sub>th</sub> Hold time, data after CLKAB ↑ or CLKBA ↑			MIN	1	1
t <sub>PH</sub>	CLK	A or B	MAX	4.9	11.8
t <sub>PHL</sub>				4.9	11.7
t <sub>PZH</sub>	OE	A or B	MAX	4.9	11.9
t <sub>PZL</sub>				6.8	13.4
t <sub>PHZ</sub>	OE	A or B	MAX	5.5	9.9
t <sub>PZL</sub>				5.3	9.5
t <sub>PZH</sub>	CLKEN	A or B	MAX	5.7	12.5
t <sub>PZL</sub>				7.2	14.3
t <sub>PHZ</sub>	CLKEN	A or B	MAX	5.8	11.2
t <sub>PZL</sub>				5.4	10.9

UNIT f<sub>max</sub> : MHz other : ns

Logic Diagram



FUNCTION TABLE

INPUTS			OUTPUT	
OEAB	LEAB	CLKAB	A	B
L	X	X	X	Z
H	H	X	L	L
H	H	X	H	H
H	L	↓	L	L
H	L	↓	H	H
H	L	H	X	$B_0^{\dagger}$
H	L	L	X	$B_0^{\ddagger}$

† A-to-B data flow is shown; B-to-A flow is similar but uses OEBA, LEBA, and CLKBA.

‡ Output level before the indicated steady-state input conditions were established.

§ Output level before the indicated steady-state input conditions were established, provided that CLKAB was low before LEAB went low.

## ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

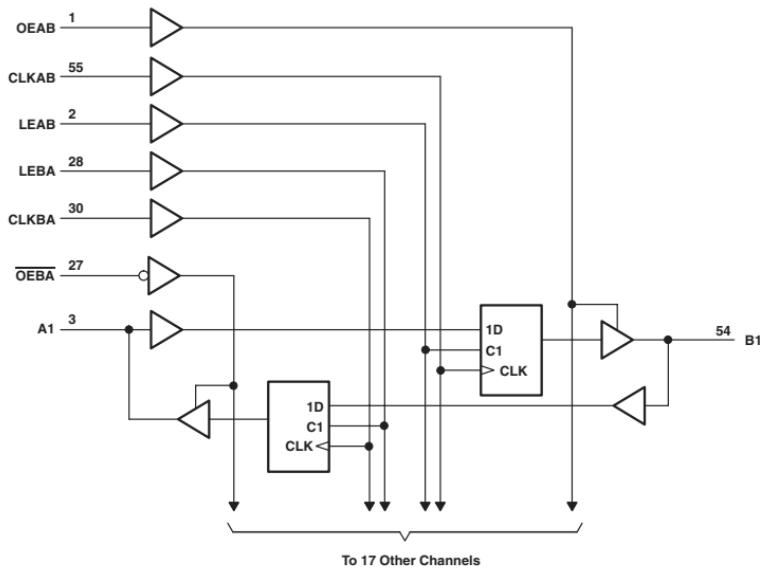
PARAMETER	MAX or MIN	ABT	LVTH 3V	ALVCH 3V	UNIT
$I_{CC}$	MAX	36	5	0.04	mA
$I_{OH}$	MAX	-32	-32	-24	mA
$I_{OL}$	MAX	64	64	24	mA

## TIMING REQUIREMENTS AND SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	ABT	LVTH 3V	ALVCH 3V
$t_{max}$			MIN	150	150	150
$t_{W}$ Pulse duration	LEAB or LEBA high		MIN	2.5	3.3	3.3
	CLKAB or CLKBA high or low			3	3.3	3.3
$t_{SU}$ Setup time	A before CLKAB ↓			3	2.9	1.3
	B before CLKBA ↓			3	2.9	1.3
	A before LEAB ↓ or LEBA ↓ CLK high		MIN	1	1.4	1
	A before LEAB ↓ or LEBA ↓ CLK low			2.5	2.9	1.4
$t_{H}$ Hold time	A after CLKAB ↓ or B after CLKBA ↓			0	0.4	1.3
	A after LEAB ↓ or B after LEBA ↓ high		MIN	2	1.6	1.5
	A after LEAB ↓ or B after LEBA ↓ low			2	1.6	1.2
$t_{PLH}$	A or B	B or A	MAX	4	3.7	3.9
$t_{PHL}$				4.9	3.7	3.9
$t_{PZH}$	LEAB or LEBA	B or A	MAX	5	5.1	4.7
$t_{PZL}$				5	5.1	4.7
$t_{PZH}$	CLKAB or CLKBA	B or A	MAX	5.3	5	5.5
$t_{PZL}$				5.3	5	5.5
$t_{PZH}$	OEAB	B	MAX	5.1	4.8	4.6
$t_{PZL}$				5.4	4.8	4.6
$t_{PZH}$	OEAB	B	MAX	6.5	5.8	5
$t_{PZL}$				5.4	5.8	5
$t_{PZH}$	OEBA	A	MAX	5.1	4.8	5.2
$t_{PZL}$				5.4	4.8	5.2
$t_{PZH}$	OEBA	A	MAX	6.5	5.8	4.3
$t_{PZL}$				5.4	5.8	4.3

UNIT  $f_{max}$  : MHz other : ns

Logic Diagram



FUNCTION TABLE

INPUTS			OUTPUT
OEAB	LEAB	CLKAB	B
L	X	X	X
H	H	X	L
H	H	X	H
H	L	↑	L
H	L	↑	H
H	L	H	X
H	L	L	X
			$B_0^{\dagger}$
			$B_0^{\ddagger}$

† A-to-B data flow is shown; B-to-A flow is similar but uses  $\bar{OEBA}$ ,  $LEBA$ , and  $CLKBA$ .

‡ Output level before the indicated steady-state input conditions were established, provided that  $CLKAB$  was high before  $LEAB$  went low.

§ Output level before the indicated steady-state input conditions were established.

## ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	ABT	LVTH 3V	ALVCH 3V	AUC 1.8V	AUC 2.3V	UNIT
$I_{CC}$	MAX	76	5	0.04	0.02	0.02	mA
$I_{OH}$	MAX	-32	-32	-24	-8	-9	mA
$I_{OL}$	MAX	64	64	24	8	9	mA

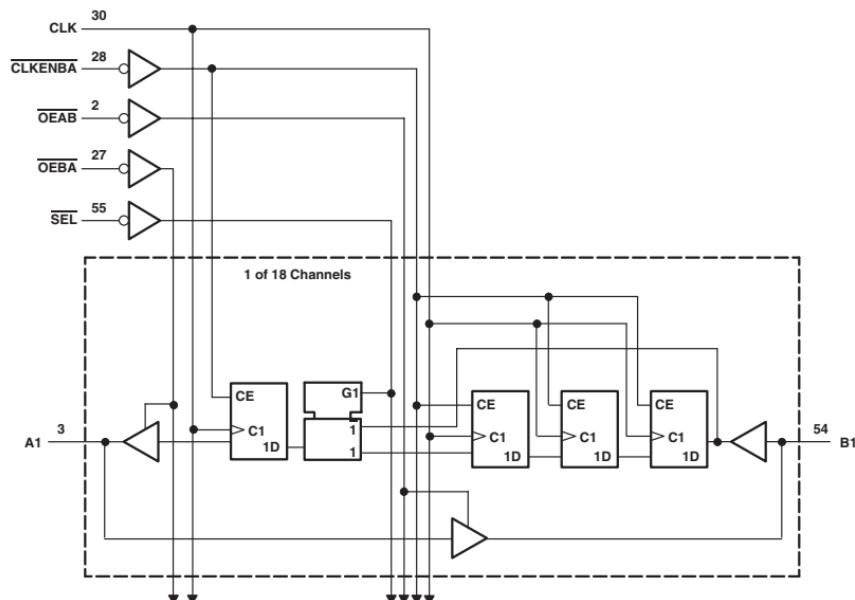
## TIMING REQUIREMENTS AND SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	ABT	LVTH 3V	ALVCH 3V	AUC 1.8V	AUC 2.3V
$t_{max}$			MIN	105	150	150	300	350
$t_{W}$ Pulse duration	LEAB or LEBA high CLKAB or CLKBA high or low		MIN	3.3	3.3	3.3	1.5	1.5
$t_{W}$ Setup time	A before CLKAB ↑ B before CLKBA ↑ A before LEAB ↓ or LEBA ↓ CLK high A before LEAB ↓ or LEBA ↓ CLK low		MIN	4.7	3.3	3.3	1.5	1.5
$t_{H}$ Hold time	A after CLKAB ↑ or B after CLKBA ↑ A after LEAB ↓ or B after LEBA ↓		MIN	1	1	0.7	0.9	0.9
$t_{PLH}$	A or B	B or A	MAX	3.7	3.7	3.9	2.8	2.3
$t_{PHL}$				4	3.7	3.9	2.8	2.3
$t_{PZH}$	LEAB or LEBA	B or A	MAX	5.1	5.1	4.6	3.8	3
$t_{PZL}$	CLKAB or CLKBA	B or A	MAX	4.4	5.1	4.6	3.8	3
$t_{PZL}$	OEAB	B	MAX	4.7	4.8	4.6	3.4	2.8
$t_{PZH}$	OEAB	B	MAX	6.5	4.8	4.6	3.4	2.8
$t_{PLZ}$	OEAB	A	MAX	5.8	5.8	5	3.2	3.1
$t_{PZH}$	OEBA	A	MAX	4.9	5.8	5	3.2	3.1
$t_{PZL}$	OEBA	A	MAX	4.7	4.8	5	3.7	3
$t_{PZH}$	OEBA	A	MAX	6.5	4.8	5	3.7	3
$t_{PZL}$	OEBA	A	MAX	5.8	5.8	4.2	5.2	3
				4.9	5.8	4.2	5.2	3

UNIT fmax : MHz other : ns

AUC:Preview

Logic Diagram



**FUNCTION TABLE**
**B-TO-A STORAGE ( $\bar{OEBA} = L$ )**

INPUTS				OUTPUT
CLKENBA	CLK	SEL	B	A
H	X	X	X	A <sub>0</sub> <sup>T</sup>
L	↑	H	L	L
L	↑	H	H	H
L	↑	L	L	L <sup>‡</sup>
L	↑	L	H	H <sup>‡</sup>

<sup>T</sup> Output level before the indicated steady-state input conditions were established.

<sup>‡</sup> Four positive CLK edges are needed to propagate data from B to A when SEL is low.

**ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS**

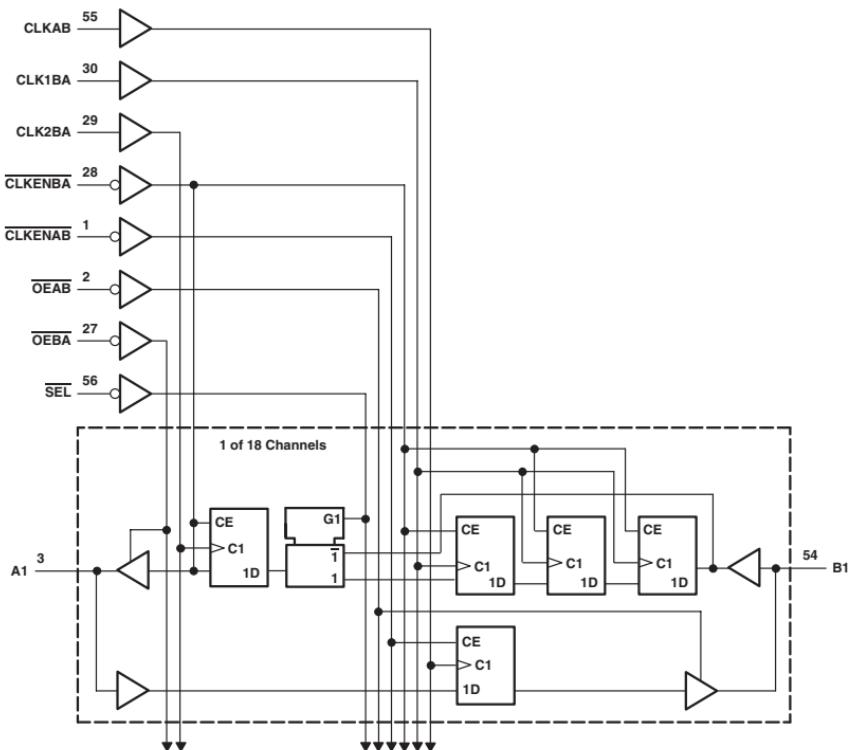
PARAMETER	MAX or MIN	ALVCH 3V	UNIT
I <sub>CC</sub>	MAX	0.04	mA
I <sub>OH</sub>	MAX	-24	mA
I <sub>OL</sub>	MAX	24	mA

**TIMING REQUIREMENTS AND SWITCHING CHARACTERISTICS**

PARAMETER	INPUT	OUTPUT	MAX or MIN	ALVCH 3V
t <sub>max</sub>			MIN	150
t <sub>w</sub>	Pulse duration, CLK high or low		MIN	3
t <sub>u</sub> Setup time	B data before CLK ↑		MIN	1.1
	SEL before CLK ↑		MIN	2.1
	CLKENBA before CLK ↑		MIN	2
t <sub>h</sub> Hold time	B data after CLK ↑		MIN	1.2
	SEL after CLK ↑		MIN	0.8
	CLKENBA after CLK ↑		MIN	0.3
t <sub>pd</sub>	A	B		3.2
	CLK	A	MAX	5.2
t <sub>en</sub>	OEAB or OEBA	A or B		5.1
t <sub>dis</sub>	OEAB or OEBA	A or B	MAX	4.9

UNIT f<sub>max</sub> : MHz other : ns

Logic Diagram



### FUNCTION TABLE

#### A-TO-B STORAGE ( $\text{OEAB} = \text{L}$ )

INPUTS		OUTPUT	
CLKENAB	CLK2BA	A	B
H	X	X	$B_0 \dagger$
L	↑	L	L
L	↑	H	H
L	↑	L	L
L	↑	L	$H \ddagger$

† Output level before the indicated steady-state input conditions were established

#### B-TO-A STORAGE ( $\text{OEBA} = \text{L}$ )

INPUTS					OUTPUT
CLKENA	CLK2BA	CLK1BA	SEL	B	A
H	X	X	X	X	$A_0 \dagger$
L	↑	X	H	L	L
L	↑	X	H	H	H
L	↑	↑	L	L	$L \ddagger$
L	↑	↑	L	H	$H \ddagger$

† Output level before the indicated steady-state input conditions were established

‡ Three CLK1BA edges and one CLK2BA edge are needed to propagate data from B to A when SEL is low.

### ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	ALVCH 3V	UNIT
$I_{CC}$	MAX	0.04	mA
$I_{OH}$	MAX	-24	mA
$I_{OL}$	MAX	24	mA

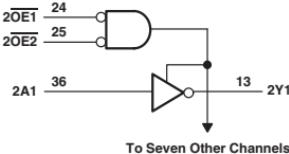
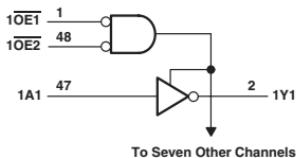
### TIMING REQUIREMENTS AND SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	ALVCH 3V
$t_{max}$			MIN	150
$t_W$	Pulse duration, CLK high or low		MIN	3
$t_{su}$ Setup time	A data before CLKAB ↑		MIN	1.3
	B data before CLK2BA ↑		MIN	1.7
	B data before CLK1BA ↑		MIN	1.1
	SEL before CLK2BA ↑		MIN	3.3
	CLKENAB before CLKAB ↑		MIN	1.6
	CLKENBA before CLK1BA ↑		MIN	2.1
	CLKENBA before CLK2BA ↑		MIN	2.2
$t_h$ Hold time	A data after CLKAB ↑		MIN	0.9
	B data after CLK2BA ↑		MIN	0.6
	B data after CLK1BA ↑		MIN	1
	SEL after CLK2BA ↑		MIN	0.1
	CLKENAB after CLKAB ↑		MIN	0.3
	CLKENBA after CLK1BA ↑		MIN	0.1
	CLKENBA after CLK2BA ↑		MIN	0
$t_{pd}$	CLKAB or CLK2BA	A or B		4.2
$t_{on}$	$\text{OEAB}$ or $\text{OEBA}$	A or B	MAX	5.1
$t_{dis}$	$\text{OEAB}$ or $\text{OEBA}$	A or B		4.9

UNIT fmax : MHz other : ns

## 16-BIT BUFFERS/DRIVERS WITH 3-STATE OUTPUTS

Logic Diagram

FUNCTION TABLE  
(each 8-bit section)

INPUTS			OUTPUT
OE1	OE2	A	Y
L	L	L	H
L	L	H	L
H	X	X	Z
X	H	X	Z

## ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	ABT	ACT	AHC	AHCT	LVCH 3V	UNIT
I <sub>CC</sub>	MAX	34	0.08	0.04	0.04	0.02	mA
I <sub>OH</sub>	MAX	-32	-24	-8	-8	-24	mA
I <sub>OL</sub>	MAX	64	24	8	8	24	mA

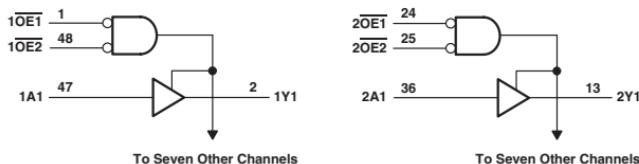
## SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	ABT	ACT	AHC	AHCT	LVCH 3V
t <sub>PLH</sub>	A	Y	MAX	4.1	7.5	8.5	10.5	3.7
t <sub>PHL</sub>				4.3	9.5	8.5	10.5	3.7
t <sub>PZH</sub>			MAX	5.1	8.9	10.5	13	4.8
t <sub>PZL</sub>	OE	Y		5.9	10.5	10.5	13	4.8
t <sub>PHZ</sub>			MAX	5.7	11.9	10.5	13	5.9
t <sub>PZL</sub>	OE	Y		4.7	11.1	10.5	13	5.9

UNIT: ns

## 16-BIT BUFFERS/DRIVERS WITH 3-STATE OUTPUTS

Logic Diagram

FUNCTION TABLE  
(each 8-bit section)

INPUTS			OUTPUT
OE1	OE2	A	Y
L	L	L	L
L	L	H	H
H	X	X	Z
X	H	X	Z

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

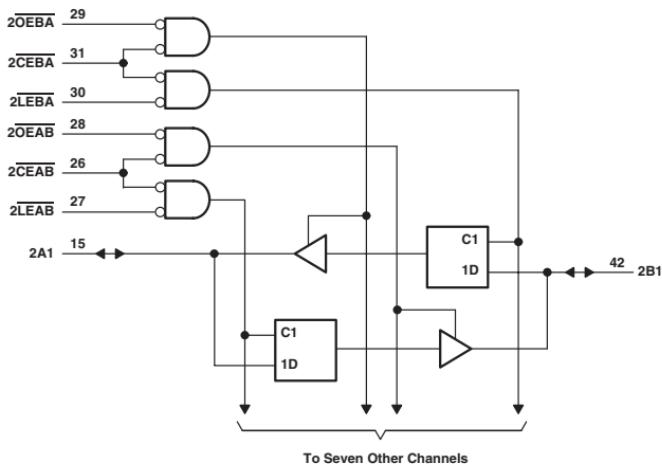
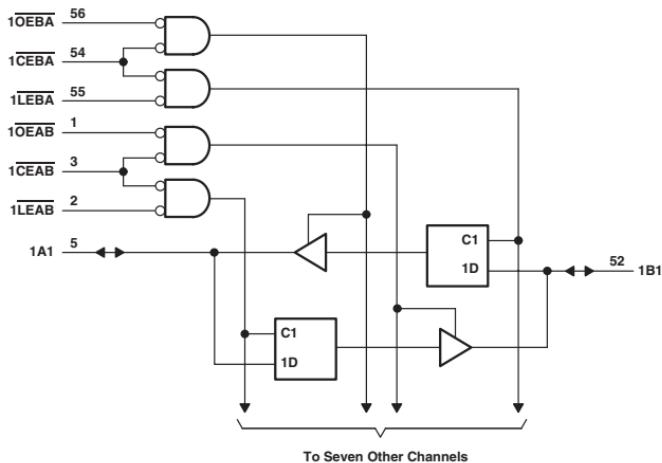
PARAMETER	MAX or MIN	ABT	LVTH 3V	ACT	AHC	AHCT	LVCH 3V	UNIT
$I_{CC}$	MAX	34	5	0.08	0.04	0.04	0.02	mA
$I_{OH}$	MAX	-32	-32	-24	-8	-8	-24	mA
$I_{OL}$	MAX	64	64	24	8	8	24	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	ABT	LVTH 3V	ACT	AHC	AHCT	LVCH 3V
$t_{PLH}$	A	Y	MAX	3.4	3.5	9	8.5	10.5	4.2
$t_{PHL}$				4.2	3.5	9.2	8.5	10.5	4.2
$t_{PZH}$	$\overline{OE}$	Y	MAX	5.2	4.6	9.7	10.5	13	5.6
$t_{PLZ}$				6	4.6	11	10.5	13	5.6
$t_{PHZ}$	$\overline{OE}$	Y	MAX	5.4	5.9	11.3	10.5	13	6.8
$t_{PLZ}$				4.3	5.4	10.7	10.5	13	6.8

UNIT: ns

Logic Diagram



**FUNCTION TABLE**  
(each 8-bit section)

INPUTS				OUTPUT B
CEAB	LEAB	OEAB	A	
H	X	X	X	Z
X	X	H	X	Z
L	H	L	X	B <sub>0</sub> #
L	L	L	L	L
L	L	L	H	H

† A-to-B data flow is shown; B-to-A flow control is the same except that it uses CEBA, LEBA, and OEBA.

# Output level before the indicated steady-state input conditions were established.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

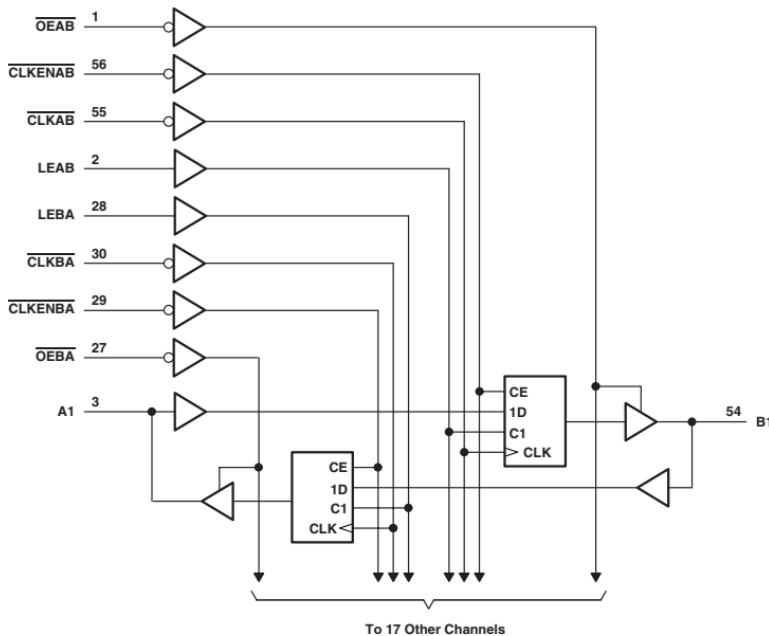
PARAMETER	MAX or MIN	ABT	LVT 3V	LVTH 3V	AC	ACT	LVCH 3V	ALVCH 3V	UNIT
I <sub>CC</sub>	MAX	35	5	5	0.08	0.08	0.02	0.04	mA
I <sub>OH</sub>	MAX	-32	-32	-32	-24	-24	-24	-24	mA
I <sub>OL</sub>	MAX	64	64	64	24	24	24	24	mA

TIMING REQUIREMENTS AND SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	ABT	LVT 3V	LVTH 3V	AC	ACT	LVCH 3V	ALVCH 3V
t <sub>W</sub> Setup time	Pulse duration, LEAB or LEBA low		MIN	4	3.3	3.3	4	7.5	3.3	3.3
	Data before LEAB↑ or LEBA↑, high		MIN	1.5	0.8	0.5	1	2.5	1.1	1.2
	Data before LEAB↑ or LEBA↑, low		MIN	3.5	1.5	0.8	1	2.5	1.1	1.2
	Data before CEAB↑ or CEBA↑, high		MIN	-	0.7	0	-	-	1.1	1.2
	Data before CEAB↑ or CEBA↑, low		MIN	-	1.6	0.6	-	-	1.1	1.2
t <sub>H</sub> Hold time	Data after LEAB↑ or LEBA↑, high		MIN	1.5	0.8	1.5	3	4	1.9	1.3
	Data after LEAB↑ or LEBA↑, low		MIN	2	1.2	1.2	3	4	1.9	1.3
	Data after CEAB↑ or CEBA↑, high		MIN	-	0.8	1.7	-	-	1.9	1.3
	Data after CEAB↑ or CEBA↑, low		MIN	-	1.3	1.6	-	-	1.9	1.3
t <sub>PLH</sub>	A or B	B or A	MAX	3.8	4.6	3.2	8.8	10.5	5.4	4.3
t <sub>PHL</sub>			MAX	5.1	4.6	3.2	9.2	11.6	5.4	4.3
t <sub>PLH</sub>	LE	A or B	MAX	5.2	6.3	3.9	11.5	13.8	6.1	5
t <sub>PZH</sub>	OE	A or B	MAX	5.2	5.8	4.3	9.6	11.4	6.3	5.3
t <sub>PZL</sub>			MAX	7	6.2	4.3	11.3	13.2	6.3	5.3
t <sub>PZH</sub>	OE	A or B	MAX	5.7	6.5	4.7	8.9	11.1	6.3	4.6
t <sub>PZL</sub>			MAX	4.6	5.8	4.4	8.4	9.6	6.3	4.6
t <sub>PZH</sub>	OE	A or B	MAX	6.2	6	4.5	9.8	11.7	6.6	5.6
t <sub>PZL</sub>			MAX	7.8	6.4	4.5	11.5	13.5	6.6	5.6
t <sub>PZH</sub>	OE	A or B	MAX	6.6	6.4	4.9	9.3	11.6	6.6	5.1
t <sub>PZL</sub>			MAX	5.4	5.4	4.7	8.8	10.5	6.6	5.1

UNIT: ns

Logic Diagram



### FUNCTION TABLE

INPUTS					OUTPUT B
CLKENAB	OEAB	LEAB	CLKAB	A	
X	H	X	X	X	Z
X	L	H	X	L	L
X	L	H	X	H	H
H	L	L	X	X	B <sub>0</sub> †
H	L	L	X	X	B <sub>0</sub> ‡
L	L	L	↓	L	L
L	L	L	↓	H	H
L	L	L	H	X	B <sub>0</sub> ‡
L	L	L	L	X	B <sub>0</sub> §

† A-to-B data flow is shown. B-to-A flow is similar but uses OEBA, LEBA, CLKBA and CLKENBA.

‡ Output level before the indicated steady-state input conditions were established.

§ Output level before the indicated steady-state input conditions were established, provided that CLKAB was low before LEAB went low.

### ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

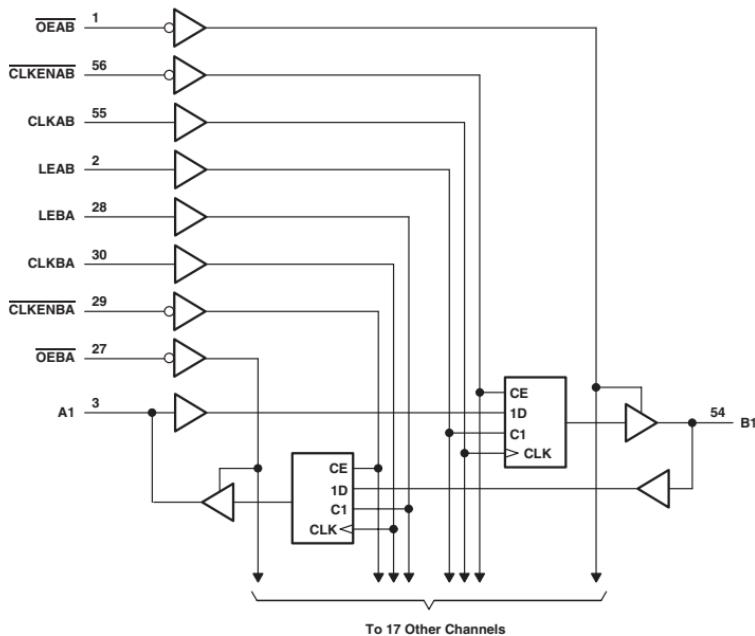
PARAMETER	MAX or MIN	ABT	ALVCH 3V	UNIT
I <sub>CC</sub>	MAX	36	0.04	mA
I <sub>OH</sub>	MAX	-32	-24	mA
I <sub>OL</sub>	MAX	64	24	mA

### TIMING REQUIREMENTS AND SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	ABT	ALVCH 3V
t <sub>max</sub>			MIN	150	150
t <sub>w</sub> Pulse duration	LEAB or LEBA high		MIN	2.5	3.3
	CLKAB or CLKBA high or low		MIN	3	3.3
t <sub>u</sub> Setup time	A before CLKAB ↓ or B before CLKBA ↓		MIN	3	-
	Data before CLK ↑			-	1.2
	A before LEAB ↓ or B before LEBA ↓, CLK high		MIN	2.5	1.1
	A before LEAB ↓ or B before LEBA ↓, CLK low		MIN	2.5	1.5
	CLKEN after CLK ↓			2.5	-
	CLKEN after CLK ↑		MIN	2.5	0.8
t <sub>h</sub> Hold time	A after CLKAB ↓ or B after CLKBA ↓		MIN	0	-
	Data after CLK ↑			-	1.5
	A after LEAB ↓ or B after LEBA ↓, CLK high		MIN	2	1.6
	A after LEAB ↓ or B after LEBA ↓, CLK low		MIN	2	1.3
	CLKEN after CLK ↓			1	-
	CLKEN after CLK ↑		MIN	-	1.4
t <sub>PLH</sub>	A or B	B or A	MAX	4	4
t <sub>PHL</sub>				4.9	4
t <sub>PLH</sub>	LEAB or LEBA	B or A	MAX	5	4.8
t <sub>PHL</sub>				5	4.8
t <sub>PLH</sub>	CLKAB or CLKBA	B or A	MAX	5.3	5.7
t <sub>PHL</sub>				5	5.7
t <sub>PZH</sub>	OEAB	B	MAX	5.1	5.2
t <sub>PZL</sub>				5.4	5.2
t <sub>PZH</sub>	OEAB	B	MAX	6.2	4.4
t <sub>PZL</sub>				5.4	4.4
t <sub>PZH</sub>	OEBA	A	MAX	5.1	5.2
t <sub>PZL</sub>				5.4	5.2
t <sub>PZH</sub>	OEBA	A	MAX	6.2	4.4
t <sub>PZL</sub>				5.4	4.4

UNIT fmax : MHz other : ns

Logic Diagram



FUNCTION TABLE

INPUTS					OUTPUT
CLKENAB	OEAB	LEAB	CLKAB	A	B
X	H	X	X	X	Z
X	L	H	X	L	L
X	L	H	X	H	H
H	L	L	X	X	$B_0\ddagger$
H	L	L	X	X	$B_0\ddagger$
L	L	L	$\uparrow$	L	L
L	L	L	$\uparrow$	H	H
L	L	L	L	X	$B_0\ddagger$
L	L	L	H	X	$B_0\$$

† A-to-B data flow is shown; B-to-A flow is similar but uses  $\overline{OEBA}$ ,  $\overline{LEBA}$ ,  $\overline{CLKBA}$  and  $\overline{CLKENBA}$ .

‡ Output level before the indicated steady-state input conditions were established.

§ Output level before the indicated steady-state input conditions were established, provided that CLKAB was low before LEAB went low.

## ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

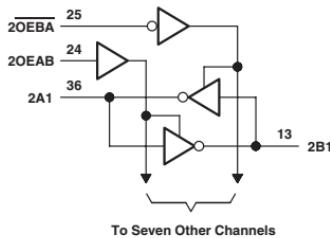
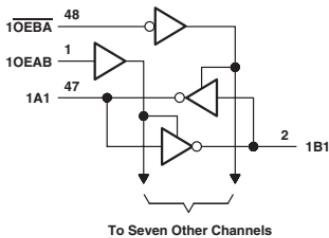
PARAMETER	MAX or MIN	ABT	ALVTH 3V	ALVCH 3V	ALVCHR 3V
$I_{CC}$	MAX	36	5	0.04	0.04
$I_{OH}$	MAX	-32	-32	-24	-12
$I_{OL}$	MAX	64	64	24	12

## TIMING REQUIREMENTS AND SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	ABT	ALVTH 3V	ALVCH 3V	ALVCHR 3V
$t_{max}$			MIN	150	150	150	150
$t_{w}$ Pulse duration	LEAB or LEBA high		MIN	2.5	1.8	3.3	3.3
	CLKAB or CLKBA high or low		MIN	3	2.3	3.3	3.3
$t_{su}$ Setup time	Data before CLK $\uparrow$ high		MIN	4	2.4	2.1	2.1
	Data before CLK $\uparrow$ low		MIN	4	3.8	2.1	2.1
	A before LEAB $\downarrow$ or B before LEBA $\downarrow$ , CLK high		MIN	2.5	1	1.6	1.6
	A before LEAB $\downarrow$ or B before LEBA $\downarrow$ , CLK low		MIN	1	0.6	1.1	1.1
	CLKEN before $\uparrow$ high		MIN	2.5	1.4	1.7	1.7
	CLKEN before $\uparrow$ low		MIN	2.5	1.9	1.7	1.7
$t_h$ Hold time	Data after CLK $\uparrow$ high		MIN	0	0.5	0.8	0.8
	Data after CLK $\uparrow$ low		MIN	0	0.5	0.8	0.8
	A after LEAB $\downarrow$ or B after LEBA $\downarrow$ , CLK high		MIN	2	2	1.4	1.4
	A after LEAB $\downarrow$ or B after LEBA $\downarrow$ , CLK low		MIN	2	2.3	1.7	1.7
	CLKEN after $\uparrow$ high		MIN	0	0.6	0.6	0.6
	CLKEN after $\uparrow$ low		MIN	0	0.5	0.6	0.6
$t_{PLH}$	A or B	B or A	MAX	4	3.9	4.1	4.4
				4.9	3.9	4.1	4.4
$t_{PHL}$	LEAB or LEBA	B or A	MAX	5	4.6	4.7	5.1
				5.2	4.6	4.7	5.1
$t_{PLH}$	CLKAB or CLKBA	B or A	MAX	4.7	4.5	5	5.4
				4.6	4.6	5	5.4
$t_{PZH}$	$\overline{OEAB}$	B	MAX	5.5	4.2	5.2	5.6
				5.8	4.4	5.2	5.6
$t_{PZL}$	$\overline{OEAB}$	B	MAX	6.2	5.3	4.4	4.7
				5.4	4.6	4.4	4.7
$t_{PZL}$	$\overline{OEBA}$	A	MAX	5.5	4.2	5.2	5.6
				5.8	4.4	5.2	5.6
$t_{PZH}$	$\overline{OEBA}$	A	MAX	6.2	5.3	4.4	4.7
				5.4	4.6	4.4	4.7

UNIT  $f_{max}$  : MHz other : ns

Logic Diagram



FUNCTION TABLE

INPUTS		OPERATION
OEBA	OEAB	
L	L	B data to A bus
L	H	B data to A bus, Ā data to B bus
H	L	Isolation
H	H	Ā data to B bus

## ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	AC	ACT	UNIT
I <sub>CC</sub>	MAX	0.08	0.08	mA
I <sub>OH</sub>	MAX	-24	-24	mA
IOL	MAX	24	24	mA

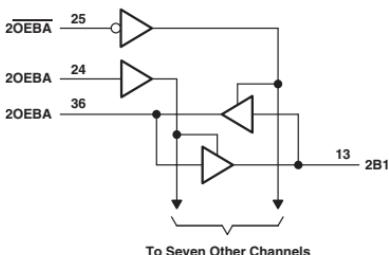
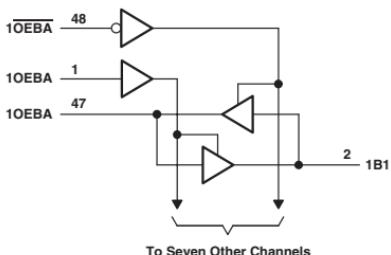
## SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	AC	ACT
t <sub>PLH</sub>	A	B	MAX	6.8	8.5
t <sub>PHL</sub>				8.2	10.5
t <sub>PLH</sub>	B	A	MAX	6.8	8.5
t <sub>PHL</sub>				8.2	10.5
t <sub>PZH</sub>				7.9	9.1
t <sub>PLZ</sub>	OEBA	A	MAX	9.4	10.9
t <sub>PHZ</sub>	OEBA	A	MAX	9.2	11.9
t <sub>PLZ</sub>				8.3	10.6
t <sub>PZH</sub>				7.3	8.9
t <sub>PLZ</sub>	OEAB	B	MAX	9.1	10.5
t <sub>PHZ</sub>	OEAB	B	MAX	9	10.8
t <sub>PLZ</sub>				8	9.6

UNIT: ns

## 16-BIT BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

Logic Diagram

FUNCTION TABLE  
(each 8-bit section)

INPUTS		OPERATION
OEBA	OEAB	
L	L	B data to A bus
L	H	B data to A bus, A data to B bus
H	L	Isolation
H	H	A data to B bus

## ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	ABT	ACT	UNIT
I <sub>CC</sub>	MAX	35	0.08	mA
I <sub>OH</sub>	MAX	-32	-24	mA
I <sub>OL</sub>	MAX	64	24	mA

## SWITCHING CHARACTERISTICS

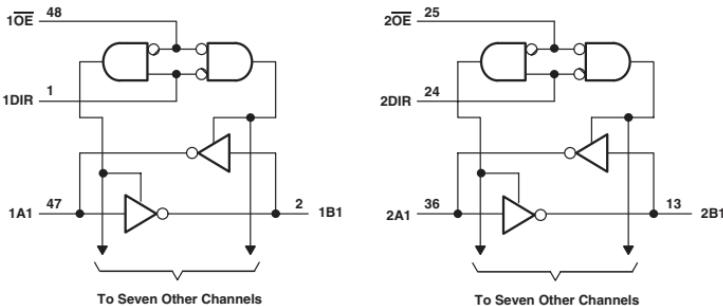
PARAMETER	INPUT	OUTPUT	MAX or MIN	ABT	ACT
t <sub>PLH</sub>				3.6	7.7
t <sub>PHL</sub>	A or B	B or A	MAX	4.3	8.6
t <sub>PZH</sub>				4.9	9.5
t <sub>PZL</sub>				6	11.1
t <sub>PHZ</sub>				6	12
t <sub>PZL</sub>				5.4	10.7
t <sub>PZH</sub>	OEBA	A	MAX	4.9	9.3
t <sub>PZL</sub>	OEAB	B	MAX	6	10.6
t <sub>PHZ</sub>	OEAB	B	MAX	6	10.4
t <sub>PZL</sub>				5.4	9.5

UNIT: ns

# 16640

## 16-BIT BUS TRANSCEIVER WITH 3-STATE OUTPUTS

**Logic Diagram**



**FUNCTION TABLE**  
(each 8-bit section)

INPUTS		OPERATION
$\overline{OE}$	DIR	
L	L	$\bar{B}$ data to A bus
L	H	$\bar{A}$ data to B bus
H	X	Isolation

### ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	ABT	AC	ACT	UNIT
$I_{CC}$	MAX	32	0.08	0.08	mA
$I_{OH}$	MAX	-32	-24	-24	mA
$I_{OL}$	MAX	64	24	24	mA

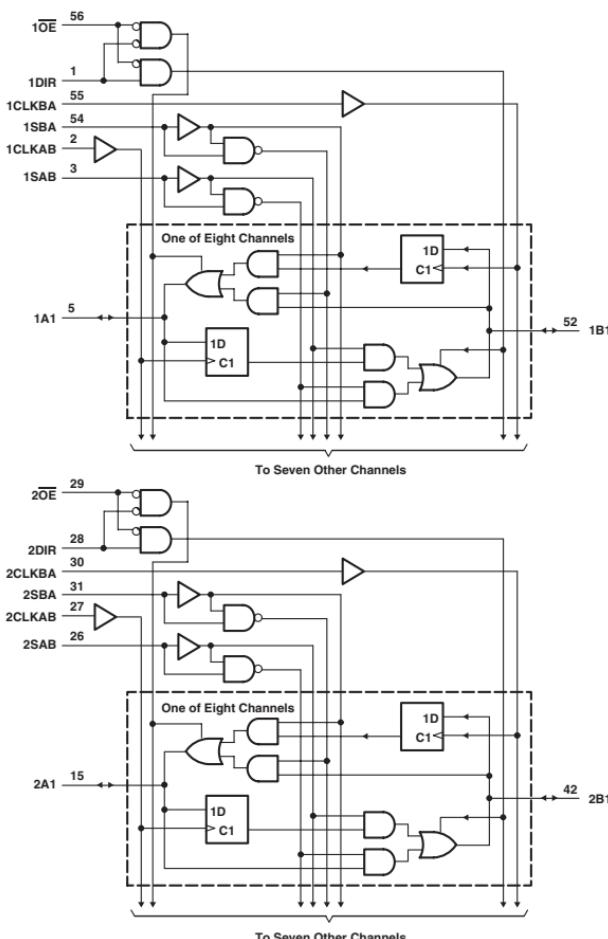
### SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	ABT	AC	ACT
$t_{PLH}$	A or B	B or A	MAX	4.3	7.3	9.1
$t_{PHL}$				3.9	8.6	10.5
$t_{PZH}$	$\overline{OE}$	A or B	MAX	5.5	8	9.8
$t_{PZL}$				6.3	9.9	11.5
$t_{PHZ}$	$\overline{OE}$	A or B	MAX	6.3	9.9	12.5
$t_{PLZ}$				4.2	9	11

UNIT: ns

## 16-BIT BUS TRANSCEIVERS AND REGISTERS WITH 3-STATE OUTPUTS

Logic Diagram



FUNCTION TABLE

INPUTS					DATA I/O		OPERATION OR FUNCTION	
OE	DIR	CLKAB	CLKBA	SAB	A1 THRU A8	B1 THRU B8		
X	X	↑	X	X	Input	Unspecified †	Store A, B unspecified †	
X	X	↑	X	X	Unspecified †	Input	Store B, A unspecified †	
H	X	↑	↑	X	Input	Input	Store A and B data	
H	X	H or L	H or L	X	X	Input	Isolation, hold storage	
L	L	X	X	L	Output	Input	Real-time B data to A bus	
L	L	X	H or L	X	Output	Input	Stored B data to A bus	
L	H	X	X	L	Input	Output	Real-time A data to B bus	
L	H	H or L	X	H	Input	Output	Stored A data to B bus	

† The data output functions may be enabled or disabled by various signals at the OE and DIR inputs. Data input functions are always enabled; i.e., data at the bus pins will be stored on every low-to-high transition of the clock inputs.

## ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	ABT	LVT 3V	LVTH 3V	AC	ACT	LVC 3V	LVCH 3V	ALVCH 3V	AVC 3V	UNIT
I <sub>CC</sub>	MAX	32	5	5	0.08	0.08	0.02	0.02	0.04	0.04	mA
I <sub>OH</sub>	MAX	-32	-32	-32	-24	-24	-24	-24	-24	-12	mA
I <sub>OL</sub>	MAX	64	64	64	24	24	24	24	24	12	mA

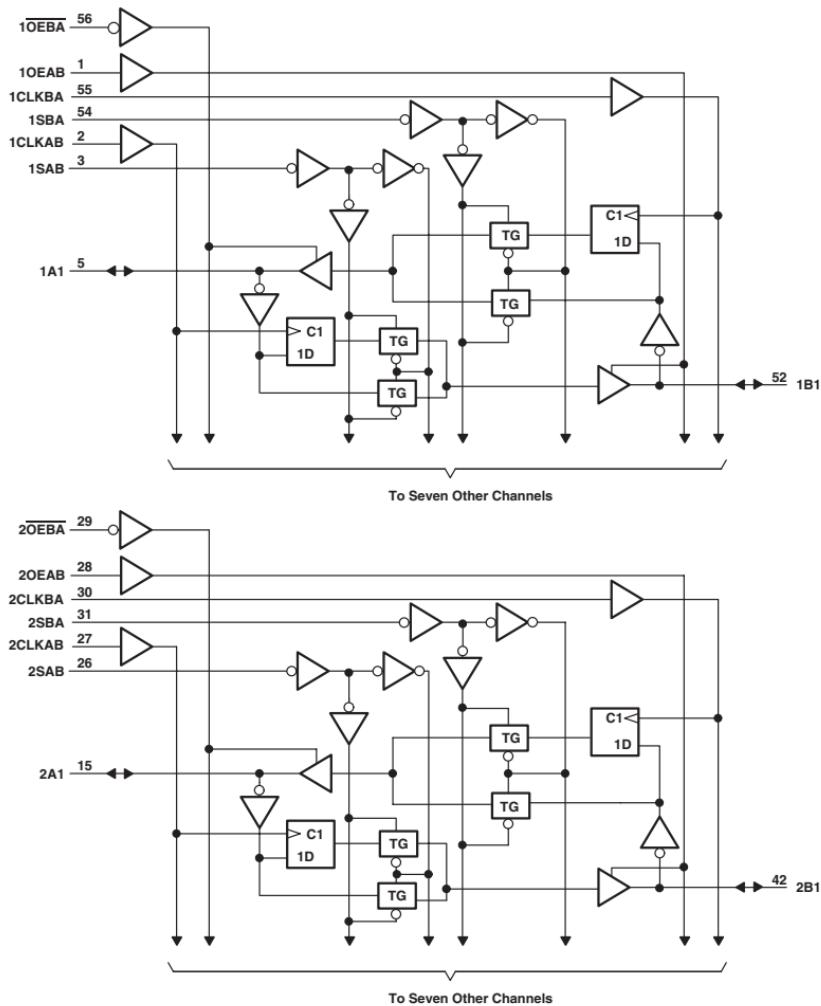
## TIMING REQUIREMENTS AND SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	ABT	LVT 3V	LVTH 3V	AC	ACT	LVC 3V	LVCH 3V
f <sub>max</sub>			MIN	125	150	150	75	90	150	150
t <sub>W</sub> Pulse duration	CLKAB or CLKBA high or low		MIN	4.3	3.3	3.3	6.5	5.5	3.3	3.3
t <sub>WS</sub> Setup time	A or B before CLKAB ↑ or CLKBA ↑, data high		MIN	3	1.3	1.2	5	4	2.7	2.9
	A or B before CLKAB ↑ or CLKBA ↑, data low		MIN	3	2.4	2	5	6	2.7	2.9
t <sub>H</sub> Hold time	A or B after CLKAB ↑ or CLKBA ↑, data high		MIN	0	0.5	0.5	1	1.5	0.3	0.3
	A or B after CLKAB ↑ or CLKBA ↑, data low		MIN	0	0.5	0.5	1	1.5	0.3	0.3
t <sub>PLH</sub>	CLKAB or CLKBA	B or A	MAX	4.9	5.7	4.2	12.1	12.2	6	6.7
t <sub>PHL</sub>				4.7	5.7	4.2	11.9	12.3	6	6.7
t <sub>PLH</sub>	A or B	B or A	MAX	3.9	4.7	3.4	9.5	10.6	5.2	5.7
t <sub>PHL</sub>				4.6	4.7	3.4	9.7	11.4	5.2	5.7
t <sub>PLH</sub>	SAB or SBA	B or A	MAX	5	6.2	4.5	12.5	15.6	6.1	7.7
t <sub>PHL</sub>				5	6.2	4.5	13.1	16.7	6.1	7.7
t <sub>PZH</sub>	OE	A or B	MAX	5.5	5.4	4.3	10.5	11.9	6.9	6.9
t <sub>PZL</sub>				5.7	5.6	4.3	12.2	13.5	6.9	6.9
t <sub>PZH</sub>	OE	A or B	MAX	5.4	6.5	5.6	8.9	10.2	6.9	6.9
t <sub>PZL</sub>				4.5	5.8	5.4	8.6	9.9	6.9	6.9
t <sub>PZH</sub>	DIR	A or B	MAX	5.4	5.7	4.4	10.9	15.2	7.2	7.2
t <sub>PZL</sub>				5.6	5.8	4.4	12.2	13.1	7.2	7.2
t <sub>PZH</sub>	DIR	A or B	MAX	6.7	7.2	5.7	9.4	10.8	7	7
t <sub>PZL</sub>				5.9	6.6	5.2	8.8	10.4	7	7

PARAMETER	INPUT	OUTPUT	MAX or MIN	ALVCH 3V	AVC 3V
f <sub>max</sub>			MIN	150	350
t <sub>W</sub> Pulse duration	CLKAB or CLKBA high or low		MIN	3.3	1.4
t <sub>WS</sub> Setup time	A or B before CLKAB ↑ or CLKBA ↑, data high		MIN	1.4	0.8
	A or B before CLKAB ↑ or CLKBA ↑, data low		MIN	1.4	0.8
t <sub>H</sub> Hold time	A or B after CLKAB ↑ or CLKBA ↑, data high		MIN	0.7	0.6
	A or B after CLKAB ↑ or CLKBA ↑, data low		MIN	0.7	0.6
t <sub>PLH</sub>	CLKAB or CLKBA	B or A	MAX	4.5	3.3
t <sub>PHL</sub>				4.5	3.3
t <sub>PLH</sub>	A or B	B or A	MAX	3.9	2.6
t <sub>PHL</sub>				3.9	2.6
t <sub>PLH</sub>	SAB or SBA	B or A	MAX	5.3	4
t <sub>PHL</sub>				5.3	4
t <sub>PZH</sub>	OE	A or B	MAX	5.1	4
t <sub>PZL</sub>				5.1	4
t <sub>PZH</sub>	OE	A or B	MAX	4.7	4.2
t <sub>PZL</sub>				4.7	4.2
t <sub>PZH</sub>	DIR	A or B	MAX	5.1	4.3
t <sub>PZL</sub>				5.1	4.3
t <sub>PZH</sub>	DIR	A or B	MAX	5.3	4.3
t <sub>PZL</sub>				5.3	4.3

UNIT f<sub>max</sub> : MHz other : ns

Logic Diagram



FUNCTION TABLE

INPUTS						DATA I/O †		OPERATION OR FUNCTION	
OEAB	OEBA	CLKAB	CLKBA	SAB	SBA	A1-A8	B1-B8		
L	H	L	L	X	X	Input	Input	Isolation	
L	H	↑	↑	X	X	Input	Input	Store A and B data	
X	H	↑	L	X	X	Input	Unspecified‡	Store A, hold B	
H	H	↑	↑	X‡	X	Input	Output	Store A in both registers	
L	X	L	↑	X	X	Unspecified‡	Input	Hold A, store B	
L	L	↑	↑	X	X‡	Output	Input	Store B in both registers	
L	L	X	X	X	L	Output	Input	Real-time B data to A bus	
L	L	X	L	X	H	Output	Input	Store B data to A bus	
H	H	X	X	L	X	Input	Output	Real-time A data to B bus	
H	H	L	X	H	X	Input	Output	Store A data to B bus	
H	L	L	L	H	H	Output	Output	Store A data to B bus and Store B data to A bus	

† The data-output functions may be enabled or disabled by a variety of level combinations at OEAB or OEBA. Data-input functions are always enabled; i.e., data at the bus terminals is stored on every low-to-high transition of the clock inputs.

‡ Select control = L; clocks can occur simultaneously.  
Select control = H; clocks must be staggered to load both registers.

## ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	ACT	UNIT
I <sub>CC</sub>	MAX	0.08	mA
I <sub>OH</sub>	MAX	-24	mA
I <sub>OL</sub>	MAX	24	mA

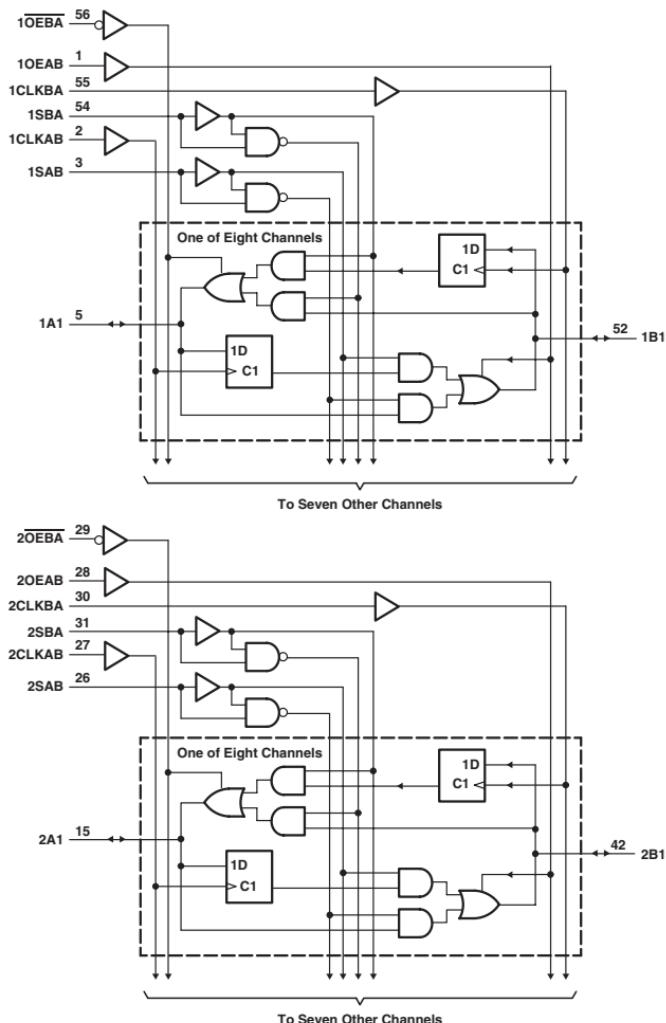
## TIMING REQUIREMENTS AND SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	ACT
f <sub>max</sub>			MIN	90
t <sub>w</sub> Pulse duration	CLKAB or CLKBA high or low		MIN	5.5
t <sub>w</sub> Setup time	A before CLKAB ↑ or B before CLKBA ↑		MIN	5.3
t <sub>h</sub> Hold time	A after CLKAB ↑ or B after CLKBA ↑		MIN	1
t <sub>PLH</sub>	A or B	B or A	MAX	11.3
t <sub>PHL</sub>				11.9
t <sub>PLH</sub>	CLKAB or CLKBA	A or B	MAX	13.7
t <sub>PHL</sub>				13.6
t <sub>PLH</sub>	SAB or SBA	A or B	MAX	17.3
t <sub>PHL</sub>				17.8
t <sub>PZH</sub>	OEBA	A	MAX	12.3
t <sub>PZL</sub>				13.9
t <sub>PZH</sub>	OEBA	A	MAX	10.6
t <sub>PZL</sub>				10.8
t <sub>PZH</sub>	OEAB	B	MAX	11.9
t <sub>PZL</sub>				13.5
t <sub>PHZ</sub>	OEAB	B	MAX	11.4
t <sub>PZL</sub>				11.6

UNIT f<sub>max</sub> : MHz other : ns

## 16-BIT BUS TRANSCEIVERS AND REGISTERS WITH 3-STATE OUTPUTS

Logic Diagram



FUNCTION TABLE

INPUTS						DATA I/O†		OPERATION OR FUNCTION		
OEAB	OEBA	CLKAB	CLKBA	SAB	SBA	A1 THRU A8	B1 THRU B8			
L	H	H or L	H or L	X	X	Input	Input	Isolation		
L	H	↑	X	X	X	Input	Input	Store A and B data		
X	H	↑	H or L	X	X	Input	Unspecified ‡	Store A, hold B		
H	H	↑	↑	X‡	X	Input	Output	Store A in both registers		
L	L	X	H or L	↑	X	Unspecified ‡	Input	Hold A, store B		
L	L	X	X	X	X‡	Output	Input	Store B in both registers		
L	L	X	H or L	X	L	Output	Input	Real-time B data to A bus		
L	L	X	X	X	H	Output	Input	Stored A data to A bus		
H	H	X	X	X	X	Input	Output	Real-time A data to B bus		
H	H	H or L	X	H	X	Input	Output	Store A data to B bus		
H	L	H or L	H or L	H	H	Output	Output	Stored A data to B bus and stored B data A bus		

† The data output functions may be enabled or disabled by a variety of level combinations at the OEAB or OEBA inputs. Data input functions are always enabled; i.e., data at the bus pins is stored on every low-to-high transition of the clock inputs.

‡ Select control = L; clocks can occur simultaneously.

Select control = H; clocks must be staggered in order to load both registers.

#### ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

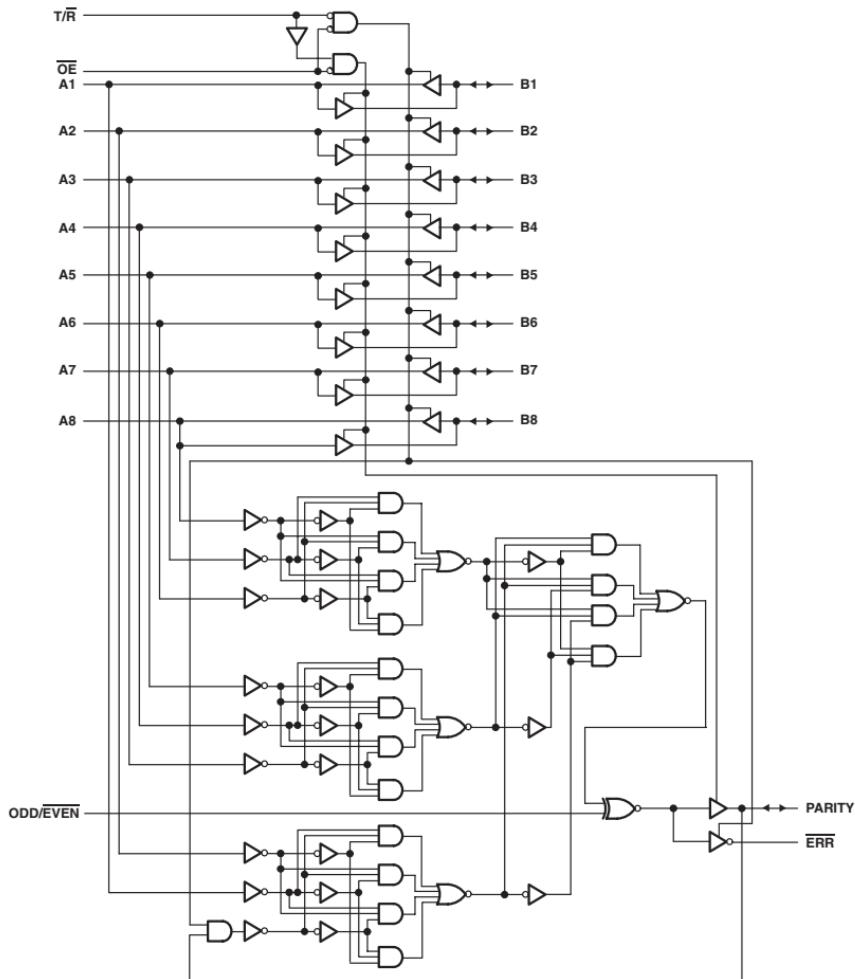
PARAMETER	MAX or MIN	ABT	LVTH 3V	AC	ACT	LVCH 3V	UNIT
I <sub>CC</sub>	MAX	32	5	0.08	0.08	0.02	mA
I <sub>OH</sub>	MAX	-32	-32	-24	-24	-24	mA
I <sub>OL</sub>	MAX	64	64	24	24	24	mA

#### TIMING REQUIREMENTS AND SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	ABT	LVTH 3V	AC	ACT	LVCH 3V
f <sub>max</sub>			MIN	125	150	95	90	150
t <sub>w</sub> Pulse duration	CLKAB or CLKBA high or low		MIN	4.3	3.3	5	5.5	3.3
t <sub>su</sub> Setup time	A before CLKAB ↑ or B before CLKBA ↑, high		MIN	3	1.2	4.5	4.5	3
	A before CLKAB ↑ or B before CLKBA ↑, low		MIN	3	2	4.5	4.5	3
t <sub>h</sub> Hold time	A after CLKAB ↑ or B after CLKBA ↑, high		MIN	0	0.5	0	1	0.2
	A after CLKAB ↑ or B after CLKBA ↑, low		MIN	0	0.5	0	1	0.2
t <sub>PLH</sub>	CLKAB or CLKBA	A or B	MAX	4.9	4.2	12.2	12.3	6.4
t <sub>PHL</sub>				4.7	4.2	12.3	12.3	6.4
t <sub>PLH</sub>	A or B	B or A	MAX	3.9	3.4	9.9	10.5	6.3
t <sub>PHL</sub>				4.6	3.4	10.2	11.6	6.3
t <sub>PLH</sub>	SAB or SBA	A or B	MAX	5	4.5	13.8	16	7.4
t <sub>PHL</sub>				5	4.5	13.8	16.9	7.4
t <sub>PZH</sub>	OEBA	A	MAX	5	4.3	10.7	11.7	6.3
t <sub>PZL</sub>				5.3	4.3	13.2	13.4	6.3
t <sub>PHZ</sub>	OEBA	A	MAX	4.9	5.6	8.8	9.5	6.2
t <sub>PZL</sub>				4	5.4	8.7	9.2	6.2
t <sub>PZH</sub>	OEAB	B	MAX	4.2	4.2	10.5	10.8	6.3
t <sub>PZL</sub>				4.6	4.2	13	12.4	6.3
t <sub>PHZ</sub>	OEAB	B	MAX	5.9	5.5	8	10.5	6.2
t <sub>PZL</sub>				5.2	5.5	7.8	9.9	6.2

UNIT f<sub>max</sub> : MHz other : ns

Logic Diagram



**FUNCTION TABLE**  
(each 8-bit section)

NUMBER OF A OR B INPUTS THAT ARE HIGH	INPUTS			INPUT/OUTPUT PARITY	OUTPUTS	
	$\overline{OE}$	T/R	ODD/EVEN		$\overline{ERR}$	OUTPUT MODE
0, 2, 4, 6, 8	L	H	H	H	Z	Transmit
	L	H	L	L	Z	Transmit
	L	L	H	H	H	Receive
	L	L	H	L	L	Receive
	L	L	L	H	L	Receive
	L	L	L	L	H	Receive
1, 3, 5, 7	L	H	H	L	Z	Transmit
	L	H	L	H	Z	Transmit
	L	L	H	H	L	Receive
	L	L	H	L	H	Receive
	L	L	L	H	H	Receive
	L	L	L	L	L	Receive
Don't care	H	X	X	Z	Z	Z

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

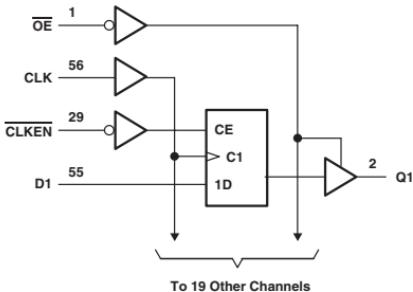
PARAMETER	MAX or MIN	ABT	ACT	UNIT
$I_{CC}$	MAX	36	0.08	mA
$I_{OH}$	MAX	-32	-24	mA
$I_{OL}$	MAX	64	24	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	ABT	ACT
$t_{PLH}$	A or B	B or A	MAX	4.1	10.7
$t_{PHL}$				4.3	10.6
$t_{PLH}$	A or B	PARITY	MAX	6.7	14.3
$t_{PHL}$				6.1	14.3
$t_{PLH}$	ODD / EVEN	PARITY, $\overline{ERR}$	MAX	6.7	13.7
$t_{PHL}$				6.1	14.1
$t_{PLH}$	B	$\overline{ERR}$	MAX	6.7	14.6
$t_{PHL}$				6.1	14.7
$t_{PLH}$	PARITY	$\overline{ERR}$	MAX	6.7	13.8
$t_{PHL}$				6.1	14.2
$t_{PZH}$	$\overline{OE}$	A or B	MAX	5.6	11.3
$t_{PZL}$				6	13
$t_{PZH}$	$\overline{OE}$	A or B	MAX	5.4	11.2
$t_{PZL}$				4.3	10.5
$t_{PZH}$	$\overline{OE}$	PARITY, $\overline{ERR}$	MAX	5.6	11.3
$t_{PZL}$				6	13
$t_{PZH}$	$\overline{OE}$	PARITY, $\overline{ERR}$	MAX	5.4	11.2
$t_{PZL}$				4.3	10.5

UNIT: ns

## 20-BIT FLIP-FLOP WITH 3-STATE OUTPUTS

FUNCTION TABLE  
(each flip-flop)

INPUTS				OUTPUT
OE	CLKEN	CLK	D	Q
L	H	X	H	Q <sub>O</sub>
L	L	↑	H	H
L	L	↑	L	L
L	L	L	X	Q <sub>O</sub>
H	X	X	X	Z

## ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	ALVCH 3V	UNIT
I <sub>CC</sub>	MAX	0.04	mA
I <sub>OH</sub>	MAX	-24	mA
I <sub>OL</sub>	MAX	24	mA

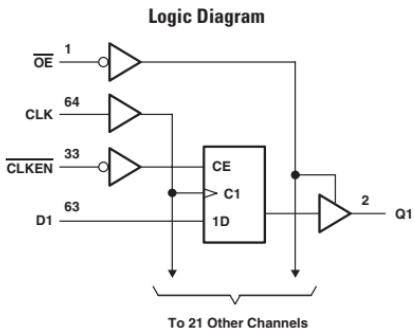
## TIMING REQUIREMENTS AND SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	ALVCH 3V
t <sub>max</sub>			MIN	150
t <sub>w</sub> Pulse duration	CLK high or low		MIN	3.3
t <sub>su</sub> Setup time	Data before CLK ↑		MIN	3.1
	CLKEN before CLK ↑		MIN	2.7
t <sub>h</sub> Hold time	Data after CLK ↑		MIN	0
	CLKEN after CLK ↑		MIN	0
t <sub>PLH</sub>	CLK	Q	MAX	4.3
t <sub>PHL</sub>				4.3
t <sub>PZH</sub>	OE	Q	MAX	4.8
t <sub>PZL</sub>				4.8
t <sub>PHZ</sub>	OE	Q	MAX	4.4
t <sub>PZL</sub>				4.4

UNIT fmax : MHz other : ns

# 16722

## 22-BIT FLIP-FLOP WITH 3-STATE OUTPUTS



**FUNCTION TABLE**  
(each flip-flop)

INPUTS				OUTPUT
$\overline{OE}$	CLKEN	CLK	D	Q
L	H	X	X	Q <sub>0</sub>
L	L	↑	H	H
L	L	↑	L	L
L	L	L or H	X	Q <sub>0</sub>
H	X	X	X	Z

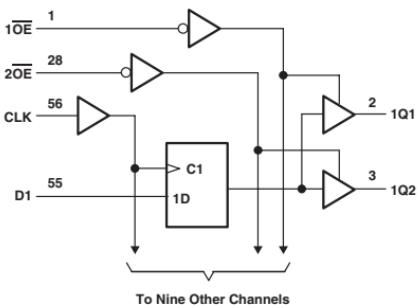
### ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	AVC 3V	UNIT
I <sub>CC</sub>	MAX	0.04	mA
I <sub>OH</sub>	MAX	-12	mA
I <sub>OL</sub>	MAX	12	mA

### TIMING REQUIREMENTS AND SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	AVC 3V
f <sub>max</sub>			MIN	150
t <sub>W</sub> Pulse duration	CLK high or low		MIN	2.8
t <sub>SU</sub> Setup time	Data before CLK ↑		MIN	2.5
	CLKEN before CLK ↑		MIN	1.4
t <sub>H</sub> Hold time	Data after CLK ↑		MIN	0
	CLKEN after CLK ↑		MIN	1.2
t <sub>PLH</sub>	CLK	Q	MAX	2.6
t <sub>PHL</sub>			MAX	2.6
t <sub>PZH</sub>	$\overline{OE}$	Q	MAX	4.3
t <sub>PZL</sub>			MAX	4.3
t <sub>PLZ</sub>	$\overline{OE}$	Q	MAX	3.4
t <sub>PLZ</sub>			MAX	3.4

UNIT f<sub>max</sub> : MHz other : ns

**10-BIT EDGE-TRIGGERED D-TYPE FLIP-FLOPS  
WITH DUAL OUTPUTS**
**Logic Diagram**

To Nine Other Channels

**FUNCTION TABLE**  
(each flip-flop)

INPUTS			OUTPUT
$\overline{OE}_n^\dagger$	CLK	D	$Q_n^\dagger$
L	↑	H	H
L	↑	L	L
L	L	X	$Q_0$
H	X	X	Z

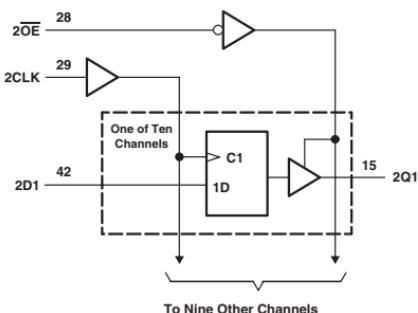
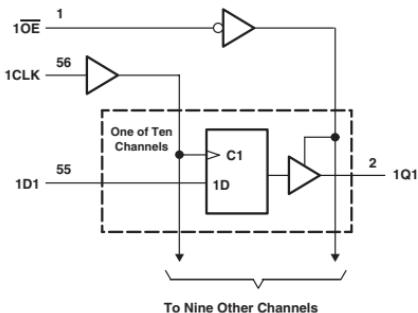
<sup>†</sup>n = 1, 2**ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS**

PARAMETER	MAX or MIN	ALVCH 3V	UNIT
$I_{CC}$	MAX	0.04	mA
$I_{OH}$	MAX	-24	mA
$I_{OL}$	MAX	24	mA

**TIMING REQUIREMENTS AND SWITCHING CHARACTERISTICS**

PARAMETER	INPUT	OUTPUT	MAX or MIN	ALVCH 3V
$t_{max}$			MIN	150
$t_w$ Pulse duration	CLK high or low		MIN	3.3
$t_{su}$ Setup time	Data before CLK ↑		MIN	1.4
$t_h$ Hold time	Data after CLK ↑		MIN	1
$t_{PLH}$	CLK	Q	MAX	4.8
$t_{PHL}$				4.8
$t_{PZH}$	$\overline{OE}$	Q	MAX	5
$t_{PZL}$				5
$t_{PHZ}$	$\overline{OE}$	Q	MAX	4.5
$t_{PLZ}$				4.5

UNIT fmax : MHz other : ns

**16821**
**20-BIT BUS INTERFACE FLIP-FLOPS  
WITH 3-STATE OUTPUTS**
**Logic Diagram**
**FUNCTION TABLE**  
(each flip-flop)

INPUTS	OUTPUT		
$\overline{OE}$	CLK	D	Q
L	↑	H	H
L	↑	L	L
L	L	X	$Q_0$
H	X	X	Z

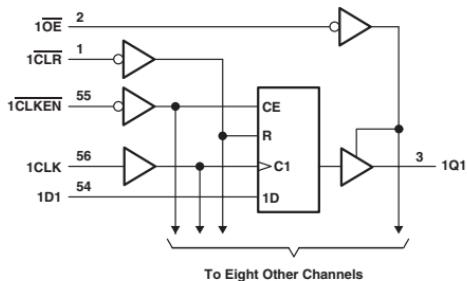
**ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS**

PARAMETER	MAX or MIN	ABT	ALVTH 3V	ACT	ALVCH 3V	UNIT
$I_{CC}$	MAX	89	5	0.08	0.04	mA
$I_{OH}$	MAX	-32	-32	-24	-24	mA
$I_{OL}$	MAX	64	64	24	24	mA

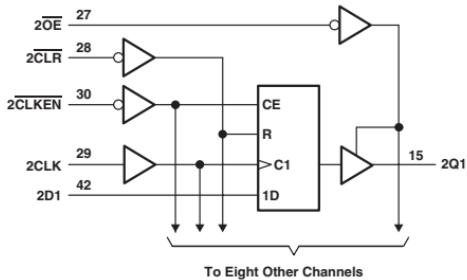
**TIMING REQUIREMENTS AND SWITCHING CHARACTERISTICS**

PARAMETER	INPUT	OUTPUT	MAX or MIN	ABT	ALVTH 3V	ACT	ALVCH 3V
$t_{max}$			MIN	150	150	70	150
$t_{W}$ Pulse duration	CLK high or low		MIN	3.3	1.5	7	3.3
$t_{WS}$ Setup time	Data before CLK ↑ , low		MIN	1.8	1.5	7.5	3.4
	Data before CLK ↑ , high		MIN	1.8	1.5	7.5	3.4
$t_H$ Hold time	Data after CLK ↑ , high		MIN	1.3	1	0.5	0
	Data after CLK ↑ , low		MIN	1.3	1	0.5	0
$t_{PLH}$	CLK	Q	MAX	6.1	3.5	13.4	4.5
$t_{PHL}$				5.4	3.5	14	4.5
$t_{PZH}$	$\overline{OE}$	Q	MAX	5.7	4.1	11.9	5.1
$t_{PZL}$				5.6	3.6	14.7	5.1
$t_{PHZ}$	$\overline{OE}$	Q	MAX	6.5	4.8	10.7	4.6
$t_{PLZ}$				7.1	4.8	10	4.6

UNIT  $f_{max}$  : MHz other : ns

**18-BIT EDGE-TRIGGERED  
D-TYPE FLIP-FLOPS  
WITH DUAL OUTPUTS**
**Logic Diagram**

To Eight Other Channels



To Eight Other Channels

**FUNCTION TABLE**  
(each 9-bit flip-flop)

INPUTS				OUTPUT
OE	CLR	CLKEN	CLK	Q
L	L	X	X	X
L	H	L	↑	H
L	H	L	↑	L
L	H	L	L	X
L	H	H	X	X
H	X	X	X	Z

**ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS**

PARAMETER	MAX or MIN	ABT	ABTH	AC	ACT	ALVCH 3V	UNIT
I <sub>CC</sub>	MAX	80	80	0.08	0.08	0.04	mA
I <sub>OH</sub>	MAX	-32	-32	-24	-24	-24	mA
I <sub>OL</sub>	MAX	64	64	24	24	24	mA

**TIMING REQUIREMENTS AND SWITCHING CHARACTERISTICS**

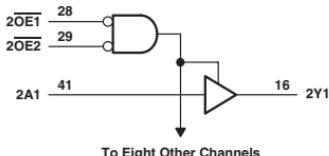
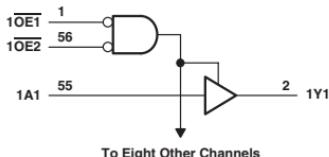
PARAMETER	INPUT	OUTPUT	MAX or MIN	ABT	ABTH	AC	ACT	ALVCH 3V
f <sub>max</sub>			MIN	150	150	115	90	150
t <sub>w</sub> Pulse duration	CLR low		MIN	3.3	3.3	3.3	3.3	3.3
	CLK high or low		MIN	3.3	3.3	4.4	5.5	3.3
t <sub>su</sub> Setup time	CLR inactive		MIN	1.6	1.6	0.6	0.5	0.8
	Data high before CLK ↑		MIN	1.7	1.7	5	7	1
	Data low before CLK ↑		MIN	1.7	1.7	5	7	1.3
	CLK low before CLK ↑		MIN	2.8	2.8	4.2	3.5	1.5
t <sub>h</sub> Hold time	Data high after CLK ↑		MIN	1.2	1.2	1.3	0.5	0.8
	Data low after CLK ↑		MIN	1.2	1.2	1.3	0.5	0.5
	CLKEN low after CLK ↑		MIN	0.6	0.6	1.4	2.5	0.4
t <sub>PLH</sub>	CLK	Q	MAX	6.8	6.8	12	12.1	4.5
t <sub>PHL</sub>			6	6	12.7	12.9	4.5	
t <sub>PLH</sub>	CLR	Q	MAX	-	-	-	-	4.6
t <sub>PHL</sub>			6.1	6.7	11	12.5	4.6	
t <sub>PZH</sub>	OE	Q	MAX	4.9	4.9	9.7	10.7	4.8
t <sub>PZL</sub>			5.5	5.5	11.8	12.8	4.8	
t <sub>PHZ</sub>	OE	Q	MAX	6.1	6.1	9.3	10.3	4.5
t <sub>PZL</sub>			8.7	8.7	8.6	9.4	4.5	

UNIT: f<sub>max</sub>: MHz other: ns

# 16825

## Logic Diagram

### 18-BIT BUS BUFFERS/DRIVERS WITH 3-STATE OUTPUTS



**FUNCTION TABLE**  
(each 9-bit section)

INPUTS			OUTPUT
OE1	OE2	A	Y
L	L	L	L
L	L	H	H
H	X	X	Z
X	H	X	Z

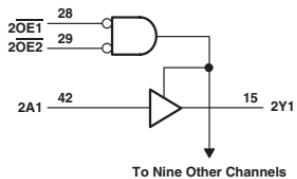
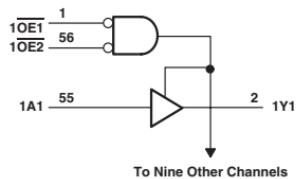
ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	ABT	ACT	ALVCH 3V	UNIT
I <sub>CC</sub>	MAX	32	0.08	0.04	mA
I <sub>OH</sub>	MAX	-32	-24	-24	mA
I <sub>OL</sub>	MAX	64	24	24	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	ABT	ACT	ALVCH 3V
t <sub>PLH</sub>	A	Y	MAX	3.9	10.5	3.4
t <sub>PHL</sub>				4.4	10.3	3.4
t <sub>PZH</sub>	OE	Y	MAX	6.1	11	4.7
t <sub>PZL</sub>				6	13.2	4.7
t <sub>PHZ</sub>	OE	Y	MAX	6.9	11.5	4.5
t <sub>PZL</sub>				6.6	10.6	4.5

UNIT: ns

**20-BIT BUS BUFFERS/DRIVERS  
WITH 3-STATE OUTPUTS****Logic Diagram**

**FUNCTION TABLE**  
(each 10-bit section)

INPUTS			OUTPUT
OE1	OE2	A	Y
L	L	L	L
L	L	H	H
H	X	X	Z
X	H	X	Z

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	ABT	ALVTH 3V	ACT	ALVCH 3V	AVC 3V	UNIT
I <sub>CC</sub>	MAX	32	6	0.08	0.04	0.04	mA
I <sub>OH</sub>	MAX	-32	-32	-24	-24	-12	mA
I <sub>OL</sub>	MAX	64	64	24	24	12	mA

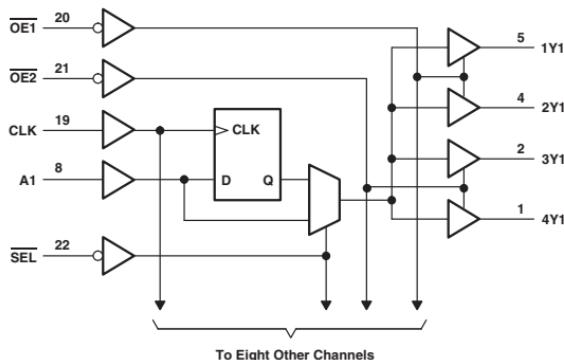
SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	ABT	ALVTH 3V	ACT	ALVCH 3V	AVC 3V
t <sub>PLH</sub>	A	Y	MAX	3.4	3	11	3.4	1.7
t <sub>PHL</sub>				4.2	2.8	10.8	3.4	1.7
t <sub>PZH</sub>	OE	Y	MAX	5.6	3.9	11.7	4.7	5.1
t <sub>PZL</sub>				5.5	3.4	14	4.7	5.1
t <sub>PHZ</sub>	OE	Y	MAX	6.6	5.8	12.4	4.5	4.7
t <sub>PZL</sub>				6.1	4.6	11.5	4.5	4.7

UNIT: ns

## 1-TO-4 ADDRESS REGISTER/DRIVER WITH 3-STATE OUTPUTS

Logic Diagram



FUNCTION TABLE

OE	INPUTS			OUTPUT Y
	SEL	CLK	A	
H	X	X	X	Z
L	H	X	L	L
L	H	X	H	H
L	L	↑	L	L
L	L	↑	H	H

## ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	ALVCH 3V	UNIT
I <sub>CC</sub>	MAX	0.04	mA
I <sub>OH</sub>	MAX	-24	mA
I <sub>OL</sub>	MAX	24	mA

## TIMING REQUIREMENTS AND SWITCHING CHARACTERISTICS

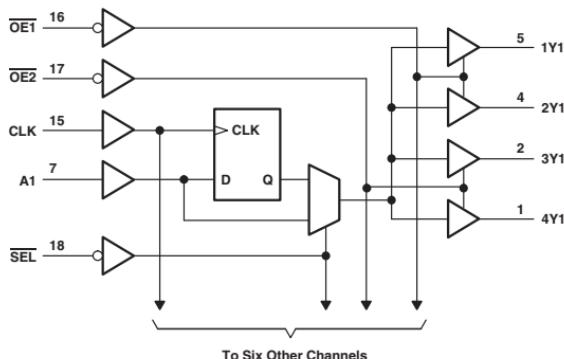
PARAMETER	INPUT	OUTPUT	MAX or MIN	ALVCH 3V
t <sub>max</sub>			MIN	150
t <sub>w</sub> Pulse duration	CLK high or low		MIN	3.3
t <sub>su</sub> Setup time	A data before CLK ↑		MIN	1.6
t <sub>h</sub> Hold time	A data after CLK ↑		MIN	1.1
t <sub>PLH</sub>	A	Y	MAX	3.6
t <sub>PHL</sub>				3.6
t <sub>PLH</sub>	CLK	Y	MAX	3.9
t <sub>PHL</sub>				3.9
t <sub>PLH</sub>	SEL	Y	MAX	4.4
t <sub>PHL</sub>				4.4
t <sub>PHZ</sub>	OE	Y	MAX	4.3
t <sub>PZL</sub>				4.3
t <sub>PHZ</sub>	OE	Y	MAX	4.5
t <sub>PZL</sub>				4.5

UNIT: fmax : MHz other : ns

■ : OBSOLETE or NOT RECOMMENDED NEW DESIGNS

## 1-TO-4 ADDRESS REGISTER/DRIVER WITH 3-STATE OUTPUTS

Logic Diagram



FUNCTION TABLE

INPUTS				OUTPUT
OE	SEL	CLK	A	Y
H	X	X	X	Z
L	H	X	L	L
L	H	X	H	H
L	L	↑	L	L
L	L	↑	H	H

## ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	ALVCH 3V	UNIT
Icc	MAX	0.04	mA
IoH	MAX	-24	mA
IoL	MAX	24	mA

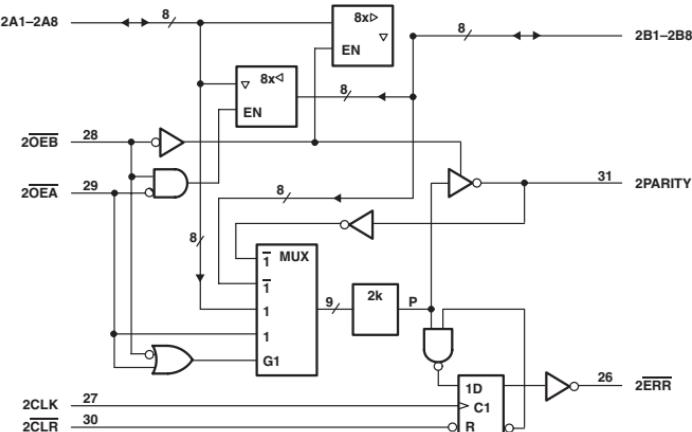
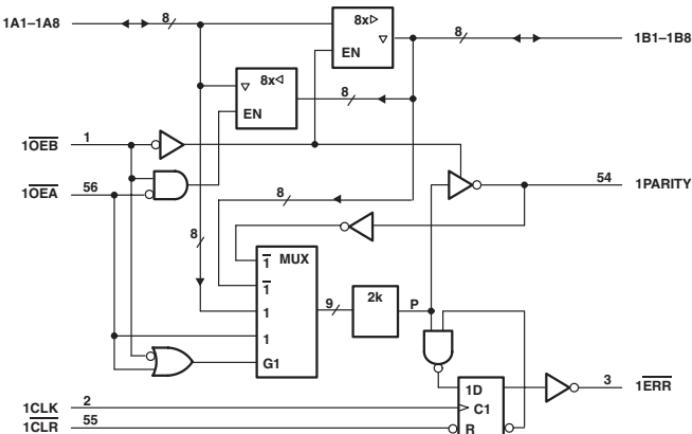
## TIMING REQUIREMENTS AND SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	ALVCH 3V
tmax			MIN	150
tw Pulse duration	CLK high or low		MIN	3.3
ts Setup time	A data before CLK ↑		MIN	1.6
th Hold time	A data after CLK ↑		MIN	1.1
tPLH	A	Y	MAX	3.6
tPHL			MAX	3.6
tPLH	CLK	Y	MAX	3.9
tPHL			MAX	3.9
tPLH	SEL	Y	MAX	4.4
tPHL			MAX	4.4
tPZH	OE	Y	MAX	4.3
tPZL			MAX	4.3
tPHZ	OE	Y	MAX	4.5
tPZL			MAX	4.5

UNIT fmax : MHz other : ns

## DUAL 8-BIT TO 9-BIT PARITY BUS TRANSCEIVERS

Logic Diagram



FUNCTION TABLE

INPUTS						OUTPUT AND I/O				FUNCTION
OEB	OE <sub>A</sub>	CLR	CLK	A <sub>I</sub> Σ OF H	B <sup>†</sup> Σ OF H	A	B	PARITY	ERR <sup>‡</sup>	
L	H	X	X	Odd Even	NA	NA	A	L	NA	A data to B bus and generate parity
H	L	H	↑	NA	Odd Even	B	NA	NA	H L	B data to A bus and check parity
X	X	L	X	X	X	X	NA	NA	H	Check error flag register
H	H	H	↑	No ↑ L	X	Z	Z	Z	H L	Isolation§
H	H	H	↑	Odd Even	X	Z	Z	Z	H L	
L	L	X	X	Odd Even	NA	NA	A	H L	NA	A data to B bus and generate inverted parity

NA = not applicable. NC = no change. X = don't care.

† Output states shown assume ERR was previously high.

‡ Summation of high-level inputs includes PARITY along with Bi inputs.

§ In this mode, ERR (when clocked) shows inverted parity of the A bus.

ERROR-FLAG FUNCTION TABLE

INPUTS		INTERNAL OUTPUT TO DEVICE		OUTPUT PRE-STATE	OUTPUT ERR	FUNCTION
CLR	CLK	POINT P	ERR <sub>n-1</sub> †			
H	↑	H	H	H		
H	↑	X	L	L	Sample	
H	↑	L	X	L		
L	X	X	X	H	Clear	

† State of ERR before any changes at CLR, CLK, or point P

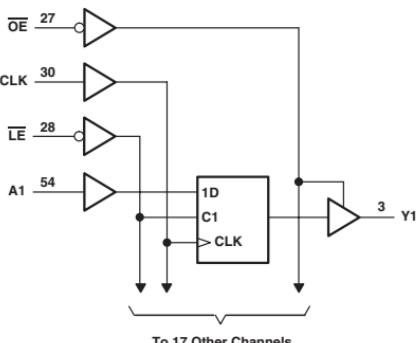
## ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	ABT	ACT	UNIT
I <sub>CC</sub>	MAX	36	0.08	mA
I <sub>OH</sub>	MAX	-32	-24	mA
I <sub>OL</sub>	MAX	64	24	mA

## TIMING REQUIREMENTS AND SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	ABT	ACT	
t <sub>w</sub> Pulse duration	CLK high or low		MIN	3	4	
	CLR low			-	4	
t <sub>ws</sub> Setup time	A data before CLK ↑ , A port		MIN	4..5	-	
	A data before CLK ↑ , CLR			1	1.5	
	A data before CLK ↑ , OE <sub>A</sub>			5	-	
t <sub>th</sub> Hold time	A data after CLK ↑ , A port or OE <sub>A</sub>		MIN	0	0	
t <sub>PLH</sub>	A or B	B or A	MAX	4.1	10.4	
				4.3	10.7	
t <sub>PLH</sub>	A	PARITY	MAX	6.7	13.5	
				6.1	13.8	
t <sub>PZH</sub>	OEB or OE <sub>A</sub>	A or B	MAX	5.6	11.2	
t <sub>PZL</sub>	OEB or OE <sub>A</sub>	A or B	MAX	6	13	
t <sub>PZH</sub>	OEB or OE <sub>A</sub>	A or B	MAX	5.4	10.8	
t <sub>PZL</sub>	OEB or OE <sub>A</sub>	A or B	MAX	4.3	10.1	
t <sub>PLH</sub>	CLK, CLR	ERR	MAX	4.6	15.8	
				3.9	11.6	
t <sub>PLH</sub>	OE <sub>B</sub>	PARITY	MAX	6.7	-	
				6.1	-	
t <sub>PLH</sub>	OE <sub>A</sub>	PARITY	MAX	6.7	13.2	
				6.1	13.6	
t <sub>PZH</sub>	OEB	PARITY	MAX	5.7	9.5	
t <sub>PZL</sub>	OEB	PARITY	MAX	6.5	10.7	
t <sub>PZH</sub>	OEB	PARITY	MAX	4.7	10.2	
t <sub>PZL</sub>	OEB	PARITY	MAX	4.1	9.7	
t <sub>PLH</sub>	OE <sub>A</sub>	PARITY	MAX	5.7	-	
				6.5	-	
t <sub>PLH</sub>	OE <sub>A</sub>	PARITY	MAX	4.7	-	
				4.1	-	

UNIT: ns

**16-BIT UNIVERSAL BUS DRIVER  
WITH 3-STATE OUTPUTS**
**Logic Diagram**

**FUNCTION TABLE**

INPUTS				OUTPUT
OE	LE	CLK	A	Y
H	X	X	X	Z
L	L	X	L	L
L	L	X	H	H
L	H	↑	L	L
L	H	↑	H	H
L	H	H	X	$Y_0^\dagger$
L	H	H	L	$Y_0^\ddagger$

† Output level before the indicated steady-state input conditions were established, provided that CLK is high before LE goes high.

‡ Output level before the indicated steady-state input conditions were established.

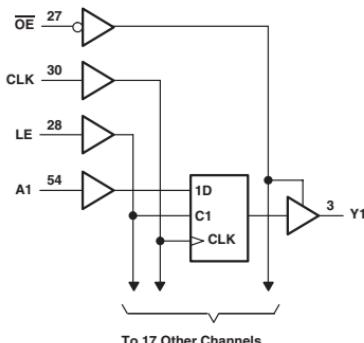
**ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS**

PARAMETER	MAX or MIN	AVLVC 3V	AVC 3V	UNIT
I <sub>CC</sub>	MAX	0.04	0.04	mA
I <sub>OH</sub>	MAX	-24	-12	mA
I <sub>OL</sub>	MAX	24	12	mA

**TIMING REQUIREMENTS AND SWITCHING CHARACTERISTICS**

PARAMETER	INPUT	OUTPUT	MAX or MIN	AVLVC 3V	AVC 3V
f <sub>max</sub>			MIN	150	150
t <sub>w</sub> Pulse duration	LE low		MIN	3.3	3.3
	CLK high or low		MIN	3.3	3.3
t <sub>su</sub> Setup time	Data before CLK ↑		MIN	1.7	0.7
	Data before LE ↑ , CLK high		MIN	1.9	1
	Data before LE ↑ , CLK low		MIN	1.5	1
t <sub>th</sub> Hold time	A data after CLK ↑		MIN	0.7	0.9
	Data after LE ↑ , CLK high		MIN	0.9	1.4
	Data after LE ↑ , CLK low		MIN	0.9	1.3
t <sub>PLH</sub>	A	Y	MAX	3.6	2.5
t <sub>PHL</sub>				3.6	2.5
t <sub>PLH</sub>	LE	Y	MAX	4.9	4
t <sub>PHL</sub>				4.9	4
t <sub>PLH</sub>	CLK	Y	MAX	4.6	3.1
t <sub>PHL</sub>				4.6	3.1
t <sub>PZH</sub>	OE	Y	MAX	5	6.2
t <sub>PZL</sub>				5	6.2
t <sub>PHZ</sub>	OE	Y	MAX	4.5	5.3
t <sub>PLZ</sub>				4.5	5.3

UNIT fmax : MHz other : ns

**3.3-V ABT 18-BIT UNIVERSAL BUS DRIVER  
WITH 3-STATE OUTPUTS**


FUNCTION TABLE

INPUTS				OUTPUT
OE	LE	CLK	A	Y
H	X	X	X	Z
H	H	X	L	L
L	H	X	H	H
L	L	↑	L	L
L	L	H	X	$Y_0^{\dagger}$
L	L	X	X	$Y_0^{\ddagger}$

† Output level before the indicated steady-state condition was established, provided that CLK was high before LE went low.

‡ Output level before the indicated steady-state input conditions were established.

## ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	LVTH 3V	ALVC 3V	ALVCH 3V	AVC 3V	UNIT
I <sub>CC</sub>	MAX	5	0.04	0.04	0.04	mA
I <sub>OH</sub>	MAX	-32	-24	-24	-12	mA
I <sub>OL</sub>	MAX	64	24	24	12	mA

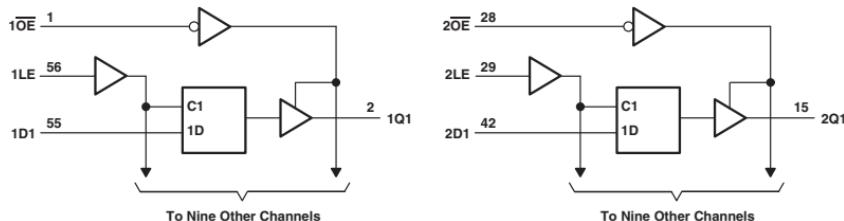
## TIMING REQUIREMENTS AND SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	LVTH 3V	ALVC 3V	ALVCH 3V	AVC 3V
f <sub>max</sub>			MIN	150	150	150	150
t <sub>w</sub> Pulse duration	LE low		MIN	3.3	3.3	3.3	3.3
	CLK high or low		MIN	3.3	3.3	3.3	3.3
t <sub>su</sub> Setup time	Data before CLK ↑		MIN	2.1	1.7	1.7	0.7
	Data before LE ↓, CLK high		MIN	2.3	1.5	1.5	0.8
t <sub>hl</sub> Hold time	Data before LE ↓, CLK low		MIN	1.5	1	1	0.5
	A data after CLK ↑		MIN	1	0.7	0.7	1.3
t <sub>phz</sub>	Data after LE ↓, CLK high		MIN	0.8	1.4	1.4	1.6
	Data after LE ↓, CLK low		MIN	0.8	1.4	1.4	1.4
t <sub>PLH</sub>	A	Y	MAX	3.7	3.6	3.6	2.5
t <sub>PHL</sub>			MAX	3.7	3.6	3.6	2.5
t <sub>PLH</sub>	LE	Y	MAX	5.1	4.2	4.2	3.8
t <sub>PHL</sub>			MAX	5.1	4.2	4.2	3.8
t <sub>PLH</sub>	CLK	Y	MAX	5.1	4.5	4.5	3.1
t <sub>PHL</sub>			MAX	5.1	4.5	4.5	3.1
t <sub>PZH</sub>	OE	Y	MAX	4.6	4.6	4.6	6.2
t <sub>PZL</sub>			MAX	4.6	4.6	4.6	6.2
t <sub>PHZ</sub>	OE	Y	MAX	5.8	3.9	3.9	5.3
t <sub>PLZ</sub>			MAX	5.8	3.9	3.9	5.3

UNIT f<sub>max</sub> : MHz other : ns

## 20-BIT BUS INTERFACE D-TYPE LATCHES WITH 3-STATE OUTPUTS

Logic Diagram

FUNCTION TABLE  
(each 10-bit latch)

INPUTS			OUTPUT		
$\overline{OE}$	LE	D	Q		
L	H	H	H		
L	H	L	L		
L	L	X	$Q_0$		
H	X	X	Z		

## ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	ABT	ACT	ALVCH 3V	UNIT
$I_{CC}$	MAX	89	0.08	0.04	mA
$I_{OH}$	MAX	-32	-24	-24	mA
$I_{OL}$	MAX	64	24	24	mA

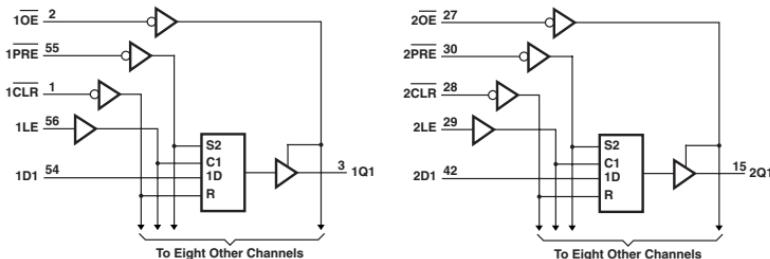
## TIMING REQUIREMENTS AND SWITCHING CHARACTERISTICS

PARAMETER	INPUT		OUTPUT		MAX or MIN	ABT	ACT	ALVCH 3V
$t_w$ Pulse duration	LE	high			MIN	4	4	3.3
		low				4	-	3.3
$t_{su}$ Setup time	Data before LE ↓				MIN	1	1.5	-
	Data before LE ↑					-	-	1.1
$t_h$ Hold time	Data after LE ↓	high			MIN	2	3	-
		low				2	4.5	-
	Data after LE ↑				MIN	-	-	1.1
						5	11.8	3.9
$t_{PLH}$	D		Q		MAX	5.1	12.2	3.9
$t_{PHL}$						5	12.7	4.3
$t_{PHL}$	LE		Q		MAX	5	12.7	4.3
$t_{PZH}$						5.7	11.3	4.9
$t_{PZL}$	$\overline{OE}$		Q		MAX	5.6	13.7	4.9
$t_{PHZ}$						6.5	10.2	4.1
$t_{PLZ}$	$\overline{OE}$		Q		MAX	7.1	9.6	4.1

UNIT : ns

## 18-BIT BUS INTERFACE D-TYPE LATCHES WITH 3-STATE OUTPUTS

Logic Diagram

FUNCTION TABLE  
(each 9-bit latch)

INPUTS				OUTPUT Q
PRE	CLR	OE	LE	D
L	X	L	X	X
H	L	L	X	X
H	H	L	H	L
H	H	L	H	H
H	H	L	L	X
X	X	H	X	X
				Q <sub>0</sub>
				Z

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	ABT	UNIT
I <sub>CC</sub>	MAX	85	mA
I <sub>OH</sub>	MAX	-32	mA
I <sub>OL</sub>	MAX	64	mA

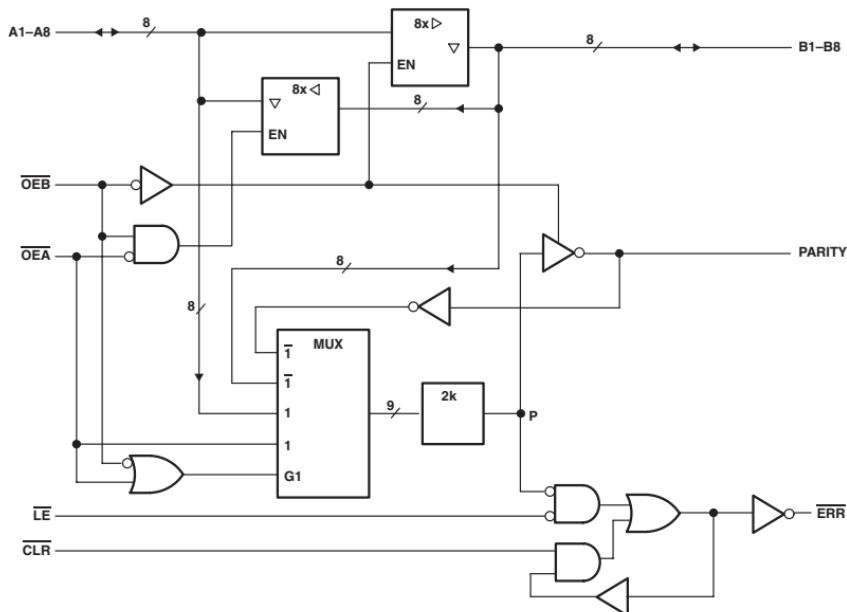
TIMING REQUIREMENTS AND SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	ABT	
t <sub>w</sub> Pulse duration	CLR low		MIN	3.3	
	PRE low			3.3	
	LE high			3.3	
t <sub>su</sub> Setup time	Data before LE ↓, high		MIN	0.9	
	Data before LE ↓, low			0.6	
t <sub>th</sub> Hold time	Data after LE ↓, high		MIN	1.7	
	Data after LE ↓, low			1.8	
t <sub>PLH</sub>	D	Q	MAX	4.8	
t <sub>PHL</sub>			MAX	4.8	
t <sub>PLH</sub>	LE	Q	MAX	5.9	
t <sub>PHL</sub>			MAX	5.3	
t <sub>PLH</sub>	PRE	Q	MAX	6.1	
t <sub>PHL</sub>			MAX	5	
t <sub>PLH</sub>	CLR	Q	MAX	5.4	
t <sub>PHL</sub>			MAX	6	
t <sub>PZH</sub>	OE	Q	MAX	5.4	
t <sub>PZL</sub>			MAX	5.8	
t <sub>PHZ</sub>	OE	Q	MAX	6.3	
t <sub>PZL</sub>			MAX	5.2	

UNIT: ns

## DUAL 8-BIT TO 9-BIT PARITY BUS TRANSCEIVERS

Logic Diagram



FUNCTION TABLE

INPUTS				OUTPUT AND I/Os				FUNCTION				
OEB	OEA	CLR	LE	$\Sigma$ OF H	Bi†	$\Sigma$ OF H	A	B	PARITY	ERR‡		
L	H	X	X	Odd Even	NA	NA	N	A	L	NA	A data to B bus and generate parity	
H	L	H	L	NA	Odd Even	NA	B	NA	H	L	B data to A bus and check parity	
H	L	H	H	NA	X	X	X	NA	NA	NC	Store error flag	
X	X	L	H	X	X	X	X	NA	NA	H	Clear error flag register	
		H	H	X				Z	Z	Z	NC	Isolation§ (parity check)
H	H	L	H	X		X	Z	Z	H	L		
		X	L	L Odd								
		X	L	H Even								
L	L	X	X	Odd Even	NA	NA	N	A	H	L	NA	A data to B bus and generate inverted parity

NA = not applicable, NC = no change, X = don't care

† Summation of high-level inputs includes PARITY along with Bi inputs.

‡ Output states shown assume ERR was previously high.

§ In this mode, ERR (when clocked) shows inverted parity of the A bus.

ERROR-FLAG FUNCTION TABLE

INPUTS	INTERNAL OUTPUT TO DEVICE		OUTPUT ERR	FUNCTION
	POINT P	ERR <sub>n-1</sub> †		
L L	L	X	L	Pass
H L	L	X	L	Sample
L H	X	L	L	Clear
H H	X	H	L	Store

† State of ERR before changes at CLR, LE, or point P

## ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	ABT	UNIT
I <sub>CC</sub>	MAX	40	mA
I <sub>OH</sub>	MAX	-32	mA
I <sub>OL</sub>	MAX	64	mA

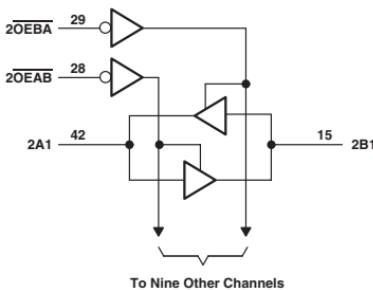
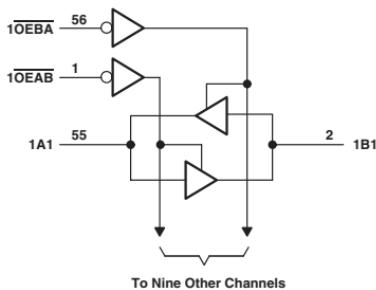
## TIMING REQUIREMENTS AND SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	ABT
t <sub>w</sub> Pulse duration	LE high or low		MIN	8.5
	CLR low			4
t <sub>su</sub> Setup time	A, B and PARITY before LE ↓		MIN	10
	CLR before LE ↓			0
t <sub>h</sub> Hold time	A, B and PARITY after LE ↓		MIN	0
	CLR after LE ↓			0
t <sub>PLH</sub>	A or B	B or A	MAX	4.1
t <sub>PHL</sub>				4.3
t <sub>PLH</sub>	A or OE	PARITY	MAX	7.1
t <sub>PHL</sub>				7.2
t <sub>PLH</sub>	CLR	ERR	MAX	5.7
t <sub>PZH</sub>	OE	A or B	MAX	5.6
t <sub>PZL</sub>				6
t <sub>PHZ</sub>	OE	A or B	MAX	5.4
t <sub>PZL</sub>				4.3
t <sub>PHZ</sub>	OE	PARITY	MAX	5.7
t <sub>PZL</sub>				6.5
t <sub>PHZ</sub>	OE	PARITY	MAX	4.7
t <sub>PZL</sub>				4.1
t <sub>PLH</sub>	LE	ERR	MAX	4.8
t <sub>PHL</sub>				4.9
t <sub>PLH</sub>	A, B or PARITY	ERR	MAX	7.2
t <sub>PHL</sub>				7.4

UNIT: ns

## 20-BIT BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

Logic Diagram

FUNCTION TABLE  
(each 10-bit section)

INPUTS		OPERATION
OEA <sub>B</sub>	OEB <sub>A</sub>	
L	L	Latch A and B (A = B)
L	H	A to B
H	L	B to A
H	H	Isolation

## ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	ACT	UNIT
I <sub>CC</sub>	MAX	0.08	mA
I <sub>OH</sub>	MAX	-24	mA
I <sub>OL</sub>	MAX	24	mA

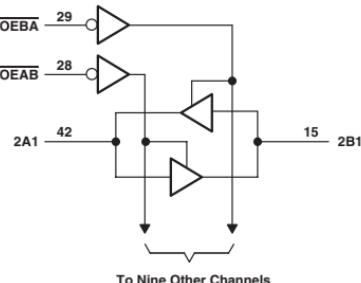
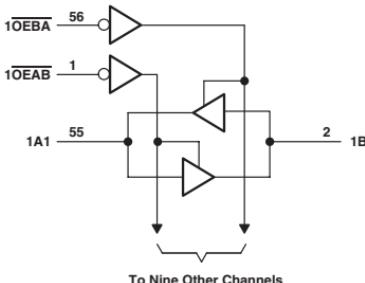
## SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	ACT
t <sub>PLH</sub>	A or B	B or A	MAX	10.4 11.1
t <sub>PHL</sub>	OEBA or OEAB	A or B	MAX	10 12.7
t <sub>PZH</sub>	OEBA or OEAB	A or B	MAX	10.7 10
t <sub>PLZ</sub>	OEBA or OEAB	A or B	MAX	10

UNIT: ns

## 18-BIT BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

Logic Diagram

FUNCTION TABLE  
(each 9-bit section)

INPUTS		OPERATION
OEAB	OEBA	
H	L	B data to A bus
L	H	A data to B bus
H	H	Isolation

## ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	ABT	ACT	ALVCH 3V	UNIT
Icc	MAX	32	0.08	0.04	mA
IoH	MAX	-32	-24	-24	mA
IoL	MAX	64	24	24	mA

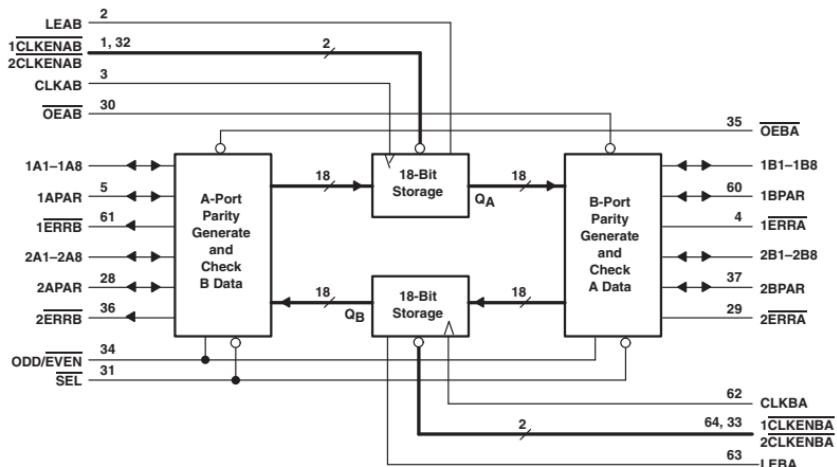
## SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	ABT	ACT	ALVCH 3V
t <sub>PLH</sub>	A or B	B or A	MAX	3.5	11.1	3.4
t <sub>PHL</sub>				3.9	11.8	3.4
t <sub>PZH</sub>	OEBA or OEAB	A or B	MAX	5.4	10.6	4.7
t <sub>PZL</sub>				4.8	13.6	4.7
t <sub>PHZ</sub>	OEBA or OEAB	A or B	MAX	6	11.6	4.2
t <sub>PZL</sub>				5	11	4.2

UNIT: ns

## 18-BIT UNIVERSAL BUS TRANSCEIVER WITH PARITY GENERATORS/CHECKERS

Block Diagram



FUNCTION TABLE

INPUTS				OUTPUT B
CLKENAB	OEAB	LEAB	CLKAB	A
X	H	X	X	X
X	L	H	X	L
X	L	H	X	H
H	L	L	X	X
L	L	L	↑	L
L	L	L	↑	H
L	L	L	L	X
L	L	L	H	X

† Output level before the indicated steady-state input conditions were established

§ Output level before the indicated steady-state input conditions were established, provided that CLKAB was low before LEAB went low

PARITY-ENABLE FUNCTION TABLE

INPUTS			OPERATION OR FUNCTION		
SEL	OEBA	OEAB	SEL	OEBA	OEAB
L	H	L			Parity is checked on port A and is generated on port B.
L	L	H			Parity is checked on port B and is generated on port A.
L	H	H			Parity is checked on port B and port A.
L	L	L			Parity is generated on port A and B if device is in FF mode.
H	L	L			Parity functions are disabled; device acts as a standard 18-bit registered transceiver.
H	L	H			QA data to B, QB data to A
H	H	L			QB data to A, QA data to B
H	H	H			Isolation

PARITY FUNCTION TABLE

INPUTS				OUTPUTS							
SEL	OEBA	OEAB	ODD/EVEN	Σ OF INPUTS A1-A8 = H	Σ OF INPUTS B1-B8 = H	APAR	BPAR	APAR	ERRA	BPAR	ERRB
L	H	L	L	0, 2, 4, 6, 8	N/A	L	N/A	N/A	H	L	Z
L	H	L	L	1, 3, 5, 7	N/A	L	N/A	N/A	L	H	Z
L	H	L	L	0, 2, 4, 6, 8	N/A	H	N/A	N/A	L	L	Z
L	H	L	L	1, 3, 5, 7	N/A	H	N/A	N/A	H	H	Z
L	H	L	L	N/A	0, 2, 4, 6, 8	N/A	L	L	Z	N/A	H
L	L	H	L	N/A	1, 3, 5, 7	N/A	L	H	Z	N/A	L
L	L	H	L	N/A	0, 2, 4, 6, 8	N/A	H	L	Z	N/A	L
L	L	H	L	1, 3, 5, 7	N/A	H	N/A	H	Z	N/A	H
L	H	L	H	0, 2, 4, 6, 8	N/A	L	N/A	N/A	L	H	Z
L	H	L	H	1, 3, 5, 7	N/A	L	N/A	N/A	H	L	Z
L	H	L	H	0, 2, 4, 6, 8	N/A	H	N/A	N/A	H	H	Z
L	H	L	H	1, 3, 5, 7	N/A	H	N/A	N/A	L	L	Z
L	L	H	H	N/A	0, 2, 4, 6, 8	N/A	L	H	Z	N/A	L
L	L	H	H	N/A	1, 3, 5, 7	N/A	L	L	Z	N/A	H
L	L	H	H	N/A	0, 2, 4, 6, 8	N/A	H	H	Z	N/A	H
L	L	H	H	1, 3, 5, 7	N/A	H	N/A	H	L	Z	L
L	H	H	H	0, 2, 4, 6, 8	0, 2, 4, 6, 8	L	L	Z	H	Z	H
L	H	H	H	1, 3, 5, 7	1, 3, 5, 7	L	L	Z	L	Z	L
L	H	H	H	0, 2, 4, 6, 8	0, 2, 4, 6, 8	H	H	Z	H	Z	H
L	H	H	H	1, 3, 5, 7	1, 3, 5, 7	H	H	Z	L	Z	L
L	L	L	L	N/A	N/A	N/A	N/A	PET	Z	PET	Z
L	L	L	H	N/A	N/A	N/A	N/A	POT	Z	POT	Z

† Parity output is set to the level so that the specific bus side is set to even parity.

‡ Parity output is set to the level so that the specific bus side is set to odd parity.

## ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

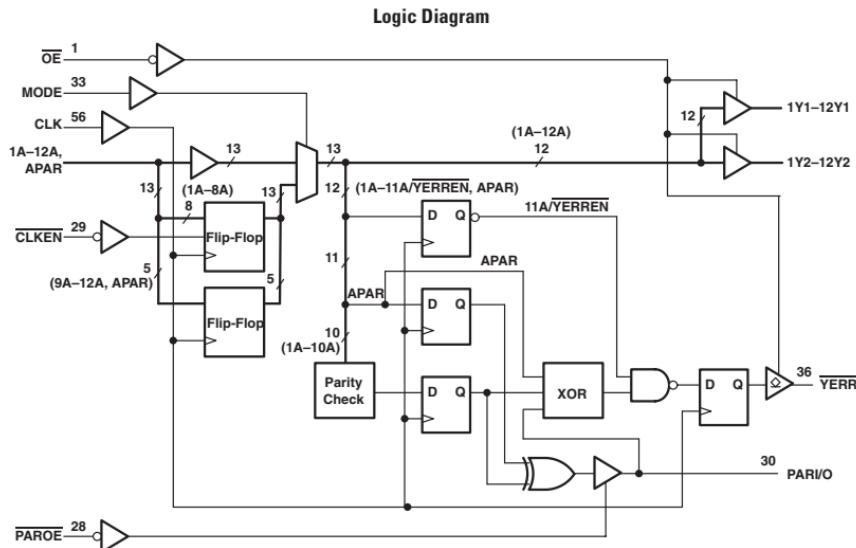
PARAMETER	MAX or MIN	LVCH 3V	ALVCH 3V	UNIT
I <sub>CC</sub>	MAX	0.02	0.04	mA
I <sub>OH</sub>	MAX	-24	-24	mA
I <sub>OL</sub>	MAX	24	24	mA

## TIMING REQUIREMENTS AND SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	LVCH 3V	ALVCH 3V
t <sub>max</sub>			MIN	125	125
t <sub>w</sub> Pulse duration	CLK ↑ LE high		MIN	3	3
t <sub>su</sub> Setup time	A, APAR or B, BPAR before CLK ↑ CLKEN before CLK ↑		MIN	2.5	1.7
	A, APAR or B, BPAR before LE ↓		MIN	2	1.2
t <sub>h</sub> Hold time	A, APAR or B, BPAR after CLK ↑ CLKEN after CLK ↑		MIN	1.3	0.5
	A, APAR or B, BPAR after LE ↓		MIN	1.7	0.9
t <sub>PLH</sub>	A or B	B or A	MAX	5.4	4.4
t <sub>PHL</sub>				5.4	4.4
t <sub>PLH</sub>	A or B	BPAR or APAR	MAX	7.7	6.7
t <sub>PHL</sub>				7.7	6.7
t <sub>PLH</sub>	APAR or BPAR	BPAR or APAR	MAX	5.7	4.7
t <sub>PHL</sub>				5.7	4.7
t <sub>PLH</sub>	APAR or BPAR	ERRA or ERRB	MAX	8.5	7.5
t <sub>PHL</sub>				8.5	7.5
t <sub>PLH</sub>	ODD / EVEN	ERRA or ERRB	MAX	7.8	6.8
t <sub>PHL</sub>				7.8	6.8
t <sub>PLH</sub>	ODD / EVEN	BPAR or APAR	MAX	7.5	6.5
t <sub>PHL</sub>				7.5	6.5
t <sub>PLH</sub>	SEL	BPAR or APAR	MAX	6.1	5.1
t <sub>PHL</sub>				6.1	5.1
t <sub>PLH</sub>	CLKAB or CLKBA	A or B	MAX	6.1	5.1
t <sub>PHL</sub>				6.1	5.1
t <sub>PLH</sub>	CLKAB or CLKBA	BPAR or APAR parity feedthrough	MAX	6.6	5.6
t <sub>PHL</sub>				6.6	5.6
t <sub>PLH</sub>	CLKAB or CLKBA	BPAR or APAR parity generated	MAX	8.7	7.7
t <sub>PHL</sub>				8.7	7.7
t <sub>PLH</sub>	CLKAB or CLKBA	ERRA or ERRB	MAX	8.9	7.9
t <sub>PHL</sub>				8.9	7.9
t <sub>PLH</sub>	LEAB or LEBA	A or B	MAX	5.8	4.8
t <sub>PHL</sub>				5.8	4.8
t <sub>PLH</sub>	LEAB or LEBA	BPAR or APAR parity feedthrough	MAX	6.3	5.3
t <sub>PHL</sub>				6.3	5.3
t <sub>PLH</sub>	LEAB or LEBA	BPAR or APAR parity generated	MAX	8.4	7.4
t <sub>PHL</sub>				8.4	7.4
t <sub>PLH</sub>	LEAB or LEBA	ERRA or ERRB	MAX	8.5	7.5
t <sub>PHL</sub>				8.5	7.5
t <sub>PZH</sub>	OEAB or OEB	B, BPAR or A, APAR	MAX	6.3	5.3
t <sub>PZL</sub>				6.3	5.3
t <sub>PZH</sub>	OEAB or OEB	B, BPAR or A, APAR	MAX	5.9	4.9
t <sub>PZL</sub>				5.9	4.9
t <sub>PZH</sub>	OEAB or OEB	ERRA or ERRB	MAX	5.9	4.9
t <sub>PZL</sub>				5.9	4.9
t <sub>PZH</sub>	OEAB or OEB	ERRA or ERRB	MAX	6.7	5.7
t <sub>PZL</sub>				6.7	5.7
t <sub>PZH</sub>	SEL	ERRA or ERRB	MAX	6.5	5.5
t <sub>PZL</sub>				6.5	5.5
t <sub>PZH</sub>	SEL	ERRA or ERRB	MAX	5.9	4.9
t <sub>PZL</sub>				5.9	4.9

UNIT fmax : MHz other : ns

## 3.3-V 12-BIT UNIVERSAL BUS DRIVER WITH PARITY CHECKER AND DUAL 3-STATE OUTPUTS

**FUNCTION TABLE**

INPUTS				OUTPUTS		
OE	MODE	CLKEN	CLK	A	1Y <sub>n</sub> <sup>†</sup> -8Y <sub>n</sub> <sup>†</sup>	9Y <sub>n</sub> <sup>†</sup> -12Y <sub>n</sub> <sup>†</sup>
L	L	L	↑	H	H	H
L	L	L	↑	L	L	L
L	L	H	↑	H	Y <sub>0</sub>	H
L	L	H	↑	L	Y <sub>0</sub>	L
L	H	X	X	H	H	H
L	H	X	X	L	L	L
H	X	X	X	X	Z	Z

† n=1, 2

**PARI/O FUNCTION†**

INPUTS		OUTPUT	
PAROE	Σ OF INPUTS 1A - 10A = H	APAR	PARI/O
L	0, 2, 4, 6, 8, 10	L	L
L	1, 3, 5, 7, 9	L	H
L	0, 2, 4, 6, 8, 10	H	H
L	1, 3, 5, 7, 9	H	L
H	X	X	Z

† This table applies to the first device of a cascaded pair of ALVCH16903 devices.

**PARITY FUNCTION**

INPUTS		Σ OF INPUTS 1A - 10A = H	APAR	OUTPUT YERR
OE	PAROE <sup>‡</sup>	11A/YERREN <sup>§</sup>	PARI/O	
L	H	L	L	0, 2, 4, 6, 8, 10
L	H	L	L	1, 3, 5, 7, 9
L	H	L	L	0, 2, 4, 6, 8, 10
L	H	L	L	1, 3, 5, 7, 9
L	H	L	H	0, 2, 4, 6, 8, 10
L	H	L	H	1, 3, 5, 7, 9
H	X	X	X	X
L	X	H	X	X

‡ When used as a single device, PAROE must be tied high.

§ Valid after appropriate number of clock pulses have set internal register.

## ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

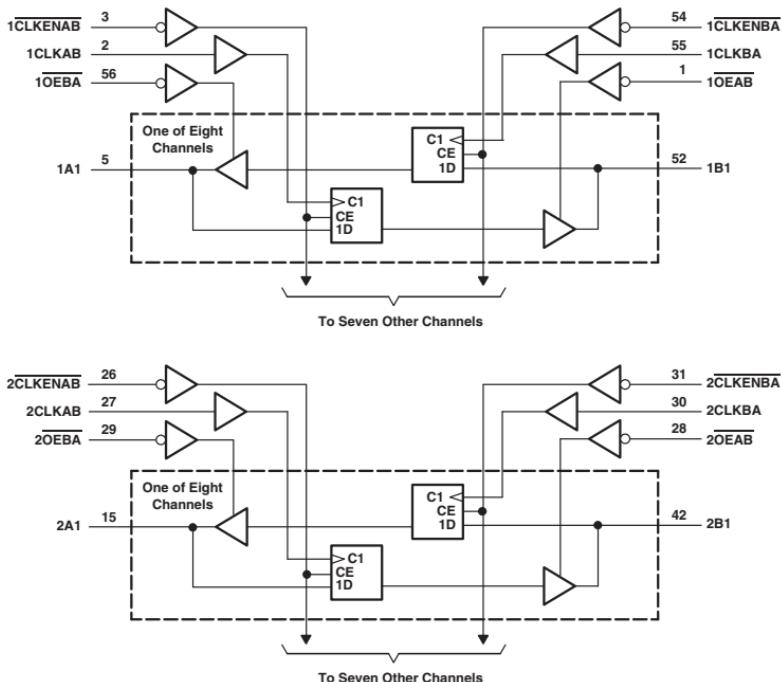
PARAMETER	MAX or MIN	ALVCH 3V	UNIT
I <sub>CC</sub>	MAX	0.04	mA
I <sub>OH</sub>	MAX	-24	mA
I <sub>OL</sub>	MAX	24	mA

## TIMING REQUIREMENTS AND SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	ALVCH 3V
f <sub>max</sub>			MIN	125
t <sub>tr</sub> Pulse duration	CLK ↑		MIN	3
	1A-12A before CLK ↑ , resister mode		MIN	1.45
	1A-10A before CLK ↑ , buffer mode		MIN	4.4
t <sub>su</sub> Setup time	APAR before CLK ↑ , resister mode		MIN	1.3
	APAR before CLK ↑ , buffer mode		MIN	3.1
	PARI/O before CLK ↑ , both mode		MIN	1.7
	PARI/O before CLK ↑ , buffer mode		MIN	1.6
	11A/YERREN before CLK ↑ , buffer mode		MIN	2.2
	CLKEN before CLK ↑ , resister mode		MIN	0.55
	1A-12A after CLK ↑ , resister mode		MIN	0.25
t <sub>th</sub> Hold time	1A-10A after CLK ↑ , buffer mode		MIN	0.7
	APAR after CLK ↑ , resister mode		MIN	0.25
	APAR after CLK ↑ , buffer mode		MIN	0.4
	PARI/O before CLK ↑ , resister mode		MIN	0.5
	PARI/O before CLK ↑ , buffer mode		MIN	0.4
	11A/YERREN after CLK ↑ , buffer mode		MIN	0.4
	CLKEN after CLK ↑ , resister mode		MIN	0.4
I <sub>PLH</sub>	Buffer mode	A	Y	MAX
I <sub>PHL</sub>				3.8
I <sub>PLH</sub>	Both mode	CLK	YERR	MAX
I <sub>PHL</sub>				4.4
I <sub>PLH</sub>	Both mode	CLK	PARI / O	MAX
I <sub>PHL</sub>				6.6
I <sub>PLH</sub>	Both mode	MODE	Y	MAX
I <sub>PHL</sub>				4.9
I <sub>PLH</sub>	Resister mode	CLK	Y	MAX
I <sub>PHL</sub>				4.6
I <sub>PZH</sub>	Both mode	OE	Y	MAX
I <sub>PZL</sub>				5.4
I <sub>PZH</sub>	Both mode	PAROE	PARI / O	MAX
I <sub>PZL</sub>				4.8
I <sub>PZH</sub>	Both mode	OE	Y	MAX
I <sub>PZL</sub>				5
I <sub>PZH</sub>	Both mode	PAROE	PARI / O	MAX
I <sub>PZL</sub>				3.8
I <sub>PLH</sub>	Both mode	OE	YERR	MAX
I <sub>PHL</sub>				4
I <sub>PLH</sub>				4.2

UNIT fmax : MHz other : ns

Logic Diagram



FUNCTION TABLE

INPUTS			OUTPUT B
CLKENAB	CLKAB	OEAB	A
H	X	L	X
X	L	L	X
L	↑	L	L
L	↑	L	H
H	X	H	X
			Z

† A-to-B data flow is shown; B-to-A data flow is similar but uses CLKENBA, CLKBA, and OEBA.

‡ Level of B before the indicated steady-state input conditions were established.

## ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	ABT	ACT	LVT 3V	LVTH 3V	LVCH 3V	ALVCH 3V	UNIT
Icc	MAX	35	0.08	5	5	0.02	0.04	mA
IoH	MAX	-32	-24	-32	-32	-24	-24	mA
IoL	MAX	64	24	64	64	24	24	mA

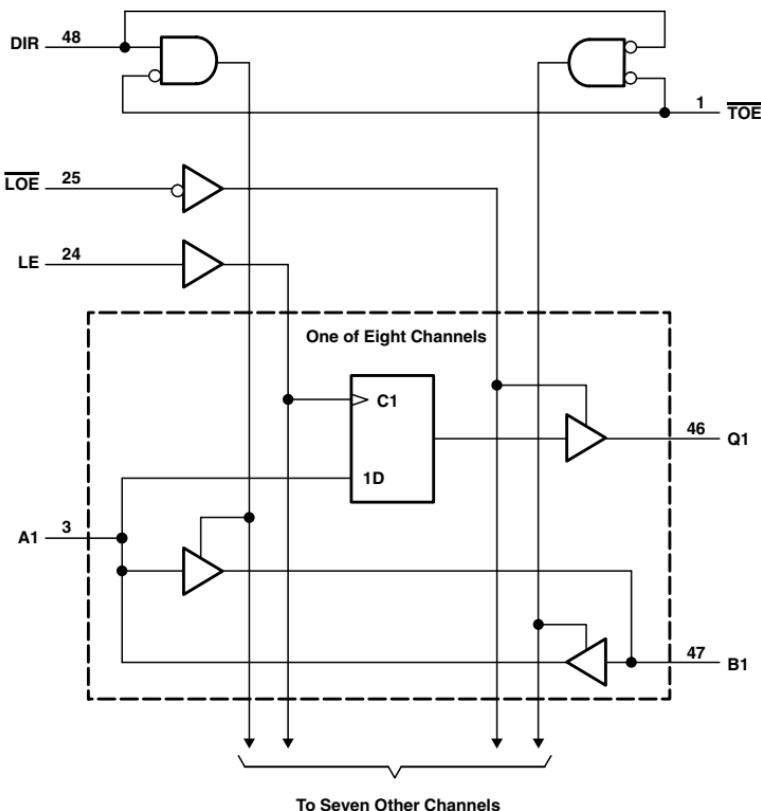
## TIMING REQUIREMENTS AND SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	ABT	ACT	LVT 3V	LVTH 3V	LVCH 3V	ALVCH 3V
tmax			MIN	150	75	150	150	150	150
tw Pulse duration	CLKEN high (SN74LVT: CLKEN high)		MIN	-	-	3.3	-	-	3.3
	CLK high or low			3.3	6.7	3.3	3.3	3.3	3.3
t <sub>su</sub> Setup time	Data before CLK		MIN	3.5	5	2.1	1.7	2.8	1.5
	CLKEN before CLK			3	6.5	1.2	2	1.4	1
t <sub>h</sub> Hold time	Data after CLK		MIN	1	1	0.7	0.8	0.5	0.8
	CLKEN after CLK			1	0	1.4	0.4	1.9	1.1
t <sub>PLH</sub>	CLK	A or B	MAX	4.3	11.8	5.8	4.4	6.6	3.9
t <sub>PHL</sub>				4.5	11.7	5.8	4.4	6.6	3.9
t <sub>PZH</sub>	OEBA or OEAB	A or B	MAX	4.6	11.2	5.6	4.9	6.6	4.4
t <sub>PZL</sub>				6	13	6.5	4.9	6.6	4.4
t <sub>PHZ</sub>	OEBA or OEAB	A or B	MAX	5.5	9.4	6.3	6.2	6.7	4
t <sub>PZL</sub>				4.2	8.7	5.1	5.3	6.7	4

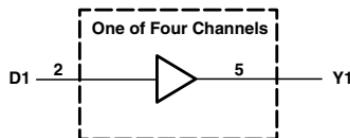
UNIT tmax : MHz other : ns

**8-BIT BUS TRANSCEIVER AND TRANSPARENT D-TYPE LATCH  
WITH FOUR INDEPENDENT BUFFERS**

Logic Diagram



To Seven Other Channels



### FUNCTION TABLE

INPUTS		OPERATION
TOE	DIR	
L	L	B data to A bus
L	H	A data to B bus
H	X	A bus and B bus Isolation

INPUTS			OUTPUT Q
LOE	LE	A	
L	H	H	H
L	H	L	L
L	L	X	Q <sub>O</sub>
H	X	X	Z

INPUT D	OUTPUT Y
L	L
H	H

### ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	ALVCH 3V	UNIT
I <sub>CC</sub>	MAX	0.03	mA
I <sub>OH</sub>	MAX	-24	mA
I <sub>OL</sub>	MAX	24	mA

### TIMING REQUIREMENTS AND SWITCHING CHARACTERISTICS

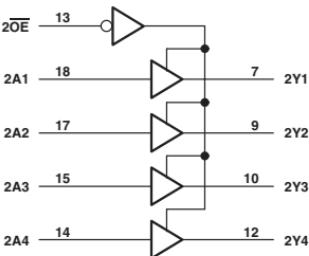
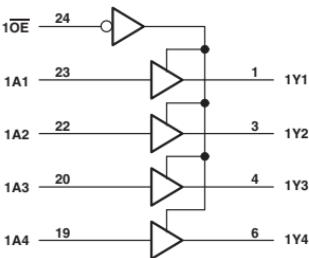
PARAMETER	INPUT	OUTPUT	MAX or MIN	ALVCH 3V
t <sub>w</sub> Pulse duration	LE high		MIN	2
t <sub>ws</sub> Setup time	data before LE ↓		MIN	0.9
t <sub>h</sub> Hold time	data after LE ↓		MIN	0.9
t <sub>PLH</sub>	D	Y	MAX	3
t <sub>PHL</sub>				3
t <sub>PLH</sub>	A	Q	MAX	3
t <sub>PHL</sub>				3
t <sub>PLH</sub>	LE	Q	MAX	3
t <sub>PHL</sub>				3
t <sub>PLH</sub>	A or B	B or A	MAX	3
t <sub>PHL</sub>				3
t <sub>PZH</sub>	LOE	Q	MAX	4.7
t <sub>PZL</sub>				4.7
t <sub>PZH</sub>	TOE	A or B	MAX	4.4
t <sub>PZL</sub>				4.4
t <sub>PZH</sub>	DIR	A or B	MAX	4.7
t <sub>PZL</sub>				4.7
t <sub>PHZ</sub>	LOE	Q	MAX	4.1
t <sub>PZL</sub>				4.1
t <sub>PHZ</sub>	TOE	A or B	MAX	4.1
t <sub>PZL</sub>				4.1
t <sub>PHZ</sub>	DIR	A or B	MAX	4.7
t <sub>PZL</sub>				4.7

UNIT: ns

**25- $\Omega$  OCTAL BUFFER/DRIVER WITH 3-STATE OUTPUTS**

- High Output Drive Current
- Distributed  $V_{CC}$  and GND Pins Minimize Noise Generated by the Simultaneous Switching of Outputs

Logic Diagram

FUNCTION TABLE  
(each buffer/driver)

INPUTS		OUTPUT
OE	A	Y
L	H	H
L	L	L
H	X	Z

## ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	SN74 BCT	SN64 BCT	UNIT
$I_{CC}$	MAX	119	119	mA
$I_{OH}$	MAX	-80	-80	mA
$I_{OL}$	MAX	188	188	mA

## SWITCHING CHARACTERISTICS

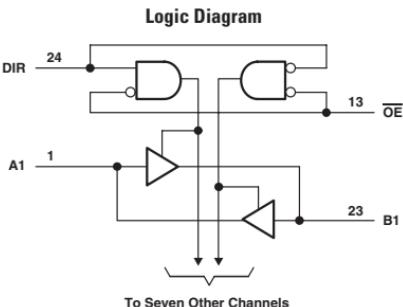
PARAMETER	INPUT	OUTPUT	MAX or MIN	SN74 BCT	SN64 BCT
$t_{PLH}$	A	Y	MAX	5.5	5.5
$t_{PHL}$				6	6.3
$t_{PZH}$	$\overline{OE}$	Y	MAX	9.3	9.7
$t_{PZL}$				10.2	10.4
$t_{PHZ}$	$\overline{OE}$	Y	MAX	6.3	6.5
$t_{PLZ}$				8.4	9.5

UNIT: ns

# 25245

## 25- $\Omega$ OCTAL BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

- High Output Drive Current
- Distributed  $V_{CC}$  and GND Pins Minimize Noise Generated by the Simultaneous Switching of Outputs

**FUNCTION TABLE**

INPUTS	OPERATION	
OE	DIR	
L	L	B data to A bus
L	H	A data to B bus
H	X	Isolation

**ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS**

PARAMETER	MAX or MIN	SN74 BCT	SN64 BCT	ABTH	UNIT
I <sub>CC</sub>	MAX	125	125	20	mA
I <sub>OH</sub> (A port)	MAX	-80	-80	-80	mA
I <sub>OL</sub> (B port)	MAX	-3	-3	-32	mA
I <sub>OL</sub> (A port)	MAX	188	188	188	mA
I <sub>OL</sub> (B port)	MAX	24	24	64	mA

**SWITCHING CHARACTERISTICS**

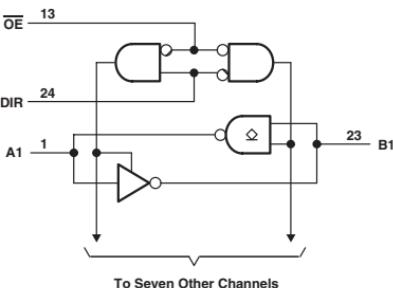
PARAMETER	INPUT	OUTPUT	MAX or MIN	SN74 BCT	SN64 BCT	ABTH
t <sub>PLH</sub>	A	B	MAX	5.7	5.7	3.9
t <sub>PHL</sub>				7.2	7.3	4.3
t <sub>PLH</sub>	B	A	MAX	5.5	5.5	3.9
t <sub>PHL</sub>				6.2	6.3	4.3
t <sub>PZH</sub>	OE	A	MAX	9.6	9.7	6.5
t <sub>PZL</sub>				10.3	10.6	6.8
t <sub>PHZ</sub>	OE	A	MAX	6.2	6.2	7.2
t <sub>PZL</sub>				8.3	8.8	6.4
t <sub>PZH</sub>	OE	B	MAX	8.9	8.9	6.5
t <sub>PZL</sub>				9.7	9.9	6.8
t <sub>PHZ</sub>	OE	B	MAX	6.9	6.9	7.2
t <sub>PZL</sub>				7.5	7.7	6.4

UNIT: ns

25- $\Omega$  OCTAL BUS TRANSCEIVER

- High Output Drive Current
- Distributed  $V_{CC}$  and GND Pins Minimize Noise Generated by the Simultaneous Switching of Outputs

Logic Diagram



## FUNCTION TABLE

INPUTS	OPERATION	
OE	DIR	
L	L	B data to A bus
L	H	A data to B bus
H	X	Isolation

## ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	SN74 BCT	UNIT
$I_{CC}$	MAX	125	mA
$I_{OH}$ (B port)	MAX	-3	mA
$I_{OL}$ (A port)	MAX	188	mA
$I_{OL}$ (B port)	MAX	24	mA
$V_{OH}$ (A port)	MAX	5.5	V

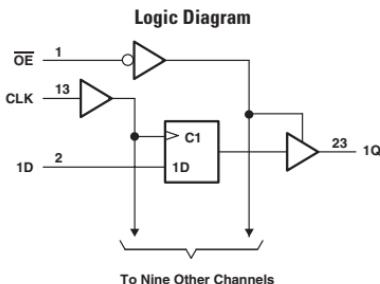
## SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	SN74 BCT
$t_{PLH}$	A	B	MAX	6.2
$t_{PHL}$				4
$t_{PLH}$	B	A	MAX	6.3
$t_{PHL}$				5.9
$t_{PLH}$	$\overline{OE}$	A	MAX	11.6
$t_{PHL}$				11.3
$t_{PZH}$	$\overline{OE}$	B	MAX	9.1
$t_{PZL}$				9.8
$t_{PHZ}$	$\overline{OE}$	B	MAX	7.3
$t_{PLZ}$	$\overline{OE}$	B	MAX	7.3

UNIT: ns

## 10-BIT BUS-INTERFACE FLIP-FLOPS WITH 3-STATE OUTPUTS

- 3-State Outputs
- Data Flow-Through Pinout



**FUNCTION TABLE**  
(each flip-flop)

INPUTS			OUTPUT
OE	CLK	D	Q
L	↑	H	H
L	↑	L	L
L	H or L	X	Q <sub>0</sub>
H	X	X	Z

### ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	ALS	SN74 BCT	UNIT
I <sub>CC</sub>	MAX	115	35	mA
I <sub>OH</sub>	MAX	-24	-24	mA
I <sub>OL</sub>	MAX	48	48	mA

### TIMING REQUIREMENTS AND SWITCHING CHARACTERISTICS

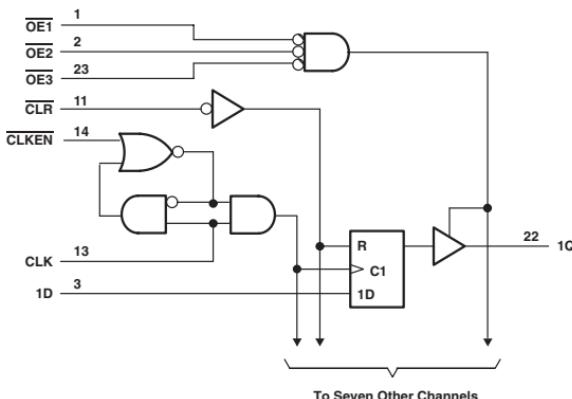
PARAMETER	INPUT	OUTPUT	MAX or MIN	ALS	SN74 BCT
t <sub>max</sub>				-	125
t <sub>w</sub> Pulse duration	CLK high or low		MIN	7	7
t <sub>su</sub> Setup time	Data before CLK ↑		MIN	4	7
t <sub>h</sub> Hold time	Data after CLK ↑		MIN	2	1
t <sub>PLH</sub>	CLK	Q	MAX	10	12
t <sub>PHL</sub>				10	10
t <sub>PZH</sub>	OE	Q	MAX	14	12
t <sub>PZL</sub>				14	13
t <sub>PHZ</sub>	OE	Q	MAX	14	8
t <sub>PZL</sub>				12	8

UNIT f<sub>max</sub> : MHz other : ns

## 8-BIT BUS-INTERFACE FLIP-FLOPS WITH 3-STATE OUTPUTS

- 3-State Outputs
- Data Flow-Through Pinout

Logic Diagram



FUNCTION TABLE

INPUTS				OUTPUT
OE <sub>1</sub>	CLR	CLKEN	CLK	Q
L	L	X	X	L
L	H	L	↑	H
L	H	L	↑	L
L	H	H	H or L	X
H	X	X	X	Z

† OE = H if any of the output-enable inputs is high.

OE = L if all of the output-enable inputs are low.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	SN74 BCT	UNIT
I <sub>CC</sub>	MAX	40	mA
I <sub>OH</sub>	MAX	-24	mA
I <sub>OL</sub>	MAX	48	mA

TIMING REQUIREMENTS AND SWITCHING CHARACTERISTICS

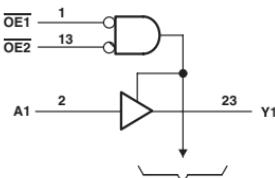
PARAMETER	INPUT	OUTPUT	MAX or MIN	SN74 BCT
t <sub>max</sub>			MIN	125
t <sub>w</sub> Pulse duration	CLK low		MIN	4
	CLK high or low		MIN	4
t <sub>su</sub> Setup time	Before CLK ↑, data high		MIN	6
	Before CLK ↑, data low		MIN	3.5
t <sub>CL</sub>	CLR		MIN	1
	CLKEN before CLK ↑		MIN	8
t <sub>h</sub> Hold time	After CLK ↑, data high		MIN	1.5
	After CLK ↑, data low		MIN	0
t <sub>CLKEN</sub>	CLKEN after CLK ↑		MIN	0.5
			MAX	9
t <sub>PLH</sub>	CLK	Q	MAX	8.4
t <sub>PHL</sub>			MAX	9.5
t <sub>PHL</sub>	CLR	Q	MAX	10.3
t <sub>PZH</sub>	OE	Q	MAX	10.2
t <sub>PZL</sub>	OE	Q	MAX	9
t <sub>PZL</sub>			MAX	8.2

UNIT f<sub>max</sub> : MHz other : ns

# 29827

## 10-BIT BUFFERS/DRIVERS WITH 3-STATE OUTPUTS

- pnp Inputs Reduce dc Loading
- 3-State Outputs
- Data Flow-Through Pinout

**Logic Diagram****FUNCTION TABLE**

INPUTS			OUTPUT
OE1	OE2	A	Y
L	L	L	L
L	L	H	H
L	X	X	Z
H	H	X	Z

**ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS**

PARAMETER	MAX or MIN	ALS	SN74 BCT	UNIT
I <sub>CC</sub>	MAX	40	40	mA
I <sub>OH</sub>	MAX	-24	-24	mA
I <sub>OL</sub>	MAX	48	48	mA

**SWITCHING CHARACTERISTICS**

PARAMETER	INPUT	OUTPUT	MAX or MIN	ALS	SN74 BCT
t <sub>PLH</sub>	A	Y	MAX	7	5.5
t <sub>PHL</sub>				7.5	7.5
t <sub>PZH</sub>	OE	Y	MAX	15	9.1
t <sub>PZL</sub>				15	12.8
t <sub>PHZ</sub>	OE	Y	MAX	17	8.8
t <sub>PLZ</sub>				12	8.4

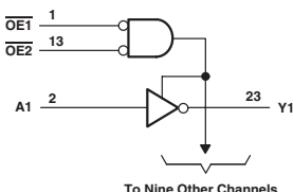
UNIT: ns

# 29828

## 10-BIT BUFFERS/DRIVERS WITH 3-STATE OUTPUTS

- pnp Inputs Reduce dc Loading
- 3-State Outputs
- Data Flow-Through Pinout

Logic Diagram



### ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	ALS	UNIT
I <sub>CC</sub>	MAX	40	mA
I <sub>OH</sub>	MAX	-24	mA
I <sub>OL</sub>	MAX	48	mA

### SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	ALS
t <sub>PLH</sub>	A	Y	MAX	7
t <sub>PHL</sub>				7.5
t <sub>PZH</sub>	OE	Y	MAX	15
t <sub>PZL</sub>				15
t <sub>PHZ</sub>	OE	Y	MAX	17
t <sub>PZL</sub>				12

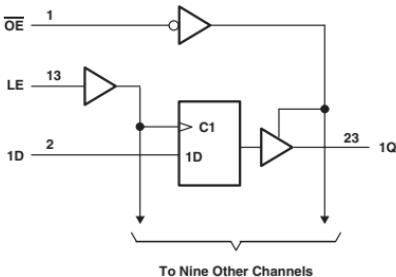
UNIT: ns

**NOTICE : ALS IS NOT RECOMMENDED FOR NEW DESIGNS**

## 10-BIT BUS INTERFACE D-TYPE LATCHES WITH 3-STATE OUTPUTS

- 3-State Outputs
- Data Flow-Through Pinout

Logic Diagram



FUNCTION TABLE

INPUTS	OUTPUT		
OE	LE	D	Q
L	H	H	H
L	H	L	L
L	L	X	Q <sub>0</sub>
H	X	X	Z

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	ALS	SN74 BCT	UNIT
I <sub>CC</sub>	MAX	85	35	mA
I <sub>OH</sub>	MAX	-24	-24	mA
I <sub>OL</sub>	MAX	48	48	mA

TIMING REQUIREMENTS AND SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	ALS	SN74 BCT
t <sub>W</sub> Pulse duration	LE high or low		MIN	6	4
t <sub>WS</sub> Setup time	Data before LE ↓		MIN	2.5	2
t <sub>H</sub> Hold time	Data after LE ↓, high		MIN	4.5	1.5
	Data after LE ↓, low		MIN	4.5	3.5
t <sub>PLH</sub>	D	Q	MAX	9.5	7.5
t <sub>PHL</sub>				9.5	8.6
t <sub>PLH</sub>	LE	Q	MAX	12	8.6
t <sub>PHL</sub>				12	8.1
t <sub>PZH</sub>	OE	Q	MAX	14	9.2
t <sub>PZL</sub>				14	12.8
t <sub>PHZ</sub>	OE	Q	MAX	15	6.9
t <sub>PZL</sub>				12	6.9

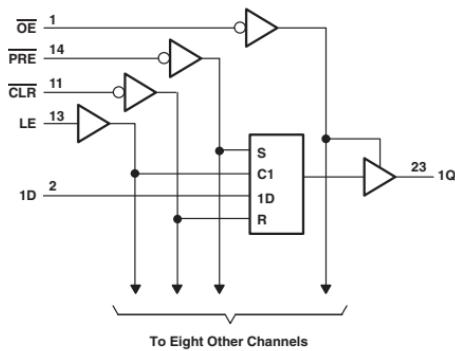
UNIT: ns

**29843**

**9-BIT BUS INTERFACE D-TYPE LATCHES WITH 3-STATE OUTPUTS**

- 3-State Outputs
- Data Flow-Through Pinout

**Logic Diagram**



FUNCTION TABLE

INPUTS				OUTPUT Q
PRE	CLR	OE	LE	D
L	X	L	X	X
H	L	L	X	X
H	H	L	H	L
H	H	L	H	H
H	H	L	L	X
X	X	H	X	X
				Q <sub>0</sub>
				Z

## ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

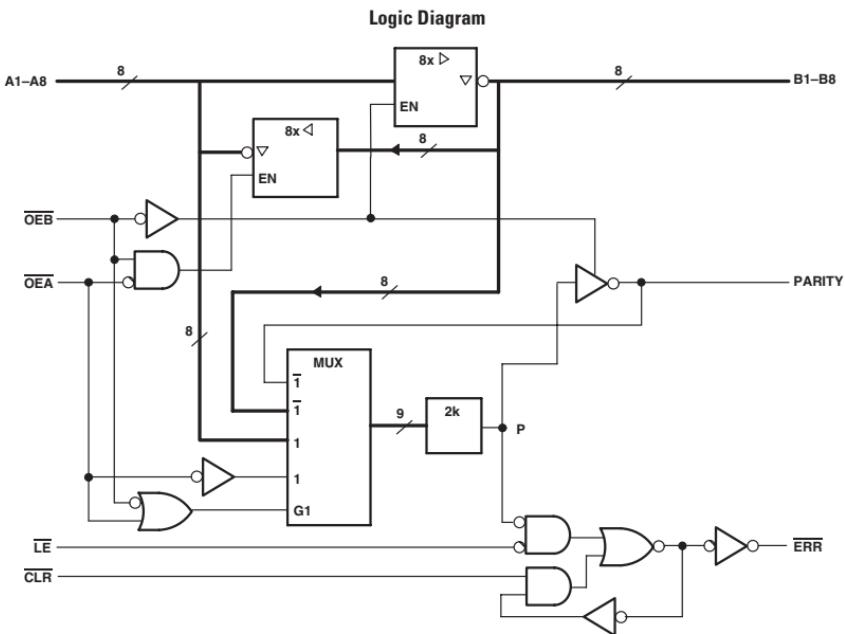
PARAMETER	MAX or MIN	SN74 BCT	UNIT
I <sub>CC</sub>	MAX	35	mA
I <sub>OL</sub>	MAX	-24	mA
I <sub>OL</sub>	MAX	48	mA

## TIMING REQUIREMENTS AND SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	SN74 BCT
t <sub>w</sub> Pulse duration	PRE low		MIN	7
	CLR low			5
	LE high			4
t <sub>su</sub> Setup time	Data before LE ↓ , high or low		MIN	1.5
	PRE or CLR inactive			2
t <sub>h</sub> Hold time	Data after LE ↓ , high or low		MIN	3.5
t <sub>PLH</sub>	D	Q	MAX	8
t <sub>PHL</sub>				9
t <sub>PLH</sub>	LE	Q	MAX	10
t <sub>PHL</sub>				10
t <sub>PLH</sub>	PRE	Q	MAX	12
t <sub>PHL</sub>				12
t <sub>PLH</sub>	CLR	Q	MAX	12
t <sub>PHL</sub>				12
t <sub>PZH</sub>	OE	Q	MAX	15
t <sub>PZL</sub>				15
t <sub>PHZ</sub>	OE	Q	MAX	8
t <sub>PZL</sub>				8

UNIT: ns

## 8-BIT TO 9-BIT PARITY BUS TRANSCEIVER



FUNCTION TABLE

INPUTS						OUTPUT AND I/O				OPERATION
OEB	OE <sub>A</sub>	CLR	LE	Bi <sub>i</sub>	Σ of Hs	Bit	A	B	PARITY	ERR <sup>‡</sup>
L	H	X	X	Odd Even	NA	NA	Ā	H <sub>L</sub>	NA	Ā data to B bus and generate parity
H	L	X	L	NA	Odd Even	Ā	NA	NA	H <sub>L</sub>	Ā data to A bus and check parity
H	L	H	H	NA	X	X	NA	NA	N-1	Store error flag
X	X	L	H	X	X	X	NA	NA	H	Clear error-flag register
H	H	H	X						NC	
H	H	L	H	X		Z	Z	Z	H <sub>L</sub>	Isolation <sup>§</sup>
X	X	L	L Odd	X		X			H	
		L	H Even							
L	L	X	X	Odd Even	NA	NA	Ā	L <sub>H</sub>	NA	Ā data to B bus and generate inverted parity

NA = not applicable, NC = no change, X = don't care

<sup>†</sup> Summation of high-level inputs includes PARITY along with Bi inputs.<sup>‡</sup> Output states shown assume ERR was previously high.<sup>§</sup> In this mode, ERR, when enabled, shows inverted parity of the A bus.

## ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	ALS	SN74 BCT	UNIT
I <sub>CC</sub>	MAX	100	80	mA
I <sub>OH</sub>	MAX	-24	-24	mA
I <sub>OL</sub>	MAX	48	48	mA

## TIMING REQUIREMENTS AND SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	ALS	SN74 BCT
t <sub>w</sub> Pulse duration	LE high		MIN	10	-
	LE low		MIN	10	10
	CLR low		MIN	10	10
t <sub>su</sub> Setup time	Before LE ↓, Bi and PARITY		MIN	10	18
	Before LE ↓, CLR high		MIN	15	-
t <sub>h</sub> Hold time	Bi and PARITY after LE ↓		MIN	3	8
t <sub>PLH</sub>	A or B	B or A	MAX	8	8
t <sub>PHL</sub>			MAX	8	8
t <sub>PLH</sub>	A	PARITY	MAX	15	15
t <sub>PHL</sub>			MAX	18	15
t <sub>PZH</sub>	OE <sub>A</sub> or OEB	A or B	MAX	17	17
t <sub>PZL</sub>			MAX	17	19
t <sub>PHZ</sub>	OE <sub>A</sub> or OEB	A or B	MAX	15	15
t <sub>PZL</sub>			MAX	8	17
t <sub>PLH</sub>	LE	ERR	MAX	12	9
t <sub>PLH</sub>	CLR	ERR	MAX	12	15
t <sub>PLH</sub>	OE <sub>A</sub>	PARITY	MAX	17	15
t <sub>PHL</sub>			MAX	19	16
t <sub>PLH</sub>	Bi / PARITY	ERR	MAX	20	20
t <sub>PHL</sub>			MAX	20	15

UNIT: ns

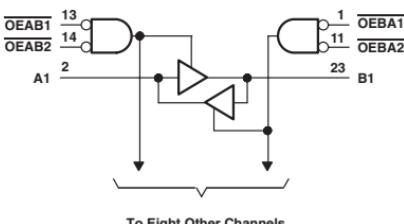
# 29863

## 9-BIT BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

- True Outputs

**FUNCTION TABLE**

INPUTS				OPERATION
OEAB1	OEAB2	OEBA1	OEBA2	
L	L	L	L	Latch A and B
L	L	H	X	A to B
L	L	X	H	
H	X	L	L	B to A
X	H	L	L	
H	X	H	X	
H	X	X	H	
X	H	X	H	
X	H	H	X	Isolation

**Logic Diagram**

To Eight Other Channels

**ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS**

PARAMETER	MAX or MIN	ALS	SN74 BCT	UNIT
I <sub>CC</sub>	MAX	65	45	mA
I <sub>OH</sub>	MAX	-24	-24	mA
I <sub>OL</sub>	MAX	48	48	mA

**SWITCHING CHARACTERISTICS**

PARAMETER	INPUT	OUTPUT	MAX or MIN	ALS	SN74 BCT
t <sub>PLH</sub>	A or B	B or A	MAX	8	5
t <sub>PHL</sub>				8	7.5
t <sub>PZH</sub>	OEAB or OEBA	A or B	MAX	15	8.4
t <sub>PZL</sub>				15	12.6
t <sub>PHZ</sub>	OEAB or OEBA	A or B	MAX	17	8.8
t <sub>PZL</sub>				12	8.1

UNIT: ns

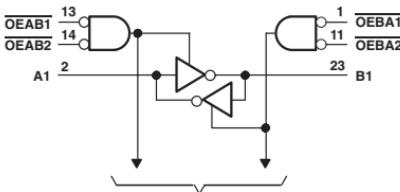
**29864**
**9-BIT BUS TRANSCEIVER  
WITH 3-STATE OUTPUTS**

- Inverted Outputs

FUNCTION TABLE

INPUTS				OPERATION
OEAB1	OEAB2	OEBA1	OEBA2	
L	L	L	L	Latch A and B
L	L	H	X	Ā to B
L	L	X	H	
H	X	L	L	B̄ to A
X	H	L	L	
H	X	H	X	
H	X	X	H	
X	H	X	H	Isolation
X	H	H	X	

Logic Diagram



To Eight Other Channels

## ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

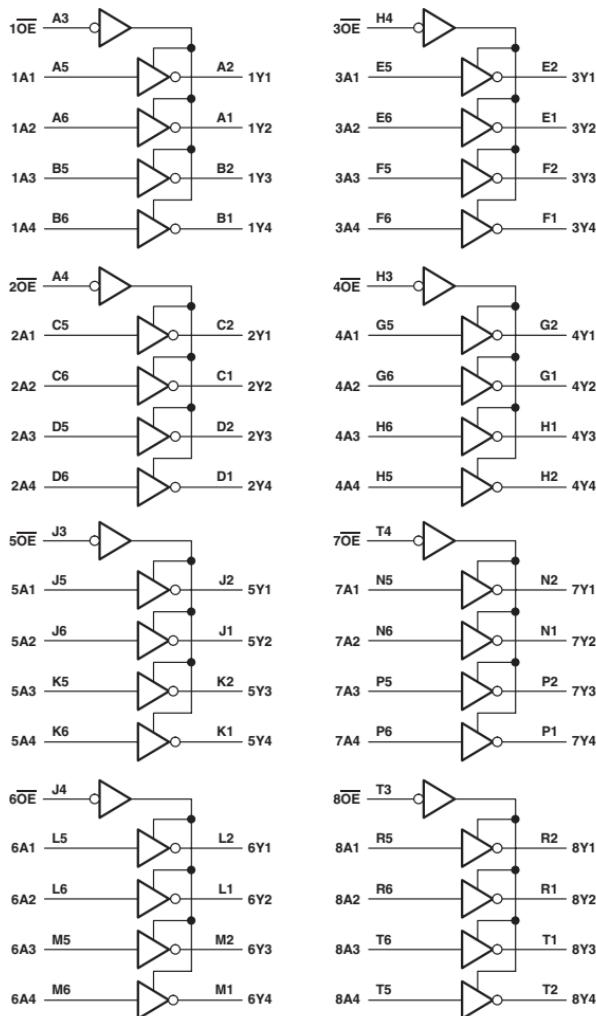
PARAMETER	MAX or MIN	SN74 BCT	UNIT
I <sub>C</sub>	MAX	45	mA
I <sub>OH</sub>	MAX	-24	mA
I <sub>OL</sub>	MAX	48	mA

## SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	SN74 BCT
t <sub>PLH</sub>	A or B	B or A	MAX	6.1
t <sub>PHL</sub>				4.8
t <sub>PZH</sub>	OEAB or OEBA	A or B	MAX	8.4
t <sub>PZL</sub>				12.5
t <sub>PHZ</sub>	OEAB or OEBA	A or B	MAX	8.4
t <sub>PZL</sub>				8.2

UNIT: ns

Logic Diagram



**FUNCTION TABLE**

(each 4bit buffer/driverr)

INPUTS	OUTPUT	
OE	A	Y
L	H	L
L	L	H
H	X	Z

## ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	LVCZ 3V	LVT	UNIT
I <sub>CC</sub>	MAX	0.2	10	mA
I <sub>OH</sub>	MAX	-24	-32	mA
I <sub>OL</sub>	MAX	24	64	mA

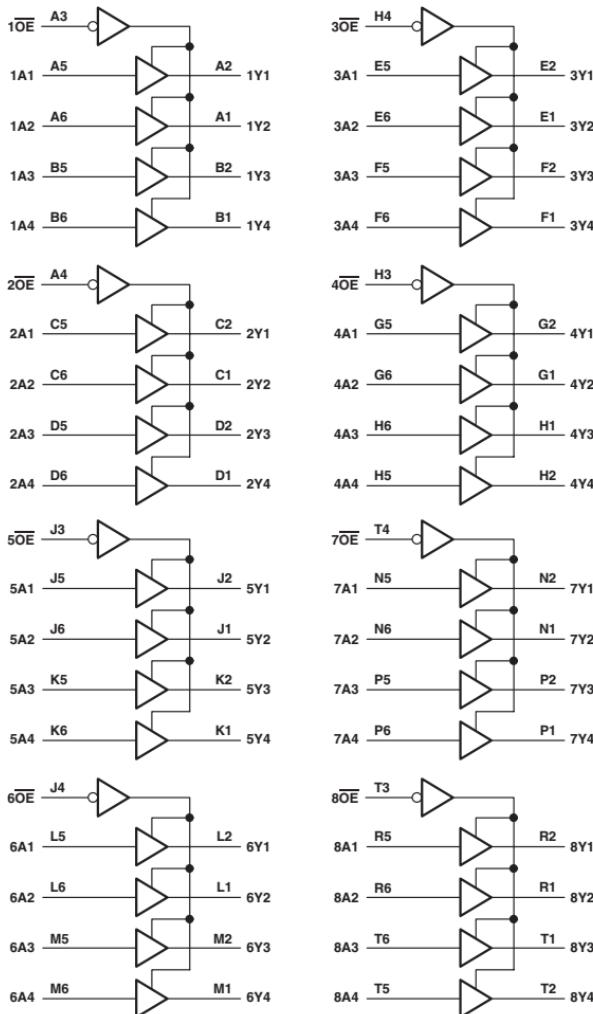
## SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	LVCZ 3V	LVT
t <sub>PLH</sub>	A	Y	MAX	4.2	3.5
t <sub>PHL</sub>			MAX	4.2	3.5
t <sub>PZH</sub>	$\overline{OE}$	Y	MAX	4.7	4
t <sub>PZL</sub>			MAX	4.7	4.4
t <sub>PHZ</sub>	$\overline{OE}$	Y	MAX	5.9	4.5
t <sub>PZL</sub>			MAX	5.9	4.2

UNIT:ns

## 32-BIT BUFFER/DRIVER WITH 3-STATE OUTPUTS

Logic Diagram



**FUNCTION TABLE**

INPUTS		OUTPUT
OE	A	Y
L	H	H
L	L	L
H	X	Z

**ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS**

PARAMETER	MAX or MIN	LVT 3V	LVTH 3V	ALVTH 3V	LVC 3V	LVCH 3V	LVCZ 3V	ALVCH 3V	AUC 1.8V	AUC 2.3V	AUCH 1.8V	AUCH 2.3V	UNIT
I <sub>CC</sub>	MAX	10	10	5	0.04	0.04	0.2	0.08	0.04	0.04	0.04	0.04	mA
I <sub>OH</sub>	MAX	-32	-32	-32	-24	-24	-24	-24	-8	-9	-8	-9	mA
I <sub>OL</sub>	MAX	64	64	64	24	24	24	24	8	9	8	9	mA

**SWITCHING CHARACTERISTICS**

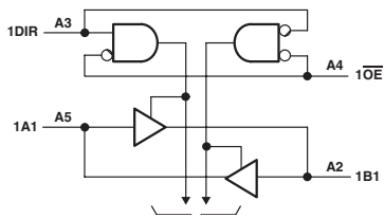
PARAMETER	INPUT	OUTPUT	MAX or MIN	LVT 3V	LVTH 3V	ALVTH 3V	LVC 3V	LVCH 3V	LVCZ 3V	ALVCH 3V	AUC 1.8V
t <sub>PLH</sub>	A	Y	MAX	3.2	3.2	2.4	4.1	4.1	4.1	3	1.8
t <sub>PHL</sub>				3.2	3.2	2.5	4.1	4.1	4.1	3	1.8
t <sub>PZH</sub>	OE	Y	MAX	4	4	3.8	4.6	4.6	4.6	4.4	2.5
t <sub>PZL</sub>				4	4	2.9	4.6	4.6	4.6	4.4	2.5
t <sub>PHZ</sub>	OE	Y	MAX	4.5	4.5	4.2	5.8	5.8	5.8	4.1	4.0
t <sub>PLZ</sub>				4.2	4.2	3.6	5.8	5.8	5.8	4.1	4.0

PARAMETER	INPUT	OUTPUT	MAX or MIN	AUC 2.3V	AUCH 1.8V	AUCH 2.3V
t <sub>PLH</sub>	A	Y	MAX	1.8	1.8	1.8
t <sub>PHL</sub>				1.8	1.8	1.8
t <sub>PZH</sub>	OE	Y	MAX	1.9	2.5	1.9
t <sub>PZL</sub>				1.9	2.5	1.9
t <sub>PHZ</sub>	OE	Y	MAX	2	4.0	2
t <sub>PLZ</sub>				2	4.0	2

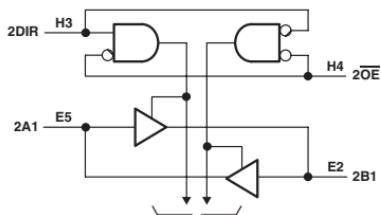
UNIT: ns

## 32-BIT BUS TRANSCEIVER WITH 3-STATE OUTPUTS

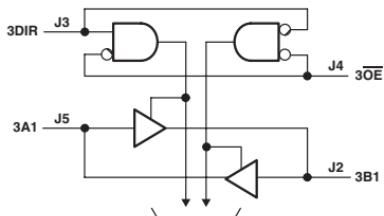
Logic Diagram



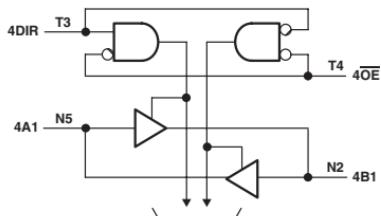
To Seven Other Channels



To Seven Other Channels



To Seven Other Channels



To Seven Other Channels

FUNCTION TABLE  
(each 9-bit section)

INPUTS	OPERATION
OE	DIR
L	L
L	H
H	X

B data to A bus  
A data to B bus  
Isolation

## ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	ABT	ABTH	LVTH 3V	LVC 3V	LVCH 3V	LVCHR 3V	LVCR 3V	LV CZ 3V	ALVCH 3V	AUC 1.8V	AUC 2.3V	UNIT
I <sub>CC</sub>	MAX	20	20	10	0.02	0.04	0.04	0.02	0.12	0.08	0.04	0.04	mA
I <sub>OH</sub>	MAX	-32	-32	-32	-24	-24	-12	-12	-24	-24	-8	-9	mA
I <sub>OL</sub>	MAX	64	64	64	24	24	12	12	24	24	8	9	mA

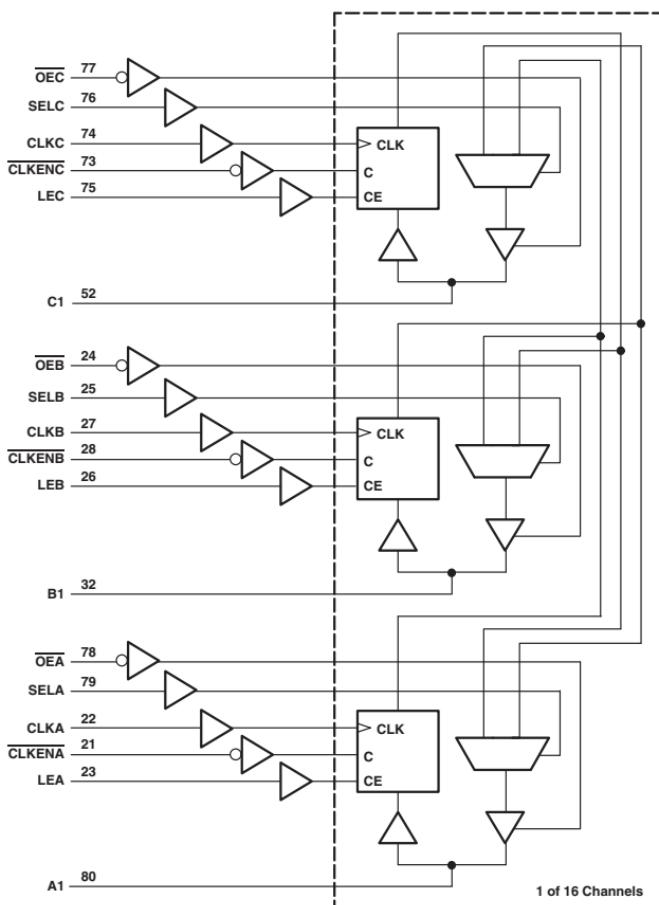
## SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	ABT	ABTH	LVTH 3V	LVC 3V	LVCH 3V	LVCHR 3V	LVCR 3V	LV CZ 3V
I <sub>PLH</sub>	A or B	B or A	MAX	5	5	3.3	4	4	4.8	4.8	4.0
I <sub>PHL</sub>				5.2	5.2	3.3	4	4	4.8	4.8	4.0
I <sub>PZH</sub>	$\overline{OE}$	B or A	MAX	7.3	7.3	4.5	5.5	5.5	6.3	6.3	5.6
I <sub>PZL</sub>				8.1	8.1	4.6	5.5	5.5	6.3	6.3	5.6
I <sub>PHZ</sub>	$\overline{OE}$	B or A	MAX	6.5	6.5	5.1	6.6	6.6	7.4	7.4	6.6
I <sub>PZL</sub>				6.9	6.9	5.1	6.6	6.6	7.4	7.4	6.6

PARAMETER	INPUT	OUTPUT	MAX or MIN	ALVCH 3V	AUC 1.8V	AUC 2.3V
I <sub>PLH</sub>	A or B	B or A	MAX	3	2.0	1.9
I <sub>PHL</sub>				3	2.0	1.9
I <sub>PZH</sub>	$\overline{OE}$	B or A	MAX	4.4	3.1	2.6
I <sub>PZL</sub>				4.4	3.1	2.6
I <sub>PHZ</sub>	$\overline{OE}$	B or A	MAX	4.1	4.8	2.9
I <sub>PZL</sub>				4.1	4.8	2.9

UNIT: ns

Logic Diagram



**FUNCTION TABLE**  
**STORAGE†**

INPUTS				OUTPUT
CLKENA	CLKA	LEA	A	
H	X	L	X	Q0‡
L	↑	L	L	L
L	↑	L	H	H
X	H	L	X	Q0‡
X	L	L	X	Q0‡
X	X	H	L	L
X	X	H	H	H

† A-port register shown. B and C ports are similar but use CLKENB, CLKENC, CLKB, CLKC, LEB, and LEC.  
‡ Output level before the indicated steady-state input conditions were established.

**A-PORT OUTPUT**

INPUTS		OUTPUT A
OEA	SEL A	
H	X	Z
L	H	Output of C register
L	L	Output of B register

**B-PORT OUTPUT**

INPUTS		OUTPUT B
OEB	SEL B	
H	X	Z
L	H	Output of B register
L	L	Output of C register

**C-PORT OUTPUT**

INPUTS		OUTPUT C
OEC	SEL C	
H	X	Z
L	H	Output of B register
L	L	Output of A register

**ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS**

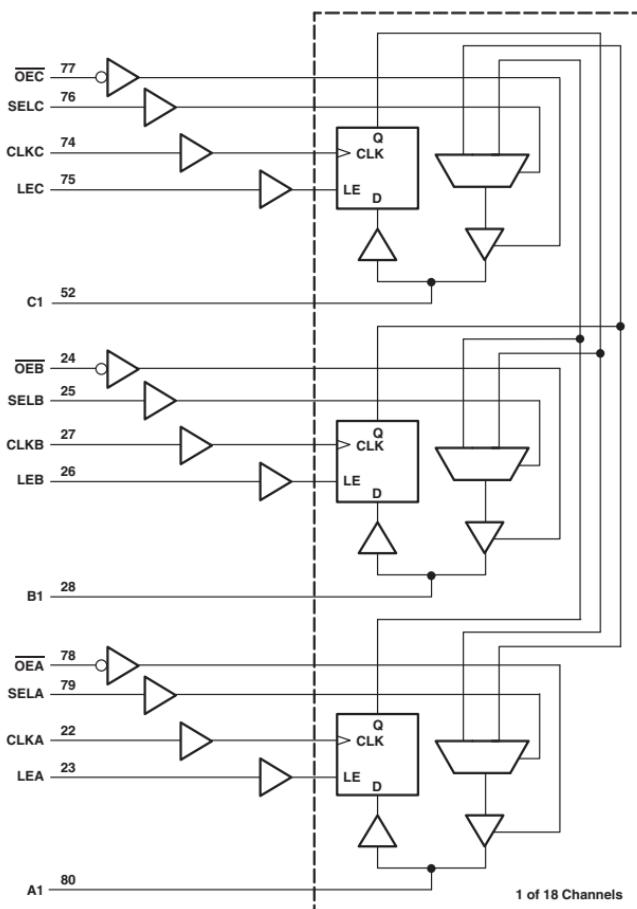
PARAMETER	MAX or MIN	ABTH	UNIT
I <sub>CC</sub>	MAX	40	mA
I <sub>DH</sub>	MAX	-32	mA
I <sub>OL</sub>	MAX	64	mA

**TIMING REQUIREMENTS AND SWITCHING CHARACTERISTICS**

PARAMETER	INPUT	OUTPUT	MAX or MIN	ABTH
f <sub>max</sub>			MIN	150
t <sub>w</sub>	Pulse duration	LE high CLK high or low	MIN MIN	3.3 3.3
t <sub>su</sub>	Setup time	A, B, or C before CLK ↑ A or B before LE ↓ CLKEN before CLK ↑	MIN MIN MIN	2.4 2.1 3.2
t <sub>h</sub>	Hold time	A, B, or C after CLK ↑ A or B after LE ↓ CLKEN after CLK ↑	MIN MIN MIN	1.4 2.1 1.1
t <sub>PLH</sub>		A, B, or C	MAX	6.1
t <sub>PHL</sub>				6.6
t <sub>PLH</sub>		SEL	MAX	6.5
t <sub>PHL</sub>				6.5
t <sub>PLH</sub>		LE	MAX	7.5
t <sub>PHL</sub>				6.9
t <sub>PLH</sub>		CLK	MAX	7.5
t <sub>PHL</sub>				6.7
t <sub>PZH</sub>		OE	MAX	6.4
t <sub>PZL</sub>				6.8
t <sub>PHZ</sub>		OE	MAX	6
t <sub>PZL</sub>				6.1

UNIT f<sub>max</sub> : MHz other : ns

Logic Diagram



**FUNCTION TABLE  
STORAGE†**

INPUTS			OUTPUT
CLKA	LEA	A	
↑	L	L	L
↑	L	H	H
H	L	X	Q0‡
L	L	X	Q0‡
X	H	L	L
X	H	H	H

† A-port register shown, B and C ports are similar but use CLKB, CLKC, LEB, and LEC.  
‡ Output level before the indicated steady-state input conditions were established.

**A-PORT OUTPUT**

INPUTS		OUTPUT A
OEA	SEL A	
H	X	Z
L	H	Output of C register
L	L	Output of B register

**B-PORT OUTPUT**

INPUTS		OUTPUT B
OEB	SEL B	
H	X	Z
L	H	Output of A register
L	L	Output of C register

**C-PORT OUTPUT**

INPUTS		OUTPUT C
OEC	SEL C	
H	X	Z
L	H	Output of B register
L	L	Output of A register

**ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS**

PARAMETER	MAX or MIN	ABTH	UNIT
I <sub>CC</sub>	MAX	45	mA
I <sub>OH</sub>	MAX	-32	mA
I <sub>OL</sub>	MAX	64	mA

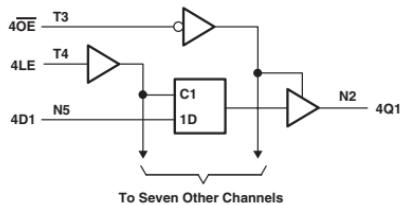
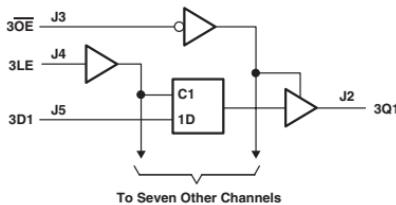
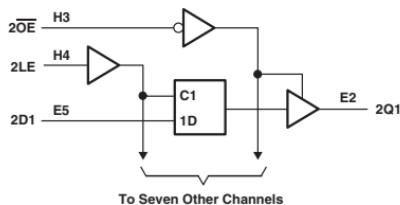
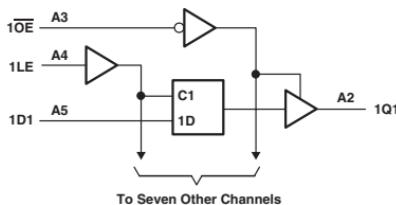
**TIMING REQUIREMENTS AND SWITCHING CHARACTERISTICS**

PARAMETER	INPUT	OUTPUT	MAX or MIN	ABTH
f <sub>max</sub>			MIN	150
t <sub>W</sub> Pulse duration	LE high		MIN	3.3
	CLK high or low		MIN	3.3
t <sub>su</sub> Setup time	A, B, or C before CLK ↑		MIN	2.4
	A, B, or C before LE ↓		MIN	2.1
t <sub>h</sub> Hold time	A, B, or C after CLK ↑		MIN	1.4
	A, B, or C after LE ↓		MIN	2.1
t <sub>PLH</sub>	A, B, or C	C, B, or A	MAX	6.1
t <sub>PHL</sub>				6.6
t <sub>PLH</sub>	SEL	A, B, or C	MAX	6.5
t <sub>PHL</sub>				6.5
t <sub>PLH</sub>	LE	A, B, or C	MAX	7.5
t <sub>PHL</sub>				6.9
t <sub>PLH</sub>	CLK	A, B, or C	MAX	7.4
t <sub>PHL</sub>				6.7
t <sub>ZH</sub>	OE	A, B, or C	MAX	6.8
t <sub>PLZ</sub>				7.1
t <sub>HZ</sub>	OE	A, B, or C	MAX	6.2
t <sub>PLZ</sub>				6

UNIT f<sub>max</sub> : MHz other : ns

## 32-BIT TRANSPARENT D-TYPE LATCH WITH 3-STATE OUTPUTS

Logic Diagram



FUNCTION TABLE

INPUTS			OUTPUT
OE	LE	D	Q
L	H	H	H
L	H	L	L
L	L	X	$Q_0$
H	X	X	Z

## ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	LVTH 3V	ALVTH 3V	LVC 3V	LVCH 3V	UNIT
I <sub>CC</sub>	MAX	10	5	0.04	0.04	mA
I <sub>OH</sub>	MAX	-32	-32	-24	-24	mA
I <sub>OL</sub>	MAX	64	64	24	24	mA

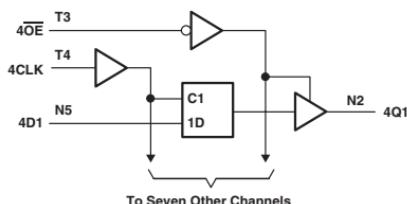
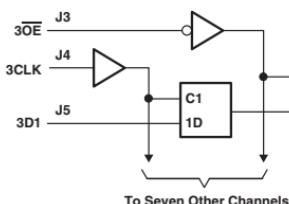
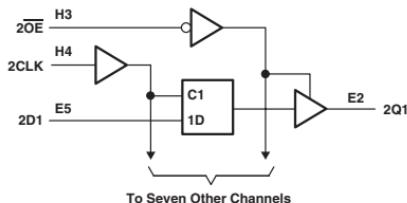
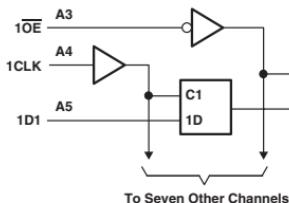
## TIMING REQUIREMENTS AND SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	LVTH 3V	ALVTH 3V	LVC 3V	LVCH 3V
t <sub>w</sub> Pulse duration, LE high or low			MIN	3	1.5	3.3	3.3
t <sub>su</sub> Setup time	Data before LE ↓, data high		MIN	1	1.4	1.7	1.7
	Data before LE ↓, data low		MIN	1	0.9	1.7	1.7
t <sub>h</sub> Hold time	Data after LE ↓, data high		MIN	1	0.9	1.2	1.2
	Data after LE ↓, data low		MIN	1	1.4	1.2	1.2
t <sub>PLH</sub>	D	Q	MAX	3.8	3.1	4.2	4.2
t <sub>PHL</sub>				3.6	3.3	4.2	4.2
t <sub>PLH</sub>	LE	Q	MAX	4.3	3.3	4.6	4.6
t <sub>PHL</sub>				4	3.5	4.6	4.6
t <sub>PZH</sub>	OE	Q	MAX	4.3	4	4.7	4.7
t <sub>PZL</sub>				4.3	3.4	4.7	4.7
t <sub>PHZ</sub>	OE	Q	MAX	5	4.9	5.9	5.9
t <sub>PZL</sub>				4.7	4.5	5.9	5.9

UNIT: ns

## 32-BIT EDGE-TRIGGERED D-TYPE FLIP-FLOP WITH 3-STATE OUTPUTS

Logic Diagram



**FUNCTION TABLE**  
(each flip-flop)

INPUTS			OUTPUT Q
OE	CLK	D	
L	↑	H	H
L	↑	L	L
L	H or L	X	Q <sub>0</sub>
H	X	X	Z

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	LVTH 3V	ALVTH 3V	LVC 3V	LVCH 3V	ALVCH 3V	AUC 1.8V	AUC 2.3V	AUCH 1.8V	AUCH 2.3V	UNIT
I <sub>CC</sub>	MAX	10	5	0.04	0.04	0.08	0.04	0.04	0.04	0.04	mA
I <sub>OH</sub>	MAX	-32	-32	-24	-24	-24	-8	-9	-8	-9	mA
I <sub>OL</sub>	MAX	64	64	24	24	24	8	9	8	9	mA

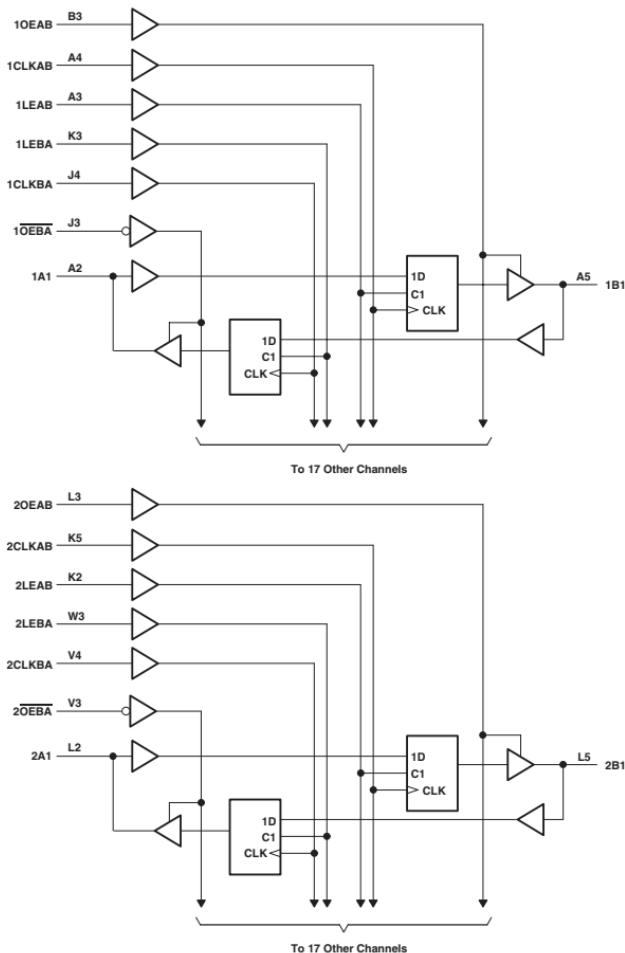
TIMING REQUIREMENTS AND SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	LVTH 3V	ALVTH 3V	LVC 3V	LVCH 3V	ALVCH 3V	AUC 1.8V	AUC 2.3V
f <sub>max</sub>				160	250	150	150	150	250	250
t <sub>W</sub> Pulse duration, CLK high or low			MIN	3	1.5	3.3	3.3	1.9	1.9	1.9
t <sub>WS</sub> Setup time	Data before CLK ↑ , data high		MIN	1.8	1	1.9	1.9	1.9	0.6	0.6
	Data before CLK ↑ , data low		MIN	1.8	1.5	1.9	1.9	1.9	0.6	0.6
t <sub>WH</sub> Hold time	Data after CLK ↑ , data high		MIN	0.8	0.5	1.9	1.1	0.5	0.4	0.4
	Data after CLK ↑ , data low		MIN	0.8	1	1.9	1.1	0.5	0.4	0.4
t <sub>PLH</sub>	CLK	Q	MAX	4.5	3.2	4.5	4.5	4.2	2.8	2.2
t <sub>PHL</sub>			4	3.2	4.5	4.5	4.2	2.8	2.2	
t <sub>PZH</sub>	$\overline{OE}$	Q	MAX	4.5	3.8	4.6	4.6	4.8	2.9	2.2
t <sub>PZL</sub>			4.4	3.3	4.6	4.6	4.8	2.9	2.2	
t <sub>PHZ</sub>	$\overline{OE}$	Q	MAX	5	4.6	5.5	5.5	4.3	4.5	2.2
t <sub>PZL</sub>			4.6	4.2	5.5	5.5	4.3	4.5	2.2	

PARAMETER	INPUT	OUTPUT	MAX or MIN	AUCH 1.8V	AUCH 2.3V
f <sub>max</sub>				250	250
t <sub>W</sub> Pulse duration, CLK high or low			MIN	1.9	1.9
t <sub>WS</sub> Setup time	Data before CLK ↑ , data high		MIN	0.6	0.6
	Data before CLK ↑ , data low		MIN	0.6	0.6
t <sub>WH</sub> Hold time	Data after CLK ↑ , data high		MIN	0.4	0.4
	Data after CLK ↑ , data low		MIN	0.4	0.4
t <sub>PLH</sub>	CLK	Q	MAX	2.8	2.2
t <sub>PHL</sub>			2.8	2.2	
t <sub>PZH</sub>	$\overline{OE}$	Q	MAX	2.9	2.2
t <sub>PZL</sub>			2.9	2.2	
t <sub>PHZ</sub>	$\overline{OE}$	Q	MAX	4.5	2.2
t <sub>PZL</sub>			4.5	2.2	

UNIT f<sub>max</sub> : MHz other : ns

Logic Diagram



**FUNCTION TABLE†**

INPUTS				OUTPUT
OEAB	LEAB	CLKAB	A	B
L	X	X	X	Z
H	H	X	L	L
H	H	X	H	H
H	L	↑	L	L
H	L	↑	H	H
H	L	H	X	B0‡
H	L	L	X	B0§

† A-to-B data flow is shown; B-to-A flow is similar but uses OEBA, LEBA, and CLKBA.

‡ Output level before the indicated steady-state input conditions were established.

§ Output level before the indicated steady-state input conditions were established, provided that CLKAB was high before LEAB went low.

**ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS**

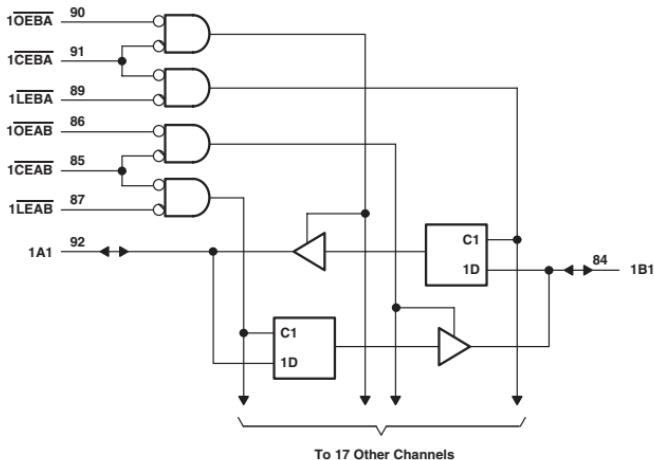
PARAMETER	MAX or MIN	ABTH	ALVCH 3V	UNIT
I <sub>CC</sub>	MAX	90	0.08	mA
I <sub>OH</sub>	MAX	-32	-24	mA
I <sub>OL</sub>	MAX	64	24	mA

**TIMING REQUIREMENTS AND SWITCHING CHARACTERISTICS**

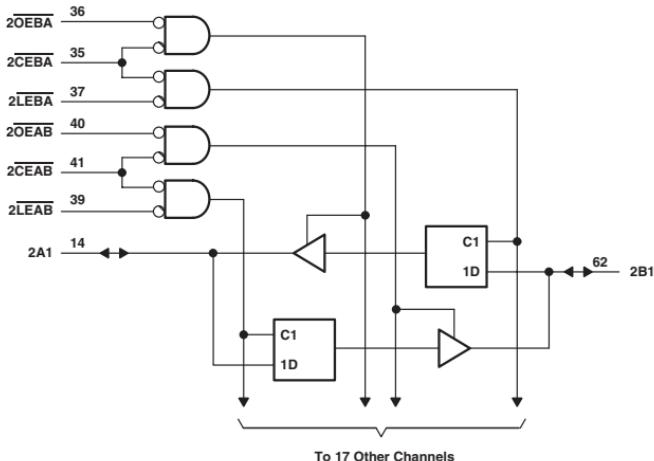
PARAMETER	INPUT	OUTPUT	MAX or MIN	ABTH	ALVCH 3V
f <sub>max</sub>				MIN	150 150
t <sub>w</sub> Pulse duration	LEAB or LEBA high		MIN	3.3	3.3
	CLKAB or CLKBA high or low		MIN	3.3	3.3
t <sub>su</sub> Setup time	A before CLKAB ↑		MIN	3.5	1.7
	B before CLKBA ↑		MIN	3.5	1.7
	A before LEAB ↓ or LEBA ↓ CLK high		MIN	1.6	1.5
	A before LEAB ↓ or LEBA ↓ CLK low		MIN	1.6	1
t <sub>h</sub> Hold time	A after CLKAB ↑ or B after CLKBA ↑		MIN	0	0.7
	A after LEAB ↓ or B after LEBA ↓		MIN	1.6	1.4
t <sub>PLH</sub>	A or B	B or A	MAX	4.8	3.9
t <sub>PHL</sub>				5.4	3.9
t <sub>PZH</sub>	LEAB or LEBA	B or A	MAX	5.3	4.6
t <sub>PZL</sub>				5.5	4.6
t <sub>PHZ</sub>	CLKAB or CLKBA	B or A	MAX	5.3	4.9
t <sub>PLZ</sub>				5.4	4.9
t <sub>PZH</sub>	OEAB	B	MAX	5.6	4.6
t <sub>PZL</sub>				6	4.6
t <sub>PHZ</sub>	OEAB	B	MAX	5.9	5
t <sub>PLZ</sub>				5.6	5
t <sub>PZH</sub>	OEBA	A	MAX	5.6	5
t <sub>PZL</sub>				6	5
t <sub>PHZ</sub>	OEBA	A	MAX	5.9	4.2
t <sub>PLZ</sub>				5.6	4.2

UNIT f<sub>max</sub> : MHz other : ns

Logic Diagram



To 17 Other Channels



To 17 Other Channels

FUNCTION TABLE

INPUTS			OUTPUT
CEAB	LEAB	OEAB	A
H	X	X	X
X	X	H	X
L	H	L	X
L	L	L	L
L	L	H	H

† A-to-B data flow is shown. B-to-A flow conditions

is the same time it uses CEBA, LEBA, and OEBA.

‡ Output level before the indicated steady-state

input conditions were established

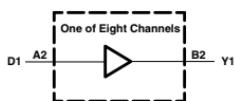
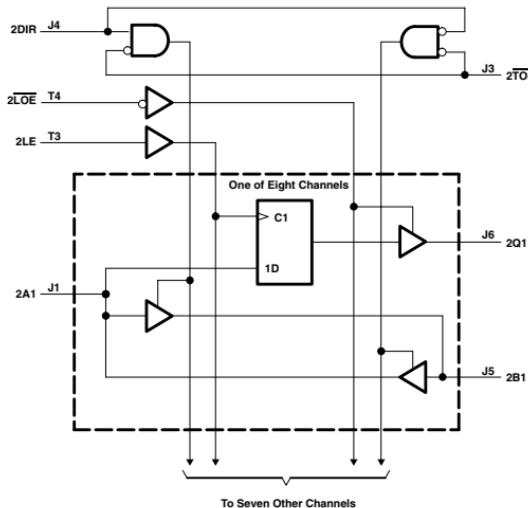
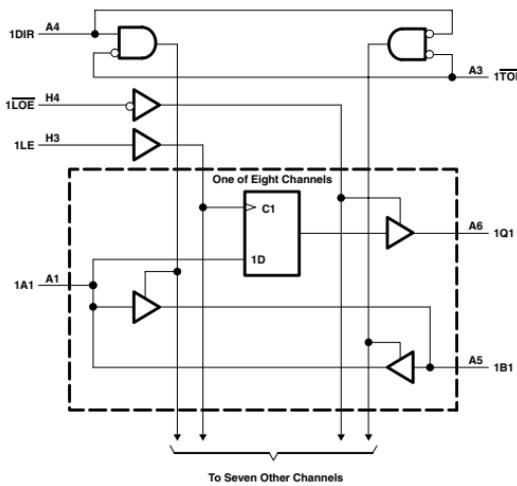
## ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	ABTH	UNIT
I <sub>CC</sub>	MAX	20	mA
I <sub>OH</sub>	MAX	-32	mA
I <sub>OL</sub>	MAX	64	mA

## TIMING REQUIREMENTS AND SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	ABTH
t <sub>W</sub>	Pulse duration, LEAB or LEBA low		MIN	3.3
t <sub>SU</sub>	Data before LEAB ↑ or LEBA ↑		MIN	2.1
	Data before CEAB ↑ or CEBA ↑		MIN	1.7
t <sub>H</sub>	Data after LEAB ↑ or LEBA ↑		MIN	0.6
	Data after CEAB ↑ or CEBA ↑		MIN	0.9
t <sub>PLH</sub>	A or B	B or A	MAX	5.9
t <sub>PLH</sub>				5.7
t <sub>PLH</sub>	LE	A or B	MAX	7.5
t <sub>PLH</sub>				6.6
t <sub>PZH</sub>	CE	A or B	MAX	8
t <sub>PZL</sub>	CE	A or B	MAX	8.8
t <sub>PHZ</sub>	CE	A or B	MAX	7.1
t <sub>PZL</sub>	OE	A or B	MAX	7.5
t <sub>PZH</sub>	OE	A or B	MAX	7.3
t <sub>PZL</sub>	OE	A or B	MAX	8.1
t <sub>PHZ</sub>	OE	A or B	MAX	6.5
t <sub>PZL</sub>				6.9

UNIT: ns

**16-BIT BUS TRANSCEIVER AND TRANSPARENT D-TYPE LATCH WITH EIGHT INDEPENDENT BUFFERS**
**Logic Diagram**


FUNCTION TABLE

INPUTS		OPERATION
TOE	DIR	
L	L	B data to A bus
L	H	A data to B bus
H	X	A bus and B bus Isolation

INPUTS			OUTPUT
LOE	LE	A	Q
L	H	H	H
L	H	L	L
L	L	X	Q <sub>0</sub>
H	X	X	Z

INPUT	OUTPUT
D	Y
L	L
H	H

## ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

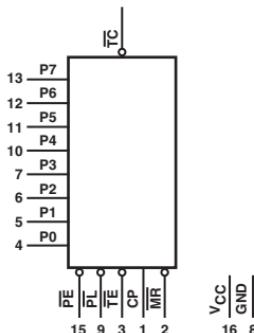
PARAMETER	MAX or MIN	ALVCH 3V	UNIT
I <sub>CC</sub>	MAX	0.06	mA
I <sub>OH</sub>	MAX	-24	mA
I <sub>OL</sub>	MAX	24	mA

## TIMING REQUIREMENTS AND SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	ALVCH 3V
t <sub>pw</sub> Pulse duration	LE high		MIN	2
t <sub>su</sub> Setup time	data before LE ↓		MIN	0.9
t <sub>th</sub> Hold time	data after LE ↓		MIN	0.9
t <sub>PLH</sub>	D	Y	MAX	3
t <sub>PHL</sub>				3
t <sub>PLH</sub>	A	Q	MAX	3
t <sub>PHL</sub>				3
t <sub>PLH</sub>	LE	Q	MAX	3
t <sub>PHL</sub>				3
t <sub>PLH</sub>	A or B	B or A	MAX	3
t <sub>PHL</sub>				3
t <sub>PZH</sub>	LOE	Q	MAX	4.7
t <sub>PZL</sub>				4.7
t <sub>PZH</sub>	TOE	A or B	MAX	4.4
t <sub>PZL</sub>				4.4
t <sub>PZH</sub>	DIR	A or B	MAX	4.7
t <sub>PZL</sub>				4.7
t <sub>PZH</sub>	LOE	Q	MAX	4.1
t <sub>PZL</sub>				4.1
t <sub>PZH</sub>	TOE	A or B	MAX	4.1
t <sub>PZL</sub>				4.1
t <sub>PZH</sub>	DIR	A or B	MAX	4.7
t <sub>PZL</sub>				4.7

UNIT: ns

## 8-STAGE SYNCHRONOUS DOWN COUNTERS



FUNCTION TABLE

CONTROL INPUTS				PRESET MODE	ACTION
MR	PL	PE	TE		
L	X	X	L	Synchronous	Inhibit Counter Count Down
X	H	X	L		Preset On Next Positive Clock Transition
X	X	L	L		Preset Asynchronously
H	L	L	L		Clear to Maximum Count
H	L	H	L		

## ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	CD74 HC	CD74 HCT	UNIT
I <sub>CC</sub>	MAX	0.16	0.16	mA
I <sub>OH</sub>	MAX	-4	-4	mA
I <sub>OL</sub>	MAX	4	4	mA

## TIMING REQUIREMENTS AND SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	CD74 HC	CD74 HCT
<i>t<sub>AV</sub></i>	CP			50	53
	<u>PL</u>		MIN	38	65
	<u>MR</u>			38	53
<i>t<sub>su</sub></i>	P to CP			30	36
	<u>PE</u> to CP		MIN	22	30
	<u>TE</u> to CP			45	60
<i>t<sub>h</sub></i>	P to CP			5	5
	<u>TE</u> to CP		MIN	0	0
	<u>PE</u> to CP			2	2
<i>t<sub>PLH</sub></i>	CP	<u>TC</u> (Async Preset)	MAX	90	90
<i>t<sub>PHL</sub></i>	CP	<u>TC</u> (Sync Preset)	MAX	90	95
<i>t<sub>PLH</sub></i>	<u>TE</u>	<u>TC</u>	MAX	60	75
<i>t<sub>PHL</sub></i>	<u>PL</u>	<u>TC</u>	MAX	60	75
<i>t<sub>PLH</sub></i>	<u>MR</u>	<u>TC</u>	MAX	83	102
<i>t<sub>PHL</sub></i>				83	83
<i>t<sub>PLH</sub></i>				83	83

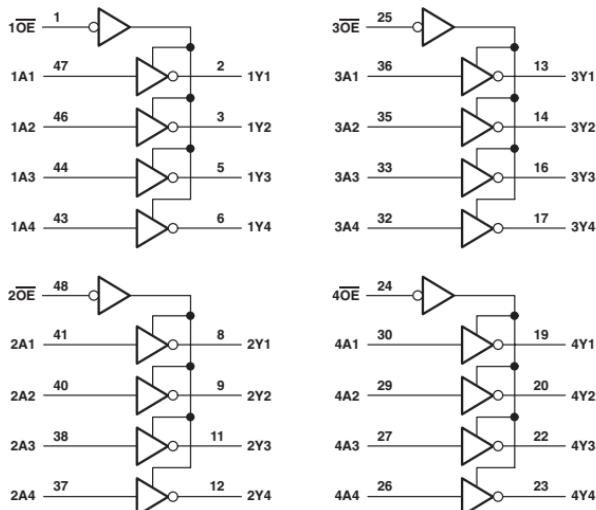
UNIT : ns

# 162240

## 3.3-V ABT 16-BIT BUFFERS/DRIVERS WITH 3-STATE OUTPUTS

- SN74LVT162240, SN74LVTH162240: Output Ports Have Equivalent 22- $\Omega$  Series Resistors

**Logic Diagram**



**FUNCTION TABLE**

INPUTS	OUTPUT	
OE	A	Y
L	H	L
L	L	H
H	X	Z

### ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	LVT 3V	LVTH 3V	UNIT
I <sub>CC</sub>	MAX	5	5	mA
I <sub>OH</sub>	MAX	-12	-12	mA
I <sub>OL</sub>	MAX	12	12	mA

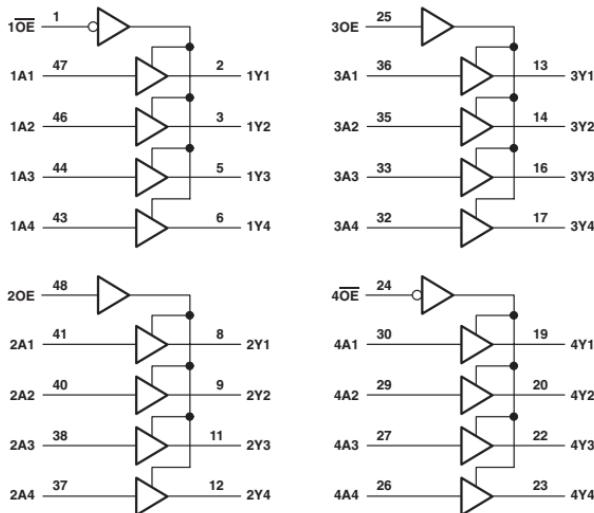
### SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	LVT 3V	LVTH 3V
t <sub>PLH</sub>	A	Y	MAX	4	4
t <sub>PHL</sub>				4	4
t <sub>PZH</sub>	OE	Y	MAX	4.8	4.8
t <sub>PZL</sub>				4.7	4.7
t <sub>PHZ</sub>	OE	Y	MAX	4.7	4.7
t <sub>PZL</sub>				4.5	4.5

UNIT: ns

## 3.3-V ABT 16-BIT BUFFERS/DRIVERS WITH 3-STATE OUTPUTS

Logic Diagram



FUNCTION TABLE

INPUTS		OUTPUT
$1\overline{OE}, 4\overline{OE}$		$1A, 4A$
L	H	H
L	L	L
H	X	Z

INPUTS		OUTPUT
$2\overline{OE}, 3\overline{OE}$		$2A, 3A$
H	H	H
H	L	L
L	X	Z

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	LVTH 3V	UNIT
$I_{CC}$	MAX	5	mA
$I_{OH}$	MAX	-12	mA
$I_{OL}$	MAX	12	mA

SWITCHING CHARACTERISTICS

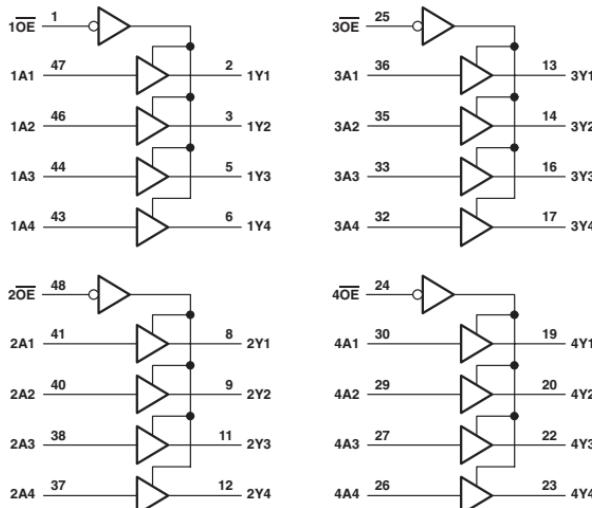
PARAMETER	INPUT	OUTPUT	MAX or MIN	LVTH 3V
$t_{PLH}$	A	Y	MAX	4.1
$t_{PHL}$				4.1
$t_{PZH}$	$\overline{OE}$ or OE	Y	MAX	4.9
$t_{PZL}$				4.8
$t_{PHZ}$	$\overline{OE}$ or OE	Y	MAX	5.3
$t_{PLZ}$				4.9

UNIT: ns

## 16-BIT BUFFERS/DRIVERS WITH 3-STATE OUTPUTS

- SN74ABT162244: Output Ports Have Equivalent 25- $\Omega$  Series Resistors
- SN74LVT162244A, LVTH162244: Output Ports Have Equivalent 22- $\Omega$  Series Resistors
- SN74ALVTH162244: Output Ports Have Equivalent 30- $\Omega$  Series Resistors
- SN74LVC162244A: Output Ports Have Equivalent 26- $\Omega$  Series Resistors
- SN74LVCH162244A: Output Ports Have Equivalent 26- $\Omega$  Series Resistors
- SN74ALVCH162244: Output Ports Have Equivalent 26- $\Omega$  Series Resistors

Logic Diagram

FUNCTION TABLE  
(each 4-bit buffer)

INPUTS	OUTPUT	
OE	A	Y
L	H	H
L	L	L
H	X	Z

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	ABT	LVT 3V	LVTH 3V	ALVTH 3V	LVC 3V	LVCH 3V	ALVCH 3V	UNIT
$I_{CC}$	MAX	30	5	5	5	0.02	0.02	0.04	mA
$I_{OH}$	MAX	-12	-12	-12	-12	-12	-12	-12	mA
$I_{OL}$	MAX	12	12	12	12	12	12	12	mA

SWITCHING CHARACTERISTICS

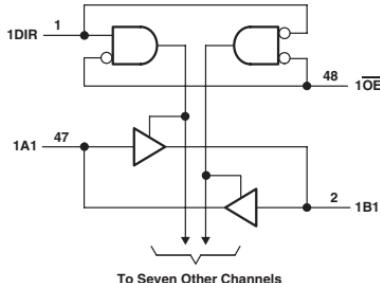
PARAMETER	INPUT	OUTPUT	MAX or MIN	ABT	LVT 3V	LVTH 3V	ALVTH 3V	LVC 3V	LVCH 3V	ALVCH 3V
$t_{PLH}$	A	Y	MAX	3.9	4	4	3.3	4.4	4.4	4.2
$t_{PHL}$				4.8	3.6	3.6	3.3	4.4	4.4	4.2
$t_{PZH}$	$\overline{OE}$	Y	MAX	5.4	5.1	5.1	4.9	5.5	5.5	5.6
$t_{PZL}$				5.1	4.5	4.5	3.3	5.5	5.5	5.6
$t_{PHZ}$	$\overline{OE}$	Y	MAX	4.6	5	5	4.9	6.3	6.3	5.5
$t_{PLZ}$				4.5	5	5	4.3	6.3	6.3	5.5

UNIT: ns

## 16-BIT TRANSCEIVER WITH 3-STATE OUTPUTS

- SN74ABT162245, SN74ABTH162245: A-Port Outputs Have Equivalent 25- $\Omega$  Series Resistors
- SN74LVT162245A, SN74LVTH162245: A-Port Outputs Have Equivalent 22- $\Omega$  Series Resistors
- SN74ALVTH162245: A-Port Outputs Have Equivalent 30- $\Omega$  Series Resistors
- SN74LVC162245: All Outputs Have Equivalent 26- $\Omega$  Series Resistors

Logic Diagram

FUNCTION TABLE  
(each 8-bit section)

INPUTS		OPERATION
OE	DIR	
L	L	B data to A bus
L	H	A data to B bus
H	X	Isolation

## ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	ABT	ABTH	LVT 3V	LVTH 3V	ALVTH 3V	UNIT
I <sub>CC</sub>	MAX	32	32	5	5	5	mA
I <sub>OH</sub> (A port)	MAX	-12	-12	-12	-12	-12	mA
I <sub>OL</sub> (B port)	MAX	-32	-32	-32	-32	-32	mA
I <sub>OL</sub> (A port)	MAX	12	12	12	12	12	mA
I <sub>OL</sub> (B port)	MAX	64	64	64	64	64	mA

## SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	ABT	ABTH	LVT 3V	LVTH 3V	ALVTH 3V
I <sub>PLH</sub>	A	B	MAX	3.9	3.9	3.3	3.3	3.1
I <sub>PLH</sub>				4.2	4.2	3.3	3.3	3
I <sub>PLH</sub>	B	A	MAX	4.6	4.6	4	4	3.7
I <sub>PLH</sub>				5.1	5.1	3.4	3.4	3.4
I <sub>PZH</sub>	$\bar{OE}$	B	MAX	6.3	6.3	4.6	4.6	3.8
I <sub>PZH</sub>				6.4	6.4	4.6	4.6	3.4
I <sub>PZL</sub>	$\bar{OE}$	B	MAX	6.3	6.3	5.2	5.2	4.7
I <sub>PZL</sub>				5.2	5.2	5.1	5.1	4.8
I <sub>PZH</sub>	$\bar{OE}$	A	MAX	7.1	7.1	5.3	5.3	4.7
I <sub>PZH</sub>				7	7	5.1	5.1	3.9
I <sub>PZL</sub>	$\bar{OE}$	A	MAX	6.6	6.6	5.6	5.6	5
I <sub>PZL</sub>				5.7	5.7	5.5	5.5	4.9

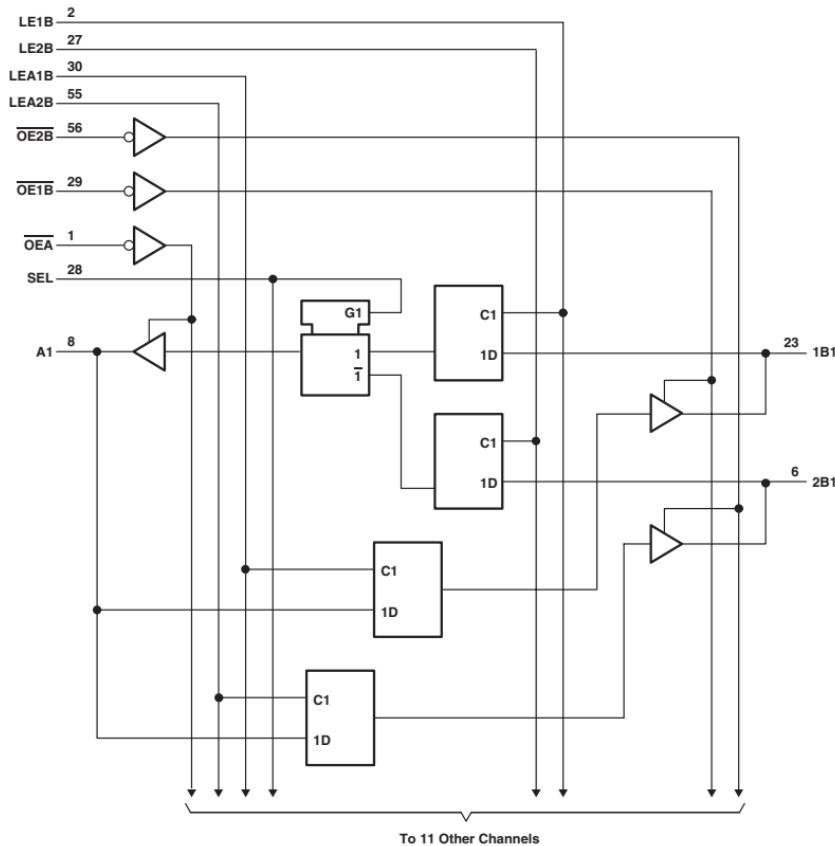
UNIT: ns

# 162260

## 12-BIT TO 24-BIT MULTIPLEXED D-TYPE LATCH WITH 3-STATE OUTPUTS

- SN74ABT162260: B-Port Outputs Have Equivalent  $25\Omega$  Series Resistors
- SN74ALVCH162260: B-Port Outputs Have Equivalent  $26\Omega$  Series Resistors

Logic Diagram



**FUNCTION TABLE**
**B TO A ( $\bar{OE}_B = H$ )**

INPUTS						OUTPUT
1B	2B	SEL	LE1B	LE2B	$\bar{OE}_A$	A
H	X	H	H	X	L	H
L	X	H	H	X	L	L
X	X	H	L	X	L	$A_0$
X	H	L	X	H	L	H
X	L	L	X	H	L	L
X	X	L	X	L	L	$A_0$
X	X	X	X	X	H	Z

**A TO B ( $\bar{OE}_A = H$ )**

INPUTS					OUTPUTS	
A	LEA1B	LEA2B	OE1B	OE2B	1B	2B
H	H	H	L	L	H	H
L	H	H	L	L	L	L
H	H	L	L	L	H	$2B_0$
L	H	L	L	L	L	$2B_0$
H	L	H	L	L	$1B_0$	H
L	L	H	L	L	$1B_0$	L
X	L	L	L	L	$1B_0$	$2B_0$
X	X	X	H	H	Z	Z
X	X	X	L	H	Active	Z
X	X	X	H	L	Z	Active
X	X	X	L	L	Active	Active

**ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS**

PARAMETER	MAX or MIN	ABTH	ALVCH 3V	UNIT
$I_{CC}$	MAX	63	0.04	mA
$I_{OH}$ (A port)	MAX	-32	-24	mA
$I_{OL}$ (B port)	MAX	-32	-12	mA
$I_{OL}$ (A port)	MAX	64	24	mA
$I_{OL}$ (B port)	MAX	12	12	mA

**TIMING REQUIREMENTS AND SWITCHING CHARACTERISTICS**

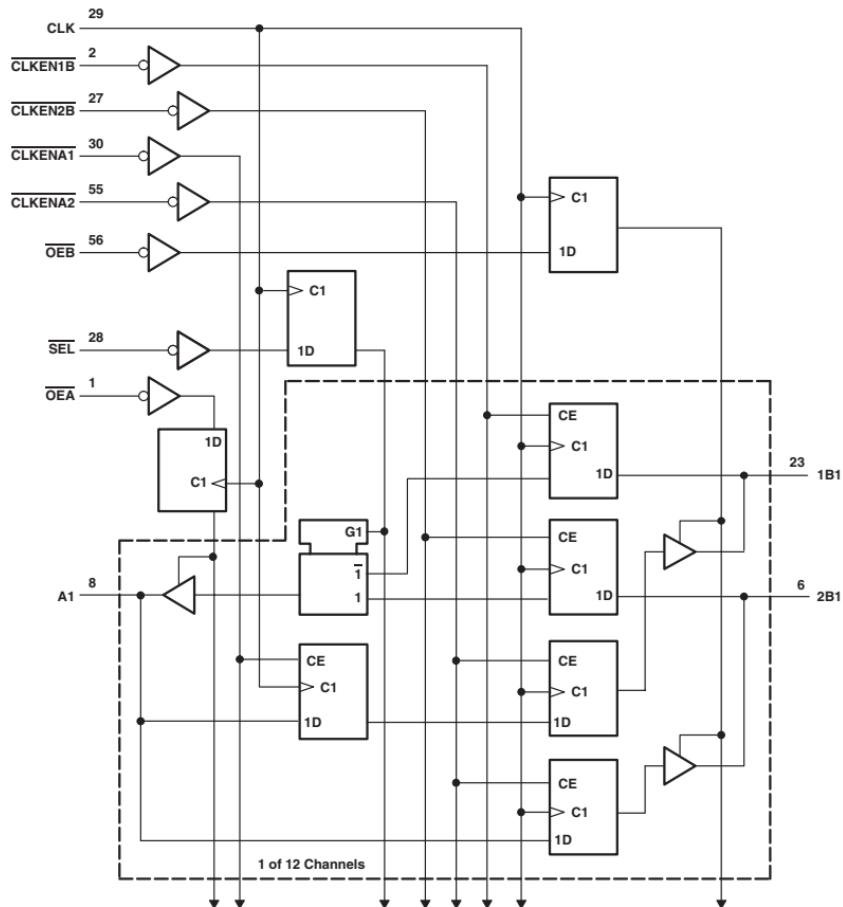
PARAMETER	INPUT	OUTPUT	MAX or MIN	ABTH	ALVCH 3V
$t_{max}$				-	150
$t_W$	Pulse duration, LE1B, LE2B, LEA1B, or LEA2B high		MIN	3.3	3.3
$t_{SU}$	Setup time, data before LE1B, LE2B, LEA1B, or LEA2B ↓		MIN	1.5	1.1
$t_H$	Hold time, data after LE1B, LE2B, LEA1B, or LEA2B ↓		MIN	1	1.5
$t_{PLH}$	A	B	MAX	6.1	4.9
$t_{PHL}$				7.1	4.9
$t_{PLH}$	B	A	MAX	6	4.3
$t_{PHL}$				6.2	4.3
$t_{PLH}$	LE	A	MAX	6.3	4.4
$t_{PHL}$				5.8	4.4
$t_{PLH}$	LE	B	MAX	6.1	5
$t_{PHL}$				7.1	5
$t_{PLH}$	SEL (1B)			MAX	5.6
$t_{PLH}$	SEL (2B)				5.6
$t_{PHL}$	SEL (1B)			MAX	5
$t_{PHL}$	SEL (2B)				5.6
$t_{PZH}$	$\bar{OE}$	A	MAX	6.3	5.4
$t_{PZL}$	$\bar{OE}$			6.5	5.4
$t_{PZH}$	$\bar{OE}$	B	MAX	6.3	6
$t_{PZL}$				8.2	6
$t_{PHZ}$	$\bar{OE}$	A	MAX	6.7	4.6
$t_{PLZ}$				5.2	4.6
$t_{PHZ}$	$\bar{OE}$	B	MAX	7.5	5.1
$t_{PLZ}$				6.2	5.1

UNIT  $t_{max}$  : MHz other : ns

## 12-BIT TO 24-BIT REGISTERED BUS EXCHANGER WITH 3-STATE OUTPUTS

- SN74ALVCH162268: B-Port Outputs Have Equivalent 26- $\Omega$  Series Resistors

Logic Diagram



**FUNCTION TABLE**  
**OUTPUT ENABLE**

INPUTS	OUTPUTS		
CLK	OE <sub>A</sub> OE <sub>B</sub>	A	1B, 2B
↑	H H	Z	Z
↑	H L	Z	Active
↑	L H	Active	Z
↑	L L	Active	Active

**A-TO-B STORAGE (OE<sub>B</sub> = L)**

INPUTS		OUTPUTS	
CLKEN <sub>A1</sub>	CLKEN <sub>A2</sub>	CLK	A
			1B 2B
H	H	X X	1B <sub>0‡</sub> 2B <sub>0‡</sub>
L	X	↑ L	L <sub>t</sub> X
L	X	↑ H	H <sub>t</sub> X
X	L	↑ L	X L
X	L	↑ H	X H

† Two CLK edges are needed to propagate data.

‡ Output level before the indicated steady-state input conditions were established

**B-TO-A STORAGE (OE<sub>A</sub> = L)**

INPUTS						OUTPUT
CLKEN <sub>1B</sub>	CLKEN <sub>2B</sub>	CLK	SEL	1B	2B	A
H	X	X	H	X	X	A <sub>0‡</sub>
X	H	X	L	X	X	A <sub>0‡</sub>
L	X	↑ H	H	X	X	L
L	X	↑ H	L	X	X	H
X	L	↑ L	X	L	L	L
X	L	↑ L	X	X	H	H

‡ Output level before the indicated steady-state input conditions were established

**ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS**

PARAMETER	MAX or MIN	ALVCH 3V	UNIT
I <sub>cc</sub>	MAX	0.04	mA
I <sub>oh</sub> (A port)	MAX	-24	mA
I <sub>oh</sub> (B port)	MAX	-12	mA
I <sub>ol</sub> (A port)	MAX	24	mA
I <sub>ol</sub> (B port)	MAX	12	mA

**TIMING REQUIREMENTS AND SWITCHING CHARACTERISTICS**

PARAMETER	INPUT	OUTPUT	MAX or MIN	ALVCH 3V
f <sub>max</sub>			MIN	150
t <sub>W</sub> Pulse duration, CLK high or low			MIN	3.3
t <sub>su</sub> Setup time	A data before CLK ↑		MIN	3.4
	B data before CLK ↑		MIN	1
	SEL before CLK ↑		MIN	1.3
	CLKEN <sub>A1</sub> or CLKEN <sub>A2</sub> before CLK ↑		MIN	2.8
	CLKEN <sub>B1</sub> or CLKEN <sub>B2</sub> before CLK ↑		MIN	2.5
	OE before CLK ↑		MIN	3.2
t <sub>h</sub> Hold time	A data after CLK ↑		MIN	0.2
	B data after CLK ↑		MIN	1.3
	SEL after CLK ↑		MIN	1
	CLKEN <sub>A1</sub> or CLKEN <sub>A2</sub> after CLK ↑		MIN	0.4
	CLKEN <sub>B1</sub> or CLKEN <sub>B2</sub> after CLK ↑		MIN	0.5
	OE after CLK ↑		MIN	0.2
t <sub>pd</sub>	CLK	B		5.4
		A (1B)	MAX	4.8
		A (2B)		4.8
		A (SEL)		5.8
t <sub>sn</sub>	CLK	B	MAX	6.1
		A		5.1
t <sub>dis</sub>	CLK	B	MAX	5.9
		A		5

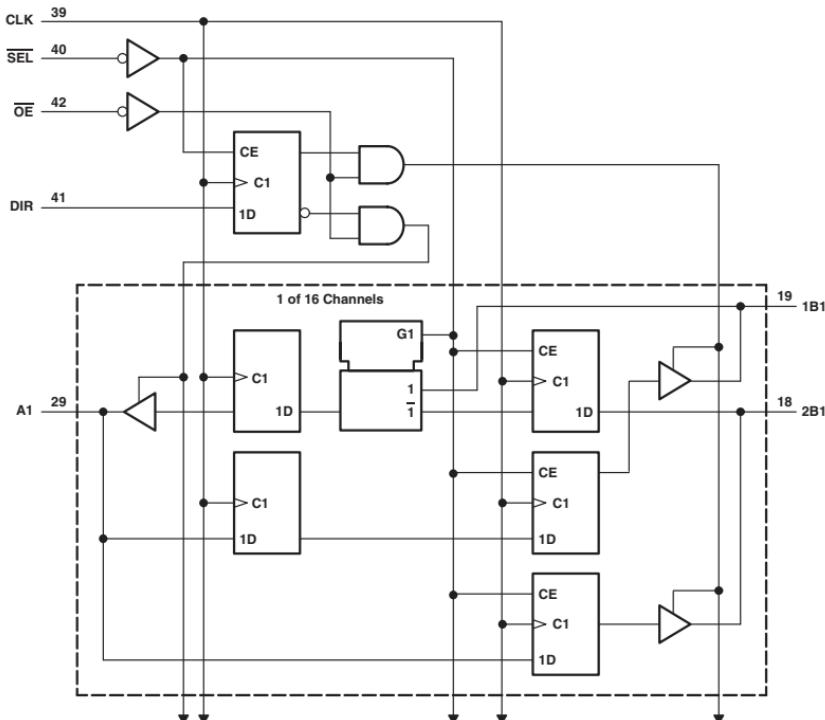
UNIT f<sub>max</sub> : MHz other : ns

# 162280

## 16-BIT TO 32-BIT REGISTERED BUS EXCHANGER WITH BYTE MASKS AND 3-STATE OUTPUTS

- SN74ALVCHG162280: A-Port Outputs Have Equivalent 50- $\Omega$  Series Resistors
- B-Port Outputs Have Equivalent 20- $\Omega$  Series Resistors

Logic Diagram



**FUNCTION TABLE**
**A-TO-B STORAGE ( $\overline{OE} = L$ ,  $DIR = H$ )**

INPUTS			OUTPUTS	
SEL	CLK	A	1B	2B
H	X	X	1B <sup>†</sup>	2B <sup>†</sup>
L	L	L	L <sup>‡</sup>	X
L	H	H	H <sup>‡</sup>	X

<sup>†</sup> Output level before indicated steady-state input conditions were established  
<sup>‡</sup> Two CLK edges are needed to propagate the data.

**B-TO-A STORAGE ( $\overline{OE} = L$ ,  $DIR = L$ )**

INPUTS			OUTPUT	
CLK	SEL	1B	2B	A
↑	H	X	L	L <sup>§</sup>
↑	H	X	H	H <sup>§</sup>
↑	L	L	X	L
↑	L	H	X	H

<sup>§</sup> Two CLK edges are needed to propagate the data. The data is loaded in the first register when SEL is low and propagates to the second register when SEL is high.

**C-TO-D STORAGE ( $\overline{OE} = L$ )**

INPUTS			OUTPUT	
SEL	CLK	C	1D	2D
H	X	X	1B <sup>†</sup>	2B <sup>†</sup>
L	↑	L	L <sup>‡</sup>	L

<sup>†</sup> Output level before indicated steady-state input conditions were established  
<sup>‡</sup> Two CLK edges are needed to propagate the data.

**OUTPUT ENABLE**

INPUTS			OUTPUT		
CLK	OE	DIR	A	1B, 2B	1D, 2D
↑	H	X	Z	Z	Z
↑	L	H	Z	Active	Active
↑	L	L	Active	Z	Active

**ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS**

PARAMETER	MAX or MIN	ALVCHG 3V	UNIT
I <sub>CC</sub>	MAX	0.04	mA
I <sub>OH(A to B)</sub>	MAX	8	mA
I <sub>OL(B to A)</sub>	MAX	6	mA
I <sub>OL(A to B)</sub>	MAX	8	mA
I <sub>OL(B to A)</sub>	MAX	6	mA

**TIMING REQUIREMENTS AND SWITCHING CHARACTERISTICS**

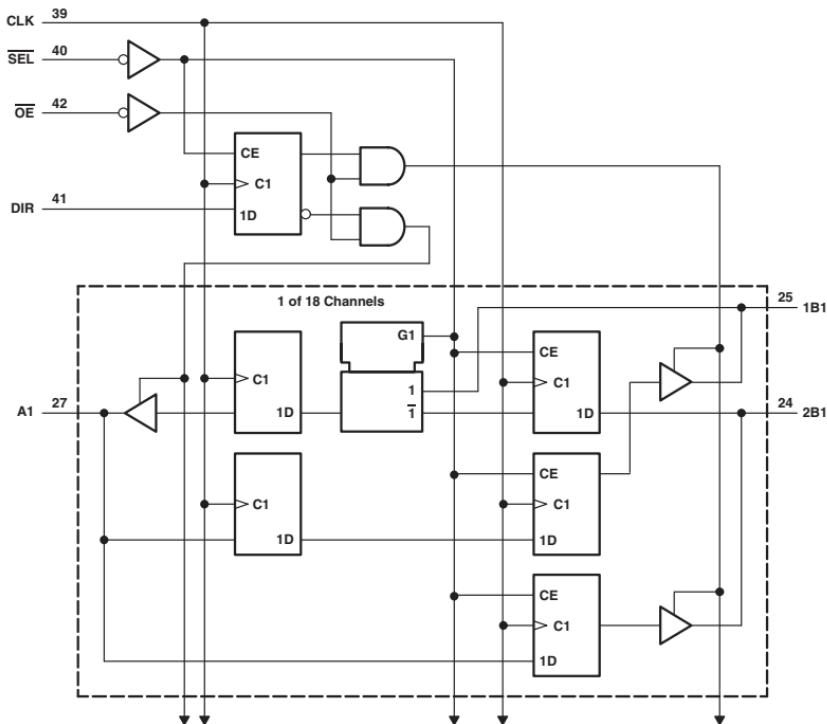
PARAMETER	INPUT	OUTPUT	MAX or MIN	ALVCHG 3V
f <sub>max</sub>			MIN	160
t <sub>w</sub>	Pulse duration, CLK high or low		MIN	2.3
t <sub>su</sub>	A data before CLK ↑ , high or low		MIN	1.4
	B data before CLK ↑ , high or low		MIN	2
	C data before CLK ↑ , high or low		MIN	1.3
	DIR before CLK ↑ , high or low		MIN	2
	SEL before CLK ↑ , high or low		MIN	2
t <sub>th</sub>	A data after CLK ↑ , high or low		MIN	0.3
	B data after CLK ↑ , high or low		MIN	0.3
	C data after CLK ↑ , high or low		MIN	0.3
	DIR after CLK ↑ , high or low		MIN	0.3
	SEL after CLK ↑ , high or low		MIN	0.3
t <sub>pd</sub>	CLK	A		5
		B	MAX	7.4
		D		7.2
t <sub>en</sub>	CLK	A	MAX	6.2
		B		9.4
	OE	A		6
t <sub>dis</sub>	CLK	B	MAX	9.5
		D		7.9
	OE	A	MAX	6.4
		B		7.8
		A		5
		B	MAX	7.6
		D		6.7

 UNIT f<sub>max</sub> : MHz other : ns

## 18-BIT TO 36-BIT REGISTERED BUS EXCHANGER WITH 3-STATE OUTPUTS

- SN74ALVCHG162282: A-Port Outputs Have Equivalent 50- $\Omega$  Series Resistors
- B-Port Outputs Have Equivalent 20- $\Omega$  Series Resistors

Logic Diagram



**FUNCTION TABLE**
**A-TO-B STORAGE  
( $\overline{OE} = L$ ,  $DIR = H$ )**

INPUTS		OUTPUTS	
SEL	CLK	A	1B 2B
H	X	X	$1B_0^T$ $2B_0^T$
L	↑	L	$L^T$ L
L	↑	H	$H^T$ H

† Output level before indicated steady-state input conditions were established.

‡ Two CLK edges are needed to propagate the data.

**B-TO-A STORAGE**
**( $\overline{OE} = L$ ,  $DIR = L$ )**

INPUTS		OUTPUT	
CLK	SEL	1B	2B
↑	H	X	L
↑	H	X	$H^S$
↑	L	L	X
↑	L	H	X
			H

§ Two CLK edges are needed to propagate the data. The data is loaded in the first register when SEL is low, and prepares to the second register when SEL is high.

**OUTPUT ENABLE**

INPUTS			OUTPUTS	
CLK	$\overline{OE}$	DIR	A	1B, 2B
↑	H	X	Z	Z
↑	L	H	Z	Active
↑	L	L	Active	Z

**ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS**

PARAMETER	MAX or MIN	ALVCHG 3V	UNIT
$I_{CC}$	MAX	0.04	mA
$I_{OH}(A \text{ to } B)$	MAX	8	mA
$I_{OL}(B \text{ to } A)$	MAX	6	mA
$I_{OL}(A \text{ to } B)$	MAX	8	mA
$I_{OL}(B \text{ to } A)$	MAX	6	mA

**TIMING REQUIREMENTS AND SWITCHING CHARACTERISTICS**

PARAMETER	INPUT	OUTPUT	MAX or MIN	ALVCHG 3V
$t_{max}$			MIN	160
$t_{w}$	Pulse duration, CLK high or low		MIN	2.3
$t_{hu}$	A data before CLK ↑		MIN	1.5
	B data before CLK ↑		MIN	2
	DIR before CLK ↑		MIN	2
	SEL before CLK ↑		MIN	2
$t_{hl}$	A data after CLK ↑		MIN	0.3
	B data after CLK ↑		MIN	0.3
	DIR after CLK ↑		MIN	0.3
	SEL after CLK ↑		MIN	0.3
$t_{pd}$	CLK	A	MAX	5
		B		7.4
$t_{en}$	CLK	A	MAX	6.3
		B		9.4
	$\overline{OE}$	A	MAX	6
		B		9.5
$t_{dis}$	CLK	A	MAX	6.4
		B		7.8
	$\overline{OE}$	A	MAX	5
		B		7.6

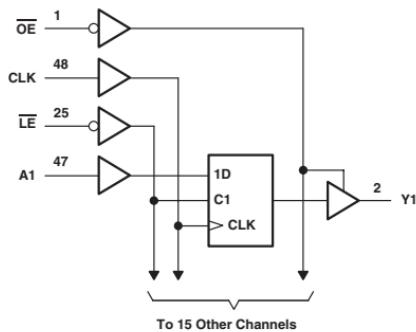
 UNIT  $t_{max}$  : MHz other : ns

# 162334

## 16-BIT UNIVERSAL BUS DRIVER WITH 3-STATE OUTPUTS

- SN74ALVC162334: Output Ports Have Equivalent 26- $\Omega$  Series Resistors
- SN74ALVCH162334: Output Port Has Equivalent 26- $\Omega$  Series Resistors

Logic Diagram



FUNCTION TABLE

INPUTS			OUTPUT	
OE	LE	CLK	A	Y
H	X	X	X	Z
L	L	X	L	L
L	L	X	H	H
L	H	↑	L	L
L	H	↑	H	H
L	H	L or H	X	$Y_0 \dagger$

† Output level before the indicated steady-state input conditions were established

## ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	ALVC 3V	ALVCH 3V	UNIT
I <sub>CC</sub>	MAX	0.04	0.04	mA
I <sub>OH</sub>	MAX	-12	-12	mA
I <sub>OL</sub>	MAX	12	12	mA

## TIMING REQUIREMENTS AND SWITCHING CHARACTERISTICS

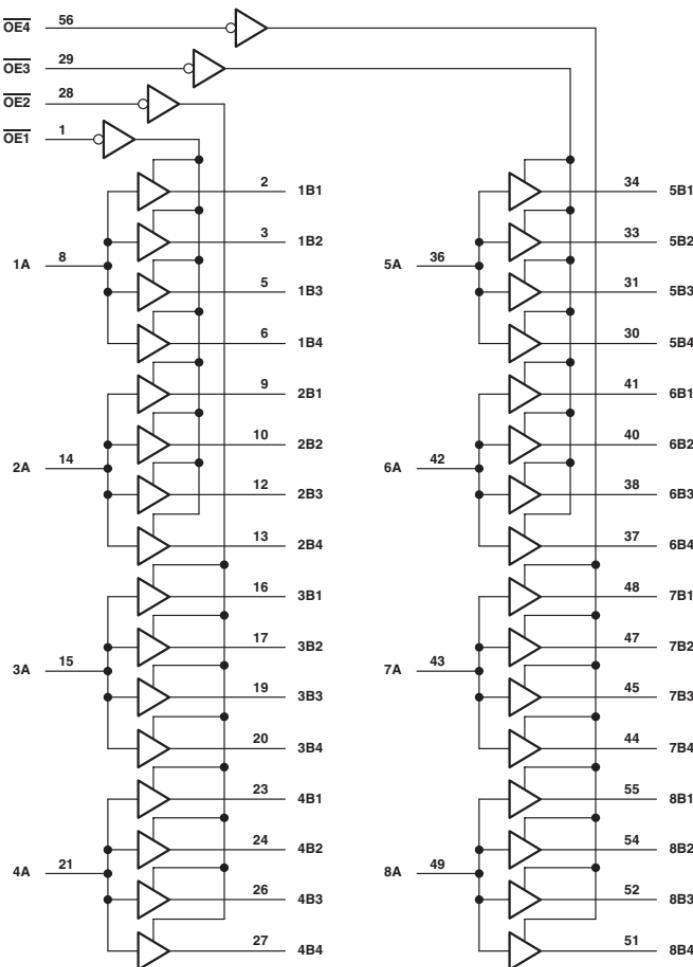
PARAMETER	INPUT	OUTPUT	MAX or MIN	ALVC 3V	ALVCH 3V
f <sub>max</sub>			MIN	150	150
t <sub>W</sub> Pulse duration	LE low			3.3	3.3
	CLK high or low		MIN	3.3	3.3
t <sub>W</sub> Setup time	Data before CLK ↑		MIN	1.5	1.5
	Data before LE ↑ CLK high		MIN	1.3	1.3
	Data before LE ↑ CLK low		MIN	1.2	1.2
t <sub>H</sub> Hold time	Data after CLK ↑		MIN	0.9	0.9
	Data after LE ↑ CLK high		MIN	1.1	1.1
	Data after LE ↑ CLK low		MIN	1.1	1.1
t <sub>pd</sub>	A		MAX	3.9	3.9
	LE	Y		5	5
	CLK		MAX	4.9	4.9
t <sub>en</sub>	OE	Y		5.4	5.4
t <sub>dis</sub>	OE	Y	MAX	5	5

UNIT f<sub>max</sub> : MHz other : ns

## 1-BIT TO 4-BIT ADDRESS DRIVER WITH 3-STATE OUTPUTS

- SN74ALVCH162344: Output Ports Have Equivalent 26- $\Omega$  Series Resistors

Logic Diagram



**FUNCTION TABLE**

INPUTS		OUTPUT
OE	A	Bn
L	H	H
L	L	L
H	X	Z

**ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS**

PARAMETER	MAX or MIN	ALVCH 3V	UNIT
I <sub>CC</sub>	MAX	0.04	mA
I <sub>OH</sub>	MAX	-12	mA
I <sub>OL</sub>	MAX	12	mA

**SWITCHING CHARACTERISTICS**

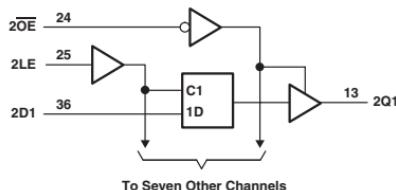
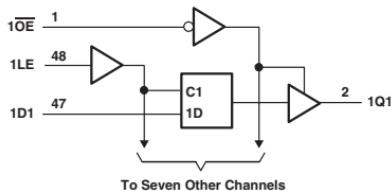
PARAMETER	INPUT	OUTPUT	MAX or MIN	ALVCH 3V
t <sub>PLH</sub>	A	B	MAX	4.4
t <sub>PHL</sub>				4.4
t <sub>PZH</sub>	OE	B	MAX	5.7
t <sub>PZL</sub>				5.7
t <sub>PHZ</sub>	OE	B	MAX	4.5
t <sub>PZL</sub>				4.5

UNIT: ns

## 3.3-V ABT 16-BIT TRANSPARENT D-TYPE LATCHES WITH 3-STATE OUTPUTS

- SN74LVTH162373: Output Ports Have Equivalent 22- $\Omega$  Series Resistors

Logic Diagram

FUNCTION TABLE  
(each 8-bit section)

INPUTS			OUTPUT
OE	LE	D	Q
L	H	H	H
L	H	L	L
L	L	X	Q <sub>0</sub>
H	X	X	Z

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	LVTH 3V	ALVCH 3V	UNIT
I <sub>CC</sub>	MAX	5	0.04	mA
I <sub>OH</sub>	MAX	-12	-12	mA
I <sub>OL</sub>	MAX	12	12	mA

TIMING REQUIREMENTS AND SWITCHING CHARACTERISTICS

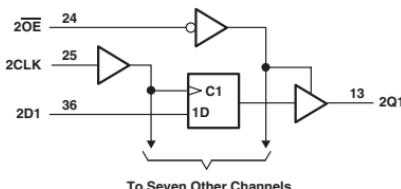
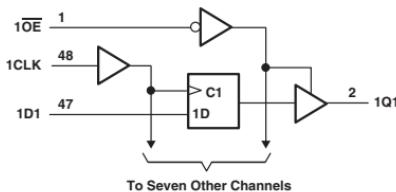
PARAMETER	INPUT	OUTPUT	MAX or MIN	LVTH 3V	ALVC 3V
t <sub>w</sub>	Pulse duration, LE high or low		MIN	3	3.3
t <sub>su</sub>	Data before LE ↓, data high		MIN	1	1.1
	Data before LE ↓, data low		MIN	1	1.1
t <sub>h</sub>	Data after LE ↓, data high		MIN	1	1.1
	Data after LE ↓, data low		MIN	1	1.1
t <sub>PLH</sub>	D	Q	MAX	4.6	4
t <sub>PHL</sub>				4	4
t <sub>PLH</sub>	LE	Q	MAX	5.1	4.2
t <sub>PHL</sub>				4.6	4.2
t <sub>PZH</sub>	OE	Q	MAX	5.4	5
t <sub>PZL</sub>				4.9	5
t <sub>PHZ</sub>	OE	Q	MAX	5.4	4.5
t <sub>PZL</sub>				5.1	4.5

UNIT: ns

## 3.3-V ABT 16-BIT EDGE-TRIGGERED D-TYPE FLIP-FLOPS WITH 3-STATE OUTPUTS

- SN74LVTH162374: Output Ports Have Equivalent 22- $\Omega$  Series Resistors
- SN74ALVCH162374: Output Ports Have Equivalent 26- $\Omega$  Series Resistors

Logic Diagram

FUNCTION TABLE  
(each flip-flop)

INPUTS			OUTPUT
$\overline{OE}$	CLK	D	Q
L	↑	H	H
L	↑	L	L
L	L	X	$Q_0$
H	X	X	Z

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	LVTH 3V	ALVCH 3V	UNIT
$I_{CC}$	MAX	5	0.04	mA
$I_{OH}$	MAX	-12	-12	mA
$I_{OL}$	MAX	12	12	mA

TIMING REQUIREMENTS AND SWITCHING CHARACTERISTICS

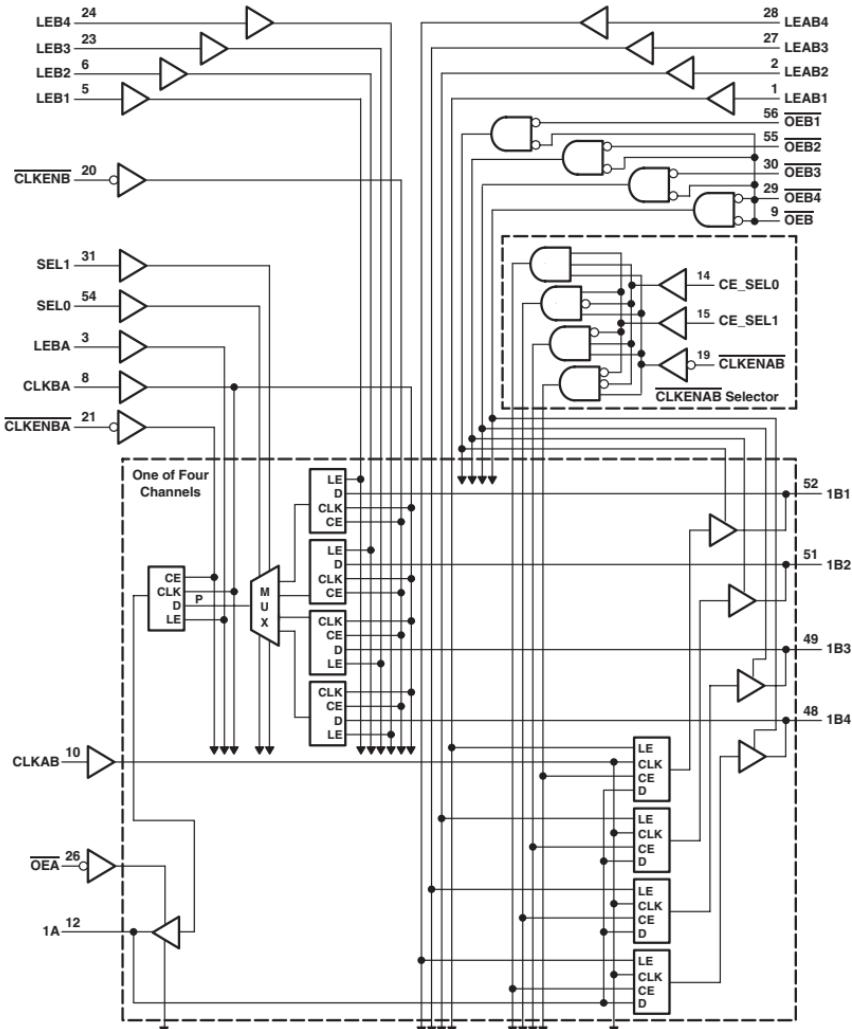
PARAMETER	INPUT	OUTPUT	MAX or MIN	LVTH 3V	ALVCH 3V
$t_{max}$				160	150
$t_{w}$ Pulse duration, CLK high or low			MIN	3	3.3
$t_{su}$ Setup time	Data before CLK ↑ , data high		MIN	1.8	1.9
	Data before CLK ↑ , data low		MIN	1.8	1.9
$t_h$ Hold time	Data after CLK ↑ , data high		MIN	0.8	0.5
	Data after CLK ↑ , data low		MIN	0.8	0.5
$t_{PLH}$	CLK	Q	MAX	5.3	4.6
$t_{PHL}$				4.9	4.6
$t_{PZH}$	$\overline{OE}$	Q	MAX	5.6	5.2
$t_{PZL}$				4.9	5.2
$t_{PHZ}$	$\overline{OE}$	Q	MAX	5.4	4.5
$t_{PLZ}$				5	4.5

UNIT fmax : MHz other : ns

**4-TO-1 MULTIPLEXED/DEMULTIPLEXED REGISTERED TRANSCEIVERS  
WITH 3-STATE OUTPUTS**

- SN74ABTH162460: B-Port Outputs Have Equivalent 25- $\Omega$  Series Resistors

Logic Diagram



**FUNCTION TABLE**
**A-TO-B OUTPUT ENABLE**

INPUTS	OUTPUT
OEB	OEBn
H	Z
H	L
L	H
L	Active

 $t_n = 1, 2, 3, 4$ 
**A-TO-B STORAGE  
(assuming OEB = L, OEBn = L)**

INPUTS										OUTPUTS				B1	B2	B3	B4		
CLKENAB		CE_SEL1		CE_SELO		CLKAB		LEAB1		LEAB2		LEAB3		LEAB4		B1	B2	B3	B4
X	X	X	X	H	or L	H	L	L	L	A	A <sub>0</sub>	A <sub>0</sub>	A <sub>0</sub>						
X	X	X	X	H	or L	H	H	H	L	A	A	A	A						
L	X	X	X	L	L	L	L	L	L	A <sub>0</sub>	A <sub>0</sub>	A <sub>0</sub>	A <sub>0</sub>						
L	L	X	X	L	L	L	L	L	L	A	A <sub>0</sub>	A <sub>0</sub>	A <sub>0</sub>						
L	L	L	X	H	L	L	L	L	L	A <sub>0</sub>	A <sub>0</sub>	A	A <sub>0</sub>						
L	L	H	X	H	L	L	L	L	L	A <sub>0</sub>	A <sub>0</sub>	A	A <sub>0</sub>						
H	X	X	X	X	↑	L	L	L	L	A <sub>0</sub>	A <sub>0</sub>	A <sub>0</sub>	A <sub>0</sub>						

**B-TO-A STORAGE  
(after point P)**

INPUTS										P							
CLKENB		CLKBA		LEB1		LEB2		LEB3		LEB4	SEL1	SEL0					
X	X	H	L	L	L	L	L	L	L	B1							
X	X	L	H	L	L	L	H	L	H	B2							
X	X	L	L	H	L	H	L	H	L	B3							
X	X	L	L	L	H	H	H	H	H	B4							
L	↑	L	L	L	L			L	L	B1 <sub>0†</sub>							
L	L	L	L	L	L			L	H	B2 <sub>0†</sub>							
								L	H	B3 <sub>0†</sub>							
								H	H	B4 <sub>0†</sub>							

**B-TO-A STORAGE  
(after point P)**

INPUTS					OUTPUT		
CLKENBA		CLKBA		LEBA	OE <sub>A</sub>	B	A
X	X	X	X	H	L	L	X
X	X	X	X	H	L	H	H
X	X	X	X	H	L	X	A <sub>0†</sub>
L	↑	L	L	L	L	L	L
L	L	L	L	L	L	H	H
						X	A <sub>0†</sub>

<sup>†</sup> Output level before the indicated steady-state input conditions were established

**ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS**

PARAMETER	MAX or MIN	ABTH	UNIT
I <sub>CC</sub>	MAX	32	mA
I <sub>OH</sub> (A port)	MAX	-32	mA
I <sub>OL</sub> (B port)	MAX	-12	mA
I <sub>OL</sub> (A port)	MAX	64	mA
I <sub>OL</sub> (B port)	MAX	12	mA

**TIMING REQUIREMENTS AND SWITCHING CHARACTERISTICS**

PARAMETER		MAX or MIN	ABTH
f <sub>max</sub>		MIN	160
	CLKAB high or low	MIN	3.8
	CLKBA high or low	MIN	4.5
t <sub>w</sub> Pulse duration	LEAB1, 2, 3 or 4 high	MIN	2.8
	LEBA high	MIN	2.8
	LEB1, 2, 3 or 4 high	MIN	3
	A bus	MIN	2.5
	CE_SEL0/1	MIN	3.2
	CLKENAB	MIN	3.2
t <sub>tr</sub> Setup time	Before CLKAB ↑	MIN	3.6
	B bus	MIN	3.8
	CLKENB	MIN	2.3
	Before CLKBA ↑	MIN	2.5
	LEB1, 2, 3 or 4	MIN	4.3
	SEL0/1	MIN	4.5
	Before LEAB1, 2, 3, or 4 ↓ B bus	MIN	3.2
	B bus	MIN	4
	Before CLKBA ↑	MIN	4.4
	SEL0/1	MIN	4.3
t <sub>th</sub> Hold time	A bus	MIN	0.5
	CE_SEL0/1	MIN	1.1
	CLKENAB	MIN	0.5
	After LEAB1, 2, 3, or 4 ↓ A bus	MIN	1.2
	B bus	MIN	1.3
	CLKENB	MIN	1
	CLKENBA	MIN	1
	SEL0/1	MIN	0
	After LEAB1, 2, 3, or 4 ↓ B bus	MIN	1.5
	B bus	MIN	0.4
	After CLKBA ↑	MIN	0.1

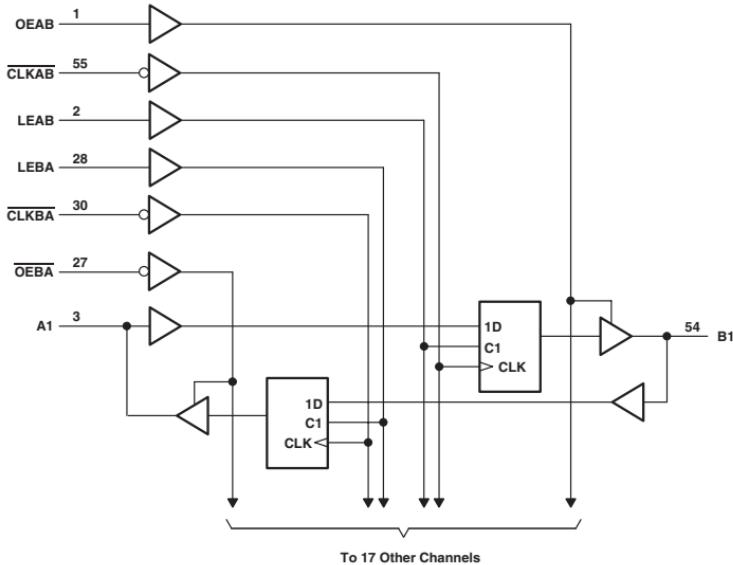
PARAMETER	INPUT	OUTPUT	MAX or MIN	ABTH
I <sub>PLH</sub>	B	A	MAX	6.5
I <sub>PHL</sub>			6.5	
I <sub>PZH</sub>	OE <sub>A</sub>	A	MAX	5.6
I <sub>PZL</sub>			5.5	
I <sub>PHZ</sub>	OE <sub>A</sub>	A	MAX	5.9
I <sub>PZL</sub>			6.5	
I <sub>PLH</sub>	A	B	MAX	6.2
I <sub>PHL</sub>			6.5	
I <sub>PZH</sub>	OE <sub>B</sub>	B	MAX	6.8
I <sub>PZL</sub>			6.3	
I <sub>PHZ</sub>	OE <sub>B</sub>	B	MAX	6.2
I <sub>PZL</sub>			5.8	
I <sub>PLH</sub>	OE <sub>B1, 2, 3, 4</sub>	B	MAX	6.6
I <sub>PLZ</sub>			6.2	
I <sub>PHZ</sub>	OE <sub>B1, 2, 3, 4</sub>	B	MAX	5.3
I <sub>PZL</sub>			4.9	
I <sub>PLH</sub>	CLKBA	A	MAX	7.4
I <sub>PHL</sub>			7.7	
I <sub>PZH</sub>	CLKAB	B	MAX	6.5
I <sub>PZL</sub>			6.5	
I <sub>PLH</sub>	LEBA	A	MAX	5.8
I <sub>PHL</sub>			5.8	
I <sub>PZH</sub>	LEAB1, 2, 3, 4	B	MAX	6.2
I <sub>PZL</sub>			6.2	
I <sub>PHZ</sub>	LEBA1, 2, 3, 4	A	MAX	7.2
I <sub>PZL</sub>			6.8	
I <sub>PLH</sub>	SEL	A	MAX	7.5
I <sub>PHL</sub>			7.5	
I <sub>PZH</sub>	SEL	A	MAX	6.9
I <sub>PZL</sub>			6.9	
UNIT	f <sub>max</sub> : MHz	other : ns		

# 162500

## 18-BIT UNIVERSAL BUS TRANSCEIVER WITH 3-STATE OUTPUTS

- SN74ABT162500: B-Port Outputs Have Equivalent 25- $\Omega$  Series Resistors

Logic Diagram



FUNCTION TABLE

INPUTS				OUTPUT B
OEAB	LEAB	$\bar{CLKAB}$	A	
L	X	X	X	Z
H	H	X	L	L
H	H	X	H	H
H	L	↓	L	L
H	L	↓	H	H
H	L	H	X	$B_0^{\ddagger}$
H	L	L	X	$B_0^{\$}$

‡ Output level before the indicated steady-state input conditions were established.

§ Output level before the indicated steady-state input conditions were established, provided that  $\bar{CLKAB}$  was low before LEAB went low.

## ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	ABT	UNIT
$I_{CC}$	MAX	36	mA
$I_{OH}$ (A port)	MAX	-32	mA
$I_{OL}$ (B port)	MAX	-12	mA
$I_{OL}$ (A port)	MAX	64	mA
$I_{OL}$ (B port)	MAX	12	mA

## TIMING REQUIREMENTS AND SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	ABT
$t_{max}$			MIN	150
$t_{W}$ Pulse duration	LEAB or LEBA high		MIN	2.5
	$\bar{CLKAB}$ or $\bar{CLKBA}$ high or low		MIN	3
	A before $\bar{CLKAB} \downarrow$		MIN	3.3
	B before $\bar{CLKBA} \downarrow$		MIN	3.3
$t_{SU}$ Setup time	A before LEAB ↓ or LEBA ↓ $\bar{CLK}$ high		MIN	1
	A before LEAB ↓ or LEBA ↓ $\bar{CLK}$ low		MIN	2.5
$t_h$ Hold time	A after $\bar{CLKAB} \downarrow$ or B after $\bar{CLKBA} \downarrow$		MIN	0
	A after LEAB ↓ or B after LEBA ↓		MIN	2
$t_{PLH}$	A or B	B or A	MAX	4.8
$t_{PHL}$				5.7
$t_{PZH}$	LEAB or LEBA	B or A	MAX	5.6
$t_{PZL}$				5.9
$t_{PHZ}$	$\bar{CLKAB}$ or $\bar{CLKBA}$	B or A	MAX	5.9
$t_{PLZ}$				6
$t_{PZH}$	OEAB	B	MAX	5.3
$t_{PZL}$				5.4
$t_{PHZ}$	OEAB	B	MAX	6.5
$t_{PLZ}$				5.8
$t_{PZH}$	OEBA	A	MAX	5.3
$t_{PZL}$				5.4
$t_{PHZ}$	OEBA	A	MAX	6.5
$t_{PLZ}$				5.8

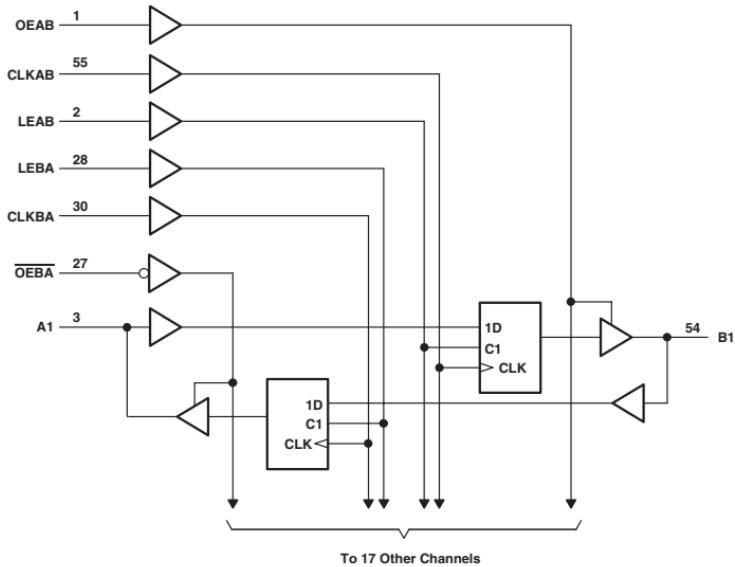
UNIT  $f_{max}$  : MHz other : ns

# 162501

## 18-BIT UNIVERSAL BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

- SN74ABT162501: B-Port Outputs Have Equivalent 25- $\Omega$  Series Resistors

Logic Diagram



**FUNCTION TABLE<sup>†</sup>**

INPUTS				OUTPUT
OEAB	LEAB	CLKAB	A	Y
L	X	X	X	Z
H	H	X	L	L
H	H	X	H	H
H	L	↑	L	L
H	L	↑	H	H
H	L	H	X	B <sub>0</sub> <sup>‡</sup>
H	L	L	X	B <sub>0</sub> <sup>§</sup>

<sup>†</sup> A-to-B data flow is shown; B-to-A flow is similar but uses OEBA, LEBA, and CLKBA.

<sup>‡</sup> Output level before the indicated steady-state input conditions were established, provided that CLKAB was high before LEAB went low.

<sup>§</sup> Output level before the indicated steady-state input conditions were established.

**ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS**

PARAMETER	MAX or MIN	ABT	UNIT
I <sub>CC</sub>	MAX	36	mA
I <sub>OH</sub> (A port)	MAX	-32	mA
I <sub>OL</sub> (B port)	MAX	-12	mA
I <sub>OL</sub> (A port)	MAX	64	mA
I <sub>OL</sub> (B port)	MAX	12	mA

**TIMING REQUIREMENTS AND SWITCHING CHARACTERISTICS**

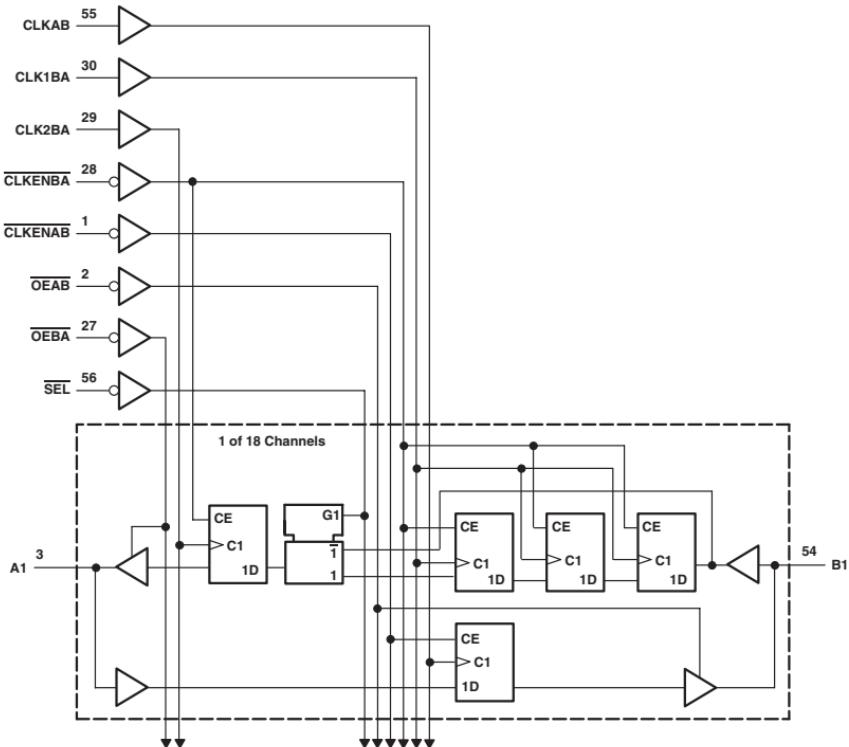
PARAMETER	INPUT	OUTPUT	MAX or MIN	ABT
t <sub>max</sub>			MIN	150
t <sub>w</sub> Pulse duration	LEAB or LEBA high CLKAB or CLKBA high or low		MIN	3
			MIN	3.3
	A before CLKAB ↑		MIN	4.3
	B before CLKBA ↑		MIN	4.3
t <sub>su</sub> Setup time	A before LEAB ↓ or LEBA ↓ CLK high		MIN	2.5
	A before LEAB ↓ or LEBA ↓ CLK low		MIN	1
t <sub>h</sub> Hold time	A after CLKAB ↑ or B after CLKBA ↑		MIN	0
	A after LEAB ↓ or B after LEBA ↓		MIN	2
t <sub>PLH</sub>	A or B	B or A	MAX	4.8
t <sub>PHL</sub>				5.7
t <sub>PZH</sub>	LEAB or LEBA	B or A	MAX	5.6
t <sub>PZL</sub>				5.9
t <sub>PHZ</sub>	CLKAB or CLKBA	B or A	MAX	5.5
t <sub>PZL</sub>				5.3
t <sub>PZH</sub>	OEAB	B	MAX	5.3
t <sub>PZL</sub>				5.4
t <sub>PHZ</sub>	OEAB	B	MAX	6.5
t <sub>PZL</sub>				5.8
t <sub>PZH</sub>	OEBA	A	MAX	5.3
t <sub>PZL</sub>				5.4
t <sub>PHZ</sub>	OEBA	A	MAX	6.5
t <sub>PZL</sub>				5.8

UNIT: f<sub>max</sub> : MHz other : ns

## 18-BIT REGISTERED BUS TRANSCEIVER WITH 3-STATE OUTPUTS

- SN74ALVCH162525: B-Port Outputs Have Equivalent 26- $\Omega$  Series Resistors

Logic Diagram



### FUNCTION TABLE

A-TO-B STORAGE( $\overline{OEAB} = L$ )

INPUTS		OUTPUT B
CLKNAB	OLKAB	A
H	X	X
L	↑	L
L	↑	H
		H

† Output level before the indicated steady-state input conditions were established

B-TO-A STORAGE ( $\overline{OEBA} = L$ )

INPUTS					OUTPUT A
CLKENBA	CLK2BA	CLK1BA	SEL	B	
H	X	X	X	X	$A_0 \dagger$
L	↑	X	H	L	L
L	↑	X	H	H	H
L	↑	↑	L	L	$L \ddagger$
L	↑	↑	L	H	$H \ddagger$

† Output level before the indicated steady-state input conditions were established

‡ Three CLK1BA edges and one CLK2BA edge are needed to propagate data from B to A when SEL is low.

### ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	ALVCH 3V	UNIT
Icc	MAX	0.04	mA
IoH (A port)	MAX	-24	mA
IoH (B port)	MAX	-12	mA
IoL (A port)	MAX	24	mA
IoL (B port)	MAX	12	mA

### TIMING REQUIREMENTS AND SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	ALVCH 3V
fmax			MIN	150
t <sub>w</sub> Pulse duration, CLK high or low			MIN	3
t <sub>su</sub> Setup time	A data before CLKAB ↑		MIN	1.3
	B data before CLK2BA ↑		MIN	1.7
	B data before CLK1BA ↑		MIN	1.1
	SEL before CLK2BA ↑		MIN	3.3
	CLKENAB before CLKAB ↑		MIN	1.6
	CLKENBA before CLK1BA ↑		MIN	2.1
	CLKENBA before CLK2BA ↑		MIN	2.2
t <sub>h</sub> Hold time	A data after CLKAB ↑		MIN	0.9
	B data after CLK2BA ↑		MIN	0.6
	B data after CLK1BA ↑		MIN	1
	SEL after CLK2BA ↑		MIN	0.1
	CLKENAB after CLKAB ↑		MIN	0.3
	CLKENBA after CLK1BA ↑		MIN	0.1
	CLKENBA after CLK2BA ↑		MIN	0
t <sub>pd</sub>	CLKAB	B	MAX	4.7
	CLK2BA	A	MAX	4.2
t <sub>en</sub>	OEBA	A	MAX	5.1
	OEAB	B	MAX	5.7
t <sub>dis</sub>	OEBA	A	MAX	4.9
	OEAB	B	MAX	4.9

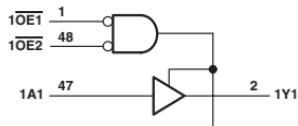
UNIT fmax : MHz other : ns

# 162541

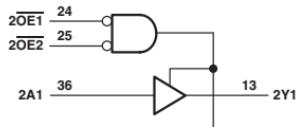
## 3.3-V ABT 16-BIT BUFFERS/DRIVERS WITH 3-STATE OUTPUTS

- SN74LVTH162541: Output Ports Have Equivalent 22- $\Omega$  Series Resistors

Logic Diagram



To Seven Other Channels



To Seven Other Channels

**FUNCTION TABLE**  
(each 8-bit section)

INPUTS			OUTPUT
OE1	OE2	A	Y
L	L	L	L
L	L	H	H
H	X	X	Z
X	H	X	Z

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	LVTH 3V	UNIT
I <sub>CC</sub>	MAX	5	mA
I <sub>OH</sub>	MAX	-12	mA
I <sub>OL</sub>	MAX	12	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	LVTH 3V
t <sub>PLH</sub>	A	Y	MAX	4.1
t <sub>PHL</sub>				4.1
t <sub>PZH</sub>	OE	Y	MAX	5
t <sub>PZL</sub>				4.8
t <sub>PHZ</sub>	OE	Y	MAX	5.9
t <sub>PZL</sub>				5.4

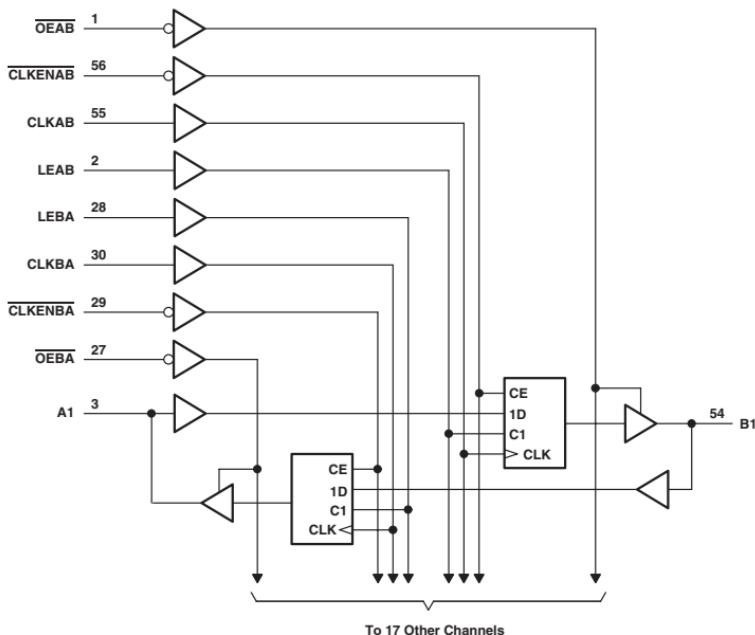
UNIT: ns

# 162601

## 18-BIT UNIVERSAL BUS TRANSCEIVER WITH 3-STATE OUTPUTS

- SN74ABT162601: B-Port Outputs Have Equivalent  $25\text{-}\Omega$  Series Resistors
- SN74ALVCH162601: B-Port Outputs Have Equivalent  $26\text{-}\Omega$  Series Resistors

Logic Diagram



FUNCTION TABLE

INPUTS					OUTPUT B
CLKENAB	OEAB	LEAB	CLKAB	A	
X	H	X	X	X	Z
X	L	H	X	L	L
X	L	H	X	H	H
H	L	L	X	X	B <sub>0</sub> †
H	L	L	X	X	B <sub>0</sub> †
L	L	L	↑	L	L
L	L	L	↑	H	H
L	L	L	L	X	B <sub>0</sub> †
L	L	L	H	X	B <sub>0</sub> §

† A-to-B data flow is shown; B-to-A flow is similar but uses OEBA, LEBA, CLKBA, and CLKENBA.

‡ Output level before the indicated steady-state input conditions were established.

§ Output level before the indicated steady-state input conditions were established, provided that CLKAB was low before LEAB went low.

## ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	ABT	ALVCH 3V	UNIT
I <sub>CC</sub>	MAX	36	0.04	mA
I <sub>OH</sub> (A port)	MAX	-32	-24	mA
I <sub>OH</sub> (B port)	MAX	-12	-12	mA
I <sub>OL</sub> (A port)	MAX	64	24	mA
I <sub>OL</sub> (B port)	MAX	12	12	mA

## TIMING REQUIREMENTS AND SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	ABT	ALVCH 3V
f <sub>max</sub>			MIN	150	150
t <sub>V</sub> Pulse duration	LEAB or LEBA high		MIN	2.5	3.3
	CLKAB or CLKBA high or low		MIN	3	3.3
t <sub>su</sub> Setup time	Data before CLK ↑		MIN	4.3	2.1
	A before LEAB ↓ or B before LEBA ↓, CLK high		MIN	2.5	1.6
	A before LEAB ↓ or B before LEBA ↓, CLK low		MIN	1	1.1
	CLKEN before ↑		MIN	2.7	1.7
t <sub>h</sub> Hold time	Data after CLK ↑		MIN	0	0.8
	A after LEAB ↓ or B after LEBA ↓, CLK high		MIN	0.5	1.4
	A after LEAB ↓ or B after LEBA ↓, CLK low		MIN	0.5	1.7
	CLKEN after ↑		MIN	0	0.6
t <sub>PLH</sub>	A	B	MAX	4.8	4.5
				5.7	4.5
t <sub>PHL</sub>	B	A	MAX	4	4.1
				4.9	4.1
t <sub>PLH</sub>	LEBA	A	MAX	5	4.7
				5	4.7
t <sub>PHL</sub>	LEAB	B	MAX	5.6	5.1
				5.9	5.1
t <sub>PLH</sub>	CLKBA	A	MAX	5.3	5
				5	5
t <sub>PHL</sub>	CLKAB	B	MAX	5.5	5.5
				5.3	5.5
t <sub>PZH</sub>	OEBA	A	MAX	5.1	5.2
				5.4	5.2
t <sub>PZL</sub>	OEAB	B	MAX	6.1	5.7
				5.7	5.7
t <sub>PZH</sub>	OEBA	A	MAX	6.2	4.4
				5.4	4.4
t <sub>PZL</sub>	OEAB	B	MAX	5.4	4.8
				5.2	4.8

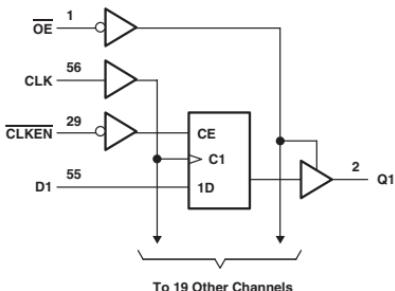
UNIT f<sub>max</sub> : MHz other : ns

# 162721

## 3.3-V 20-BIT FLIP-FLOP WITH 3-STATE OUTPUTS

- SN74ALVCH162721: Output Ports Have Equivalent 26- $\Omega$  Series Resistors

Logic Diagram



FUNCTION TABLE  
(each flip-flop)

INPUTS				OUTPUT
$\overline{OE}$	$\overline{CLKEN}$	CLK	D	Q
L	H	X	X	$Q_0$
L	L	$\uparrow$	H	H
L	L	$\uparrow$	L	L
L	L	L or H	X	$Q_0$
H	X	X	X	Z

### ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	ALVCH 3V	UNIT
$I_{CC}$	MAX	0.04	mA
$I_{OH}$	MAX	-12	mA
$I_{OL}$	MAX	12	mA

### TIMING REQUIREMENTS AND SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	ALVCH 3V
$t_{max}$			MIN	150
$t_w$ Pulse duration	CLK high or low		MIN	3.3
$t_{su}$ Setup time	Data before CLK $\uparrow$		MIN	3.1
	CLKEN before CLK $\uparrow$		MIN	2.7
$t_h$ Hold time	Data after CLK $\uparrow$		MIN	0
	CLKEN after CLK $\uparrow$		MIN	0
$t_{PLH}$	CLK	Q	MAX	5.3
$t_{PHL}$				5.3
$t_{PZH}$	OE	Q	MAX	5.8
$t_{PLZ}$				5.8
$t_{PHZ}$	OE	Q	MAX	5
$t_{PLZ}$				5

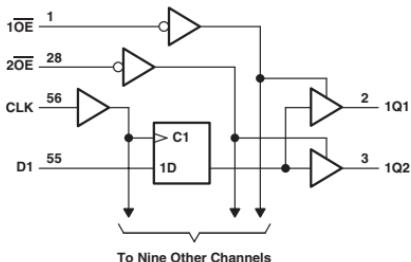
UNIT  $f_{max}$  : MHz other : ns

# 162820

## 3.3-V 10-BIT FLIP-FLOP WITH DUAL OUTPUTS AND 3-STATE OUTPUTS

- SN74ALVCH162820: Output Ports Have Equivalent 26- $\Omega$  Series Resistors

**Logic Diagram**



**FUNCTION TABLE**  
(each flip flop)

INPUTS			OUTPUT
OE <sub>n</sub> <sup>t</sup>	CLK	D	Q
L	↑	H	H
L	↑	L	L
L	L	X	Q <sub>0</sub>
H	X	X	Z

<sup>t</sup> n = 1,2

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	ALVCH 3V	UNIT
I <sub>CC</sub>	MAX	0.04	mA
I <sub>OH</sub>	MAX	-12	mA
I <sub>OL</sub>	MAX	12	mA

TIMING REQUIREMENTS AND SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	ALVCH 3V
f <sub>max</sub>			MIN	150
t <sub>W</sub> Pulse duration	CLK high or low		MIN	3.3
t <sub>SU</sub> Setup time	Data before CLK ↑		MIN	1.4
t <sub>H</sub> Hold time	Data after CLK ↑		MIN	1
t <sub>PLH</sub>	CLK	Q	MAX	5.4
t <sub>PHL</sub>				5.4
t <sub>PZH</sub>	OE	Q	MAX	5.6
t <sub>PZL</sub>				5.6
t <sub>PHZ</sub>	OE	Q	MAX	5
t <sub>PZL</sub>				5

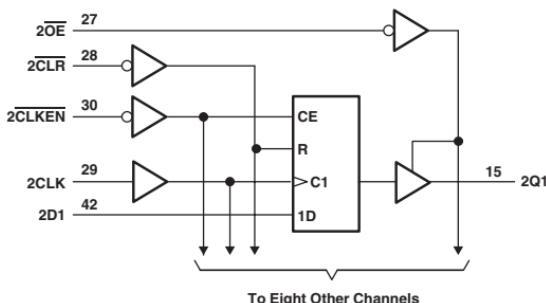
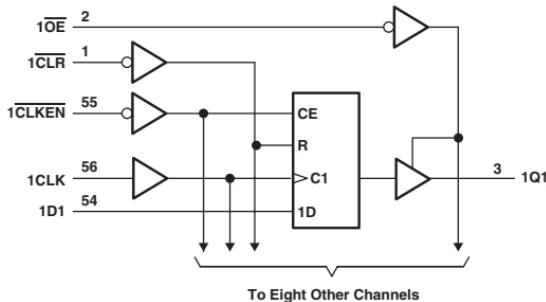
UNIT f<sub>max</sub> : MHz other : ns

# 162823

## 18-BIT BUS-INTERFACE FLIP-FLOPS WITH 3-STATE OUTPUTS

- SN74ABT162823A: Output Ports Have Equivalent  $25\Omega$  Series Resistors

Logic Diagram



FUNCTION TABLE

INPUTS				OUTPUT Q
OE	CLR	CLENK	CLK	D
L	L	X	X	X
L	H	L	↑	H
L	H	L	↑	L
L	H	L	L	X
L	H	H	X	X
H	X	X	X	X

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	ABT	UNIT
$I_{CC}$	MAX	80	mA
$I_{OH}$	MAX	-12	mA
$I_{OL}$	MAX	12	mA

TIMING REQUIREMENTS AND SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	ABT
$t_{max}$			MIN	150
$t_w$ Pulse duration	CLR low CLK high or low CLR inactive		MIN	3.3
$t_{au}$ Setup time	Data before CLK ↑ CLKEN low before CLK ↑		MIN	1.6
$t_h$ Hold time	Data after CLK ↑ CLKEN low after CLK ↑		MIN	0.6
$t_{PLH}$	CLK	Q	MAX	7.5
$t_{PHL}$	CLR	Q	MAX	6.7
$t_{PHL}$			MIN	7
$t_{PZH}$	$\bar{OE}$	Q	MAX	5.9
$t_{PLZ}$	$\bar{OE}$	Q	MAX	7
$t_{PHZ}$	$\bar{OE}$	Q	MAX	6.6
$t_{PLZ}$	$\bar{OE}$	Q	MAX	9

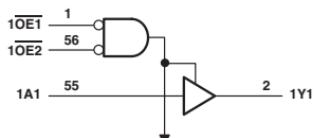
UNIT:  $f_{max}$ : MHz other : ns

# 162825

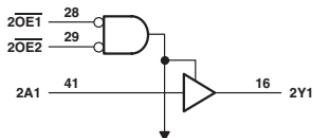
## 18-BIT BUFFERS/DRIVERS WITH 3-STATE OUTPUTS

- SN74ABT162825: Output Ports Have Equivalent  $25\text{-}\Omega$  Series Resistors

**Logic Diagram**



To Eight Other Channels



To Eight Other Channels

**FUNCTION TABLE**

INPUTS	OUTPUT		
$OE1$	$OE2$	A	Y
L	L	L	L
L	L	H	H
H	X	X	Z
X	H	X	Z

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	ABT	UNIT
$I_{CC}$	MAX	32	mA
$I_{OH}$	MAX	-12	mA
$I_{OL}$	MAX	12	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	ABT
$t_{PLH}$	A	Y	MAX	3.9
$t_{PHL}$				4.7
$t_{PZH}$	$\overline{OE}$	Y	MAX	6.9
$t_{PZL}$				6.3
$t_{PHZ}$	$\overline{OE}$	Y	MAX	6.6
$t_{PLZ}$				6.3

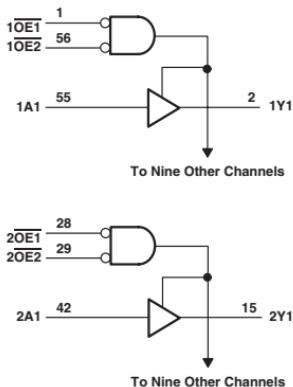
UNIT: ns

# 162827

## 20-BIT BUS BUFFERS/DRIVERS WITH 3-STATE OUTPUTS

- SN74ABT162827A: Output Ports Have Equivalent 25- $\Omega$  Series Resistors
- SN74ALVTH162827: Output Ports Have Equivalent 30- $\Omega$  Series Resistors
- SN74ALVCH162827: Output Ports Have Equivalent 26- $\Omega$  Series Resistors

**Logic Diagram**



### FUNCTION TABLE

(each flip flop)

INPUTS		OUTPUT	
OE1	OE2	A	Y
L	L	L	L
L	L	H	H
H	X	X	Z
X	H	X	Z

### ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	ABT	ALVTH 3V	ALVCH 3V	UNIT
Icc	MAX	32	5.5	0.04	mA
IOH	MAX	-12	-12	-12	mA
iol	MAX	12	12	12	mA

### SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	ABT	ALVTH 3V	ALVCH 3V
tPLH	A	Y	MAX	3.9	3.9	3.8
tPHL				4.7	3.7	3.8
tPZH	OE	Y	MAX	6.9	5.6	5.1
tPZL				6.3	4.1	5.1
tPHZ	OE	Y	MAX	6.6	6.3	4.7
tPLZ				6.3	5.1	4.7

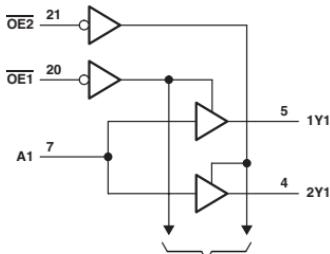
UNIT: ns

162830

# 1-BIT TO 2-BIT ADDRESS DRIVER WITH 3-STATE OUTPUTS

- SN74ALVCH162830, SN74ALVCHS162830: Output Ports Have Equivalent 26- $\Omega$  Series Resistors

## Logic Diagram



#### To 17 Other Channels

### FUNCTION TABLE

INPUTS			OUTPUTS	
OE1	OE2	A	Yn	2Yn
L	H	H	H	Z
L	H	L	L	Z
H	L	H	Z	H
H	L	L	Z	L
L	L	H	H	H
L	L	L	L	L
H	H	X	Z	Z

#### ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	ALVCH 3V	ALVCHS 3V	UNIT
$I_{CC}$	MAX	0.04	0.04	mA
$I_{OH}$	MAX	-12	-12	mA
$I_{OL}$	MAX	12	12	mA

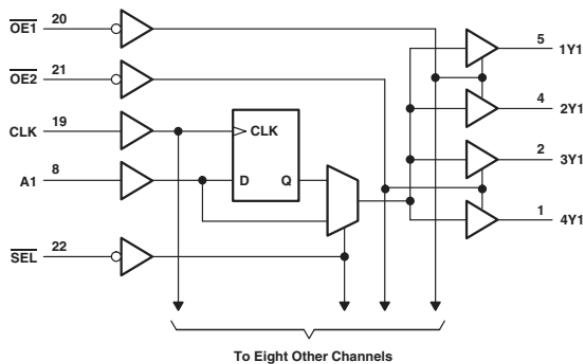
## SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	ALVCH 3V	ALVCHS 3V
IPLH	A	Y	MAX	3.5	3.5
IPLHL				3.5	3.5
IPLZH	OE	Y	MAX	4.8	4.8
IPLZL				4.8	4.8
IPLHZ	OE	Y	MAX	5.2	5.2
IPLZL				5.2	5.2

**UNIT:** ns

## 1-BIT TO 4-BIT ADDRESS REGISTER/DRIVER WITH 3-STATE OUTPUTS

- SN74ALVC162831, SN74ALVCH162831: Output Ports Have Equivalent 26- $\Omega$  Series Resistors



FUNCTION TABLE

INPUTS			OUTPUT	
OE	SEL	CLK	A	Y
H	X	X	X	Z
L	H	X	L	L
L	H	X	H	H
L	L	↑	L	L
L	L	↑	H	H

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	ALVC 3V	ALVCH 3V	UNIT
$I_{CC}$	MAX	0.04	0.04	mA
$I_{OH}$	MAX	-12	-12	mA
$I_{OL}$	MAX	12	12	mA

TIMING REQUIREMENTS AND SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	ALVC 3V	ALVCH 3V
$t_{max}$			MIN	150	150
$t_W$ Pulse duration	CLK high or low		MIN	3.3	3.3
$t_{SU}$ Setup time	A data before CLK ↑		MIN	1.6	1.6
$t_h$ Hold time	A data after CLK ↑		MIN	1.1	1.1
$t_{PLH}$	A	Y	MAX	4.3	4.3
$t_{PHL}$				4.3	4.3
$t_{PLH}$	CLK	Y	MAX	4.7	4.7
$t_{PHL}$				4.7	4.7
$t_{PLH}$	SEL	Y	MAX	4.8	4.8
$t_{PHL}$				4.8	4.8
$t_{PZH}$	OE	Y	MAX	5.1	5.1
$t_{PZL}$				5.1	5.1
$t_{PZH}$	OE	Y	MAX	5.1	5.1
$t_{PZL}$				5.1	5.1

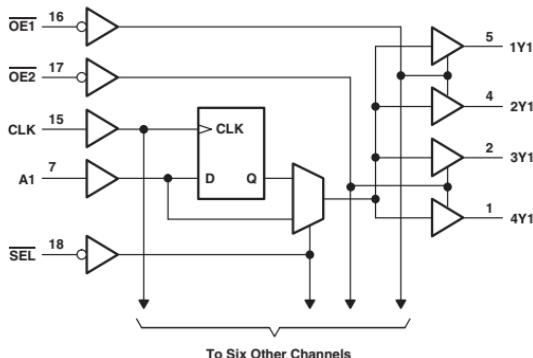
UNIT fmax : MHz other : ns

# 162832

## 1-BIT TO 4-BIT ADDRESS REGISTER/DRIVER WITH 3-STATE OUTPUTS

- SN74ALVCH162832: Output Ports Have Equivalent 26- $\Omega$  Series Resistors

Logic Diagram



FUNCTION TABLE

INPUTS				OUTPUT
OE	SEL	CLK	A	Y
H	X	X	X	Z
L	H	X	L	L
L	H	X	H	H
L	L	↑	L	L
L	L	↑	H	H

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	ALVCH 3V	UNIT
I <sub>CC</sub>	MAX	0.04	mA
I <sub>OH</sub>	MAX	-12	mA
I <sub>OL</sub>	MAX	12	mA

TIMING REQUIREMENTS AND SWITCHING CHARACTERISTICS

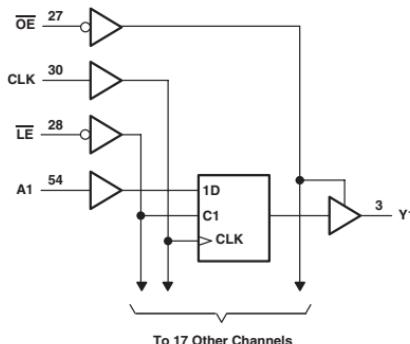
PARAMETER	INPUT	OUTPUT	MAX or MIN	ALVCH 3V
f <sub>max</sub>			MIN	150
t <sub>w</sub> Pulse duration	CLK high or low		MIN	3.3
t <sub>su</sub> Setup time	A data before CLK ↑		MIN	1.6
t <sub>hl</sub> Hold time	A data after CLK ↑		MIN	1.1
t <sub>PLH</sub>	A	Y	MAX	4.3
t <sub>PHL</sub>				4.3
t <sub>PLH</sub>	CLK	Y	MAX	4.7
t <sub>PHL</sub>				4.7
t <sub>PLH</sub>	SEL	Y	MAX	4.8
t <sub>PHL</sub>				4.8
t <sub>PZH</sub>	OE	Y	MAX	5.1
t <sub>PLZ</sub>				5.1
t <sub>PHZ</sub>	OE	Y	MAX	5.1
t <sub>PLZ</sub>				5.1

UNIT f<sub>max</sub> : MHz other : ns

## 18-BIT UNIVERSAL BUS DRIVER WITH 3-STATE OUTPUTS

- SN74ALVC162834: Outputs Have Equivalent 26- $\Omega$  Series Resistors

Logic Diagram



FUNCTION TABLE

INPUTS				OUTPUT
OE	LE	CLK	A	Y
H	X	X	X	Z
L	L	X	L	L
L	L	X	H	H
L	H	↑	L	L
L	H	H	H	H
L	H	H	X	Y <sub>0†</sub>
L	H	L	X	Y <sub>0†</sub>

† Output level before the indicated steady-state input conditions were established, provided that CLK is high before LE goes high.

‡ Output level before the indicated steady-state input conditions were established.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	ALVC 3V	ALVCF 3V	UNIT
I <sub>CC</sub>	MAX	0.04	0.04	mA
I <sub>OH</sub>	MAX	-12	-18	mA
I <sub>OL</sub>	MAX	12	18	mA

TIMING REQUIREMENTS AND SWITCHING CHARACTERISTICS

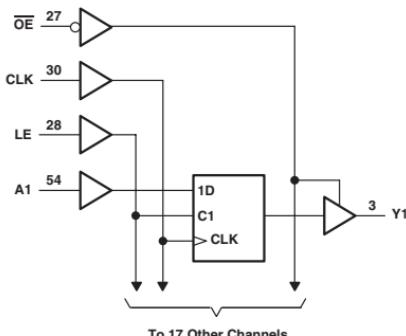
PARAMETER	INPUT	OUTPUT	MAX or MIN	ALVC 3V	ALVCF 3V
f <sub>max</sub>			MIN	150	150
t <sub>w</sub> Pulse duration	LE low CLK high or low		MIN	3.3	3.3
t <sub>su</sub> Setup time	Data before CLK ↑ Data before LE ↑, CLK high Data before LE ↑, CLK low		MIN	3.3	3.3
t <sub>th</sub> Hold time	A data after CLK ↑ Data after LE ↑, CLK high Data after LE ↑, CLK low		MIN	1.7	1.0
t <sub>PLH</sub>	A	Y	MAX	4.2	3.5
t <sub>PHL</sub>				4.2	3.5
t <sub>PLH</sub>	LE	Y	MAX	5.8	4.6
t <sub>PHL</sub>				5.8	4.6
t <sub>PLH</sub>	CLK	Y	MAX	5.4	3.5
t <sub>PHL</sub>				5.4	3.5
t <sub>PZH</sub>	OE	Y	MAX	5.9	5.0
t <sub>PZL</sub>				5.9	5.0
t <sub>PHZ</sub>	OE	Y	MAX	5	4.2
t <sub>PZL</sub>				5	4.2

UNIT f<sub>max</sub> : MHz other : ns

# 162835

## 18-BIT UNIVERSAL BUS DRIVER WITH 3-STATE OUTPUTS

- SN74ALVC162835, SN74ALVCH162835: Output Port Has Equivalent 26- $\Omega$  Series Resistors

**Logic Diagram****FUNCTION TABLE**

INPUTS			OUTPUT	
OE	LE	CLK	A	Y
H	X	X	X	Z
L	H	X	L	L
L	H	X	H	H
L	L	↑	L	L
L	L	↑	H	H
L	L	L or H	X	Y <sub>0†</sub>

† Output level before the indicated steady-state input conditions were established

**ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS**

PARAMETER	MAX or MIN	ALVC 3V	ALVCF 3V	ALVCH 3V	UNIT
I <sub>CC</sub>	MAX	0.04	0.04	0.04	mA
I <sub>OH</sub>	MAX	-12	-18	-12	mA
I <sub>OL</sub>	MAX	12	18	12	mA

**TIMING REQUIREMENTS AND SWITCHING CHARACTERISTICS**

PARAMETER	INPUT	OUTPUT	MAX or MIN	ALVC 3V	ALVCF 3V	ALVCH 3V
f <sub>max</sub>			MIN	150	150	150
t <sub>W</sub> Pulse duration	LE low		MIN	3.3	3.3	3.3
	CLK high or low		MIN	3.3	3.3	3.3
t <sub>W</sub> Setup time	Data before CLK ↑		MIN	1.7	1.0	1.7
	Data before LE ↓, CLK high		MIN	1.5	1.5	1.5
	Data before LE ↓, CLK low		MIN	1	1.0	1
t <sub>H</sub> Hold time	A data after CLK ↑		MIN	0.7	0.6	0.7
	Data after LE ↓, CLK high		MIN	1.4	1.4	1.4
	Data after LE ↓, CLK low		MIN	1.4	1.4	1.4
t <sub>PLH</sub>	A	Y	MAX	4.2	3.5	4.2
t <sub>PHL</sub>				4.2	3.5	4.2
t <sub>PLH</sub>	LE	Y	MAX	5.1	4.6	5.1
t <sub>PHL</sub>				5.1	4.6	5.1
t <sub>PLH</sub>	CLK	Y	MAX	5.4	3.5	5.4
t <sub>PHL</sub>				5.4	3.5	5.4
t <sub>PZH</sub>	OE	Y	MAX	5.5	5.0	5.5
t <sub>PHZ</sub>				5.5	5.0	5.5
t <sub>PZL</sub>	OE	Y	MAX	4.5	4.2	4.5
t <sub>PZL</sub>				4.5	4.2	4.5

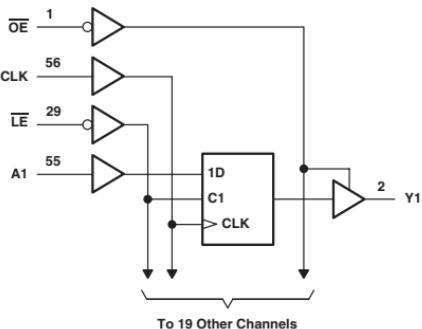
UNIT f<sub>max</sub> : MHz other : ns

# 162836

## 20-BIT UNIVERSAL BUS DRIVER WITH 3-STATE OUTPUTS

- SN74ALVC162836, SN74ALVCH162836: Output Port Has Equivalent 26- $\Omega$  Series Resistors

### Logic Diagram



### FUNCTION TABLE

INPUTS				OUTPUT
OE	LE	CLK	A	Y
H	X	X	X	Z
L	L	X	L	L
L	L	X	H	H
L	H	↑	L	L
L	H	↑	H	H
L	H	L or H	X	Y <sub>0f</sub>

† Output level before the indicated steady-state input conditions were established

### ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	ALVC 3V	ALVCH 3V	UNIT
I <sub>CC</sub>	MAX	0.04	0.04	mA
I <sub>OH</sub>	MAX	-12	-12	mA
I <sub>OL</sub>	MAX	12	12	mA

### TIMING REQUIREMENTS AND SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	ALVC 3V	ALVCH 3V
f <sub>max</sub>			MIN	150	150
t <sub>w</sub> Pulse duration	LE low		MIN	3.3	3.3
	CLK high or low		MIN	3.3	3.3
t <sub>su</sub> Setup time	Data before CLK ↑		MIN	1.5	1.5
	Data before LE ↓, CLK high		MIN	1.3	1.3
	Data before LE ↓, CLK low		MIN	1.2	1.2
t <sub>h</sub> Hold time	A data after CLK ↑		MIN	0.9	0.9
	Data after LE ↓, CLK high		MIN	1.1	1.1
	Data after LE ↓, CLK low		MIN	1.1	1.1
t <sub>PLH</sub>	A	Y	MAX	4	4
t <sub>PHL</sub>				4	4
t <sub>PLH</sub>	LE	Y	MAX	5.1	5.1
t <sub>PHL</sub>				5.1	5.1
t <sub>PLH</sub>	CLK	Y	MAX	5	5
t <sub>PHL</sub>				5	5
t <sub>PZH</sub>	OE	Y	MAX	5.5	5.5
t <sub>PZL</sub>				5.5	5.5
t <sub>PHZ</sub>	OE	Y	MAX	5.1	5.1
t <sub>PLZ</sub>				5.1	5.1

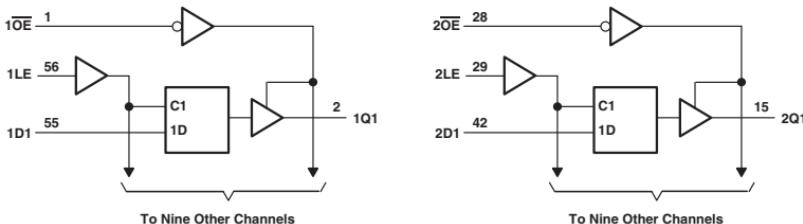
UNIT f<sub>max</sub>: MHz other : ns

# 162841

## 20-BIT BUS-INTERFACE D-TYPE LATCH WITH 3-STATE OUTPUTS

- SN74ABT162841: Output Ports Have Equivalent 25- $\Omega$  Series Resistors
- SN74ALVCH162841: Output Ports Have Equivalent 26- $\Omega$  Series Resistors

### Logic Diagram



### FUNCTION TABLE (each 10-bit latch)

INPUTS	OUTPUT		
$\overline{OE}$	LE	D	Q
L	H	H	H
L	H	L	L
L	L	X	$Q_0$
H	X	X	Z

### ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	ABT	ALVCH 3V	UNIT
$I_{CC}$	MAX	89	0.04	mA
$I_{OH}$	MAX	-12	-12	mA
$I_{OL}$	MAX	12	12	mA

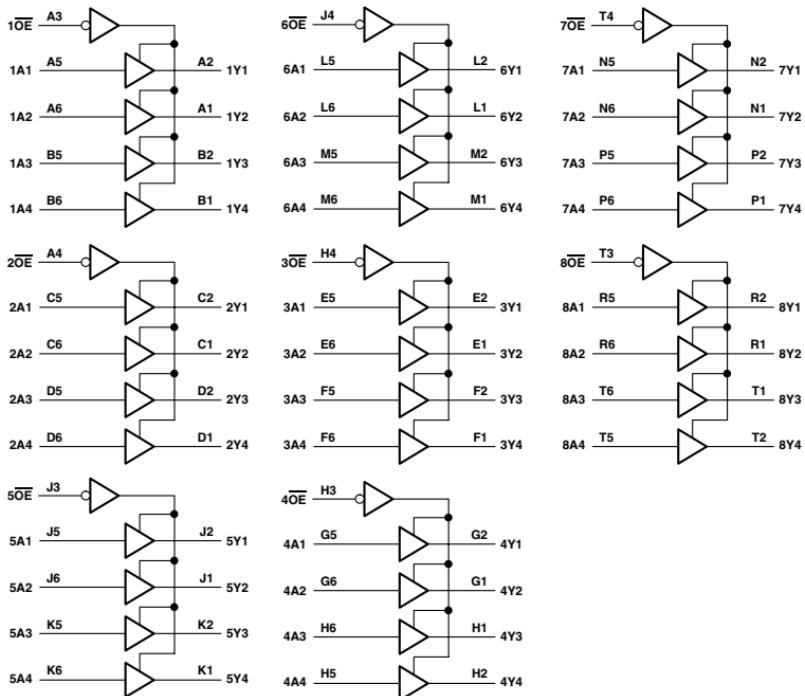
### TIMING REQUIREMENTS AND SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	ABT	ALVCH 3V
$t_{by}$ Pulse duration	LE higher low		MIN	4	3.3
$t_{su}$ Setup time	Data before LE ↓		MIN	0.8	-
	Data before LE ↑		MIN	-	1.1
$t_h$ Hold time	Data after LE ↓		MIN	1.8	-
	Data after LE ↑		MIN	-	1.1
$t_{PLH}$	D	Q	MAX	5.2	4.3
$t_{PHL}$			MAX	6	4.3
$t_{PLH}$	LE	Q	MAX	5.4	4.7
$t_{PHL}$			MAX	5.8	4.7
$t_{PZH}$	$\overline{OE}$	Q	MAX	5.7	5.3
$t_{PZL}$			MAX	6.5	5.3
$t_{PHZ}$	$\overline{OE}$	Q	MAX	6.5	4.4
$t_{PLZ}$			MAX	7.1	4.4

UNIT : ns

## 32-BIT BUFFER/DRIVER WITH 3-STATE OUTPUTS

Logic Diagram



## ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	LVCH 3V	UNIT
$I_{CC}$	MAX	0.04	mA
$I_{OH}$	MAX	-12	mA
$I_{OL}$	MAX	12	mA

## SWITCHING CHARACTERISTICS

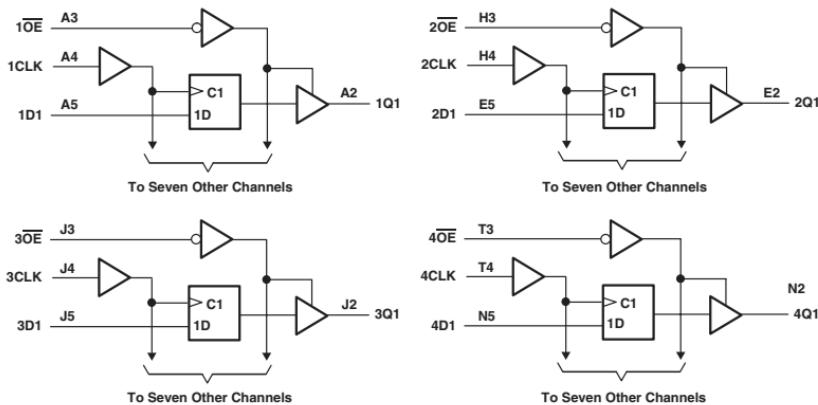
PARAMETER	INPUT	OUTPUT	MAX or MIN	LVCH 3V
$t_{PLH}$	A	Y	MAX	4.4
$t_{PHL}$				4.4
$t_{PZH}$	$\overline{DE}$	Y	MAX	5.5
$t_{PZL}$				5.5
$t_{PHZ}$	$\overline{DE}$	Y	MAX	6.3
$t_{PZL}$				6.3

UNIT: ns

## 3.3-V ABT 32-BIT EDGE-TRIGGERED D-TYPE FLIP-FLOP

- Output Ports Have Equivalent 22- $\Omega$  Series Resistors

Logic Diagram

FUNCTION TABLE  
(each 8bit flip-flop)

INPUTS	OUTPUT		
$\bar{OE}$	CLK	D	Q
L	$\uparrow$	H	H
L	$\uparrow$	L	L
L	H or L	X	$Q_0$
H	X	X	Z

ELECTRICAL CHARACTERISTICS AND  
RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	LVTH 3V	UNIT
$I_{CC}$	MAX	10	$\mu A$
$I_{OH}$	MAX	-12	$\mu A$
$I_{OL}$	MAX	12	$\mu A$

## TIMING REQUIREMENTS AND SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	LVTH 3V
$t_{max}$				
$t_w$	Pulse duration, CLK high or low		MIN	160
$t_{sw}$	Setup time	Data before CLK $\uparrow$ , data high	MIN	3
		Data before CLK $\uparrow$ , data low	MIN	1.8
$t_h$	Hold time	Data after CLK $\uparrow$ , data high	MIN	1.8
		Data after CLK $\uparrow$ , data low	MIN	0.8
$t_{PLH}$	CLK	Q	MAX	5.3
$t_{PHL}$				4.9
$t_{PZH}$	$\bar{OE}$	Q	MAX	5.6
$t_{PZL}$				4.9
$t_{PHZ}$	$\bar{OE}$	Q	MAX	5.4
$t_{PLZ}$				5
UNIT fmax : MHz other : ns				

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