

1. Description

1.1. Project

Project Name	STM32_Cat1
Board Name	NUCLEO-L476RG
Generated with:	STM32CubeMX 6.1.1
Date	12/21/2020

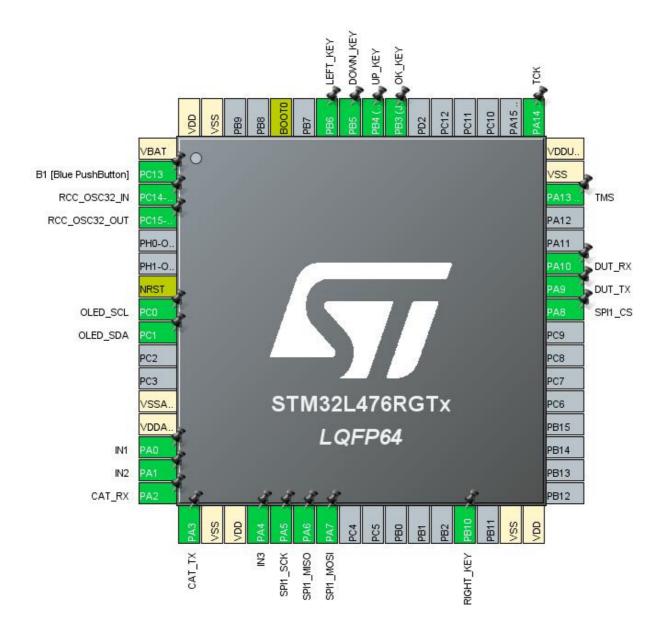
1.2. MCU

MCU Series	STM32L4
MCU Line	STM32L4x6
MCU name	STM32L476RGTx
MCU Package	LQFP64
MCU Pin number	64

1.3. Core(s) information

Core(s)	Arm Cortex-M4

2. Pinout Configuration

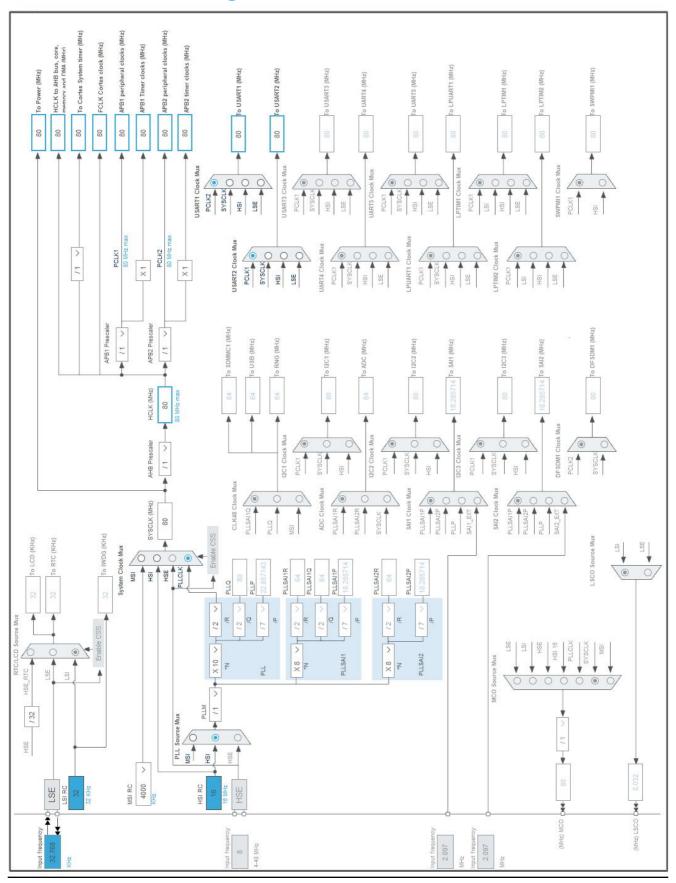


3. Pins Configuration

Pin Number	Pin Name	Pin Type	Alternate	Label
LQFP64	(function after		Function(s)	
	reset)		()	
1	VBAT	Power		
2	PC13	I/O	GPIO_EXTI13	B1 [Blue PushButton]
3	PC14-OSC32_IN (PC14)	I/O	RCC_OSC32_IN	
4	PC15-OSC32_OUT (PC15)	I/O	RCC_OSC32_OUT	
7	NRST	Reset		
8	PC0 *	I/O	GPIO_Output	OLED_SCL
9	PC1 *	I/O	GPIO_Output	OLED_SDA
12	VSSA/VREF-	Power		
13	VDDA/VREF+	Power		
14	PA0 *	I/O	GPIO_Output	IN1
15	PA1 *	I/O	GPIO_Output	IN2
16	PA2	I/O	USART2_TX	CAT_RX
17	PA3	I/O	USART2_RX	CAT_TX
18	VSS	Power		
19	VDD	Power		
20	PA4 *	I/O	GPIO_Output	IN3
21	PA5	I/O	SPI1_SCK	
22	PA6	I/O	SPI1_MISO	
23	PA7	I/O	SPI1_MOSI	
29	PB10	I/O	GPIO_EXTI10	RIGHT_KEY
31	VSS	Power		
32	VDD	Power		
41	PA8 *	I/O	GPIO_Output	SPI1_CS
42	PA9	I/O	USART1_TX	DUT_TX
43	PA10	I/O	USART1_RX	DUT_RX
46	PA13 (JTMS-SWDIO)	I/O	SYS_JTMS-SWDIO	TMS
47	VSS	Power		
48	VDDUSB	Power		
49	PA14 (JTCK-SWCLK)	I/O	SYS_JTCK-SWCLK	TCK
55	PB3 (JTDO-TRACESWO)	I/O	GPIO_EXTI3	OK_KEY
56	PB4 (NJTRST)	I/O	GPIO_EXTI4	UP_KEY
57	PB5	I/O	GPIO_EXTI5	DOWN_KEY
58	PB6	I/O	GPIO_EXTI6	LEFT_KEY
60	воото	Boot		
63	VSS	Power		
64	VDD	Power		

* The pin is affected with an I/O function

4. Clock Tree Configuration



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5. Software Project

5.1. Project Settings

Name	Value
Project Name	STM32_Cat1
Project Folder	D:\huimeng\newtimeda\dut\STM32_Cat1
Toolchain / IDE	EWARM V7
Firmware Package Name and Version	STM32Cube FW_L4 V1.16.0
Application Structure	Basic
Generate Under Root	No
Do not generate the main()	No
Minimum Heap Size	0x200
Minimum Stack Size	0x400

5.2. Code Generation Settings

Name	Value
STM32Cube MCU packages and embedded software	Copy only the necessary library files
Generate peripheral initialization as a pair of '.c/.h' files	No
Backup previously generated files when re-generating	No
Keep User Code when re-generating	Yes
Delete previously generated files when not re-generated	Yes
Set all free pins as analog (to optimize the power	No
consumption)	
Enable Full Assert	No

5.3. Advanced Settings - Generated Function Calls

Rank	Function Name	Peripheral Instance Name
1	MX_GPIO_Init	GPIO
2	SystemClock_Config	RCC
3	MX_SPI1_Init	SPI1
4	MX_USART1_UART_Init	USART1
5	MX_USART2_UART_Init	USART2

6. Power Consumption Calculator report

6.1. Microcontroller Selection

Series	STM32L4
Line	STM32L4x6
MCU	STM32L476RGTx
Datasheet	DS10198_Rev4

6.2. Parameter Selection

Temperature	25
Vdd	3.0

6.3. Battery Selection

Battery	Li-SOCL2(A3400)
Capacity	3400.0 mAh
Self Discharge	0.08 %/month
Nominal Voltage	3.6 V
Max Cont Current	100.0 mA
Max Pulse Current	200.0 mA
Cells in series	1
Cells in parallel	1

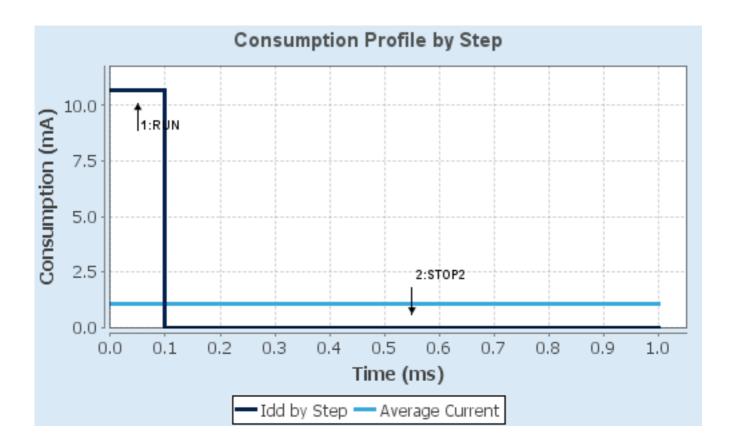
6.4. Sequence

Step	Step1	Step2
Mode	RUN	STOP2
Vdd	3.0	3.0
Voltage Source	Battery	Battery
Range	Range1-High	NoRange
Fetch Type	SRAM2	n/a
CPU Frequency	80 MHz	0 Hz
Clock Configuration	HSE PLL	ALL CLOCKS OFF
Clock Source Frequency	4 MHz	0 Hz
Peripherals		
Additional Cons.	0 mA	0 mA
Average Current	10.7 mA	1.18 μΑ
Duration	0.1 ms	0.9 ms
DMIPS	100.0	0.0
Ta Max	103.56	105
Category	In DS Table	In DS Table

6.5. Results

Sequence Time	1 ms	Average Current	1.07 mA
Battery Life	4 months, 10	Average DMIPS	100.0 DMIPS
	days, 3 hours	_	

6.6. Chart



7. Peripherals and Middlewares Configuration

7.1. RCC

Low Speed Clock (LSE): Crystal/Ceramic Resonator

7.1.1. Parameter Settings:

System Parameters:

VDD voltage (V) 3.3
Instruction Cache Enabled
Prefetch Buffer Enabled *
Data Cache Enabled

Flash Latency(WS) 4 WS (5 CPU cycle)

RCC Parameters:

HSI Calibration Value 16

MSI Calibration Value 0

MSI Auto Calibration Disabled

HSE Startup Timout Value (ms) 100

LSE Startup Timout Value (ms) 5000

Power Parameters:

Power Regulator Voltage Scale Power Regulator Voltage Scale 1

7.2. SPI1

Mode: Full-Duplex Master

7.2.1. Parameter Settings:

Basic Parameters:

Frame Format Motorola

Data Size 8 Bits *

First Bit MSB First

Clock Parameters:

Prescaler (for Baud Rate) 128 *

Baud Rate 625.0 KBits/s *

Clock Polarity (CPOL) Low
Clock Phase (CPHA) 1 Edge

Advanced Parameters:

CRC Calculation Disabled

NSSP Mode Enabled

NSS Signal Type Software

7.3. SYS

Debug: Serial Wire

Timebase Source: SysTick

7.4. USART1

Mode: Asynchronous

7.4.1. Parameter Settings:

Basic Parameters:

Baud Rate 115200

Word Length 8 Bits (including Parity)

Parity None Stop Bits 1

Advanced Parameters:

Data Direction Receive and Transmit

Over Sampling 16 Samples
Single Sample Disable

Advanced Features:

Auto Baudrate Disable TX Pin Active Level Inversion Disable RX Pin Active Level Inversion Disable **Data Inversion** Disable TX and RX Pins Swapping Disable Enable Overrun DMA on RX Error Enable MSB First Disable

7.5. **USART2**

Mode: Asynchronous

7.5.1. Parameter Settings:

Basic Parameters:

Baud Rate 115200

Word Length 8 Bits (including Parity)

Parity None Stop Bits 1

Advanced Parameters:

Data Direction Receive and Transmit

Over Sampling 16 Samples
Single Sample Disable

Advanced Features:

Auto Baudrate Disable TX Pin Active Level Inversion Disable RX Pin Active Level Inversion Disable Disable Data Inversion TX and RX Pins Swapping Disable Enable Overrun DMA on RX Error Enable MSB First Disable

^{*} User modified value

8. System Configuration

8.1. GPIO configuration

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
RCC	PC14- OSC32_IN (PC14)	RCC_OSC32_IN	n/a	n/a	n/a	
	PC15- OSC32_OU T (PC15)	RCC_OSC32_O UT	n/a	n/a	n/a	
SPI1	PA5	SPI1_SCK	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PA6	SPI1_MISO	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PA7	SPI1_MOSI	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
SYS	PA13 (JTMS- SWDIO)	SYS_JTMS- SWDIO	n/a	n/a	n/a	TMS
	PA14 (JTCK- SWCLK)	SYS_JTCK- SWCLK	n/a	n/a	n/a	TCK
USART1	PA9	USART1_TX	Alternate Function Push Pull	No pull-up and no pull-down	Very High	DUT_TX
	PA10	USART1_RX	Alternate Function Push Pull	No pull-up and no pull-down	Very High	DUT_RX
USART2	PA2	USART2_TX	Alternate Function Push Pull	No pull-up and no pull-down	Very High	CAT_RX
	PA3	USART2_RX	Alternate Function Push Pull	No pull-up and no pull-down	Very High	CAT_TX
GPIO	PC13	GPIO_EXTI13	External Interrupt Mode with Falling edge trigger detection	No pull-up and no pull-down	n/a	B1 [Blue PushButton]
	PC0	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	OLED_SCL
	PC1	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	OLED_SDA
	PA0	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	IN1
	PA1	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	IN2
	PA4	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	IN3
	PB10	GPIO_EXTI10	External Interrupt Mode with Rising edge trigger detection	Pull-up *	n/a	RIGHT_KEY
	PA8	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	SPI1_CS

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
	PB3 (JTDO- TRACESWO	GPIO_EXTI3	External Interrupt Mode with Rising edge trigger detection	Pull-up *	n/a	OK_KEY
	PB4 (NJTRST)	GPIO_EXTI4	External Interrupt Mode with Rising edge trigger detection	Pull-up *	n/a	UP_KEY
	PB5	GPIO_EXTI5	External Interrupt Mode with Rising edge trigger detection	Pull-up *	n/a	DOWN_KEY
	PB6	GPIO_EXTI6	External Interrupt Mode with Rising edge trigger detection	Pull-up *	n/a	LEFT_KEY

8.2. DMA configuration

nothing configured in DMA service

8.3. NVIC configuration

8.3.1. NVIC

Interrupt Table	Enable	Preenmption Priority	SubPriority	
Non maskable interrupt	true	0	0	
Hard fault interrupt	true	0	0	
Memory management fault	true	0	0	
Prefetch fault, memory access fault	true	0	0	
Undefined instruction or illegal state	true	0	0	
System service call via SWI instruction	true	0	0	
Debug monitor	true	0	0	
Pendable request for system service	true	0	0	
System tick timer	true	0	0	
EXTI line3 interrupt	true	1	0	
EXTI line4 interrupt	true	1	0	
EXTI line[9:5] interrupts	true	1	0	
USART1 global interrupt	true	2	0	
USART2 global interrupt	true	3	0	
EXTI line[15:10] interrupts	true	1	0	
PVD/PVM1/PVM2/PVM3/PVM4 interrupts through EXTI lines 16/35/36/37/38	unused			
Flash global interrupt	unused			
RCC global interrupt	unused			
SPI1 global interrupt	unused			
FPU global interrupt	unused			

8.3.2. NVIC Code generation

Enabled interrupt Table	Select for init sequence ordering	Generate IRQ handler	Call HAL handler
Non maskable interrupt	false	true	false
Hard fault interrupt	false	true	false
Memory management fault	false	true	false
Prefetch fault, memory access fault	false	true	false
Undefined instruction or illegal state	false	true	false
System service call via SWI instruction	false	true	false
Debug monitor	false	true	false
Pendable request for system service	false	true	false
System tick timer	false	true	true
EXTI line3 interrupt	false	true	true
EXTI line4 interrupt	false	true	true
EXTI line[9:5] interrupts	false	true	true

Enabled interrupt Table	Select for init	Generate IRQ	Call HAL handler	
	sequence ordering	handler		
USART1 global interrupt	false	true	true	
USART2 global interrupt	false	true	true	
EXTI line[15:10] interrupts	false	true	true	

^{*} User modified value

9. System Views

9.1. Category view

9.1.1. Current

			Middleware			
System Core	Analog	Timers	Connectivity	Multimedia	Security	Computing
DMA			SPH 📀			
GPIO ⊘			USART1 ⊘			
NVIC ⊘			USART2 ⊘			
RCC ♥						
sys 🤣						

10. Docs & Resources

Type Link

Datasheet http://www.st.com/resource/en/datasheet/DM00108832.pdf

Reference http://www.st.com/resource/en/reference_manual/DM00083560.pdf

manual

Programming http://www.st.com/resource/en/programming manual/DM00046982.pdf

manual

Errata sheet http://www.st.com/resource/en/errata_sheet/DM00111498.pdf

Application note http://www.st.com/resource/en/application_note/CD00160362.pdf

Application note http://www.st.com/resource/en/application_note/CD00167594.pdf

Application note http://www.st.com/resource/en/application_note/CD00211314.pdf

Application note http://www.st.com/resource/en/application_note/CD00259245.pdf

Application note http://www.st.com/resource/en/application_note/CD00264321.pdf

Application note http://www.st.com/resource/en/application_note/CD00264342.pdf

Application note http://www.st.com/resource/en/application_note/CD00264379.pdf

Application note http://www.st.com/resource/en/application_note/DM00042534.pdf

Application note http://www.st.com/resource/en/application_note/DM00072315.pdf

Application note http://www.st.com/resource/en/application_note/DM00073742.pdf

Application note http://www.st.com/resource/en/application_note/DM00073853.pdf

Application note http://www.st.com/resource/en/application_note/DM00080497.pdf

Application note http://www.st.com/resource/en/application_note/DM00081379.pdf

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Application note	http://www.st.com/resource/en/application_note/DM00493651.pdf
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Application note	http://www.st.com/resource/en/application_note/DM00209772.pdf
Application note	http://www.st.com/resource/en/application_note/DM00476869.pdf
Application note	http://www.st.com/resource/en/application_note/DM00660597.pdf