ECE552 – Project Report

Introduction

This project entailed designing a 16 bit WISC-S25 microprocessor. Over the semester the project was split into 3 phases which documented the certain milestones which were to be met at certain times. These phases creates an overview of how the project was transformed and maintained whilst more intricate features were added. The three phases can be seen documented below:

Phase 1: This phase explored creating the baseline of the microprocessor which involved creating core modules such as the ALU in which would decide what arithmetic would take place depending on the opcode sent to the ALU. These different arithmetic functions and their opcode can be seen in figure 1.

Phase 2: This phase utilised the baseline which was created in phase 1 and implemented 5 stage pipelining into the system. This entailed using registers to store necessary values for each instruction inbetween the 5 stages: IF, ID, EX, MEM, and WB. This pipelined system would work on a predict-not-taken branch handling system as well as data hazard forwarding (EX to MEM, MEM to EX, and MEM to MEM). As well as this, a global flush/stall logic was also implemented to ensure in order completion of instructions.

Phase 3:

|  |  |
| --- | --- |
| Instruction | Opcode |
| ADD | 0000 |
| SUB | 0001 |
| XOR | 0010 |
| RED | 0011 |
| SLL | 0100 |
| SRA | 0101 |
| ROR | 0110 |
| PADDSB | 0111 |
| LW | 1000 |
| SW | 1001 |
| LLB | 1010 |
| LHB | 1011 |
| B | 1100 |
| BR | 1101 |
| PCS | 1110 |
| HLT | 1111 |

**Responsibilities/Task Breakdown**

|  |  |  |
| --- | --- | --- |
| Phase 1 | Charlie |  |
|  | Peter |  |
|  | Steve |  |
|  | Shane |  |
| Phase 2 | Charlie |  |
|  | Peter |  |
|  | Steve |  |
|  | Shane |  |
| Phase 3 | Charlie |  |
|  | Peter |  |
|  | Steve |  |
|  | Shane |  |