3C7 Digital System Design

LAB F

Shane O'Donnell – 21364002

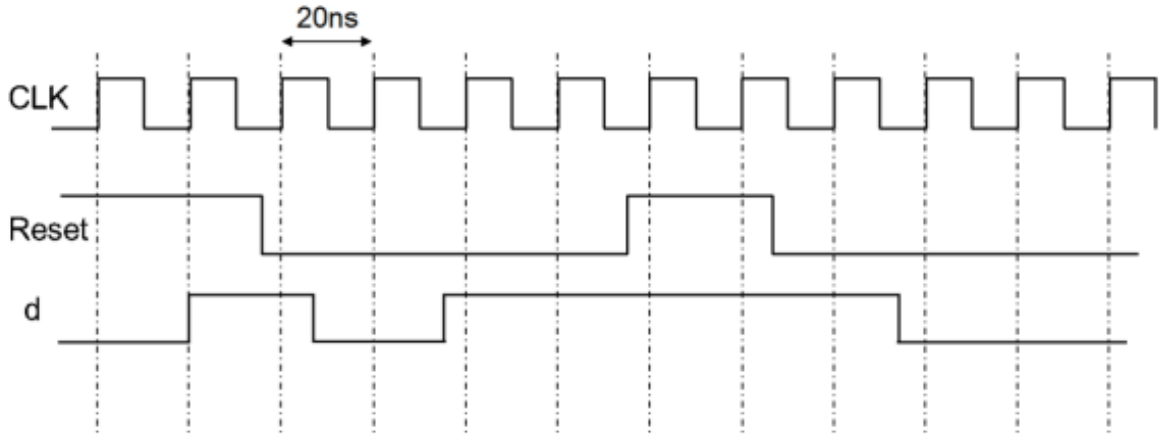
Lab Description:

The purpose of this session is to simulate and explore sequential logic circuits in Vivado and implement them on the Basys-3 Board.

Learning Outcomes:

On completing this lab session, you will be able to:

- Write a Verilog module using sequential logic
- Set up a clock and reset in a Verilog testbench
- Construct an LFSR in Verilog
- Write a simple Verilog testbench for a sequential circuit



Implementation:

This laboratory involved implementing a clock and reset signal within Verilog which would be subsequently implemented onto the basys 3 board to represent a functioning 22 bit LFSR circuit. In order to complete this objective, a further knowledge of clock signals was necessary.

Part a

The first part of this investigation entailed implementing a clock and reset signal using a d-type flip flop circuit. In order to do this a 20ns clock was implemented using a testbench as well the d signal displayed in figure 1 below. The variable q displays the output of the d-type flip flop circuit, from figure 1 it can be seen that the signal is positive when d is positive and the clock signal has a rising edge.

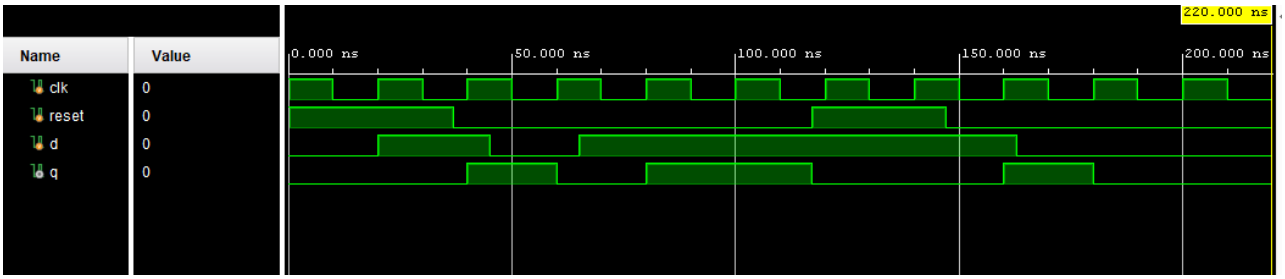


Figure 1: Positive Edge D-type Flip Flop

Once the d-type flip flop was changed to a negative edge flip flop circuit the output signal was altered, this can be seen in the figure 2. The q output is positive when d is positive and the clock signal has a falling edge. The first increment of a positive output q is cut short due to a reset signal pulse.

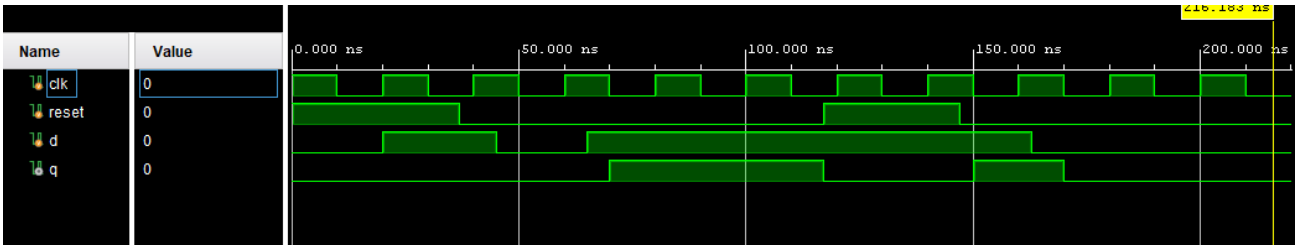


Figure 2: Negative Edge D Type Flip Flop

Part b

The second objective of this laboratory was to design an interface which allows a user to toggle different Fahrenheit values on the board, as well as this the middle button should reset the current value back to 22. The up and right arrow increased the number while the down and left arrow decreased it. In order to accomplish this task, the provided Verilog modules for this lab were utilized and combined using a top module accordingly. The generated Verilog schematic is displayed in figure 3.

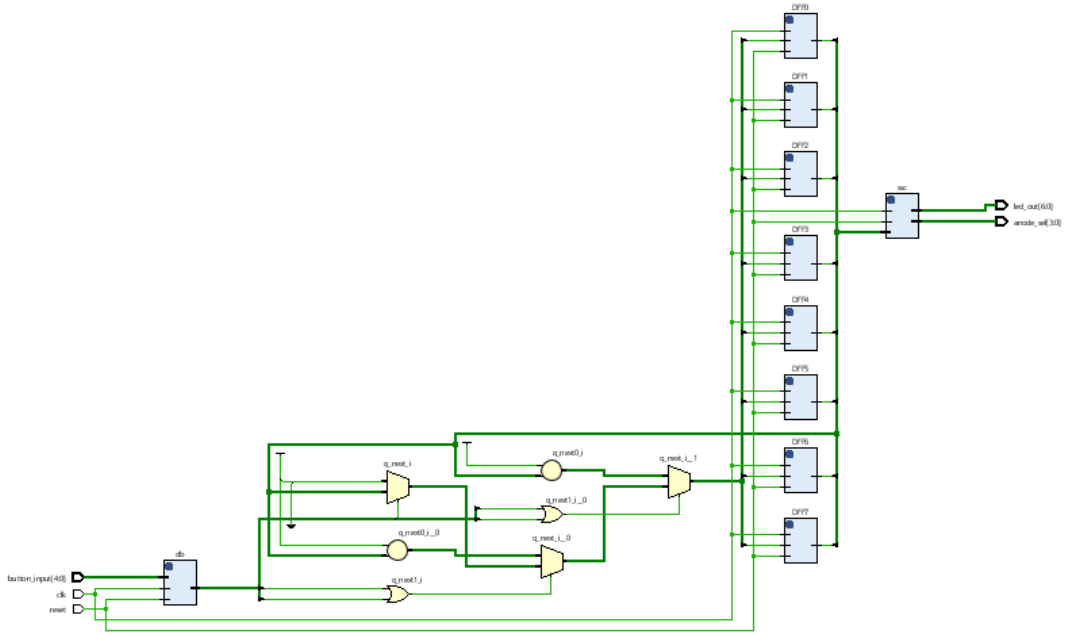


Figure 3: Fehrenheit counter schematic

Once the design was programmed to the board it was possible to adequately test the circuit to ensure the necessary functions operate as needed. This can be seen in figure 4 as the screen outputs a 22 value due to the middle button on the board being pressed.

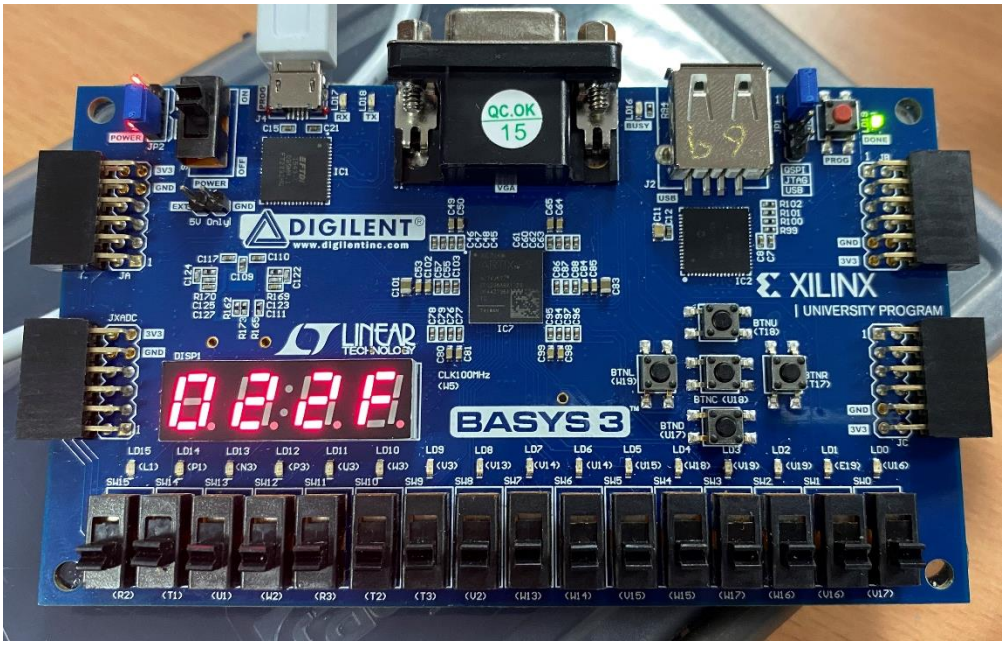


Figure 4: Basys 3 board targetting

Part c

For part c of this lab a 22 bit nxor LFSR (Linear Feedback Shift Register) was to be implemented. The seed number for this investigation was decided by performing a bitwise nxor for the users board number and the last three digits of their student number. In the case of this report this was outputted to be “11111111111111110111000”. The following diagram in figure 5 displays the use of an xnor gate on bits 17 and 22 in order to decide the output of the generated bit to be shifted to the first bit position. Once this generated bit is shifted accordingly the rest of the remaining bits shift upwards one space.

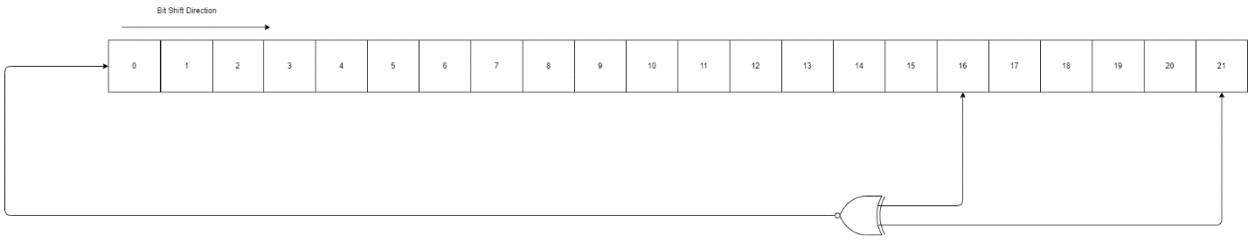


Figure 5: Flow Diagram of 22 bit LFSR

In order to ensure the LFSR circuit functioned correctly a relevant testbench was created, figure 6 displays the a functioning lfsr register which displays whether a one or zero bit is generated, these generations are monitored using both a one and zero counter.

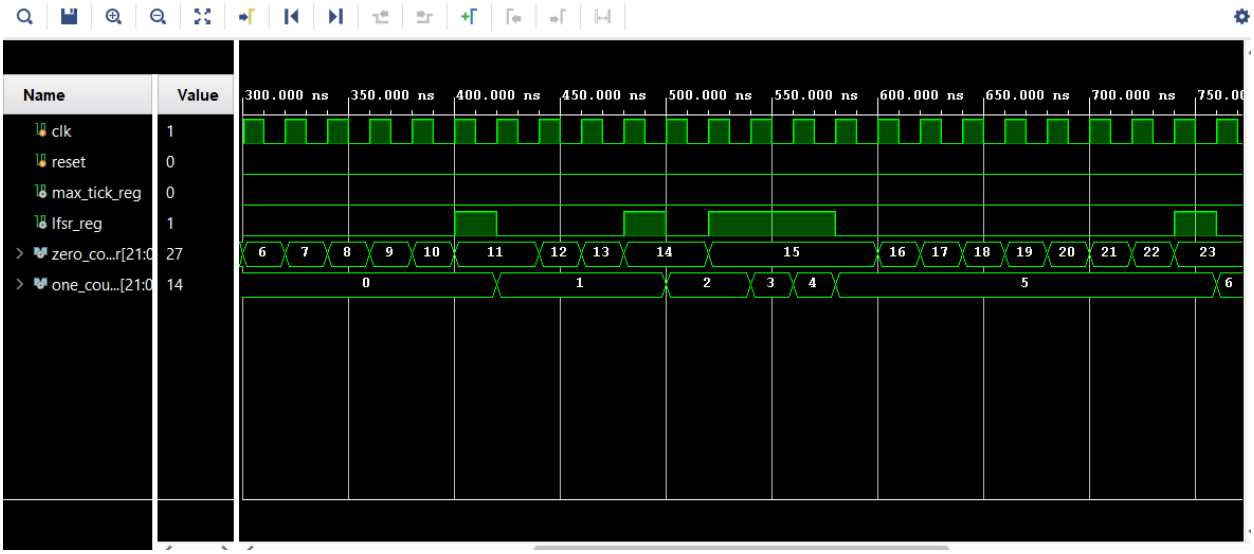


Figure 6: LFSR output

As well as this to ensure the count will reset once the seed value is outputted once more figure 7 displays the counters resetting to zero once this value is met. In order to ensure that this event is occurring at the correct time the following calculations were done below; the final values proves that this reset occurred at the correct time.

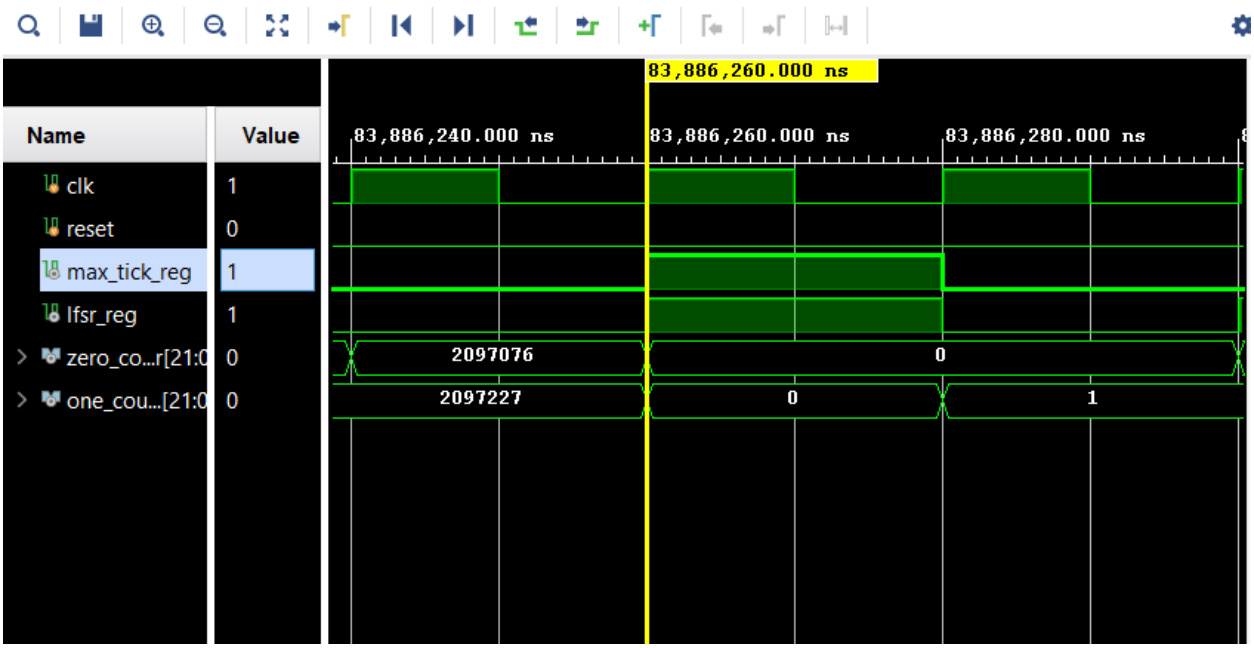


Figure 7: Counter reset of LFSR

$$reset\ time = (2^{22} - 1) * 20\ nanoseconds$$

$$reset\ time = 83{,}886{,}060\ nanoseconds$$

$$83{,}886{,}260\ nanoseconds = 83{,}886{,}060\ nanoseconds + 200\ nanseconds\ (initial\ reset)$$

Part d

For part d, the objective entailed targeting the design from part c on to the Basys 3 board and initialize the clock signal to operate at a 1Hz frequency. In order to do this a top module was initialized as well as an independent clock module. This is displayed below using the provided block diagram.

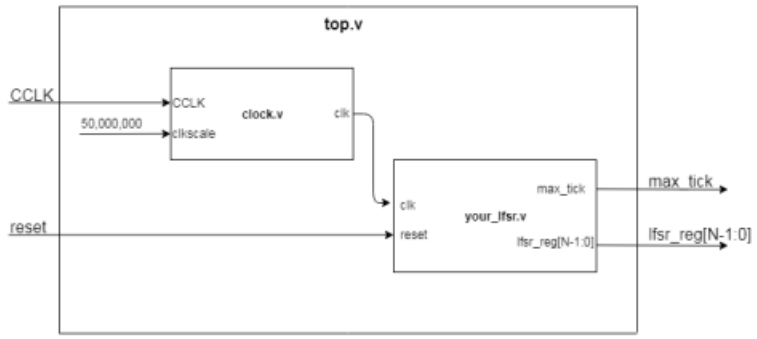


Figure 8: Provided Diagram of Top Module connections

After constructing the necessary modules and initializing the necessary connections to the top module the following schematic displayed in figure 9 was generated using Verilog. Similar to the provided schematic, the clock module has one input from the top module and one output which is then used as the clock signal for the LFSR module. The R2 switch was utilized to switch the LED display in order to display both the first and second half of the 22 bit number.

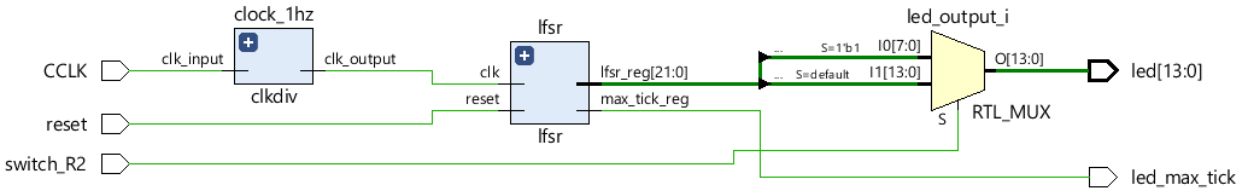


Figure 9: Verilog Schematic

Basys 3 Board

In order to ensure the design created worked as needed, it was necessary to target the design to the provided Basys 3 board. For our design, the rightmost LED was defined at the max_tick_reg input, therefore when the LFSR cycles through 4194303 cycles this LED will light up. The LED next to the right most LED was skipped to add more clarity to where the 22 bit number begins, the rest of the LED's are then utilized to output the first 13 bits of the number. Once the R2 switch is turned on the output changes so that the max_tick_reg and skipped LED's stay the same but the rest of the necessary LED's are used to output the rest of the 22 bit number.

Figure 10 displays the LED output on the basys 3 board, as seen in the photo the R2 switch is off so the board is displaying the first 13 bits of the 22 bit number.

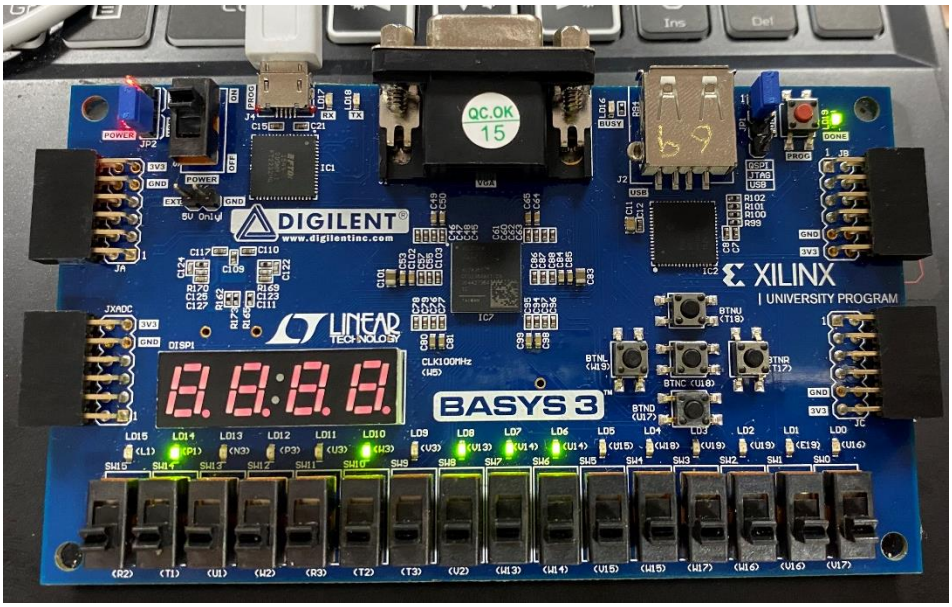


Figure 10: Board target displaying current first 13 bits

In Figure 11 the use of the R2 switch is shown in order for the onboard LED's to output the second part of the 22 bit number (bit 14 to 22).

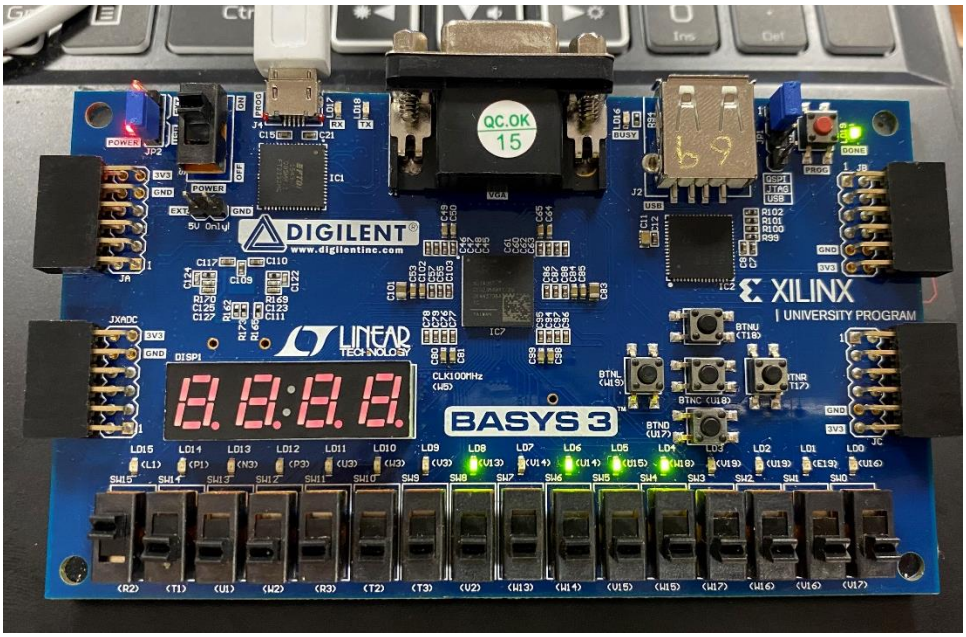


Figure 11: Board target displaying bits 14 to 22 using the R2 switch

Figure 12 displays the reset switch being utilized as well as the R2 switch being on, while the reset watch is kept on the bit generation is paused and brought back to start.

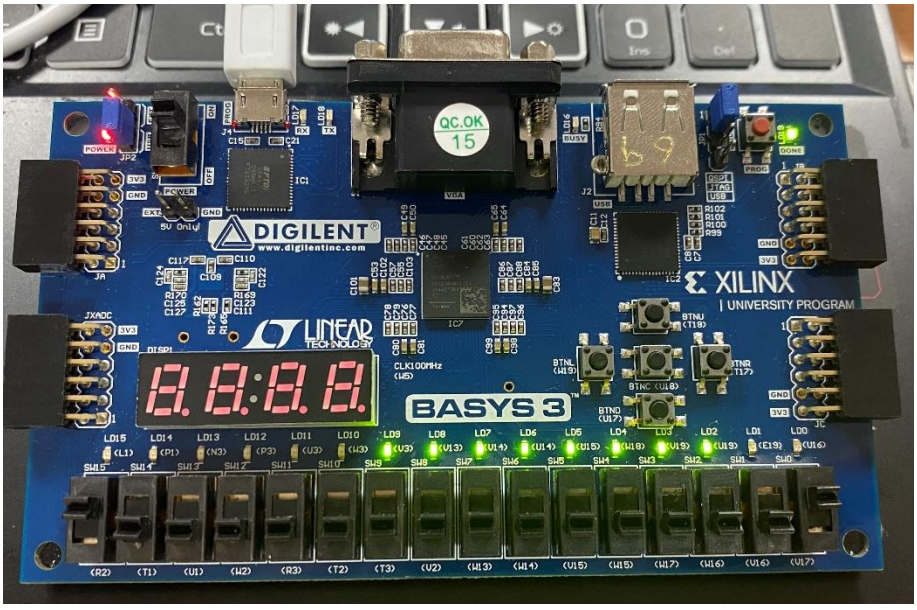


Figure 12: Board target utilizing reset switch

Conclusion

To conclude, the 22 bit lfsr and 1Hz clock signal was successfully implemented onto the board. Due to the length of the 22 bit number and the constraint of the limitation of the basys3 board only supplying 16 onboard LED's, this problem was intuitively tackled utilizing the switches present on the board to change the view of the bit length.

Appendix

The relevant Verilog files are provided in this submission and uploaded accordingly.