AN10997

TDA8035 Smart Card Reader

Rev. 1.3 — 4 October 2012 **Application note**

Document information

Info	Content
Keywords	TDA8035HN, Smart Card Interface, Pay TV, STB, NDS, ISO 7816-3
Abstract	This application note describes the smart card interface integrated circuit TDA8035HN. This document helps to design the TDA8035HN in an application. The general characteristics are presented and different application examples are described.

Revision history

Rev	Date	Description
1.3	20121004	Update DC/DC capacitors description
1.2	20120404	Entering test mode description
1.1	20120124	PRESN pull-up resistor calculation added
1.0	20110401	Initial version

Contact information

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1. Introduction

1.1 Presentation

The TDA8035HN is a smart card interface device forming the electrical interface between a micro controller and a smart card. This device mainly supports asynchronous cards (micro controller-based IC cards).

The electrical characteristics of the TDA8035HN are in accordance with NDS requirements (IRD Electrical Interface Specifications doc n° LC-T056) and also comply with ISO7816-3 for class A, B and C cards.

The TDA8035HN can be used in various applications such as pay-TV, Point-Of-Sale terminals (POS), public phones, vending machines, and many conditional access applications (i.e. Internet,..).

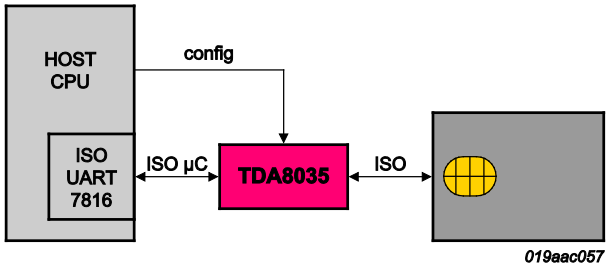


Fig 1. Simplified interfacing view

In the whole document, the TDA8035HN will be referred as TDA8035.

2. Power supply

2.1 Power supply pins

Two input pins are used to supply the TDA8035: $V_{DD(INTF)}$ and V_{DDP}. One voltage is internally generated by the TDA8035 and used for the internal digital part. It is available on V_{REG} pin for external decoupling.

$V_{DD(INTF)}$ is dedicated to the interface supply. All signals which are interfaced with the host are referenced to this voltage supply.

The next table describes all the pins that must be referenced to $V_{DD(INTF)}$.

Table 1. $V_{DD(INTF)}$ referenced pins

Pin name	Comment
IOUC	Smart card data. Controlled by the microcontroller
PORADJ	External configuration of $V_{DD(INTF)}$ supervision threshold
CMDVCCN	Smart card activation. Controlled by a microcontroller GPIO
CLKDIV1	Control of the clock division. Can be controlled by the microcontroller or connected directly to GND or $V_{DD(INTF)}$
CLKDIV2	Control of the clock division. Can be controlled by the microcontroller or connected directly to GND or $V_{DD(INTF)}$
EN5V_3VN	Choice of the smart card voltage. Can be controlled by the microcontroller or connected directly to GND or $V_{DD(INTF)}$
EN1.8VN	Choice of the 1.8V smart card voltage. Can be controlled by the microcontroller or connected directly to GND or $V_{DD(INTF)}$
RSTIN	RST pin management. Controlled by a microcontroller GPIO
OFFN	Output to the host. Must be connected to the microcontroller and therefore have the same level
XTAL1	External oscillator, or crystal input
XTAL2	Crystal output
CS	Chip select signal
PRESN	Not connected to the microcontroller but reference to $V_{DD(INTF)}$. The smart card connector presence switch must use $V_{DD(INTF)}$
AUX1UC	Management of AUX1. Controlled by the microcontroller
AUX2UC	Management of AUX2. Controlled by the microcontroller

V_{DDP} is used to supply the DC/DC converter of the TDA8035 and the internal regulator used to generate V_{REG}. 校准电压

V_{REG} supplies the core of the TDA8035. It is generated by the TDA8035. Its value is always 1.8 V. 一直都是1.8V

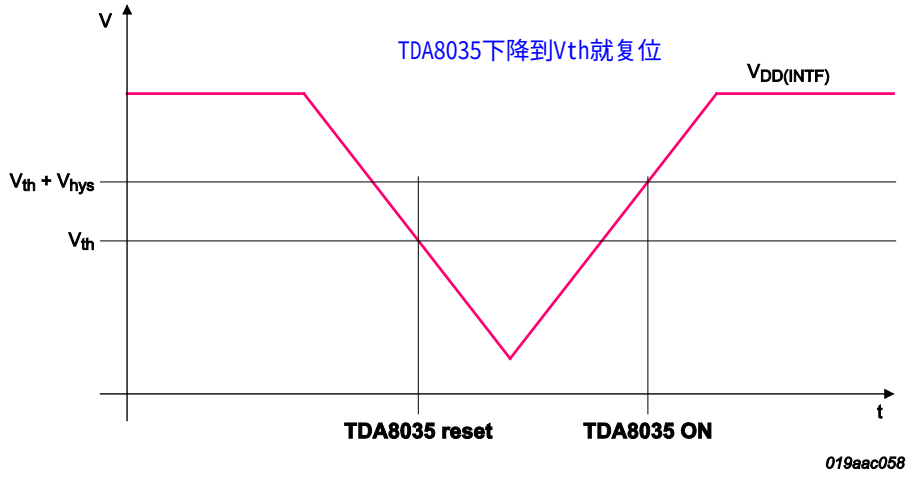
2.2 Supply supervisor 监管

2.2.1 Main principles

The TDA8035 supervises the voltage level of V_{REG}, V_{DDP} and $V_{DD(INTF)}$. For V_{REG} and V_{DDP} supervision, the threshold is internally fixed. For $V_{DD(INTF)}$, the threshold can be fixed either internally or externally using the PORAdj pin.

The following figure explains the supervision for all the supplies.

Then the table gives the threshold values for each input.



(1) When one power supply input falls below its corresponding threshold, the TDA8035 is in reset mode. When all the levels are above their threshold + the hysteresis, the TDA8035 is ON.

Fig 2. Supply supervisor principles

2.2.2 Supervision with PORAdj used

The TDA8035 allows to fix externally the threshold on $V_{DD(INTF)}$. This can be done by using an external resistor bridge on the PORAdj pin.

The supervision principle is given in the next two pictures:

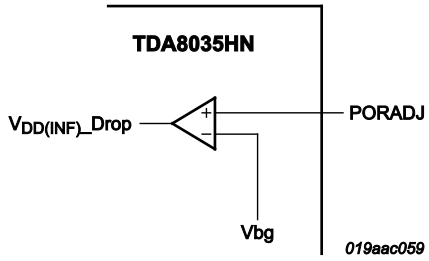


Fig 3. $V_{DD(INTF)}$ supervision – PORADJ level detector

The TDA8035 compares the pin voltage level on pin PORADJ to an internal voltage reference called Vbg.

When PORADJ falls below Vbg, the TDA8035 is reset:

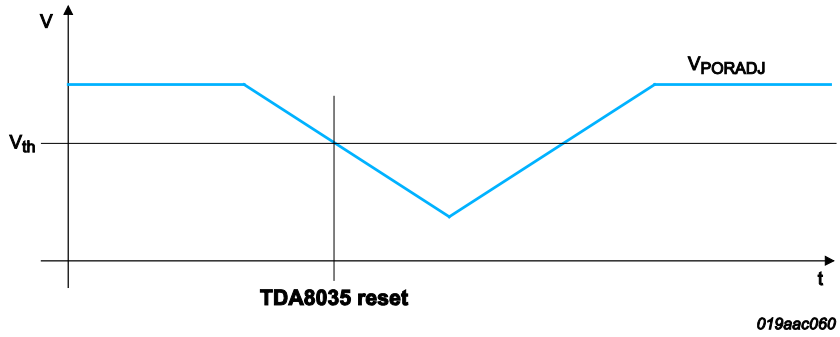


Fig 4. $V_{DD(INTF)}$ supervision – Reset when PORADJ falls

In order to set a specific supply supervisor value on $V_{DD(INTF)}$, a resistor bridge referred to $V_{DD(INTF)}$ must be connected to PORADJ:

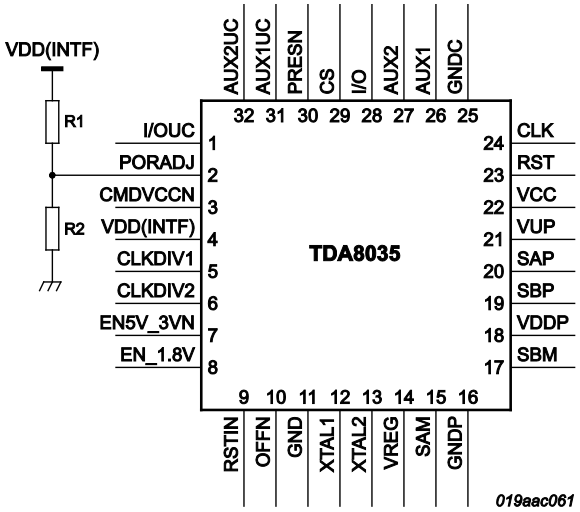


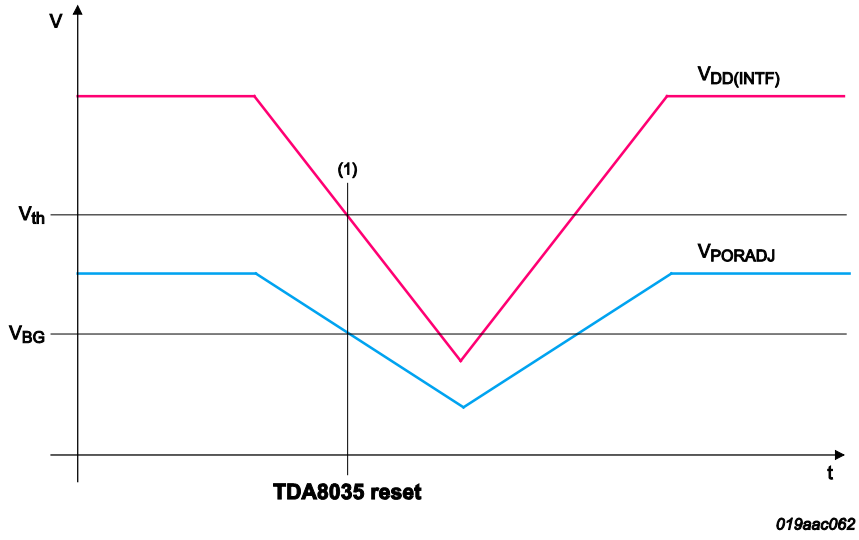
Fig 5. $V_{DD(INTF)}$ supervision – Resistor bridge

In this case $V_{PORADJ} = V_{DD(INTF)}.R2/(R1+R2)$ and $V_{DD(INTF)}$ is monitored indirectly: the TDA8035 enters the reset mode when $V_{DD(INTF)}.R2/(R1 + R2)$ falls below Vbg.

This corresponds to a “virtual” threshold on $V_{DD(INTF)}$ which value is obtained when

$Vbg = V_{DD(INTF)}.R2/(R1+R2)$ ➔ $V_{DD(INTF)} = Vbg.(1+R1/R2)$

This virtual threshold is the Vth corresponding to $V_{DD(INTF)}$. This is called virtual as $V_{DD(INTF)}$ is never compared to Vth. Only V_{PORADJ} is compared to Vbg. The following drawing shows this behavior:



(1) When $V_{DD(INTF)}$ falls below V_{th_VDDI}, V_{PORADJ} falls below Vbg then the drop-off is detected

Fig 6. $V_{DD(INTF)}$ supervision – Virtual $V_{DD(INTF)}$ threshold Vth

The resistor bridge is needed only in the case a specific threshold on $V_{DD(INTF)}$ must be chosen for the application, but in the general case, $V_{DD(INTF)}$ can be input directly on PORADJ. 一般情况下，PORADJ可以直接和VDD相连

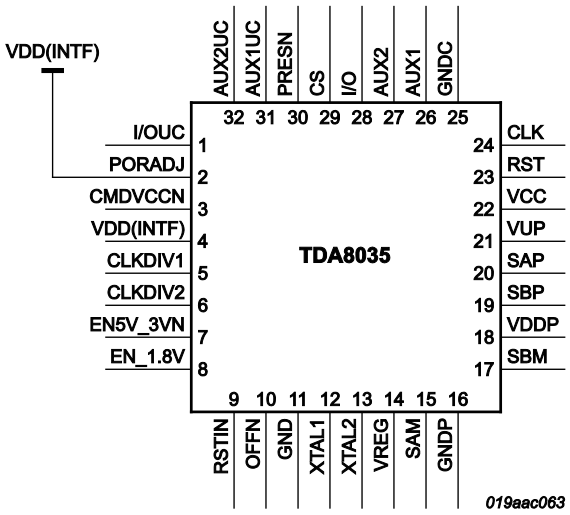


Fig 7. $V_{DD(INTF)}$ supervision – No resistor bridge

This is a particular case of the previous description with R1 = 0Ω and R2 = ∞.

Here Vth = Vbg.(1+R1/R2) = Vbg.

2.2.3 Summary

The following table gives the different threshold values for each supply input pin.

Table 2. Supply supervisor - Typical threshold values

	V_{REG}	V_{DDP} (VCC = 5V)	$V_{DD(INTF)}$ (No PORADJ bridge)	$V_{DD(INTF)}$ (PORADJ bridge used)
Typ. V_{th}	1.45V	2.25V	0.86V	0.86 x (1+R1/R2)
Typ. V_{hys}	100mV	100mV	60mV	60mV

2.3 DC/DC Converter

The TDA8035 embeds a DC/DC converter that allows converting a voltage level as low as 2.7 V to an output on the card side up to 5 V.

This block is supplied through VDDP, and its reference ground is GNDP.

2.3.1 Schematics

This DC/DC converter works with a capacitor step-up mechanism, and uses 3 capacitors on SAM-SAP, SBM-SBP and VUP

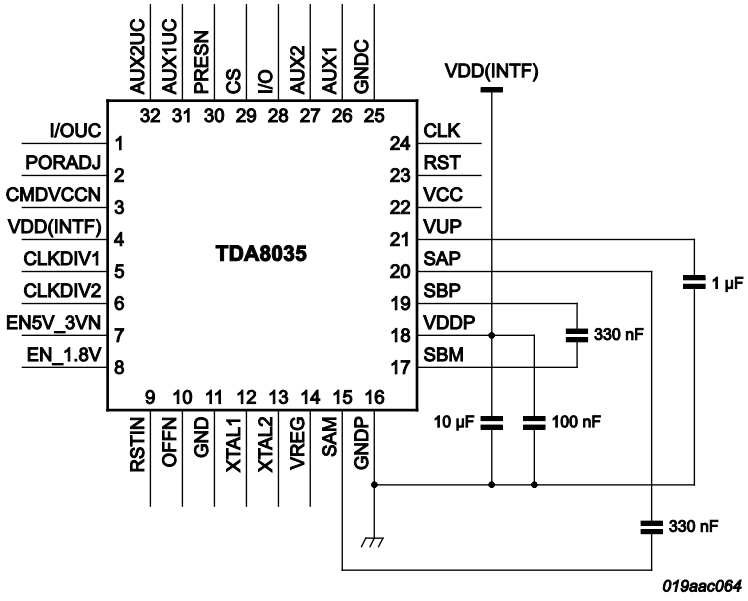


Fig 8. DC/DC converter capacitors

The DC/DC converter operates as a charge pump using capacitors on SAx pins, SBx pins and Vup. With these 5 pins the converter can operate as a voltage follower, doubler, or even tripler. This allows to use a VDDP down to 2.7 V, and then allows to use the same level voltage for VDDP and VDD(INTF).

2.3.2 Layout

The DC/DC converter components layout must be implemented respecting the following guidelines:

- The 10 µF capacitor on VDDP has to be routed close to the VDDP pin and with a very short and low resistive connection to the GNDP pin.
- The 1 µF capacitor on Vup has to be placed close to Vup and with a very short and low resistive connection to the GNDP pin.
- The 100 nF on VDDP must be placed close to the VDDP pin.
- The capacitors on SAP/SAM and SBP/SBM must be placed close to their pins.

2.4 Low consumption

The TDA8035 has two different low consumption states where the current consumption differs:

- Shutdown mode, when no card is active and the TDA8035 is in stand by
- Deep shutdown mode, when the TDA8035 is forced in a sleeping state.

2.4.1 Shutdown mode

CMDVCCN=1

CMDVCCN是高的时候，VCC是低

The shutdown mode is the default mode when the card is not active (CMDVCCN HIGH). The max consumption in this mode is 500 µA.

Active 时序需要改写，TDA8024

Due to this mode, the activation timing changes a bit compared to the TDA8024. Refer to the “Activation” chapter to see the exact difference induced by this mode.

In this mode the supervisors are active, card presence detection is available.

2.4.2 Deep shutdown mode

CMDVCCN=1，EN5V3VN=0，EN1V8N=0

The deep shutdown mode is a very low consumption mode (2 µA max). This mode can be entered when the card is not active (CMDVCCN HIGH) by tying EN5V3VN and EN1V8N to the LOW state.

也就是说，OFFN检测到卡插入的时候，改变EN5V3VN的值

In this mode, the supervisors are turned off, but the presence detection is still available: the OFFN pin follows the status of the presence (PRESN inverted).

OFFN跟踪ＰＲＥＳＮ的状态

！此时TDA8035不能用，卡只能等待卡插入

当没有卡插入的时候，可以作为这个模式

This mode can for example be used when no card is present. In this case, the TDA8035 cannot be used and the host can only wait for a card insertion before activating it. The following figure gives a usage example with 5V smart cards:

Note: in the case that in the application the clock is supplied by the host controller, the clock input shall be stopped prior to entering deep shutdown mode.

In case of external crystal, it will be automatically stopped by the TDA8035.

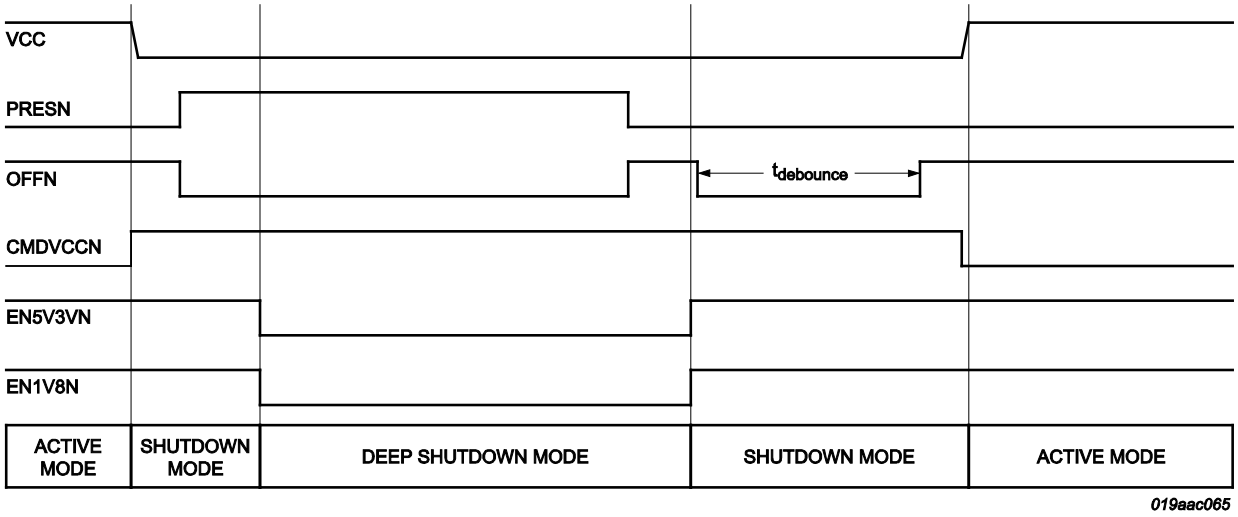


Fig 9. Deep shutdown mode example

In order to use the two configuration pins EN3V5VN and EN1V8N as card voltage selection mode, refer to the chapter 6.1 Card voltage.

3. Input Clock

3.1 Clock selection

There are two possibilities to provide the clock to the TDA8035: using a crystal or applying an external clock provided by the microcontroller.

Any value of crystal can be used from 2 MHz to 27 MHz.

The XTAL pins are referenced to $V_{DD(INTF)}$. In the case of a crystal, the high level of the clock is equal to $V_{DD(INTF)}$, and in case of an input clock, it must be referenced to $V_{DD(INTF)}$.

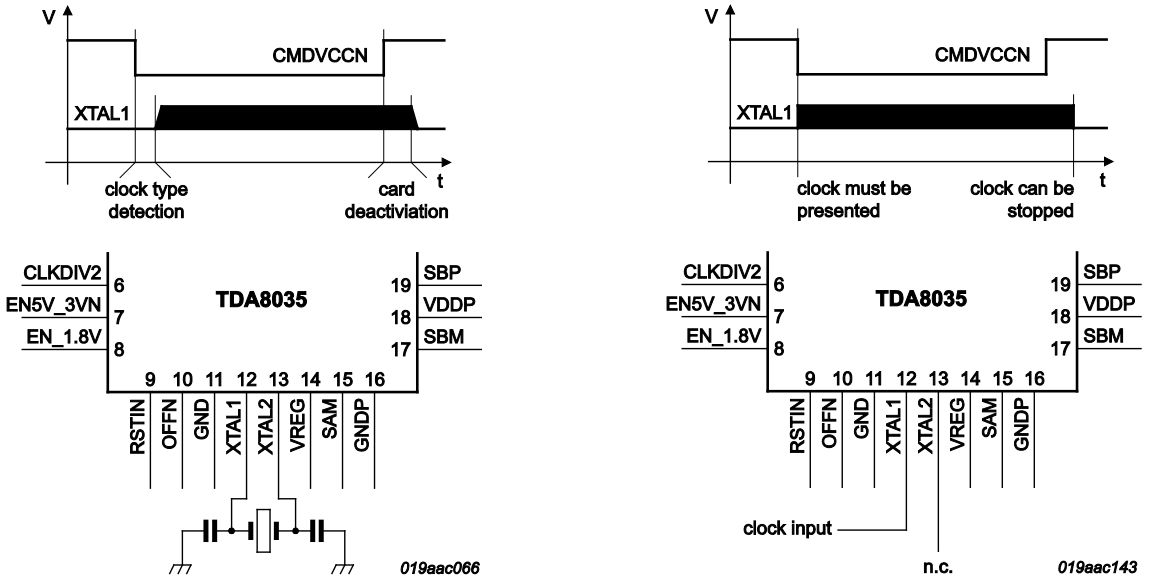
The type of clock is detected automatically by the TDA8035. Hence there is no specific configuration. 自动检测，不怎么需要特别的设置

强制

The clock is not mandatory outside of the card session. This means that if a crystal is used, it will only toggle when CMDVCCN is low. There is no activity on XTAL1 when CMDVCCN is HIGH.

If an external clock signal is applied to XTAL1, it is mandatory to start it before CMDVCCN is LOW, but it is not necessary to apply it when the card must not be activated. 时钟必须在CMDVCCN为HIGH的时候开始起振

The following figures represent the two configurations and the way they are used.



a. XTAL

b. External clock

Fig 10. TDA8035 clock

3.2 Duty cycle 所以还是建议使用TDA生成的CLK来做时钟

On the card side, the duty cycle of the clock line must be in the range 45 % to 55 % to be compliant with most of the standards.

This duty cycle is guaranteed by the TDA8035 for any clock generated by the TDA with a division by 2, 4 or 8.TDA自身产生的时钟都能保证能满足这个0

Therefore, whatever the input clock frequency, duty cycle, voltage levels on the host side, as long as they respect the input specification, the card CLK duty cycle will be in the range.

但是如果外部CLK信号没有经过divided来产生CLK，那么这些都不能保证了。
But if the input clock is not divided to generate the card CLK, the duty cycle will directly depend on the input clock parameters.

The most probable case is having an external input clock which is not centered on $V_{DD(INTF)}/2$. In this case, due to the V_{IL} and V_{IH} parameters, the output clock to the card may not have a correct duty cycle, as shown on the following oscilloscope picture.

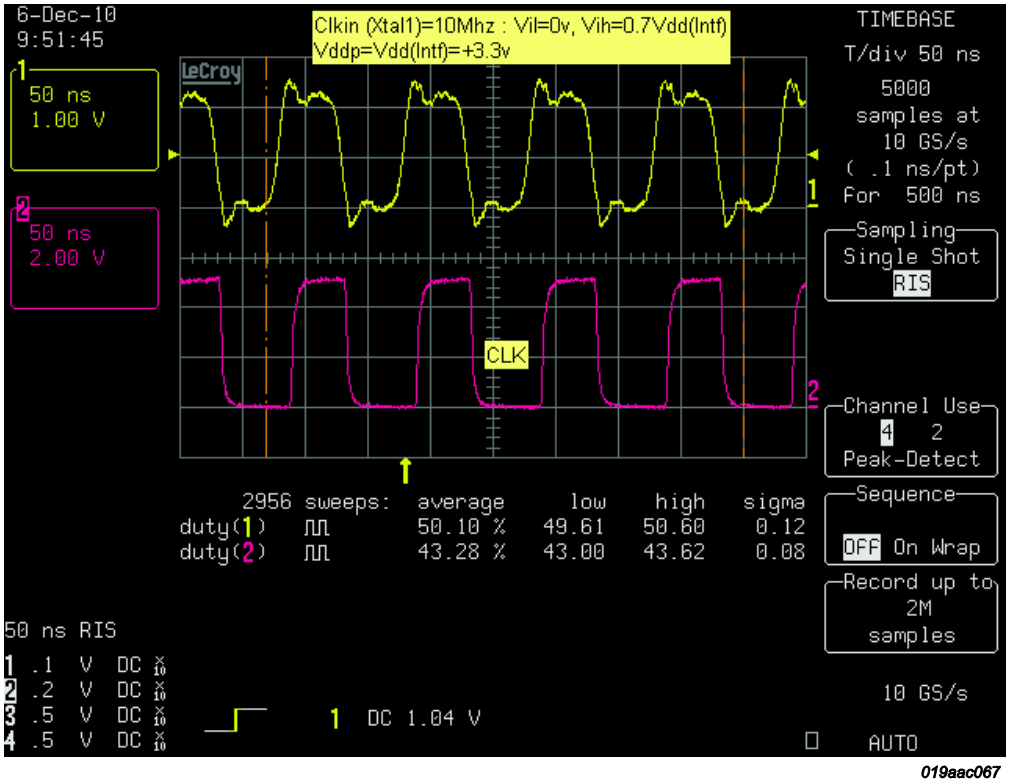


Fig 11. Input clock not centered on $V_{DD(INTF)}/2$

This test shows that even though the input clock has a 50% duty cycle, as it is not centered on $V_{DD(INTF)}/2$, the duty cycle of generated clock on CLK pin is not equal to 50%.

To avoid this issue, it is recommended to center the input clock by adding a serial 56 pF capacitor in serial in the XTAL1 line, as described on the following drawing.

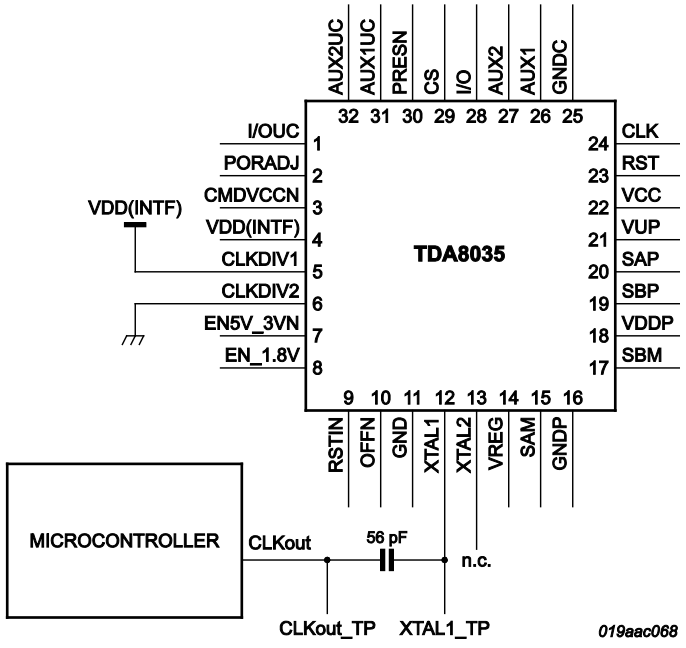


Fig 12. XTAL1 serial capacitor

Thanks to this serial capacitor, the clock signal DC level is cancelled, and the signal is now centered on $V_{DD(INTF)}/2$.

The result is that the CLK line duty cycle is now equal to the input duty cycle.

The result is shown in the next figure, showing the different signals:

- Yellow – Voltage Level on XTAL1_TP
- Blue – Voltage Level on CLKOut_TP
- Pink – Output on CLK (pin #24)

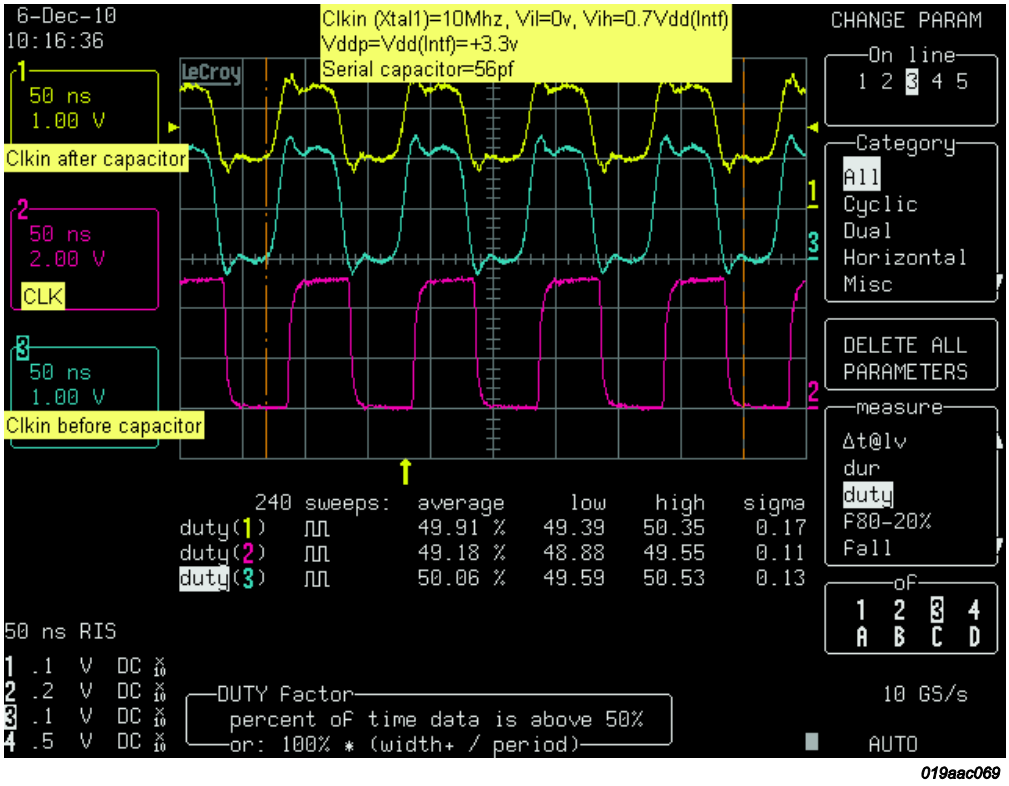


Fig 13. Input clock after serial capacitor correction – Output Duty cycle ~ 50%

The duty cycle is now around 50% on the CLK line.

4. Chip select

The TDA8035 implements a functionality that allows to cascade several devices using the same connection pins. The following signals can be multiplexed:

- CMDVCCN
- RSTIN
- CLKDIV1
- CLKDIV2
- EN5V/3VN
- EN1V8N
- IOUC
- AUX1UC
- AUX2UC
- OFFN

测试成功，CMDVCCN可以控制

4.1 Active device

VCC=1

To drive a TDA8035, its corresponding CS pin must be tied to high level. Then all the configuration pins behaves as expected.

假如CS为低的话，其他所有的pin脚为高阻态

If the CS pin is pulled to low, then all the pins are high impedance 高阻态 and the TDA8035 keeps internally its last configuration. 内部保持了最后一次配置

The following figure shows the behavior, when the TDA8035 is fixed in its state when CS is low. Whatever the value of any configuration pin, the behavior is always the same. The figure shows this behavior with CMDVCCN. The value on CMDVCCN only has an action on the chip when CS is high, or becomes high. 只有CS为high才能用

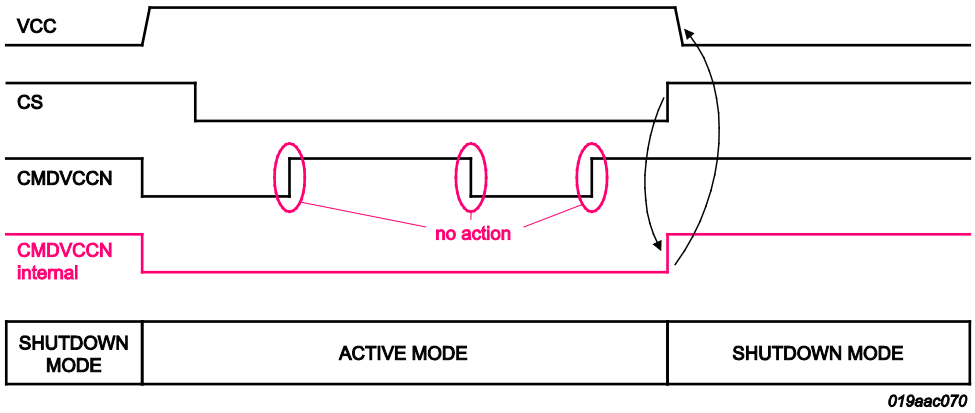


Fig 14. CS action on CMDVCCN behavior

The signal CMDVCCN Internal represents the value that is seen by the TDA8035: the value is latched as soon as CS goes low, and can only change after CS goes back high.

In this case, when CS rises, CMDVCCN internal become high, which causes the deactivation.

OFFN常态为高电平

OFFN保持高位

The behavior of OFFN is affected in the same way by CS. OFFN from any unactive device will always be kept to high level. Then the host must regularly check each device to know its state. 经常检测OFFN电平

The following figure gives an example with a card removal when the device is not active:

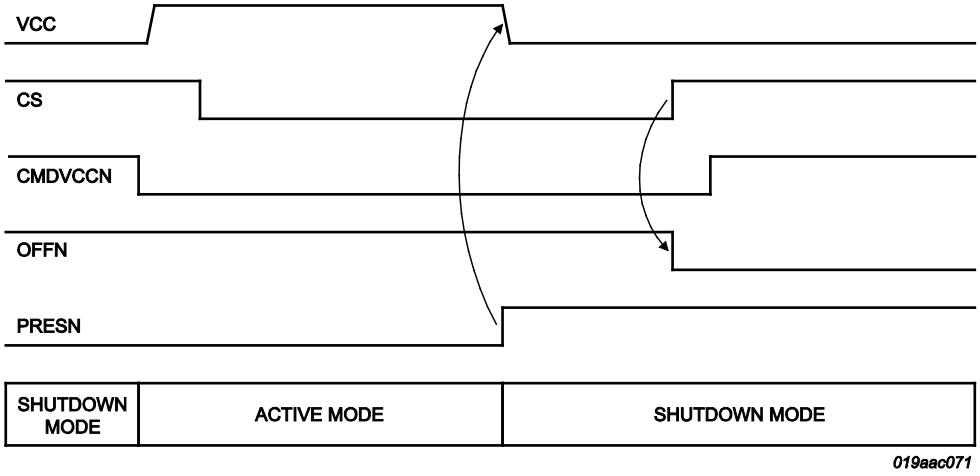


Fig 15. CS action on OFFN behavior

This shows that when the card is removed (or by extension when any fault is detected), the TDA automatically deactivate the card, in order to protect it. 自动失活卡，VCC=0

But the host is not warned if the CS pin is low. It will only know that the fault occurred after it has pulled the CS pin high.

4.2 Schematics

The following schematics give an example on how to connect 2 TDA8035 to a host.

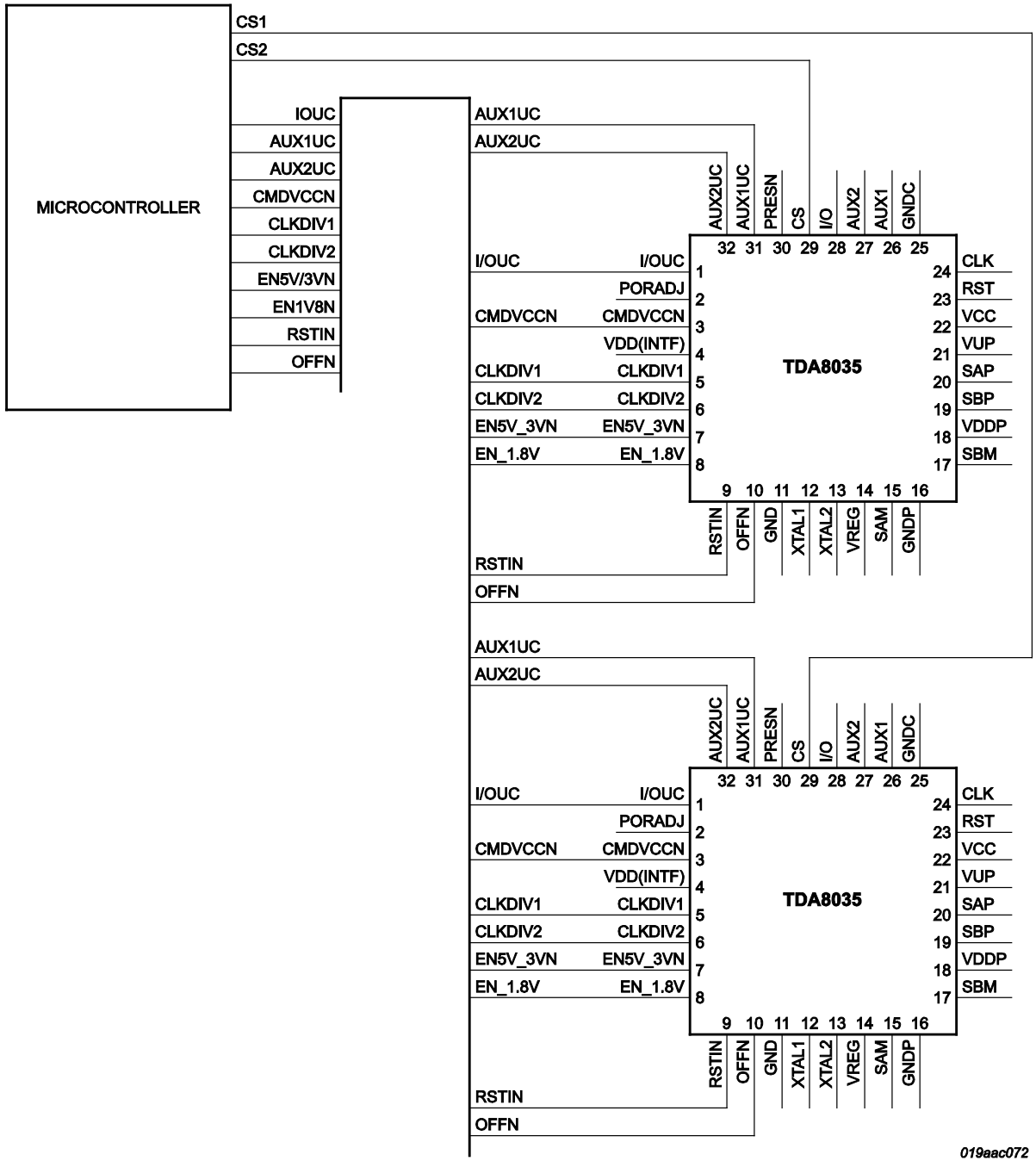


Fig 16. 2 cascaded TDA8035 devices

4.3 Device switch

Using the previous design, some precautions must be taken when switching from one device to another:

Only one CSx signal must be active at the same time

The configuration signals must be saved before clearing the CSx pin, and restored before rising the CSx pin.

The following picture shows the sequence that must be followed to activate smart card from device 1, then activate smart card from device 2, and finally send APDU to device 1.

Only CMDVCCN behavior is shown here, but all input signals must be handled in the same way (save and restore).

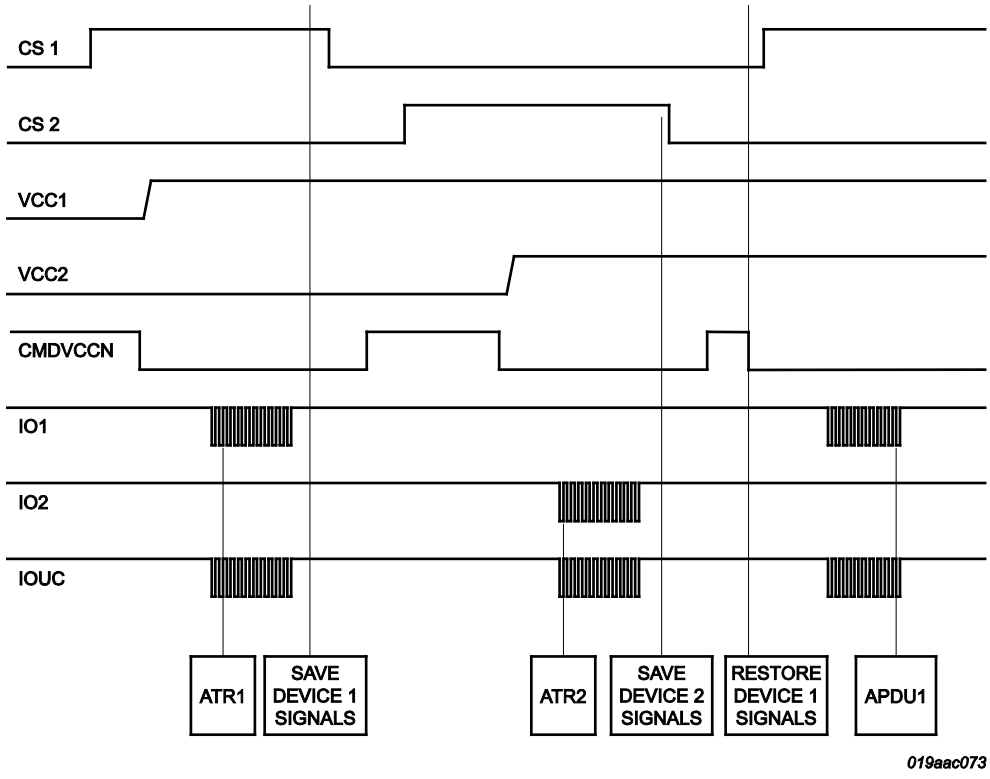


Fig 17. 2 devices management with CS

5. Card connector

5.1 Presence pin

One input pin is available to detect the card presence: PRESN.

This pin is active LOW and embeds an internal resistor to GND. Therefore, when the pin is left open, the card is assumed to be present.

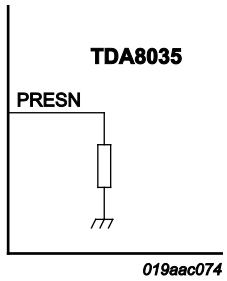


Fig 18. Presence input pin

The way to connect the switch of a smart card connector depends on its gender (normally open or normally closed).

5.1.1 Normally closed presence switch

The TDA8035 is planned to be used with this type of card connector without any external component. The connection of this card connector presence switch is shown in the next figure:

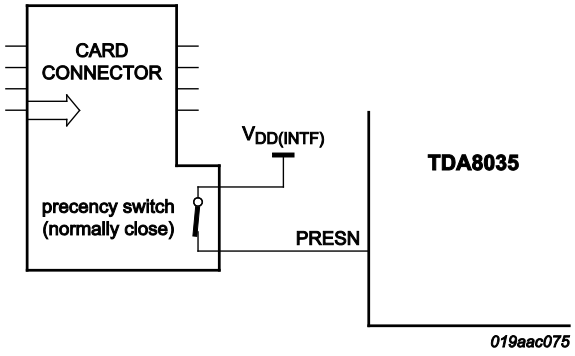


Fig 19. Normally closed card connector connection

When the card is not inserted, the switch is closed, and the PRESN pin is not active and the card is assumed to be absent.

When the card is inserted, the switch is opened and the PRESN pin is driven to low by its internal resistor connected to the ground. The pin is active and the card is seen as present.

5.1.2 Normally open presence switch

5.1.2.1 Schematics

To use this type of card connector, an external resistor is mandatory, and the schematics must be used as shown hereafter:

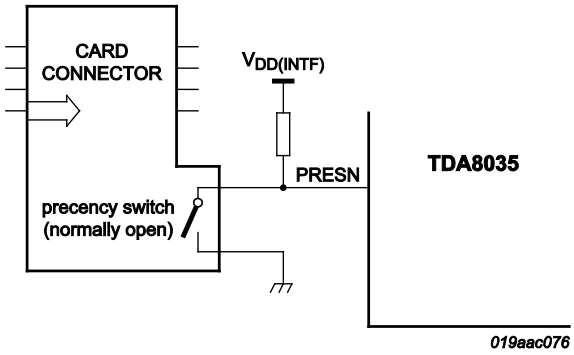


Fig 20. Normally closed card connector connection

When the card is not inserted, the switch is open and PRESN is pulled-up to HIGH level. The pin is not active so the card is seen as absent.

When the card is inserted, the switch is closed. Then the PRESN pin is directly connected to ground. PRESN is then active and the card is seen as present.

5.1.2.2 Pull-up resistor calculation

The PRESN is internally connected to GND through a pull-down resistor.

Depending on the PRESN level, the pull-down resistor can have different value:

- When PRESN is high (not active), the resistor value is 1MΩ (to reduce current consumption)
- When PRESN is low (active), the resistor value is 30kΩ

To choose the pull-up resistor, the 30kΩ value must be taken into account. Indeed, the goal is to pull the PRESN line to $V_{DD(INTF)}$ when the card is removed and the switch opened.

The 30kΩ pull-down has a 20% precision, then the minimum value can be 24kΩ.

If R_{ext} is the external pull-up and R_{int} the internal pull-down, then the PRESN voltage level is:

$V_{PRESN} = V_{DD(INTF)} \times R_{int} / (R_{int} + R_{ext})$

To be detected as high, V_{PRESN} must be greater than V_{IH}. Then the constraint on R_{ext} is:

$R_{ext} > R_{int} \times (V_{DD(INTF)} - V_{IH}) / V_{IH}$

For instance, if $V_{DD(INTF)}$ = 3.3V, then VIH = 0.7*3.3V = 2.31V

As Rint min is 24kΩ, Rext max = 10.28 kΩ.

A maximum value of 10kΩ must be used in this case.

5.1.3 Debouncing

With some card connectors, depending on the mechanical characteristics of the switch, bouncing may be seen on the PRESN pin when a card is inserted or extracted. This bouncing is managed by the TDA8035 which does not transfer exactly the PRESN state to the OFFN pin.

When the card is inserted, the TDA8035 waits for the PRESN pin to be stable for several milliseconds before assuming that the card is inserted. When the card is extracted, the chip acts as soon as the presence is not active. This behavior is summarized in Fig 21:

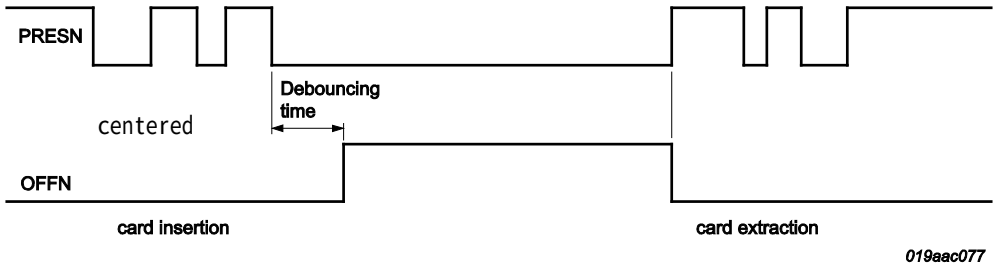


Fig 21. Debouncing feature

5.2 Schematics

To connect the smart card connector to the TDA, only two capacitors are mandatory as external components. The schematic reference is given in Fig 22.

The C1 capacitor must be placed near the TDA8035 and C2 must be connected close to the card connector.

The advised values for C1 and C2 are respectively 220 nF and 220 nF. These values are mandatory to have a ripple on VCC in the specified limits.

Pins C4 and C8 of the card connector (connected to pins AUX1 and AUX2) are optional. They can be left unconnected unless some specific operation using these pins is required.

It is not advised to leave pin VPP (C6) unconnected. It can be connected directly to VCC or GND in accordance with latest ISO 7816 standards. Connecting it to VCC allows it to be compliant with older cards which might not support VPP connected to the Ground.

For more flexibility, the design should include a 0 ohm serial resistor between VPP and VCC. Then the application can be easily adapted if needed.

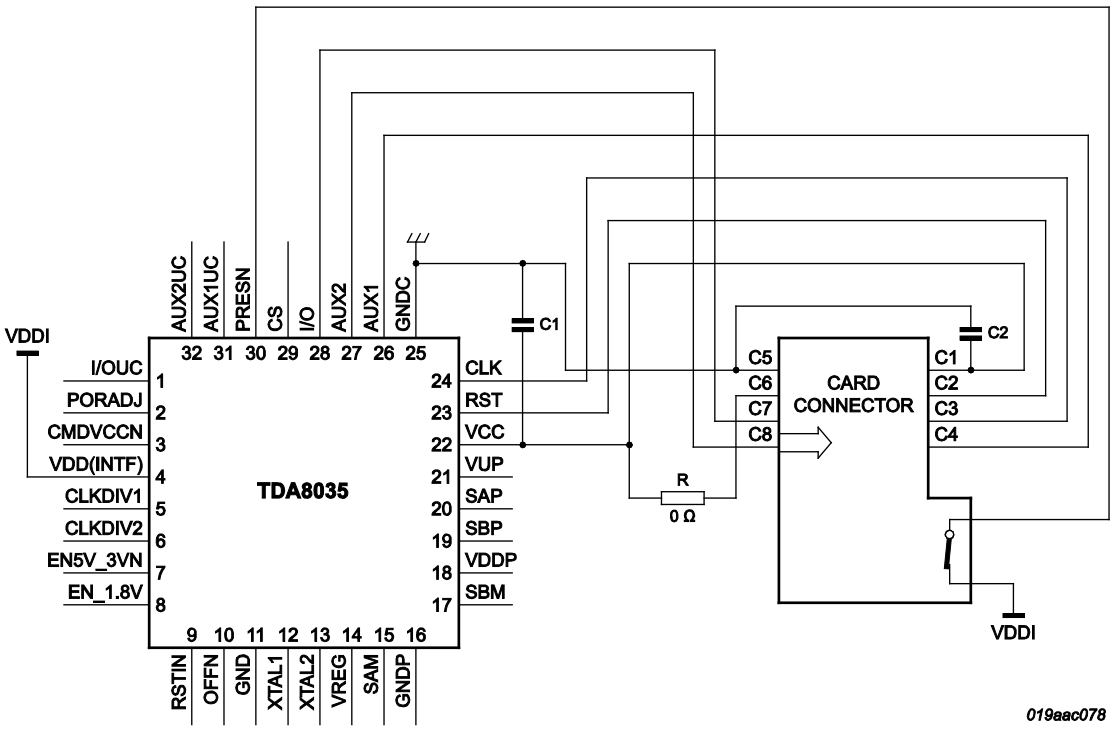


Fig 22. Card connector schematics

6. Card configuration 电压Level和时钟频率 可以配置

The chip can be configured dynamically to operate with the connected card. Two parameters can be controlled: the voltage level and the frequency of the clock signal to the card.

6.1 Card voltage

The voltage level is configured with the following pins:

- EN_1.8VN
- EN_5V/3VN

These pins must be connected to an output of the host. This connection is recommended even for applications using a dedicated 5V card, in order to be easily compliant with the next generation cards. 必须在CMDVCCD=1时进行配置

电压一定要在卡激活前配置好

The voltage level has to be configured before activation. The application MUST NOT change the value of these pins when the card is activated. 卡激活后，EN_1.8VN和EN_5V/3VN不能被改变。

To change the voltage level of the card, the host must deactivate the card, change the voltage level value and then re-activate the card. 为了改变电压，失能卡->改变卡电平值->重新激活卡

These pins are also used for the deep shutdown mode.

The following table gives the action of each combination of these inputs.

Table 3. Select voltage pin behavior

Command	EN5V3VN	EN1V8N
Deep Shutdown	0	0
VCC = 1,8V	1	0
VCC = 3V	0	1
VCC = 5V	1	1

6.2 Card clock

6.2.1 Frequency selection

Two signals are used to select the card clock:

- CLKDIV1
- CLKDIV2

These signals must be connected to the host and determine the division ratio of the input frequency in the clock which is sent to the card when activated.

The following table describes the frequency corresponding to CLKDIV1/2 values. f_{XTAL} is the frequency applied on XTAL1 (crystal or external source).

Table 4. TDA8035 - Clock division selection

CLKDIV1	CLKDIV2	CLK
0	0	$f_{XTAL}/8$
0	1	$f_{XTAL}/4$
1	1	$f_{XTAL}/2$
1	0	f_{XTAL}

6.2.2 Frequency switch

6.2.2.1 General behavior

CLKDIV1 and CLKDIV2 can be changed freely when the card is not active. The values will be adopted on activation.

When the card is active, the frequency applied to the card can be switched by changing CLKDIV1 and CLKDIV2 as shown in the following figure:

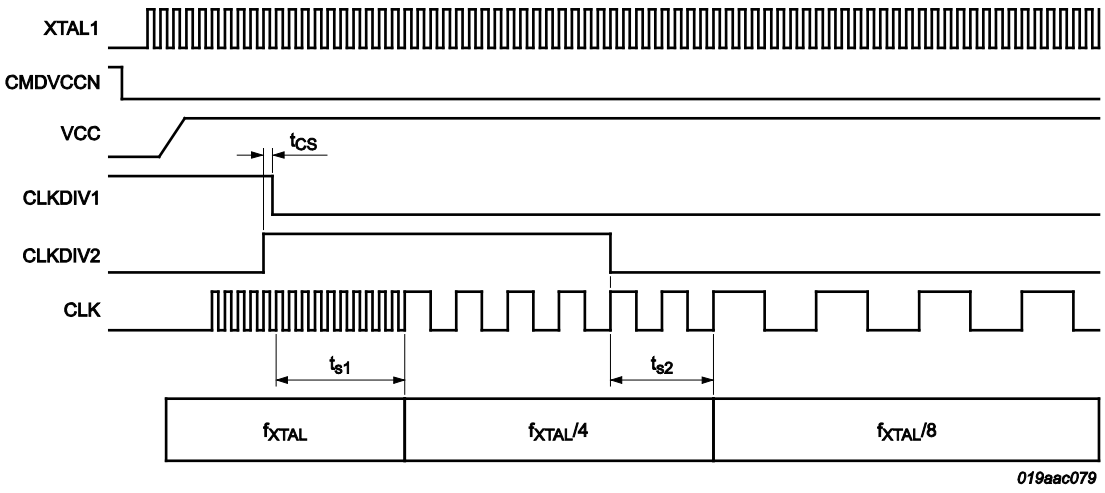


Fig 23. Clock switch during activation

The clock starts with the value specified at activation. Then the clock frequency switch occurs after a maximum of 10 XTAL1 periods after a change is seen on CLKDIV1/2 (t_s<t_{smax} = 10 clock cycles).

6.2.2.2 Simultaneous change on CLKDIV1 and CLKDIV2

When both CLKDIV1 and CLKDIV2 have to be changed simultaneously, a maximum delay of 1 XTAL1 period (t_{cs}) is required between the two edges.

If this timing is not respected, an undesired frequency can be observed during the frequency switchover as shown in the next figure: a switch from f_{XTAL} to $f_{XTAL}/4$ is performed, but a frequency of $f_{XTAL}/2$ is seen during the switchover.

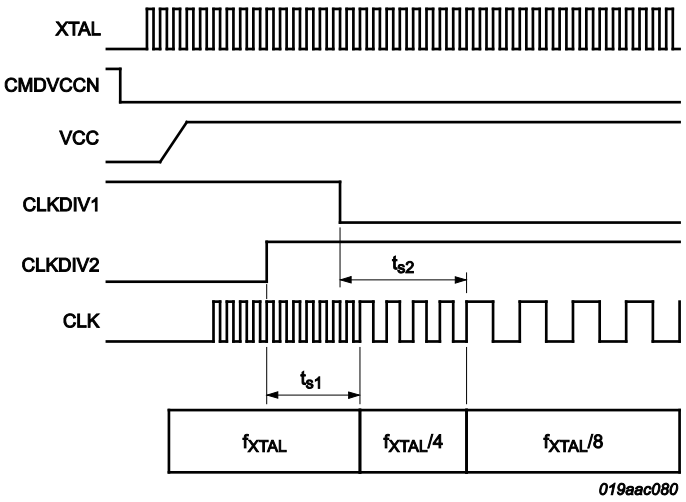


Fig 24. Unwanted frequency during the switch

7. Card Activation / Deactivation

7.1 Difference TDA8024 – TDA8035

7.1.1 Activation timing

The electrical interface between the host and the TDA is based on GPIOs and is exactly the same for TDA8035 as for TDA8024, as soon as the CS pin of the TDA8035 is High.

In the card management, the only difference between the TDA8024 and TDA8035 is the delay between CMDVCCN Low and VCC High.

This time is very low for the TDA8024 while it is equal to 3.42 ms in the TDA8035. (See next chapter)

7.1.2 Software

When the TDA8035 is implemented in a design, the software already developed for the TDA8024 can be reused, with a little modification in one case: TDA8024的代码可以被TDA8035所复用。

If, for the TDA8024, the delay between VCC High and RST High had been set to a low value (below 3.5 ms), this delay must be changed to a highest value, as described in the next chapter.

If the delay is greater than 3.5 ms, then the same code can be reused without any change.

7.1.3 Test Mode / IOUC

Due to the test mode (see chapter **Error! Reference source not found.**), it is mandatory for the host to keep IOUC high when pulling CMDVCCN to low. 在把CMDVCCN拉低时，必须保持IOUC为高

The TDA8024 does not use this test mode. Then the activation always works regardless of the state of IOUC.

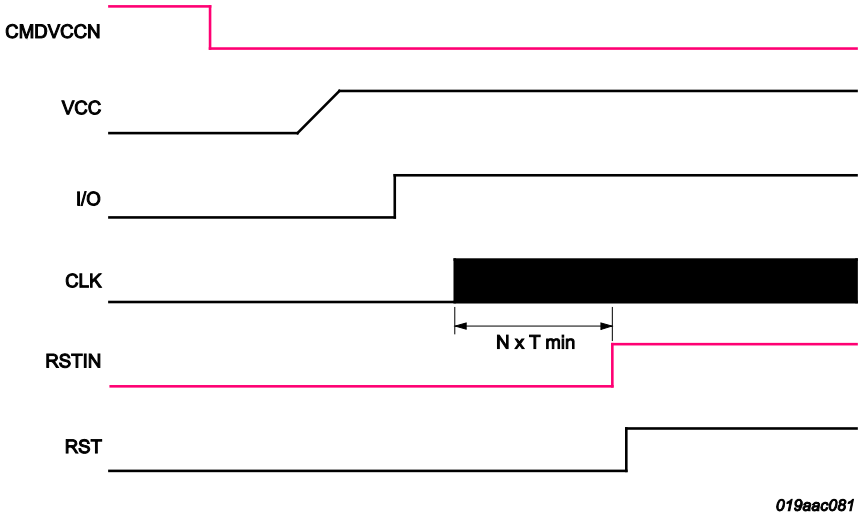
7.2 Activation 激活，CMDVCCN和RSTIN两个信号来激活

7.2.1 Timings

To activate the card, two signals are controlled by the host: CMDVCCN and RSTIN.

The first signal sets the card power supply, the second controls the reset pin of the card.

In the simplest mode, two actions are required from the host to activate the card: reset CMDVCCN and then set RSTIN. The activation sequence is shown in Fig 25.



(1) N = 400 for ISO, 40000 for NDS/EMV, T = Card clock period

Fig 25. Card activation sequence

The input clock must be OK for this sequence to occur. If the clock is supplied externally (no crystal), the clock must be present and stable before the falling edge of CMDVCCN.

The only constraint on the host is due to the standard specifications:

For the ISO 7816, the host must wait at least 400 clock cycles after the clock is active, before asserting RST.

In NDS and EMV specifications, the delay must be 40000 clock cycles

However in this mode, the host has no way of knowing when the clock starts. So it is not possible to count precisely the number of cycles.

To be sure that the right number of clock cycles are respected, the host must know the timing between CMDVCCN fall, VCC rise and CLK start.

These timings are given in the following figure

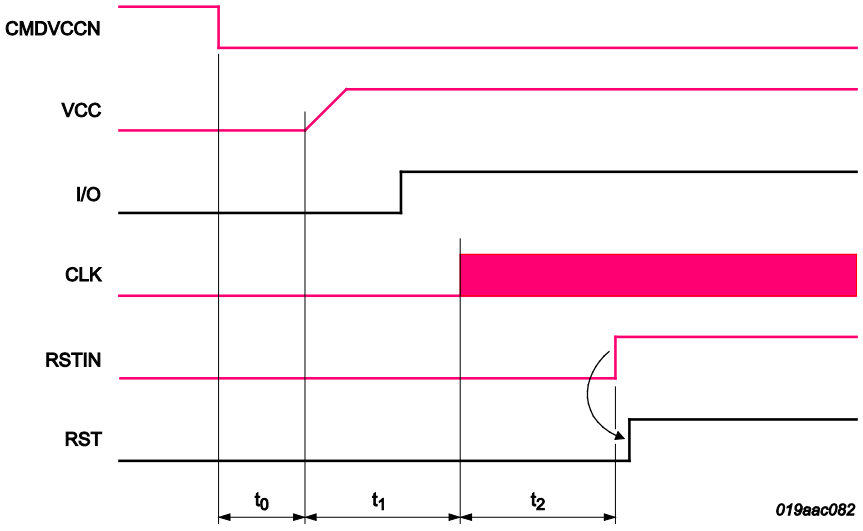


Fig 26. Activation timing

During t_0, the TDA8035 checks for the XTAL1 pin to detect if a crystal is present or if the clock is supplied from the microcontroller, and then waits for the crystal to start.

This time is fixed, even if there is no crystal, and its maximum value is 3.1 ms.

t_1 is the time between the beginning of the activation and the start of the clock on the smart card side. This time depends on the internal oscillator frequency and lasts at maximum 320 µs.

The host must then assume that the smart card clock doesn't start before 3.42 ms after CMDVCCN has been set to LOW.

To set RSTIN, the host must wait at least 400 (ISO) or 40000 (NDS/EMV) clock cycles after the start of CLK. Therefore t_2 depends on the input clock and on the division applied to supply the clock to the smart card and must be managed by the host.

The time between CMDVCCN low and RSTIN high, must respect this condition:

$\mathbf{t_0+t_1+t_2 > 3.42ms + 400/f_{CLK}}$ or

$\mathbf{t_0+t_1+t_2 > 3.42ms + 40000/f_{CLK}}$

7.2.2 IOUC / Test Mode 不要进入Test模式

The TDA8035 implements a test mode for production test purpose. This mode is not intended to be used in application.

This mode is entered by keeping IOUC Low when pulling CmDVCCN to low.

To avoid entering this test mode when activating the card, it is mandatory that IOUC is forced to high when CMDVCCN is pulled to low.

If IOUC is low while activating, the test mode is immediately entered.

It is possible to know that the test mode is entered as OFFN will fall a few nanoseconds after CMDVCCN has been pulled to low. In case of activation error in normal mode (eg shortcut on VCC or too much load on the DC/DC Converter), OFFN should never fall to low until a few milliseconds.

7.3 Deactivation 是由TDA8035完成的时序，CMDVCCN拉低就行了

The deactivation is managed entirely by the TDA8035 sequencer. Deactivation occurs when one of the following events happens:

- Rising edge of CMDVCCN (normal host deactivation)
- A fault is detected:
  - Card removal
  - Overheating
  - Short-circuit or high current on VCC
  - $V_{DD(INTF)}$, VDD or VDDP drop

The deactivation sequence is automatic and fully compliant with the standard. For more details on the activation or deactivation sequence and their timings, refer to the TDA8035 data sheet and ISO 7816-3 standard.

8. Card operation

8.1 I/O, Aux1, Aux2 这些接口，IO、Aux1、Aux2只是简单的电压转换。

The TDA8035 acts as a simple transceiver incorporating a voltage level shifting adaptation for these signals, once the card is activated. 卡激活以后，TDA8035就是个转换器

As there is no other conversion, the host must manage entirely the protocol defined by ISO 7816 (Baudrate, timing, frame…). 由host完成协议内容

The TDA8035 only limits the current on the pins. There is a limitation of 15 mA in both directions.

- I/O is linked to I/OUC,
- AUX1 to AUX1UC, and
- AUX2 to AUX2UC.

I/OUC must be connected directly to an I/O of the host. AUX1UC and AUX2UC can as well be connected to the host or left open if C4 and C8 pin are not used on the card.

8.2 Warm reset RSTIN=RST

The host can operate a warm reset with the TDA8035: as the RST card pin is the copy of the RSTIN pin, the host just needs to apply a falling edge on RSTIN, followed by a rising edge, and the card shall send its ATR again.

9. OFFN Behavior

9.1 Fault detection

The TDA8035 supervises several parameters and warns the host when a problem occurs. The OFFN pin is used to manage this communication with the host. The table below gives the state of the chip in accordance with CMDVCCN and OFFN values.

In this table it is assumed that CS pin is HIGH.

Table 5. Chip state regarding CMDVCCN and OFFN

CMDVCCN	OFFN	State	Comment
HIGH	HIGH	Card is present and not active	
HIGH	LOW	Card is absent	
LOW	HIGH	Card is active and no fault has been detected	This is the state of all card sessions
LOW	LOW	A fault has been detected (card has been deactivated)	The cause of the deactivation is not yet known.
Rising edge	Stays LOW	The fault detected was the card removal	Setting CMDVCCN allows checking if the deactivation is due to card removal. In this case the OFFN pin will stay low after CMDVCCN is high.
Rising edge	Rising edge	The fault detected was not a card removal (card is still present)	If OFFN follows CMDVCCN, the fault is due to a supply voltage drop, a VCC over-current detection or overheating.

9.2 Deep shutdown specific behavior

In shutdown or deep shutdown mode, OFFN is only informing about the card presence. Nothing else is checked.

But one specific behavior on OFFN may occur in case deep shutdown mode is used:

In one case, when exiting the deep shutdown mode, a short high level can be seen on OFFN.

This case is the following:

- Enter the deep shutdown mode with card inserted → OFFN is HIGH
- Extract the card during deep shutdown mode → OFFN falls
- Exit shutdown mode → OFFN goes HIGH, stays HIGH for ~10 µs, and goes LOW.

This behavior is a normal behavior as the digital part is resetting at this time, but it can cause unexpected behavior on the CPU in case the interrupt service routine is not correctly handling this pin.

This behavior is explained by the next drawing.

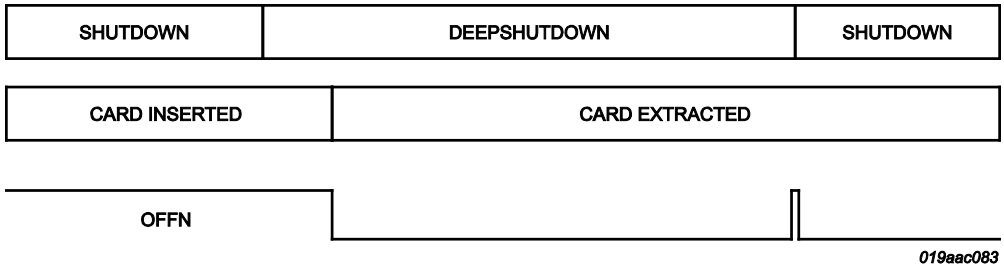


Fig 27. Deep shutdown, card extraction – OFFN behavior

10. Electrical design recommendations

10.1 Decoupling

To ensure proper behavior of the TDA8035, some external components have to be used. All supply pins must be protected against noise.

VCC pin (card contact) needs to be connected to two capacitors: twice 220 nF as described in chapter 5.2: one near the TDA8035 chip and one near the card connector. These capacitors type must be low ESR.

$V_{DD(INTF)}$ and VREG must be protected by 100nF.

VDDP must be protected by two capacitors: one 100 nF to protect particularly against high frequency noise and one 10 µF to absorb slower variations.

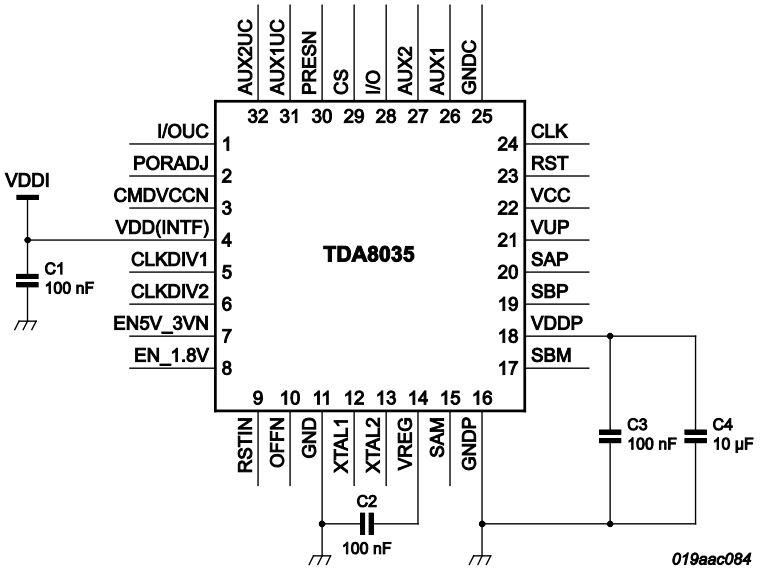


Fig 28. Power supply decoupling strategy

10.2 Layout

For noise reduction optimization, the layout of the design must adhere to the following guidelines.

10.2.1 Decoupling capacitors

Capacitors are mandatory to protect the supply pins as well as the VCC pin (TDA8035 pin and Card connector pin).

Place decoupling capacitors as close as possible to the pin that they protect.

This means that the capacitor must be physically soldered near the chip or the card connector pin, but also with a short and good connection (low resistance) between the protected pin and its capacitor.

The connection between the capacitor pin and the ground must be short low resistive as well.

10.2.2 DC/DC capacitors

The capacitors dedicated to the DC/DC converter (decoupling for VDDP, or pump capacitors on SAP/SAM, SBP/SBM; and VUP), must be physically placed close to their dedicated pin.

In addition, the capacitors on VDDP and VUP must have a short and low resistive connection to the GNDP pin, which is the ground pin dedicated to the DC/DC converter.

The nominal capacitance values must follow NXP recommendations: 330nF between SAP and SAM and between SBP and SBM, and 1µF on VUP.

!! Warning

The nominal capacitor value must be granted at any of the operating voltage.

Depending on the capacitor quality, the nominal capacitor can drop when the DC voltage on the capacitor increases.

As an example, the following chart shows the behavior of a specific 1µF capacitor with a size 0402 (inch):

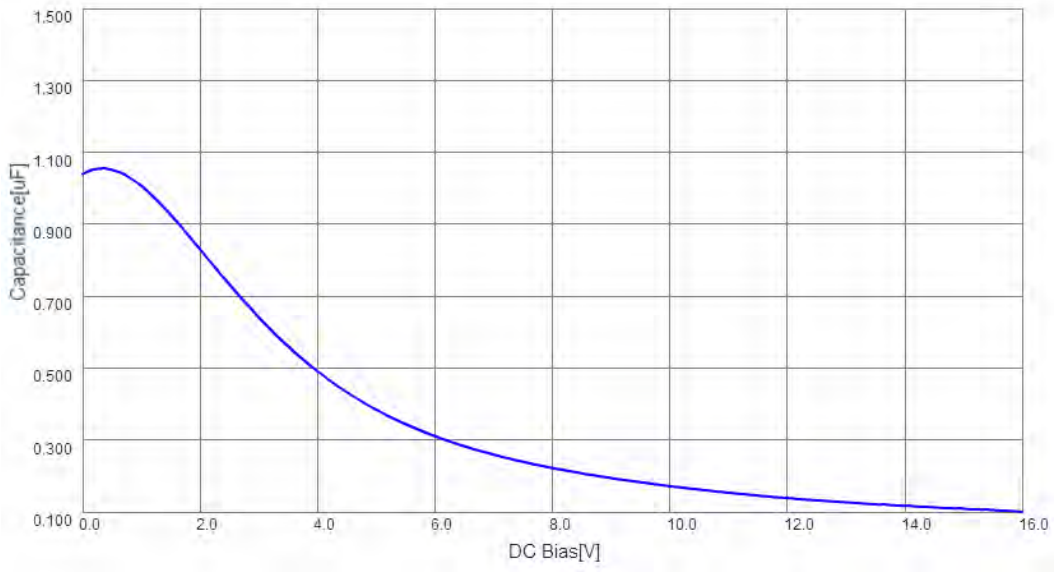


Fig 29. Capacitance vs DC characteristic – Example

This capacitor has a nominal value of 1µF at 0V, but falls to 300nF at 6V, which is the operating voltage on VUP. Then the behavior of the DC/DC is not the expected one.

In order to grant the correct behavior of the DC/DC it is mandatory to limit the drop on the VUP capacitor to less than 30%.

The risk with such a drop is to have voltage generation on VUP that overrides the maximum supported voltage of the TDA8035. This can irreversibly damage the component.

The capacitance nominal value drop is given by the capacitor manufacturer, and depends on several parameters.

The size of the capacitor is one important parameter. In order to keep the capacitance value within the specification, it is advised not to use capacitor size less than 0603 (inch) for the 1µF on VUP.

The following capacitor Part Number from Murata fulfills the above conditions:

GRM188R61A105KA61

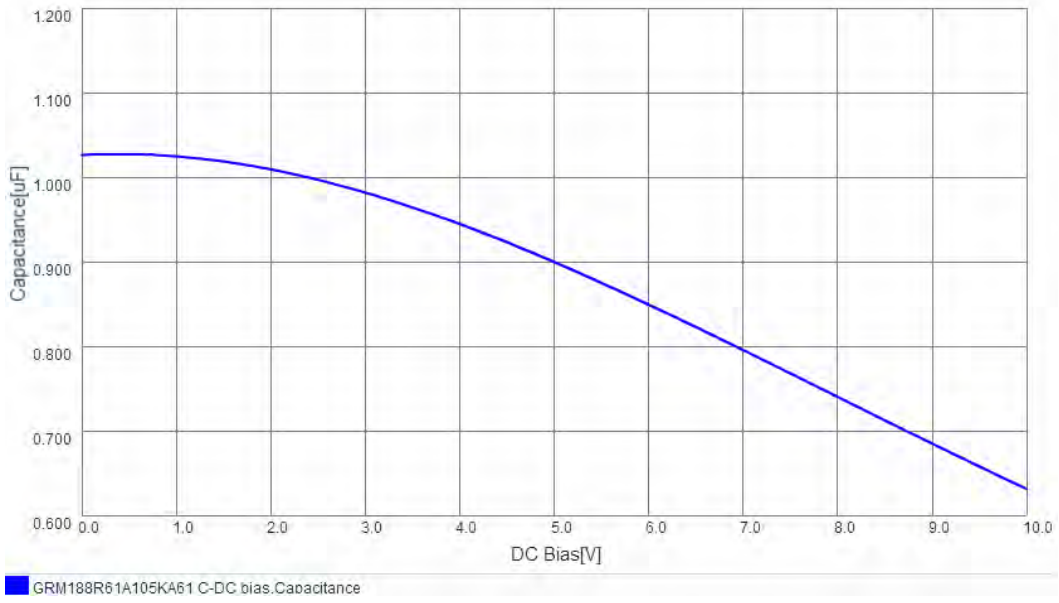


Fig 30. Capacitance vs DC characteristic – GRM188R61A105KA61

In order to keep a correct ratio on the DC/DC capacitors, and ensure a correct DC/DC behavior within the specification, the same recommendations apply to the 2 330nF capacitors: the nominal capacitance must not drop by more than 30% at 6V.

10.2.3 Clock wires

Clock (card) or oscillator signals can cause crosstalk to other signals. It is advised to isolate these signals: make the connections as short as possible and keep them far from other signals.

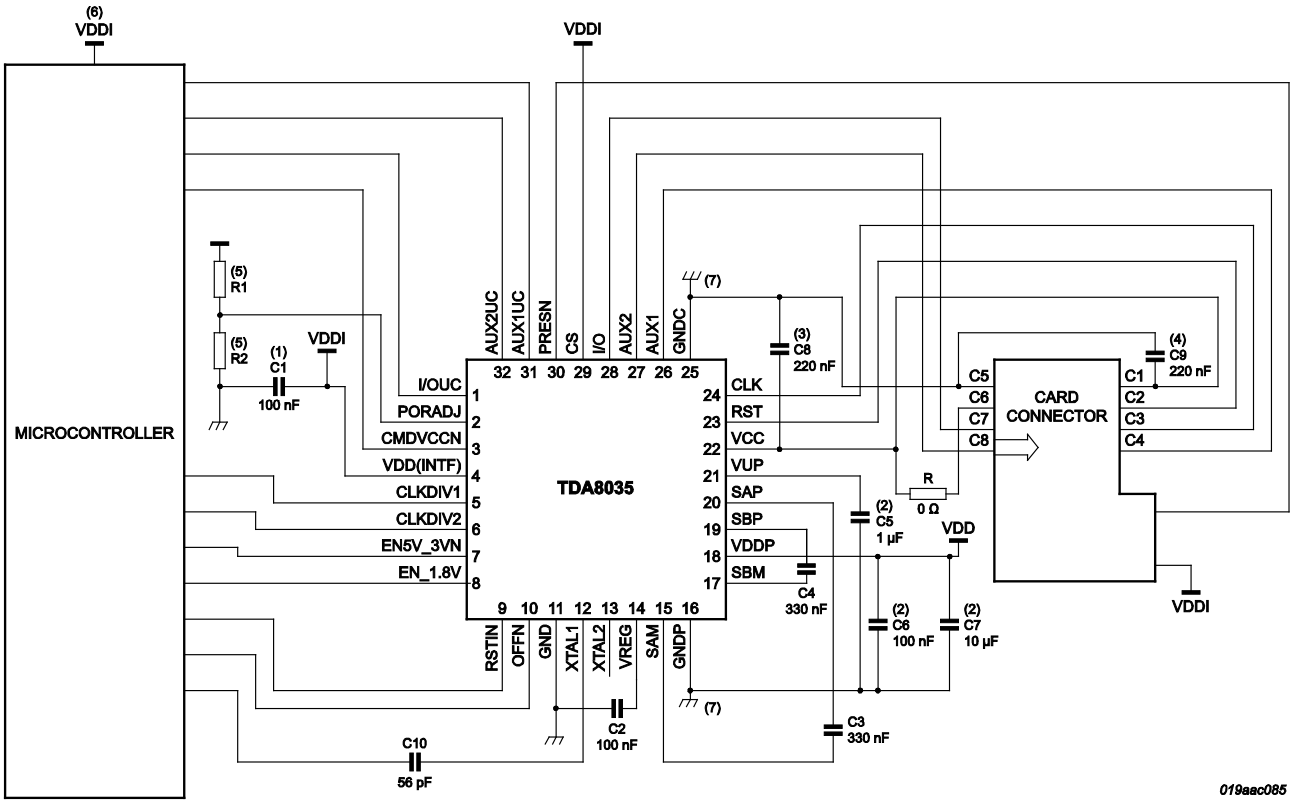
The best is to shield these signals with ground when possible.

10.2.4 Card ground connection

Pin GNDC of the TDA8035 is dedicated to the smart card connector. It is advised to connect the C5 (GND) pin of the smart card connector to this pin before connecting it to the main ground.

But it is mandatory to have this pin always connected to the main ground of the board, as well as the card connector ground pin.

10.3 Summary



(1) Place close to the protected pin with good (low resistive) and straight connection to the main ground

(2) Place close to the supply pin with good (low resistive) and straight connection to GNDP

(3) Low ESR 220nF capacitor. Must be placed close to the chip's VCC pin

(4) Low ESR 220nF capacitor. Must be placed close to the C1 contact of the card connector

(5) Optional resistor bridge. If this bridge is not required, connect PORAdj pin to $V_{DD(INTF)}$

(6) Microcontroller and TDA8035 must use the same $V_{DD(INTF)}$ supply

(7) GNDP and GNDC must be connected to the main ground with a straight and low resistive connection

Fig 31. Reference design with TDA8035HN

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