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Zynq-Based Master Controller for Formula Student Racecar

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1 Abstract

The Master Controller is a core part of electric racecar design, and many factors must be taken into consideration to optimize it. Weight, price and ease-of-use are important factors in Formula Student, but care must be taken to comply with all relevant rules and requirements when optimizing these.

In this report, a Master Controller is designed to replace the existing board used by SDU-Vikings, improving both overall size and weight. As the board must correctly interface with the many existing parts of the car, a thorough analysis is performed to include all required components. The results from this analysis is then used for a full design of hardware, resulting in a Master Controller PCB and ADC Expansion PCB. The Master Controller PCB can control the car's supply while communicating and storing data, as well as measure control sensors. The ADC Expansion PCB converts additional non-critical sensor signals and is used as proof of expansion feasibility. All primary functionalities are tested and prove that the design can be used with minor changes.

2 Foreword

This report is part of the product of the bachelor graduation project in Electronics Engineering by Jonas Fuglsang Hansen and Sebastian Rud Madsen from the Technical Faculty of the University of Southern Denmark. The project has been completed in cooperation with members of the SDU-Vikings Formula Student team, as the product must be seamlessly integrated in their existing system.

The report contains electronics and embedded programming concepts taught throughout the undergraduate courses, and the target audience is assumed to have knowledge at this level.

Thanks to Møn Print for sponsoring the PCBs, and Würth Elektronik and RS Components for sponsoring components. A special thanks to supervisor Karsten Holm Andersen for always bringing ideas and knowledge whenever needed.

3 Reading Guide

The project's main sections will be split up into three parts. The first main part will treat the analysis of the various subcircuits to be implemented in the Master Controller, the second main part will deal with the design of hardware of the various subcircuits, while the third main part will revolve around testing of the hardware.

The main parts will be enveloped by an introduction in the beginning, where the problem statement, limitations and initial analysis is described, and a discussion and conclusion in the end, where the results of the project is discussed and concluded upon. Each part will contain an introduction to the contents and focus of the part, as well as a partial conclusion that summarizes the choices and results of the part.

After the conclusion, the literature list and appendices are found. The appendices include PCB schematics, setup guides, journals and connection overviews among others.

Symbols are described the first time they appear in the text, and abbreviations are written in parenthesis after the phrase they abbreviate, after which the abbreviation is used interchangeably. The list of abbreviations is found on page 95.

Literature citations are on the form [lit. no., page no.] and the full literature list can be found on page 97.

MATLAB scripts, test software used, pictures of the Master Controller, oscilloscopes and screenshots from tests, Bill of Materials, KiCad files, PSPICE files and all literature can be found in the attached ZIP-file. If further changes are made, the newest KiCad files and software are also available on the SDU-Vikings GitLab repositories master-controller and master-controller-software respectively at:

<https://gitlab.com/sdu-vikings/future/master-controller>

<https://gitlab.com/sdu-vikings/future/master-controller-software>

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Part I

Introduction

In many racing cars, the Master Controller is the main controller in the vehicle. It measures the torque and brake pedal pressure as well as the steering angle, and controls the motors using these values. It must ensure that no mechanical or electrical malfunctions endangers the driver. Additionally, it is the focal point of most communication in the car. Currently at SDU-Vikings, the Master Controller is implemented on a heavy duty X90 programmable logic controller from B&R Automation, which is too heavy for use in a racing car. To reduce weight and improve the ease-of-use, the Zynq-based PicoZed module must be the Master Controller's core component instead.

4 Problem Statement

The goal of this project is to design and test hardware for a Zynq-7000-based Master Controller to be used in the SDU-Vikings racing car. The hardware must comply with Formula Student rules, and correctly interface with the finished parts of the car, both electrically and mechanically. As the Master Controller includes many external connections and needs to be designed with further development in mind, a thorough analysis is required. This analysis includes noting the future needs of SDU-Vikings to avoid the design quickly becoming obsolete. The conclusions from this analysis will then be used to design the individual parts of the hardware, which culminates in the design of a printed circuit board containing all required components. The hardware's capabilities must be tested and confirmed to function as expected, allowing application software to utilize all options when controlling the car.

5 Project Limitations

The Zynq-7000 contains two cores capable of working on individual workloads. While one core will perform the operations needed for safely controlling the racecar, the other will be running a webpage of live data, transmitting it over Wi-Fi. Both of these software applications are outside the scope of this project, which will only facilitate the development and use of these applications.

The Zynq-based Master Controller will be tested as an isolated node, but will not be tested in connection with other nodes within the car, nor within the real context it will be used.

6 PicoZed

The PicoZed, documented in its user guide [1], is a System-on-Module (SoM) designed by AVNET based on the Xilinx Zynq System-on-a-Chip (SoC). The Zynq-7000 devices are equipped with a single- or dual-core Cortex-A9 processor, both of which can connect to sections of Programmable Logic (PL) like that of an ordinary Field-Programmable Gate Array (FPGA). This makes the Zynq highly dynamic. The general design of the Zynq-7000 can be seen in Appendix A, which shows the variety of peripherals and interconnections. The PicoZed contains multiple high-efficiency voltage regulators for supplying the Zynq processor, as well as flash memory, Random-Access Memory (RAM), and multiple other interfaces. The connections between the Zynq and modules on the PicoZed board are listed in Appendix K. The pins that have not been connected to modules on the SoM are routed to the three receptacles on the bottom of the board, and can then be connected to the Master Controller board. The PicoZed's receptacles are referred to as JX, and each consist of 100 pins. The PicoZed variant to be used for this project is based on the XC7Z020-1CLG400 processor, commonly referred to as Zynq-7020.

An important part of the Zynq-7000's architecture is the input/output multiplexers. Most peripheral units in the Processing System (PS) are connected to both the Multiplexed Input/Output Interface (MIO) and Extended Multiplexed Input/Output Interface (EMIO). The MIO is further connected directly to PS I/O pins, while the EMIO is connected to the Programmable Logic. Signals in the PL section can then be connected to any of the PL pins. This allows almost full control of the PL pin connections, making hardware design easier. A block diagram of this interfacing from the Zynq reference manual [2, p. 47] can be seen in Figure 1.

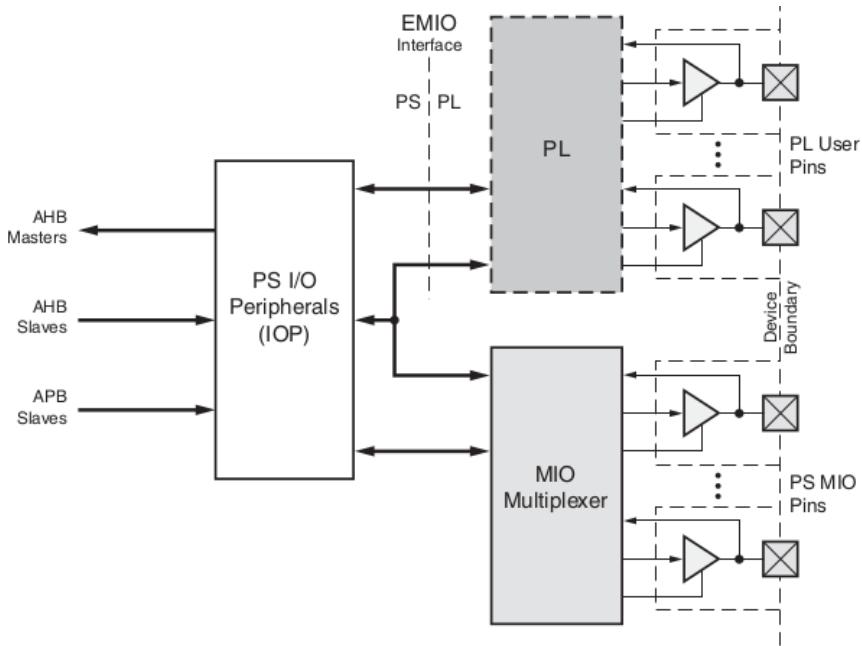


Figure 1: Block diagram of the interface between the Processing System and PL/PS pins

7 SDU-Vikings

SDU-Vikings is the Formula Student team affiliated with the University of Southern Denmark (SDU). It is a team composed of students of different fields of study, mostly mechanical and electrical/electronics engineering students. The team has been making cars since 2006, of which the first four cars were combustion vehicles. Since the fifth car, the team has been making electric vehicles exclusively. The team has already designed many of the Printed Circuit Boards (PCBs) needed in the car, which must follow the Formula Student rules for safety reasons.

7.1 Current Master Controller

The current Master Controller is based on the X90 Programmable Logic Controller (PLC) and option boards for this, made by B&R Automation. The X90-based Master Controller is 250 mm by 231 mm in size and mounted using screws. The PLC is connected to an interfacing PCB, slightly smaller in size, which has the purpose of breaking out the signals from the Molex CMC connectors and distribute them to the different devices in the vehicle. These can both be seen in Figure 2.

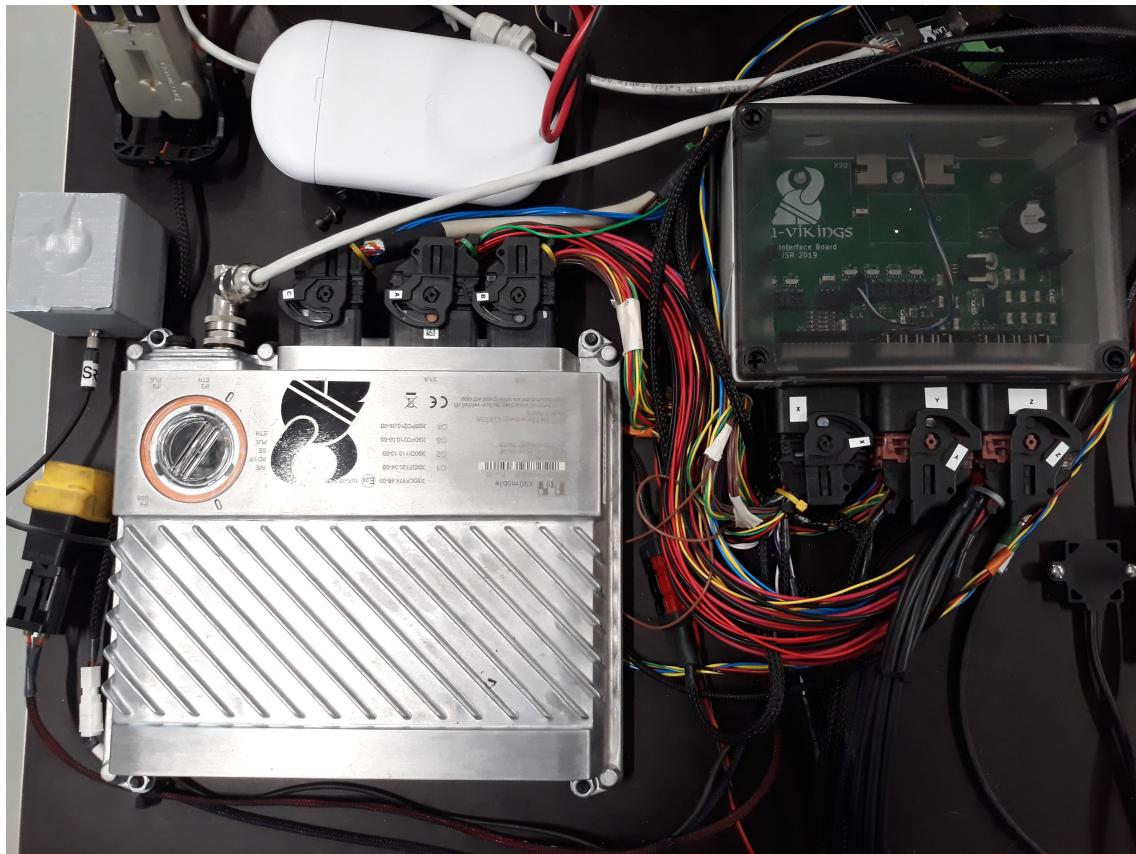


Figure 2: Picture of the current X90-based Master Controller, in metal enclosure, and the interface PCB, in see-through enclosure

The advantages of using the X90-based Master Controller is ease of programming, large amount of support, and built-in live-view. With option boards, the X90 has six Controller Area Network (CAN) buses used for communication with modules in the car. Information on the current setup is found in the SDU-Vikings X90 Master Controller Documentation [3].

The disadvantage of using the X90 Master Controller is the size, weight, power, and cost. The X90 requires a lot of space and its ruggedness adds weight. Power-wise, the X90 has most likely been optimized for low power usage, but hopefully there is something to gain. The price-point of the X90 and option board is unknown, but there is most likely money to save by producing a custom-made Master Controller.

Another advantage of making a Master Controller based on the Zynq-platform is that the Zynq is widely used in courses at SDU, and elsewhere in the vehicle. Therefore, the platform is known to the team, and software can easily be transferred between devices. Finally, designing a PCB in-house is also likely to grant more points at Formula Student competitions.

8 Initial Analysis

An initial overview of the Master Controller's responsibilities and connections is needed. The requirements must also be specified. By completing a simple initial analysis, a block diagram of the Master Controller module is created, which is shown in Figure 3. The coming subsections will further elaborate on the responsibilities of the Master Controller PCB.

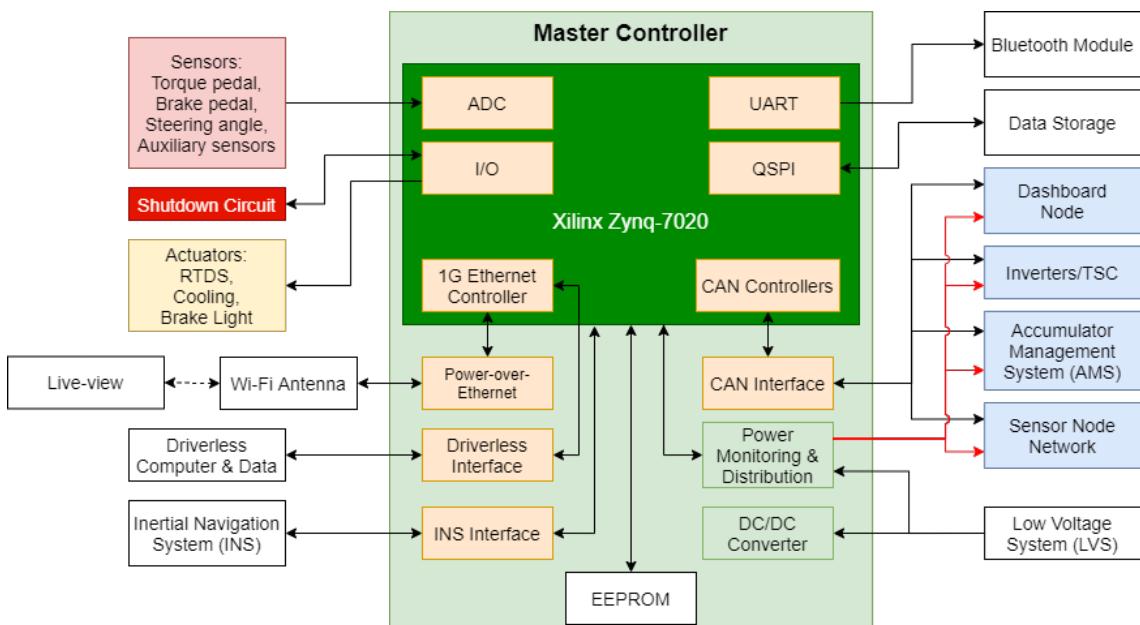


Figure 3: Resulting block diagram from the initial analysis of the Master Controller

DC/DC Converter

A converter must be implemented to supply the PicoZed with either 12 V or 5 V. The Programmable Logic I/O pins of bank 13, 34, and 35 on the Zynq must be supplied as well, as these are not supplied by the PicoZed SoM. Other Master Controller PCB components should be supplied from the same converters.

The Low Voltage System (LVS) is expected to have a voltage of 24 V. This is supplied by LiFePO batteries of type LiNANO® 26650 with a nominal voltage of 3.2 V, maximum voltage of 3.65 V, and minimum voltage of 2.5 V¹. With eight batteries in series, this results in an actual nominal voltage of 25.6 V, with 20 V and 29.2 V being minimum and maximum respectively. For flexibility, it should also be possible to supply the Master Controller with a 12 V LVS. The actual nominal voltage, using four batteries in series, is 12.8 V, while the minimum and maximum are 10 V and 14.6 V respectively. It must thus be possible to supply the Master Controller with voltages ranging from 10 V to 29.2 V.

Distribution of Low Voltage System

The Master Controller is responsible for distributing the LVS to the different nodes in the vehicle, such as Accumulator Management System (AMS) and Tractive System Container (TSC), as well as the actuators, those being the Ready-To-Drive Sound (RTDS), brake light and cooling pumps and fans. The distribution is controlled by the Zynq. The currents must also be measured to monitor the power usage of each node and actuator.

Measurements

The Master Controller must be able to measure the torque pedal travel, brake pressure and steering angle using sensors. The sensors to be measured have been picked by SDU-Vikings, and must be supplied by the Master Controller PCB. The Zynq-7000 has a built-in Mixed-Signal Analog-to-Digital Converter (XADC) to convert the voltages, but the voltages must be no higher than 1 V. The XADC is built into the PL fabric, making it more flexible than common ADCs.

The Shutdown Circuit (SC) signals must be monitored in case any of the 11 components comprising the Shutdown Circuit are open-circuited, indicating that the car is not ready to drive.

Inter-Node Communication

For communication with other nodes, CAN buses are used. As of now, six CAN buses are used for communication. As the Zynq only has two CAN Controllers, this may need to change. An analysis must be made to determine the load on the different CAN buses and determine if some buses can be combined, so the total number of buses can be reduced.

¹<https://shop.liopower.de/LiNANOZ-26650-3400-mAh-SL-FHD>

Data Storage

For diagnostic and debugging purposes, a removable high-capacity storage device is needed, which is commonly communicated with through Quad Serial Peripheral Interface (QSPI). It should also be possible to store configuration values or diagnostics on a permanent storage unit on the PCB, like Read-Only Memory (ROM).

Live-View

Data from the Zynq will be displayed on a webpage accessible through Wi-Fi. This requires use of the Ethernet Controller on the Zynq, which will connect to an antenna through an Ethernet interface on the PCB.

Future Interfaces

For future-proofing, interfaces must be implemented for the driverless computer and the Inertial Navigation System (INS).

9 Requirement Specification

The Master Controller hardware platform must be functional and compliant with SDU-Vikings' needs and Formula Student rules described in [4]. The hardware must be tested with basic software and confirmed to work for expected tasks in a laboratory environment. Further software development is not part of the project.

The hardware must be versatile, allowing external components to be changed without requiring an adjustment of the Master Controller PCB's design.

The SDU-Vikings team has previously experienced issues due to noise induced by the motors and inverters. The issues of Electromagnetic Interference (EMI) must be taken into consideration when handling Electromagnetic Compatibility (EMC) for all relevant parts of the Master Controller.

While there are no size constraints for the PCB, it should be as small as possible and be designed to fit into an IP65 or better enclosure. Connectors must be automotive grade and secure. The team currently uses Molex CMC and circular connectors.

Part II

Hardware Analysis

This part contains the complete analysis of required Master Controller subcircuits defined in the initial analysis. This includes potential solutions and the viability of these, as well as theory of operation for the picked solutions. The analysis ensures that all required parts of the Master Controller can be implemented with the available resources and hardware requirements.

10 EMC Considerations

As the Master Controller will be placed in a noisy environment due to the inverters switching large currents at 8 kHz, considerations must be made regarding the EMC of the design. External cables entering the Master Controller may pick up unwanted high-frequency signals and voltages, which can result in damaging spikes. These must be handled with Electrostatic Discharge (ESD) or Transient-Voltage Suppression (TVS) diodes that absorb the power upon entry to the PCB. Filtering the signals may also be needed. While it is undesirable to filter high-frequency data signals, these are often differential, reducing the effect of EMI. Lower-frequency signals, such as sensor signals that are changed as a result of a mechanical action, can be filtered without any problems.

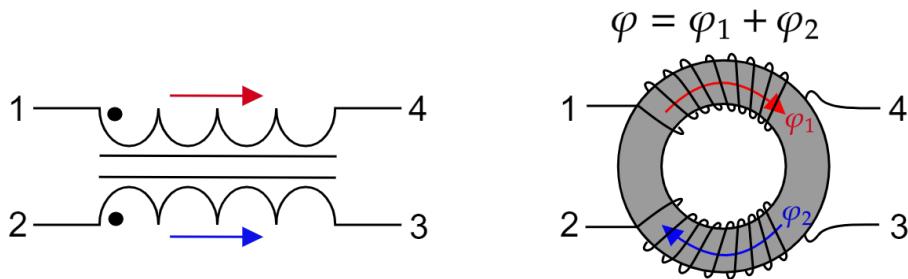
10.1 Bypassing and Ferrite Beads

Integrated Circuits (IC) and devices in the critical sections of the Master Controller should have ferrite beads in addition to bypass capacitors on the supply pins. Ferrite beads function as inductors by dissipating the power of high-frequency signals as heat. As the inductance of ferrite beads decreases heavily with higher DC currents, they should be used at around 20% of their rated maximum current, as described in the Analog Devices article of [5].

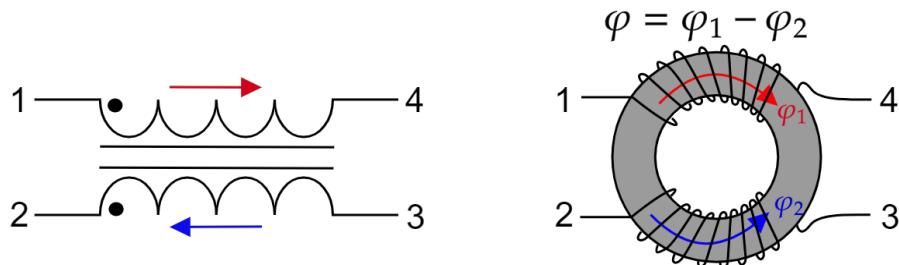
The ferrite bead blocks high-frequency current sourcing by the power supply, while the bypass capacitors sources high-frequency currents to the IC, reducing voltage drops and reducing noise in both directions.

10.2 Common-Mode Choke

A common-mode choke consists of two coils wound on the same magnetic core. It suppresses common-mode currents while passing differential currents. In designs using the common-mode choke, a differential signal pair is routed each through their own coil in the choke. When a common-mode signal, i.e. a signal where the currents in the signal group have the same direction, appears in both coils, the common-mode component of the currents will induce a flux in the magnetic core that adds up. The sum of the flux the



(a) The common-mode choke blocks common-mode signals, by means of induced magnetic field.



(b) The common-mode choke passes differential signals, as induced flux in two windings counteract each other.

Figure 4: Functionality of Common-Mode Choke with common-mode signals and differential signals (or normal signal and return path)

common-mode components create will create an opposing magnetic field that blocks the common-mode signal from passing through, as shown in Figure 4a.

In differential signals currents will typically travel in opposite directions through the coupled coils. The flux created by the current through the two windings will have opposite directions and will therefore cancel, resulting in the signal being passed through the choke. See Figure 4b for illustration of principle.

While common-mode chokes are beneficial in blocking EMI and generally improving EMC, there are also undesirable effects from using a common-mode choke described in [6]. The signal integrity on bus lines can be worsened, and damaging voltage transients can occur under bus failure, such as a short-circuit to a DC voltage. A short circuit of a bus line to a DC voltage causes an inductive flyback, which can cause high voltages to appear by the choke, possibly damaging components. Therefore, if the common-mode choke is not necessary, it should not be added despite the rarity of damaging flyback events.

11 Communication Protocols

The theory behind the required communication protocols defined in the initial analysis will be expanded in the coming subsections.

11.1 Quad Serial Peripheral Interface

The common Serial Peripheral Interface (SPI) consists of a clock, data in, data out, and active-low activation signal. These are called Serial Clock, Master In/Slave Out (MISO), Master Out/Slave In (MOSI), and Slave Select (SS) respectively. Data transfer is initiated by a master node, which pulls the SS low, starts the clock, and ensures the MOSI data center is aligned with a clock edge. The recipient is a slave node, for which the SS is unique. Clock and data lines can be shared among multiple slave nodes. Only when the slave node is clocked by the master will it send data back on the MISO line.

QSPI expands on the SPI functionality by adding two additional data lines, and making them all bidirectional. This way, four bits are sent at a time, increasing through-put. In order to receive data from the slave, the clock must continue for a set amount of time after data has been sent. A diagram of QSPI timings, as provided by Xilinx in Figure 5 of the Zynq Datasheet [7, p. 24], is shown in Figure 5.

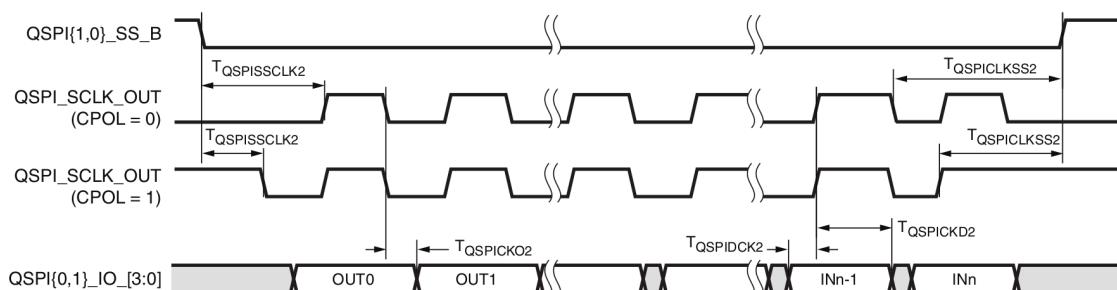


Figure 5: QSPI timings from the Zynq Datasheet showing SS, clock, and data lines

11.2 Controller Area Network

CAN is a communication interface often used in vehicles because of its robustness to EMI and induced transients on the signal lines. The communication bus consists of two lines, CANH and CANL, which together constitutes a differential pair. The common-mode signal therefore does not have any influence on the logic level being read. As a microcontroller is not capable of processing these differential signals, a CAN Transceiver is required, which the CAN Controller communicates with using serial Rx and Tx lines.

CAN conforms to the OSI network layer model, defining the two lowest layers as the Data-Link Layer and the Physical Layer. The Physical Layer includes the serial communication from the CAN Controller to the CAN Transceiver, the CAN Transceiver as well as the CAN bus, and is responsible for the transmission of raw bits. The Data-Link Layer consists of the microcontroller or -processor as well as the CAN Controller, and

is responsible for transmission of data frames between nodes connected by the physical layer.

CAN is a carrier-sense, multiple access protocol with collision detection and arbitration on message priority [8, p. 3]. This means that CAN is a multi-master communication interface, where each node must wait for a fixed period of inactivity after the last frame before attempting to transmit. If multiple nodes attempt to transmit frames simultaneously, the collision is resolved by arbitration by message priority, i.e. a bit-wise arbitration, where the message with the lowest binary identifier always wins.

An example of typical CAN bus signals can be seen in Figure 6. As illustrated in the figure, the bus is in a dominant state when the differential voltage is big and in a recessive state when the differential voltage is small. The dominant state is translated to a logic low level, while the recessive state is translated to a logic high level. The idle state of the CAN bus is recessive and a dominant bit will always overwrite a recessive. The individual nodes on the bus monitors the bits it transmits, and if these do not match the bit on the bus, the message has lost arbitration.

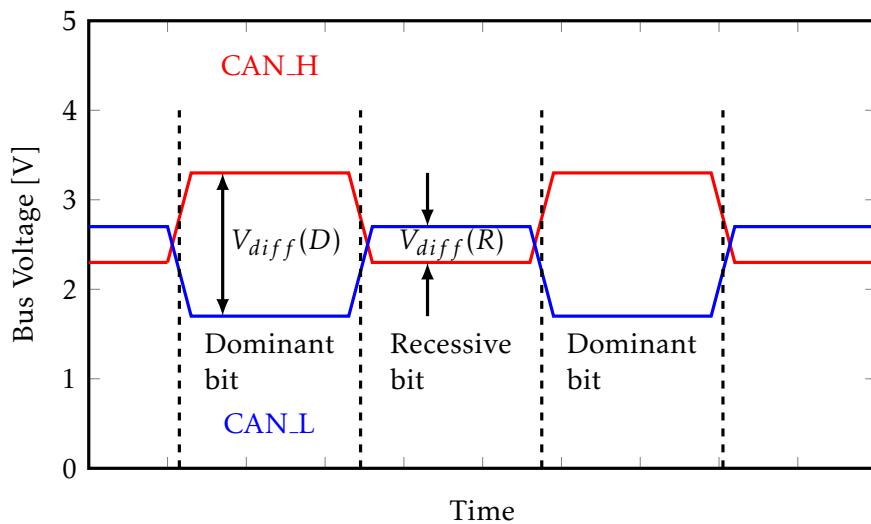


Figure 6: Typical CAN Bus signals. Dominant bit constitutes a low logic level, while a recessive bit constitutes a high logic level. The voltage levels on the bus lines are not representative, but chosen for illustrative purposes.

The CAN 2.0B standard format message frame consists of the fields shown in Table 1, and can contain up to 8 bytes of data.

As the CAN buses will be connecting every device in the vehicle, there is a high risk of EMI being induced on the bus, for which reason protective diodes must be used. These protection diodes must be placed on the signal path, so that the transients need not divert from the signal path. Furthermore, the bus signals can be filtered, so that high frequency noise can be attenuated. This will also have an undesired impact on the CAN signal waveform, and care should be taken when designing RC or LC filters for CAN networks, as a maximum capacitance load is specified in the CAN physical layer specification, ISO

Field	Length (bits)	Description
Start of Frame (SOF)	1	Must be dominant
Identifier	11	Unique Identifier for message
Remote Transmission Request (RTR)	1	Dominant in data frames, recessive in remote frames
Identifier Extension (IDE)	1	Dominant for Standard Format, recessive for Extended Format
Reserved r0	1	Must be dominant
Data Length Code (DLC)	4	Number of data bytes (0-8)
Data field	0-8 bytes	Length determined in DLC field
Cyclic Redundancy Check (CRC)	15	Data verification bits
CRC Delimiter	1	Must be recessive
Acknowledge (ACK)	1	Transmitter sends recessive, receiver asserts dominant
ACK Delimiter	1	Must be recessive
End of Frame (EOF)	7	Must be recessive

Table 1: CAN 2.0B Message format (standard format)

11898-2 and 11898-3. The recommended maximum capacitance between signal line and ground in a 1 Mbit/s CAN network is 35 pF [9, p. 9].

If the CAN bus signal lines are implemented as twisted wire pairs, the induced EMI in the CAN signals are expected to be purely common-mode interference, which the CAN transceiver should be resistant to. If the CAN transceivers Common-Mode Rejection Ratio (CMRR) is not satisfactory, it can be improved using discrete filters or common-mode chokes, the latter being described in Section 10.

11.3 Ethernet

Like CAN, Ethernet requires a Physical Layer Chip (PHY) to turn serial communication with the microcontroller into differential signals for long-distance data transfer. Ethernet communication is commonly 100 or 1000 Mbit/s, the latter also referred to as Gigabit Ethernet.

The serial communication when using 100 Mbit/s is named the Media-Independent Interface (MII), consisting of four Tx data lines, four Rx data lines, and a 25 MHz clock for each direction. This allows full-duplex communication between the microcontroller and PHY. The MII additionally contains signals indicating Transmit Enable, Transmit Error, Receive Data Valid, Receive Error, Carrier Sense, and Collision Detection [10, p. 18]. Receive Data Valid and Transmit Enable are asserted during data transfer to indicate that the line signal is not noise. Carrier Sense indicates whether data is currently being transmitted on the differential lines, while Collision Detection indicates whether multiple nodes have sent data at the same time on a half-duplex line, corrupting it.

When using 1000 Mbit/s rates, the serial communication is Gigabit MII (GMII), expanding the data lines to eight signals each, clocked at 125 MHz [11, p. 18].

To optimize the amount of signals required, Reduced MII (RMII) and Reduced GMII (RGMII) can be used. These use half the number of data pins at double the frequency and remove non-essential status signals. An overview of the entire RGMII Ethernet connection, from Zynq Ethernet Controller to LAN connector, is shown in Figure 7, as provided by the Xilinx Datasheet [7, p. 534].

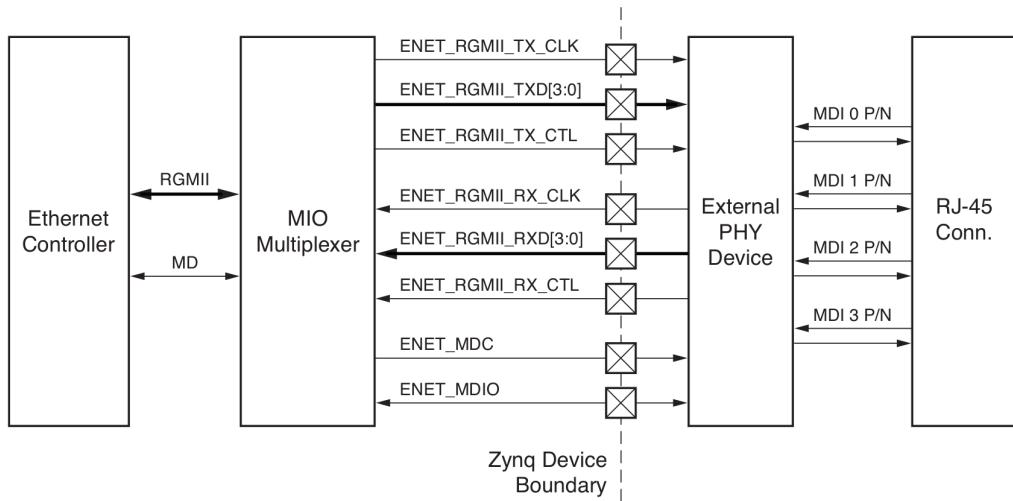


Figure 7: Gigabit Ethernet interface from Controller to LAN connector

The differential signal frequency for both Ethernet data rates is 125 MHz, but with different encoding. Additionally, 100 Mbit/s Ethernet uses one differential signal for transmitting and one for receiving, while 1000 Mbit/s contains four bidirectional differential signals [11, p. 6]. These signals must be terminated with resistors and capacitors near the PHY to avoid reflections, and must also be passed through magnetic components for EMC and signal integrity. The Common Taps (CTs) of the magnetic components must be decoupled with capacitors.

Bob Smith termination is often used for safety. This consists of four $75\ \Omega$ resistors, each connected to the same $1\ nF$, $2\ kV$ capacitor on one side and data signals on the other as described in Pulse Electronics' Guide to Ethernet Layout [12, p. 5]. The $1\ nF$ capacitor is connected to shield ground. A full overview of the 100 Mbit/s interface from PHY to connector is shown in Figure 8, taken from the Texas Instruments Ethernet Application Report [13, p. 3].

The Pulse Electronics Ethernet guide also contains best practices for routing the Ethernet signals. These must be routed with controlled impedances, length matching, robust ground connection, and reasonable distance to each other. The Media-Independent signals must have a single-ended impedance of $50\ \Omega$, while differential pairs must have differential impedance of $100\ \Omega$.

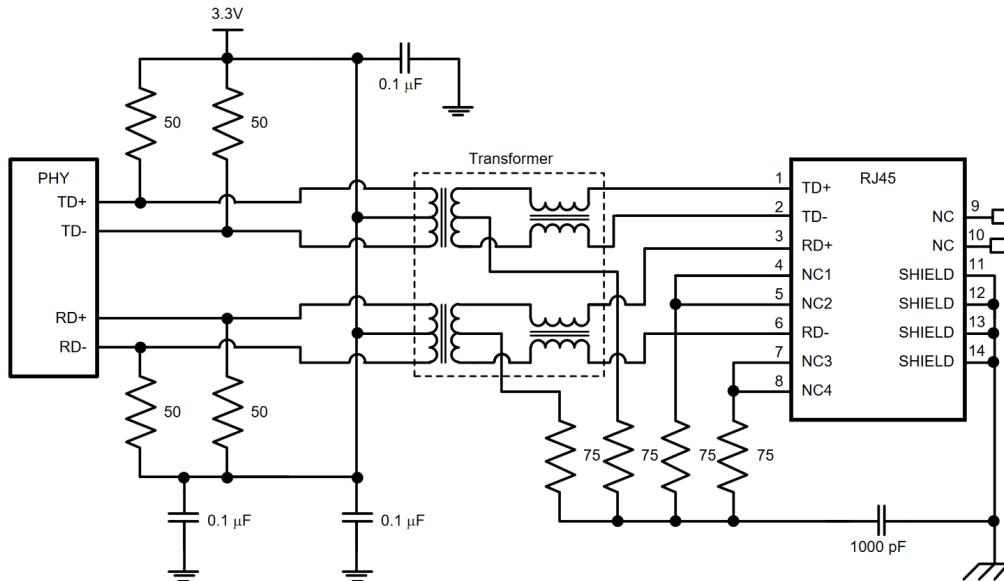


Figure 8: Typical 100 Mbit/s interface from PHY to connector

12 Power Distribution and Monitoring

As the Master Controller is critical for the car, it is also important that it is fully operational before the other nodes. This is achieved by having the other nodes disabled with switches, which are electrically controlled by the Zynq. For all switches, the minimum load voltage requirement is 30 VDC, plus a safety margin. The currents, however, differ depending on the node. Estimates of the maximum DC currents at 12 VDC have been made by the SDU-Vikings team. These values are shown in Table 2. These can be assumed to be worst-case, as currents with a 24 VDC supply would be lower.

Node	Current	Description
Low Voltage System	20 A	Expected for entire system
Accumulator	1 A	With relays and Battery Management System (BMS)
Dashboard	1 A	With all LEDs lit
Inverter 1 + 2	2.5 A	1 A per inverter plus inefficiencies
Inverter 3 + 4	2.5 A	1 A per inverter plus inefficiencies
Sensor Network	1 A	Four nodes, still in design phase
TS Container	0.2 A	Traction System control and lighting

Table 2: Estimates of the maximum DC currents for modules

For each of the nodes in the low voltage system, the Master Controller will need to monitor the currents. This is to estimate the battery's remaining capacity through Coulomb counting, and to ensure that all nodes draw correct currents. Shunt resistors can be used, where the voltages are routed into a differential amplifier. The circuit for measuring currents using a shunt resistor can be seen in Figure 9.

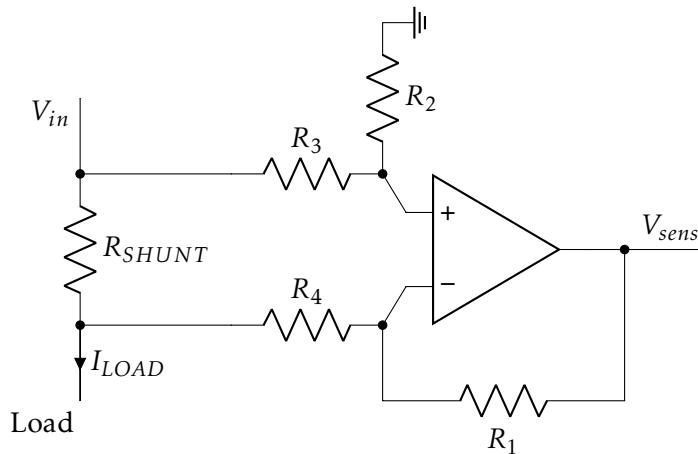


Figure 9: Schematic of current measuring using shunt and differential amplifier

For a simple differential amplifier, $R_3 = R_4$ and $R_1 = R_2$. The output voltage of the circuit can then be calculated with the equation [14, p. 685]

$$V_{sens} = \frac{R_1}{R_4} \cdot R_{SHUNT} \cdot I_{LOAD} \quad (12.1)$$

Consequently, if the peak current must result in a specific voltage output, either the shunt resistances or the amplifications must be individually adjusted due to the difference in currents for the nodes. This circuit is easy to design, cheap, and can be modified to work with most currents. The primary drawback is the voltage drop and consequential power loss in the resistor. Using an approach based on magnetic sensors is more expensive, but reduces power loss. Ultimately, the currents are not deemed large enough to warrant magnetic sensors.

Alternatively, a Smart Field-Effect Transistor (FET) can be implemented. This is a transistor incorporated in an IC, which continuously senses the current. Similar to a Solid-State Relay (SSR), SmartFETs can be activated with the Zynq's 3.3 V I/O. Using such a device would minimize the circuit size and include important safety features, such as overvoltage, overcurrent, and reverse polarity protection in the IC. The current sensed by the IC will be translated to a voltage that must be measured with the XADC. This also requires tuning depending on the maximum load current, but is equally simple. A simplified drawing with the Zynq and a SmartFET is shown in Figure 10. This leaves out electrical components and multiple connections surrounding the SmartFET.

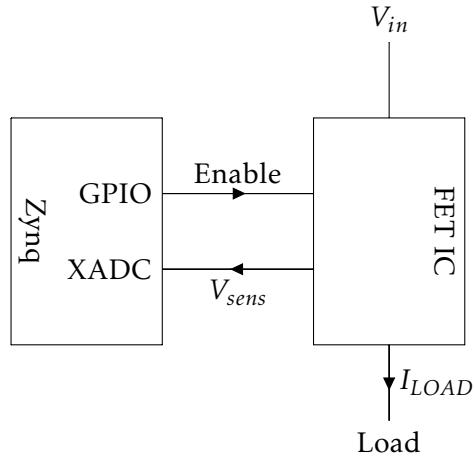


Figure 10: Simple diagram showing a SmartFET IC's integration in the system

While both price and circuit complexity are disadvantages for the SmartFET solution, the advantages outweigh this, and the SmartFETs are chosen as the primary solution for the distribution and measurement of the components supplied by the LVS.

13 Actuators

The actuators to be controlled and their requirements have been specified in Table 3. The currents are estimated from the 12 V circuits and SDU-Vikings test setups. Switches must be controlled by the Zynq to activate the actuators at the correct time. While it is not a Formula Student requirement that the currents can be measured, for safety and error spotting purposes they should. The same methods of distributing the LVS as described in Section 12 are viable. The SmartFET solution is picked for the cooling system, however SmartFETs are not accurate enough for brake light and RTDS measurements due to the low currents. Instead, Solid-State Relays with shunt resistors for current measuring are chosen.

Actuator	Voltage	Amperage	Active
Brake Light	24 V	60 mA	When hydraulic brakes are applied.
RTDS	24 V	8 mA	When the car is ready to drive.
Cooling System	24 V	7 A	Always on.

Table 3: Overview of the actuators to be controlled by the Master Controller

14 Shutdown Circuit Monitoring

Monitoring the Shutdown Circuit is an essential task for the Master Controller. Knowing which component in the SC has switched off can be used to debug the system, as well as ensure that the startup protocol is followed. Monitoring of the SC is essentially a binary measurement, as the component is either open-circuited or it is not. Therefore, the monitoring circuit can be routed to digital I/O pins of the Zynq.

The high-range digital I/O pins of the Zynq can handle voltages up to 3.3 V. The voltage levels of the SC are up to the maximum battery voltage, and must therefore be shifted down to voltage levels the Zynq can handle.

Due to the long wires used for the Shutdown Circuit, large voltages may be induced. While isolating is more expensive and bulkier than not isolating, it is needed for safety. To implement this isolation, an optocoupler can be used, which also acts as level shifter. Each monitored signal in the Shutdown Circuit is routed into the optocoupler through a current-limiting resistor. The transistor side is supplied with 3.3 V on the collector. An optocoupler circuit can be seen in Figure 11.

All the optocoupler output signals can then be routed into a multiplexer or directly into an I/O pin each. A multiplexer would only require five I/O pins as opposed to 11, but the added software complexity of driving it, as well as the price and size, means it is not worth it.

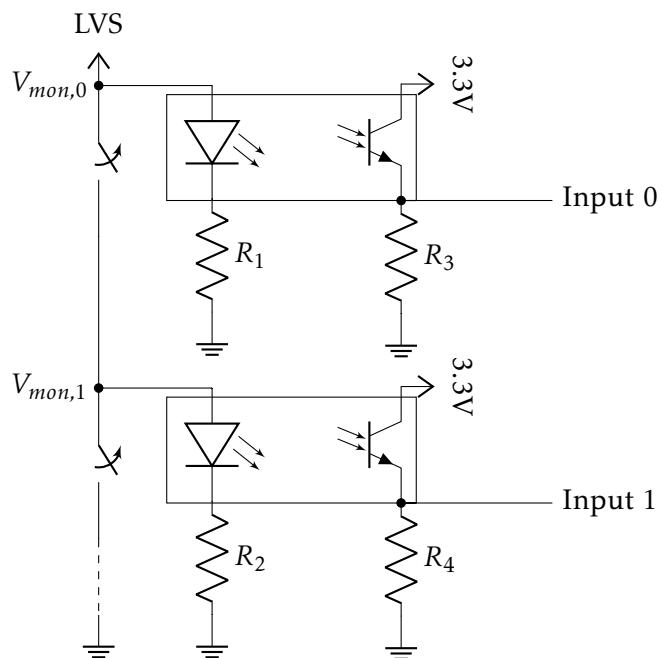


Figure 11: Implementation of optocoupler circuit for level shifting and isolation

15 Sensors

The Master Controller will be using many sensors to monitor the vehicle. These have varying inputs and outputs, which needs to be accounted for. Table 4 shows a summary of the expected sensors and their signals.

Source	Range	Description	Supply
Steering Wheel	0 - 12 V	VERT-X 31E6A736-111-402 [15]	12 V
Brake Pedal[0:1]	0 - 5 V	EPT3100-H-16000-B-5-A [16]	5 V
Torque Pedal[0:1]	0 - 5 V	ELPM50 [17]	5 V
LV Battery	0 - 30 V	Voltage measurement of LVS	-
Master Sense	0 - 5 V	Current measurement of Master	-
Dashboard/AMS Sense	0 - 1 V	Current of dashboard or AMS	-
TSC/Inv. 1 + 2 Sense	0 - 1 V	Current of TSC or inv. 1 + 2	-
S. Net/Inv. 3 + 4 Sense	0 - 1 V	Current of sensor net or inv. 3 + 4	-
Brake Sense	0 - 5 V	Current of brake light	-
RTDS Sense	0 - 5 V	Current of RTDS	-
Cooling Sense	0 - 1 V	Current of cooling system	-
PoE Sense	0 - 1 V	Current of Power-over-Ethernet	-
SC[0:10]	0 / 3.3 V	Shutdown Circuit measurements	-
Cooling Sensor[0:1]	0 - 5 V	Auxiliary. Bosch NTC M12 [18]	5 V
Auxiliary Sensors	Any	Future auxiliary sensors.	Any

Table 4: Overview of sensor signal inputs to the Zynq

This results in 14 fully analog signals, not including auxiliary signals, that must be converted in an ADC.

If any of the steering wheel, brake, or torque pedal signals are at ground or supply voltage levels, or within 10% of them for the torque pedal sensor, an error has occurred. This is required as per Formula Student rule T11.9 [4, p. 58]. Thus the circuits must be designed with this in mind by pulling the signals to ground or supply voltage when an open-circuit occurs. Additionally, the torque pedal sensors must have non-intersecting transfer functions; they must not at any point output identical voltages, as per rule T11.8 [4, p. 57].

As the sensors might be changed on the fly, the supplies for each of them should be dynamic, allowing a choice of either 5 V or 12 V. This can be implemented with 0 Ω resistors, switches, or jumper pins that are mechanically adjusted. Desoldering resistors takes special equipment and too much time. Mechanical switches and jumper pins are almost evenly matched in use, but jumpers can lead more current with lower resistance and the chosen setting is more obvious, for which reason they will be used.

While 5 V exists on the PCB, 12 V is not supplied to the board, and a dedicated DC-DC-converter must be placed for supplying the sensors.

15.1 Sensor Supply Design

Regardless of the sensors' supplies, the circuits must be designed with a specific output voltage in mind. The torque sensor is a $5\text{ k}\Omega$ potentiometer, from which the output voltage must never be below 10% or above 90% of the supply. To ensure this, resistors must be put in series with the potentiometer between supply and ground, as shown in Figure 12.

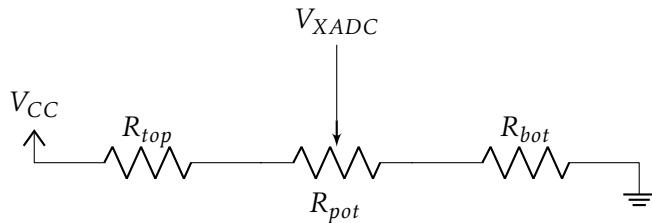


Figure 12: Supply configuration of torque sensors

Using voltage division, the output voltages at the potentiometer extremes can be calculated with the equations

$$V_{high} = V_{CC} \cdot \frac{5\text{ k}\Omega + R_{bot}}{5\text{ k}\Omega + R_{bot} + R_{top}} \quad (15.1)$$

$$V_{low} = V_{CC} \cdot \frac{R_{bot}}{5\text{ k}\Omega + R_{bot} + R_{top}} \quad (15.2)$$

This leaves two equations with two unknown variables, the resistors. The high and low voltage should have a margin of error from the extremes due to component tolerances and noise. With one sensor ranging from 15% of the supply to 75% of the supply, and the other from 25% to 85%, there is margin of error both for shutdown voltages and intersecting voltages.

The Negative Temperature Coefficient (NTC) thermistor used for measuring cooling system temperature requires a series resistor for voltage division, as shown in Figure 13. Appendix E shows that placing the NTC high-side results in higher accuracy across most of the temperature range.

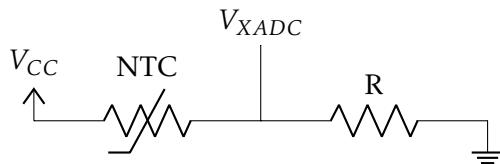


Figure 13: Supply configuration of cooling system sensors

The output voltage is then calculated from voltage division, depending on the NTC's resistance at a given temperature.

16 Analog-to-Digital Converters

The Zynq-7020's XADC module contains two 12-bit ADCs, each able to sample 1 million times per second. An internal multiplexer allows the XADC to sample up to 17 signals in total. The XADC module is designed to measure both the sensor signal and sensor ground simultaneously for a true differential measurement, reducing the impact of common mode noise on the conversion [2, p. 753]. The XADC has on-chip sensors that can be used to measure supply voltage and chip temperature, and automatically trigger an alarm if these deviate from expected values.

In the X90-based Master Controller, the SC is monitored every 50 ms, while the remaining signals are monitored every 10 ms. These timings should be replicated in the Zynq. With 14 signals sampled at 100 Hz, the XADC must convert 1400 samples per second. This is not at all an issue, meaning it is possible to use hardware averaging of the signals within the allocated time. If multiple auxiliary signals are to be measured, there will likely be a shortage of XADC input pins, for which reason an alternative must be found for the auxiliary sensors.

The XADC module has the option to drive an external multiplexer IC with up to five PL I/O pins. This means that only one pair of XADC pins is needed for up to 32 auxiliary input signals. Alternatively an external ADC IC can be placed on the Master Controller PCB. This would require communication with the Zynq, but would increase the voltage range that can be converted without voltage division. An ADC IC is slightly more expensive and less flexible, but uses less board space. The primary benefit is offloading the conversions to another ADC, which would be useful in case of future oversampling. If the inputs are well-filtered, they are likely to surpass the XADC in precision, especially without the cross-talk of a multiplexer. For the reasons listed above, an ADC IC is believed to be the best option for conversion of auxiliary sensor voltages.

While the XADC is supplied with 1.8 V, the inputs are limited to 1 V, as saturation of the module would otherwise occur. This means that some input voltages must be lowered before the conversion by using voltage dividers. The Driving the Xilinx ADC Guide [19, p. 4] has recommendations for implementation of both voltage dividers and anti-aliasing filters, one of which is shown in Figure 14. In the figure, V_{sens} is the sensor's output voltage, while $V_{XADC,X}$ are the voltages applied to the differential XADC pins.

When designing this circuit, a few calculations need to be made. For the voltage divider, the peak output voltage of 1 V is calculated with the equation

$$V_{XADC,P} = V_{sens,max} \cdot \frac{R_2}{R_1 + R_2} = 1 \text{ V} \quad (16.1)$$

Knowing the maximum sensor voltage $V_{sens,max}$ still leaves two unknown variables, meaning one must be chosen and the other calculated. A lower resistor value increases both accuracy and power consumption.

Designing the anti-aliasing filter for the XADC is a difficult task due to its dependency on sampling rate and accuracy. Commonly, the filter is expected to attenuate

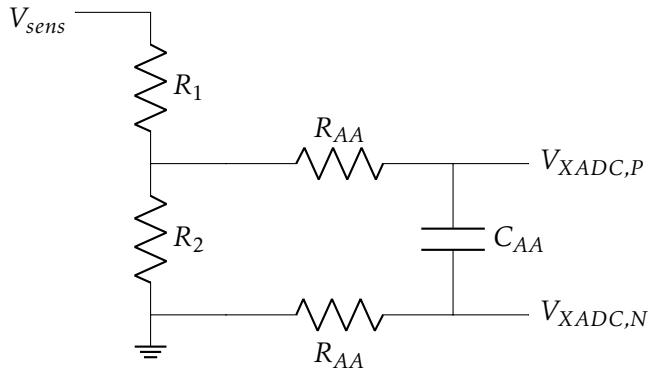


Figure 14: Schematic of XADC voltage divider and anti-aliasing filter

signals from half the sampling frequency, called the Nyquist frequency, with at least $\text{SNR} = 6.02 \text{ dB} \cdot N + 1.76 \text{ dB}$ [20], in which SNR is the Signal-to-Noise Ratio, N is the amount of bits. For a 12-bit converter, this results in 74 dB.

The Driving the Xilinx ADC Guide notes that attenuating signals at the Nyquist frequency is rarely possible in practice due to the impact on filter settling time and filter order. Instead, Xilinx recommends using filters to remove high-frequency components that might otherwise alias into the bandwidth of interest. The guide designs a simple RC filter with a 3 dB cutoff frequency at 160 kHz for filtering a signal sampled at 100 kS/s, ignoring the Nyquist frequency requirements in favor of fast settling time. The PicoZed Carrier Design Guide recommends using an RC filter with a cutoff frequency of 800 kHz for removing signal aliases [21, p. 21], which also ignores the Nyquist frequency.

As the sensor signals are sampled at 100 Hz, the analog filter requirements would be very harsh if the Nyquist frequency requirements were to be upheld. This requires many components to implement, and is less needed due to the inherently increased SNR of the true differential XADC. Instead, filters should be designed with adequate settling times in mind, while also attenuating the inverters' 8 kHz switching noise as best possible. The guide assumes a full step from 0 V to 1 V when designing filters with settling time requirements. This is unlikely to be experienced for the Master Controller's sensor signals, but should be designed for to maintain accuracy in edge cases.

For a first-order passive filter, and with an ADC accuracy of 12 bit, the filter capacitor can be calculated with the equation

$$C_{AA} = \frac{t_{sample}}{9.01 \cdot R_1 \| R_2} \quad (16.2)$$

where t_{sample} is the sampling time, and $R_1 \| R_2$ is the parallel combination of the voltage divider resistors. The sampling rate is up to 1 Msps, at which the sampling time is $t_{sample} = \frac{1}{1\text{MHz}} = 1 \mu\text{s}$. The resistor must then be calculated to result in a 12-bit settling time faster than the sampling time, having the filter impact the conversion with less than

± 0.5 LSB. The maximum resistor value can be calculated from the equation

$$R_{AA} = \left(\frac{t_{settle}}{2 \cdot 9.01 \cdot C_{AA}} \right) - R_1 \| R_2 \quad (16.3)$$

where t_{settle} is a smaller time period than t_{sample} . If the required accuracy is not 12 bits, the time constant of 9.01 changes as described in [19, p. 3]. With this resistor, the filter's cutoff frequency can be calculated. The voltage divider may have too large resistors for the anti-aliasing resistor to be practically implemented. If the divider cannot be changed, the anti-aliasing capacitance must be decreased and resistor re-calculated. If a voltage divider is implemented, a resistance equal to the parallel combination of the divider should be placed between the XADC's negative pin and ground to ensure equal impedances, maximizing interference immunity [19, p. 8]. This increases the filter resistance significantly, and the capacitor value must thus be decreased.

Damaging induced voltages are most likely to happen for sensors with external connections, for which reason these inputs should have a transient-absorbing diode placed by the connector. Due to diode forward-voltages, the XADC may still be subjected to a negative voltage, which can damage it. Implementing an active filter instead of passive filter ensures that no negative voltages will be applied to the XADC.

Many active filter topologies exist and could be used. Complex biquads like Tow-Thomas are unneeded due to the relatively low filter requirements in order to reduce settling time. Of the simpler biquads are Sallen-Key and Multiple Feedback filters. Multiple Feedback filters have higher potential amplitude roll-off and a more consistent attenuation than Sallen-Key, but require one more component and invert the signal. Inverting the signal complicates the design, for which reason a Sallen-Key filter is chosen. A general second order Sallen-Key low-pass filter can be seen in Figure 15.

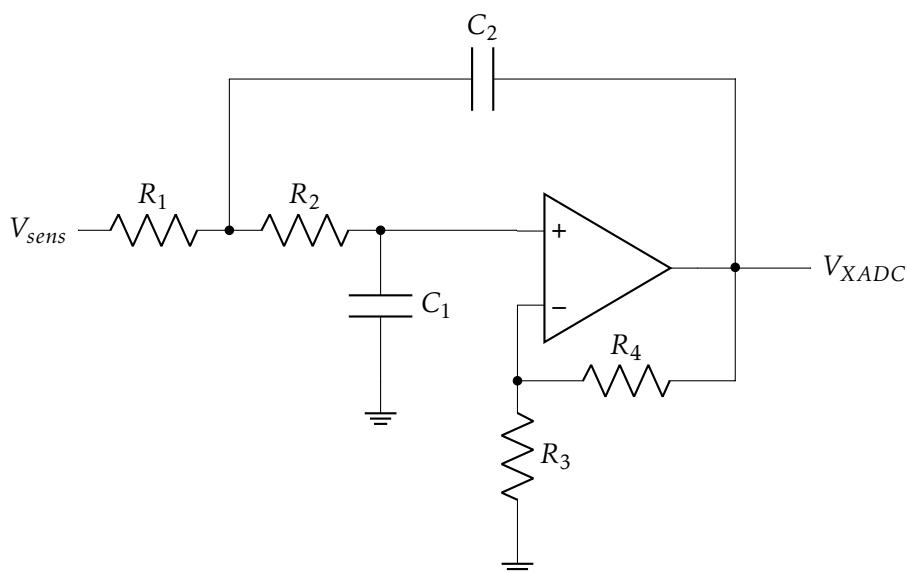


Figure 15: Schematic of second order Sallen-Key low-pass filter

As no DC amplification is needed in the filter, resistors R_3 and R_4 can be removed, leaving a voltage follower at DC. The filter is designed by first deciding filter type, cutoff frequency, stopband frequency, and attenuations at these frequencies. The transfer function is then determined and realized. A fast RC filter is needed after the active filter due to the real Sallen-Key filter's imperfections at high frequencies as explained in the article of [22, p. 6]. The filter can be designed with different attenuation characteristics. The Butterworth type is chosen over Chebyshev or Cauer due to the lack of ripples in both passband and stopband, and as the increased attenuation roll-off is not needed.

The settling time of a Sallen-Key filter reacting to a step response is calculated with the equation for a second-order system [23],

$$t_s = -\frac{\ln(E \cdot \sqrt{1 - \zeta^2})}{\zeta \cdot \omega_c} \quad (16.4)$$

In which E is the tolerance fraction, ω_c is the cutoff frequency in rad/s and ζ is the damping ratio $\frac{1}{2Q}$. Q is the quality factor of the filter, which depends on the filter type. For a Butterworth filter, this value is $Q = \frac{1}{\sqrt{2}}$. The tolerance fraction is determined by the accuracy of the ADC, and is given by Table 1 of [19, p. 3]. In a 12-bit conversion, for one half LSB error, the value is 0.000061. The resulting settling time must then be lower than the sampling time by a large margin due to tolerances, parasitic capacitances and the subsequent RC filter.

As described in Section 15, it is desired that the supply voltage for the sensors can be changed in case a different sensor is used. When using a sensor with a different supply, a different voltage division is most likely required due to a change in output voltage. Options will be made for 5 V outputs and for 12 V outputs.

16.1 Sensor Accuracy

The mechanical sensors for the steering wheel and torque pedal have an output voltage depending on the sensor position. Due to mechanical constraints in the car, the sensors are unlikely to use their entire dynamic area. If the voltage difference between lowest and highest sensor outputs is too low, the electrical inaccuracies can make the difference between for example 40% torque and 50% torque. For this reason, a minimum sensor travel range should be set to ensure that this disparity is minimized. Table 5 shows the sensors' expected voltage outputs and maximum travel ranges.

Accounting for the non-linear outputs of the sensors, the worst-case sensor resolution

Sensor	Voltage Range	Range
Steering wheel	0.1 - 10 V	360°
Torque pedal 1	0.75 - 3.75 V	50 mm
Torque pedal 2	1.25 - 4.25 V	50 mm

Table 5: Overview of expected voltages and ranges for relevant sensors

can be calculated with the equation

$$\text{res}_h = \frac{\Delta V_{output}}{\text{range}_{phys}} \cdot K_{linearity} \quad (16.5)$$

In which ΔV_{output} is the voltage range, range_{phys} the physical range, and $K_{linearity}$ the sensor's linearity factor. Since the sensor outputs must be routed through a voltage divider in order for the XADC to potentially measure the full range from ground to supply, the resolutions are similarly reduced. This also introduces a resistor tolerance inaccuracy. The resulting worst-case resolution can be calculated with the equation

$$\text{res}_l = \text{res}_h \cdot \frac{R_{2,min}}{R_{1,max} + R_{2,min}} \quad (16.6)$$

where $R_{2,min}$ is the minimum value due to tolerances of R_2 in Figure 14, and $R_{1,max}$ is the maximum value of R_1 in the same figure.

With the PicoZed using the internal voltage reference, it has been factory calibrated, removing offset and gain errors. The resulting XADC accuracy is typically ± 6 LSBs at a temperature up to 100°C and with enhanced linearity enabled. Due to filter settling time, parasitic capacitances, and the sampling capacitance, another LSB is added to the inaccuracy. With a maximum voltage of 1 V, 7 LSB is an inaccuracy of

$$V_{LSB} = \pm 7 \text{ LSB} \cdot \frac{1 \text{ V}}{4096} = \pm 1.71 \text{ mV} \quad (16.7)$$

If an active filter is used, the operational amplifier's imperfections also impact the accuracy due to offset voltage and bias current. The total inaccuracy of the op amp is calculated as specified in [24, p. 5], with the equation

$$V_{OA} = V_{OS} + I_{bias} \cdot (R_1 + R_2) \quad (16.8)$$

where V_{OS} is the offset voltage, I_{bias} is the bias current, and R_1 and R_2 are the Sallen-Key resistors as shown in Figure 15.

These inaccuracies must not impact the results more than a set percentage over the entire used range to retain the accuracy of the critical sensor signals. The minimum difference between smallest and largest measured voltage must then be

$$\Delta V_{sens,min} = \frac{(V_{LSB} + V_{OA}) \cdot 100}{\text{accuracy in \%}} \quad (16.9)$$

The minimum travel range of the sensors is then calculated with the equation

$$\text{range}_{min} = \frac{\Delta V_{sens,min}}{\text{res}_l} \quad (16.10)$$

Increasing the mechanical ranges will also increase the accuracy of the measurements, but may not be possible due to mechanical constraints in the car.

Using Equation 16.5, Equation 16.6, Equation 16.9, and Equation 16.10, a general formula can be derived for minimum travel length,

$$\text{range}_{min} = \frac{(V_{LSB} + V_{OA}) \cdot 100}{\text{accuracy in \%} \cdot \frac{\Delta V_{output}}{\text{range}_{phys}} \cdot K_{linearity} \cdot \frac{R_{2,min}}{R_{1,max} + R_{2,min}}} \quad (16.11)$$

17 CAN Modules

As previously described in Subsection 11.2, the CAN frame consists of a data frame of 0-8 bytes and an overhead of 44 bits, as seen in Table 1. The CAN buses used will have a bitrate of 1 Mbit/s.

The current Master Controller uses six CAN buses to communicate with the different devices around the car. The current usage of CAN buses is shown in Table 6, and as seen a star topology is used, where the Master Controller communicates with each device on their own bus, except for the inverters as well as AMS and Shunt. This gives reason to believe that the number of CAN buses used can be reduced significantly.

CAN Bus	Usage
1	Inverters 1 & 2
2	Inverters 3 & 4
3	AMS & Shunt
4	Dashboard
5	Sensor Network
6	FS Datalogger

Table 6: Current CAN bus usage

In theory CAN is able to handle a 100% bus load. The limit is usually set by the connected nodes' ability to process the messages and the urgency of the messages being transferred. The theoretical bus load on each bus can be calculated using the formula [25]:

$$\text{bus_load} = \frac{1}{\text{bit_rate}} \cdot \sum_{i=1}^N \frac{n_i}{T_i} \quad (17.1)$$

where bit_rate is the bit rate of the CAN bus in s^{-1} , N is the number of messages being transmitted on the bus, n_i is the length of message i in bits and T_i is the cycle time of message i in seconds. Using the CAN messages defined in Appendix B and Equation 17.1, the bus loads of the individual buses is seen in Table 7. As seen, the theoretical CAN bus loads of the individual buses are minimal, and they can easily be put on the same bus, keeping the total bus load at 21.7%.

CAN Bus	Nodes	Load [%]
1	Inverters 1 & 2	9.36
2	Inverters 3 & 4	9.36
3	AMS & Shunt	1.36
4	Dashboard	0.472
5	Sensor Network	0.844
6	FS Datalogger	0.284

Table 7: CAN bus loads on current CAN bus setup

A timing analysis is desired to get the average waiting times for the individual messages on the CAN bus. As no real-world data is available with all devices connected to the same CAN bus, a simulation of the CAN bus is the best alternative.

17.1 CAN Bus Simulator

As part of the analysis of the required CAN buses, a CAN bus simulator is written in Python. The simulator takes files containing the protocols of the individual devices communicating with the master as input, more precisely message IDs, cycle times and message lengths in bits. Using these values, the individual devices can be initialised with their own protocol as *CanDevice* objects. The *CanDevice* objects keep track of message IDs, cycle times, message lengths, remaining time until the next transmission of the message, how many cycles the message exceeds the deadline with, as well as how many times the message is transmitted. The *CanDevice* objects are passed as members to an object of the *CanBus* class. The *CanBus* object keeps track of the devices connected to it.

The *CanSim* class holds all *CanBus* objects that are required in the simulation. The object of the *CanSim* class is also passed an end time for the simulation. The *CanSim* class keeps track of the run time of the simulation, the loading of the individual buses, the idle time of the buses and lastly, the active time of the buses.

From all these parameters, the load of the buses can be computed, and it can be determined by how many cycles the individual messages are delayed in relation to the deadlines, as well as the total delay on the bus. Lastly, the average delay in % of the individual messages' cycle time can be computed so that unacceptable breaches of the deadlines can more easily be identified.

The simulator works by simulating each bus sequentially, and runs until the simulated runtime has exceeded the specified end time. The first thing done in each loop is that the runtime advances to the time of next message deadline. Here each device nominates a message, if any of its' messages are ready to be transmitted. The nomination follows the functionality of the CAN bus, namely the message with lowest ID is prioritized. The CAN bus finds the message with the lowest ID among the nominees and transmits it.

The simulator allows both worst-case analysis, where the messages' deadlines overlap, as well as an analysis where deadlines arrive randomly, in which the messages' deadlines are uniformly distributed within their cycle interval.

The CAN simulator, including input files, can be found in the attached ZIP-file.

17.2 Simulation Results

Running the simulation with all devices on one bus gives an acceptable bus load of 21.5%. Looking deeper into the results, it is seen that the average waiting time for all messages on the bus is 1452.8 CAN bit cycles. For most messages this results in a waiting time of 1-3% of the messages' cycle times, which is acceptable. In the case of the inverters, the

worst-case waiting time is 16.5% of the message's cycle time, which is unacceptable as these messages are regarded as the most important messages. It is therefore obvious that looking only at bus load is not an accurate measure of the bus' performance.

Splitting the devices up in two buses with each inverter pair on separate buses can reduce the waiting time for the inverter messages significantly. The CAN buses are configured as shown in Table 8 along with the bus loads of the two buses, calculated as $\frac{\text{active_time}}{\text{total_time}}$, as well as average waiting time on the bus.

CAN Bus	Nodes	Bus load [%]	Avg. waiting time [μs]
1	Inverters 1 & 2, AMS & Shunt	10.64	677.9
2	Inverters 3 & 4, Dashboard, Sensor Network & FS Datalogger	10.88	696.9

Table 8: Chosen distribution of devices on CAN buses

Table 9 and Table 10 show the more detailed timing information from the worst-case simulation. As seen in the tables, the average waiting times for the inverter messages have been reduced by over 50%. As can be deduced from the tables, it is the inverter messages that delay each other. Therefore, there is not much improvement to gain by giving each inverter pair their own CAN bus, as the inverter messages already have the highest priority.

As the message deadlines most likely won't arrive nor be sent simultaneously, but probably will be more uniformly distributed in the cycle intervals, it would be interesting to see the timing results that can be expected from this CAN bus configuration. Running a simulation with uniformly distributed message deadlines gives a much lower average waiting time on the buses, namely 5.11 bus cycles for bus 1 and 9.33 bus cycles for bus 2. The average waiting times for the inverter messages have also dropped significantly to <0.2% of the cycle time.

From the simulation results it is seen that the best CAN configuration is separating the two inverter pairs on separate CAN buses, and distributing the remaining devices on the two CAN buses, so that the CAN buses have similar bus loads.

As the Zynq-7000 has two CAN controllers, both CAN controllers are used. The CAN buses have light loads, and as seen from the results, the lower priority messages are transmitted without great overruns of their deadlines. Therefore, the two CAN bus configuration should be future-proof, if more devices are added in the future.

Node	ID	Cycle time [ms]	Avg. wait [ms]	Avg. wait [%]
AMS	0x300	100	0.500	0.500
	0x301	100	0.552	0.552
	0x305	50	0.566	1.133
	0x311	50	0.660	1.319
	0x312	100	0.864	0.864
	0x313	100	0.956	0.956
	0x310	100	0.688	0.688
Inv. 1 & 2	0x283	5	0.036	0.713
	0x285	5	0.252	5.035
	0x184	30	0.000	0.000
	0x284	5	0.144	2.875
	0x286	5	0.360	7.195
	0x185	30	0.108	0.360
Shunt	0x521	100	1.048	1.048
	0x522	50	0.902	1.804
	0x523	50	0.994	1.988
	0x526	100	1.324	1.324
	0x527	200	1.420	0.710
	0x528	200	1.512	0.756

Table 9: Results of worst-case simulation of CAN bus 1 (all message deadlines fall simultaneously). Third column shows cycle time of messages, while fourth and fifth column show the average time the message waits to transmit in ms and in percentage with respect to the cycle times, respectively.

Node	ID	Cycle time [ms]	Avg. wait [ms]	Avg. wait [%]
Dashboard	0x580	100	0.784	0.784
	0x581	100	0.892	0.892
	0x582	100	1.000	1.000
	0x583	100	1.060	1.060
	0x5d0	100	1.152	1.152
	0x5d1	100	1.204	1.204
Inv. 3 & 4	0x287	5	0.036	0.713
	0x289	5	0.252	5.035
	0x188	30	0.000	0.000
	0x288	5	0.144	2.875
	0x28a	5	0.360	7.195
	0x189	30	0.108	0.360
Sensor Network	0x600	20	0.649	3.246
	0x605	50	0.909	1.819
	0x60a	50	0.985	1.971
	0x610	50	1.061	2.123
	0x615	1000	1.492	0.149
FSDL	0x500	100	0.500	0.500
	0x501	100	0.608	0.608
	0x502	100	0.700	0.700

Table 10: Results of worst-case simulation of CAN bus 2 (all message deadlines fall simultaneously). Third column shows cycle time of messages, while fourth and fifth column show the average time the message waits to transmit in ms and in percentage with respect to the cycle times, respectively.

18 Internal Power Supplies

Two DC-DC converters are required for stepping down the LVS voltage and supplying the entire Master Controller PCB with 5 V and 3.3 V. As stated in the pre-analysis, the expected input voltage ranges from 10 V to 29.2 V. The DC-converters must accommodate a slightly larger range to account for variations in the voltage.

Using the Xilinx Power Estimator², a worst-case power consumption of 2.2 W for the Processing System is calculated. A 100% use of the Programmable Logic on the Zynq-7020 uses another 5 W. This does not include the other components on the PicoZed, accounting for around 2.5 W [1, p. 34], or the remaining components to be supplied on the Master Controller PCB. For this reason, and due to previous SDU-Vikings experience with the PicoZed, a 25 W converter should be used to supply $5\text{ V} \pm 5\%$.

The second DC-DC converter will supply $3.3\text{ V} \pm 5\%$ for the three high-range PL banks on the Zynq, which are not supplied by the PicoZed. According to the Zynq-7000 Datasheet [7, p. 9], the banks require 95 mA each for correct power-on. This equates to around 1 W on power-on, but could be more when fully utilized. The 3.3 V supply will also be used for multiple other components on the PCB. A minimum of 10 W power delivery is estimated for the 3.3 V based on this. The converter must not be enabled before the Zynq I/Os are operational and the PicoZed outputs the Power Good signal on header JX2 pin 10. The converter's Power Good output should be tied to the net on header JX2 pin 11. If the converter does not have a Power Good output, an undervoltage detector can be used for the same purpose [1, p. 31].

As described in Section 15, a 12 V supply must be available. As this supply will only be used for supplying sensors, the power requirements are low.

The LVS should be filtered with a common-mode choke to reduce noise into the converters. The noise dissipated in the choke could otherwise radiate through the board, reducing the general performance. The choke must be rated for the maximum Master Controller current and voltage. It should have a wide common-mode impedance peak and as little differential impedance as possible.

²<https://www.xilinx.com/products/technology/power/xpe.html>

19 Programmer

The Zynq supports programming and debugging through a standard JTAG interface. On the PicoZed [1, p. 27], the JTAG uses the header connections specified in Table 11. These are dedicated JTAG pins on the Zynq, allowing both the PS and PL domains to be programmed. The JTAG's reference voltage must be 3.3 V for signal compatibility.

Signal	Header pin	Zynq pin
JTAG_TCK	JX1 pin 1	F9
JTAG_TMS	JX1 pin 2	J6
JTAG_TDO	JX1 pin 3	F6
JTAG_TDI	JX1 pin 4	G6

Table 11: Overview of the pins used for JTAG connections on the PicoZed

It is possible to implement an in-circuit programmer and debugger that turns USB data into JTAG and UART signals. This would allow both programming and debugging of the Zynq using just a USB connector, which would greatly simplify programming, testing and debugging, but requires an isolator for safety. The primary drawback is that the ICs required for this setup are costly, and the isolation requires space. Instead, a cheap JTAG connector could be placed on the board, and an external JTAG programmer can be used, which requires much less space. The programmer is more expensive, but can then be re-used for other PCBs. The primary drawback is the lack of UART communication built into the programmer, which would need to be added separately.

The drawbacks of a USB module are outweighed by the flexibility and ease of using a USB connection for both JTAG and UART, as well as being cheaper, for which reason this solution is chosen for programming.

19.1 Bluetooth

Eventually, a UART Bluetooth connection may be needed both for live diagnostics and debugging, but also for writing firmware to the non-volatile memory wirelessly. For this reason, space should also be made for a Bluetooth module. The Bluetooth should be low-power and with decent range. While some modules have reasonable range with integrated ceramic and microstrip antennas, these are also unusable if the enclosure is grounded and used as electromagnetic shield against noise. For this reason, a module with external antenna should be chosen.

20 Live-View

Two Gigabit Ethernet Controllers are built into the Zynq-7000. On the PicoZed board, Ethernet Controller 0 has been connected to a PHY using PS pins, resulting in an RGMII Ethernet interface. The Ethernet PHY used is the Alaska 88E1512 from Marvell [26], which has its differential signals routed to JX3 on the PicoZed. The PicoZed also contains connections for implementing power and activity LEDs [1, p. 40]. The full overview of the signal connections is shown in Table 12.

JX3 Pin Number	Signal Name
47	PHY_LED0
48	PHY_LED1
51	MD1_P
52	MD2_P
53	MD1_N
54	MD2_N
57	MD3_P
58	MD4_P
59	MD3_N
60	MD4_N

Table 12: Overview of Ethernet PHY signal connections from the PicoZed

The Wireless Access Point (WAP) chosen by SDU-Vikings for the live-view is Ubiquiti's NanoStation AC Loco, which is powered through the Ethernet cable as specified in the datasheet [27]. The WAP is connected to the supply on pin pair 4-5 and ground on pin pair 7-8. This leaves data pairs 1-2 and 3-6 for a transfer rate of 100 Mbit/s. These are MD1 and MD2 respectively, while MD3 and MD4 must be left unconnected. When using 100 Mbit/s, the serial communication is 4B5B coded by the PHY, meaning four data bits are turned into a five bit code for EMI purposes. This is then MLT-3 encoded, which has three states depending on the differential voltage: -1, 0, and +1. When the clock's falling edge is registered, a bit is sampled. If the state has changed since last edge, this equates to a digital 1, while a digital 0 is registered if the state has not changed. The bits are then scrambled to reduce EMI [10, p. 15].

Due to the higher IP rating and safety, an 8-pin circular connector must be used to connect the differential Ethernet signals instead of a common RJ45. Space can be made in the enclosure for an angled connector at the edge of the PCB, making it accessible from the outside.

The NanoStation WAP supports voltages in the range 21.6 V to 26.4 V, nominally 24 V, with a current of 0.3 A. This cannot be directly supplied by the LVS, for which reason a Buck-Boost converter must be implemented. The current should be monitored and controlled by the Zynq using a SmartFET, as with other nodes supplied with the LVS.

21 Driverless

The driverless computer has not been implemented, but an adequate connector must be placed for future communication with it. This link will contain data in both directions, with the Master Controller sending current status information and receiving updated targets. The transfer rate is not known at this time, but it will not realistically carry more data than the six 1 Mbit/s CAN buses already implemented. The easiest solution for data transfer is Ethernet, as this can interface directly with most computers at high transfer rates and long distances. The 100 Mbit/s transfer rate provided by the MII serial interface is sufficient.

Using MII as opposed to GMII has the benefit of fewer connections, lower frequencies, and lower power consumption, all while still having adequate transfer rate for the needs. This will reduce the overall noise and layout complexity. The only drawback is slightly longer latency due to slower data transmission, but the timings are still much faster than the car demands. As the PicoZed is only equipped with one Ethernet PHY, another must be added to the Master Controller PCB. The PHY's differential output signals must then be routed into a circular connector, like with the live-view.

22 Data Storage

The Zynq-7000 contains an SDIO controller for writing data to SD cards through a QSPI-like serial interface. The SDIO interface expands on QSPI with a command signal, card detect signal, and write protect signal. SD cards are space efficient, and up to 32 GB storage is supported according to the PicoZed Carrier Card Hardware Guide [28, p. 32]. If the SDIO peripheral uses the MIO interface, the writing frequency is up to 50 MHz, equating to 25 MB/s [2, p. 367], while it is limited to 25 MHz with the EMIO interface. The transfer rate on the X90 is not known, however an estimate can be calculated. It is assumed that 300 variables' types and values are written 10 times a second, which is the frequency on the X90 [3, p. 12]. Calculating with an average value being 5 ASCII characters long, while the average type is 20 ASCII characters long, the required transfer rate can then be calculated as

$$\text{rate} = (5 \text{ bytes} + 20 \text{ bytes}) \cdot 300 \text{ variables} \cdot 10 \text{ Hz} = 75 \text{ KB/s} \quad (22.1)$$

This should not be a problem. A 32 GB card will, with a data rate of 75 KB/s, be filled in around 110 hours, meaning no additional storage is needed.

To remove noise and protect the circuits, EMI filters and ESD diodes are needed on the PCB. Pull-up resistors must also be used to avoid floating pins.

23 Configuration Parameter Storage

During operation, several parameters may need to be stored. These parameters could include calibration values and offsets used in calculations. Usually such parameters are stored as constants in ROM when the microcontroller is programmed. These parameters may be modified during operation if, for example, new calibration values are found or the motors' positions must be stored between runs. These stored parameters must not be lost when power cycling or turning off the Master Controller. The parameters should therefore be stored in programmable ROM or similar, whereby the parameters are readily available the next time the Master Controller is enabled, and the vehicle is put in drive mode.

Electrically Erasable Programmable ROM (EEPROM) is slow with write times of 10 ms and has limited, albeit long, life cycles. An alternative to EEPROM is non-volatile Static RAM (nvSRAM). Non-volatile RAM is usually battery-backed, so the non-volatile cells are always supplied. This makes the nvSRAM option more expensive and bulkier. The advantage of using nvSRAM is that it has faster access times and almost unlimited lifetime.

EEPROM or nvSRAM can either be parallel or serial. Parallel memories use one data line per data bit and one address line per address bit. Serial memories communicate with the master over serial protocols such as I₂C or SPI, and therefore require fewer connections. A parallel memory will be able to read close to a byte per clock cycle, while the serial memory is much slower and usually has a lot of message overhead.

As the memory should be accessed quickly, nvSRAM is chosen as storage technology. To limit the amount of signal lines, a serial connection is preferred.

24 Inertial Navigation System

The INS has not been implemented, but a navigation module has been chosen by the SDU-Vikings team. This is the VectorNav VN-200 [29], which among other things contains gyros, accelerometers, magnetometers, and GPS. The rugged packaging option has been chosen, which implements a 10-pin connector. A description of the pinouts of this connector can be seen in Table 13.

For communication, two serial Universal Asynchronous Receiver-Transmitter (UART) options are available. Transistor-Transistor Logic (TTL) voltage levels are between 0 V and 3 V, while RS-232 ranges from $-V_{cc}$ to $+V_{cc}$. The transmitted data is identical. TTL voltage levels can be routed directly to the Zynq, but are more susceptible to noise due to the lower voltages. Conversely, the RS-232 levels need to be translated by an IC. This IC could potentially include both ESD protection and filtering of the lines, which is needed either way. For this reason, the price and size difference is minimal, and so RS-232 outputs are used and TTL outputs are left unconnected.

Connections should be made for the synchronization signals and GPS pulse, as they

Pin	Pin Name	Description
1	VCC	+3.3 V to +17 V
2	TX1	RS-232 level Serial UART1 output
3	RX1	RS-232 level Serial UART1 input
4	SYNC_OUT	Configurable synchronization output
5	GND	Ground
6	RESTORE	Restores factory default if high at reset
7	SYNC_IN	Configurable synchronization input
8	TX2_TTL	TTL level Serial UART0 output
9	RX2_TTL	TTL level Serial UART0 input
10	GPS_PPS	TTL level GPS Pulse Per Second

Table 13: Pinout description of rugged VN-200 module

could prove useful when programming the INS. In the event of the VN-200 becoming inoperable, it should be possible to restore the device by pressing a switch connected to the RESTORE pin when powering on the Master Controller.

As the Zynq-7020 only provides 2 UART controllers, the programmer, Bluetooth, and INS cannot all be connected at the same time. Any of them could be connected to the PL, in which a UART interface is created manually. This requires only a small amount of logic, but increases complexity of the software. Alternatively, modules can be active or left unused by implementing $0\ \Omega$ resistors in series. As the programmer and Bluetooth are unlikely to be used at the same time, the latter option is chosen for these.

25 Expansion Board

One of the big advantages to the X90-based Master Controller is the relative ease of adding extra functionality. Option boards can be bought and attached to the X90, allowing additional analog or digital I/O, like CAN buses. Due to the flexibility of the Zynq's PL pins, a similar feature can be added to the Master Controller PCB.

By adding a large number of pin headers, like those found on Arduino boards or development kits, future functionality can be added by designing a matching expansion PCB containing the needed components. The headers will need to provide adequate supply and ground, as well as a reasonable number of connections to both the Zynq PL pins and external connectors. Receptacles like those used for the PicoZed can also be used in place of pin headers. These are smaller, but can carry less current and are more expensive. As board space is valuable, receptacles are chosen as expansion connection.

An example of an expansion board contains an ADC for sampling auxiliary sensor voltages. This ADC will need to be supplied, and the PCB must also further supply the external sensors, having the option of using different voltages. The ADC is connected to the Zynq's PL pins for serial communication.

25.1 Zynq Connections

To confirm that there are enough available resources to implement the expansion board, the Zynq's connections are analyzed. Table 14 contains the Zynq I/O pins available on the JX headers, as well as the required pins for each Master Controller module. The flexibility of the Zynq means that most peripherals can be used on a variety of pins, even if Processing System pins are used. As Bank 500 is supplied with 1.8 V on the PicoZed, the pins in that bank may need to be level shifted to be used. Optimally, all free PL pins would be routed to the expansion board. This is deemed impractical and not needed, and instead half the free pins are assigned to it.

Purpose	1.8V PS	3.3V PS	3.3V PL
Available	12	8	125
Actuators	2	1	0
ADC	0	0	28
Bluetooth Misc.	0	0	2
CAN 0	0	0	2
CAN 1	0	0	2
Ethernet 1	0	0	20
INS Misc.	0	0	3
LVS Distribution	9	0	0
nvSRAM Misc.	0	0	2
PoE Distribution	0	0	1
Shutdown Circuit	0	0	11
SPI 0	0	0	4
SDIO 1	0	7	0
UART 0	0	0	4
UART 1	0	0	2
Expansion Board	0	0	22
Total free	1	0	22

Table 14: Zynq pins available through the PicoZed JX headers

25.2 External Connectors

The large amount of used pins consequently also require large connectors to be placed on the PCB for connecting to the entire car. The connectors commonly used in SDU-Vikings are automotive Molex CMC, which exist with various pin counts and current ratings. As most CMC connectors are not rated for currents higher than 12 A, the LVS should supply the Master Controller through multiple pins. Only the two Ethernet connections will not be using the CMC connectors, instead using circular connectors. An overview of the needed connections on the Molex CMC connectors is shown in Table 15, which includes 22 connections for the expansion board. This ensures that the expansion board will not be limited by CMC connections.

Purpose	CMC Pins
AMS Supply	2
Brake Light	2
Brake Sensor 1	3
Brake Sensor 2	3
CAN Bus 1	6
CAN Bus 2	6
Cooling System	8
Dashboard Supply	2
INS	8
Inverter 1+2 Supply	2
Inverter 3+4 Supply	2
LVS Supply	6
Ready-to-Drive-Sound	2
Sensor Network Supply	2
Shutdown Circuit	21
Steering Sensor	3
Torque Sensor 1	3
Torque Sensor 2	3
TSC Supply	2
Expansion Board	22
Total	108

Table 15: Molex CMC connections needed for each part of the Master Controller

26 Summary of Analysis

The analysis confirms that the Zynq-7020 contains enough resources for use in the Master Controller, including providing enough connections for expansion of functionality.

The Low Voltage System will be distributed with a SmartFET solution to all electronic nodes and the cooling system, while the RTDS and brake light will be controlled by Solid-State Relays. The SmartFETs have built-in current sensing, while the relay currents are to be measured across shunt resistors.

The Shutdown Circuit will be isolated with optocouplers and monitored with the GPIO. Solutions for flexible sensor supply and filter circuits have been chosen, and theory of conversion accuracy has been examined. Sallen-Key filters will be used by external sensors, while RC filters are used for signals originating on the PCB.

The CAN bus load has been simulated, confirming that the two Zynq CAN controllers are sufficient.

For live-view and driverless communication, 100 Mbit/s Ethernet has been chosen. Live-view requires a 24 V converter for Power-over-Ethernet.

Data storage types have been chosen, an SD card being used for diagnostics storage and nvSRAM for configuration parameters.

Considerations have been made in regards to EMC of the board by using ESD diodes, ferrite beads, and a common-mode choke for relevant circuits.

Part III

Hardware Design

Using the analysis performed in the previous part, subcircuits can be designed that meet the set requirements. The design culminates in a PCB that must also fulfill mechanical necessities when used in the car.

27 Power Distribution and Monitoring

The SmartFETs for distributing and monitoring the LVS are chosen from Infineon's PROFET™+24V series, which contain an assortment of 5-36 V switches. These have between one and four independent channels, with on-resistance down to 10 mΩ and nominal load currents up to 9 A. The FETs can be enabled with a digital 3.3 V signal, and output a sense current based on the measured load current.

The multi-channel FETs have higher resistances and thus lower nominal load currents, and are well-suited for the low-current nodes. The PROFET chosen for this is the dual-channel BTT6030-2EKA, with 30 mΩ on-resistance and a nominal load current of 4 A on each channel when both are active [30]. The nodes, as previously listed in Table 2, have been assigned to specific PROFETs as specified in Table 16 to spread out the currents evenly among the three needed dual-channel FETs, consequently distributing the heat evenly. The downside of this is that current measurements will be less accurate, as the voltage is designed to be 1 V at the maximum current in each FET.

Node	Current	Assigned PROFET
Dashboard	1 A	1
Accumulator	1 A	1
TS Container	0.2 A	2
Inverter 1 + 2	2.5 A	2
Inverter 3 + 4	2.5 A	3
Sensor Network	1 A	3

Table 16: Each module, estimated current, and PROFET for even distribution of currents

For currents over 4 A, the single-channel PROFET BTT6010-1EKB, with 10 mΩ on-resistance and a nominal load current of 9 A [31], can be used. The FET could also be used for lower currents, resulting in lower losses. As this would require more components, it is not deemed worth it both due to size and price.

The circuits surrounding the PROFETs are designed using the recommendations of the PROFET datasheets [30][31] and PROFET™+ 24 V Application Note [32]. For loss-of-ground protection, 4.7 kΩ resistors are placed serially on the digital pins used for interfacing with the Zynq. Additionally, a 33 Ω resistor and Schottky diode are placed between the GND pin and ground to limit the current and voltage, and for reverse polar-

ity protection.

The Zynq pins chosen for digital interface with the PROFETs are 1.8 V, meaning they must be level translated to 3.3 V. This is accomplished by using the SN74LV4T125, a 4-channel level translator [33]. To save board space when not all four channels are needed, the SN74LV1T34 single-channel level translator [34] is used.

The current sense circuits must be designed carefully. The Zynq's XADC dynamic area is 0-1 V, and the absolute maximum input voltage on the XADC channels is 1.8 V. As the output voltage of the current sense port is only limited by the supply voltage, the voltage should be clamped for safety. The current sense port output can be represented as a current source, whose output current is proportional to the load current by a factor k_{ILIS} . The maximally expected load current, $I_{L,max}$ should produce 1 V on the XADC channel. The current sense resistor R_{IS} can be calculated by

$$R_{IS} = \frac{V_{ADC,max}}{I_{L,max}/(k_{ILIS}(1 - k_{ILIS,tol}))} \quad (27.1)$$

where the factor $(1 - k_{ILIS,tol})$ is a result of k_{ILIS} having a tolerance of $\pm k_{ILIS,tol}$. The value k_{ILIS} of the BTT6030-2EKA is 2240, while the tolerance is $\pm 8\%$. The tolerance gives an interval for the resistor. Using only -8% results in the lowest resistor value, and thus the lowest and safest voltage. For the BTT6010-1EKB, these values are $k_{ILIS} = 3900$ and $k_{ILIS,tol} = \pm 9\%$.

As the voltage on the XADC channel should be kept well below 1.8 V, a Zener diode is used to clamp the voltage. The lowest breakdown voltage found on Zener diodes, however, is 1.8 V. To keep a safe distance to the absolute maximum voltage on the XADC input, a voltage divider is implemented by the sense current pin. R_{IS} must not be changed, but the accompanying resistor is designed for a higher voltage, where a fitting Zener breakdown voltage can be found. Figure 16 shows the circuit surrounding the sense pin with the safety changes implemented.

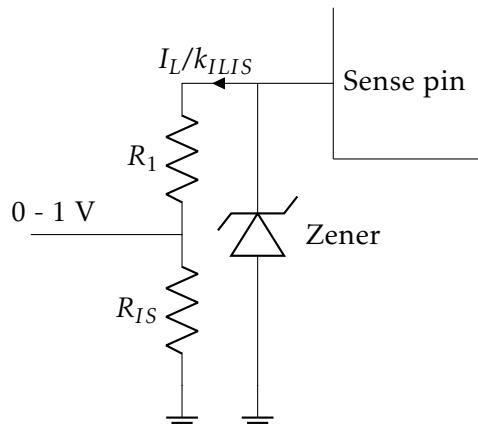


Figure 16: PROFET current sense pin output circuit for connecting to XADC

Choosing to use the 5.6 V Zener diode MMSZV6T3G [35], the resistor used for voltage division can then be calculated giving

$$R_1 = 4.6 \cdot R_{IS} \quad (27.2)$$

The resulting values for R_{IS} and R_1 , using real resistor values, are shown in Table 17.

PROFET	R_{IS}	R_1
1	2.05 kΩ	9.42 kΩ
2	825 Ω	3.79 kΩ
3	825 Ω	3.79 kΩ

Table 17: Current sense resistors calculated for each PROFET

Using the above resistors results in a voltage between 0 V and 1 V on the XADC pins. At short-circuit conditions, the XADC will read the maximum value due to voltage clamping. Knowing the voltage, the current can be approximated with the equation

$$I_L = \frac{V_{ADC}}{R_{IS}} \cdot k_{ILIS} \quad (27.3)$$

Since the Master Controller must also measure its own current, a shunt resistor must be used. The Master Controller is expected to draw a current of up to 4 A. The voltage difference across the shunt must then be amplified, for which the TSC2012IDT current sense differential amplifier IC [36] is used. This IC contains EMI filters for accurate measurements, and has a fixed difference gain of 100. A shunt resistor must then be chosen for accurate use across the entire dynamic range while minimizing power loss. For this, Equation 2 from the TSC2012IDT datasheet is used [36, p. 30]. This equation aids in determining the maximum shunt resistor size to balance the losses and dynamic range, and for this application is

$$4A \cdot R_{sense} = \frac{5V - 0.2V}{100 \cdot (1 + 0.3\%)} - 2 \cdot 500 \mu V \quad (27.4)$$

This results in a maximum sense resistance of 11.7 mΩ. The resistor LVK12R010CER, with a resistance of 10 mΩ and power rating of 0.5 W [37], has been chosen for this application.

The output voltage from the IC will then at most be

$$V_{out,MCI} = 4A \cdot 10m\Omega \cdot 100 = 4V \quad (27.5)$$

This must be routed through a voltage divider to ensure that it is no higher than 1 V before conversion in the Zynq XADC. For safety, it must be assumed that a 5 V output is possible due to the IC supply, which should result in 1 V on the XADC pin. Knowing the converted voltage, the current can then be calculated as

$$I_L = \frac{V_{ADC} \cdot 5}{R_{sense} \cdot 100} \quad (27.6)$$

27.1 Test of SmartFETs

In Appendix C, a PCB for testing the functionality of the SmartFETs is designed, manufactured and tested with the purpose of determining whether the PROFETs are suitable for use in power distribution and power monitoring in the Master Controller. The results of the test are in summary that the PROFETs are controllable by the Zynq, the voltage to be measured by the XADCs are proportional to the load current and that the heat generated by the PROFETs can be a problem if running at the nominal load current of the devices. It is also seen that the on-resistance of the PROFET channel increases with increasing package temperature. Lastly, it was concluded that the PROFETs act as fuses when conducting currents exceeding the nominal value.

28 Actuators

The approach to the actuators is similar to power distribution and monitoring from Section 27. For the cooling system, which draws up to 7 A, the single-channel PROFET is used. This will be referred to as PROFET 4. The surrounding circuits are designed as before, with the BTT6010-1EKB having a $k_{ILIS} = 3900$ and $k_{ILIS,tol} = \pm 9\%$ resulting in $R_{IS} = 510\Omega$ and $R_1 = 2.37\text{k}\Omega$.

Knowing the voltage, the current can thus be approximated with the equation

$$I_L = \frac{V_{ADC}}{510\Omega} \cdot 3900 \quad (28.1)$$

For the RTDS and Brake Light, a Solid-State Relay must be used in combination with a sense resistor and differential amplifier to measure the current. Once more using the TSC2012IDT differential amplifier, the resistor values are calculated as previously. This results in a maximum resistance for the Brake Light of 0.78Ω , and 5.86Ω for the RTDS. The chosen resistors are CRL0805-FW-R750ELF [38], a 0.75Ω 1% resistor with a $1/8\text{ W}$ power rating, and the ERJ-3RQF5R6V [39] with 5.6Ω 1% resistance and a $1/10\text{ W}$ power rating.

The maximum output voltages from each differential amplifier are thus

$$V_{out,BLI} = 0.06\text{ A} \cdot 0.75\Omega \cdot 100 = 4.5\text{ V} \quad (28.2)$$

$$V_{out,RTDSI} = 0.008\text{ A} \cdot 5.6\Omega \cdot 100 = 4.48\text{ V} \quad (28.3)$$

Like with the Master Controller current measurement, this must be routed through a voltage divider, assuming a maximum value of 5 V, before conversion, and the current can be calculated with Equation 27.6.

The SSR used for enabling the actuator outputs is the CPC1017N [40], capable of delivering 100 mA at 60 V. The relay can be activated with a voltage above 1.4 V and current above 1 mA, which can be delivered by the Zynq's 1.8 V PS pins. A resistor must be put in series to limit the current.

29 Shutdown Circuit Monitoring

The optocouplers used for isolation and level shifting of the Shutdown Circuit signals are the LTV-8x7 [41], which have a phototransistor output. The input to the diode-side of the optocouplers is the SC output of the individual devices in the SC. The current through the diode must be limited by a resistor. As the diode and phototransistor in the optocoupler are coupled through the diode's emitted infrared light, the common-emitter saturation voltage, $V_{CE(sat)}$, in the phototransistor is dependent on the forward current, I_F , in the diode. A low $V_{CE(sat)}$ is desirable, as this lowers the conduction losses in the phototransistor at a given collector current, I_C .

From the optocoupler's datasheet, several characteristic curves are found for the optocouplers. It is noted from Figure 3 in the datasheet that a low collector current, I_C , and high forward current, I_F , result in a low collector-emitter saturation voltage, $V_{CE(sat)}$. At $I_F = 5\text{ mA}$ and $I_C = 1\text{ mA}$, it is found that $V_{CE(sat)} \approx 0.2\text{ V}$. Using load-line analysis on an approximate curve of the 25°C curve in Figure 4 in the datasheet, a current-limiting resistor can be found. With the LV supply of 24 V , a $4.7\text{ k}\Omega$ resistor in series with the diode will give a forward current of $\sim 4.9\text{ mA}$. With a 12 V supply, the current is halved, but diode and transistor characteristics are not notably changed. Pulling the phototransistor's collector up to 3.3 V through a resistor gives logical high at the collector pin when the diode is not conducting. When the diode is conducting, the phototransistor should conduct a current $I_C \approx 1\text{ mA}$. Choosing a pull-up resistor of $2.7\text{ k}\Omega$ should give a collector current of about 1 mA , taking V_{CE} into account.

30 Analog-to-Digital Converter

All sensors are supplied with either 5 V or 12 V , depending on the position of the jumper. Using Equation 15.1 and Equation 15.2, the torque pedal sensor resistors are found, limiting the output voltages to $15\% - 75\%$ of supply for torque sensor 0 and $25\% - 85\%$ of supply for torque sensor 1. A summary of the design is shown in Table 18.

Sensor	Supply	Component	Value
Torque 0	Any	R_{top}	$2.1\text{ k}\Omega$
Torque 0	Any	R_{bot}	$1.24\text{ k}\Omega$
Torque 0	5 V	Range	$0.74\text{ V} - 3.74\text{ V}$
Torque 0	12 V	Range	$1.78\text{ V} - 8.98\text{ V}$
Torque 1	Any	R_{top}	$1.24\text{ k}\Omega$
Torque 1	Any	R_{bot}	$2.1\text{ k}\Omega$
Torque 1	5 V	Range	$1.26\text{ V} - 4.26\text{ V}$
Torque 1	12 V	Range	$3.02\text{ V} - 10.22\text{ V}$

Table 18: Summary of the design parameters for the torque sensors

All inputs from external sensors have had the unidirectional ESD diode ESD5Z12T1G

[42] placed by the connector. This diode has a working voltage of 12 V and clamping voltage of 17 V. Additionally, a $200\text{ k}\Omega$ pull-down resistor has been placed by the diode to ensure that an open circuit does not result in floating pins.

The sensor voltages are routed through voltage dividers depending on jumper pin configuration. These voltage dividers are designed to ensure that a short-circuit to supply will result in 1 V on the XADC pin. Typical Surface-Mount Device (SMD) resistors have a tolerance of $\pm 1\%$, which introduces a gain error to the conversion. More expensive resistors with lower tolerance can be used to reduce the error. To separate the voltage dividers from offset resistors in the torque pedal supply, a voltage buffer has been placed between the ESD diode and voltage divider. This introduces an additional offset voltage.

All external sensor signals are then passed through a second-order Sallen-Key active Butterworth filter and high-frequency passive filter. The Sallen-Key filter has been designed with a cut-off frequency of 450 Hz, with an attenuation requirement of 50 dB at 8 kHz. The op amp used for the design is the MCP6L02T-E/SN [43], which contains two rail-to-rail channels with high bandwidth. The operational amplifier has a high offset voltage of up to 5 mV, but a low bias current of 2 pA. Other operational amplifiers in the same price range have either high offset voltage or high bias current. More expensive amplifiers do have lower values for both offset voltage and bias current, but as the offset error can be somewhat mitigated by software calibration, cheaper hardware can be used. The full circuit for a torque pedal signal can be seen in Figure 17.

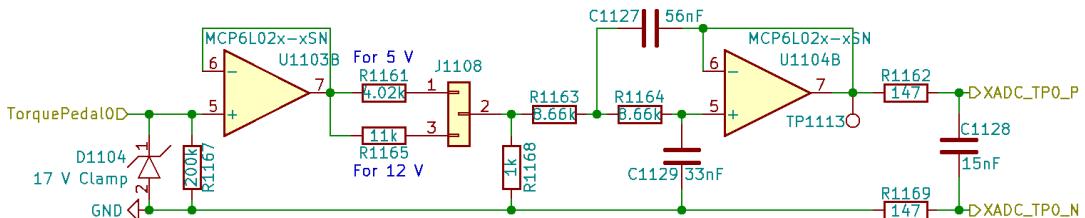


Figure 17: KiCad circuit diagram of circuits used for filtering and attenuation of torque pedal sensor signal

Sensor pairs are connected to the same op amp to ensure identical noise impact. The passive filters' resistors have been designed to limit current from the op amp to ensure stability when supplying the capacitor. Carrying over the component references from Figure 15, the filters' component values are shown in Table 19. This table also shows the Sallen-Key filter's settling time calculated with Equation 16.4. These are actual component values, resulting in changes to cut-off frequency and settling time. The settling time is slightly higher than the requirement of 5 ms, but the requirement was set with a deviation like this in mind. As the total settling must be less than 10 ms, the difference should not impact performance.

With the component values, the filter's transfer function is found using the general low-pass transfer function from [22, p. 4], being

$$G(s) = \frac{1}{1.39 \cdot 10^{-7} \cdot s^2 + 0.0005716 \cdot s + 1} \quad (30.1)$$

Component	Value
R_1	8.66 kΩ
R_2	8.66 kΩ
C_1	33 nF
C_2	56 nF
f_c	428 Hz
t_s	5.4 ms
R_{AA}	147 Ω
C_{AA}	15 nF
f_c	36.1 kHz
t_s	39.7 μs

Table 19: Summary of the filter values for the Sallen-Key filter and associated passive filter

The 'stepinfo()' function from the Control System Toolbox in MATLAB returns a settling time for this transfer function of roughly 2.6 ms. This does not correspond to the calculated value, and a simulation is thus well-warranted.

The signals originating from the Master Controller PCB, used for measuring currents and the LVS voltage, do not have ESD diodes, and the filtering requirements are lower. The voltage dividers have been implemented by the current sense pin on the PROFET, and vary by module, as described in Section 27. The measurements are filtered with an RC circuit with a cut-off frequency of 285 Hz, resulting in a 5 ms settling time. The components used for accomplishing this, as they differ depending on voltage divider resistance, are listed in Table 20.

Measurement	Resistor	Capacitor
LVS Voltage	24.3 Ω	280 nF
Master PCB Current	41.2 Ω	330 nF
Dashboard/AMS Current	160 Ω	150 nF
TSC/Inverter 1 + 2 Current	160 Ω	330 nF
Sensor Net/Inverter 3 + 4 Current	160 Ω	330 nF
RTDS Current	41.2 Ω	330 nF
Brake Light Current	41.2 Ω	330 nF
Cooling System Current	137 Ω	470 nF
Power-over-Ethernet Current	137 Ω	82 nF

Table 20: Component values of RC low-pass filters for on-PCB measurements

30.1 Simulation of Sallen-Key filter

The Sallen-Key filter is simulated in ngspice using a real operational amplifier. The settling time of the Sallen-Key filter with a 1 V pulse is shown in Figure 18, which once more is satisfying. The overshoot is not high enough to damage the XADC.

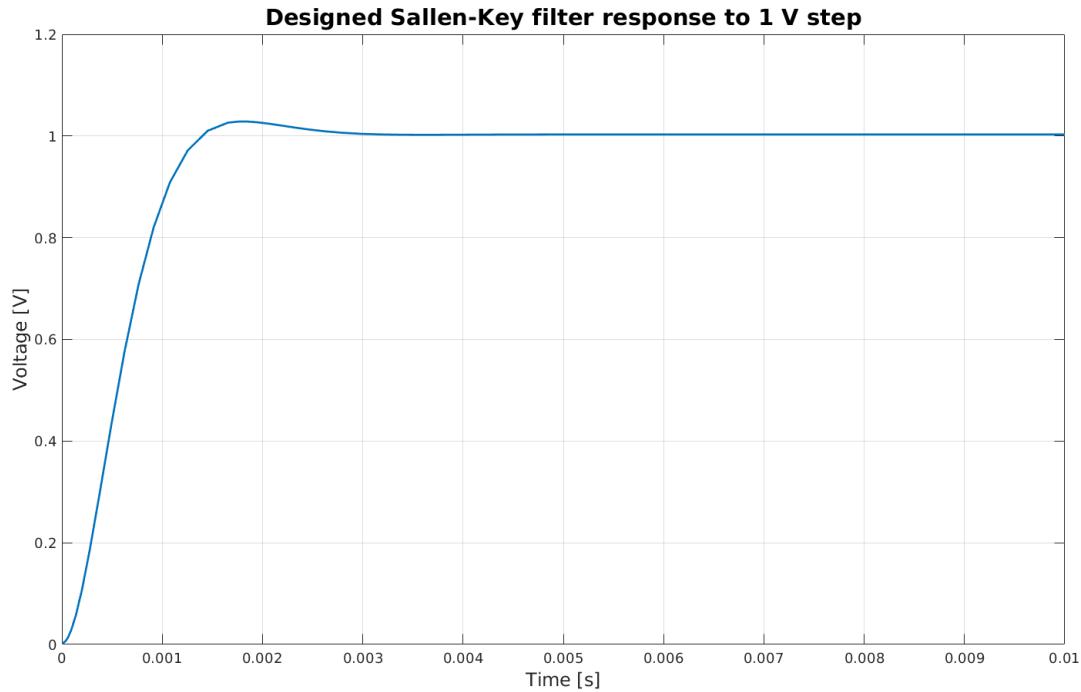


Figure 18: Simulation of the Sallen-Key filter's settling time with a 1 V pulse

The Sallen-Key filter is also simulated with and without the subsequent RC filter to compare transfer functions. The results are shown in Figure 19 and indicate that the Sallen-Key filter's attenuation is reduced above 100 kHz, which is outweighed by the RC filter. The filter attenuates 8 kHz signals with 51 dB, meeting the set requirements.

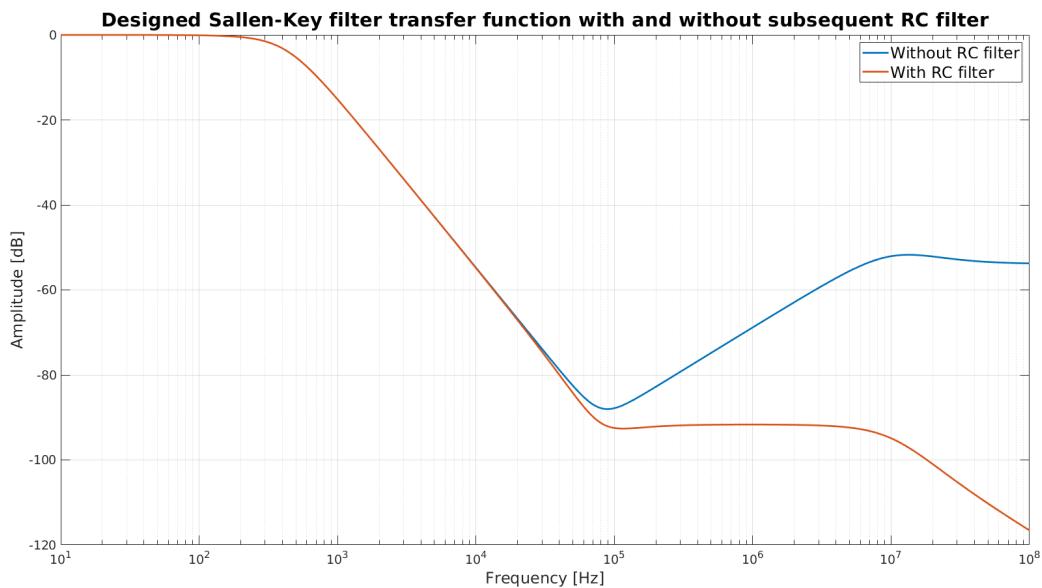


Figure 19: Transfer function of Sallen-Key filter with and without subsequent RC filter

30.2 Sensor Accuracy

Following the approach of Subsection 16.1, the minimum mechanical ranges of the steering wheel sensor and torque pedal sensors are found. The steering wheel sensor is linear to within 0.5% across its range, while the torque pedal sensor is linear to within 1%.

The inaccuracy due to the active filter for the steering wheel is calculated with Equation 16.8, using the MCP6L02T's characteristics. This results in an inaccuracy of

$$V_{OA,sw} = 5 \text{ mV} + 2 \text{ pA} \cdot (8.66 \text{ k}\Omega + 8.66 \text{ k}\Omega) \approx 5 \text{ mV} \quad (30.2)$$

As the torque sensors also contain a buffer with the same op amp, but placed before the voltage divider, the offset voltage is increased to a worst-case value of

$$V_{OA,tp} = \left(1 + \frac{1}{5}\right) \cdot 5 \text{ mV} + \left(1 + \frac{1}{5}\right) \cdot 2 \text{ pA} \cdot (8.66 \text{ k}\Omega + 8.66 \text{ k}\Omega) \approx 6 \text{ mV} \quad (30.3)$$

Using the values of Table 5, and assuming 0.5% resistors are used, the minimum range for 1% accuracy for the steering wheel sensor is

$$\text{range}_{\min,sw} = \frac{(1.71 \text{ mV} + 5.00 \text{ mV}) \cdot 100}{1\% \cdot \frac{9.9 \text{ V}}{360^\circ} \cdot 0.995 \cdot \frac{1 \text{ k}\Omega \cdot 0.995}{1 \text{ k}\Omega \cdot 0.995 + 11 \text{ k}\Omega \cdot 1.005}} = 296.98^\circ \quad (30.4)$$

This is a very high range, and improbable in actual use. Reducing the accuracy to $\pm 2\%$ results in a more realistic range of 148.49° . For the torque sensors, the minimum range is

$$\text{range}_{\min,tp} = \frac{(1.71 \text{ mV} + 6.00 \text{ mV}) \cdot 100}{1\% \cdot \frac{3 \text{ V}}{50 \text{ mm}} \cdot 0.99 \cdot \frac{1 \text{ k}\Omega \cdot 0.995}{1 \text{ k}\Omega \cdot 0.995 + 4.02 \text{ k}\Omega \cdot 1.005}} = 65.68 \text{ mm} \quad (30.5)$$

This is not possible, as the sensor only has a travel range of 50 mm. Reducing the accuracy to $\pm 2\%$ results in a range of 32.84 mm, which is more probable. The largest error for both signals can be attributed to the op amps' maximum offset voltage. Typically it is only 1 mV, but this does not guarantee the specified sensor accuracy. Should higher accuracy be needed for the signals, the op amp MCP607T, while three times more expensive, has a maximum offset voltage of 250 μ V and identical bias current. The op amp is footprint compatible with the MCP6L02T. With this op amp and 1% accuracy, the minimum ranges are 86.75° and 18.82 mm for the steering wheel sensor and torque pedal sensors respectively. Alternatively, software calibration of each XADC channel can improve the accuracy to acceptable levels.

31 CAN Modules

For communication with other devices in the vehicle, two identical CAN Transceiver circuits must be designed, as specified in the analysis of the CAN network in Subsection 17.2. The CAN Transceiver is chosen based on its automotive qualifications and the fact that it must be compatible with the Zynq and its 3.3 V supply. As the Master Controller must communicate with a lot of different devices, the CAN Transceiver must be compatible with both 5 V and 3.3 V CAN. High common-mode transients can appear on the bus lines which the CAN Transceiver must be able to withstand.

The SN65HVD235 [44] is chosen as a CAN Transceiver, as it complies with the requirements put forward and has a low power consumption. When designing the EMI/ESD bus protection circuit for the CAN Transceiver, many factors must be taken into account. These include maximum supply voltage, common-mode voltage, maximum transmission speed, ESD rating and coupled electrical disturbances [9, p. 9].

The TVS diode must be chosen such that the minimum breakdown voltage is greater than the maximum system supply voltage. Furthermore, the TVS device must not clamp the transmission signal during normal operating conditions. When choosing a TVS device, the internal capacitance of the device must also be less than 35 pF as discussed in Subsection 11.2.

The recommended operating voltages on the bus terminals is between -7 and 12 V. Any voltages outside this range is considered outside normal operating range. The TVS diode should therefore not clamp the signal while within this range. The VCAN16A2 [45] is chosen for its low maximum diode capacitance, 17 pF, and its working voltage of ± 16 V. The TVS diode has a maximum breakdown voltage of ± 20 V and reverse clamping voltage of ± 23 V at 1 A. As the SN65HVD235 has a maximum bus terminal voltage of ± 36 V this should be well within range.

To provide noise protection, split termination can be implemented as seen in Figure 20. R_H and R_L should both be 60Ω . This creates a common node between the two resistors that is terminated through a capacitor, C_{term} . The terminating capacitor works in conjunction with the terminating resistors as a low-pass-filter. The cut-off frequency can therefore be found with the equation

$$f_c = \frac{1}{2 \cdot \pi \cdot (R_H \| R_L) \cdot C_{term}} \quad (31.1)$$

A cut-off frequency above 1 MHz is desired, as this is the bitrate of the CAN bus. Using standard E6-series capacitors, a capacitance of $C_{term} = 2.2\text{nF}$ gives a cut-off frequency of 2.41 MHz, which is acceptable.

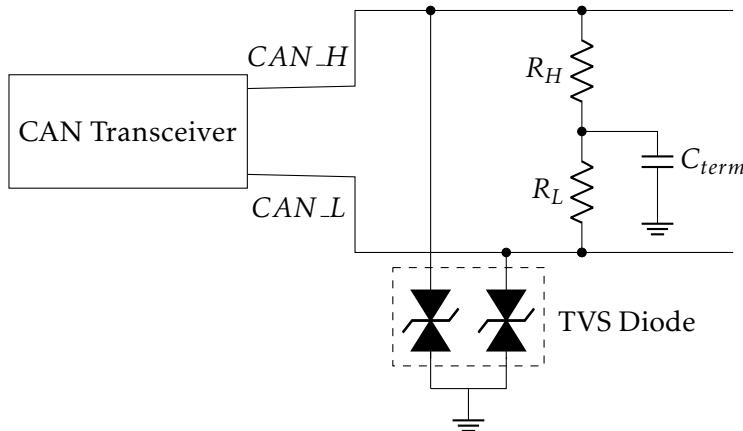


Figure 20: Split termination circuit for CAN Transceiver

32 Programmer

In order to connect the Master Controller to a computer with USB, a connector must be placed on the board. A Micro USB Type B connector is chosen for minimal size. The specific connector is the 10118194-0011LF SMD connector [46]. To protect the data lines, the PRTR5V0U4D,125 ESD suppressor [47] is connected to the data lines. The suppressor has very low capacitance and is designed for USB and similar high-frequency connections. A generic Würth header is placed by the connector, to be used as an additional method of connecting to the board.

The USB data is transmitted through the ADuM3160BRWZ USB Isolator [48], which allows transfers up to 12 Mbit/s. The USB-side is supplied by the USB's 5 V input. The Zynq-side is supplied with 3.3 V. 24 Ω series termination resistors must be placed on both USB-side and Zynq-side data lines to avoid line reflections impacting the signals [48, p. 10]. The isolated side of the USB transceiver can be seen in Figure 21.

The USB data will be interpreted by the JTAG-SMT3-NC SoM [49], which is designed for programming Xilinx FPGAs. The SoM will then transmit the data as JTAG or UART automatically. UART transmissions from the Zynq will be sent via USB to the computer. The voltage detection pin is driven by an optocoupler, which pulls the pin high when the USB connector is occupied. When not, it is pulled low and the SoM is disabled.

As a JTAG connector can be added to the board at a low cost, the Molex 87832-1420 14-pin connector [50] will also be connected to the JTAG lines. To ensure correct operation, a 50 Ω resistor must be placed between the JTAG connector and the TDO line, while the TMS, TDI, and TCK lines must be connected through 100 Ω resistors [49, p. 5].

32.1 Bluetooth

The RN4871U-V/RM118 [51] Bluetooth module is picked, which interfaces with the Pi-coZed using UART, uses little power, and is supplied with 3.3 V. The module connects to an external antenna through an SMA coaxial connector.

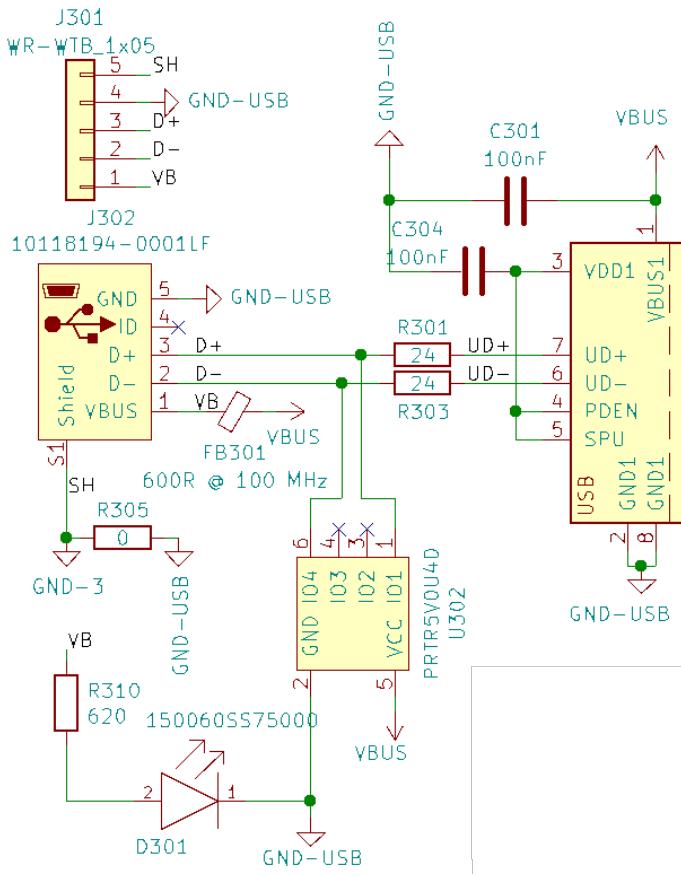


Figure 21: Isolated side of the USB transceiver circuit

As the Zynq is limited in UART interfaces, only one of the JTAG-SMT3-NC and Bluetooth UART lines are connected to the Zynq at any time. Initially, the JTAG-SMT3-NC will be used for programming and debugging. Eventually, the software is sophisticated enough to debug wirelessly via Bluetooth, after which point the Bluetooth UART lines can be connected with $0\ \Omega$ resistors and the JTAG-SMT3-NC resistors desoldered.

33 Live-View

The wide-input DC-converter chosen for supplying 24 V for Power-over-Ethernet is the isolated PDQE15-Q24-S24-D [52], with input voltages between 9 V and 36 V. The converter can supply up to 0.625 A at 24 V. The converter requires large input and output capacitors, which are specified in the datasheet [52, p. 6], for low ripple voltages. An EMC filter is placed by the input in accordance with the datasheet's recommendation for improved performance.

The converter's output is connected to a BTT6010-1EKB PROFET, which allows the Zynq to control whether the WAP is powered, and to measure the current. The PROFET will be referred to as PROFET 5. Using the same design approach as in Section 27, the resistors

$R_{IS} = 7.15\text{ k}\Omega$ and $R_1 = 33\text{ k}\Omega$ are calculated.

The 7490120110 magnetics IC [53], which is designed for Power-over-Ethernet, has been chosen for filtering of the differential signals.

The circular connector to be used for 100 Mbit/s Power-over-Ethernet is the Phoenix Contact 1437009 [54], which is M12, 8-pin, A-coded, and angled. The connector is capable of supplying up to 1.5 A, which satisfies the requirements. The connector's pins are shown in Figure 22. There is no industry standard for 8-pin M12 Ethernet connections. The connections are thus made by comparing an M12-to-RJ45 adapter to the RJ45 industry standard [55]. This results in the connections specified in Table 21.

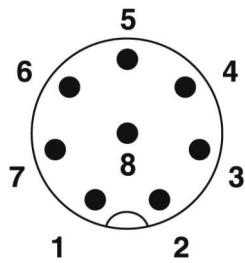


Figure 22: Pinout diagram of 8-pin M12

Pin	Signal
1	24 V
2	Ground
3	Ground
4	Tx-
5	Rx+
6	Tx+
7	24 V
8	Rx-

Table 21: Signals for 8-pin M12

Bob Smith termination for Power-over-Ethernet as specified in Figure 10 of [12] is placed by the connector. The circuits for the magnetics, termination, and circular connector are shown in Figure 23.

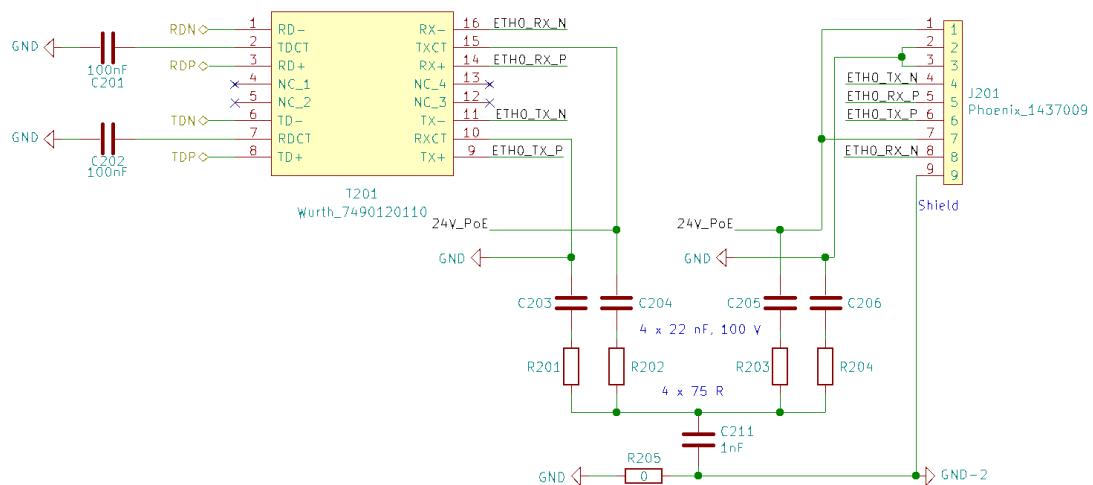


Figure 23: KiCad schematic of the live-view Power-over-Ethernet magnetics, Bob Smith termination, and connections to M12 connector

34 Driverless

The Ethernet PHY KSZ8081MNX [10] has been chosen for driverless Ethernet, as it uses the MII protocol, allowing 100 Mbit/s communication at a low cost and with a small size. The IC has built-in termination resistors, and can control LEDs. The datasheet [10] and hardware design checklist [56] have been used for designing the PHY subcircuits.

The IC core requires a 1.2 V supply, which is made internally with a Low-Dropout (LDO) regulator from the 3.3 V supply. The 3.3 V supply must be well-filtered with both a ferrite bead as well as bulk and decoupling capacitors. During power-on, certain pin values are latched and used for configuration of the PHY. To ensure that the correct settings are used, pull-up and pull-down resistors have been connected to these pins. The datasheet recommends 4.7 k Ω resistors for pull-up and 1 k Ω resistors for pull-down. A summary of the configuration is shown in Table 22.

Pin	Setting	Resistor
13	PHY Address 0	Pull-up (1)
14	PHY Address 1	Pull-down (0)
15	PHY Address 2	Pull-down (0)
16	Duplex	Pull-down (Full-duplex)
18	Config 2	Pull-up (MII)
19	Broadcast off	Pull-down (PHY add. 0 is broadcast)
20	Isolate mode	Pull-down (Disable)
21	NAND Tree	Pull-up (Disable)
28	Config 0	Pull-up (MII)
29	Config 1	Pull-up (MII)
30	Auto-negotiation	Pull-up (Enable)
31	Speed	Pull-up (100 Mbps)

Table 22: Summary of pull-up and pull-down resistors used for latch configuration of the KSZ8081MNX Ethernet PHY

The PHY's 3.3 V supply must be monitored to avoid risk of damaging the IC. This is done by asserting the PHY's reset pin in case of undervoltage. The voltage supervisor MIC826TYMT-TR [57] pulls the reset pin low while the voltage is under 3.075 V. The supervisor is also connected to a Zynq pin, allowing the software application to reset the Ethernet PHY by pulling it low.

The 25 MHz crystal ECS-250-18-33B-CKY-TR [58] with a ± 10 ppm tolerance is used for clocking the PHY. A crystal with sine wave is chosen over an oscillator with square wave due to lower EMI emissions. Cypress Semiconductor has made a design guideline and best practices document [59] for designing crystal circuits. Within the Ethernet PHY is a driver and feedback resistor, as well as internal capacitances. The crystal along with discrete capacitors are placed outside the chip. An illustration of this can be seen in Figure 24, which also includes parasitic capacitances.

On the X_{in} and X_{out} pins, the equivalent load capacitances, including parasitics, as

seen in Figure 24 are

$$\begin{aligned} C_{eq,1} &= C_{int,1} + C_{ext,1} + C_{trace,1} \\ C_{eq,2} &= C_{int,2} + C_{ext,2} + C_{trace,2} \end{aligned} \quad (34.1)$$

Here, C_{int} is pin and internal capacitances for the IC, C_{trace} is routing capacitance, while the two C_{ext} are discrete capacitors. The load capacitance of the circuit surrounding the crystal can be calculated as

$$C_L = \frac{C_{eq,1} \cdot C_{eq,2}}{C_{eq,1} + C_{eq,2}} + C_{parasitic} \quad (34.2)$$

where $C_{parasitic}$ is the parasitic capacitance of the crystal. This load capacitance must match the specified load capacitance of the crystal for it to oscillate at its nominal frequency. A higher load capacitance will cause the crystal to oscillate faster than specified, and a lower load capacitance will cause the crystal to oscillate slower than specified.

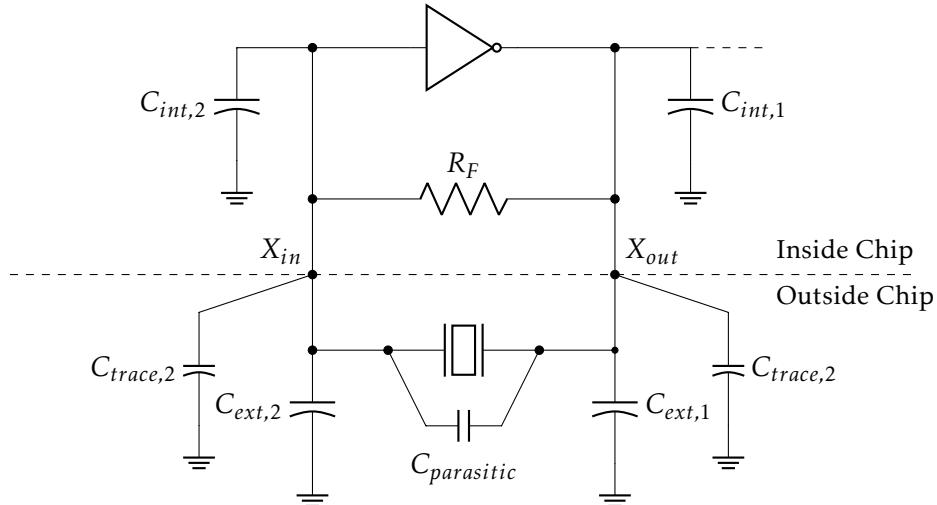
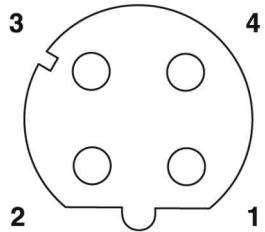


Figure 24: Circuit diagram of crystal circuit including equivalent internal circuit and parasitic capacitances. $C_{trace,1}$, $C_{trace,2}$ and $C_{parasitic}$ are parasitic capacitances due to the traces connecting the components and mount pads.

The crystal's specified load capacitance is 18 pF, and the discrete load capacitors must be designed to match this value. Assuming an internal capacitance of 1 pF, an external trace capacitance of 2 pF, and a parasitic capacitance of 3 pF, both C_1 and C_2 must have a capacitance of 27 pF for a resulting load capacitance of 18 pF. These capacitors should have a low tolerance of $\pm 5\%$. Due to the very low ± 10 ppm tolerance of the crystal versus maximum requirement of ± 50 ppm for the PHY, a minor deviation in capacitance does not critically impact the frequency.

The signals between the PHY and Zynq must be series terminated with resistors to avoid reflections. A value of 33Ω is recommended in the hardware design checklist. The two differential Ethernet signal pairs are connected to the magnetics component 7490100111A [60]. The circular connector to be used is the Phoenix Contact 1432457 [61], which is

M12, 4-pin, D-coded, and angled. Aside from being cheaper than an 8-pin connector, an additional benefit is also ensuring that connectors cannot be switched around, hindering communication and potentially damaging equipment. The D-coded connector is also used on the X90, for which reason cables can be re-used. The M12 connector's pins are shown in Figure 25. The 4-pin M12 connector does have an industry standard for Ethernet, which is shown in Table 23.



Pin	Signal
1	Tx+
2	Rx+
3	Tx-
4	Rx-

Figure 25: Pinout diagram of 4-pin M12

Table 23: Signals for 4-pin M12

Bob Smith termination is placed by the connector. The KiCad schematic of the magnetics, termination, and circular connector is shown in Figure 26

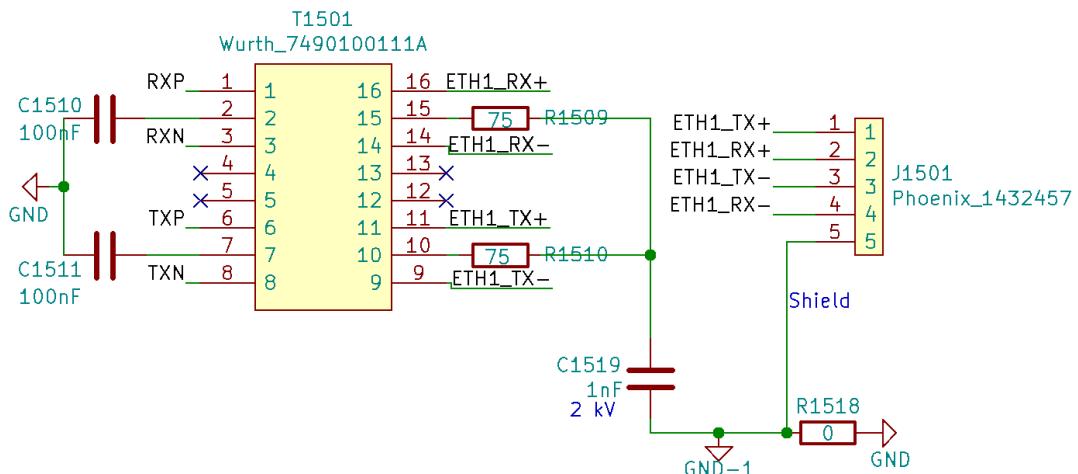


Figure 26: KiCad schematic of driverless Ethernet magnetics, Bob Smith termination, and connections to M12 connector

35 Data Storage

To utilize the board space as well as possible, a microSD card is chosen for data storage. A common push-pull connector would need to be placed at the board edge, which is not a guaranteed possibility and would require longer routing. Instead, the microSD hinge connector 47219-2001 [62] has been chosen.

For filtering and ESD protection the EMIF06-MSD02N16 [63], which is designed for microSD filtering up to 52 MHz, has been chosen. The IC allows electrical card detection. Write protect is not supported by microSD.

Due to the in-rush current when the SD card is connected, a voltage drop may be

experienced on the 3.3 V supply, potentially causing a system reset. A common 100 nF will not mitigate this issue, as it cannot supply the full current. Instead a larger capacitor with capacitance 22 μ F is placed close to the supply pin.

36 Configuration Parameter Storage

The configuration parameter storage device chosen in this project is the CY14B256PA, a 256-Kbit nvSRAM from Cypress Semiconductor with integrated Real-Time Clock (RTC) [64]. The nvSRAM communicates serially with the Zynq over SPI. The nvSRAM has a minimum data retention of 20 years, which is much longer than the Master Controller is expected to be in operation.

The nvSRAM contains both 256-Kbit of SRAM and 256-Kbit of nvSRAM. During operation, data is written to and read from the SRAM portion. When powering off the Master Controller, the nvSRAM detects the diminishing supply voltage and begins storing the data written in the SRAM to the nvSRAM. This operation is powered by a capacitor placed on the V_{CAP} pin. During power-on, this capacitor is charged by the supply, so that it is ready to supply the necessary current for an AutoStore during power-off. The data in the nvSRAM is automatically recalled during power-on.

A desirable feature of the nvSRAM is the RTC driven by an external crystal oscillator. The RTC keeps track of time, with an error of +2.5/-5 seconds per month [64, p. 23]. The RTC requires connecting a 32.768 kHz RTC crystal oscillator to the X_{in} and X_{out} pins.

To keep the RTC running even when power is off, a backup supply circuit must be added to the design. The datasheet recommends either a coin-cell battery or a capacitor. The advantage of using a capacitor is that the nvSRAM chip will charge the capacitor when powered. The disadvantage is the short backup time. The datasheet provides reference values for capacitor sizes and backup time, e.g. a 1 F capacitor can last around 25 days. In contrast to the capacitor, coin-cell batteries can usually provide a small current for months or years. As 25 days backup time is considered too short, since the Master Controller can be expected to be left unpowered for more than a month at a time, a coin-cell battery is used.

36.1 Choice of Storage Capacitor

An application note [65] made by Cypress Semiconductor describes the considerations the designer must make when choosing a storage capacitor. The storage capacitor for the CY14B256PA must have a capacitance between 42 μ F and 180 μ F, to ensure that the capacitor is able to deliver enough current to store the data in the nvSRAM and that the capacitor can be fully charged during power-on. Recommended capacitors are of the type Niobium Oxide, Tantalum, Polymer Aluminium or MLCC, with capacitance 47 μ F and a tolerance of 10%. The application note makes several recommendations of capacitors based on the typical VCAP capacitance, of which the NOJC686M010SWJ [66] was chosen.

This capacitor has a slightly higher capacitance than the typical to account for the higher tolerance, namely 68 μF and 20% tolerance. The voltage rating of the capacitor is 10 V.

36.2 RTC Oscillator Design

As mentioned above, the RTC integrated in the nvSRAM requires an external 32.768 kHz crystal. Using the same approach as in Section 34, the shunt capacitors can be found.

The chosen crystal oscillator is the Fox FK161EIHM0.032768 [67], which has a load capacitance of 12.5 pF and is described in Table 24.

Typical values for the externally placed capacitors are $C_1 = 12 \text{ pF}$ and $C_2 = 68 \text{ pF}$. These capacitors must have a very low tolerance, namely $\pm 5\%$. The values allow for a little parasitic capacitance to reach the specified load capacitance. These two components are also shown in Table 24.

Component	Manufacturer & Part No.	Description
C1	Common	12 pF capacitor, $\pm 5\%$ tolerance
C2	Common	68 pF capacitor, $\pm 5\%$ tolerance
X	Fox FK161EIHM0.032768	32.768 kHz, 12.5 pF load capacitance, $\pm 20 \text{ ppm}$ tolerance, -0.04 ppm frequency stability, $90 \text{ k}\Omega$ ESR, 0.1 μF drive level

Table 24: Crystal and capacitors chosen for the RTC oscillator circuit.

36.3 RTC Backup Design

The backup voltage for the nvSRAM must be between 1.8 V and 3.6 V. 3 V coin-cell batteries have a nominal voltage of 3 V, a maximum voltage of 3.4 V and a cut-off voltage of 2.5 V. Either a rechargeable or non-rechargeable battery can be used. Non-rechargeable coin-cell batteries, such as the CR2032, usually have capacities of above 200 mAh, while rechargeable batteries of the same size usually have capacities of around 20-30 mAh.

As stated in the nvSRAM datasheet, the RTC backup current is typically 450 nA [64, p. 35]. Rechargeable batteries usually have a self-discharge rate of below 2% of its full capacity per year, which for a 20 mAh battery is

$$i_{self-discharge} = 2\% \cdot \frac{20 \text{ mAh}}{365.25 \frac{\text{days}}{\text{year}} \cdot 24 \frac{\text{hrs}}{\text{day}}} = 45.6 \text{ nA}$$

With a self-discharge rate of 45.6 nA and a RTC backup current of 450 nA, a 20 mAh rechargeable battery can last

$$t = \frac{20 \text{ mAh}}{495.6 \text{ nA}} = 40353 \text{ hrs} = 1681.4 \text{ days} = 4.6 \text{ yrs}$$

The battery will therefore be able to last 4.6 years without recharge, which is much more

than required. In comparison, a non-rechargeable, 220 mAh battery with the same self-discharge rate will be able to last

$$t = \frac{220 \text{ mAh}}{951.9 \text{ nA}} = 231.1 \cdot 10^3 \text{ hrs} = 9629.5 \text{ days} = 26.4 \text{ yrs}$$

The rechargeable battery found is the VL-2020/HFN [68, p. 71], which has the same diameter, and therefore footprint, as a CR2032 coin cell battery.

To be able to use both a rechargeable or non-rechargeable battery, a charging circuit is designed for the VL-2020 battery. When charging coin-cell batteries, constant voltage charging must be used. Trickle charging, where a current equal to the discharge rate of the battery is supplied constantly, is not allowed. Inspired by the charge circuits in Panasonic's Lithium Technical Handbook [68, p. 69] a charging circuit is designed as shown in Figure 27. The maximum charge current should be 1.5 mA, and the charge voltage should be 3.4 V. The $0\ \Omega$ resistor allows the charge circuit to be disconnected. The voltage divider from the 5 V source ensures a voltage of ~ 3.6 V on the Schottky diode anode. The chosen Schottky diode has a 0.3 V voltage drop across it at 1.5 mA forward current, which is the maximum charge current for the battery. When the battery voltage is above 3.3 V, the Schottky diode will stop conducting and the charging will be stopped. The Schottky diode used in this design is the RB500VM-40TE-17 [69].

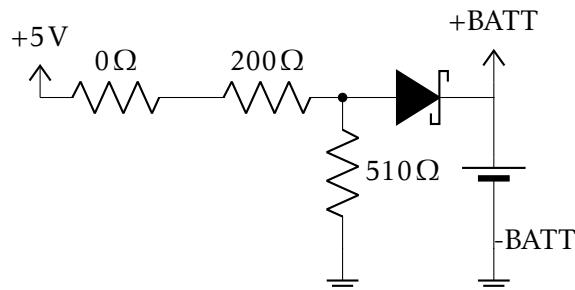


Figure 27: Charging circuit for rechargeable coin cell battery backup for RTC

36.4 PCB Design Considerations

Care must be taken when routing the signals for the RTC Oscillator circuit. A few guidelines recommended by the nvSRAM application note [59, p. 12] is that the crystal must be placed as close to the X_{in} and X_{out} pins as possible, with equal length traces of width less than 0.2 mm. A guard ring should be placed around the crystal oscillator circuitry, and other high-speed signals should be kept at a distance from the RTC traces. An isolated ground plane should be placed beneath the oscillator circuit that should be connected to the board ground through the guard ring [59, p. 12].

37 Inertial Navigation System

An IC must be implemented to translate the RS-232 voltage levels to Zynq-compatible 3.3 V. The component chosen for this is the SN65C3221 transceiver [70], which also implements ESD protection. The component is able to transmit at data rates up to 1 Mbit/s, similar to the VN-200, meaning it will not bottleneck the connection.

The surrounding circuits are designed from the application information in the datasheet. The voltages are translated using Schmitt triggers within the IC, which act as a filter of the signal lines going into the PCB, reducing general noise. The SYNC_OUT and GPS_PPS signals have ESD diodes placed by the connector and are low-pass filtered with an RC circuit.

38 Internal Power Supplies

In Section 18, the need for 5 V, 3.3 V and 12 V power supplies was outlined.

As a 12 V supply is also needed, a Buck-Boost converter would be required for converting from the LVS. Buck-Boost topologies typically require larger components, due to increased stress and higher voltage and current ratings, for which reason it is decided that the 5 V supply will be boosted to 12 V through a low-power Boost converter.

The LVS used as input to the DC-DC converters is first filtered through a common-mode choke to prevent common-mode signals induced on the LVS lines to enter the system. As described in Section 18, the common-mode choke is chosen based on having a wide common-mode impedance curve and as little differential impedance as possible. Furthermore, the common-mode choke should be rated for at least 4 A to power the Master Controller. The common-mode choke used to filter the LVS is the 74429056 [71] by Würth Elektronik. This has a DC impedance of 4.7 mΩ, an inductance of 56 mH, and is rated for currents up to 7 A.

38.1 LV-to-5V Buck Converter

The LV-to-5V converter will be supplying the PicoZed and multiple other components. In Table 25 a worst-case estimate of the power requirements for the 5 V supply is shown. As is seen in the table, the worst-case power usage of the 5 V supply is 24.34 W, including inefficiencies and safety margins. A 25 W converter would therefore be fitting.

From prior experience, it has been found that Würth Elektronik makes efficient and small DC-DC Converters for stepping down from voltages in the LVS range. In the Würth MagI³C Power Modules catalog, the Würth 171050601 [72] from the Variable Step Down Regulator Module (VDRM) series is found. This Buck converter takes inputs in the range 6-36 V and outputs an adjustable voltage in the range 0.8-6 V with a maximum load current of 5 A, i.e. for a 5 V output it has a maximum output power of 25 W.

5 V Supply	Amperage	Power
PicoZed	2 A	10 W
Expansion Board	200 mA	1 W
Brake Pedal	20 mA	0.1 W
Torque Pedal	≈ 0 A	0 W
INS	250 mA	1.25 W
Sallen-Key	10 mA	0.05 W
LVS Distribution	60 mA	0.3 W
12 V Supply	1 A	5 W
Inefficiencies	-	10%
Safety Margin	-	25%
Total	4.87 A	24.34 W

Table 25: Worst-case estimate of 5 V supply's power usage including overhead

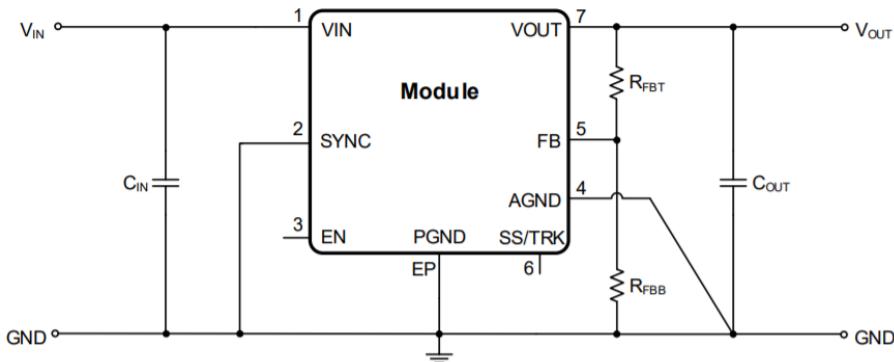


Figure 28: Typical Circuit Diagram for Würth 171050601 DC-DC converter. Taken from datasheet [72, p. 1]

Following the design flow section of the 171050601 [72, p. 18] datasheet, feedback resistors, input and output capacitors as well as soft-start capacitor can be determined. The buck converter has an internal error amplifier used to regulate the output voltage with a reference voltage of 0.796 V. The voltage on the FB pin must also be 0.796 V, when the output voltage is 5 V. This is achieved with a voltage divider, as seen in Figure 28. The ratio between R_{FBT} and R_{FBB} is determined by

$$\frac{R_{FBT}}{R_{FBB}} = \frac{V_{out}}{V_{FB}} - 1 \quad (38.1)$$

With $V_{out} = 5\text{V}$ and $V_{FB} = 0.796\text{V}$ the resistor ratio is

$$\frac{R_{FBT}}{R_{FBB}} = \frac{5\text{V}}{0.796\text{V}} - 1 = 5.2814$$

A MATLAB function has been written which takes the resistor E-series used and the resistor ratio as input and generates voltage divider resistor values from the given E-series that has the closest match to the inputted resistor ratio. As the resistor values should be in the range of 1-20 kΩ, the resistor values are $R_{FBT} = 11.3\text{k}\Omega$ and $R_{FBB} = 2.15\text{k}\Omega$.

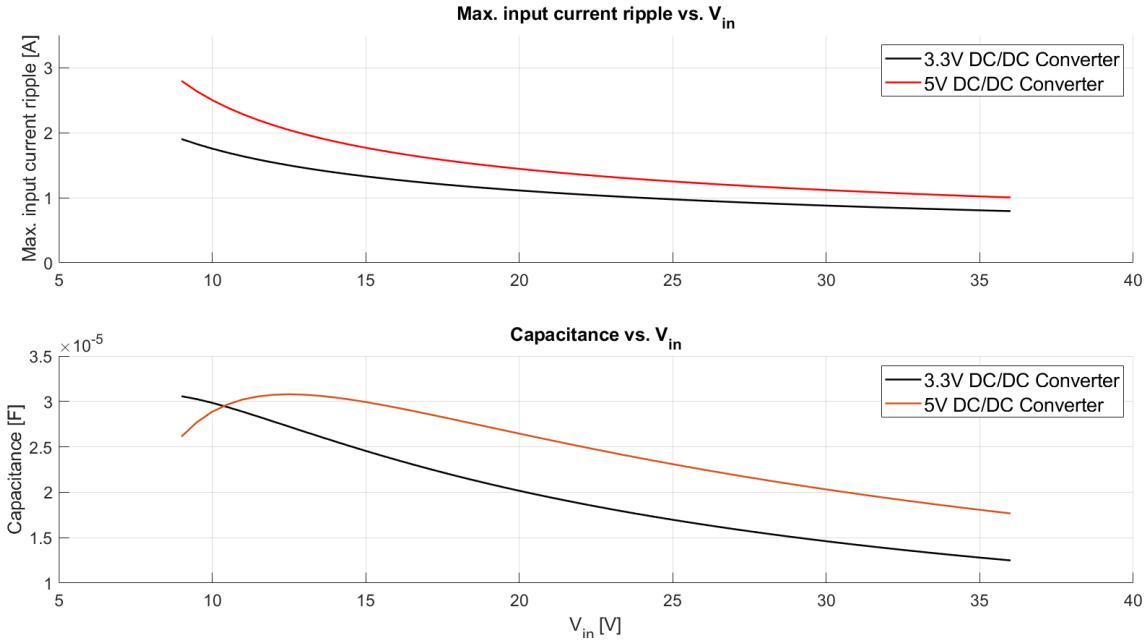


Figure 29: Parameters relevant in choosing input capacitor. The red curves are used in the design of the 5 V buck converter, and the black curves are used in the design of the 3.3 V buck converter. Upper graph shows the maximum input current ripple as a function of input voltages. The lower graph shows the minimum required capacitance as a function of input voltages.

The input capacitor is determined from the worst-case input current and voltage ripples. The capacitor must be able to handle the worst-case input current ripple, which is determined by

$$I_{C_{in,RMS}} \approx \frac{1}{2} \cdot I_{out} \cdot \sqrt{\frac{D}{1-D}}, \quad \text{where } D \approx \frac{V_{out}}{V_{in}} \quad (38.2)$$

Given the input voltage range of 9-36 V and output voltage of 5 V, the input current ripple is plotted against the input voltage in the upper graph of Figure 29. As seen the maximum input current ripple is found when $V_{in} = 9$ V, where the current ripple is $I_{C_{in,RMS}} = 2.8$ A.

Using the minimum value of the peak-to-peak input voltage ripple $V_{in,ripple}$, the minimum value of input capacitance can be determined by the equation

$$C_{in} \geq \frac{I_{out} \cdot D \cdot (1-D)}{f_{sw} \cdot (V_{IN,ripple} - ESR \cdot I_{out} \cdot D)}, \quad \text{where } D = \frac{V_{out}}{V_{in} \cdot \eta} \quad (38.3)$$

With a maximum I_{out} of 5 A, a switch frequency of $f_{sw} = 812$ kHz, assuming a minimum input voltage ripple of $V_{in,ripple} = 0.05$ V_{p-p}, a very small ESR and a worst-case efficiency $\eta = 0.8$, a plot of the minimum required capacitance against the input voltage is presented in the lower graph of Figure 29. The minimum required capacitance is found at the maximum of the graph at 30.8 μF. The input capacitor must be able to handle a current ripple of 2.8 A, and have a minimum capacitance of 30.8 μF.

To handle the large current ripple, a 63 V, 39 μF Aluminium Polymer [73] capacitor

able to handle a maximum current ripple of 3.5 A is chosen in parallel with a 680 nF MLCC X7R [74] capacitor that can handle the higher frequency ripples and transients. Additionally, a 10 A ferrite bead is placed for EMC filtering.

The minimum recommended output capacitance is 200 μ F. To be on the safe side, a 16 V, 220 μ F Aluminium Polymer [75] capacitor is placed in parallel with two 22 μ F, MLCC X5R [76] capacitors, as is also recommended by the DC-DC converter's datasheet [72, p. 24].

The soft-start capacitor is chosen based on the desired soft-start time from the equation [72, p. 26]

$$C_{SS} = t_{SS} \cdot \frac{50 \mu\text{A}}{0.796 \text{V}} \quad (38.4)$$

For a recommended soft-start time of $t_{SS} = 7.5 \text{ ms}$, $C_{SS} = 470 \text{ nF}$ is chosen.

The enable pin of the 171050601 is left unconnected, as recommended by the datasheet when the converter should always be running.

38.2 LV-to-3.3V Buck Converter

The worst-case power requirements of the 3.3 V supply is seen in Table 26. To future-proof the Master Controller, the 171050601 Würth Elektronik Buck Converter is also used here. At 3.3 V output voltage, the maximum output power is 16.5 W.

3.3 V Supply	Amperage	Power
PicoZed	500 mA	1.66 W
Expansion Board	300 mA	1.00 W
Bluetooth	20 mA	0.06 W
CAN	200 mA	0.66 W
Driverless Ethernet PHY	100 mA	0.33 W
LEDs	50 mA	0.17 W
JTAG Interface	200 mA	0.66 W
NVSRAM	3.3 mA	0.01 W
SD Card	400 mA	1.33 W
Inefficiencies	-	10%
Safety Margin	-	25%
Total	2.45 A	8.10 W

Table 26: Worst-case estimate of 3.3 V supply's power usage including overhead

Following the same design flow as above, $R_{FBT}/R_{FBB} = 3.1457$, which gives $R_{FBT} = 10.7 \text{ k}\Omega$ and $R_{FBB} = 3.4 \text{ k}\Omega$. As seen in Figure 29, the maximum input current ripple is $I_{C_{in,RMS}} = 1.9 \text{ A}$ at $V_{in} = 9 \text{ V}$ and the minimum required capacitance is 30.6 μF found at $V_{in} = 9 \text{ V}$. Because of the similarities with the LV-to-5V Buck Converter, the LV-to-3.3V Converter is designed with identical input capacitors [73][74], output capacitors [75][76] and soft-start capacitor. The enable pin of the converter is connected to the *VCCIO_EN* signal from the PicoZed that indicates that the I/O bank supplies can be brought online [1, p. 31].

38.3 5V-to-12V Boost Converter

As the 12 V supply will only be used to supply the sensors, it does not need to supply a large current. Therefore, a low power Boost regulator with integrated switch is used, namely the MCP1663 [77]. This Boost regulator requires designing the Boost converter around the regulator. The full Boost converter circuit is shown in Figure 30.

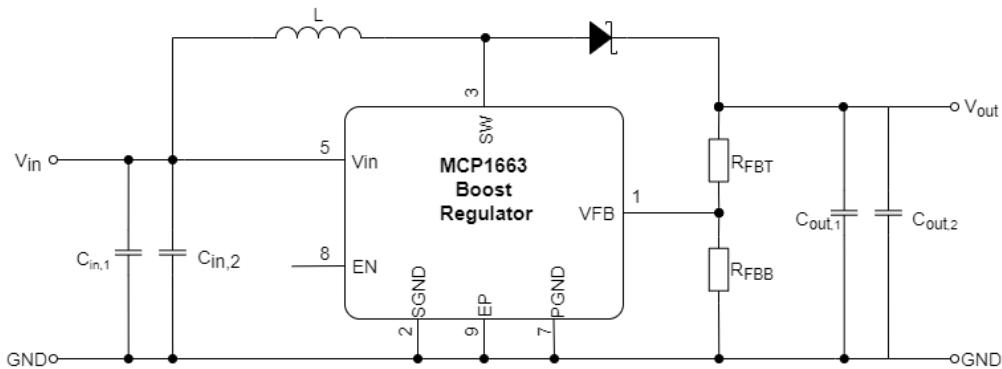


Figure 30: Implemented 5V-in-12V-out Boost Converter.

As was the case for the LV-to-5V and LV-to-3.3V, a voltage divider is used to determine the output voltage. The reference voltage for the error amplifier is 1.227 V. To generate an output voltage of 12 V, the resistor ratio must be:

$$\frac{R_{FBT}}{R_{FBB}} = \frac{12 \text{ V}}{1.227 \text{ V}} - 1 = 8.78 \quad (38.5)$$

Recommended resistor values for the MCP1663 Boost regulator are between 100 kΩ and 1 MΩ. A resistor ratio of 8.78 gives the feedback resistors, $R_{FBT} = 1.65 \text{ M}\Omega$ and $R_{FBB} = 187 \text{ k}\Omega$. As the datasheet recommends [77, p. 16], the input capacitor should be above 4.7 μF. Two parallel 10 μF X7R MLCC capacitors [78] are used to sustain high currents and high temperatures. A 4 A ferrite bead is placed for EMC. The MLCC X7R capacitors are recommended for use as output capacitors for their low ESR. The recommended minimum output capacitance is 10 μF. Therefore, two parallel 10 μF MLCC X7R capacitors are placed between the output and ground to further reduce the ESR in the capacitors. The same type of capacitors are used on the output filter as on the input filter.

The datasheet recommends an inductance of 4.7 μH for below 15 V output voltages. The chosen inductor is a 4.7 μH Würth 74404042047 WE-LQS inductor with a saturation current of 2.2 A and a DC resistance of 70 mΩ. The rectifying diode used in the Boost converter is a Schottky diode to reduce losses. The datasheet recommends a few Schottky diodes based on the output voltage. For 12 V output, the MBRM120 [79] Schottky diode is used. At 1 A forward current it offers a 0.35 V forward voltage at room temperature. The Boost regulator is used in its TFDN-6 package, as it offers a much lower thermal resistance, namely $\theta_{JA} = 52.5 \text{ }^{\circ}\text{C/W}$ compared to the SOT-23 package which has almost the quadrupled thermal resistance, $\theta_{JA} = 201.0 \text{ }^{\circ}\text{C/W}$.

39 PCB Design

With all subcircuits designed, the final components can be picked, and a PCB designed.

39.1 Connector

With the connection requirement given in Subsection 25.2, a Molex CMC connector can be chosen. The one to be used is the 3-pocket 64333-0100 [80], with a total of 112 pins and mixed colour-coding. The pins are distributed as 32 pins on two connectors and 48 pins on the last. The connectors contain pins of mixed sizes, with maximum currents of either 6 A or 12 A. A full overview of the CMC connections is found in Appendix M.

39.2 Pre-Fusing

The fuses placed on the PCB are the Littelfuse NANO2 157 SMD fuses [81] and the Littelfuse Mini blade fuses [82]. The former are small, fast-acting, and available in variants up to 10 A. Due to the clip mounting design, they can be replaced with relative ease. The blade fuses are much larger, but are available with a current rating up to 30 A. They are very common and can be bought in regular stores, and are easier to replace.

Section EV 3.2 of the Formula Student rules specifies overcurrent protection for all PCBs. EV 3.2.2 specifies the current ratings of the fuses: "The continuous current rating of the overcurrent protection must not be greater than the continuous current rating of any [conductor] that it protects. I.e. if multiple pins of a connector are used to carry currents in parallel, each pin must be appropriately protected" [4, p. 73].

That is, if a wire is used that could potentially short to ground, the fuse must blow before the wire reaches critical temperature levels. This means that most external wires from the PCB must be fused. To save space, blade fuses have only been used for protection of other electronic nodes and the Shutdown Circuit, as they are at the highest risk of blowing. NANO2 fuses have been used for the remaining signals like sensors, DC-converter inputs, and low-current actuators. The PROFETs are an additional layer of overcurrent protection, as they will instantly deactivate when short-circuit currents are measured. When currents are higher than the FETs' ratings, the temperature of the FET steadily increases until the overtemperature protection activates. Tests showing this behaviour are seen in Appendix C. In this way, PROFETs reliably act as resettable fuses.

39.3 Mechanical

The PCB is designed with a restriction to the dimensions, as it must fit in an enclosure. The team has previously used Fibox enclosures, for which reason the MNX-series enclosure with outer dimensions 255 mm x 180 mm x 63 mm [83] is chosen. A large drill hole is placed near the middle of the PCB for placing a support rod. This will ensure that neither the enclosure nor the PCB is damaged should it be stepped on.

39.4 EMC and High-Frequency Design

A 4-layer PCB is used, with layer 2 and 3 being ground and supply layers respectively. The ground layer ensures a shorter signal return path, reducing emitted EMI. In general, current loop lengths are minimized for high-frequency and power switching routes. Critical tracks, such as high-frequency signals, must be routed above ground planes. If there are slots in the ground plane, the critical tracks should be rerouted so that it runs over the ground plane [84, p. 76].

When routing the high-frequency signals on the PCB, the trace widths are chosen with specific target impedances in mind to minimize reflections. These have been chosen in accordance with the PicoZed Carrier Design Guide [21, p. 19]. The impedances are calculated with the KiCad PCB Calculator, and are shown in Table 27. The table also shows the difference in length between the longest and shortest traces, which is minimized to avoid phase-shifting of the high-frequency data. Series termination resistors are placed near the transmitting device to minimize the distance reflections must travel.

Signal	Impedance	Width	Gap	Length difference
Antenna	50 Ω	0.37 mm	-	-
Ethernet 0 (differential)	100 Ω	0.30 mm	0.23 mm	±3 mm
Ethernet 1	50 Ω	0.37 mm	-	±6 mm
Ethernet 1 (differential)	100 Ω	0.25 mm	0.15 mm	±5 mm
SDIO	50 Ω	0.37 mm	-	±2 mm
USB (differential)	90 Ω	0.30 mm	0.35 mm	±2 mm

Table 27: Overview of target impedances and dimensions for high-frequency signals

The circular connectors used for Ethernet have dedicated shield ground planes under them, which can be connected to signal ground through a $0\ \Omega$ resistor, while ground has been removed entirely under the magnetics as described in [12]. Furthermore, a $1\ \mu\text{F}$ bypass capacitor is placed near the M12 Power-over-Ethernet connector to ensure that the long supply line from the lower right corner to the upper left corner along the PCB edge will not induce noise on the PCB.

Crystal oscillator circuits on the PCB have been encircled by a guard ring and protected from external signals according to the guidelines provided by Cypress Semiconductor [59, p. 12]

A 2.4 GHz inverted-F microstrip antenna for Bluetooth, as designed by Texas Instruments and documented in [85], is placed by the edge of the PCB. Copper on all layers is pulled back from the antenna to ensure optimal performance.

When the relays of the Shutdown Circuit switch, a spike current of up to 4 A has been experienced in the Shutdown Circuit wires. To avoid critical voltage drops on the PCB, short and wide tracks have been used.

A full list of all JX header connections and signal names is found in Appendix L and a 3D rendering of the top of the Master Controller PCB can be seen in Figure 31.

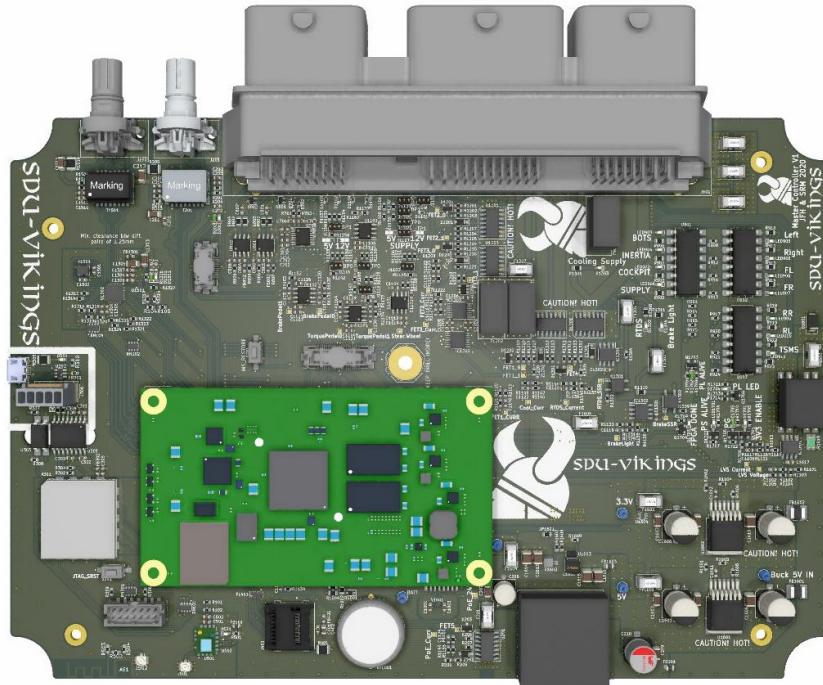


Figure 31: KiCad 3D rendering of the Master Controller PCB

40 Expansion Board

The receptacles chosen for the expansion board are from the Molex SlimStack 52885 series [86]. The receptacles can mate with five kinds of plugs, resulting in a mated height between 6 mm and 10 mm, leaving enough space below the board to place components. The maximum voltage rating is 100 V, while the current rating per pin is 0.5 A, as specified in the datasheet.

Due to the low maximum current, to reduce resistance and noise, and to increase flexibility, multiple pins are used to supply the voltages and provide ground.

For stability of the expansion board, two receptacles are used. A 20 pin and a 40 pin receptacle is chosen, and they are placed askew. This way, the orientation of the expansion board is obvious, and it cannot be connected incorrectly.

Four differential pairs between the Zynq and expansion receptacles are routed with a $100\ \Omega$ differential impedance. One of these pairs is routed to the Zynq XADC pins for auxiliary input 14, providing design flexibility. The connections for the CMC connector have been routed with different widths depending on the associated CMC pin. An overview of both Zynq and CMC connections used for the Expansion Board can be found in Appendix N.

40.1 ADC Expansion

An example of an expansion board implements an external ADC for converting cooling system and auxiliary sensor voltages and communicating results to the Zynq.

The ADC chosen for the ADC Expansion PCB is the MCP3208-CI [87]. This ADC has eight conversion channels, converts up to 100 kS/s with a 12-bit accuracy, and communicates with SPI. The ADC can convert the channels as single-ended, or as pseudo-differential pairs. It is supplied with 5 V, thus allowing conversion of voltages up to 5 V. Summing the inaccuracies gives a maximum ADC inaccuracy of ± 11 LSB, though they are more likely to partially cancel out each other and are typically lower.

The cooling system temperature sensor will, as specified in Section 15, be the Bosch NTC M12 thermistor [18]. This thermistor must have a series resistor with a size of 6.98 k Ω , as detailed in the tests in Appendix E. This resistor will limit the measurement current and thus heating of the NTC during use, improving accuracy. Appendix E also shows multiple equations for the temperature as function of ADC voltage, with varying accuracy and processing complexity. The most accurate equations are Equation 40.1, used at or below 30 °C, and Equation 40.2, used above 30 °C.

$$T_C = -35 + 6.11 \cdot V_{in} + 2.46 \cdot V_{in}^2 \quad (40.1)$$

$$T_C = -29104 + 19644 \cdot V_{in} - 4424 \cdot V_{in}^2 + 333 \cdot V_{in}^3 \quad (40.2)$$

Where T_C is the measured temperature, and V_{in} is the converted voltage. As shown in the appendix, the maximum temperature deviation due to all inaccuracies is low when below 60 °C, but peaks at 8.5 °C when the measurement is around 90 °C.

ESD diodes with 5 V working voltage are placed by the sensor signal connector. All sensor voltages can be converted directly in the ADC, however they must first be filtered by a second-order Sallen-Key filter and subsequent RC filter identical to the one designed in Section 30. The SlimStack receptacles' matching plugs with a mated height of 10 mm, the 53627 series, are chosen for connecting to the Master Controller PCB. The SPI signals are connected to Zynq pin pairs Exp_1P/1N and Exp_4P/4N on header JX2, which all have the same length, for optimal performance even at high frequencies. The sensor supplies and grounds are connected to the CMC with wide PCB traces.

A KiCad 3D rendering of the top of the PCB designed for the ADC expansion is shown in Figure 32.

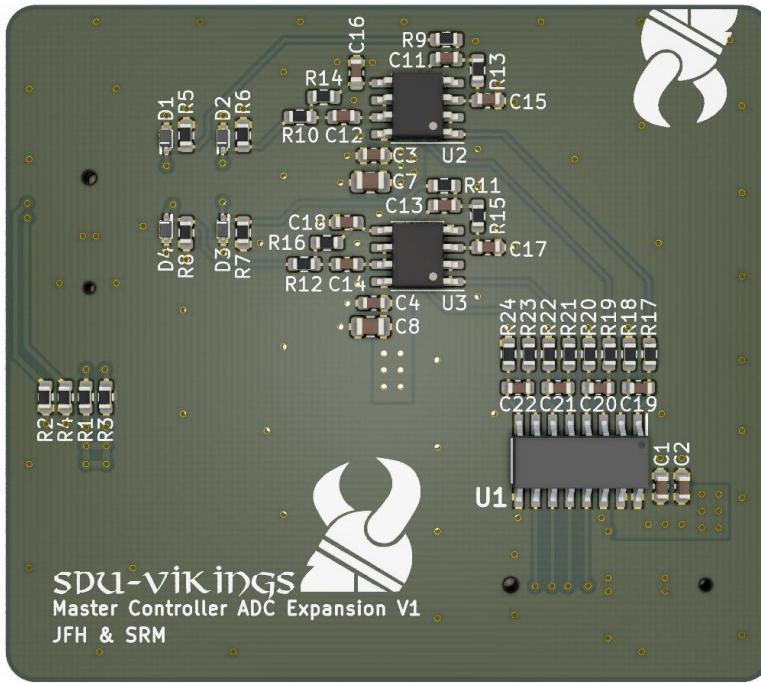


Figure 32: KiCad 3D rendering of the ADC Expansion PCB top

41 Power Dissipation

The Master Controller PCB will be placed in a confined space with no airflow. For this reason, the power consumption and thus produced heat are of great interest to ensure that no components are at risk of critical derating or damage. The consumption will vary depending on the input voltage, as the used DC-converters have varying efficiencies across their input ranges. A higher input voltage will also result in lower currents both into the converters and PROFETs.

From the results of the calculations in the MATLAB script `PowerConsumption.m`, Table 28 is created. These calculations are made from efficiency data from the converter datasheets, and estimations of 12 V and 24 V currents. The values used are not worst-case, but rather the expected actual currents and thus expected power.

The MATLAB script also calculates the time required for a 30 °C heating of a 24.6 cm x 17.1 cm x 5.7 cm case in common weather conditions and with no heat convection. 30 °C heating was chosen as, in a 30 °C ambient environment, this is the critical temperature for the most heat-sensitive components. The time required for this heating is 77.4 minutes and 76.4 minutes for 12 V and 24 V respectively, which is longer than the Master Controller is expected to be powered.

Using the thermal resistances listed in the component datasheets, the resulting temperature increases for each component can also be found. For the PROFETs, these are limited to below 20 °C, while they are up to 32 °C for the 3.3 V and 5 V converters. This is not an issue, especially if heat on the PCB is spread evenly with large planes and relief vias.

Component	12 V Dissipation	24 V Dissipation
3.3 V Converter	0.57 W	1.02 W
5 V Converter	1.13 W	1.75 W
12 V Converter	0.06 W	0.06 W
24 V Converter	0.80 W	0.80 W
CAN	0.13 W	0.13 W
Fuses	2.09 W	1.07 W
Ethernet	0.20 W	0.20 W
Expansion Board	1.50 W	1.50 W
LEDs	0.37 W	0.55 W
NVSRAM	0.01 W	0.01 W
Operational Amplifiers	0.25 W	0.25 W
Optocouplers	0.64 W	1.27 W
PicoZed	8.00 W	8.00 W
Power Measurements	0.15 W	0.15 W
PROFETs	1.89 W	1.56 W
SD Card	0.33 W	0.33 W
Shunt Resistors	0.40 W	0.20 W
Total	18.52 W	18.85 W

Table 28: Power dissipation calculations for 12 V and 24 V low-voltage systems

With the PicoZed's high power dissipation and the Zynq's junction-to-ambient thermal resistance of up to 19 °C/W, the temperature may become critical under heavy load. It is not possible to estimate the PicoZed's ability to spread the heat on the PCB, for which reason care should be taken. The Zynq is 17 mm by 17 mm, and the PicoZed is designed to allow passive heat sinks up to 20mm by 20mm. With this in mind, an adhesive heat sink can be chosen and placed on the Zynq to improve cooling. The APF19-19-10CB/A01, an adhesive 19 mm by 19 mm heat sink [88] is chosen for this.

42 Design Summary

Using the analysis results, components have been picked for all subcircuits that meet the set requirements for voltages, currents, and functionality.

M12 connectors have been picked for Ethernet, while a 112-pin CMC connector is used for the remaining signals. A Fibox enclosure of size 255 mm x 180 mm x 63 mm has been chosen for the PCB. Fuses have been placed in accordance with Formula Student rules. The PCB has been designed with attention to noise and high-frequency design. An ADC Expansion PCB has also been designed to extend the Master Controller's functionality. Using the datasheets to infer performance characteristics, power dissipation within the Fibox enclosure was calculated, confirming that heat will not impact performance.

Part IV

Hardware Testing

With the hardware design completed, it must be tested to confirm that the design can be used for controlling the car. For this, software must be written for each test. Zynq peripherals should be isolated during initial testing. When all peripherals work individually, larger projects can be created for testing multiple sections of hardware at once.

43 Test Specifications

For all tests, the Master Controller PCB will be powered by an EA-PSI 5200-10 A power supply with serial number 2855381026 outputting either 12 V or 24 V. Both voltages are used for test of hardware using it directly, while it remains unchanged when testing 5 V or 3.3 V components. The general test setup can be seen in Figure 33.

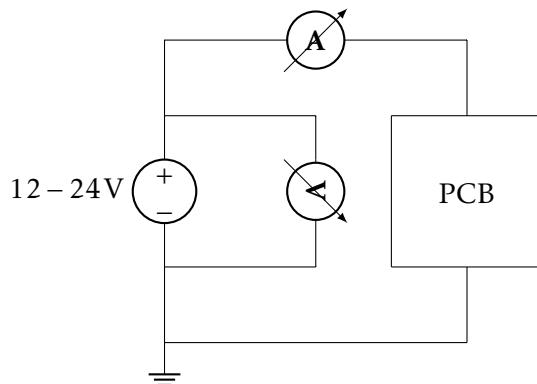


Figure 33: General test setup used for testing the Master Controller PCB

Measurements will be performed with an RTH1004 oscilloscope with serial number 103724. Initially, the voltages and crystals on the board must be measured to ensure that all values are as expected and can be used by the board.

The 3.3 V and 5 V converters' output must vary no more than $\pm 5\%$ from the nominal voltages. The 24 V converter should not be soldered before the Ethernet PHY has been tested. When soldered, its output may vary up to $\pm 10\%$. The oscillators must not measurably vary from their rated frequencies of 32.768 kHz and 25 MHz.

The following Zynq peripherals and the associated hardware on the Master Controller must be tested:

- CAN
- Ethernet
- SDIO
- SPI
- UART/JTAG
- XADC

For each of the tests, the Vivado and Vitis projects will be set up as described in Appendix F. Only the peripheral being tested, as well as UART for communication and the DDR memory, is enabled. If further modifications of the Vivado block diagram setup are required, they will be specified in the individual tests. The ports are connected to Zynq pins as listed in Appendix K and Appendix L.

After peripherals have been tested, further tests must be performed on the Master Controller PCB to ensure correct hardware functionality. This is completed by writing a test application in Vitis and both confirming the outcome in the PS and by measuring signals with an oscilloscope. The hardware to be tested is:

- Power distribution / actuator level shifts and switching capability
- Current measurement circuits
- Shutdown circuit optocouplers
- nvSRAM and the associated RTC
- Power-over-Ethernet
- ADC Expansion Board

The coming subsections will describe the approaches for completing the tests specified above. All test software can be found in the Master Controller Software repository on GitLab, and has been added to the ZIP file.

43.1 UART/JTAG

The first priority is UART, which cannot be tested without also testing the JTAG interface, as it allows easier debugging by sending data and status to the computer.

In the Vivado project, modem signals are enabled for UART0, but ports are only created for CTS and RTS as the remaining are unused. The Vivado block diagram is shown in Figure 34. In Vitis, an application that reads the input and writes it back is created using the Xilinx UART driver designed for the Zynq. This test should be repeated enough times to ensure that the FIFO does not fill at any point.

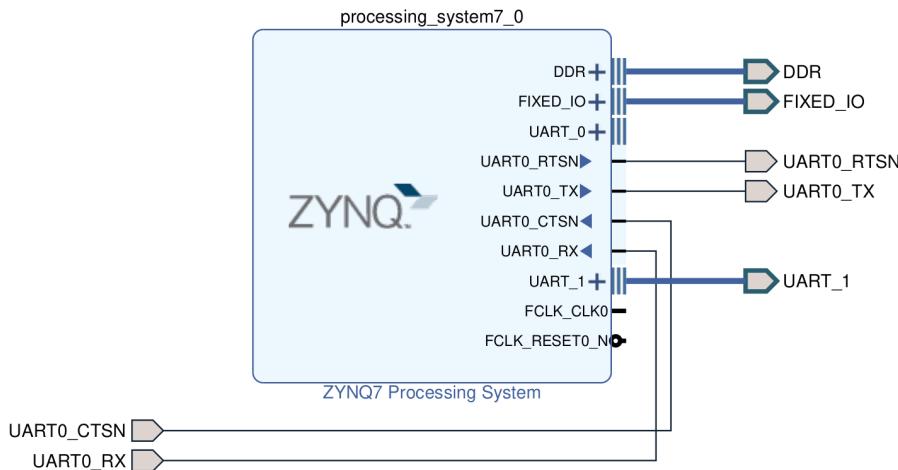


Figure 34: Vivado block diagram containing the Zynq7 Processing System and UART ports

This test is performed by connecting the micro-USB connector to a computer. The connection between the computer and the Master Controller is opened with the terminal program PuTTY, using a baud rate of 115200 bit/s. The Zynq is then programmed with Vitis over the same USB connector. The Zynq is then programmed to transmit a known sequence of bytes, which are verified in the serial terminal and with an oscilloscope. Both the JTAG and UART0 interfaces are thus tested, as they are implemented in the JTAG-SMT3-NC module. The isolation will inadvertently be tested as well. The UART1 transmit signal can be measured with an oscilloscope.

43.2 XADC

The XADC block in Vivado is configured to continuously convert the five XADC auxiliary input (AUX) channels connected to the CMC; channel 0, 1, 3, 8, and 9. The current measurement channels cannot be isolated in testing, and are thus left out of this test. The XADC block is connected through the standard AXI Master interface. This is shown in Figure 35.

The XADC test application in Vitis uses the Xilinx XADC driver for the Zynq. This is tested by applying a known signal to the CMC pins connected to XADC filters as shown in Figure 36.

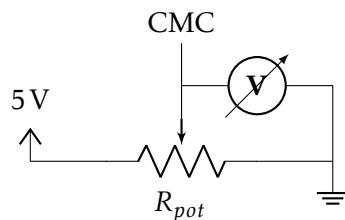


Figure 36: Circuit used for testing the XADC peripheral

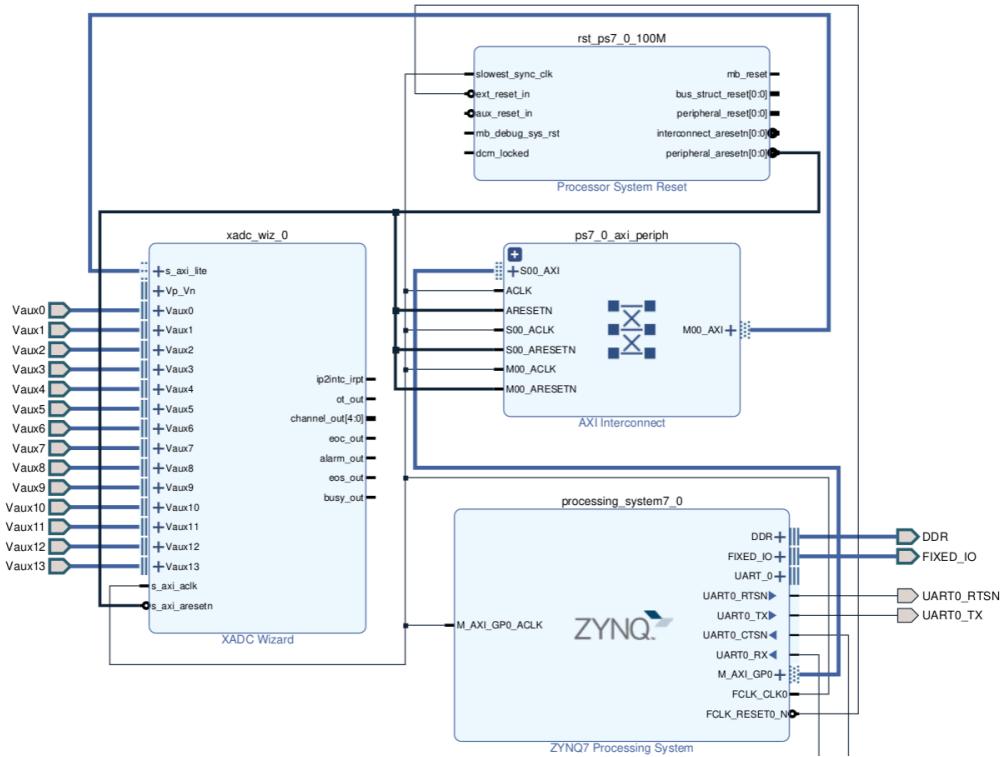


Figure 35: Vivado block diagram containing the Zynq7 Processing System, XADC IP, AXI interconnect, and auxiliary ports

The converted value is then transmitted over UART to the computer. It should be ensured that all the conversions are with expected accuracy. The maximum expected inaccuracy for channel 1 and 9, the torque pedals, is

$$V_{inacc} = \pm 1.71 \text{ mV} \pm 6.0 \text{ mV} \pm \left(5 \text{ V} \cdot \frac{1 \text{ k}\Omega \cdot 1.005}{1 \text{ k}\Omega \cdot 1.005 + 4.02 \text{ k}\Omega \cdot 0.995} - 1 \text{ V} \right) = \pm 11.7 \text{ mV} \quad (43.1)$$

due to XADC inaccuracy, the two op amps' imperfections, and tolerances. When converted in a 12-bit converter, this equates to a digital value of $\pm 11.7 \text{ mV} \cdot 2^{12} = \pm 48 \text{ LSB}$. For channels 0, 3, and 8 with one operational amplifier each, the digital inaccuracy value is $\pm 10.7 \text{ mV} \cdot 2^{12} = \pm 44 \text{ LSB}$.

These values are applicable for the entire 0-5 V range of the sensors.

43.3 SPI

In Vivado, the Slave Select input is connected to a Constant block with high output, as it is not needed. Ports are only created for the clock, MISO, MOSI and Slave Select 0 signals, as the remaining are not used. The block diagram is shown in Figure 37. The SPI clock frequency is set to 167 MHz, which is further divided by the Vitis software.

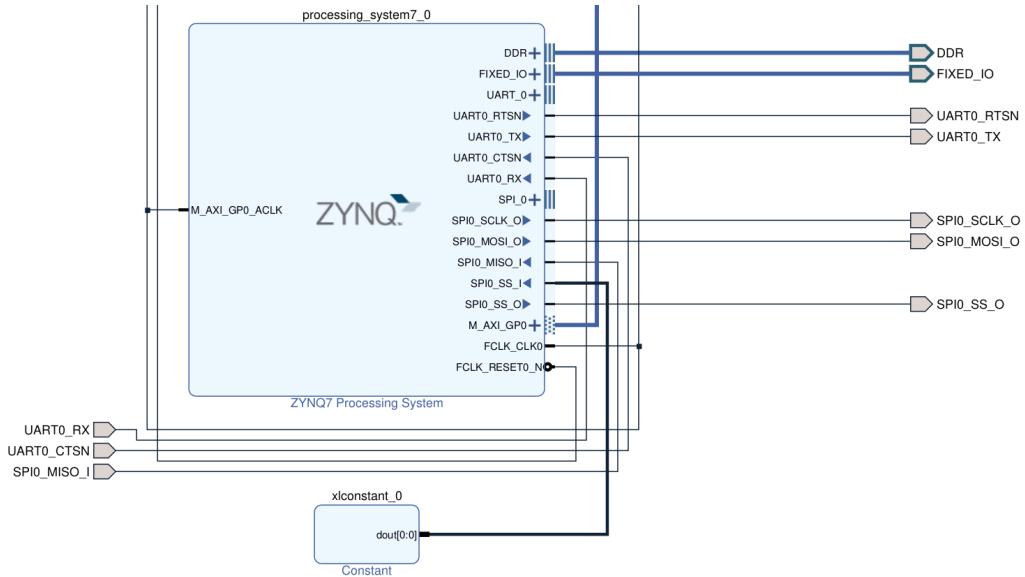


Figure 37: Vivado block diagram containing the Zynq7 Processing System, Constant, and SPI ports

A SPI test application is made using the Xilinx SPI drivers which sends a known sequence of data to the expansion connectors, where signals can be measured with an oscilloscope and verified.

43.4 CAN

The CAN peripheral frequency is set to 24 MHz in Vivado. Due to the clock dividers being only integers, the true frequency is 23.8 MHz. The Xilinx CAN drivers are used for a Vitis application. For setting the time quantums in the application code, a pre-scaler of 2 is selected, which is the minimum recommendation from the Zynq reference manual [2, p. 566]. The resulting time quantum is thus $t_{TQ} = \frac{1}{(23.8\text{MHz})/(2+1)} = 0.126\mu\text{s}$.

For a 1 Mbit/s baud rate, the following segments are chosen: Propagation segment of 3 time quanta. First segment of 3 time quanta. Second segment of 2 time quanta. The resulting baud rate is $BR = \frac{23.8\text{MHz}}{(2+1)\cdot(3+3+2)} = 0.9917\text{ Mbit/s}$, calculated with the equation given in [2, p. 581]. The sampling point is at 77.7% of the transmission.

An internal loopback can be created in software for debugging purposes, sending known values from CAN Tx to CAN Rx, and transmitting the received values over UART. This will verify that the CAN peripherals function correctly. To test the SN65HVD transceiver, the CAN drivers must not be in loopback mode. The CANH/CANL signals are possible to read with a PCAN-USB sniffer and associated program for a PC, which can be used to confirm that serial data is correctly converted to differential signals. The CANH/CANL signals should also be measured using an oscilloscope.

43.5 SDIO

In Vivado, the SDIO frequency is set to 50 MHz and the card detect feature is enabled. The SDIO interface is tested by writing known characters to a micro SD card. This test application uses the Xilinx 'xilffs' library, which is a light-weight library for managing file systems on an SD card.

The test procedure will be to insert an SD card onto the Master Controller with an existing file named "File1.txt" on it. The file will contain known text written on a PC. The Master Controller will firstly mount the SD card. Then, the software will create a new file called "DATA.TXT", in which a table will be written. The file contents will be read back and verified. Thereafter, the file will be closed and the existing file, "File1.txt", will be opened, read, and verified to match what was expected. Lastly, the file pointer is moved to the end of the file, and text is appended to the file and the file is closed. Correct functionality of the SD card circuit will also be determined upon checking the contents of the SD card after the test.

43.6 Ethernet

In Vivado, both Ethernet MACs are set to 100 Mb/s with Management Data I/O (MDIO) activated. As the MAC routed through the PL by default uses GMII, the TXD must be sliced to only output TXD[3:0], while the input RXD[3:0] is concatenated with zeros. The transmit error signal is unconnected, as it is unused on the KSZ8081MNX. The Vivado block diagram can be seen in Figure 38.

As clock timings are critical to synchronize signals within the FPGA, these must be configured. The KSZ8081MNX datasheet contains timing diagrams with setup and hold times for 100BASE-TX communication with the PHY [10, p. 50].

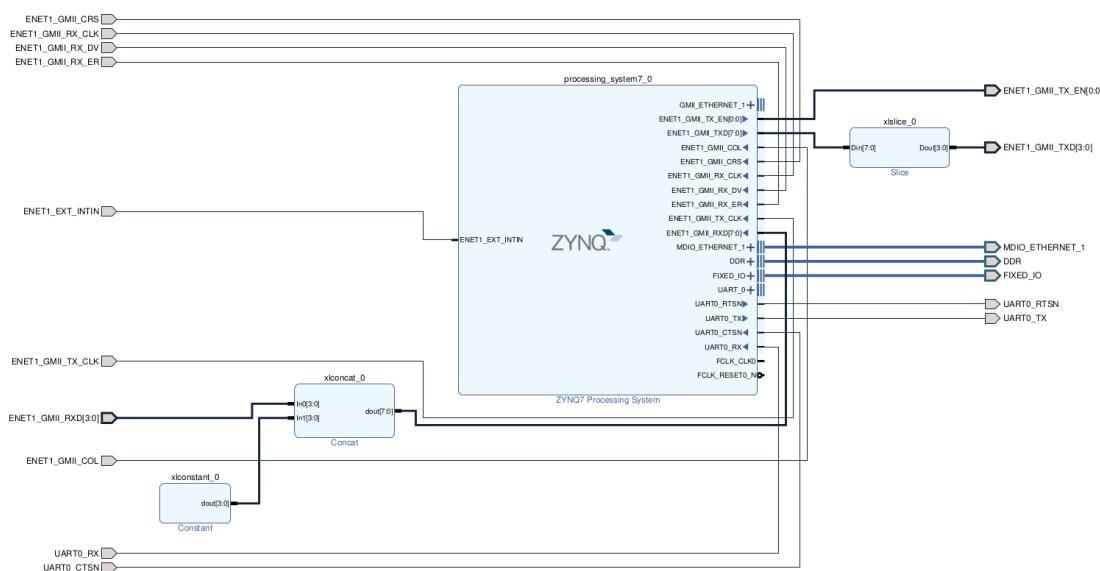


Figure 38: Vivado block diagram containing Zynq7 Processing System and Ethernet ports

The Ethernet functionality is tested with the Xilinx 'lwip' library, which contains light-weight functions for setting up the MAC and network configuration. An application is created that echoes whichever character is received over Ethernet from a host PC running PuTTY. This allows the Zynq to be pinged and both receive and transmit data through an Ethernet cable. Activity will also be indicated by the LEDs. The MLT-3 encoded differential signals should be measured with an oscilloscope, and are expected to behave as described in Section 20. As both Ethernet circuits should be tested, both the 4-pin and 8-pin M12s must be connected one at a time. To avoid damage to the PC, the 24 V converter must not be present on the PCB at the time of testing.

43.7 Power Distribution / Actuators

In Vivado, the PL GPIO used for enabling the Power-over-Ethernet FET is connected to the PS through an AXI GPIO IP block. The remaining signals are MIO GPIO. The Vivado block diagram is shown in Figure 39.

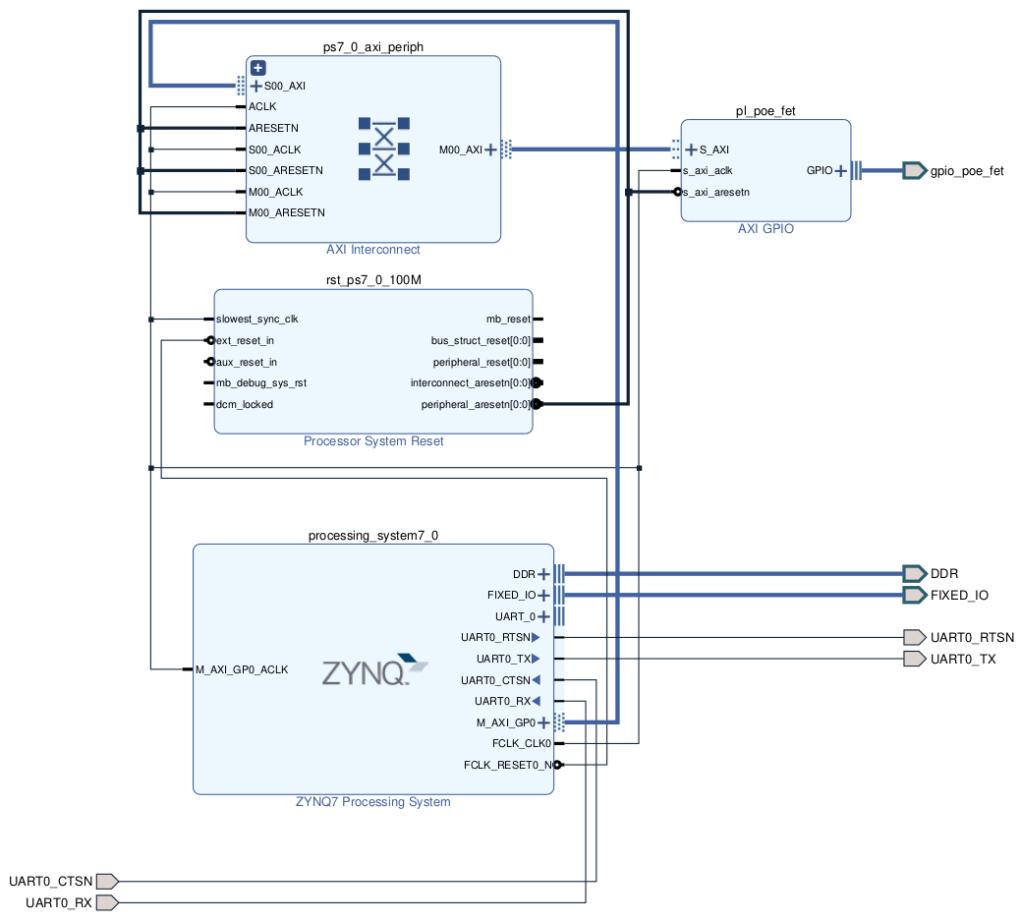


Figure 39: Vivado block diagram containing the Zynq7 Processing System, AXI interconnect, and AXI GPIO IP

It must be ensured that the Zynq is capable of activating all PROFETs and relays with its I/O pins. This is most easily confirmed by putting a voltage across the PROFETs and

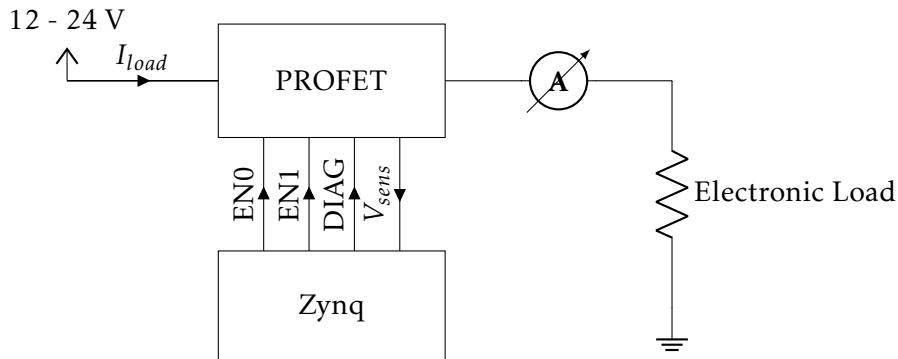


Figure 40: Circuit used for testing the Power Distribution and Actuator hardware

measuring the current. The I/O voltages after level shifting must also be measured to confirm correct values. Finally, the Zynq must also be able to change diagnostics channel on the PROFET to measure currents of both channels. Both the Xilinx AXI GPIO driver for PL pins and the Xilinx GPIO driver for PS pins are used to create a test application for asserting and deasserting the pins. The test setup is shown in Figure 40, which uses the electronic load EA-EL 9160-100 with serial number 1444030001.

43.8 Current Measurements

A unified test of both the XADC and the Power Distribution / Actuators must be performed to test the measurement accuracy of PROFET and TSC2012IDT, as well as confirm the functionality of remaining AUX channels. The Zynq also must be capable of changing the measured current in the PROFETs. The test must be performed similarly to the isolated XADC and Power Distribution tests, with the conversion results being communicated through UART, and the current being measured externally to verify. The test setup shown in Figure 40 will be used again, but with different software. The currents will be measured using a N2783A Current Probe powered by a N2779A Power Supply with serial number JP48040256. For actuator measurements, the electronic load cannot be used due to low resolution, and common resistors are used instead. Using the conversion results, the currents can be calculated using Equation 27.3 and Equation 28.1 for PROFETs, and Equation 27.6 for shunt resistor measurements.

The current measurement test will also examine the accuracy of the PROFETs' current measurements, so that the roughness of the battery capacity estimate can be determined.

43.9 Shutdown Circuit

All Shutdown Circuit signals are inputs to the PL, which is connected to the PS in Vivado with an AXI GPIO IP block. The signals on the Zynq-side of the Shutdown Circuit must be either 0 V or 3.3 V. It must be ensured that all signals function correctly. This is done by applying 12-24 V on the various CMC pins connected to the optocoupler and measuring the voltage on the isolated side, as well as observing the LEDs.

43.10 nvSRAM

A driver is created for communication with the CY14B256PA, which uses the SPI driver tested previously and defines transmission protocols for ease-of-use.

When a coin cell battery is connected, the RTC must continue unhindered even when power-cycling. The nvSRAM must be tested and confirmed to work as expected. An application is written with a variety of commands sent over SPI to confirm that data can be written to and stored in the nvSRAM. When power-cycling, the nvSRAM must store the data before turning off, which can be read when the board is powered on again.

The battery charging circuit should be tested with a rechargeable battery to confirm that the voltage is correct.

43.11 Power-over-Ethernet

Once the Ethernet communication and Power-over-Ethernet FET have been tested, the 24 V converter can be soldered into place. The WAP to be used can then be connected and confirmed to turn on by checking the power LED. The Wi-Fi should also be possible to connect to and keep a stable connection with by using a receiver WAP. While connected to the Wi-Fi, an echo test can be performed as before.

43.12 ADC Expansion Board

By setting up a SPI peripheral in Vivado, and by using the SPI driver once more, communication with the ADC can be established. A voltage should be applied to the ADC, and the resulting conversions confirmed to be accurate. This ensures that both the board and inter-communication works correctly.

44 Test Results

The coming subsections document the results from each test performed on the Master Controller PCB. The 3.3 V and 5 V voltages and crystal frequencies are as expected at both 12 V and 24 V input. The 5 V converter's output is 4.977 V with 63 mV peak-to-peak ripple. The mean value deviates from the expected value by $\frac{4.977-5}{5} \cdot 100 = -0.46\%$ and the ripple corresponds to $\pm 0.63\%$ of the mean value. The 5 V converter therefore satisfies the specification. The 3.3 V converter's output is 3.306 V with 47 mV peak-to-peak ripple. The mean value is a deviation 0.18% from the expected value, and the ripple results in another $\pm 0.7\%$. The 5 V and 3.3 V converter outputs can be seen in Figure 41a. The ripples are measured when supplying the idle Master Controller PCB. In this state, it draws around 0.25 A at 12 V, resulting in a power consumption of 3 W. The ripple values are expected to be higher when larger currents are supplied.



(a) Oscillosogram of 3.3 V and 5 V converters' outputs with 12 V input



(b) Oscillosogram of 12 V Boost converter's output from 5 V input

(c) Oscillosogram of 24 V converter's output from 12 V input

Figure 41: Oscillosograms of all converter outputs

In the current state, the 12 V converter does not activate. This is found to be because the enable pin requires a voltage of at least 85% of the 5 V input voltage, which the 3.3 V power good signal does not comply with. An alternative solution must thus be found.

By applying 5 V with an external power supply, it is confirmed that the converter's output is 12 V when enabled, as seen in Figure 41b. The peak-to-peak ripple is 125.5 mV, which is $\sim \pm 0.5\%$ of the mean value. After soldering the 24 V converter in, it is confirmed that the converter output is within $24 \text{ V} \pm 10\%$ at all times, as the output is 23.9 V with a peak-to-peak ripple of 392.2 mV, less than 1% of the mean value, which is seen in Figure 41c.

The crystals are also measured using the oscilloscope to confirm their respective expected frequencies. The oscillograms can be seen in Figure 42. As seen from the oscilloscopes, the RTC crystal has a measured frequency of $\sim 32.76 \text{ kHz}$. As only two significant figures are shown and the desired frequency contains three significant figures, the frequency deviation cannot be determined. The 25 MHz crystal has a measured frequency of 25.00 MHz, which is satisfactory.

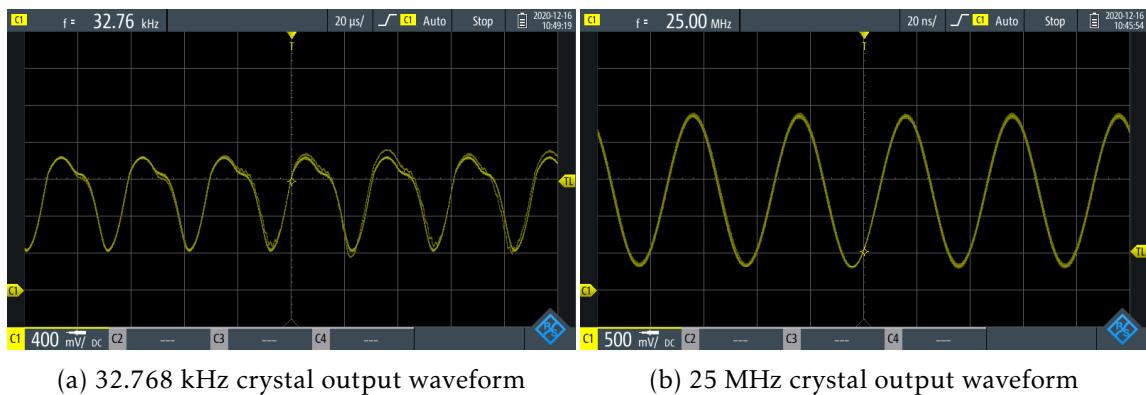


Figure 42: Oscillograms of both crystal outputs

44.1 UART/JTAG

The PC to Zynq connection is tested with a USB cable. The Zynq is successfully programmed with JTAG and echoes any data received over UART with no issue. The Tx signal from UART1 was also measured with an oscilloscope and confirmed to be correct, as seen in Figure 43. The oscilloscope shows idling, a start bit, 8 data bits sent with LSB first, and stop bit. The resulting values are 0x0D and 0x0A, being carriage return and line feed respectively, which is as expected.

Due to limited time and accessibility issues, the Bluetooth module and INS communication were not tested.

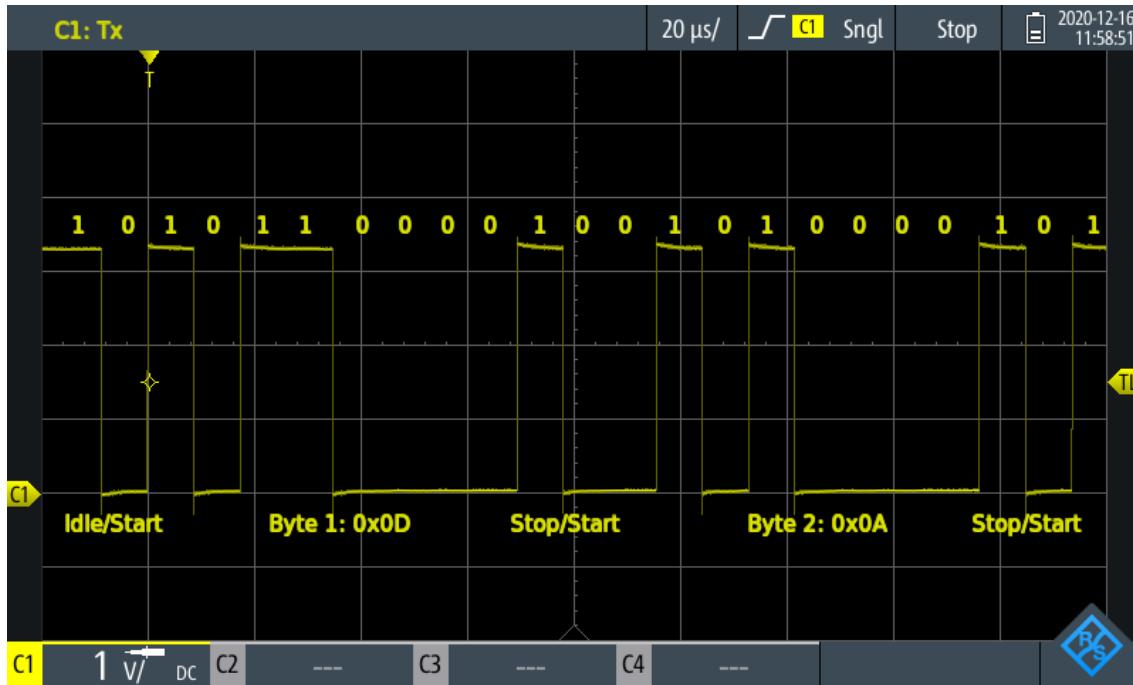


Figure 43: Annotated screenshot of oscilloscope measurement of UART1 Tx signal

44.2 XADC

The XADC is tested as previously specified. For AUX0, the results are shown in Table 29. For AUX channels 1, 3, 8, and 9, the results are shown in Appendix I. It is found that the voltage buffer used for torque pedals saturates at 3.3 V, as this is the supply voltage for it. When ignoring this, all results are well within the expected ranges, having a maximum inaccuracy of ± 17 LSB, equating to 4.15 mV. Using the equations of Subsection 16.1, the resulting mechanical ranges can be found for a $\pm 1\%$ accuracy with the maximum observed inaccuracy. For the torque sensor, the range would need to be 34.6 mm, while the steering wheel sensor would need a range of 181.1°.

AUX0 sensor voltage	Expected value	Converted value	Error
0.015 V	12	15	3 LSB
0.515 V	422	415	-7 LSB
1.015 V	831	820	-11 LSB
1.515 V	1241	1230	-11 LSB
2.010 V	1646	1638	-8 LSB
2.520 V	2064	2050	-14 LSB
3.010 V	2465	2463	-2 LSB
3.520 V	2883	2868	-15 LSB
4.020 V	3292	3275	-17 LSB
4.515 V	3698	3685	-13 LSB
5.010 V	4095	4095	0 LSB

Table 29: Results of AUX0 conversion tests

It would be valuable to calculate the guaranteed accuracy when the steering wheel sensor and torque pedal sensors are mounted with the minimum ranges. Solving for the accuracy in equation Equation 16.11 and using a range of 180° for the steering wheel sensor, gives a guaranteed accuracy of 1.65%, when using resistors with 0.5% tolerance and the MCP6L02T. Using a range of 35 mm for the torque pedal sensors gives a guaranteed accuracy of 1.88%.

44.3 SPI

The SPI0 peripheral is used to transmit to exposed headers, where the signals are measured. An oscilloscope screenshot showing the SPI clock and the Zynq's outgoing data can be seen in Figure 44. The slave select signal was also measured, and behaved as expected. Each transmission consists of three data bytes, the first being 0x04, 0x00, and 0xAA. The second transmission consists of 0x04, 0x80, and 0xAA. Between transmissions are an idle period. This is as expected, as it is the protocol for initiating conversion of channel 0 and 2 respectively on the MCP3208 ADC on the expansion board.

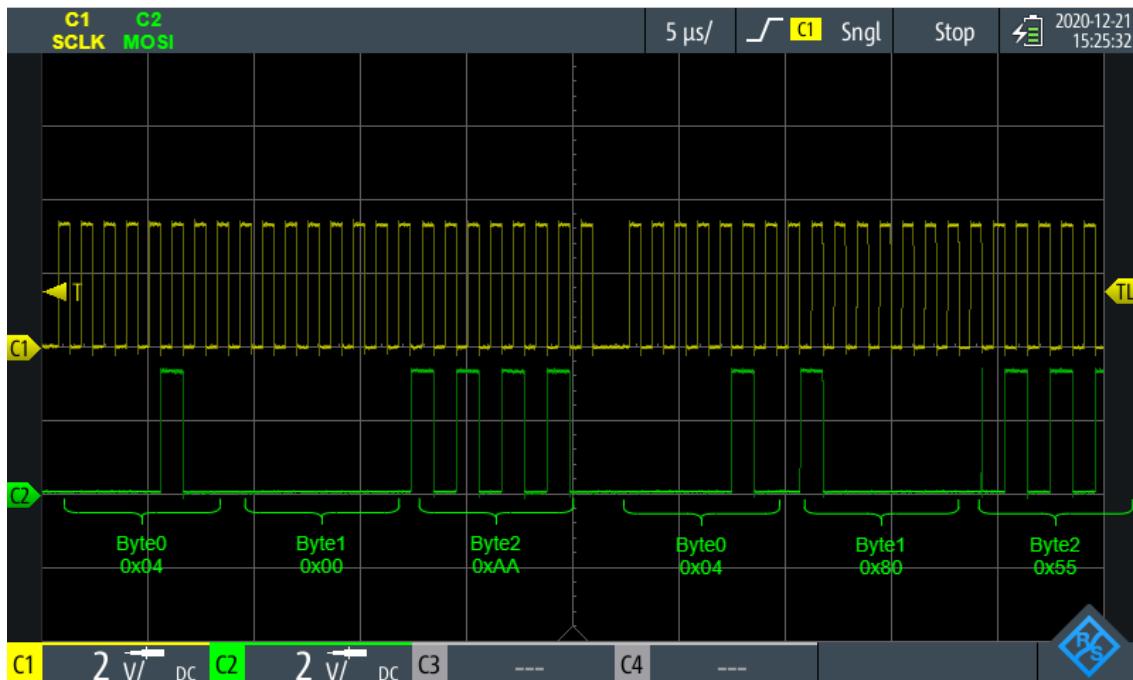


Figure 44: Annotated screenshot of oscilloscope measurement showing the SPI clock and the Zynq's data out pin

44.4 CAN

The loopback mode confirms that both CAN peripherals function correctly. The CAN-to-USB sniffer could not be used. Instead, the differential signals are measured with an oscilloscope, with the results of a CAN transmission being seen in Figure 45. This shows an ID, 6 data bytes with data, cyclic redundancy, and end of frame, as well as the other

symbols defined in Table 1. Bit stuffing is automatically added by the transceiver for synchronization; if five bits in a row are identical, a sixth is added that is the inverse, regardless of whether the next bit is already the inverse. This bit will be ignored by the receiver. The differential signals are driven correctly by the transceiver, as all values are as expected. The bit rate is 1 Mbit/s as configured. The transmitted message was a six-byte data frame containing the data: 0x33, 0x55, 0x77, 0x99, 0xAA, 0xCC with an identifier of 0x7D0, as is confirmed by Figure 45.

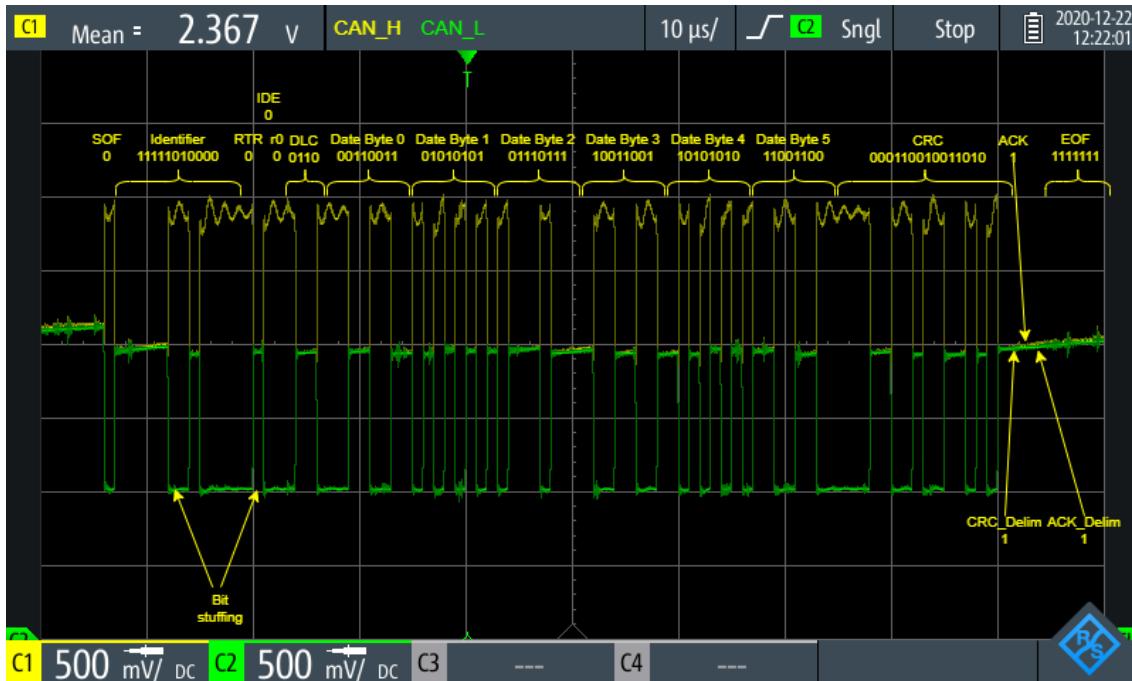


Figure 45: Annotated screenshot of oscilloscope measurement showing the CAN bus differential signals

44.5 SDIO

The SD card functionality is tested. The software can mount the card, create new files or open existing ones, and write characters to them. The card detect feature does not work correctly, and must be disabled in Vivado. The SD card can be hot-swapped without any issues.

44.6 Ethernet

Both Ethernet connections are tested and successfully echo the received characters at 100 Mbit/s. A screenshot from the terminal while testing Ethernet MAC 0 is shown in Figure 46.

The differential pair from the KSZ8081MNX connected to Ethernet MAC 1 is shown in Figure 47, which also shows the differential voltage. This is MLT-3 encoded as expected, with correct frequency. Due to the complex protocols, data encoding, and scram-

bling, values cannot be compared to expected values. The coded data is decoded to find individual bits, which is shown annotated in Figure 47.

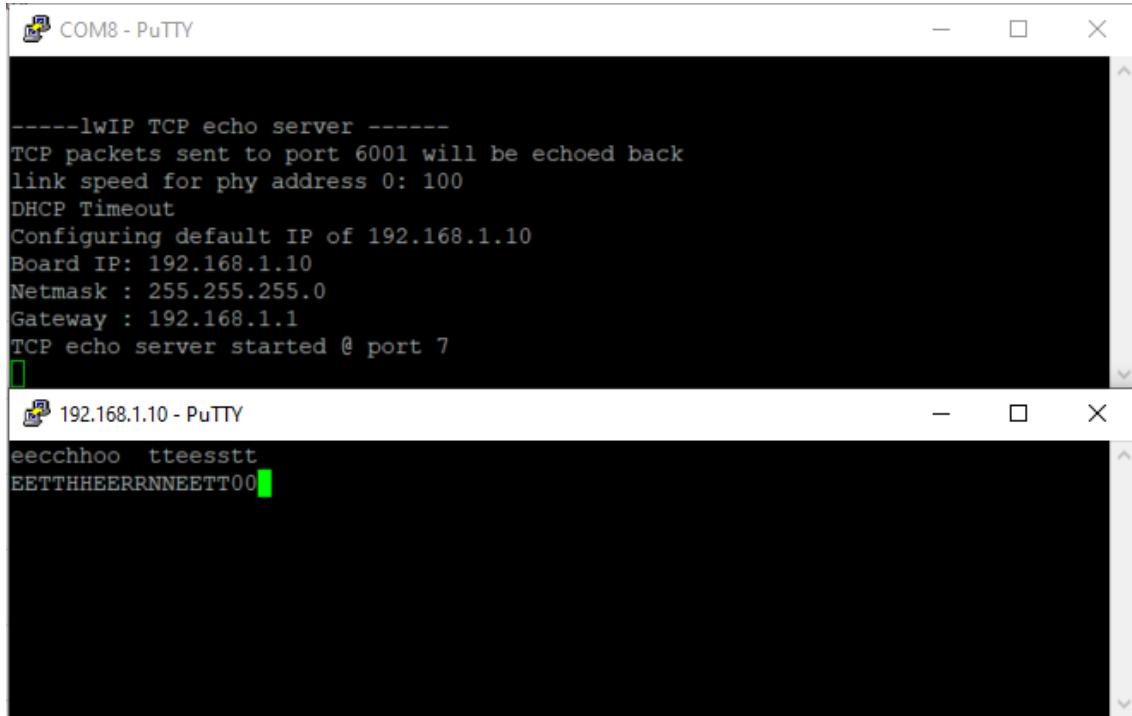


Figure 46: Screenshot of PuTTY terminal communicating with Zynq over Ethernet



Figure 47: Annotated screenshot of oscilloscope measurement showing the MLT3-encoded KSZ8081MNX differential signals

44.7 Power Distribution / Actuators

The PROFETs and Solid-State Relays are tested and confirmed to activate correctly with the Zynq's GPIO pins. The level translators output 3.3 V as expected.

44.8 Current Measurements

The current measurement test is completed as a merge of the XADC and Power Distribution tests. For PROFET 1, the results are shown in Table 30. For PROFET 2 through 4, as well as TSC2012IDT currents, the results are shown in Appendix J. The PROFET 5 for Power-over-Ethernet is not tested due to lack of time and the connector type. The Master Controller current measurement could not be tested due to its positioning.

PROFET 1 current	Converted value	Calculated current	Error
0 mA	8	2 mA	2 mA (-%)
79 mA	265	71 mA	-8 mA (-10.13%)
149 mA	530	141 mA	-8 mA (-5.37%)
270 mA	970	259 mA	-11 mA (-4.07%)
342 mA	1243	332 mA	-10 mA (-2.92%)
466 mA	1687	450 mA	-16 mA (-3.43%)
562 mA	2055	548 mA	-14 mA (-2.49%)
670 mA	2425	647 mA	-23 mA (-3.43%)
755 mA	2800	747 mA	-8 mA (-1.06%)
850 mA	3171	846 mA	-4 mA (-0.47%)
940 mA	3548	946 mA	6 mA (0.64%)
1050 mA	3921	1046 mA	-4 mA (-0.38%)

Table 30: Results of PROFET 1 current measurement test

The PROFET conversions for dual-channel PROFETs have a maximum error of $\pm 3.49\%$ at medium and high currents. The single-channel PROFET has conversion errors up to $\pm 4.78\%$. The current for RTDS and Brake Light also includes driving the LED indicating activity. For the RTDS, this accounts for over 25% of the maximum current, and thus always contributes to a large error. When accounted for, the measurements are accurate for both actuators, although a gain error is measured for the brake light.

44.9 Shutdown Circuit

The SC voltages are correctly level shifted, allowing the GPIO to measure the values. The LEDs are clearly lit up both with a 12 V and 24 V input. When an LED is lit up, the Zynq reads logic 0 on the associated pin as expected.

44.10 nvSRAM

The RTC continues correctly when the nvSRAM supply is powered off, and data is stored and recalled when transitioning. A screenshot of terminal output showing the RTC's

value read after power-cycling is seen in Figure 48.

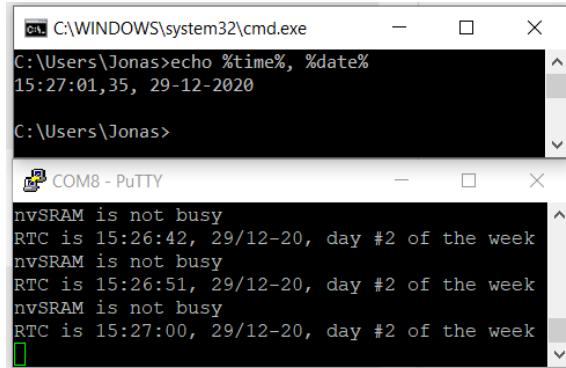

 A screenshot of a Windows Command Prompt window (cmd.exe) and a PuTTY terminal window. The cmd window shows the command 'echo %time%, %date%' and its output '15:27:01,35, 29-12-2020'. The PuTTY window shows several lines of text from the RTC, including 'nvSRAM is not busy', 'RTC is 15:26:42, 29/12-20, day #2 of the week', 'nvSRAM is not busy', 'RTC is 15:26:51, 29/12-20, day #2 of the week', 'nvSRAM is not busy', and 'RTC is 15:27:00, 29/12-20, day #2 of the week'.

Figure 48: Screenshot of PuTTY terminal showing values read from the RTC by Zynq after power-cycling

Due to limited time, and a discrepancy between the footprint and the rechargeable battery pins, the battery charging circuit was not tested.

44.11 Power-over-Ethernet

The 24 V converter is able to fully supply the WAP, turning it on and establishing a Wi-Fi network, which can be connected to. The WAP draws just below 0.2 A in steady-state. Due to limited time, the receiving WAP used for communication with the Master Controller PCB could not be configured, and the echo test was not completed.

44.12 ADC Expansion Board

The communication with the ADC Expansion Board works correctly. Conversion results are within ± 14 LSB of the expected values.

Channel 0 sensor voltage	Expected value	Converted value	Error
0.015 V	12	11	-1 LSB
0.503 V	422	415	-7 LSB
1.040 V	831	828	-3 LSB
1.512 V	1241	1238	-3 LSB
2.010 V	1646	1653	7 LSB
2.520 V	2064	2068	4 LSB
3.013 V	2465	2479	14 LSB
3.522 V	2883	2890	7 LSB
4.025 V	3292	3304	12 LSB
4.522 V	3698	3712	14 LSB
5.023 V	4095	4090	-5 LSB

Table 31: Results of Expansion Board conversion tests

45 Test Summary

The hardware design has been tested successfully. All Zynq peripherals function during isolated testing. Bluetooth, INS communication, communication with the WAP, and battery charging was not tested. Of the remaining hardware, it is found that the 12 V converter does not enable correctly, and the torque pedal voltage buffers saturate at a low voltage. The SD card detection does not work at all. These are the only issues with primary functions, while the remaining hardware functions correctly. A full summary of the testing results is shown in Table 32.

Test Specification	Result
3.3 V converter output	Passed
5 V converter output	Passed
12 V converter output	Failed
24 V converter output	Passed
Converters when LVS ranges from 12 V to 24 V	Passed
25 MHz crystal frequency	Passed
32.768 kHz crystal frequency	Passed
Programming Zynq through USB-JTAG	Passed
UART communication through USB	Passed
UART communication through Bluetooth	Not tested
UART communication with INS	Not tested
XADC conversion accuracy	Passed
Sensor signal voltages	Failed
SPI controller signals	Passed
CAN controller signals	Passed
SD card interfacing	Passed
SD card detection	Failed
Liveview Ethernet communication	Passed
Driverless Ethernet communication	Passed
Power Distribution GPIO signals	Passed
PROFET current measurement	Passed
Shutdown Circuit signals	Passed
Real-Time Clock operation	Passed
nvSRAM operation	Passed
Battery charging circuit	Not tested
Wireless Access Point power	Passed
Wireless Access Point operation	Not tested
ADC Expansion Board operation and accuracy	Passed

Table 32: Summary of testing results for Master Controller PCB

Part V

Discussion

The Master Controller has in the previous sections and parts been designed and tested. Overall, most of the tested subcircuits functioned as intended. All voltages and crystal frequencies are well within the expected ranges for use on the PCB. Furthermore, the 5 V and 3.3 V converters worked with a wide range of LVS voltages. The 12 V sensor supply converter was found to not activate, as the enable pin must receive a 5 V enable signal. This can either be directly from the 5 V converter, or by level shifting the 3.3 V power good signal, which is preferred due to the power sequencing. Programming and UART communication functions as expected. SPI communication worked as intended, both when communicating with the nvSRAM as well as with the external ADC on the ADC Expansion Board. The CAN interface seemed to work as well when measuring the signals with an oscilloscope. Dominant and recessive symbols were easily separable, and the CAN bit rate was verified to be 1 Mbit/s. Although the bus signals looked good, the messages failed to be picked up by a CAN sniffer. As time was sparse, further work on fixing this issue has not been done.

Ethernet communication also worked even though the differential signals seemed noisier than those of the CAN bus. It worked in an isolated environment, but it should be examined whether the communication works in a more noise-ridden environment, such as in an electric racecar.

On the measurement side of the PCB, both Shutdown Circuit monitoring as well as power distribution worked with no issues. The Zynq was able to detect open-circuits in the Shutdown Circuit, and was able to both control the PROFETs and SSRs distributing the LVS to the other nodes in the vehicle, as well as measure the currents with very satisfying accuracies. The worst error observed at medium-to-high current flows was found to be $\pm 4.78\%$ in Table J.3 in Appendix J. This is accurate enough for rough Coulomb counting and for knowing whether the nodes are active. The accuracy can be further improved by hardware averaging the conversions and by using lower tolerance resistors. The TSC2012IDT actuator current measurements proved largely inaccurate due to the LED currents being measured along with the actuator current. The LEDs should be moved to the other side of the shunts to fix this.

The XADC tests indicate that conversion accuracies are well within the theoretical expected values, resulting in lower mechanical ranges needed for adequate sensor accuracy. The worst observed conversion error of ± 17 LSB results in a sensor accuracy of $\pm 1\%$ when the mechanical range of the steering wheel is 181.1° and the range of the torque pedal sensors is 34.6 mm. Using worst-case component tolerances and errors, a mechanical range of 180° for the steering wheel sensor results in a guaranteed accuracy of $\pm 1.65\%$. A mechanical range of 35 mm for the torque pedal sensors results in a guaranteed accu-

racy of $\pm 1.88\%$. These accuracies are acceptable, as a human is not expected to be able to actuate a steering wheel nor torque pedal with a better precision anyway.

The overall sensor accuracy can be improved by using a more expensive operational amplifier, lower tolerance components, and with software calibration to remove any offset error. The voltage divider resistor tolerances introduce a gain error to the conversion, which can similarly be negated by finding a factor to be multiplied with the conversion result.

Through testing it was also found that the torque pedal voltage buffers saturate due to a low supply voltage. They should be supplied with 12 V, which would require a different op amp. Alternatively, the used resistors can be changed to result in a maximum output of 3.3 V, although it would reduce sensor accuracy and impact supply flexibility.

On this revision of the PCB, the Sallen-Key filters have been placed after the voltage dividers and close to the CMC connectors. Further testing of the board's EMC may show that having voltage division after the filter improves performance, as noise and Sallen-Key imperfections are also reduced. This would require supplying the operational amplifiers with 12 V instead of 3.3 V. If the filters are placed closer to the Zynq, less noise makes it into the XADC, but more noise makes it onto the board instead. If the Sallen-Key filters are placed before the voltage division, the voltage buffers for torque pedals are not needed.

46 Future Work

During design of the PCB, Electromagnetic Compatibility has been prioritized by using chokes and ferrite beads. The performance has not been tested due to lack of testing facilities. The University of Southern Denmark in Sønderborg has an EMC laboratory, which might be possible to use for these tests.

Due to the COVID-19 pandemic, it was not possible to use a network analyzer like the Bode 100 for measuring the Sallen-Key filters' transfer functions. To ensure that the filter meets the set requirements, this analysis should be performed once possible.

An overall test of the Master Controller PCB, in which the PCB is tested in the system it is to operate in, has not been performed due to a lack of time, and not having access to all the nodes and components required for such a test. Such a hardware-in-the-loop test setup would also be very laborious to assemble and perform. Furthermore, it would require a substantial amount of time for developing the test software, as it would mean writing an application and piecing together the code for all the different parts. This test would make it clear whether the Master Controller PCB can be used by SDU-Vikings without further modifications. For optimization of the board, the fixes mentioned in the discussion must be implemented.

No application software to be used in the car has been implemented. The drivers used for testing peripherals and hardware may be useful during development of this. Members of SDU-Vikings have previously used the RTOS µC/OS developed by Micrium, which facilitates task scheduling and inter-task communication in the application. The OS would make it easier to replicate the X90 application, as well as expand on the functionalities. An initial software analysis with high abstraction level has been performed in Appendix H.

While one core is executing the application, the other will be hosting the live-view page. This will be designed using an embedded Linux variant, as creating a GUI and showcasing data is much easier and more flexible with Linux. Xilinx offers the PetaLinux Tools and Linux peripheral drivers, which can be used to ease the implementation of a Linux Distribution. AVNET also supplies a PetaLinux BSP for the PicoZed.

Part VI

Conclusion

This project revolved around designing a Master Controller PCB based on the PicoZed with Zynq-7020 for use in an electric Formula Student racecar. The Master Controller has a considerable amount of responsibilities, including sensor measurements, distributing the Low Voltage System, Ethernet and CAN communication, and data-logging. The analysis showed that the Zynq-7020 is capable of lifting these responsibilities.

The Master Controller PCB was designed with flexibility in mind, assembled, and tested to verify that it functions as intended. The needs were both set by the rules of the Formula Student Competition and the SDU-Vikings' mechanical and electrical requirements. As not all parts of the Master Controller PCB have been tested, it is not everything that can be concluded upon. This includes the Bluetooth, RS232 UART and wireless communication through the Ethernet modules, as well as the battery charging circuit.

It can however be concluded that a wide range of voltages from the LVS can be used for supplying the PCB. The 12 V converter does not turn on presently, as it requires a 5 V signal to enable. The tests demonstrated that the JTAG/UART module works as expected, as the Zynq is programmable and able to communicate through micro-USB.

The sensor accuracy and XADC tests established that the conversion accuracy was within 17 LSB, which gives a high degree of accuracy when finding the position of mechanical sensors. For the torque pedal sensors, voltage buffers were implemented before the voltage division that saturated at 3.3 V, reducing the voltage range significantly. To fix this error, the buffers must be supplied by at least 12 V. The Shutdown Circuit can be monitored to find open-circuited components.

The communication tests were all successful, as SPI, CAN, SDIO, and Ethernet communication worked. SPI communication with the nvSRAM with built-in RTC also proved successful. The nvSRAM was able to store data and retain it, and the RTC continued counting when only powered by a battery. A minor flaw was found in the SDIO design, as the SD card detection functionality did not work.

The power distribution circuits using PROFETs and Solid-State Relays were able to distribute the LVS to the various external nodes as controlled by the Zynq. The PROFET current measurements were accurate to within 4.78% at medium and high currents, which is reasonable for Coulomb counting and error finding, while TSC2012IDT current measurements of actuators were inaccurate due to LED currents.

To find whether the Master Controller PCB is usable by SDU-Vikings, the PCB should be inserted in the system it should operate in, or a test bench emulating the system. As stated above, the Master Controller PCB mostly meets the requirements imposed on it, with few flaws. These can be worked around initially, but another PCB revision must be made to fix errors for optimal performance.

List of Abbreviations

Abbreviation	Description
ADC	Analog-to-Digital Converter
AMS	Accumulator Management System
AUX	Auxiliary XADC Input
AXI	Advanced Extensible Interface
BMS	Battery Management System
BSP	Board Support Package
CAN	Controller Area Network
CT	Center Tap
CMRR	Common-Mode Rejection Ratio
DMA	Direct Memory Access
DSP	Digital Signal Processor
EEPROM	Electrically Erasable Programmable ROM
EMC	Electromagnetic Compatibility
EMI	Electromagnetic Interference
EMIO	Extended Multiplexed I/O
ESD	Electrostatic Discharge
FET	Field-Effect Transistor
FPGA	Field-Programmable Gate Array
GMII	Gigabit Media-Independent Interface
GPIO	General Purpose I/O
I2C	Inter-Integrated Circuit
IC	Integrated Circuit
INS	Inertial Navigation System
IP	Intellectual Property
JTAG	Joint Test Action Group
LDO	Low-Dropout
LED	Light-Emitting Diode
LVS	Low Voltage System
MDIO	Management Data I/O
MII	Media-Independent Interface
MOSI	Master Out/Slave In
MISO	Master In/Slave Out
MIO	Multiplexed I/O
NTC	Negative Temperature Coefficient
nvSRAM	Non-Volatile Static RAM
Op Amp	Operational Amplifier
OS	Operating System

Abbreviation	Description
PCB	Printed Circuit Board
PHY	Physical Layer IC
PL	Programmable Logic
PLC	Programmable Logic Controller
PoE	Power-over-Ethernet
PS	Processing System
QSPI	Quad-SPI
RAM	Random-Access Memory
RGMII	Reduced Gigabit Media-Independent Interface
RMII	Reduced Media-Independent Interface
ROM	Read-Only Memory
RTC	Real-Time Clock
RTDS	Ready-To-Drive Sound
RTOS	Real-Time Operating System
SC	Shutdown Circuit
SDU	University of Southern Denmark
SMD	Surface-Mount Device
SoC	System-on-a-Chip
SoM	System-on-Module
SPI	Serial Peripheral Interface
SS	Slave Select
SSR	Solid-State Relay
TCL	Tool Command Language
TS	Tractive System
TSC	Tractive System Container
TTL	Transistor-Transistor Logic
TVS	Transient-Voltage-Suppression
UART	Universal Asynchronous Receiver-Transmitter
WAP	Wireless Access Point
XADC	Mixed-Signal ADC

Table 33: List of Abbreviations

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Part VII

Appendices

A Zynq-7000 Processor Design

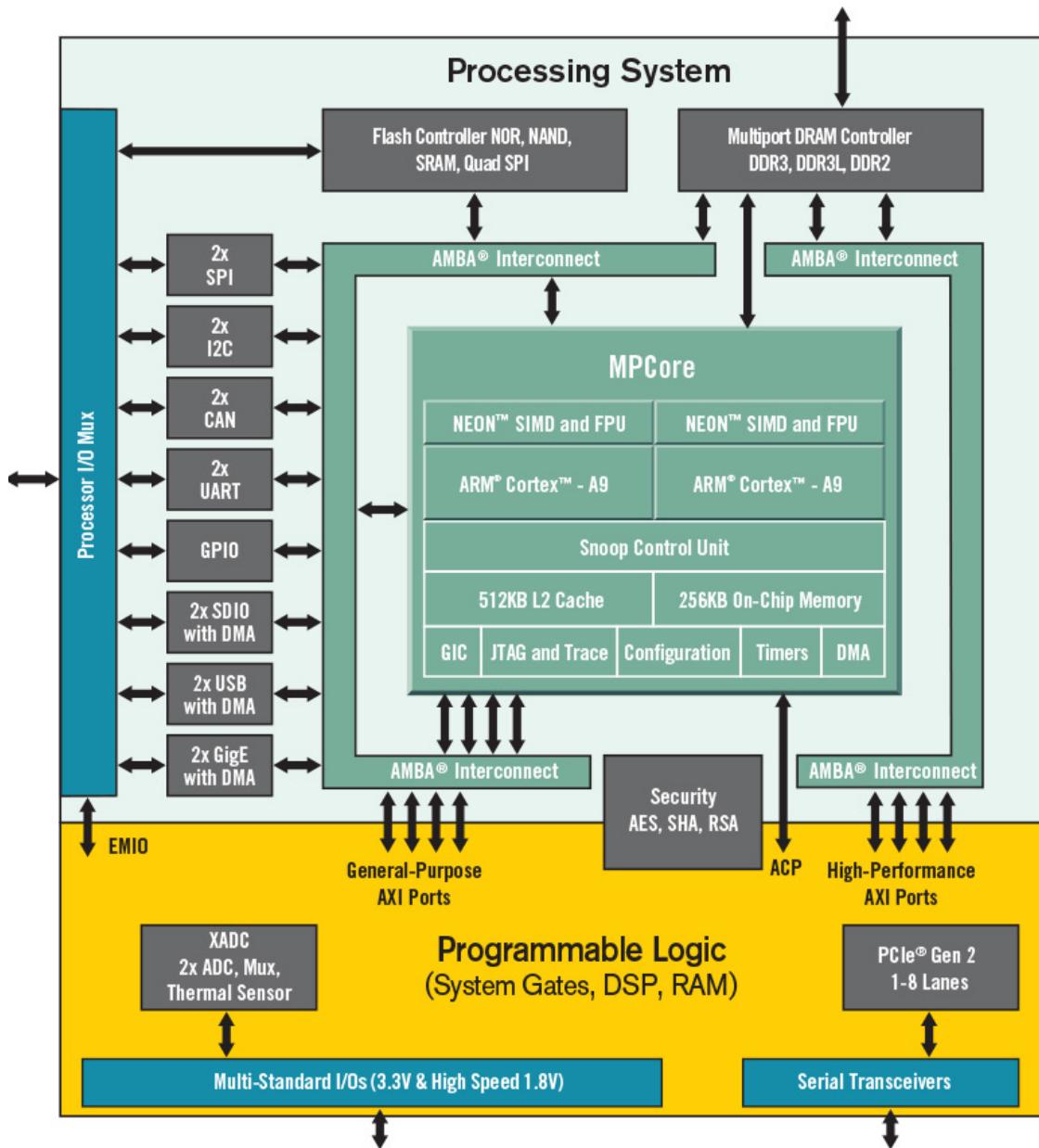


Figure A.1: Block diagram of the general Zynq-7000 processor design³

³<https://www.xilinx.com/content/dam/xilinx/imgs/block-diagrams/zynq-mp-core-dual.png>

B CAN Protocols

Inverters

Message ID	Description	Rate [ms]	Size [bytes]
0x283, 0x284, 0x287, 0x288	AMK Actual Values 1	5	8
0x285, 0x286, 0x289, 0x28A	AMK Actual Values 2	5	8
0x184, 0x185, 0x188, 0x189	AMK Setpoints	30	8

Table B.1: CAN Protocol for Inverters. There are four inverters, hence four IDs per message

AMS

Message ID	Description	Rate [ms]	Size [bytes]
0x300	AMS Status (Master)	100 + Aperiodic	1
0x301	AMS Status (charger)	100 + Aperiodic	4
0x305	Car Status	50	2
0x310	Charger Commands	100	3
0x311	Cell Voltages	1000	8
0x312	Cell Temperatures	1000	6
0x313	Discharge Cell Temperatures	1000	8
0x314	AMS Error	Aperiodic	3
0x350	Override Charge Current	Aperiodic	1
0x351	Override Bank Count	Aperiodic	1

Table B.2: CAN Protocol for communication between AMS and Master Controller

Shunt

Message ID	Description	Rate [ms]	Size [bytes]
0x411	Command Message	Aperiodic	8
0x521	Current	100	6
0x522	Voltage, phase 1	50	6
0x523	Voltage, phase 2	50	6
0x526	Power (w/ phase 1 voltage)	100	6
0x527	Coulomb Counter	200	6
0x528	Energy Counter	200	6

Table B.3: CAN Protocol for communication between IVT-S Shunt and Master Controller

Dashboard

Message ID	Description	Rate [ms]	Size [bytes]
580	Driving Data	100	6
0x581	Car Status	100	6
0x582	Dashboard LED Status	100	2
0x583	Mission Data	100	6
0x584	Driving Data 2	100	4
0x5C0	Dashboard Button Status	100	1
0x5C1	Dashboard Status	100	1
0x5C2	Set Mission	Aperiodic	1

Table B.4: CAN Protocol between Dashboard and Master Controller

Sensor Network

Message ID	Description	Rate [ms]	Size [bytes]
0x601	Select Sensor	Aperiodic	1
0x602	IIR Filter Coefficients	Aperiodic	5
0x603	IIR Gain Value	Aperiodic	5
0x604	Window Value	Aperiodic	5
0x605	Polynomial Value	Aperiodic	5
0x606	Show Node ID	Aperiodic	0
0x607	Transmit Rate	Aperiodic	5
0x6A1	Signal Error	Aperiodic	1
0x6A2	Initialization Request	Aperiodic	0
0x6A3	Signal Value	10-50	5
0x67F	Node ID	Aperiodic	1

Table B.5: CAN Protocol between Sensor Network and Master Controller

FS Datalogger

Message ID	Description	Rate [ms]	Size [bytes]
0x500	DV Driving Dynamics 1	100	8
0x501	DV Driving Dynamics 2	100	6
0x502	DV System Status	100	5

Table B.6: CAN Protocol between FS Datalogger and Master Controller

C SmartFET Test Journal

Functional and destructive test of Infineon's Automotive Smart High-Side Switches

September 2020

Authors: Jonas Fuglsang Hansen & Sebastian Rud Madsen
University of Southern Denmark

Purpose of tests

The purpose of this journal is to determine whether Infineon's PROFETs are suitable for use as smart switches for power distribution in an automotive Master Controller. The PROFETs will be controlling the current flow to nodes that draw a substantial amount of current.

A functional test of the PROFETs is performed, where it is determined whether the PROFETs can be controlled as intended by 3.3 V digital I/O signals, whether the designed current sense circuit works as intended and what the precision of the current sense circuit is. Furthermore, it is tested how much power is dissipated in the PROFETs, how much heat is generated and whether this could prove a problem. A temperature test is performed, where it is determined how much power is dissipated in the PROFETs when running at nominal load. The temperature of the casing is also measured regularly. Lastly, a destructive test is performed, where the PROFETs are tested with load currents above the nominal load current. In this final test it is examined how the PROFETs handle high load currents, i.e. whether they are destroyed or their protection features set in.

Design of PROFET Evaluation Board

A PCB for testing the functionality of the PROFETs is designed and manufactured. The PROFETs output a current on the sense pin that is proportional to the load current. The load current can be measured by measuring the voltage over a current sense resistor between the sense pin and ground. The PCB includes two PROFETs, one single-channel PROFET, namely the BTT6010-1EKB [1], and a dual-channel PROFET, the BTT6030-2EKA [2].

The design of the sense circuit follows the application note for the PROFET [3, p. 78]: "PROFET™+24V, Short Introduction to PROFET™+24V". The maximum current sense resistor value can be calculated with the formula

$$R_{IS} = \frac{V_{ADC,max}}{I_{L,max}/(k_{ILIS}(1 - k_{ILIS,tol}))} \quad (C.1)$$

Where $V_{ADC,max}$ is the maximally allowed voltage on the ADC input, $I_{L,max}$ is the maximally expected load current, k_{ILIS} is the load-current-to-sense-current ratio and $k_{ILIS,tol}$ is this ratio's tolerance. With $V_{ADC,max} = 1\text{V}$ and for the BTT6010-1, the maximum load current $I_{L,max} = 10\text{A}$, $k_{ILIS} = 3900$ and $k_{ILIS,tol} = \pm 9\%$. Inserting these values into Equation C.1 gives a current sense resistor value of $R_{IS} = 330\Omega$, when rounding to the nearest E6-series value. With this current sense resistor, the load current that results in $V_{ADC} = 1\text{V}$ can be found. First, the sense current is found:

$$I_{IS,max} = \frac{V_{ADC,max}}{R_{IS}} = 3\text{mA} \quad (\text{C.2})$$

The minimum and maximum load currents that results in $V_{ADC} = 1\text{V}$ are

$$\begin{aligned} I_{L,min} &= I_{IS,max} \cdot k_{ILIS} \cdot (1 - k_{ILIS,tol}) = 10.75\text{A} \\ I_{L,max} &= I_{IS,max} \cdot k_{ILIS} \cdot (1 + k_{ILIS,tol}) = 12.88\text{A} \end{aligned} \quad (\text{C.3})$$

To protect the ADC from voltages higher than $V_{ADC,max}$ a Zener Diode can be placed, providing a route for the current to ground, when the voltage is above the Zener Voltage. As Zener diodes with Zener voltages of 1.2-1.5 V cannot easily be found a voltage divider is implemented on the sense pin, with R_{IS} being the bottom resistor. As Zener diodes with Zener voltages above 5 V are plentiful, a voltage divider ratio of ~ 4 is desired. Using this ratio and rounding to the nearest E6-series value a resistor value of $R_{DIV} = 1500\Omega$ is found for the top resistor. This gives a desired Zener voltage of

$$V_Z = \frac{V_{ADC,max}}{\frac{R_{IS}}{R_{IS}+R_{DIV}}} = 5.55\text{V} \quad (\text{C.4})$$

A fitting Zener voltage is therefore 5.6 V. Lastly, a low-pass filter is placed on the input of the XADC channel to filter the current sense signal as well as imitate the actual circuit to be implemented. The sense circuit is simulated to verify the functionality. The output filter is an RC filter with $R = 10\text{k}\Omega$ and $C = 10\text{nF}$, giving time constant and cut-off frequency:

$$\begin{aligned} \tau &= RC = 100\mu\text{s} \\ f_c &= \frac{1}{2\pi RC} = 1.59\text{kHz} \end{aligned} \quad (\text{C.5})$$

As advised by the application note [3, p. 73] and the datasheet [1, pp. 41-42], a ground resistor and ground diode is used for ground protection. The ground resistor is a 33Ω resistor, and the ground diode is a BAS21, to protect from reverse polarity events. The circuit can be seen in Figure C.1.

The surrounding circuit for the BTT6030-2 is designed in a similar manner with a maximum load current of $I_{L,max} = 6\text{A}$. Using the same design flow as above, the sense circuit and ground circuit are similar to that of the BTT6010-1 [2, pp. 49-50].

The schematic of the evaluation PCB can be found in Appendix D.

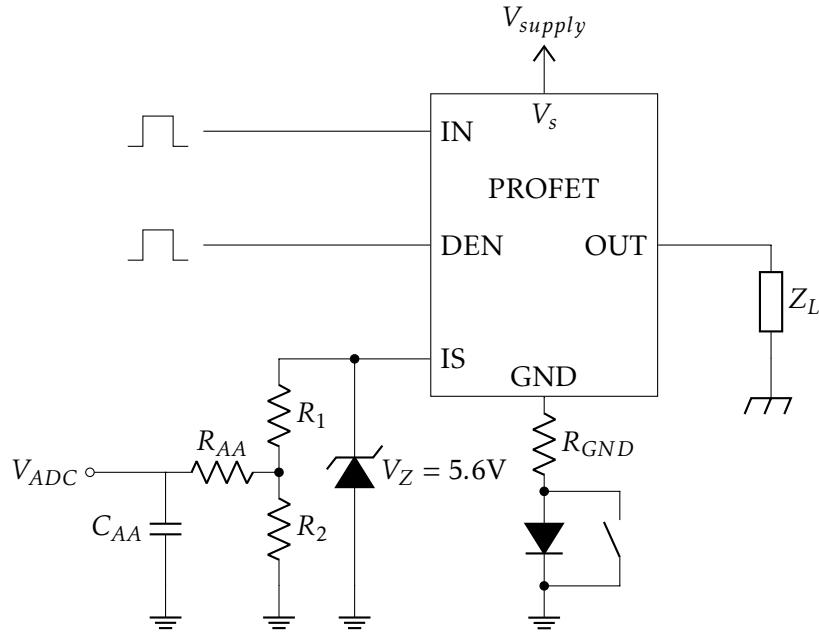


Figure C.1: Single-channel PROFET connections. IN pin turns ON switch, so the PROFET outputs V_{supply} at OUT over the load Z_L . DEN enables diagnostics, e.g. current sensing. The current sense circuit limits V_{IS} to $V_Z = 5.6V$, performs a voltage division and filters the voltage, so the signal can be sampled.

Simulation of Current Sense Circuit

The current sense pin of the PROFET can be represented by a current source, I_{IS} , dependent on the load current, I_L . The PSPICE schematic of the current sense circuit is as shown in Figure C.2. Using the method described above, a voltage divider of is used.

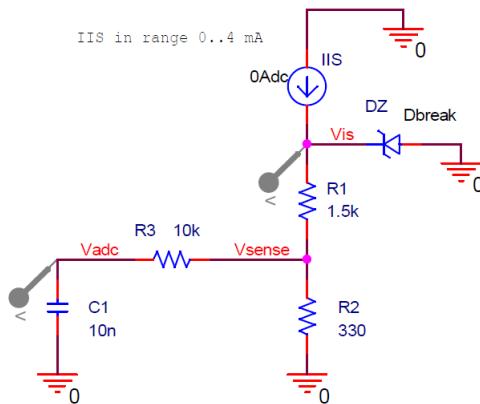


Figure C.2: Simulation schematic of proposed current sense circuit. The sense pin is represented by a current source.

Performing a DC Sweep simulation of this circuit, with the sense current I_{IS} in the range from 0-4 mA, the output can be seen in Figure C.3. As seen from the plot, the ADC input voltage rises linearly with the sense current. When the output voltage of the sense pin reaches 5.6 V, it is seen that the Zener diode clamps the voltage at 5.6 V and consumes

the exceeding current. From the simulation result it is seen that the sense circuit works as intended, assuming that the sense pin can be represented by a dependent current source.

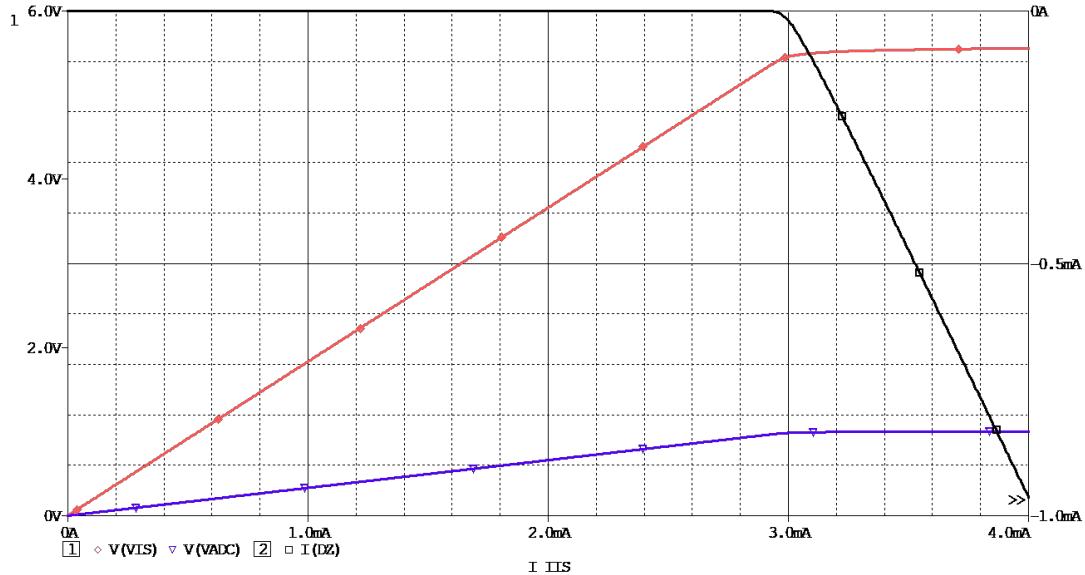


Figure C.3: PSPICE simulation of proposed current sense circuit

Test Procedure

The single-channel PROFET circuit is connected like shown in Figure C.1. The dual-channel PROFET circuit is connected similarly, but only differs in having two output channels, two IN pins, one for each channel, and a diagnostics select pin (DSEL), for selecting which channel's current is sensed.

Functional test

In the functional test, it is determined whether the PROFETs respond as intended to digital signals from the Zynq-7000. The tests include: switching on the PROFET, enabling diagnostics features and testing current sense over the range from 0 A to $I_{L(NOM)}$.

The test procedure is as follows:

1. Connect power supply, load(s) and microcontroller or other controller.
2. Test PROFET with switch OFF. Any leakage current?
3. Turn ON PROFET with 3.3 V IN signal and 3.3 V Diagnostics Enable (DEN) signal.
4. Vary load current over range $I_L \in [0, I_{L(NOM)}]$ and measure:
 - (a) sense voltage, V_{IS} ,
 - (b) voltage on ADC input, V_{ADC} , and

(c) conduction losses in switch.

This test procedure is performed on both the single-channel and dual-channel switch. As $I_{L(NOM)}$ is lower when both channels are active on the dual-channel switch, the load current is varied over the range both with one and two active channels.

Temperature Test

In the temperature test, it is determined how much power is dissipated at nominal load current, and how much heat is generated.

The test procedure is as follows:

1. Connect power supply, load(s) and microcontroller or other controller.
2. Measure the temperature of the PROFET casing running the device at nominal load current over a longer time period.
 - (a) Does power dissipation increase with increased temperatures?
 - (b) Is there a need for cooling?

This test is performed on both the single-channel and dual-channel switches.

Destructive Test

In the destructive test it is determined whether the PROFET will be destroyed when running with load currents above the nominal for a longer period of time or if the PROFET's protective features will turn it off, and how fast this will happen.

The test procedure is as follows:

1. Connect power supply, load(s) and microcontroller or other controller.
2. Measure the temperature of the PROFET casing and how long the PROFET runs before being destroyed or switched off due to overcurrent and overtemperature protection, running the device at respectively 100%, 125%, 135%, 150%, 200% and 300% of nominal load current.
 - (a) Does the PROFET act like a fuse?

The test is performed only on the dual channel PROFET, as the wires will not be able to handle the test currents for the single-channel PROFET.

Test Results

The following subsections describe the results from the individual tests and the data processing that has been done. The load currents are measured using a N2783A Current

Probe powered by a N2779A Power Supply with serial number JP48040256, both devices from Agilent Technology, connected to a Teledyne Lecroy HD4024-MS oscilloscope with serial number LCRY4013N18645. Voltages such as V_{IS} , V_{ADC} and V_{DS} are measured using 34401A 6½ digit multimeters from Agilent Technology with serial numbers MY41005194 and MY41038906. The package temperature of the PROFETs is measured using a UNI-T UT58B multimeter with a thermal couple fixed to the package of the PROFET.

Results from Functional Test

With the switch off, the load current and load voltage was equal to zero, as expected. The sense pin voltage as well as ADC input voltage was measured under differing loads for both the single-channel and dual-channel PROFETs. These are plotted in Figure C.4 along with their respective curve fits. In Figure C.4a the current sense voltages are seen for the single and dual channel PROFETs with one active channel, while the current sense voltages for the dual channel PROFET with two active channels is plotted in Figure C.4b. As illustrated in the curves, the sense pin voltages and ADC voltages follow a linear trending curve.

The expected values of V_{IS} and V_{ADC} can be found as a function of the load current, I_L by the equations

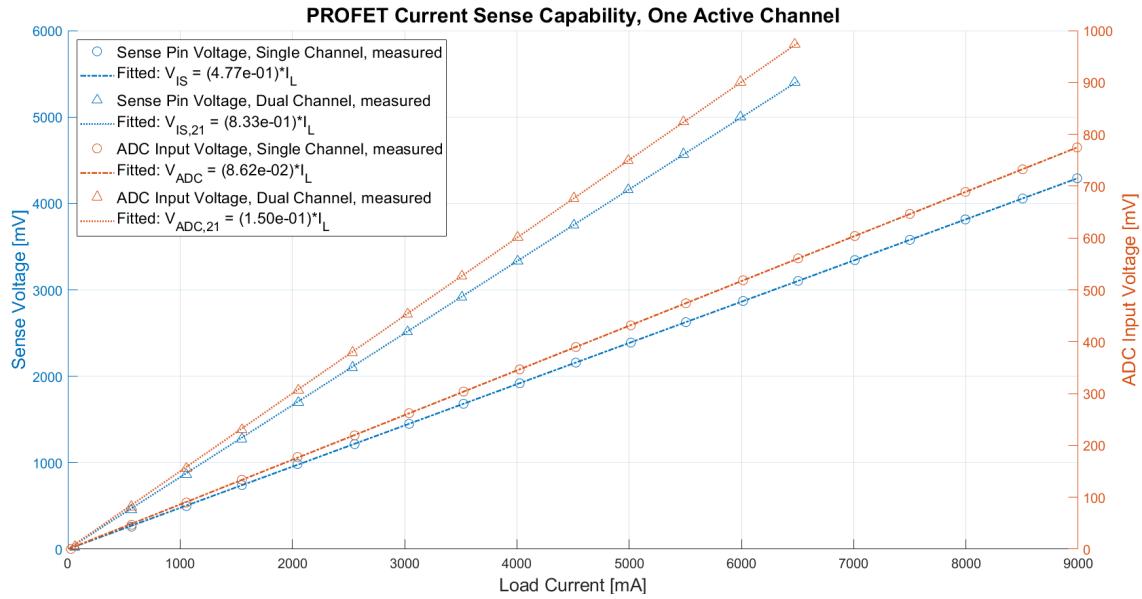
$$\begin{aligned} V_{IS} &= (R_{DIV} + R_{IS}) \cdot \frac{I_L}{k_{ILIS}} \\ V_{ADC} &= R_{IS} \cdot \frac{I_L}{k_{ILIS}} \end{aligned} \quad (\text{C.6})$$

Using these expected values, the Normalized Mean Square Error (NMSE) can be found of the measurements to evaluate the sense capabilities of the PROFET and sense circuit. The NMSE is the mean squared error normalized to the signal power, and is found using the formula:

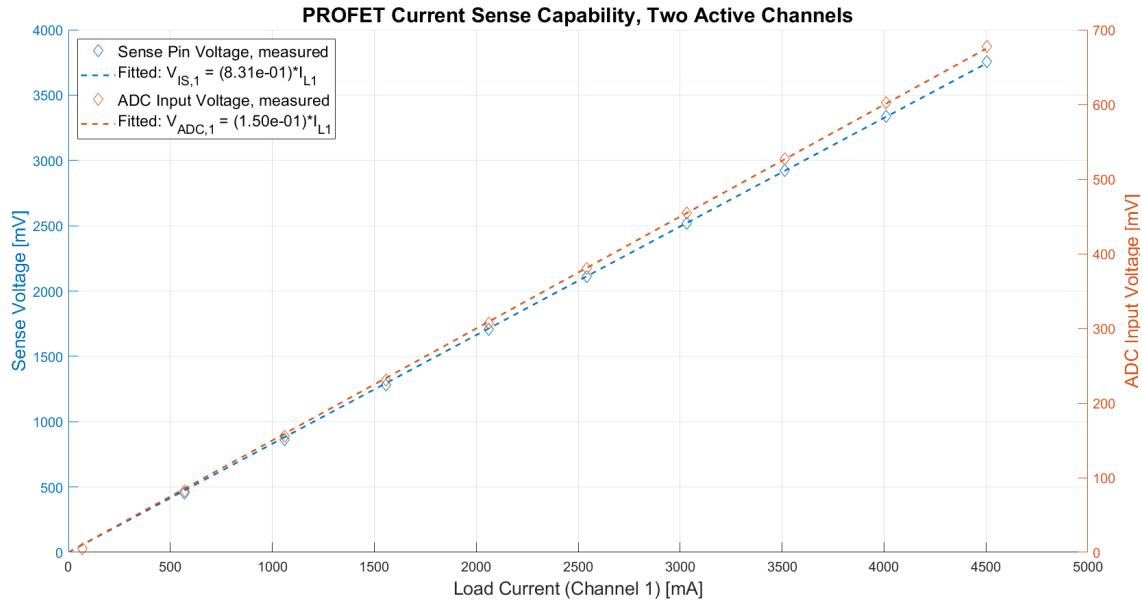
$$NMSE(Y, \hat{Y}) = \frac{MSE(Y, \hat{Y})}{VAR(Y)} = \frac{\frac{1}{N} \sum_{i=1}^N (\hat{Y}_i - Y_i)^2}{\frac{1}{N-1} \sum_{i=1}^N (Y_i - \mu)^2} \quad (\text{C.7})$$

where Y is the observed value, \hat{Y} is the expected value, and $\mu = \frac{1}{N} \sum_{i=1}^N Y_i$. Using the expected values and measurements of V_{IS} and V_{ADC} respectively gives an NMSE of $NMSE_{V_{IS}} = 1.2 \cdot 10^{-3}$ and $NMSE_{V_{ADC}} = 1.2 \cdot 10^{-3}$ for the single channel PROFET. The NMSEs for the dual channel PROFET with one active channel are $NMSE_{V_{IS}} = 1.3 \cdot 10^{-3}$ and $NMSE_{V_{ADC}} = 1.6 \cdot 10^{-3}$. The NMSEs for the dual channel PROFET with two active channels are $NMSE_{V_{IS}} = 1.1 \cdot 10^{-3}$ and $NMSE_{V_{ADC}} = 1.4 \cdot 10^{-3}$ respectively. This implies that the sense circuit and PROFETs current sense capability is satisfactory.

The curve fit is acquired using MATLABs *fit()* function using a proportional fit-type, $y = a \cdot x$. Taking the ratio of the gradients of the fits of the ADC input voltage and current sense pin voltage and comparing with the resistor divider ratio in Table C.1 it is seen that the fits are very good.



(a) Current sense capability for single- and dual-channel PROFETs with one active channel. Blue lines and markers relate to the sense pin voltage on the left y-axis, while orange lines and markers relate to the voltage measured at V_{ADC} on the right y-axis. Round markers and dot-dash lines relate to the single-channel PROFET, and up-pointing triangles and dotted lines relate to the dual-channel PROFET.



(b) Current sense capability for dual-channel PROFET with both channels active. Measurements were taken with a constant 2.12 A current flowing in channel 2.

Figure C.4: Plots of current sense voltages for both PROFETs under test.

Using the V_{IS} readings and the resistance on the current sense pin, the current sense pin's output current can be calculated:

$$I_{IS} = \frac{V_{IS}}{R_1 + R_2} \quad (\text{C.8})$$

where R_1 and R_2 are respectively the top and bottom resistor in the voltage divider on

the current sense pin, as seen in Figure C.1.

Test Condition	V_{ADC}/V_{IS}	Resistor Divider Ratio
Single-Channel PROFET	0.1806	0.1803
Dual-Channel PROFET, 1 active ch	0.1803	0.1803
Dual-Channel PROFET, 2 active chs	0.1803	0.1803

Table C.1: Comparison of Resistor Divider ratio on output of current sense pin and the ratio of the gradients of the fits on the current sense voltage data and ADC input voltage data.

Calculating I_{IS} for all data points for V_{IS} , k_{ILIS} can be calculated as a function of load current, I_L . These data points are plotted as a function of the measured load currents along with their respective curve fits in Figure C.5. The measured k_{ILIS} from the single active channel tests can be seen in Figure C.5a, while the measured k_{ILIS} from the test where both channels are active are shown in Figure C.5b. The data points are fitted with a curve of the type

$$y = a \cdot e^{b \cdot x} + c \cdot e^{d \cdot x} \quad (\text{C.9})$$

As is seen from the graphs, the curve is approximately constant for $I_L > 0.5 \text{ A}$ for the dual-channel PROFET and $I_L > 1 \text{ A}$, while for $I_L < 0.5 \text{ A}$ and $I_L < 1 \text{ A}$, respectively, the k_{ILIS} factor increases significantly for decreasing values of load current. This is consistent with the current sense accuracy shown in the PROFETs datasheets [1, p. 26][2, p. 27].

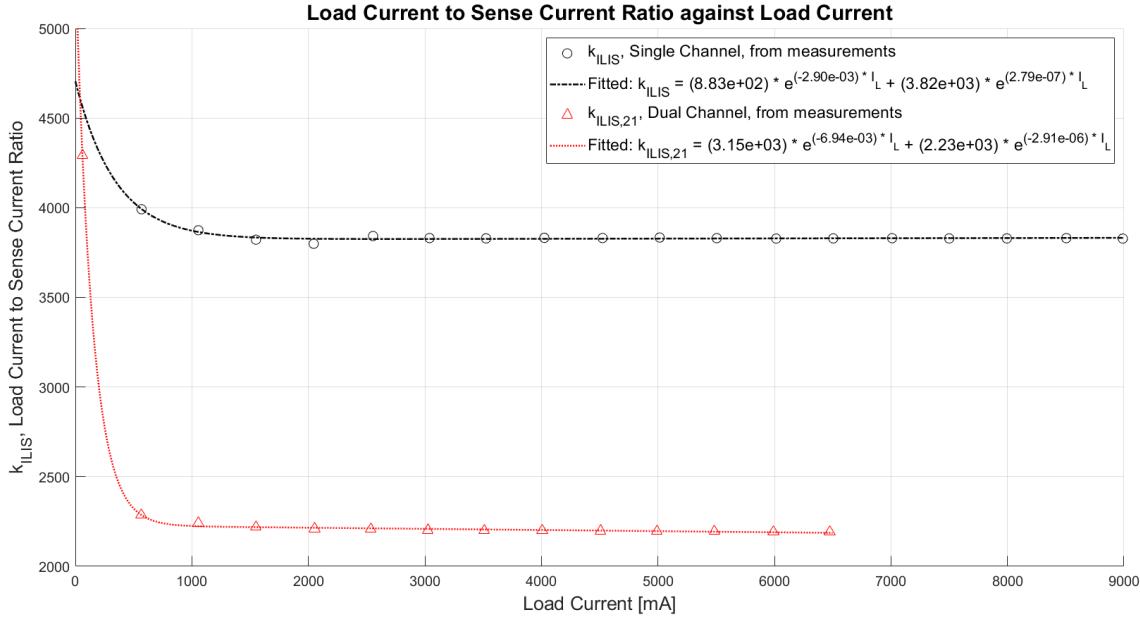
The first data point of each curve is taken at $\sim 0 \text{ A}$, but is measured to 28 mA for the single-channel PROFET measurement, 61 mA for the dual-channel PROFET with one active channel and 69.3 mA for the dual-channel PROFET with both channels active. The current measurements are taken on the oscilloscope with 2 A per division, which does not allow for a lot of accuracy on measurements of low current, as is also stated in the N2783B datasheet⁴. The load current measurements done at $< 100 \text{ mA}$ might therefore be very inaccurate, and is probably the cause of the deviation from the typical k_{ILIS} of the k_{ILIS} curves in Figure C.5.

For the single-channel PROFET, the k_{ILIS} factor flattens out at around 3830, which is a small deviation from the typical k_{ILIS} factor of 3900. For the dual-channel PROFET, the k_{ILIS} factor flattens out around 2200 in both the cases of one active channel and two active channels, which is also a small deviation from the nominal value, 2240.

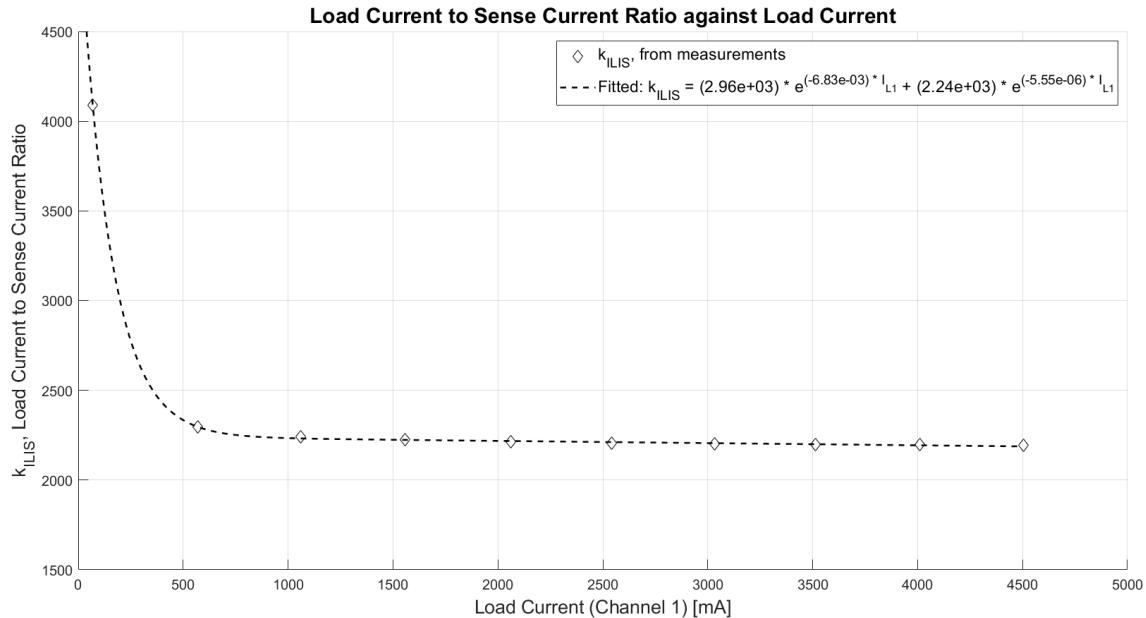
The dissipated power in the PROFETs are computed using measured values of the drain-source voltage for the PROFET and load current through the PROFET using the equation $P_{diss} = V_{DS} \cdot I_L$. Plots of the dissipated power as a function of load current can be seen in Figure C.6. Figure C.6a relates to the PROFET tests with one active channel, while Figure C.6b relates to the test with two active channels. As illustrated in the figures,

⁴<https://www.keysight.com/us/en/assets/7018-01536/data-sheets/5989-6432.pdf>

the curves are not linear as expected. This is most likely caused by R_{DS} increasing with increased temperatures, which will be further explored in the next subsection.

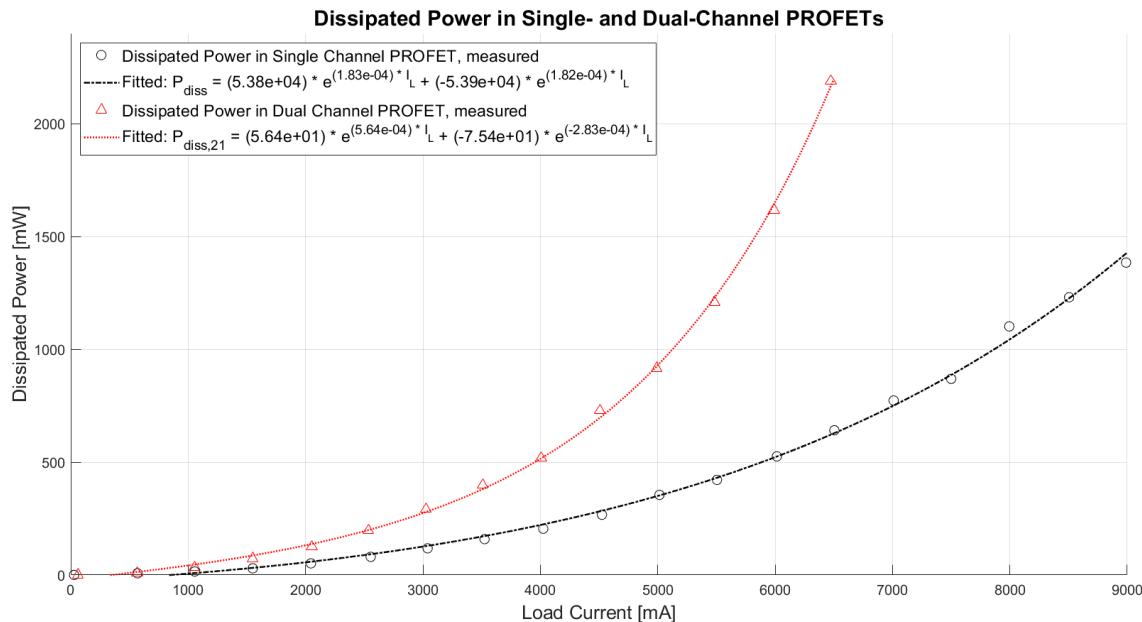


(a) Measured k_{ILIS} for single- and dual-channel PROFETs with one active channel. The black line and markers relate to the single-channel PROFETs k_{ILIS} as a function of load current. The red line and markers relate to the dual-channel PROFETs k_{ILIS} with one active channel as a function of load current.

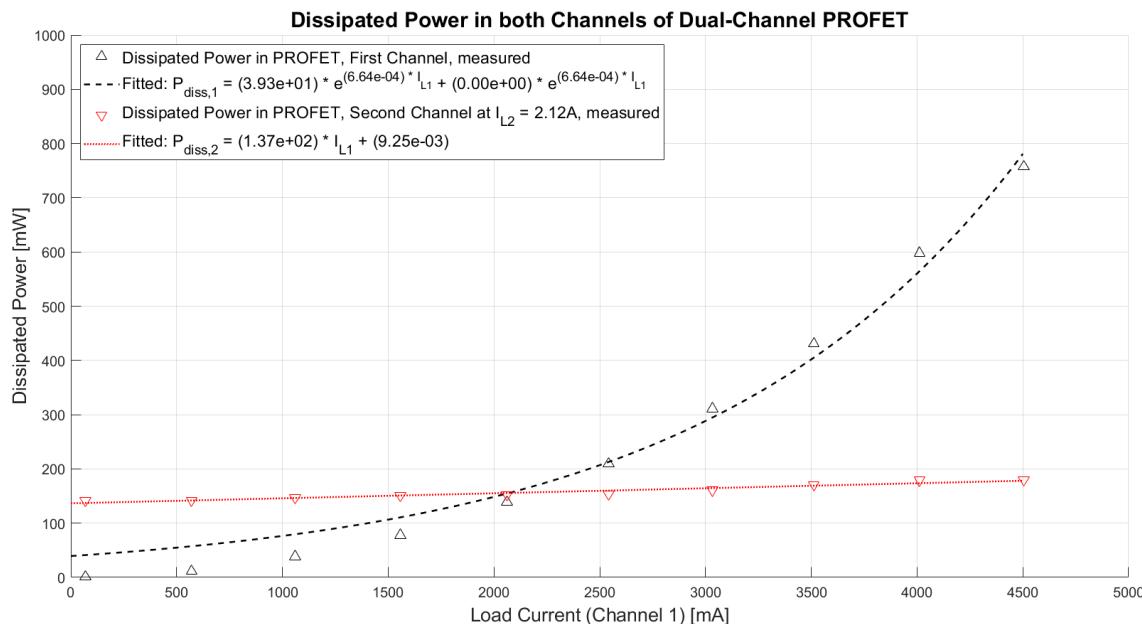


(b) Measured k_{ILIS} for dual-channel PROFET with two active channels. The measurements were taken with a constant 1.06 A current flowing in channel 2.

Figure C.5: Plots of computed k_{ILIS} as a function of load current for both PROFETs under test.



(a) Power dissipation for single- and dual-channel PROFETs with one active channel as a function of load current. The black line and markers relate to the single-channel PROFET and the red line and markers relate to the dual-channel PROFET



(b) Computed Power Dissipation for dual-channel PROFET with two active channels measured under the condition of a constant current of 2.12 A flowing in the second channel.

Figure C.6: Plots of dissipated power as a function of load current for PROFETs under test.

Results from Temperature Test

The tests was conducted by measuring the temperature of the device package over 12-15 minutes letting the nominal current flow through the PROFET. The package temperature is plotted against the time in Figure C.7 alongside the computed dissipated power in the PROFET. As is seen in the graphs, the dissipated power increases with the package temperature. This implies, the fact that the drain-source on-resistance of the PROFET channel increases with the temperature. The drain-source on-resistance of the PROFET channel is therefore computed using the formula

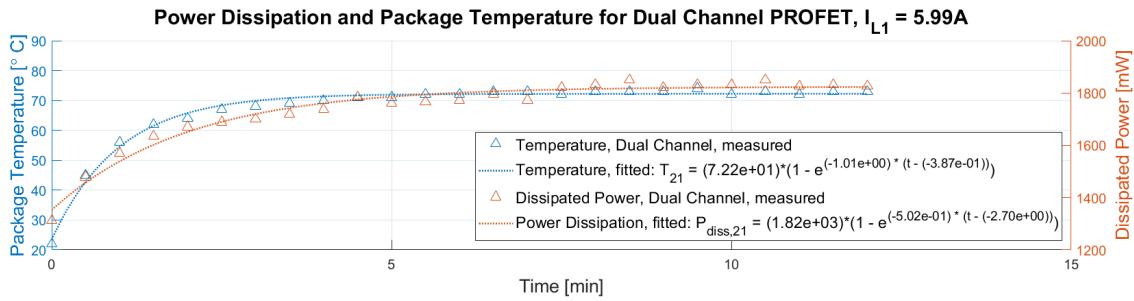
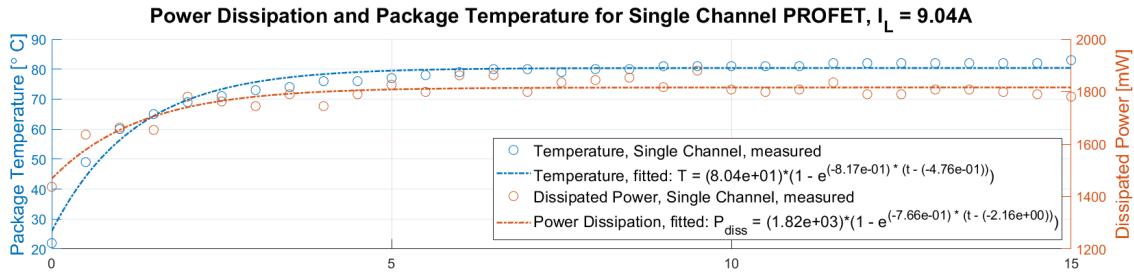
$$R_{DS(ON)} = \frac{P_{diss}}{I_L^2} \quad (\text{C.10})$$

This on-resistance is plotted against the package temperature in Figure C.8. According to the datasheet [1, p. 11][2, p. 12], $R_{DS(ON)}$ increases exponentially with the junction temperature. As it was not possible to measure the junction temperature, the package temperature is used instead. As illustrated in Figure C.8, the on-resistance of the PROFET channels increases seemingly exponentially in accordance with the exponentially increasing dissipated power with respect to load current as seen in Figure C.7.

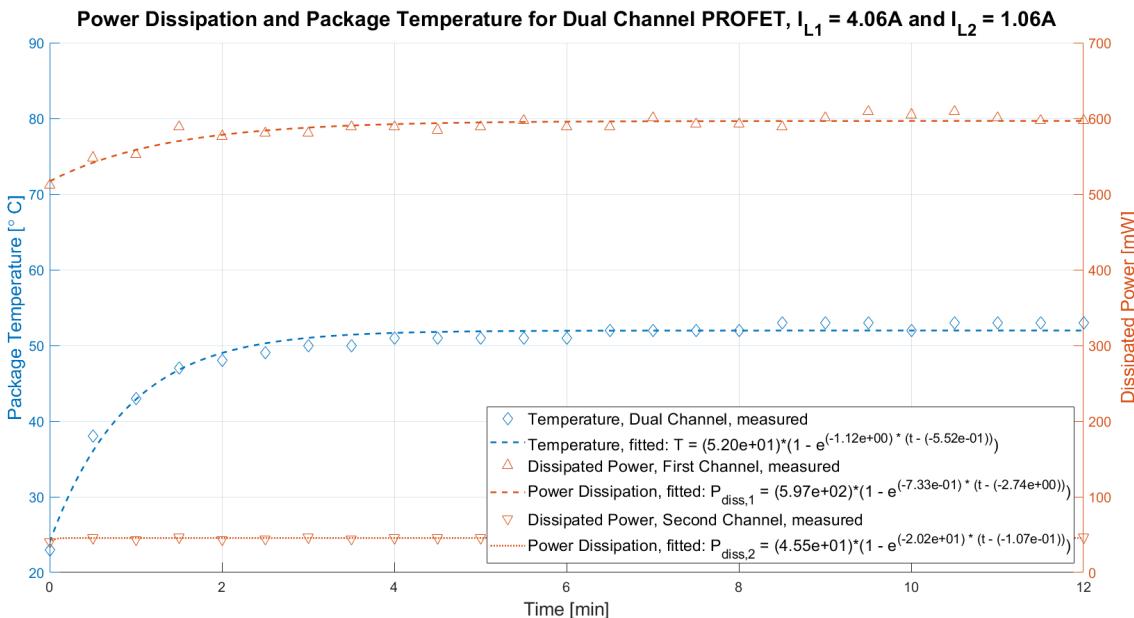
As seen in Figure C.7a, the single-channel PROFET's temperature plateaus around 80°C when running at nominal load current, while the dual-channel PROFET's package temperature plateaus around 70°C when running at nominal load current with a single active channel. In Figure C.7b it is seen that running the PROFET at sub-nominal load currents, the temperature will plateau at significantly lower values.

When the current flowing through the PROFET channels are below the nominal load current, there is no risk of the dissipated power increasing above the maximally allowed power dissipation, which is 1.6 W for the single-channel PROFET and 2.0 W for the dual-channel PROFET.

If the ambient temperature increases significantly, which is often the case when power is dissipated in an enclosure, cooling might be necessary when the load current approaches the nominal value for the PROFET.

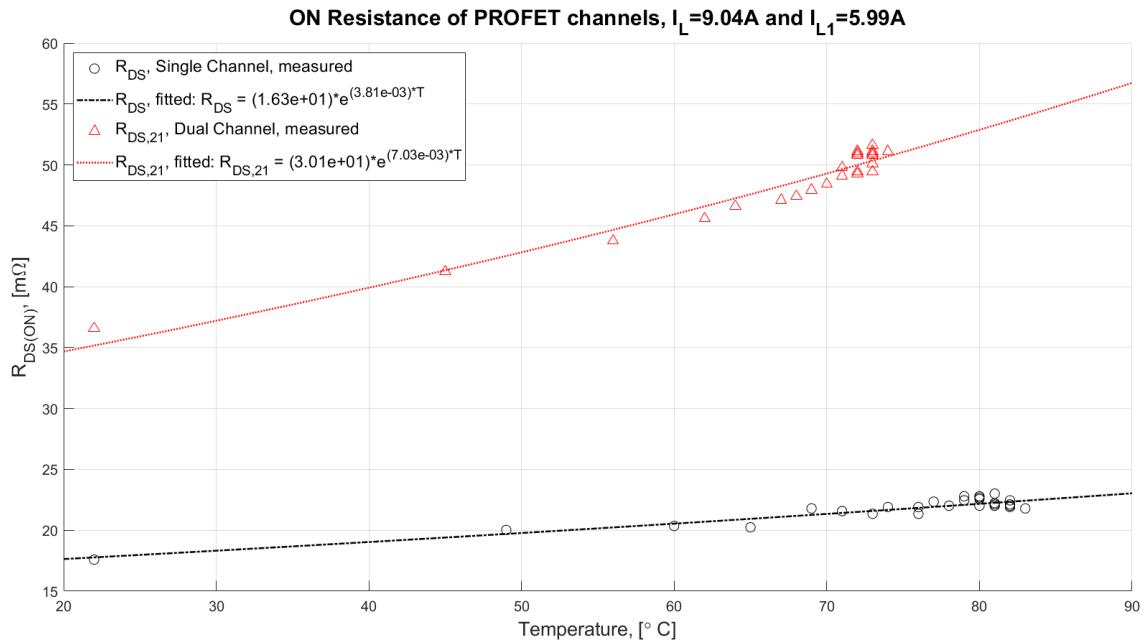


(a) Power dissipation and temperature for single- and dual-channel PROFETs with one active channel as a function of load current. The blue line and markers relate to the temperature on the left y-axis, while the orange line and markers relate to the dissipated power on the right y-axis. The round marker relates to the single-channel PROFET while the up-pointing triangle relates to the dual-channel PROFET.

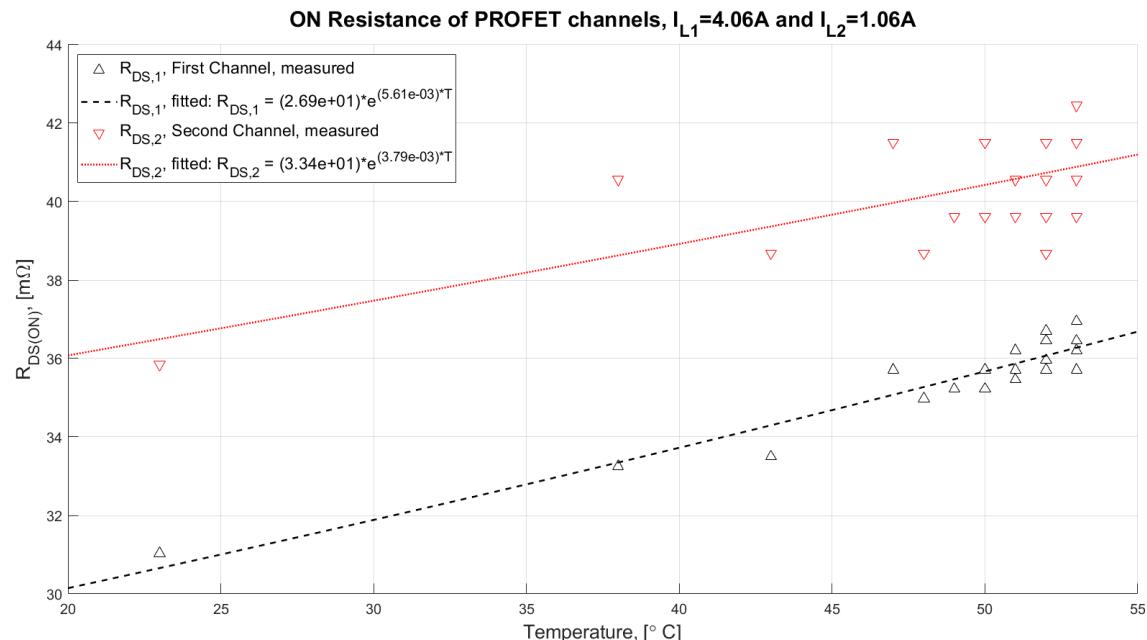


(b) Power Dissipation and temperature for dual-channel PROFET with two active channels. The diamond markers are measurements related to the temperature of the package, the up-pointing triangular markers are measurements relating to the first channel and the down-pointing triangular marker relates to the second channel.

Figure C.7: Plots of temperature and dissipated power as a function of time passed under load for the PROFETs.



(a) Power dissipation for single- and dual-channel PROFETs with one active channel as a function of load current. The black line and markers relate to the single-channel PROFET and the red line and markers relate to the dual-channel PROFET



(b) Computed Power Dissipation for dual-channel PROFET with two active channels measured under the condition of a constant current of 2.12 A flowing in the second channel.

Figure C.8: Plots of dissipated power as a function of load current for PROFETs under test.

Results of Destructive Test

In the destructive test, the dual-channel PROFET is exposed to load currents above the nominal load current. The currents used are at 110%, 125%, 135%, 150%, 200% and 300% of the nominal load current. The temperature of the casing is measured every 10 s and the time it takes for the PROFET to shut off is recorded. These results are shown in Table C.2.

Index Number / I_L	Time to shutdown
110% / 6.6 A	>300 s
125% / 7.5 A	38 s
135% / 8.1 A	17 s
150% / 9 A	9 s
200% / 12 A	2.5 s
300% / 18 A	1.5 s

Table C.2: Time until PROFET shuts down after beginning to conduct currents above the nominal load current.

The measurement of the time to shutdown for $I_L = 6.6\text{ A}$ was cut short at 300 s, as it had yet to shut off. As seen from the other measurements, the higher the load current, the shorter time it takes for the PROFET to shut down. These shutdown times can be compared to the time it takes a fuse to blow as taken from the fuse datasheets, respectively Littelfuse's 297 MINI series [4] and 157 NANO series [5]. Minimum and maximum opening times for two series of fuses are shown in Table C.3. As seen when comparing the values of Table C.2 and Table C.3, the opening time for the PROFETs are in range or similar to those of the fuses. Consequently, it is appropriate to use the PROFETs as resettable fuses.

Fuse Series	% of current rating	Opening Time Min/Max [s]
157 NANO	200%	- / 5
297 MINI	110%	360000 / -
297 MINI	135%	0.75 / 600
297 MINI	200%	0.15 / 5
297 MINI	350%	0.08 / 0.5

Table C.3: Minimum and Maximum opening times for fuses from Littelfuse's 157 NANO series and 297 MINI series.

Conclusion

In the functional test it was examined, whether the current sense capability of the PROFETs could measure the load current to an acceptable degree, how the load-current-to-sense-current ratio changed with load current and how big the conduction losses in the PROFETs were. As seen from the results, the voltage measured on the output of the current sense pin was proportional to the load current, though k_{ILIS} deviated a lot from the typical value at very low load currents. This deviation could also be a result of the inaccuracies of the measurement equipment. It was also seen that the conduction losses of the PROFET stayed below the absolute maximum value, when the load current was below the nominal value, even though the conduction loss increased exponentially with increasing temperatures.

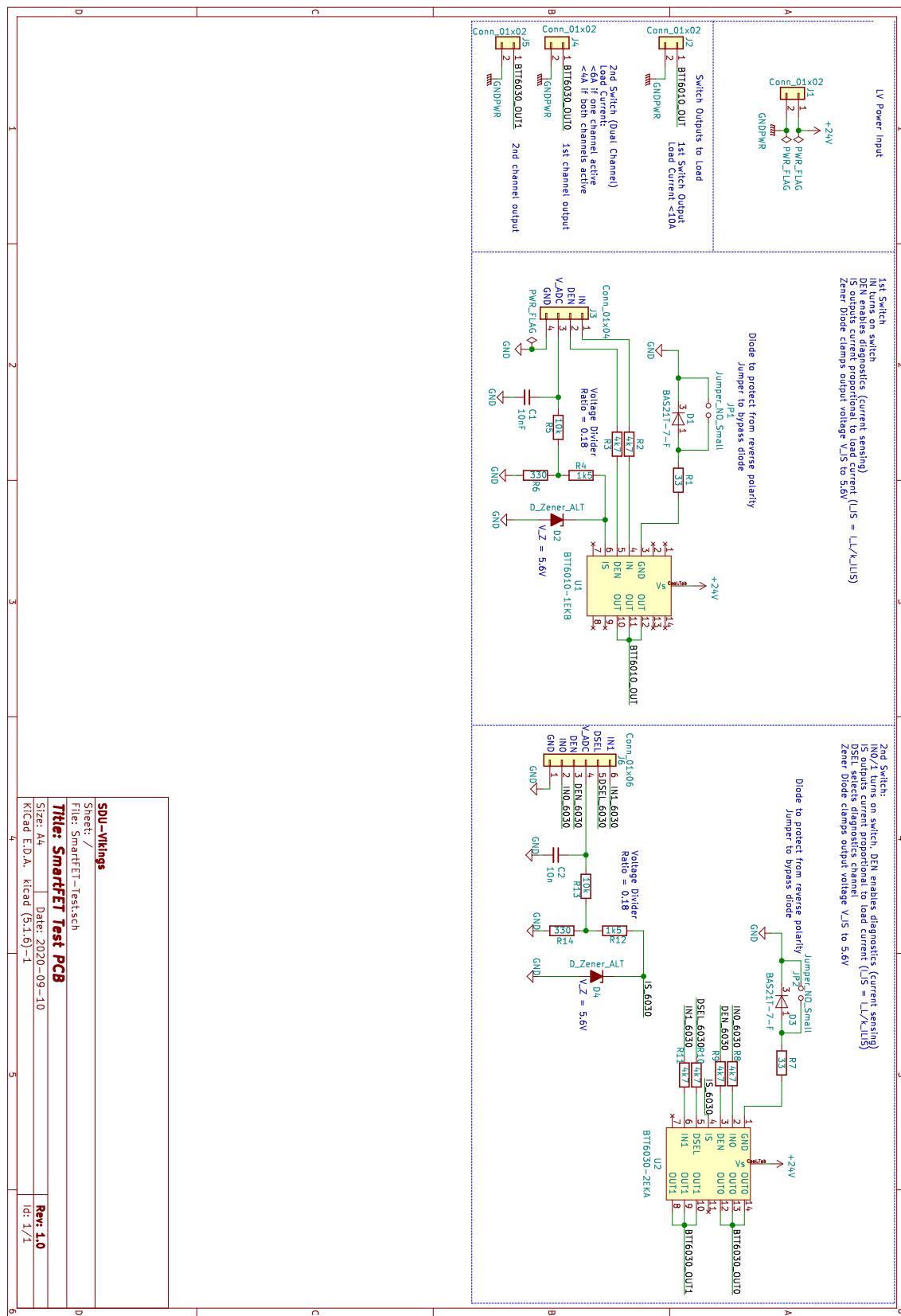
In the temperature test it was examined, whether the conduction losses increase with increasing temperatures and whether there is a need for cooling. From the results, it was seen that the on-resistance of the PROFET channel increased exponentially with the case temperature of the PROFET, which is in accordance with the conduction loss increasing exponentially with the load current. As long as the load current is kept well below the nominal value, there is no need for cooling, but if kept in an enclosure, there could be a need for cooling.

In the destructive test it was examined, whether the PROFET acts as a fuse when conducting currents exceeding the nominal value. After comparing with minimum and maximum opening times of a few fuses, it was concluded that the opening time of the switch in the PROFETs is similar to that of the fuses.

Literature

- [1] Infineon. PROFET™ +24V - BTT6010-1ERB, March 2019. https://www.infineon.com/dgdl/Infineon-BTT6010-1ERB-DS-v01_00-EN.pdf?fileId=5546d46269e1c019016a21e80b080d7a, last accessed 03/01-2021.
- [2] Infineon. PROFET™ +24V - BTT6030-2ERA, March 2019. https://www.infineon.com/dgdl/Infineon-BTT6030-2ERA-DS-v01_00-EN.pdf?fileId=5546d46269e1c019016a21fa44260d82, last accessed 03/01-2021.
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- [5] Littelfuse. NANO2 157 Fuse, March 2020. https://m.littelfuse.com/-/media/electronics/datasheets/fuses/littelfuse_fuse_157_datasheet.pdf.pdf, last accessed 03/01-2021.

D SmartFET Test Schematic



E NTC Test Journal

Functional Test of Bosch NTC M12 Thermistor

September 2020

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University of Southern Denmark

Purpose of tests

The tests within this journal will determine the limitations and practical applications of the Bosch NTC M12 thermistor to be used for measuring the temperature of liquids. The thermistor is rated for a maximum measurement current of 1 mA and maximum voltage of 5 V [1, p. 2]. A larger current through the component will result in larger power loss, heating the component and making the measurement inaccurate. By measuring the voltage drop, and by adjusting a series resistance, the effects of different currents on component temperature can be determined. This will aid in designing the series resistor to be used for best performance and output voltage. The output voltages can then be found and plotted, from which an equation for the temperature can be found. This can then be used in microprocessors to calculate the temperature after measuring the voltage with an Analog-to-Digital Converter.

Test Procedure

While a fully controlled climate is not accessible during the tests, it can reasonably be assumed that the ambient temperature in the laboratory conditions does not change significantly over the period of testing. Since the NTC is rated for 5 V, this will be applied to the thermistor with a TTI EL302RT power supply with serial number 371873. A 5 k Ω resistor will initially be put in series to limit the current to below 1 mA. The voltage across the resistor is then measured over a span of 15 minutes. If this increases, the NTC's resistance must have decreased, thus having an increased temperature. If this does not happen, the measurement current is not critically high, and the series resistor must be decreased and the test restarted. The smallest series resistor that does not result in self-heating should be used for optimal accuracy.

The MATLAB script NTCPosition.m shows inaccuracy calculations when placing the NTC either high-side or low-side. When including an ADC inaccuracy, the relative accuracy shown in Figure E.1 is calculated, which shows that placing the NTC high-side is more accurate in general. This is emphasized by using values at opposite ends of the tolerances for the NTC and series resistor.

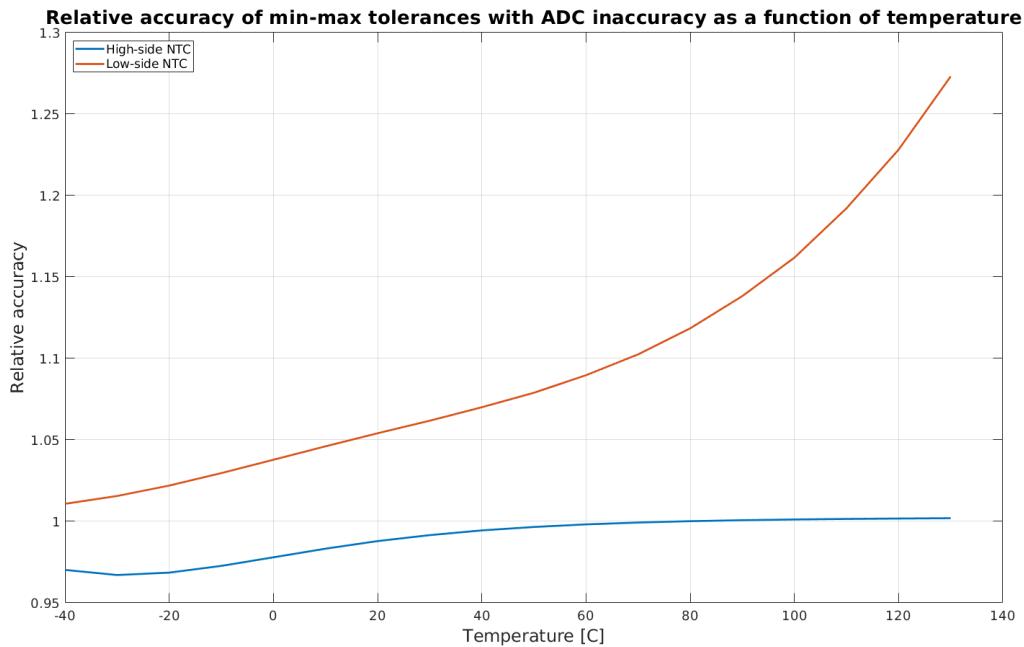


Figure E.1: Relative accuracy when placing NTC high-side (red) or low-side (blue) when including ADC conversion inaccuracy

The primary issue with this testing approach is the lack of controlled environment, as tests at higher ambient temperature are also of interest. If the measured liquid has a higher temperature, the thermistor's resistance decreases, increasing the current and potentially further increasing temperature, even if a series resistor is adequate at room temperature. This must be considered when drawing conclusions and calculating the series resistor to be used.

The test setup can be seen in Figure E.2. The voltmeter used is an Agilent Technology 34401A 6½ digit multimeter with serial number MY41005194.

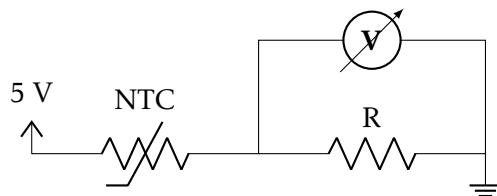


Figure E.2: Diagram of the setup used for testing the NTC self-heating

Test Results

The results of three tests are shown in Table E.1. The resistance of the NTC at the laboratory's ambient temperature is $2160\ \Omega$, which is used for calculating the current. The results show that the difference in voltage in the laboratory is minuscule, but existing, and for full sensor accuracy the self-heating needs to be limited.

The test with a $5\ k\Omega$ resistor shows a decrease in voltage, implying that the NTC was cooled. The reason for this is unknown, but may be due to inadequate rest time between touching a heated surface and testing. The phenomenon repeated in multiple $5\ k\Omega$ tests, and so may be responsible for an equal offset in tests with higher currents, but outweighed by the self-heating. The drifts are thus adjusted by removing this offset. Additionally, the difference in absolute voltage, as determined by the resistor value, also has an impact. As such, the best parameter for judging performance is drift as a percentage of starting voltage.

5 kΩ in series (0.7 mA)		2.4 kΩ in series (1.1 mA)		1.1 kΩ in series (1.53 mA)	
Time [Min.]	Voltage [V]	Time [Min.]	Voltage [V]	Time [Min.]	Voltage [V]
0	3.481	0	2.589	0	1.660
1	3.481	1	2.589	1	1.661
2	3.481	2	2.589	2	1.662
3	3.480	3	2.589	3	1.662
4	3.480	4	2.589	4	1.663
5	3.480	5	2.589	5	1.663
6	3.480	6	2.590	6	1.663
7	3.480	7	2.590	7	1.664
8	3.480	8	2.590	8	1.664
9	3.480	9	2.590	9	1.664
10	3.480	10	2.590	10	1.664
11	3.480	11	2.590	11	1.664
12	3.480	12	2.590	12	1.665
13	3.480	13	2.590	13	1.665
14	3.480	14	2.590	14	1.665
15	3.480	15	2.590	15	1.665
Diff.	-0.001 V		0.001 V		0.005 V
Adjusted diff.	0 V		0.002 V		0.006 V
Percentage	0%		0.07%		0.36%

Table E.1: Results of the tests of the Bosch NTC M12 thermistor with different currents

When this is taken into account, having a lower measurement current results in significantly less drift and higher accuracy. When including the NTC resistance, the best performance was with a resistance of $7.16\ k\Omega$. As the NTC resistance falls to $187\ \Omega$ at 100°C , a series resistance of around $7\ k\Omega$ is optimal for best accuracy across the entire temperature range. Increasing this value further would decrease power consumption and thus heating, but also become more susceptible to parasitic effects and noise. Using

a real resistor value of $6.98 \text{ k}\Omega$ with a 5 V supply results in the resistor voltages shown in Table E.2, which are to be converted in an ADC.

Temperature [°C]	NTC Resistance [Ω]	Output voltage [V]
-20	15462	1.56
-10	9397	2.13
0	5896	2.71
10	3792	3.24
20	2500	3.68
30	1707	4.02
40	1175	4.28
50	834	4.47
60	596	4.61
70	436	4.71
80	323	4.78
90	243	4.83
100	187	4.87

Table E.2: Output voltage of NTC sensor with 5 V supply at different temperatures

The ADC to be used for conversion is the MCP3208-CI [2], with an inaccuracy up to ± 11 LSB if all inaccuracies are summed up.

Plotting the measured temperature as a function of the resistor voltage proves a difficult task, as no simple function approximates the entire temperature range well. Instead, the ranges are split up, having one equation for 30 °C and below, equivalent to at most 4.02 V, and one equation above 30 °C.

The equation for voltages below 4.02 V is found as a linear function with an R^2 of 0.991:

$$T_C = 19.8 \cdot V_{in} - 52.3 \quad (\text{E.1})$$

In which V_{in} is the measured voltage. A graph showing calculated voltages as blue triangles and the equation's fit line in red is shown in Figure E.3.

For temperatures above 30 °C, a more complex function must be used. The most appropriate is a second order polynomial with an R^2 of 0.993, given by the equation

$$T_C = 2728 - 1261 \cdot V_{in} + 148 \cdot V_{in}^2 \quad (\text{E.2})$$

This equation requires a relatively large amount processing power. A simpler, but less accurate, exponential equation with $R^2 = 0.98$ is described by the equation

$$T_C = 0.0445 \cdot e^{1.57 \cdot V_{in}} \quad (\text{E.3})$$

The latter formula is inaccurate by at worst 5 °C, while the former is inaccurate by at worst 3 °C, but mostly below 2°C. The accuracy is important, and so the polynomial equation should be used. If processing time is critical, DSPs can likely be used for the calculation. A graph of both the calculated voltages as blue triangles and the polynomial equation's fit line in red is shown in Figure E.4.

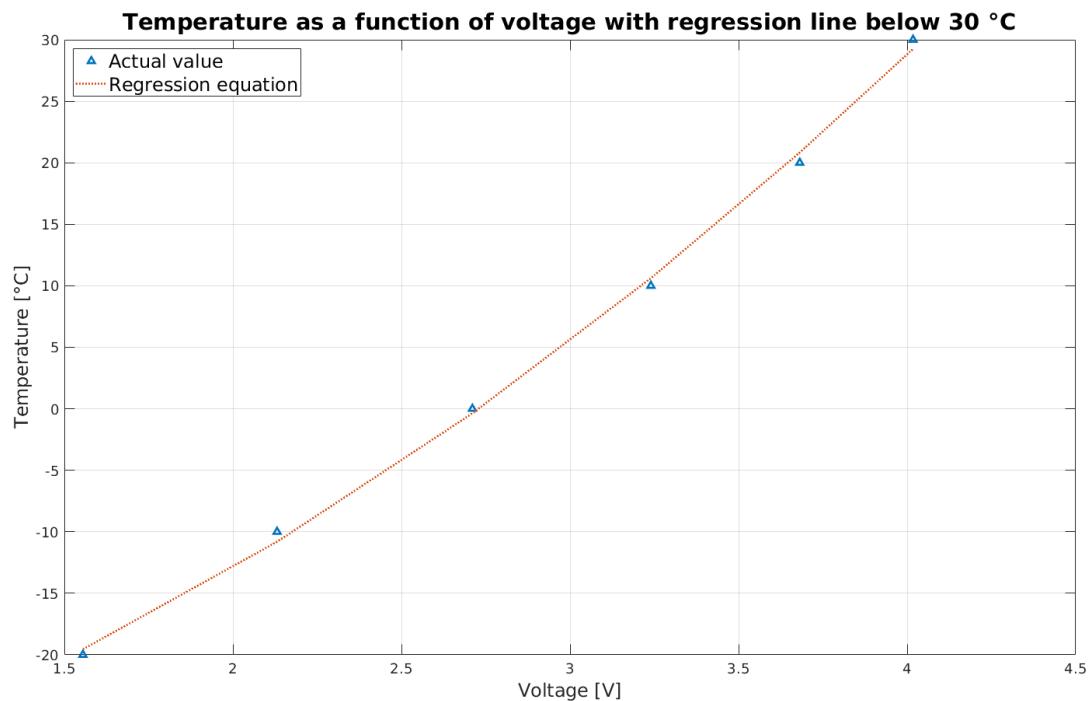


Figure E.3: Graph of voltages at low temperatures (blue) with regression line (red)

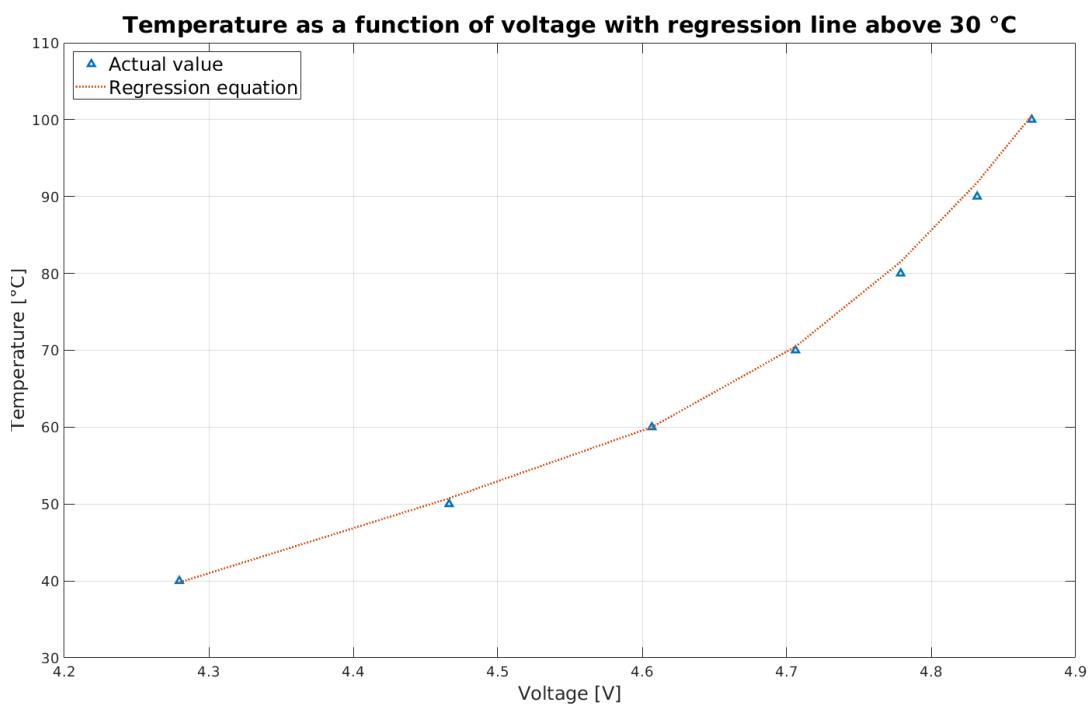


Figure E.4: Graph of voltages at high temperatures (blue) with regression line (red)

A worst-case analysis is performed in the MATLAB script NTCAcc.m by summing the absolute values of the NTC's resistance inaccuracy, the series resistor's 1% tolerance, the equation inaccuracy, and the ADC inaccuracy. It is assumed that the NTC's inaccuracy is constant below 25 °C and has a linear slope between 25 °C and 100 °C. This results in the temperature deviation shown in Figure E.5.

The inaccuracy generally rises with temperature due to the NTC and smaller voltage differences, but the equations also contribute to a large part of the deviation at times. If more complex equations are possible to execute in a timely manner, Equation E.4 can be used at or below 30 °C, while Equation E.5 can be used above 30 degrees. This results in accuracy to within 3°C at worst, but mostly below 1°C. The resulting total temperature deviation can be seen in Figure E.6, which peaks at 8°C at 90°C.

$$T_C = -35 + 6.11 \cdot V_{in} + 2.46 \cdot V_{in}^2 \quad (\text{E.4})$$

$$T_C = -29104 + 19644 \cdot V_{in} - 4424 \cdot V_{in}^2 + 333 \cdot V_{in}^3 \quad (\text{E.5})$$

In this case, the majority of the error is caused by the maximum NTC and ADC inaccuracy. In actual use, these inaccuracies are likely to be smaller or partially cancel each other out.

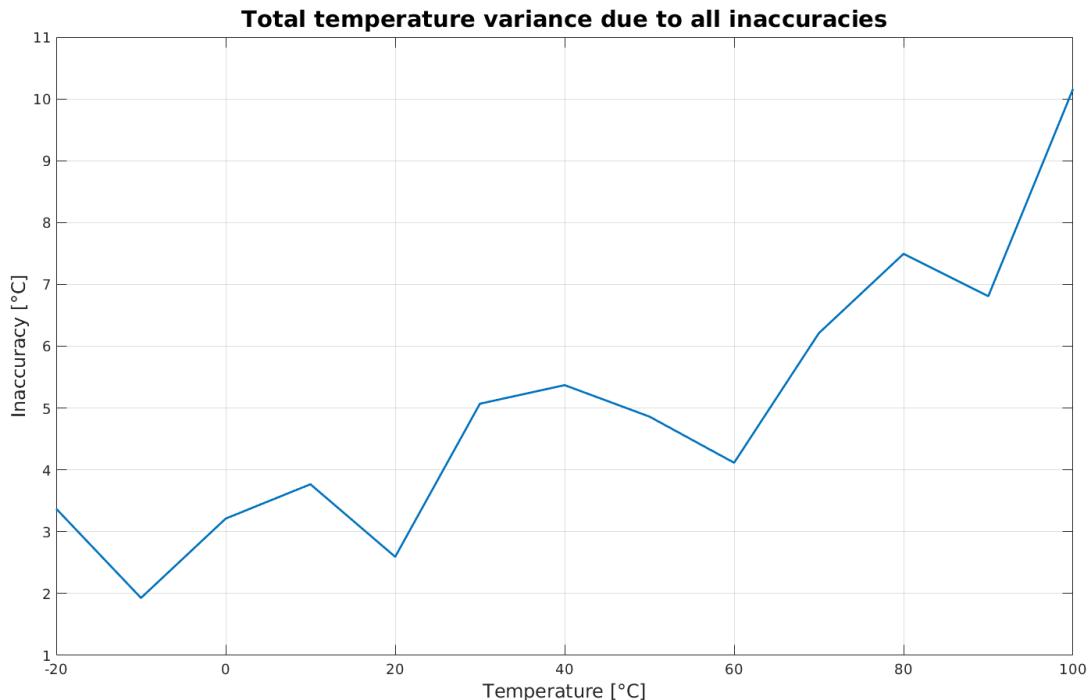


Figure E.5: Graph of worst-case temperature inaccuracy from -10 °C to 100 °C

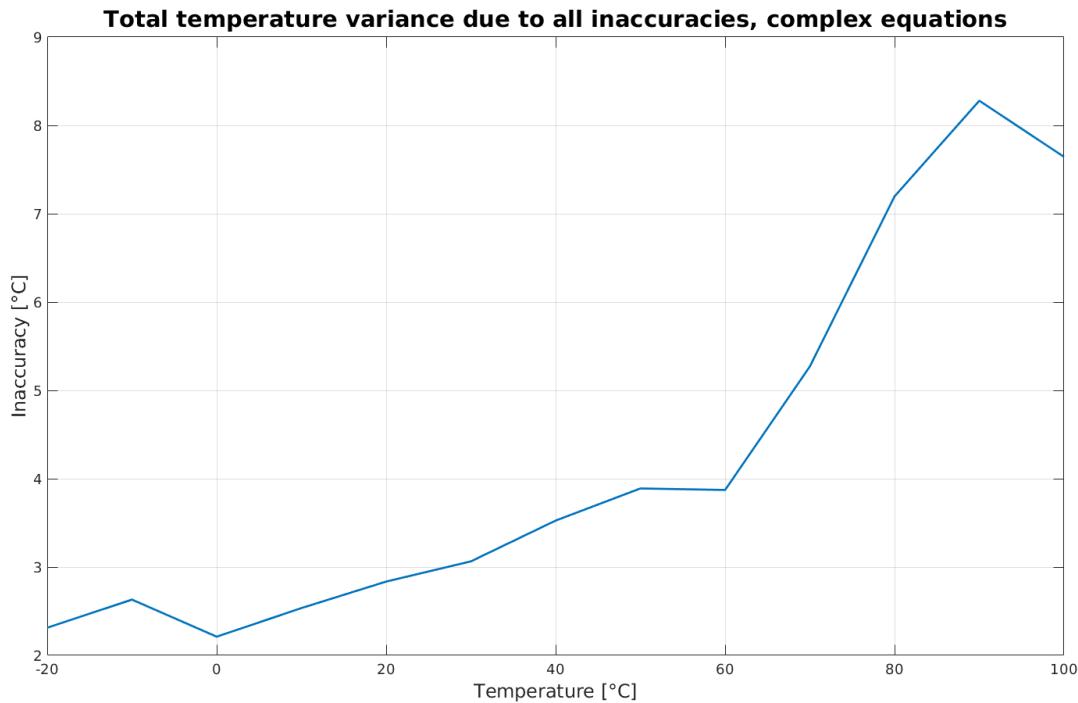


Figure E.6: Graph of worst-case temperature inaccuracy from -10 °C to 100 °C with complex equations

Conclusion

By calculating inaccuracies when placing the NTC either high-side or low-side, it is found that placing the NTC high-side results in highest degree of accuracy across the entire used temperature range.

Testing the NTC with various currents shows that the NTC experiences self-heating when a current larger than 1 mA is used. To ensure that the NTC current does not increase past this threshold at any temperature, a series resistor of 6.98 kΩ must be used.

Using the formulas shown in Equation E.4 and Equation E.5, and by including NTC inaccuracy, ADC inaccuracy, and resistor tolerances, calculations are made for finding the absolute temperature inaccuracy across the used range. This shows that the inaccuracy increases heavily above 60 °C due to the low voltage differences, being up to 8 °C deviation at 90 °C. Below 60 °C, the temperature deviation is 4 °C at most.

Literature

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- [2] Microchip. MCP3204/3208 12-bit A/D Converters with SPI Interface Datasheet, September 2008. <https://www.mouser.dk/datasheet/2/268/21298e-1101808.pdf>, last accessed 03/01-2021.

F Setup in Vivado and Vitis

The Programmable Logic within the FPGA of the Zynq-7020, as well as all interconnections between it and the Processing System, is specified in Xilinx Vivado Design Suite 2020.1. A block design is created, and Xilinx Intellectual Property (IP) blocks are dragged into it and connected automatically. The Zynq7 Processing System block is first configured using the PicoZed Tool Command Language (TCL) script supplied by Avnet, which has been added to the ZIP file. This ensures that clocks and memories are correctly configured. Afterwards, individual peripherals are enabled and assigned to MIO or EMIO as needed. Similarly, the XADC IP block is configured with needed inputs, settings, and alarms. General Purpose Input/Output (GPIO) pins in the PL are assigned with the Advanced Extensible Interface (AXI) GPIO block, which is connected to the Master AXI General Purpose Interconnect block. The AXI interfaces are used to connect the PS with the PL, and have a variety of speeds, directions, and widths. A system reset block is automatically added by Vivado to ensure correct functionality. All Zynq I/O connections are made in Vivado with ports and external ports. A full block diagram for all Master Controller FPGA hardware is shown in Appendix G.

With the design validated and synthesized, the specific package pins are chosen for each PL port in the I/O Planning layout, and voltages are specified. The Constraints Wizard must also be run to correctly configure clocks within the FPGA. The synthesis results in a constraints file used for the implementation. The implementation outputs design rule check and timing reports to ensure proper functioning. A bitstream is then generated, and a fixed hardware platform exported for software design in Xilinx Vitis 2020.1.

In Vitis, a new project platform is created using the hardware export file from Vivado and assigning it to a specific core on the PS. To use the setup from Vivado, including the PS peripherals, the xparameters.h file must be included in the C code header or source. Xilinx provides a large amount of baremetal drivers for the Zynq peripherals, which must similarly be included. The full list and links to the APIs can be found on the Xilinx wiki⁵. The list also includes libraries that can be used for more complex processing like file systems and ethernet protocols. All drivers use the setup from Vivado to correctly configure peripherals and settings, and for the most part implement all Zynq peripheral functions. Drivers have the option of being used by polling or using interrupts.

The drivers and libraries are implemented in a Board Support Package (BSP). By default Vitis contains two BSPs: the Standalone baremetal drivers, and the FreeRTOS interface drivers. Additional BSPs can be downloaded for a variety of Operating Systems (OS), allowing use of any OS for configuring and using peripherals on the Zynq.

⁵<https://xilinx-wiki.atlassian.net/wiki/spaces/A/pages/18841745/Baremetal+Drivers+and+Libraries>

G Master Controller Vivado Block Design

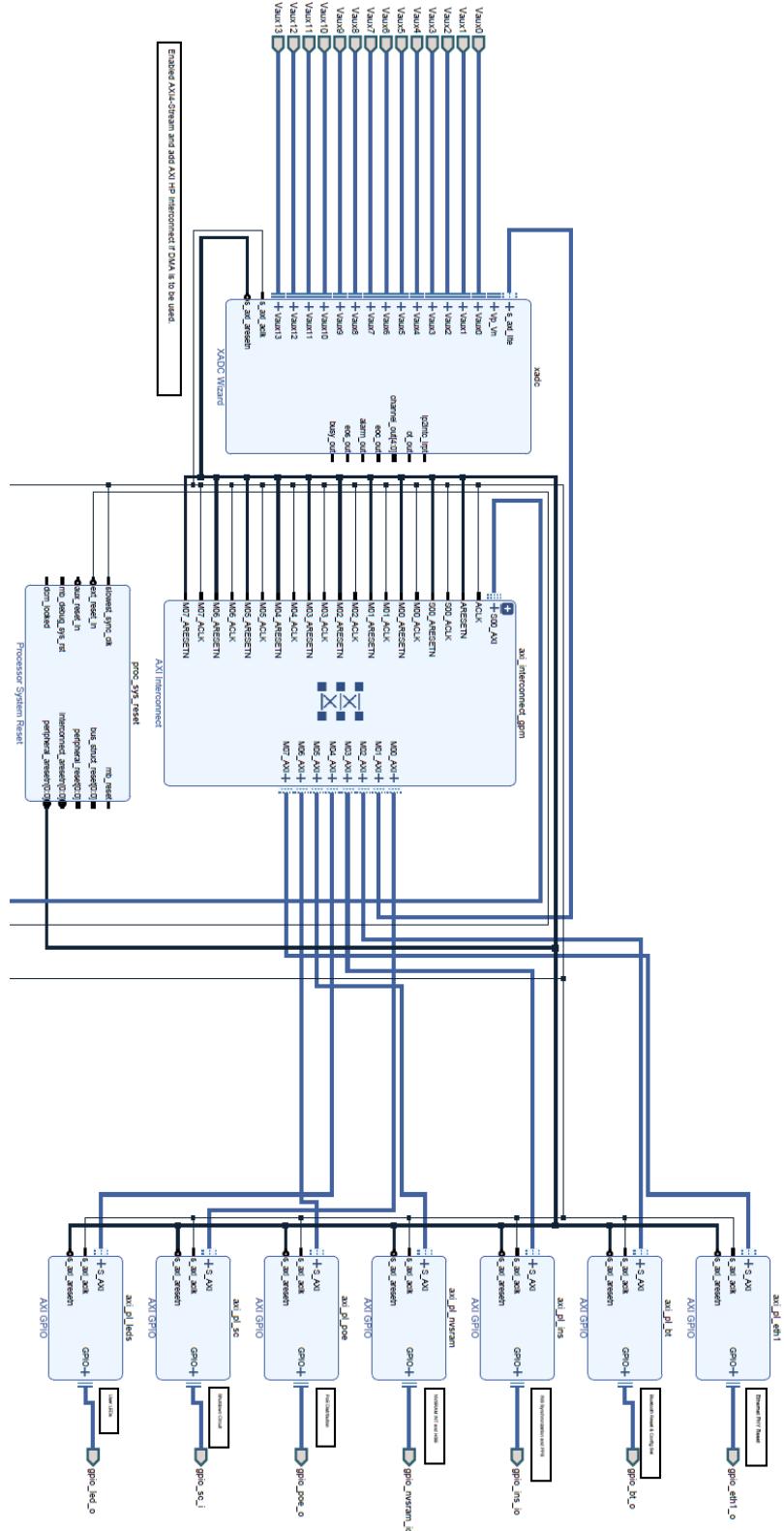


Figure G.1: Upper half of Master Controller Vivado block design

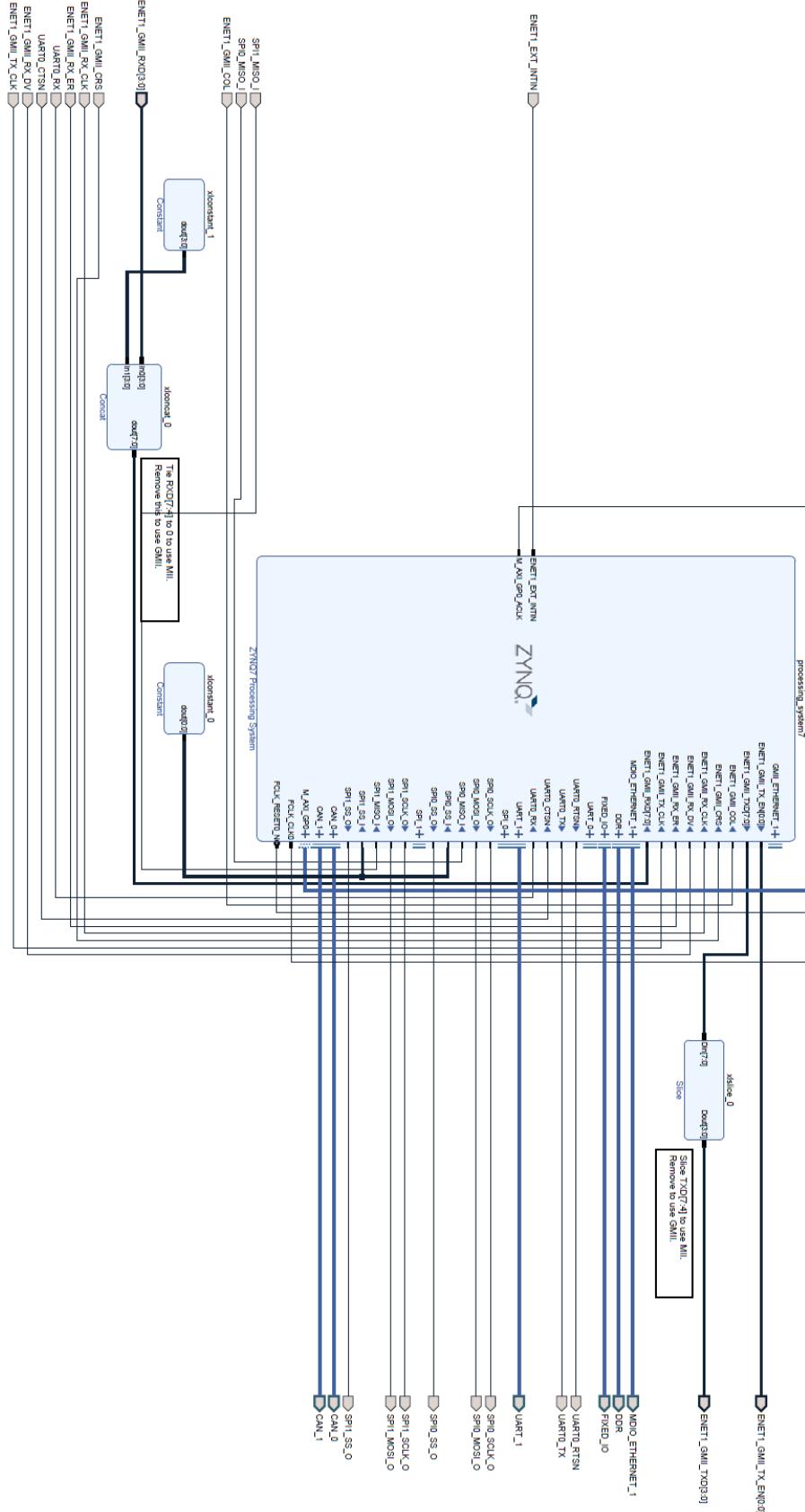


Figure G.2: Lower half of Master Controller Vivado block design

H Software Analysis

This appendix contains an analysis of the requirements for the application code, which will be executed by one of the Zynq PS cores. This draws inspiration from the X90-based Master Controller application documentation and a previous SDU-Vikings analysis made of Zynq software architecture. The analysis should not be seen as completed, but rather a starting point for a functioning application. Critical functions such as safety and protocols have not been specified to the degree needed for use.

Software Architecture

The Master Controller has a lot of responsibilities, meaning the Zynq has a lot of hardware it must interface with. The main responsibilities of the Master Controller is communication with other nodes in the vehicle, through CAN and Ethernet, measuring critical sensor values with the XADC, and distributing power to other nodes and actuators with the PROFETs that are controlled by digital signals from the GPIO. To enable efficient, standardised and easily readable code, drivers are used to access the peripherals used by the Zynq. To further hide the accesses to hardware, a Hardware Abstraction Layer (HAL) can be written and used to facilitate easier software writing. To facilitate software analysis, a Software Architecture Diagram is produced to show the hardware the Zynq must interface with, which peripherals it uses to interface with the individual devices, which drivers it uses to access the peripherals and which tasks these drivers are accessed within.

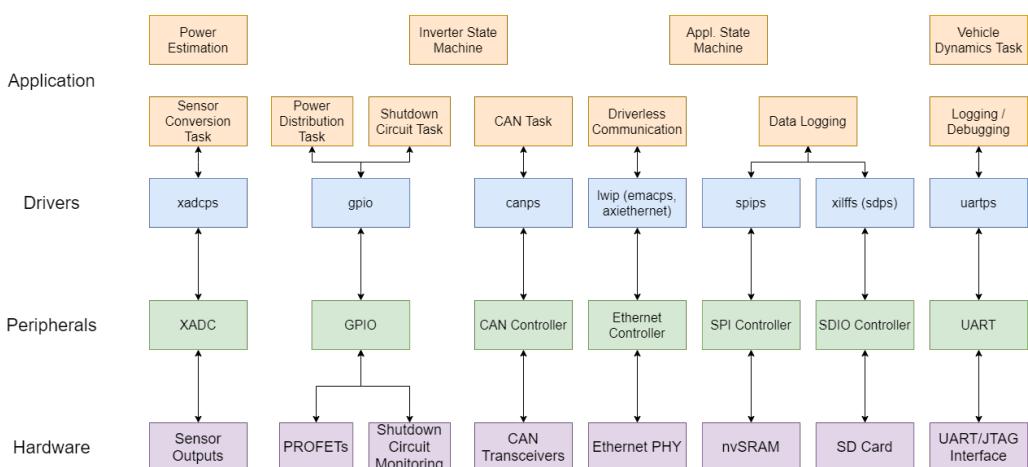


Figure H.1: Software Architecture Diagram for Master Controller

Figure H.1 illustrates the software architecture diagram for the Master Controller. The diagram consists of four layers, the highest layer (first) is the application layer. This layer consists of the tasks used in the Master Controller. The second layer is the driver layer, which consists of the drivers used by the tasks. The third layer is the peripheral layer, which lists the peripherals used to perform the Master Controllers tasks. The

fourth and last layer is the hardware layer, which depicts the hardware that the peripherals interface with. Interconnections between the various layers shows which blocks relate to each other. For example, the sensor conversion task uses the 'xadcps' driver to access the Zynq's XADC Interface which samples from the sensor outputs.

State Machine

The Formula Student ruleset contains specific rules for activating the car and putting it in drive mode, which must be followed by the Master Controller by using a state machine. The proposed state machine is shown in Figure H.2.

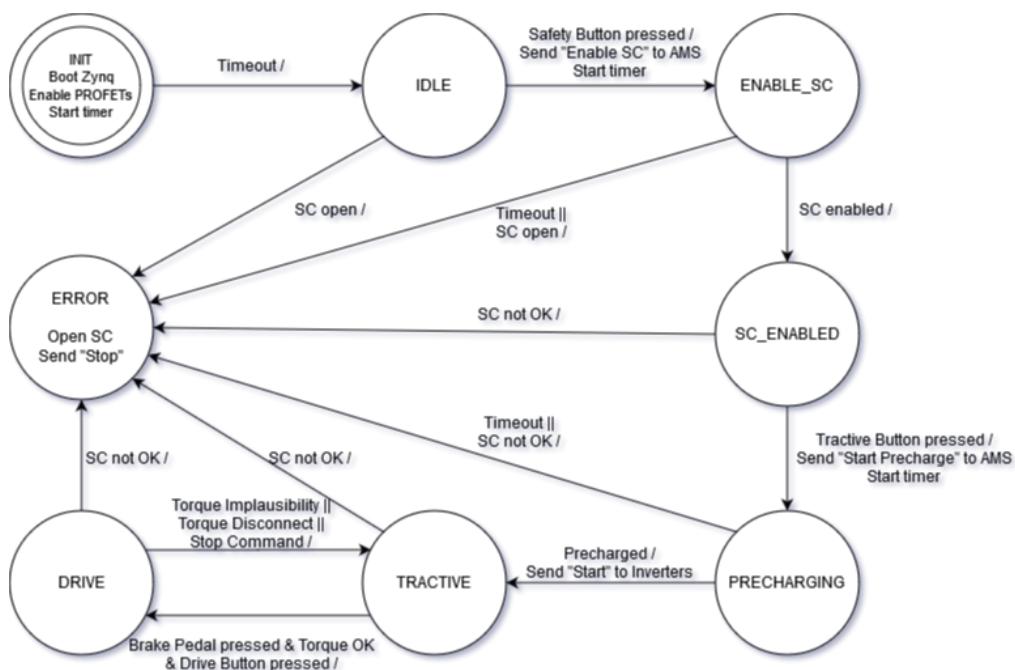


Figure H.2: Proposed State Machine for Master Controller software application

The application starts in the INIT state, where all Zynq peripherals are configured and relevant boot-up actions performed. This includes activating all other nodes by enabling the PROFETs. This allows currents and voltages to be measured immediately to confirm that nodes draw the expected power, as well as performing Coulomb counting. A timer is started which, when finished, transitions to the IDLE state. This is to ensure that all other nodes are also initialized.

Throughout all the following states, the Shutdown Circuit must be monitored regularly whenever the Master Controller is active. This means that the relays must be opened and Tractive System voltage drop to below 60 VDC / 25 VAC in less than five seconds. This is completed by transitioning to the ERROR state, which sends the "Stop" command through the CAN bus to the AMS and Inverters.

From the IDLE state, the CAN FIFO must continuously be checked for incoming communication, like AMS responses or Dashboard button presses. Outgoing communication is also needed for enabling pre-charging and starting the tractive system.

When the dashboard safety button is pressed, the AMS is instructed to enable the Shutdown Circuit within a set time in the ENABLE_SC state. If the timing is met, the application transitions to the SC_ENABLED state, where it awaits press of the dashboard tractive button. When this is registered, the "Start Precharge" command is sent to the AMS, and another timer is set for the PRECHARGING state. If the timing is met again, the "Start" command is sent to inverters. To enter DRIVE state, the brake pedal must be pressed, torque pedal must be OK, and the dashboard drive button must be pressed simultaneously.

In the DRIVE state, the analog sensor values must continuously be sampled at a fast rate. Rules for the actuators require activating the brake light when braking is detected and enabling the RTDS for 2 seconds when entering drive mode. The cooling system should additionally be always-on.

Diagnostics data must be stored on the SD card throughout all states. Relevant configuration parameters must be read from or written to the nvSRAM, for example when adjusting sensor values due to offsets.

Tasks

The continuous checks in the state machine will be performed by tasks with a specific timing. The task timings for the X90 Master Controller are specified in Table H.1.

Task Description	Cycle Time
CAN communication with AMS/Inverters	1 ms
Sensor measurement handling	10 ms
Actuator task	10 ms
Inverter state machine	10 ms
Vehicle dynamics control	10 ms
Other CAN communication	50 ms
Shutdown Circuit monitoring	50 ms
Data handling	50 ms
Application state machine	50 ms
Data logging	100 ms

Table H.1: Description of relevant X90 tasks and their associated cycle times

The cycle times of the tasks should for the most part be replicated in the Zynq Master Controller. The application state machine task in the X90 changes a global variable used by all other tasks, and has no other purpose. As it is the goal to avoid global variables,

the state machine can instead be handled by a central task, which instructs other tasks of their assignment while also executing other code.

To ensure that all timings satisfy the requirements, and to facilitate inter-task communication, a Real-Time Operating System should be implemented. The AMS, which is also based on the Zynq-7020, uses μ C/OS developed by Micrium for this. The RTOS has many important options, like preemption, queues, semaphores, and timers, while maintaining high performance and low size. The OS additionally has a tailored version for the Zynq-7020, which is confirmed to work well on the AMS, meaning it can easily be implemented. μ C/OS allows for as many tasks as needed, with individual priorities and timed suspension.

The initialization of the Zynq will take place in main, before the RTOS task scheduling is started. As mentioned, the application should be built around a central task containing the state machine. This task will inform other tasks of their purpose through messages in a queue. It will also gather data from the other tasks and use this data to change the state. If necessary. The power distribution task receives messages from the central task indicating when to turn specific PROFETs and relays on and off. The Shutdown Circuit is monitored every 50 ms, and the task will signal to the central task if any component is open, changing the state to ERROR.

A task must handle all the CAN communication with the AMS, shunt, inverters, dashboard, and sensor network. The task will send and receive messages depending on the state, as specified in the state machine. Received messages may require immediate action from the central task, or may be used for data handling. Messages to be sent are specified by the central task. The inverters' state machines are changed with CAN communication, but the task for finding new states is only run every 10 ms. For safety, if CAN messages are not received from any other node for a critical amount of time, the ERROR state must be entered.

Every 10 ms, the XADC must convert each of the sensor inputs. The values collected here must be adjusted for offset and gain errors, and then be used for data handling, like finding faults and errors. In case of errors, it must signal to the central task that an error has occurred, putting it in ERROR state. In any case, the data is put into a queue for the data logging task. Certain measurements may be needed for vehicle dynamics or Coulomb counting to estimate battery charge. The values are sent to the relevant tasks as well. Both these tasks are nice-to-have, and may eventually be implemented.

Eventually, a task will also be needed for Ethernet communication with the driverless computer. Received values are logged and sent to the central task.

As the secondary core must have access to all relevant data for the live-view, these values may be put into a protected shared memory by the data logging task, which is then read by the secondary core.

A task diagram showing all proposed tasks and the inter-task communication is shown in Figure H.3

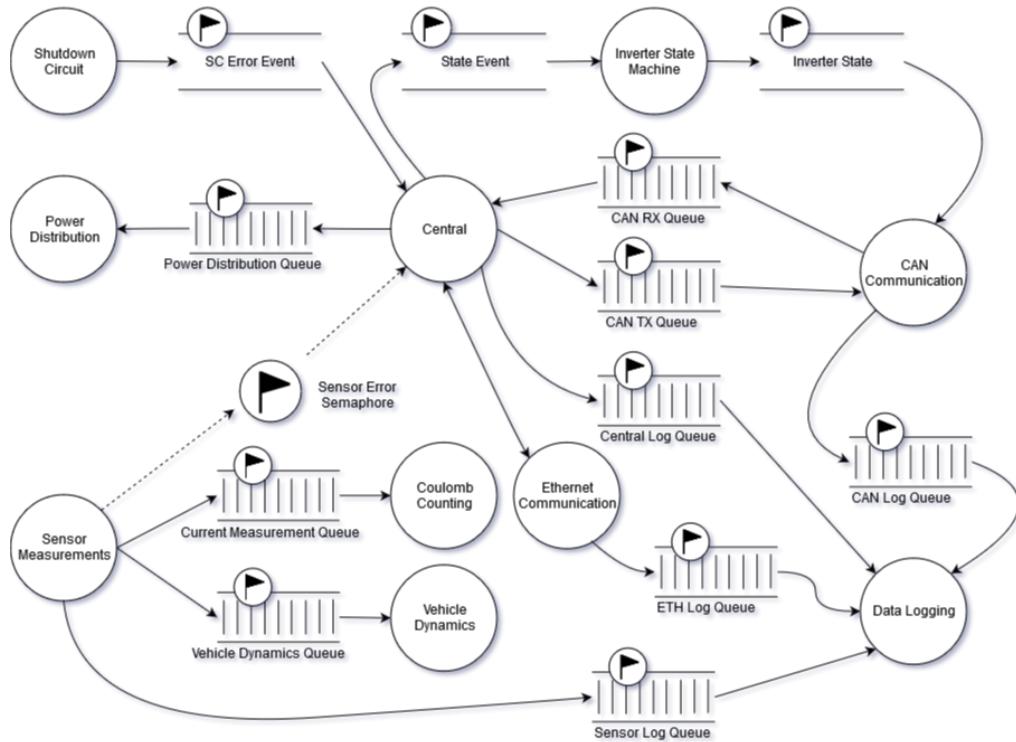


Figure H.3: Task diagram of proposed Master Controller tasks and their inter-task communication

I Results of XADC Tests

This appendix contains the results from tests performed in Section 44 to test XADC conversion accuracy, including filter and voltage divider inaccuracies.

AUX1 sensor voltage	Expected value	Converted value	Error
0.015 V	12	19	7 LSB
0.510 V	418	423	5 LSB
1.010 V	827	830	3 LSB
1.515 V	1241	1236	-5 LSB
2.010 V	1646	1644	-2 LSB
2.520 V	2064	2056	-8 LSB
3.010 V	2465	2464	-1 LSB
3.315 V	2715	2663	-52 LSB

Table I.1: Results of AUX1 conversion tests

AUX3 sensor voltage	Expected value	Converted value	Error
0.015 V	12	18	6 LSB
0.510 V	418	424	6 LSB
1.010 V	827	831	4 LSB
1.510 V	1237	1237	0 LSB
2.010 V	1646	1648	2 LSB
2.505 V	2052	2061	9 LSB
3.010 V	2465	2466	1 LSB
3.515 V	2879	2874	-5 LSB
4.020 V	3292	3285	-7 LSB
4.520 V	3702	3691	-11 LSB
5.010 V	4095	4095	0 LSB

Table I.2: Results of AUX3 conversion tests

AUX8 sensor voltage	Expected value	Converted value	Error
0.020 V	16	20	4 LSB
0.520 V	426	424	-2 LSB
1.025 V	839	830	-9 LSB
1.525 V	1249	1238	-11 LSB
2.020 V	1654	1647	-7 LSB
2.520 V	2064	2062	-2 LSB
3.020 V	2473	2464	-9 LSB
3.520 V	2883	2873	-10 LSB
4.020 V	3292	3281	-11 LSB
4.515 V	3698	3687	-11 LSB
5.010 V	4095	4095	0 LSB

Table I.3: Results of AUX8 conversion tests

AUX9 sensor voltage	Expected value	Converted value	Error
0.015 V	12	14	2 LSB
0.510 V	418	424	6 LSB
1.010 V	827	829	2 LSB
1.515 V	1241	1238	-3 LSB
2.015 V	1650	1648	-2 LSB
2.520 V	2064	2060	-4 LSB
3.010 V	2465	2466	1 LSB
3.315 V	2715	2665	-50 LSB

Table I.4: Results of AUX9 conversion tests

J Results of Current Measurement Tests

This appendix contains the results from tests performed in Section 44 to test current measurement accuracy.

PROFET 2 current	Converted value	Calculated current	Error
0.00 A	7	0.005 A	5 mA (-%)
0.277 A	413	0.274 A	-3 mA (-1.08%)
0.470 A	724	0.480 A	10 mA (2.13%)
0.763 A	1176	0.780 A	17 mA (2.23%)
0.945 A	1475	0.978 A	33 mA (3.49%)
1.247 A	1935	1.283 A	36 mA (2.89%)
1.440 A	2239	1.484 A	44 mA (3.05%)
1.804 A	2693	1.785 A	-19 mA (-1.05%)
1.997 A	2992	1.983 A	-14 mA (-0.70%)
2.291 A	3442	2.282 A	-9 mA (-0.39%)
2.493 A	3751	2.486 A	-7 mA (-0.28%)
2.690 A	4021	2.665 A	-25 mA (-0.93%)

Table J.1: Results of PROFET 2 current measurement test

PROFET 3 current	Converted value	Calculated current	Error
0.00 A	8	0.005 A	5 mA (-%)
0.260 A	377	0.250 A	-10 mA (-3.85%)
0.447 A	673	0.446 A	-1 mA (-0.22%)
0.740 A	1120	0.742 A	2 mA (0.27%)
0.934 A	1423	0.943 A	9 mA (0.96%)
1.248 A	1885	1.250 A	2 mA (0.16%)
1.443 A	2190	1.452 A	9 mA (0.62%)
1.730 A	2643	1.752 A	22 mA (1.27%)
1.916 A	2942	1.950 A	34 mA (1.77%)
2.213 A	3395	2.250 A	37 mA (1.67%)
2.412 A	3708	2.458 A	46 mA (1.91%)
2.613 A	3995	2.648 A	35 mA (1.34%)

Table J.2: Results of PROFET 3 current measurement test

PROFET 4 current	Converted value	Calculated current	Error
0.00 A	7	0.005 A	5 mA (-%)
0.643 A	346	0.646 A	3 mA (0.47%)
1.422 A	798	1.490 A	68 mA (4.78%)
2.108 A	1172	2.188 A	80 mA (3.80%)
2.910 A	1608	3.002 A	92 mA (3.16%)
3.488 A	1924	3.592 A	104 mA (2.98%)
4.166 A	2294	4.283 A	117 mA (2.81%)
4.846 A	2668	4.981 A	135 mA (2.79%)
5.532 A	3043	5.681 A	149 mA (2.69%)
6.232 A	3417	6.379 A	147 mA (2.36%)
6.902 A	3792	7.080 A	178 mA (2.58%)
7.396 A	4015	7.496 A	100 mA (1.35%)

Table J.3: Results of PROFET 4 current measurement test

RTDS current	Converted value	Calculated current	Error
0 mA	1164	2.5 mA	2.5 mA (-%)
1 mA	1620	3.5 mA	2.5 mA (250%)
2 mA	2080	4.5 mA	2.5 mA (125%)
3 mA	2528	5.5 mA	2.5 mA (83.3%)
4 mA	2987	6.5 mA	2.5 mA (62.5%)
5 mA	3435	7.5 mA	2.5 mA (50%)
6 mA	3888	8.5 mA	2.5 mA (41.7%)
7 mA	4013	8.7 mA	1.7 mA (24.2%)

Table J.4: Results of RTDS current measurement test

Brake Light current	Converted value	Calculated current	Error
0 mA	174	2.8 mA	2.8 mA (-%)
6 mA	540	8.8 mA	2.8 mA (46.7%)
12 mA	906	14.7 mA	2.7 mA (22.5%)
18 mA	1265	20.6 mA	2.6 mA (14.4%)
24 mA	1622	26.4 mA	2.4 mA (10%)
30 mA	1980	32.2 mA	2.2 mA (7.3%)
36 mA	2323	37.8 mA	1.8 mA (5%)
42 mA	2675	43.5 mA	1.5 mA (3.6%)
48 mA	3022	49.2 mA	1.2 mA (2.5%)
54 mA	3363	54.7 mA	0.7 mA (1.3%)
60 mA	3704	60.3 mA	0.3 mA (0.5%)
66 mA	4015	65.3 mA	-0.7 mA (-1.1%)

Table J.5: Results of Brake Light current measurement test

K Zynq Pins used by PicoZed

Table K.1 contains the Zynq pins used for connecting to modules on the PicoZed. These are all PS pins, with the specific MIO connection specified in the table. The USB/ULPI signals are not used by the Master Controller. Supply and RAM pins are excluded from the table. See the Zynq Pinout Guide for specification⁶.

Zynq Pin	MIO	Description
A7	1	Quad-SPI Chip Select
A5	6	Quad-SPI Serial Data Clock
B8	2	Quad-SPI Data 0
D6	3	Quad-SPI Data 1
B7	4	Quad-SPI Data 2
A6	5	Quad-SPI Data 3
D5	8	Quad-SPI Feedback
B17	22	Ethernet 0 Receive Clock
D13	21	Ethernet 0 Receive Control
D11	23	Ethernet 0 Receive Data 0
A16	24	Ethernet 0 Receive Data 1
F15	25	Ethernet 0 Receive Data 2
A15	26	Ethernet 0 Receive Data 3
A19	16	Ethernet 0 Transmit Clock
F14	21	Ethernet 0 Transmit Control
E14	17	Ethernet 0 Transmit Data 0
B18	18	Ethernet 0 Transmit Data 1
D10	19	Ethernet 0 Transmit Data 2
A17	20	Ethernet 0 Transmit Data 3
C11	53	Ethernet 0 Management Data
C10	52	Ethernet 0 Management Clock
A14	32	USB Data 0
D15	33	USB Data 1
A12	34	USB Data 2
F12	35	USB Data 3
C16	28	USB Data 4
A10	37	USB Data 5
E13	38	USB Data 6
C18	39	USB Data 7
A11	36	USB Clock
C13	29	ULPI DIR
C15	30	ULPI STP
E16	31	ULPI NXT
D8	7	USB Reset

Table K.1: List of Zynq pins in use for PicoZed modules

⁶https://www.xilinx.com/support/documentation/user_guides/ug865-Zynq-7000-Pkg-Pinout.pdf

L JX Header Connection Overview

JX1 Pin	Net Name	Zynq Pin	JX1 Pin	Net Name	Zynq Pin
1	JTAG_TCK	F9	51	GND	#N/A
2	JTAG_TMS	J6	52	GND	#N/A
3	JTAG_TDO	F6	53	EXP_15	T20
4	JTAG_TDI	G6	54	EXP_13	V20
5	NC	#N/A	55	EXP_16	U20
6	JTAG_SRST	B10	56	EXP_14	W20
7	NC	F11	57	VIN	#N/A
8	FPGA_DONE	R11	58	VIN	#N/A
9	ETH1_RX_DV	R19	59	VIN	#N/A
10	ETH1_RX_ER	T19	60	VIN	#N/A
11	UART0_CTS	T11	61	EXP_4P	Y18
12	UART0_RXD	T12	62	EXP_17	V16
13	UART0_RTS	T10	63	EXP_4N	Y19
14	UART0_TXD	U12	64	EXP_18	W16
15	GND	#N/A	65	GND	#N/A
16	GND	#N/A	66	GND	#N/A
17	CAN0_TX	U13	67	EXP_5	R16
18	ETH1_INT	V12	68	NC	T17
19	CAN0_RX	V13	69	EXP_6	R17
20	ETH1_TX_EN	W13	70	NC	R18
21	GND	#N/A	71	GND	#N/A
22	GND	#N/A	72	GND	#N/A
23	CAN1_TX	T14	73	EXP_7P	V17
24	ETH1_COL	P14	74	NC	W18
25	CAN1_RX	T15	75	EXP_7N	V18
26	ETH1_CRS	R14	76	NC	W19
27	GND	#N/A	77	GND	#N/A
28	GND	#N/A	78	VCCO_34	N19
29	INS_SYNC_I	Y16	79	VCCO_34	N19
30	ETH1_MDIO	W14	80	VCCO_34	N19
31	INS_SYNC_O	Y17	81	EXP_8	N17
32	ETH1_MDC	Y14	82	NC	P15
33	GND	#N/A	83	EXP_9	P18
34	GND	#N/A	84	NC	P16
35	UART1_TXD	T16	85	GND	#N/A
36	ETH1_PHY_RST	V15	86	GND	#N/A
37	UART1_RXD	U17	87	NC	U7
38	INS_PPS	W15	88	NC	T9
39	GND	#N/A	89	NC	V7
40	GND	#N/A	90	NC	U10
41	EXP_11	U14	91	NC	V8
42	NC	U18	92	PL_ALIVE	T5
43	EXP_12	U15	93	NC	W8
44	NC	U19	94	PL_LED	U5
45	GND	#N/A	95	GND	#N/A
46	GND	#N/A	96	GND	#N/A
47	EXP_1P	N18	97	V_0_P	K9
48	EXP_2	N20	98	DX_0_P	M9
49	EXP_1N	P19	99	V_0_N	L10
50	EXP_3	P20	100	DX_0_N	M10

JX2 Pin	Net Name	Zynq Pin	JX2 Pin	Net Name	Zynq Pin
1	SDIO1_DATA0	E9	51	GND	#N/A
2	SDIO1_DATA1	E8	52	GND	#N/A
3	SDIO1_DATA2	C5	53	/SC_BOTS_Mon	H16
4	SDIO1_DATA3	C8	54	XADC_AUX4_P	J18
5	SDIO1_CLK	D9	55	/SC_Inertia_Mon	H17
6	SDIO1_CMD	C6	56	XADC_AUX4_N	H18
7	Cool_FET_In	E6	57	VIN	#N/A
8	SDIO1_CD	B5	58	VIN	#N/A
9	NC	R10	59	VIN	#N/A
10	3V3_EN	#N/A	60	VIN	#N/A
11	PG_MODULE	C7	61	/SC_Cockpit_Mon	G17
12	VIN	#N/A	62	XADC_AUX12_P	F19
13	NC	G14	63	/SC_Supply_Mon	G18
14	NC	J15	64	XDAC_AUX12_N	F20
15	GND	#N/A	65	GND	#N/A
16	GND	#N/A	66	GND	#N/A
17	XADC_AUX0_P	C20	67	XADC_AUX13_P	G19
18	XADC_AUX8_P	B19	68	XADC_AUX5_P	J20
19	XADC_AUX0_N	B20	69	XADC_AUX13_N	G20
20	XADC_AUX8_N	A20	70	XADC_AUX5_N	H20
21	GND	#N/A	71	GND	#N/A
22	GND	#N/A	72	GND	#N/A
23	XADC_AUX1_P	E17	73	XADC_AUX6_P	K14
24	BT_Reset	D19	74	/SC_Left_Mon	H15
25	XADC_AUX1_N	D18	75	XADC_AUX6_N	J14
26	BT_ConfigSel	D20	76	/SC_Right_Mon	G15
27	GND	#N/A	77	GND	#N/A
28	GND	#N/A	78	VCCO_35	C19
29	XADC_AUX9_P	E18	79	VCCO_35	C19
30	NC	F16	80	VCCO_35	C19
31	XADC_AUX9_N	E19	81	EXP_10P	N15
32	NC	F17	82	XADC_AUX7_P	L14
33	GND	#N/A	83	EXP_10N	N16
34	GND	#N/A	84	XADC_AUX7_N	L15
35	XADC_AUX3_P	L19	85	GND	#N/A
36	XADC_AUX2_P	M19	86	GND	#N/A
37	XADC_AUX3_N	L20	87	/SC_FL_Mon	M14
38	XADC_AUX2_N	M20	88	/SC_RR_Mon	K16
39	GND	#N/A	89	/SC_FR_Mon	M15
40	GND	#N/A	90	/SC_RL_Mon	J16
41	XADC_AUX10_P	M17	91	GND	#N/A
42	XADC_AUX11_P	K19	92	GND	#N/A
43	XADC_AUX10_N	M18	93	SPI0_CS0	Y12
44	XADC_AUX11_N	J19	94	/SC_TSMS_Mon	V11
45	GND	#N/A	95	SPI0_CLK	Y13
46	GND	#N/A	96	NVSRAM_HSB	V10
47	NC	L16	97	SPI0_MO	V6
48	NC	K17	98	VCCO_13	T8
49	NC	L17	99	SPI0_MI	W6
50	PoE_FET_In	K18	100	NVSRAM_INT	V5

JX3 Pin	Net Name	Zynq Pin	JX3 Pin	Net Name	Zynq Pin
1	NC	#N/A	51	ETH_MD1_P	#N/A
2	NC	#N/A	52	ETH_MD2_P	#N/A
3	NC	#N/A	53	ETH_MD1_N	#N/A
4	NC	#N/A	54	ETH_MD2_N	#N/A
5	NC	#N/A	55	GND	#N/A
6	GND	#N/A	56	GND	#N/A
7	NC	#N/A	57	ETH_MD3_P	#N/A
8	NC	#N/A	58	ETH_MD4_P	#N/A
9	NC	#N/A	59	ETH_MD3_N	#N/A
10	NC	#N/A	60	ETH_MD4_N	#N/A
11	NC	#N/A	61	GND	#N/A
12	GND	#N/A	62	GND	#N/A
13	NC	#N/A	63	NC	#N/A
14	NC	#N/A	64	SNET_FET_In	B9
15	NC	#N/A	65	GND	#N/A
16	NC	#N/A	66	TSC_FET_In	B13
17	GND	#N/A	67	NC	#N/A
18	GND	#N/A	68	NC	#N/A
19	NC	#N/A	69	NC	#N/A
20	NC	#N/A	70	NC	#N/A
21	NC	#N/A	71	GND	#N/A
22	NC	#N/A	72	GND	#N/A
23	GND	#N/A	73	ETH1_RXD3	Y7
24	GND	#N/A	74	ETH1_TXD3	Y9
25	NC	#N/A	75	ETH1_RXD2	Y6
26	NC	#N/A	76	ETH1_TXD2	Y8
27	NC	#N/A	77	GND	#N/A
28	NC	#N/A	78	GND	#N/A
29	GND	#N/A	79	ETH1_RXD1	W10
30	NC	#N/A	80	ETH1_TXD1	U9
31	NC	#N/A	81	ETH1_RXD0	W9
32	NC	#N/A	82	ETH1_TXD0	U8
33	NC	#N/A	83	GND	#N/A
34	PS_ALIVE	C17	84	GND	#N/A
35	GND	#N/A	85	ETH1_RX_CLK	W11
36	SNET_INV34_Sel	A9	86	NC	#N/A
37	Brake_SSR_In	E12	87	ETH1_TX_CLK	Y11
38	Dash_AMS_Sel	B15	88	NC	#N/A
39	RTDS_SSR_In	F13	89	GND	#N/A
40	INV34_FET_In	B14	90	GND	#N/A
41	INV12_FET_In	D16	91	NC	#N/A
42	AMS_FET_In	B12	92	NC	#N/A
43	Dash_FET_In	D14	93	NC	#N/A
44	TSC_INV12_SEL	C12	94	NC	#N/A
45	VCCO_13	T8	95	GND	#N/A
46	VCCO_13	T8	96	GND	#N/A
47	ETH_PHY_LED0	#N/A	97	NC	#N/A
48	ETH_PHY_LED1	#N/A	98	NC	#N/A
49	GND	#N/A	99	NC	#N/A
50	GND	#N/A	100	NC	#N/A

M CMC Connection Overview

Grey Connector				
Column \ Row	4	3	2	1
H	LVS+	LVS-	LVS+	LVS+
G	Pump 1+	Pump 2+	LVS-	LVS-
F	Pump 1-	Pump 2-	LV Ground	SC_TSMS_I
E	SC_RR_I	SC_RL_O	SC_RL_I	SC_TSMS_O
D	SC_RR_O	SC_FL_I	SC_FL_O	SC_FR_I
C	SC_Left_I	SC_Right_O	SC_Right_I	SC_FR_O
B	SC_Left_O	SC_Inert_I	SC_Inert_O	SC_BOTS_I
A	SC_Supply	SC_Cock_O	SC_Cock_I	SC_BOTS_O

Table M.1: Overview of connections from the grey-marked CMC connector

Black Connector				
Column \ Row	1	2	3	4
A	TP1+	TP1-	TP2-	TP2+
B	TP1S	TP2S	BP1-	BP1+
C	BP1S	BP2S	BP2-	BP2+
D	INS_UART_TX	INS_GPS_PPS	INS_RESET	INS-
E	INS_UART_RX	INS_SYNC_I	INS_SYNC_O	INS+
F	CAN1H_IN	CAN1H_OUT	CAN1L_IN	CAN1L_OUT
G	CAN0H_IN	CAN0H_OUT	CAN1GND_IN	CAN1GND_OUT
H	CAN0L_IN	CAN0L_OUT	CAN0GND_IN	CAN0GND_OUT

Table M.2: Overview of connections from the black-marked CMC connector

Brown Connector				
Column \ Row	1	2	3	4
A	AMS+	AMS-	Dashboard-	Dashboard+
B	Sensor Net+	Sensor Net-	RTDS-	RTDS+
C	Inverter 3/4+	Inverter 3/4-	Fan 1-	Fan 1+
D	TSC+	TSC-	Fan 2-	Fan 2+
E	Inverter 1/2+	Inverter 1/2-	Brake Light-	Brake Light+
F	Expansion 22	LV Ground	LV Ground	LV Ground
G	Expansion 18	Expansion 19	Expansion 21	Expansion 20
H	Expansion 7	Expansion 8	Expansion 11	Expansion 17
J	Expansion 5	Expansion 6	Expansion 9	Expansion 15
K	Expansion 3	Expansion 2	Expansion 12	Expansion 13
L	Expansion 1	Expansion 4	Expansion 10	Expansion 14
M	Expansion 16	SW+	SWS	SW-

Table M.3: Overview of connections from the brown-marked CMC connector

N Expansion Connection Overview

20-pin Molex Slimstack Receptacle			
1	CMC_EXP1	CMC_EXP2	2
3	CMC_EXP3	CMC_EXP4	4
5	CMC_EXP5	CMC_EXP6	6
7	CMC_EXP7	CMC_EXP8	8
9	+3.3V	+3.3V	10
11	GND	GND	12
13	CMC_EXP9	CMC_EXP10	14
15	CMC_EXP11	CMC_EXP12	16
17	CMC_EXP13	CMC_EXP14	18
19	CMC_EXP15	CMC_EXP16	20

Table N.1: Overview of connections from the 20-pin expansion receptacle

40-pin Molex SlimStack Receptacle			
2	GND	GND	1
4	PL_11_GP	PL_1P	3
6	PL_12_GP	PL_1N	5
8	PL_13_GP	PL_2GP	7
10	PL_14_GP	PL_3_GP	9
12	PL_15_GP	PL_4P	11
14	PL_16_GP	PL_4N	13
16	PL_17_GP	PL_5_GP	15
18	PL_18_GP	PL_6_GP	17
20	GND	GND	19
22	GND	GND	21
24	+5V	+5V	23
26	CMC_EXP17	PL_7P	25
28	CMC_EXP18	PL_7N	27
30	CMC_EXP19	PL_8_GP	29
32	CMC_EXP20	PL_9_GP	31
34	GND	GND	33
36	CMC_EXP21	PL_10P	35
38	CMC_EXP22	PL_10N	37
40	+12V	+12V	39

Table N.2: Overview of connections from the 40-pin expansion receptacle