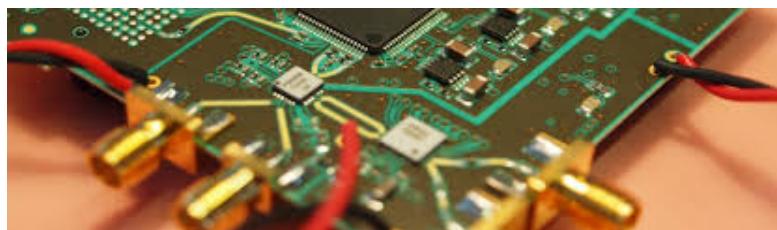


A Terabit sampling system with a photonics time-stretch ADC

Master Thesis
of

Olena Manzhura

at the Institute for Data Processing and Electronics (IPE)



Reviewer: Prof. Dr. Anke-Susanne Müller (LAS)
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15.11.2020 – 14.05.2021

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Karlsruhe, den 14.05.2021, _____
Olena Manzhura

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Abstract

Zusammenfassung

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List of abbreviations

KIT	Karlsruhe Institute of Technology
IPE	Institut für Prozessdatenverarbeitung und Elektronik
KARA	Karlsruhe Research Accelerator
KAPTURE	Karlsruhe Pulse Taking Ultra-fast Readout Electronics
ADC	Analog-To-Digital-Converter
TAH	Track-And-Hold
PLL	Phase-Locked-Loop
FMC	FPGA Mezzanine Card
LVCMOS	Low voltage complementary metal oxide semiconductor
LVDS	Low-voltage differential signaling
LVPECL	Low-voltage positive emitter-coupled logic
PCIe	PCI Express
THERESA	Terahertz Readout Sampling
RFSoC	Radio-Frequency System-On-Chip

1. Introduction

2. Theoretical Fundamentals

2.1. Coherent Synchrotron Radiation

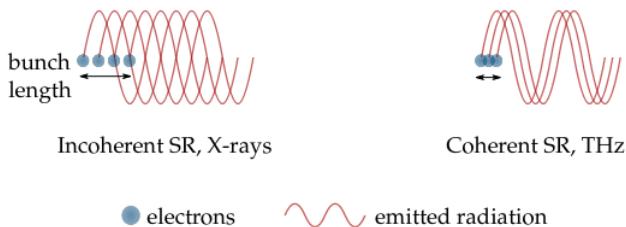


Figure 2.1.: CSR [Rot18]

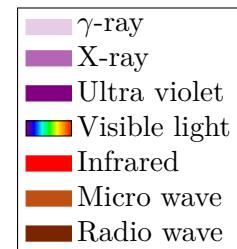
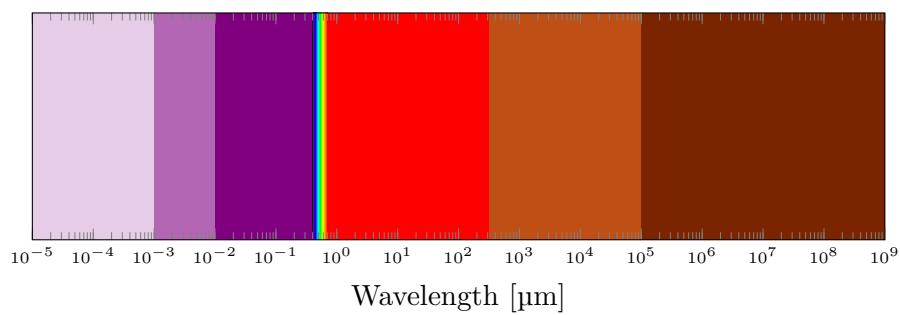


Figure 2.2.: Electro-Magnetic spectrum

KARA

- Located at the Karlsruhe Institute of Technology (KIT)
- Up to 184 electron packages (bunches) can be filled with a distance between two adjacent bunches of 2 ns
- Operated by the Institute of Beam Physics and Technology (IBPT)

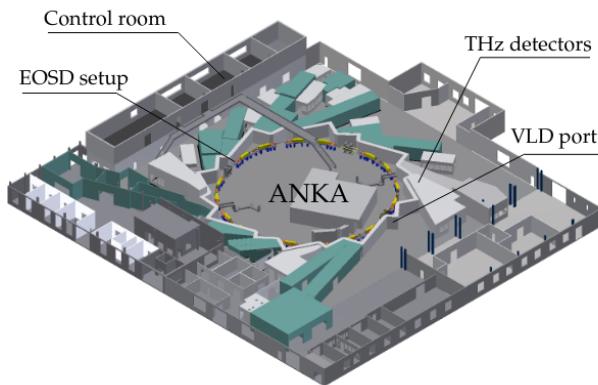


Figure 2.3.: Facility [Rot18]

2.1.1. Micro-Bunching Instability

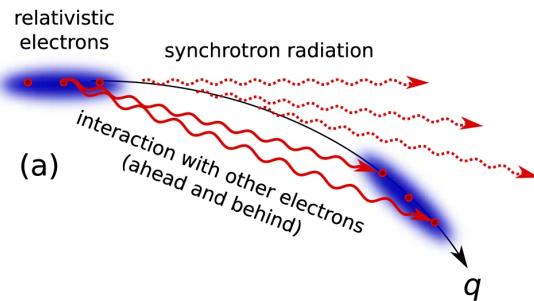


Figure 2.4.: Micro-bunching [BBB⁺19]

2.2. Photonic time-stretch analog-to-digital converter

" In recent and future synchrotron radiation facilities, relativistic electron bunches with increasingly high charge density are needed for producing brilliant light at various wavelengths, from X-rays to terahertz. In such conditions, interaction of electron bunches with their own emitted electromagnetic fields leads to instabilities and spontaneous formation of complex spatial structures. Understanding these instabilities is therefore key in most electron accelerators. However, investigations suffer from the lack of non-destructive recording tools for electron bunch shapes. In storage rings, most studies thus focus on the resulting emitted radiation. Here, we present measurements of the electric field in the immediate vicinity of the electron bunch in a storage ring, over many turns. For recording the ultrafast electric field, we designed a photonic time-stretch analog-to-digital converter with terasamples/second acquisition rate. We could thus observe the predicted link between spontaneous pattern formation and giant bursts of coherent synchrotron radiation in a storage ring. "' [BBB⁺19]

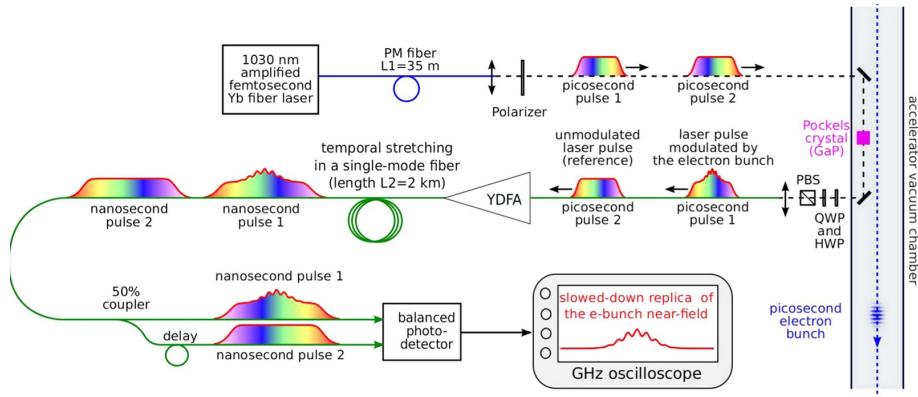


Figure 2.5.: Electro-Optical Time-Stretch Technique [BBB⁺19]

2.3. Analog-To-Digital-Converter

2.3.1. Sampling Theory

- Nyquist-Criteria
- Need for S/H

2.3.2. AC errors

- Quantization Noise
- Equivalent Input Referred Noise
- Noise-Free Code Resolution

Integral and Differential Nonlinearity Distortion

Dynamic Performance

- Harmonic Distortion, Worst Harmonic, Total Harmonic Distortion (THD), Total Harmonic Distortion + Noise (THD + N)
- Signal-to-Noise-and-Distortion Ratio (SINAD, or S/N + D), Signal-to-Noise ratio (SNR), Effective Number of Bits (ENOB)
- Analog Bandwidth (Full-Power, Small-Signal)
- Spurious Free Dynamic Range (SFDR)
- Two-Tone Intermodulation Distortion, Multi-Tone Intermodulation Distortion
- Noise Power Ratio (NPR)
- Adjacent Leakage Ratio (ACLR)
- Noise Figure
- Setting Time, Overvoltage Recovery Time

[Kes05]

2.3.3. Interleaving

- Net sample rate
- Interleaving Spurs

[MR15]

2.4. RF/Microwave Design Basics

3. Design of the system

This chapter covers the architecture and design of the system.

3.1. General architecture

In this section the general architecture of the THERESA system is described. The idea for the new system is to reuse the concept of the already existing sampling system KAPTURE (**K**arlsruhe **P**ulse **T**aking **U**ltra-fast **R**eadout **E**lectronics), which is using four ADCs, and expanding it to 16. Therefore, also the architecture of the latter is explained briefly.

3.1.1. KAPTURE-2

KAPTURE, which was developed at IPE, is a system designed to continuously sample ultra-short pulses generated by Terahertz detectors. It consists of a daughter card, holding four sampling channels, mounted on a FPGA . The FPGA is connected to a computer via PCIe for further processing of the acquired data. [Bro20] The newer version, KAPTURE-2, was designed for more accurate sampling for pulse repetition rates up to 2 GHz. The acquired data is processed with a FPGA and GPU architecture. [CAB⁺17]

The general structure of the board is shown in Figure 3.3.

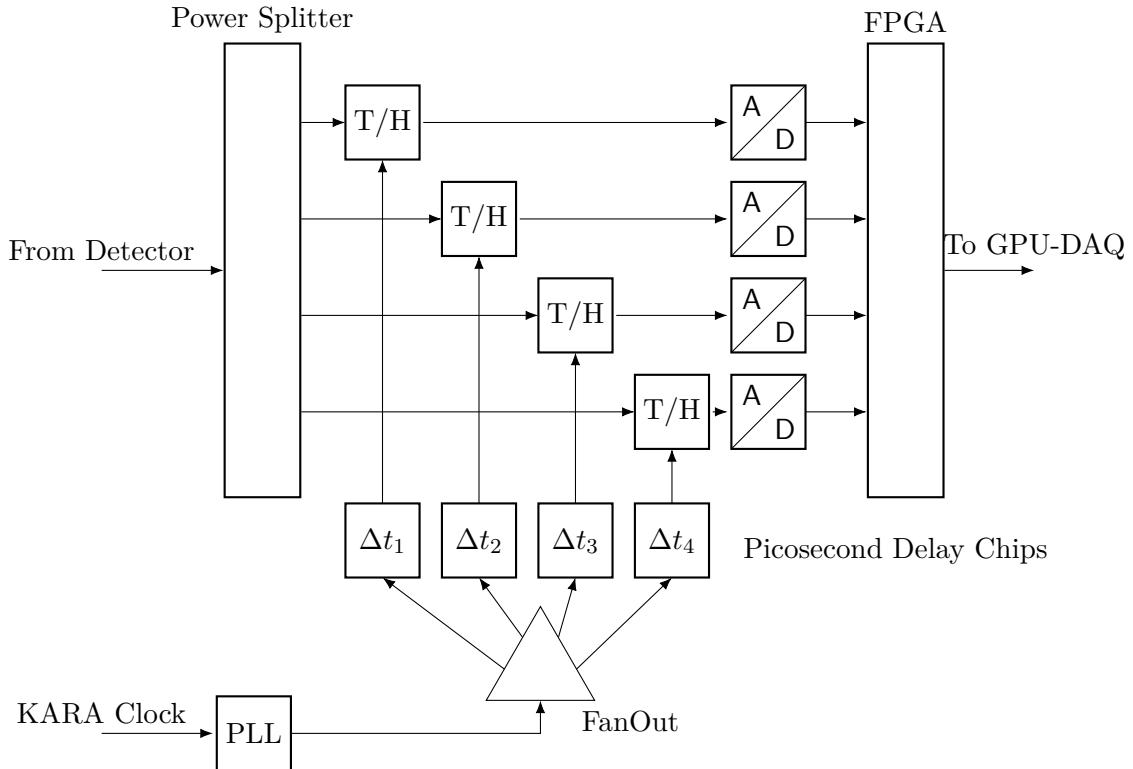


Figure 3.1.: General schema of KAPTURE-2 (cf. [CAB⁺17, p.2])

The pulse from the THz detector is fed into a power splitter, which splits the signal into four identical pulses and distributes them to four channels, consisting of a respective Track-And-Hold-Amplifier (THA) unit and a 12-bit ADC@500 MS/s. The sampling time of each unit can be adjusted individually with a Picosecond Delay Chip with a resolution of 3 ps (maximal delay range: 100 ps). The clock signal is provided by KARA, which cleared from jitter by a Phase-Locked-Loop (PLL). This ensures the synchronization of the ADCs with the RF system. The clean clock signal is distributed to the delay chips via fan-out. [CAB^{+17]}

The resulting sampling of the detector signal is shown Figure 3.2 (simplified representation).

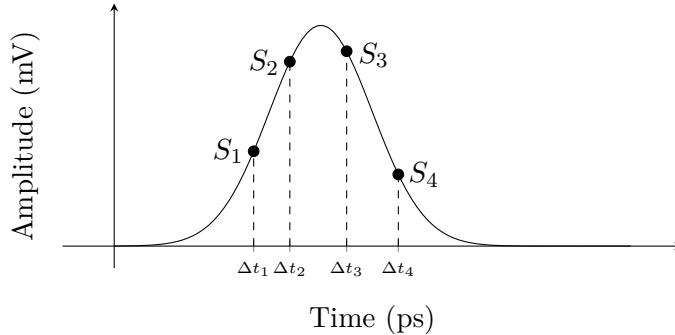


Figure 3.2.: Signal with sample points

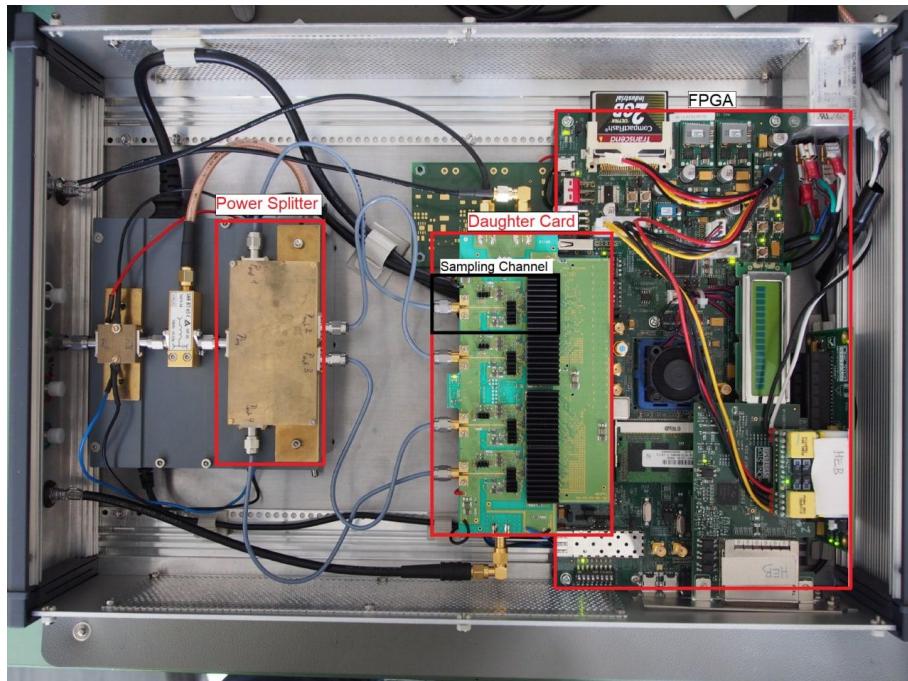


Figure 3.3.: Photo of KAPTURE with highlighted main components. [Bro20, p. 61]

3.1.2. THERESA

In principle, the new system has the same structure, as KAPTURE. Notable differences are firstly the number of ADCs, which is increased up to 16. Secondly, the latter are not located on the daughter card anymore, but inside of the FPGA on the Xilinx Zynq UltraScale+ RFSoC ZCU216 Evaluation Kit on which the front-end card is mounted. Figure 3.4 shows the general schema of the sampling system, reduced to four channels for presentation purposes.

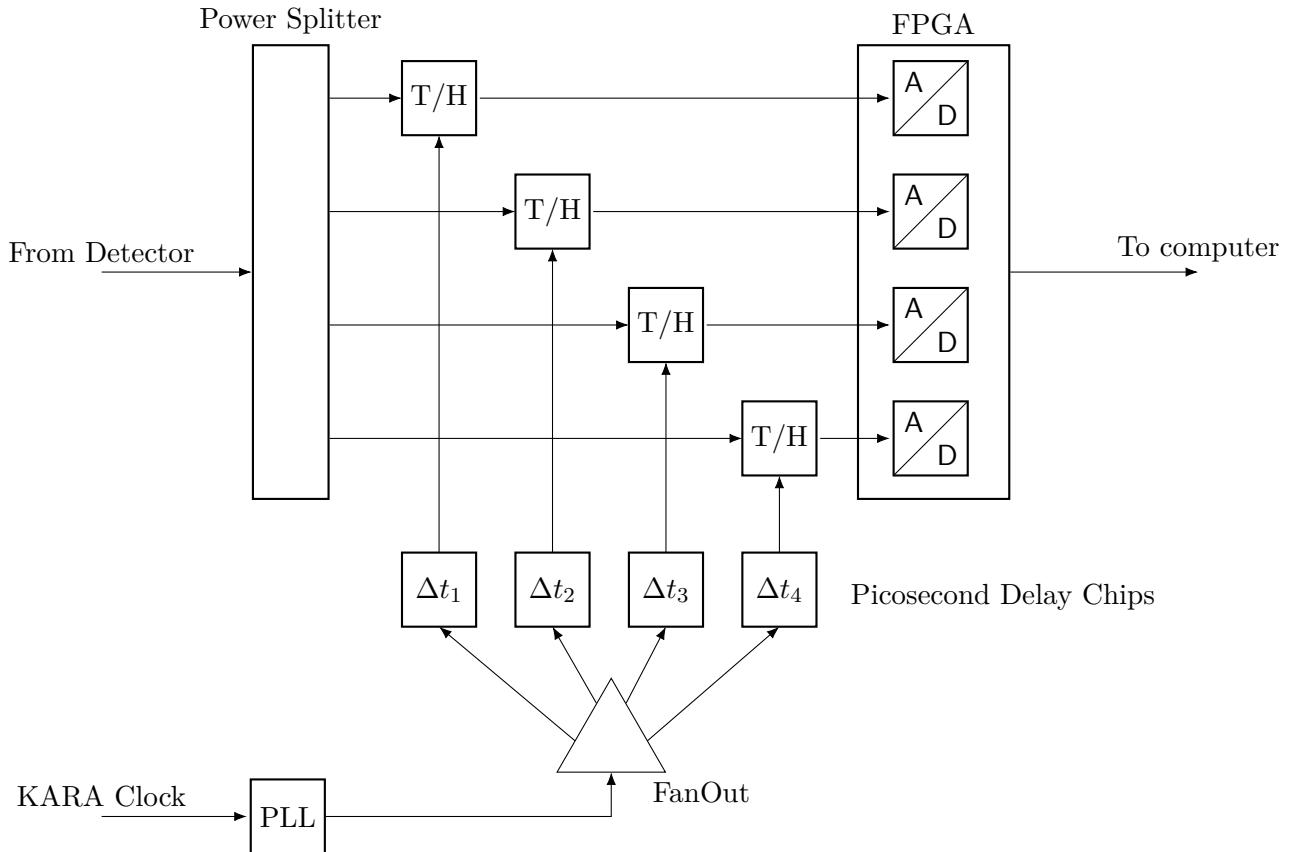


Figure 3.4.: General schema of THERESA. For presentation purposes only four channels are shown.

3.1.2.1. Xilinx Zynq UltraScale+ RFSoC ZCU216 Evaluation Kit

The card, holding the sampling channels, should be mounted on a ZCU216 evaluation board. This board is the newest generation of Xilinx' evaluation cards, which has features suitable for the purpose at hand.

- Sixteen 14-bit, 2.5GSPS RF-ADC
- Sixteen 14-bit, 10GSPS RF-DAC
- I/O expansion options – FPGA Mezzanine Card (FMC+) interfaces, RFMC 2.0 interfaces, and Pmod connections

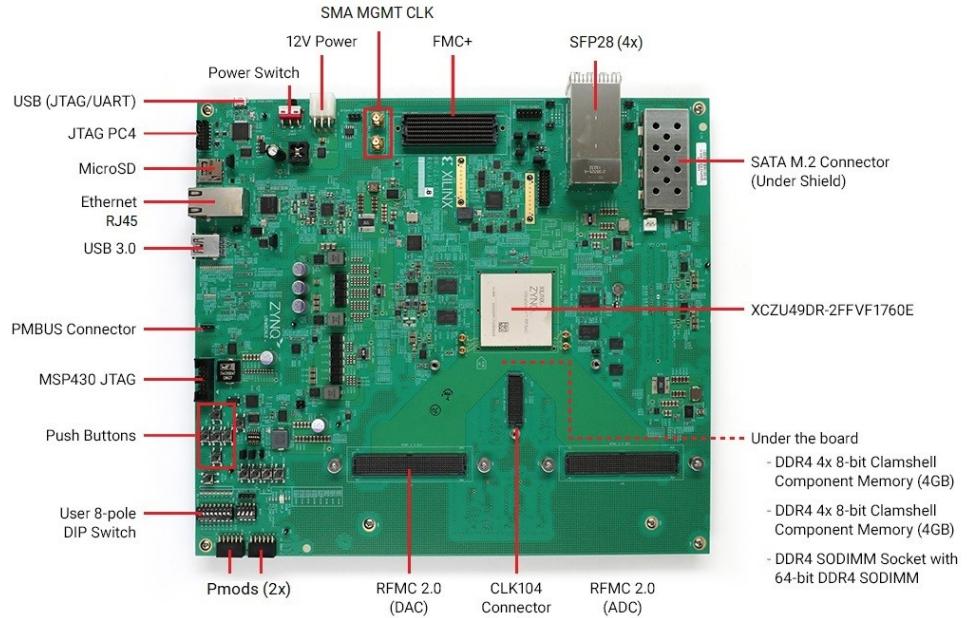


Figure 3.5.: ZCU216 evaluation board

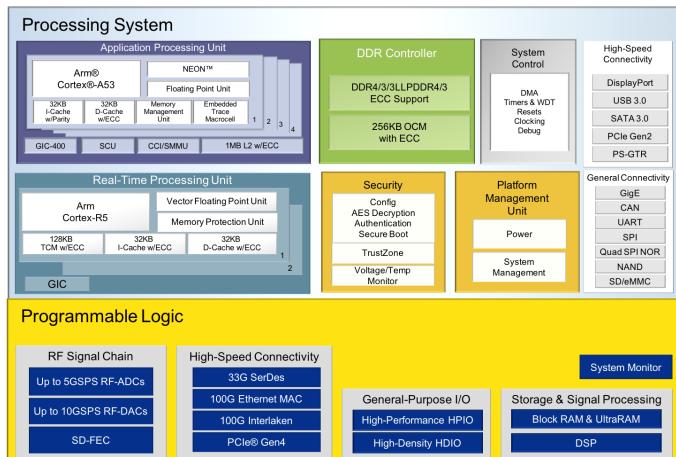


Figure 3.6.: RFSoC block diagram

3.1.3. Requirements

Step size delay chip

The necessary step size for the delay chips, when using 16 ADC@2 GS/s in time-interleaving mode, is: $\frac{2 \text{ GS/s}}{16} = 31 \text{ ps}$

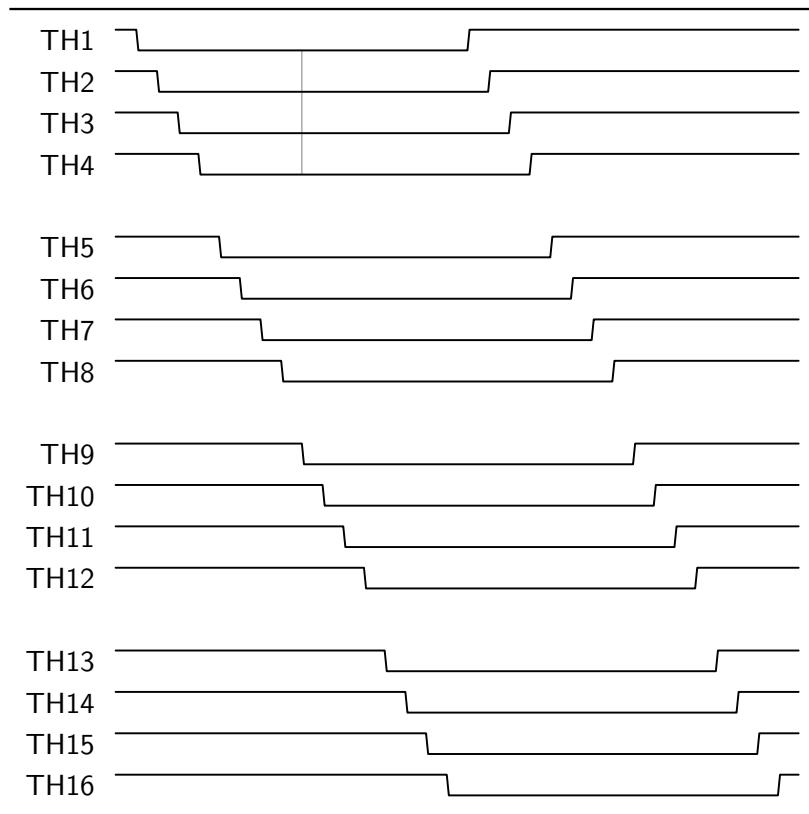
Frequency

Figure 3.7.: Track-And-Hold Timing diagram

Data Rate**Visualization/GUI**

3.2. Design of the front-end card

In this section, the design of the front-end card is covered.

3.2.1. Sampling-Channel

Delay Chip NB6L295

Dual Channel Programmable Delay Chip.

- Two individual variable delay channels
 - Dual Delay: minimal delay 3.2 ns
 - Total Delay Range: 3.2 ns to 8.8 ns per Delay Channel
 - 11 ps Increments in 511 steps
 - 100 ps Typical Rise and Fall Times

3.2.2. Clocking

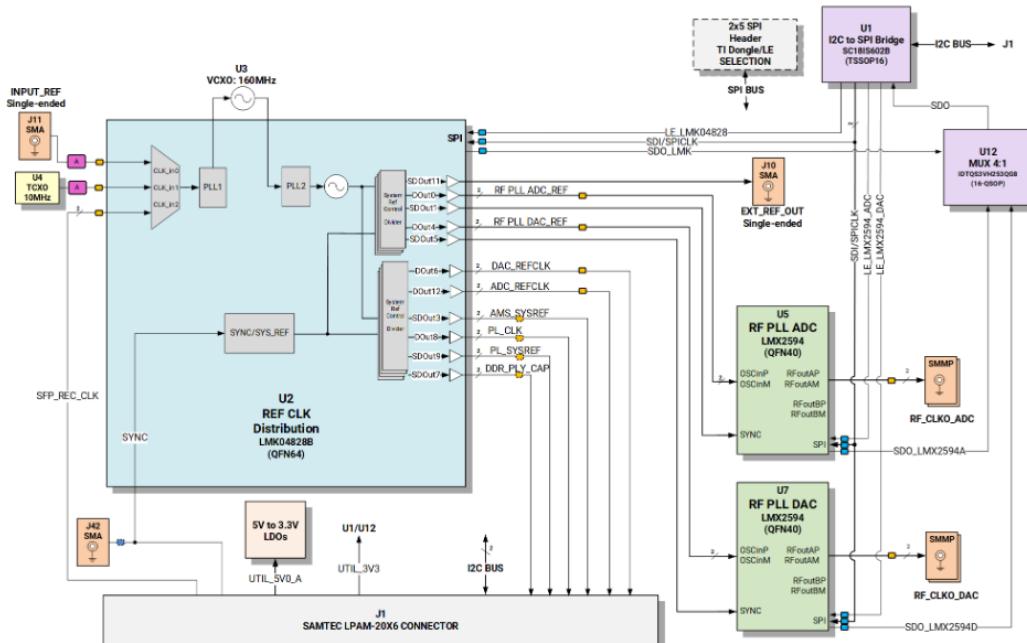
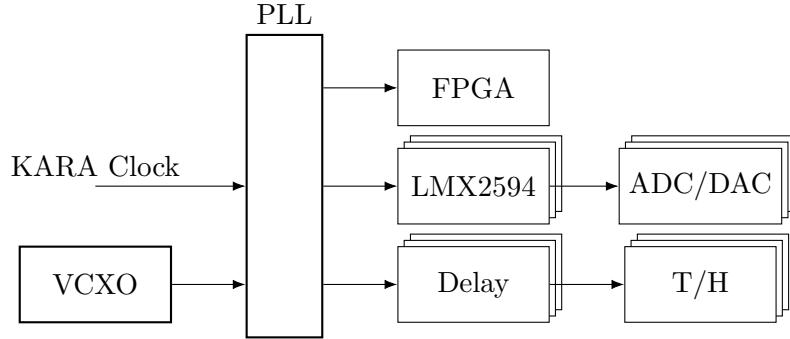


Figure 3.8.: CLK104 Add-on board clocking scheme

**Figure 3.9.:** Clocking scheme on front-end card

3.2.3. Power Supply

For the Track-And-Hold amplifiers a new power supply unit – the ADP1741 (Analog Devices) – should be used. It is necessary to think about the amount of power supply chips needed. As a rule of thumb, the power supply should provide twice the maximum power needed by the components it drives. The power consumption/maximum current for the respective components on the THERESA board is listed in Table 3.1.

Table 3.1.: Power consumption of components on the board

Component	V_{cc} (V)	I_{max} (A)	P_{max} (W)	#parts	I_{tot}^1 (A)
HMC5649 (T/H-Amplifier)	2	0.221	0.442	16	3.536
	-5	-0.242	1.21		3.872
HMC856 (Delay)	-3.3	0.185	-0.611	16	2.96
HMC987LP5E (Fan-Out)	3.3	0.234 ²	0.772	2	0.468
LMC0480 (PLL)	3.3	0.590 ³	1.947	1	0.590
VCXO	3.3	0.03	0.198	1	0.03

¹for 16 ADCs²All Outputs and RF-Buffer³All CLKs

The maximal current which the ADP1741 can provide @2 V is 2 A. This means, with one Track-And-Hold amplifier requiring a maximal current of 0.221 A, one ADP1741 can handle four units according to the rule mentioned beforehand ($I_{max_ADP1741} = 2 \text{ A} > 2 * I_{tot}, I_{tot} = 4 * 0.221 \text{ A} = 0.884 \text{ A}$).

3.3. PCB-Layout

3.3.1. General Techniques/Strategies?

3.3.2. Floor Planning

3.3.3. Transmission lines

Surface Coplanar Waveguide with Ground

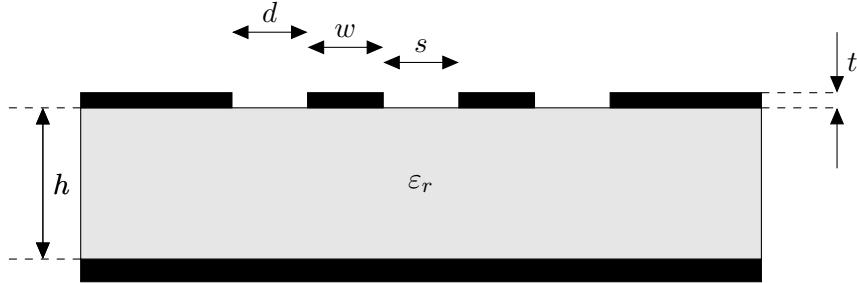


Figure 3.10.: Edge-Coupled Coplanar Waveguide

The corresponding equations are [Wad91, p197-198]:

$$Z_{0,o} = \frac{\eta_0}{\sqrt{\epsilon_{eff,o}}} \left(\frac{1.0}{2.0 \frac{K(k_o)}{K'(k_o)} + \frac{K(\beta_1)}{K'(\beta_1)}} \right) \quad (3.1)$$

$$Z_{0,e} = \frac{\eta_0}{\sqrt{\epsilon_{eff,e}}} \left(\frac{1.0}{2.0 \frac{K(k_e)}{K'(k_e)} + \frac{K(\beta_1 k_1)}{K'(\beta_1 k_1)}} \right) \quad (3.2)$$

$$\epsilon_{eff,o} = \frac{2.0 \epsilon_r \frac{K(k_o)}{K'(k_o)} + \frac{K(\beta_1)}{K'(\beta_1)}}{2.0 \frac{K(k_o)}{K'(k_o)} + \frac{K(\beta_1)}{K'(\beta_1)}} \quad (3.3)$$

$$\epsilon_{eff,e} = \frac{2.0 \epsilon_r \frac{K(k_e)}{K'(k_e)} + \frac{K(\beta_1 k_1)}{K'(\beta_1 k_1)}}{2.0 \frac{K(k_e)}{K'(k_e)} + \frac{K(\beta_1 k_1)}{K'(\beta_1 k_1)}} \quad (3.4)$$

Where

$$k_o = \Lambda \frac{-\sqrt{\Lambda^2 - t_c^2} + \sqrt{\Lambda^2 - t_B^2}}{t_B \sqrt{\Lambda^2 - t_c^2} + t_c \sqrt{\Lambda^2 - t_B^2}} \quad (3.5)$$

$$k_e = \Lambda' \frac{-\sqrt{\Lambda'^2 - t'_c^2} + \sqrt{\Lambda'^2 - t'_B^2}}{t'_B \sqrt{\Lambda'^2 - t'_c^2} + t'_c \sqrt{\Lambda'^2 - t'_B^2}} \quad (3.6)$$

$$\Lambda = \frac{\sinh^2 \left(\frac{\pi(s/2.0 + w + d)}{2.0h} \right)}{2} \quad (3.7)$$

$$t_c = \sinh^2 \left(\frac{\pi(s/2.0 + w)}{2.0h} \right) - \Lambda \quad (3.8)$$

$$t_B = \sinh^2 \left(\frac{\pi s}{4.0h} \right) - \Lambda \quad (3.9)$$

$$\Lambda' = \frac{\cosh^2 \left(\frac{\pi(s/2.0+w+d)}{2.0h} \right)}{2} \quad (3.10)$$

$$t'_c = \sinh^2 \left(\frac{\pi(s/2.0+w)}{2.0h} \right) - \Lambda' + 1.0 \quad (3.11)$$

$$t'_B = \sinh^2 \left(\frac{\pi s}{4.0h} \right) - \Lambda + 1.0 \quad (3.12)$$

The parameters have to be chosen according to

$$s + 2.0w + 2.0d \leq h \quad (3.13)$$

to guarantee coplanar propagation. [Wad91]

Surface Coplanar Waveguide with Ground

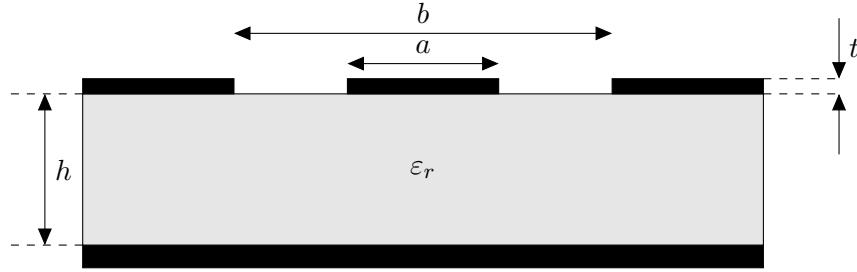


Figure 3.11.: Coplanar Waveguide with Ground

The characteristic impedance of a coplanar waveguide is given as follows [Wad91]:

$$Z_0 = \frac{60.0\pi}{\sqrt{\epsilon_{eff}}} \frac{1.0}{\frac{K(k)}{K(k')} + \frac{K(k_1)}{K(k'_1)}} \quad (3.14)$$

It comprises of the following components, with $K(k)$ being an elliptical integral of the first kind (see also [BSMM99, p. 430]):

$$k = a/b \quad (3.15)$$

$$k' = \sqrt{1.0 - k^2} \quad (3.16)$$

$$k'_1 = \sqrt{1.0 - k_1^2} \quad (3.17)$$

$$k_1 = \frac{\tanh(\frac{\pi a}{4.0h})}{\tanh(\frac{\pi b}{4.0h})} \quad (3.18)$$

$$\epsilon_{eff} = \frac{1.0 + \epsilon_r \frac{K(k')}{K(k)} \frac{K(k_1)}{K(k'_1)}}{1.0 + \frac{K(k')}{K(k)} \frac{K(k_1)}{K(k'_1)}} \quad (3.19)$$

3.3.4. Polaris

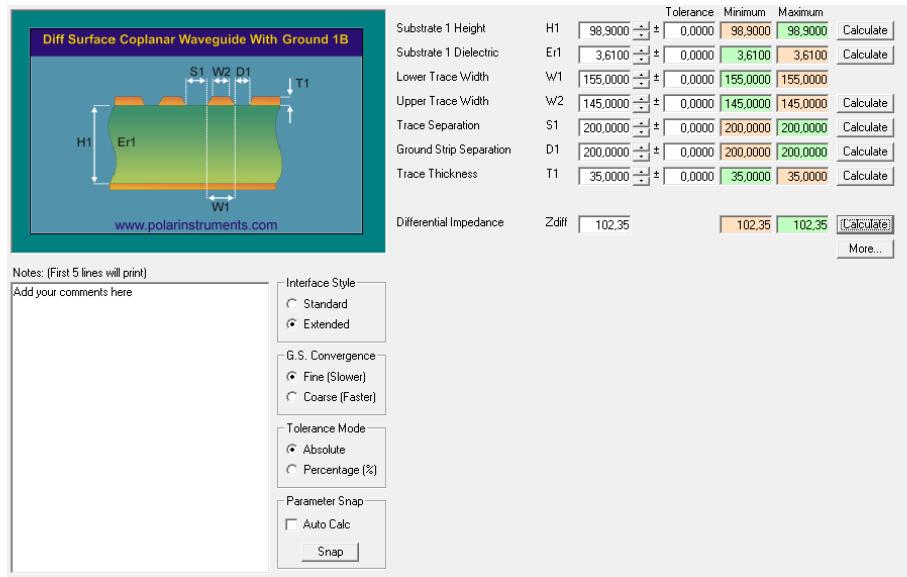


Figure 3.12.: Polaris Solver

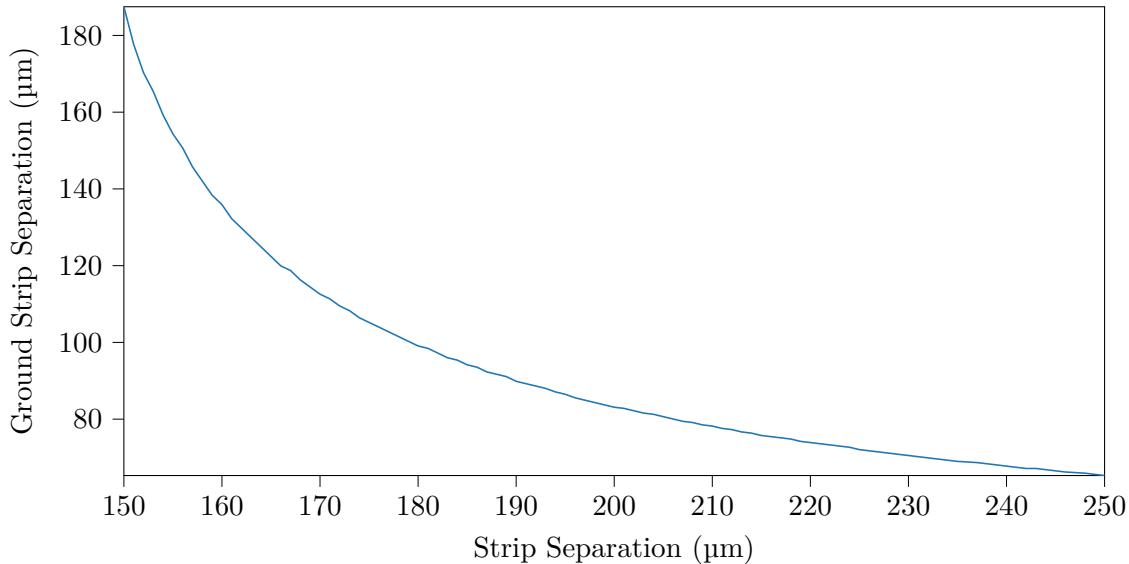


Figure 3.13.: Test Graph

3.4. Firmware

3.4.1. Xilinx Designs

3.4.2. SPI-firmware for components

3.4.3. IPE-AXI IP block

3.4.4. GUI

4. Characterization

4.1. Evaluation of the ZCU216 Board

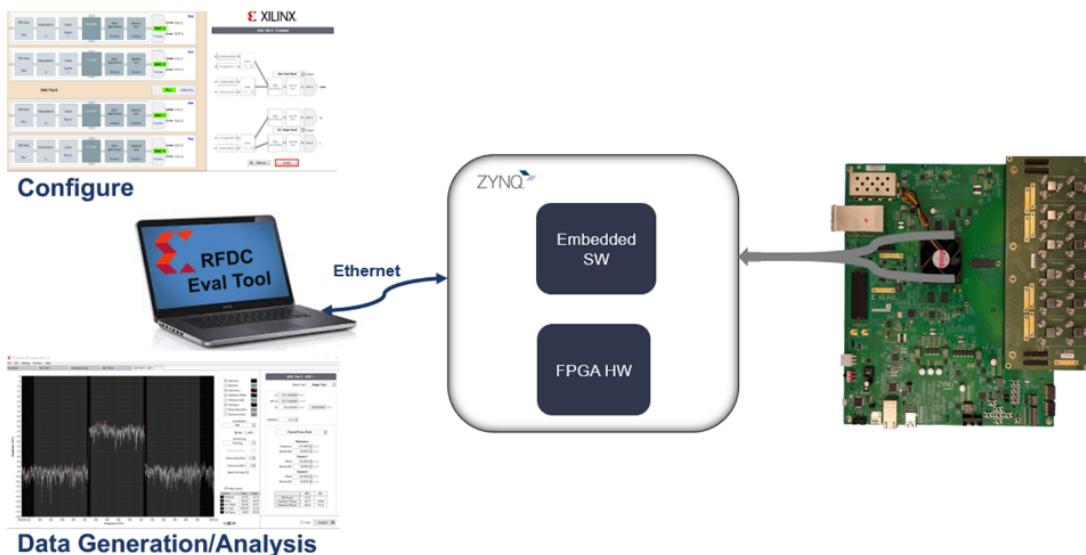


Figure 4.1.: RF DC Evaluation Tool architecture [Xil20a]

4.1.1. Measurements with Xilinx XM655 add-on card

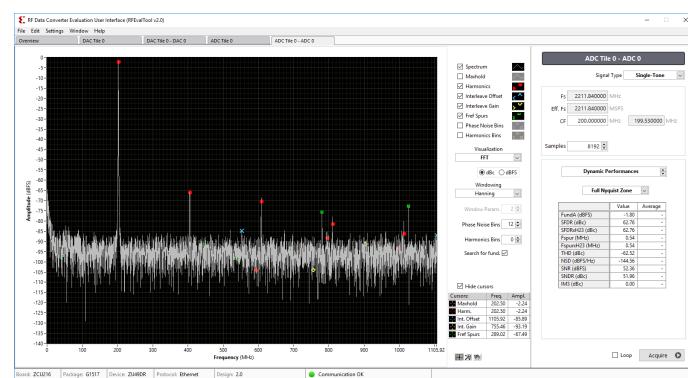


Figure 4.2.: RF DC Evaluation Tool GUI [Xil20a]

4.2. Measurements with the IPE front-end card

5. Conclusions and Outlook

Appendix

A. QuickStart Guide for Evaluation of ZCU216 Board

B. 3D model of front-end card

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