

# A Terabit Sampling System with a Photonics Time-Stretch ADC

Master Thesis  
of

Olena Manzhura

at the Institute for Data Processing and Electronics (IPE)



Reviewer: Prof. Dr. Anke-Susanne Müller (LAS)  
Second Reviewer: Dr. Michele Caselle (IPE)

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# Declaration

I hereby declare that I wrote my master thesis on my own and that I have followed the regulations relating to good scientific practice of the Karlsruhe Institute of Technology (KIT) in its latest form. I did not use any unacknowledged sources or means, and I marked all references I used literally or by content.

Karlsruhe, 13.08.2021, \_\_\_\_\_  
Olena Manzhura

Approved as an exam copy by

Karlsruhe, 13.08.2021, \_\_\_\_\_  
Prof. Dr. Anke-Susanne Müller (LAS)



# Abstract

Analysis of events occurring in the range of femtoseconds is desired in many scientific experiments. The high temporal resolution needed for measuring such events imposes a great technological challenge for Data Acquisition Systems (DAQs) and Analog-To-Digital-Converters (ADCs). In order to relax the requirements on the acquisition systems, the so-called optical time-stretch technique is used to stretch the analog input signal in time. In this way, data converters at relatively moderate sample rate can be used. Measuring the signal with commercial DAQs, such as real-time oscilloscope, still poses another challenge. Due to the limited acquisition time windows of such systems, continuous measurements at high sampling rate and time resolution over a long period of time is not possible. In applications, where measurements of long-term evolution of the ultra-fast events with high temporal resolution is necessary, this is a large limitation. Therefore new concepts of DAQ based on the time-stretch method need to be considered.

In this thesis, a first demonstrator of such a new photonic time-stretch based DAQ system was developed. The system consists of a high bandwidth front-end sampling card, mounted on a back-end readout card integrating a new generation of Radio-Frequency System-On-Chip (RFSoC) for readout of the acquired samples.

The front-end sampling card integrates 16 sampling channels, each containing a Track-And-Hold-Amplifier (THA). The sampling time of these THAs can be delayed individually in steps of 11 ps, covering a range up to 11.2 ns. In this way the so-called time-interleaving method can be implemented to sample the signal at a higher rate than that normally possible due to the Nyquist theorem. The design of the board allows it to be used with the time-stretch method as well as independently from it. Furthermore, the setup allows for different sampling modes. In single-channel mode one detector is connected to one sampling channel, therefore allowing to acquire data from up to 16 detectors at the same time with one sampling point per channel. In the “multi-channel” mode, several channels (up to 16) are connected to one detector via power splitter, therefore allowing multiple sampling points for one detector.

High-speed ADCs, integrated in the RFSoC, with 14-bit resolution and a sample rate of up to 2.5 GS/s allow continuous sampling of the signal with high temporal resolution. Using the time-interleaving technique for all sixteen ADCs results in an overall maximal achievable sample rate of 40 GS/s. When used in combination with the time-stretch technique and considering currently achievable time-stretch factors, a time resolution in the range of hundred of femtoseconds is possible.

The RFSoC on the back-end readout card integrates a processing unit and a Field Programmable Gate Array (FPGA). A firmware running on the FPGA is responsible for programming and controlling the components on the sampling card, as well as collecting the acquired samples and sending it to the following processing system via high-speed connections. The processing unit, hosting e.g. an operating system or a standalone application, allows for the user to control and monitor the overall system via common periphery, e.g. Ethernet.

The name given to the system is THERESA, an acronym for “Terahertz Readout Sampling”.

# Zusammenfassung



# Résumé



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# Acronyms

**ADC** Analog-To-Digital-Converter. v, 1–3, 8–19, 27, 28, 31, 37

**ANR** Agence Nationale de la Recherche. 6

**APU** Application Processing Unit. 27

**AXI** Advanced eXtensible Interface. 31

**CSR** Coherent Synchrotron Radiation. 1, 5, 7, 8, 38

**DAC** Digital-To-Analog-Converter. 12, 27, 28, 31

**DAQ** Data Acquisition System. v, 1–4, 31, 37

**dBc** decibels relative to the carrier. 17

**dBFS** decibels relative to full scale. 17

**DC** Direct Current. 17

**DDR** Double Data Rate. 27, 31

**DFG** Deutsche Forschungsgemeinschaft. 6

**DIMM** Dual In-Line Memory Module. 27

**DNL** Differential Nonlinearity. 15, 16

**ENOB** Effective Number Of Bits. 1, 2, 17

**EO** Electro-Optic. 7, 8

**EOS** Electro-Optic Sampling. 7

**FFT** Fast-Fourier-Transform. 16

**FMC** FPGA Mezzanine Card. 27

**FPGA** Field Programmable Gate Array. v, 2, 6, 27, 28, 31, 37, 38

**GUI** Graphical User Interface. 28

**HDL** Hardware Description Language. 32

**HWP** Half-Wave Plate. 7

**IBPT** Institute of Beam Physics and Technology. 4

**IDE** Integrated Design Environment. 32

- INL** Integral Nonlinearity. 15, 16
- IP** Intellectual Property. 28
- KAPTURE** Karlsruhe Pulse Taking Ultra-fast Readout Electronics. 2
- KARA** Karlsruhe Research Accelerator. 2–4, 38
- KIT** Karlsruhe Institute of Technology. 4
- LINAC** linear accelerator. 3
- LSB** Least Significant Bit. 9, 10, 12, 14, 15, 19
- PCIe** PCI Express. 2
- PL** programmable logic. 27–29, 31, 32
- PLL** Phase-Locked-Loop. 31
- PS** processing system. 27–29, 31–33
- QWP** Quarter-Wave Plate. 7
- RF** Radio Frequency. 4, 27, 28
- RFSoC** Radio-Frequency System-On-Chip. v, 27, 33, 37
- RMS** Root Mean Square. 16, 17, 19
- RPU** Real-Time Processing Unit. 27
- SDI** Serial Data Interface. 31, 32
- SFDR** Spurious-Free Dynamic Range. 16–18, 37
- SFP** Small Form-Factor Pluggable. 27
- SHA** Sample-And-Hold-Amplifier. 10, 11, 15, 16, 18
- SINAD** Signal-to-Noise-and-Distortion Ratio. 17, 37
- SJNR** Signal-to-Jitter-Noise-Ratio. 19
- SNR** Signal-To-Noise-Ratio. 12, 13, 16, 17, 19
- SoC** System-On-Chip. 2
- SODIMM** Small Outline Dual In-Line Memory Module. 27
- SOLEIL** Source optimisée de lumière d'énergie intermédiaire du LURE. 1
- SPI** Serial Peripheral Interface. 31, 32
- SR** synchrotron radiation. 3–5
- THA** Track-And-Hold-Amplifier. v, 11, 37
- THERESA** Terahertz Readout Sampling. 2, 6, 37, 38
- THz** Terahertz. 2–8, 38
- TS-QPI** time-stretch quantitative phase imaging. 1
- ULTRASYNC** Exploration et contrôle ULTRArapide de la dynamique des paquets d'électrons dans les sources de lumière SYNChrotron. 6
- WP** Wollaston Prism. 7

# 1. Introduction

In many scientific applications and experiments the observation of non-repetitive, statistically rare events with very fast occurrences is desired. As these events might occur on a time range of femtoseconds, real-time measurement systems with fine temporal resolution and capable of long acquisition times are necessary. This imposes high technological challenges on Data Acquisition Systems (DAQs) and Analog-To-Digital-Converters (ADCs).

One bottleneck in the acquisition of ultra-fast events is the limited performance of commercially available ADCs. The limitation posed by the converters is a trade-off between the dynamic range (Effective Number Of Bits (ENOB)) and sampling rate of the converters. As the sampling rate increases, ambiguity of the comparators (output neither '0' nor '1') in the ADC and sampling errors due to clock jitter become major limiting factors on the overall performance. [MCB<sup>+</sup>17]

A first demonstration of a concept to overcome these limitations was presented in 1999 by [CBJ99]. The idea is to stretch the analog signal in time before digitizing it in the converter and hence relax the demands on the data converter performance. This time-stretching is accomplished by using chirped optical pulses and chromatic dispersion in optical fibers. The concept is therefore called “photonic time-stretch” and was successfully tested in combination with a moderate-speed ADC in [CBJ99].

Since then, the time-stretch method has been continuously improved and has found use in many applications. For example, in biomedical diagnostics, a first demonstration of an artificial intelligence based high-speed phase microscope has been developed. It uses time-stretch quantitative phase imaging (TS-QPI), a technique based on the time-stretch concept which enables simultaneous measurement of phase and spatial intensity profiles. This allows label-free classification of cells for cancer diagnostics and drug development. [MCB<sup>+</sup>17]

The time-stretch concept is also useful for applications in particle accelerators due to the short timescales involved. In a storage ring for example, relativistic electron bunches interact with their own radiation which can lead to the formation of spatial microstructures inside the bunches, a phenomenon also called micro-bunching instability. This is a source of intense pulses of terahertz radiation (Coherent Synchrotron Radiation (CSR)) and therefore an important field of study. A first demonstration of direct observation of these instabilities was performed at the synchrotron facility Source optimisée de lumière d'énergie intermédiaire du LURE (SOLEIL) using a time-stretched signal together with a real-time oscilloscope. [RELP<sup>+</sup>15]

The use of the time-stretch method in different applications has demonstrated the advantages to measure events with femtosecond resolution. However, commercially available real-time diagnostics systems are limited in memory space (currently maximal memory depth lies in the range of few Gigasamples). This limits the acquisition time of such systems at maximum sampling rate, which lies in the range of a few milliseconds at best. It is therefore

not possible to measure data continuously over a large period of time. This creates a problem in applications where a longer observation time (up to hours) is required, e.g. in accelerator applications where the turn-by-turn analysis<sup>1</sup> of the electron bunches is desired in order to study the evolution of the bunch profiles.

This challenge was the motivation to design novel ultra-fast acquisition systems based on the photonic time-stretch ADC. Together with the next generation of Field Programmable Gate Array (FPGA)-based systems with integrated high-performance ADCs this gives rise to a new concept of DAQ, the photonic time-stretch DAQ. The photonic time-stretch DAQ consists of a photonic part, which consists of the time-stretching section and the conversion of photons into electrical signal with a photo-detector. Furthermore, such a system has one or multiple ADCs converting the analog values into digital signals. The digital signals are then processed in a computing unit and broadcast to other units as needed if the system is integrated into a cluster of measurement systems.

### 1.1. Objective

In this thesis, a first demonstrator of a DAQ-system based on the time-stretch concept is developed. This system, called Terahertz Readout Sampling (THERESA) system, enables high-speed measurements of ultrafast events with a time resolution in the range of femtoseconds.

In order to achieve such high resolution, the time-stretch technique will be used in order to stretch the input signal in the range of pico- to nano-seconds. The input signal will be continuously sampled by high-speed ADCs with a temporal resolution defined by the user as needed. To sample the signal, the ADCs need to have a sampling rate in the order of several GHz. The amplitudes of the signals to be measured are very small and an appropriate resolution of the ADCs has to be chosen in order to guarantee an ENOB of at least 10 bits. [Ser]

This leads to the next challenge: Sampling at several GHz with high resolution, implies a large amount of data, leading to a data rate in the range of Terabits per second. In order to enable such a high data-throughput, the system will be based on a new generation of System-On-Chip (SoC), integrating a FPGA and a processing unit together with the high-speed ADCs. The SoC will have high-speed peripherals in order to guarantee the continuous high-speed data-throughput. Combination with the FPGA should allow for flexible system tuning for a user-defined application. The user will be able to control and configure the system via an application or operating system running on the processing unit.

Furthermore, the system should be compatible with already existing high-speed DAQ frameworks (e.g. based on PCI Express (PCIe)) and be easily integrated into the system for the user application (e.g. through optical fibers to a distributed instrumentation system). However, stand-alone operation should also be possible. Furthermore, the DAQ should be designed in such way that usage independent from the time-stretch method is possible.

The overall thesis is structured in the following way: Chapter 2 gives the necessary theoretical background for the new THERESA system. The subject of Terahertz (THz) science in particular is touched being the main motivation for the design of the novel time-stretch sampling system. Chapter 3 covers the general architecture of THERESA, including also state of the art readout-systems, especially the Karlsruhe Pulse Taking Ultra-fast Readout Electronics (KAPTURE) which is in operation at the Karlsruhe Research Accelerator (KARA). Chapter 4 describes the design steps of the front-end sampling card

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<sup>1</sup>Turn-by-turn denotes the analysis of a specific bunch for every turn, bunch-by-bunch denotes the analysis between individual bunches

of THERESA in detail. Chapter 5 covers the description of the back-end readout card, as well as the design of the appropriate firmware. At last, results are concluded and an outlook for the newly developed system is given.



## 2. Motivation

As the main aspired use case of the newly developed time-stretch Data Acquisition System (DAQ) lies in accelerator physics applications, especially in Terahertz (THz) science e.g. at Karlsruhe Research Accelerator (KARA), an introduction into this topic is given in the following section.

After that the general architecture and basic theory of a photonic time-stretch DAQ is given. First, the basic working principle of the time-stretch concept is explained. Then, a short overview of the basic Analog-To-Digital-Converter (ADC) theory is given, together with the most prominent figures of merit. Knowledge and understanding of ADC characteristics is necessary to evaluate the overall performance of the converter.

### 2.1. Requirements in THz Science

Recent years have seen an increasing interest in THz radiation, ranging from 3 THz up to 30 THz<sup>1</sup>, as it allows non-destructive analysis of organic material. This is possible because unlike e.g. X-Rays, THz radiation is not ionizing. It is therefore of great interest to use THz radiation in fields like biology, medicine or material science. However, until recently the usage of THz radiation was very limited, as generation of such radiation has proven to be difficult.

Synchrotrons are a potential source of THz-radiation. The emission of THz radiation is closely linked to instabilities of the charged particles which are accelerated in the synchrotron. [Mü12] These instabilities occur in the time range of femtoseconds and cause bursts of THz radiation. The periodicity of these bursts depends on multiple parameters of the synchrotron and therefore imposes a challenge on controlling the emission of THz radiation. Studying the dynamics of these instabilities is an important step towards the application of synchrotrons as source of THz radiation. [Rot18]

#### 2.1.1. Coherent Synchrotron Radiation

In synchrotron radiation facilities synchrotron radiation (SR) is produced by accelerating relativistic electrons. Emission of SR occurs, when electron beams are bent or deflected with dipole magnets or using undulators. The latter are used to make the electrons oscillate by generating a periodic magnetic field. Figure 2.1 shows the general scheme of an electron storage ring.

Electrons, which are grouped to “electron bunches”, are generated with an electron gun and accelerated to relativistic speeds<sup>2</sup> by a pre-accelerator (often a linear accelerator (LINAC), a booster ring accelerator or a microtron with a booster). After being brought up to their nominal energy<sup>3</sup>, the bunches are injected into the storage ring. In the ring, the path of the

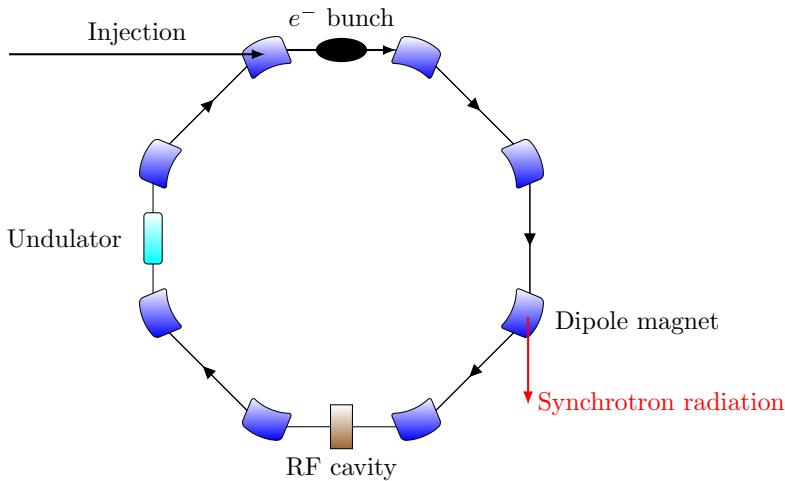
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<sup>1</sup>At KARA: 0.1 THz to 1.2 THz

<sup>2</sup>almost speed of light

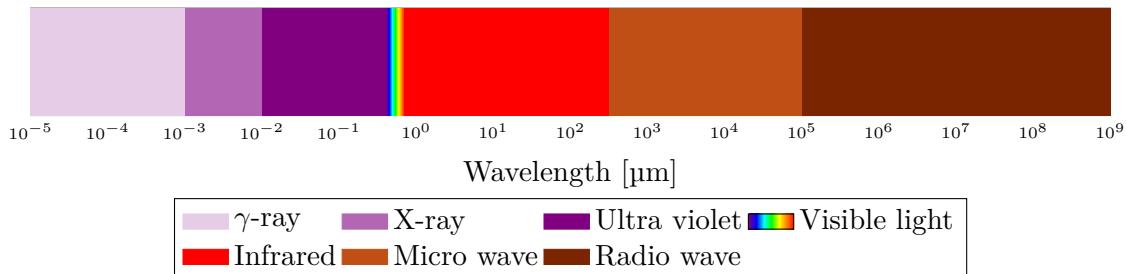
<sup>3</sup>in a booster

electron bunches is altered by dipole magnets, guiding them on a circular trajectory. Due to emission of SR at each bend, the electrons lose energy, which has to be compensated for. This is done by accelerating them with an electric field inside a Radio Frequency (RF) cavity. Not shown in the drawing are the beamlines, which lead the SR radiation, or rather chosen wavelength ranges, through an optical system to the respective user experiments. [Rou14, Rot18]



**Figure 2.1.:** Basic scheme of an electron storage ring (redrawn from [Rou14])

The range of SR reaches from hard X-rays down to the infrared region of the electromagnetic spectrum (see Figure 2.2). SR shows properties like high intensity, high collimation, polarisation and generation in pulses of well-defined time-duration. Due to this properties, synchrotrons are used for microscopy, spectroscopy, and time-resolved experiments in such fields like condensed matter physics, biology, material science and many more.



**Figure 2.2.:** Electromagnetic spectrum

### Karlsruhe Research Accelerator

At the synchrotron light source KARA, the possibility to utilize the synchrotron as a source of THz is actively researched. The photonic time-stretch DAQ, which has been developed in this thesis, should also be integrated into the beam diagnostics system at KARA. Therefore, a short overview of some parameters of this facility has been given below.

KARA is located at the Karlsruhe Institute of Technology (KIT) and is operated by the Institute of Beam Physics and Technology (IBPT). The storage ring can be filled up with up to 184 electron bunches with a distance of 2 ns ( $\cong 500$  MHz) between two adjacent bunches. The main accelerator parameters are listed in Table 2.1.

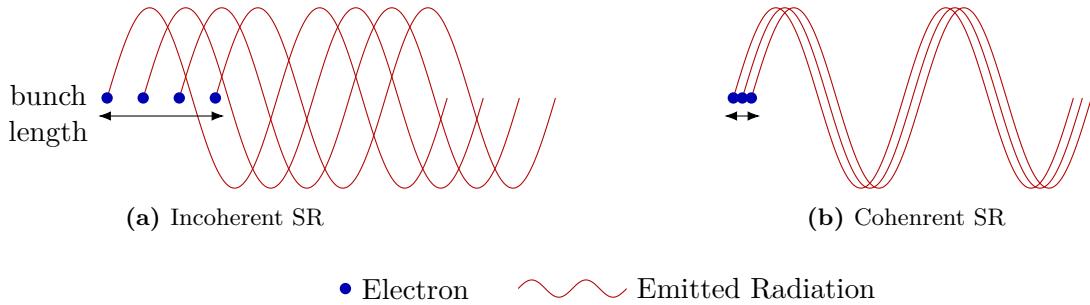
One scientific focus at KARA lies in the study of so-called “micro-bunching instabilities” which are described in the following.

**Table 2.1.:** Some KARA parameters [Rot18]

Parameter	Value
Beam energy (max.)	2.5 GeV
Circumference	110 m
Revolution Frequency (one electron)	2.7 MHz
<b>Minimum bunch spacing</b>	
multi-bunch	2 ns
single-bunch	368 ns
<b>Bunch length (rms)</b>	
normal operation	45 ps
short bunch	2 ps

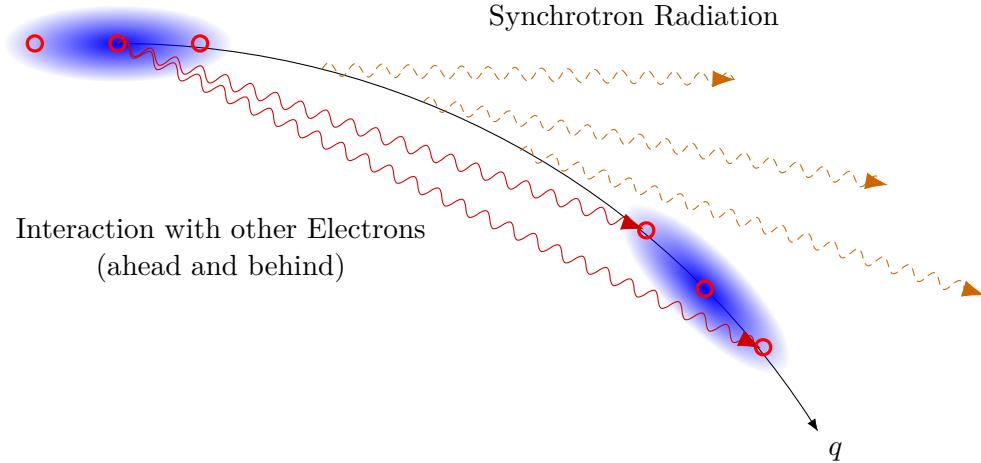
### Micro-Bunching Instabilities

Increasing demands in current and future accelerators applications call for higher brilliance of the emitted radiation. This is achieved by shortening the electron bunches. As illustrated in Figure 2.3, this results in emission of Coherent Synchrotron Radiation (CSR), the spectrum of which spans from 100 GHz up to THz. Due to this CSR the bunches interact with their own radiation as shown in Figure 2.4, which introduces complex longitudinal dynamics.

**Figure 2.3.:** Incoherent SR and coherent SR due to shorter electron bunch length [Rot18]

These dynamics are the so called micro-bunching instabilities, the formation of micro-structures (in the sub-millimeter range) in the longitudinal density profile of the electron bunches. These instabilities occur in bursts and are hard to control, as they depend on a number of system parameters. This imposes on one side a huge limitation to the stable operation of the overall system at high current density/short bunch length mode. On the other side, these instabilities themselves emit brilliant THz radiation that could be potentially used in imaging applications. Such applications however require a stable power of the radiation. Therefore, a control of these instability bursts could potentially make them a source of THz radiation for user-applications. A thorough understanding and studying of these beam dynamics is therefore an important step towards providing an applicable THz source. [Rot18, Bro20] In order to make such investigations possible, appropriate beam diagnostic systems are required, which are capable of both capturing (ultra-)fast and long-term changes in the bunch profile.

### Relativistic Electrons



**Figure 2.4.:** Electrons interact with their own radiation [BBB<sup>+</sup>19]

### Control of Micro-Bunching Instabilities

The Exploration et contrôle ULTRArapide de la dynamique des paquets d'électrons dans les sources de lumière SYNChrotron (ULTRASYNC) project, funded by ANR-DFG<sup>4</sup>, has an objective of ultrafast study and control of electron bunches in synchrotron light sources.

There is the question of control (i.e. suppression) of the bursts of THz radiation occurring during the micro-bunching instability. The goal is to obtain a high power and stable coherent emission. The current experimental setup uses a relatively simple feedback loop:

- A bolometer/Schottky barrier diode detector which produces the input signal for the feedback loop.
- A low-cost Field Programmable Gate Array (FPGA) (Red Pitaya) that controls the accelerating voltage of the synchrotron based on the input

However, there are limitations in the controllable bunch charge in the accelerator this feedback loop can handle, which is around 10 mA. Therefore, an open question is whether measuring each THz pulse using the setup

- Electro-Optical sampling and time-stretching
- Association with the new FPGA-based system, i.e. Terahertz Readout Sampling (THERESA) system
- Finding adequate feedback, programmed in the FPGA

would help in solving the problem and allow the control to succeed also at higher currents (goal: 15 mA) [Ser].

<sup>4</sup>Agence Nationale de la Recherche (ANR), Deutsche Forschungsgemeinschaft (DFG)

### 2.1.2. Electro-Optic Techniques for Longitudinal Bunch Profile Diagnostics

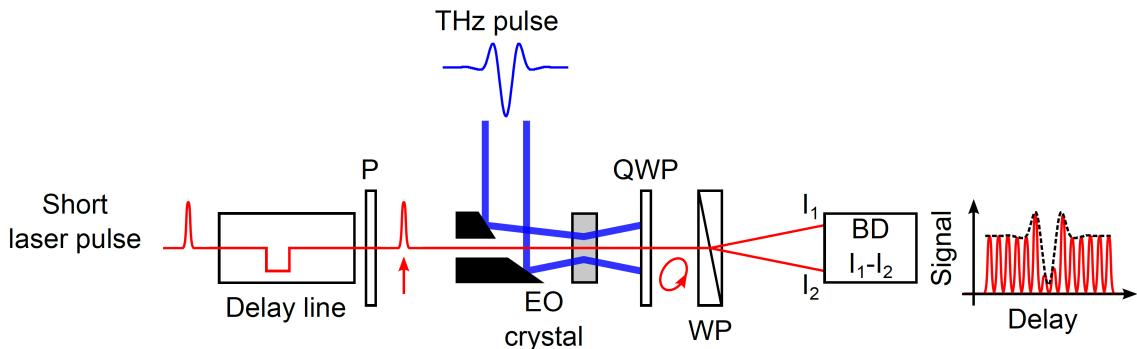
Methods for analyzing the longitudinal profile of electron bunches are based on a similar, if not the same, electro-optical concept as the time-stretch method. Two most prominent methods are briefly described for the sake of completeness.

#### Scanning-Type Electro-Optic Sampling

The scanning-type Electro-Optic Sampling (EOS) samples one point at the time of the THz pulse, emitted e.g. from an electron bunch, at each acquisition, hence the naming of this method.

A short laser pulse (duration typically hundreds of femtoseconds) co-propagates with a THz pulse from CSR (range of picoseconds) in an Electro-Optic (EO) crystal. Due to the Pockels effect the THz pulse causes a time dependent birefringence in the crystal. This modulates the polarization state of the laser pulse.

To sample the pulse, the delay between the laser and the THz pulse is varied. To detect the changing polarization, the polarization of the laser pulse is transformed into an intensity modulation. This is done by using polarizers, e.g. Quarter-Wave Plates (QWPs) and Wollaston Prism (WP) (as shown in Figure 2.5). A general scheme of the system is shown in Figure 2.5. For this technique a stable emission of the THz pulses is crucial, as they are not measured in one acquisition. [Rou14]



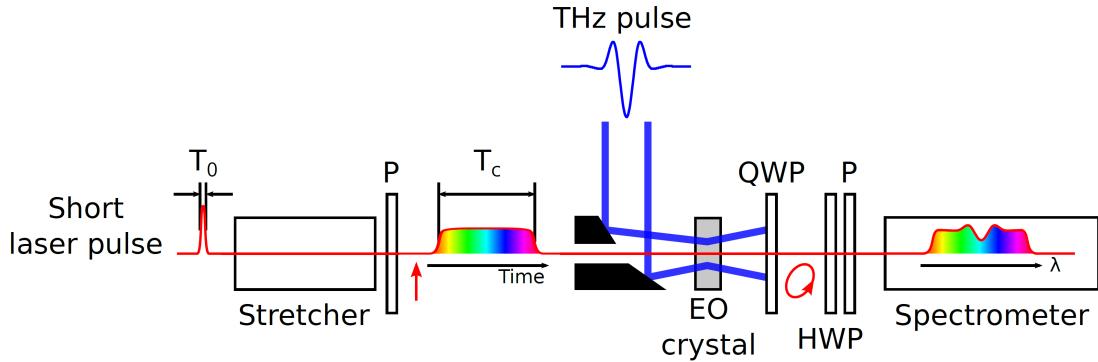
**Figure 2.5.:** Scheme of Scanning-Type Electro-Optical Sampling System [Rou14]

#### Spectrally Resolved Electro-Optic Detection

In contrast to the EOS, single-acquisition is possible with the spectrally resolved EO detection technique. The short laser pulse is first stretched to a duration similar to the THz pulse in a dispersive material, called stretcher. In this way the pulse is chirped, meaning the instantaneous frequency of the pulse varies over time. Together with the THz pulse, the laser pulse propagates through an EO crystal. Again, the induced birefringence modulates the laser pulse, not only in time, but also in the spectral domain. The polarization state of the pulse is converted into an amplitude/intensity modulation. This is done with a series of QWP, Half-Wave Plate (HWP) and a polarizer (P) (as shown in Figure 2.6). To retrieve the THz pulse shape in time, the spectrum of the laser pulse is measured with a spectrometer. A general scheme of the system is shown in Figure 2.6. [Rou14]

The temporal resolution of this method is limited due to the finite chirp rate

$$\text{chirp rate} = \frac{\text{laser bandwidth}}{\text{laser pulse duration after stretcher}}. \quad (2.1)$$



**Figure 2.6.:** Scheme of Spectrally Encoded Electro-Optical Detection System [Rou14]

The minimal resolution  $T_{\min}$  depends on the bandwidth-limited pulse duration (before stretcher)  $T_0$  and the duration of the chirped laser pulse  $T_c$ :

$$T_{\min} = \sqrt{T_0 T_c} \quad (2.2)$$

## 2.2. Photonic Time-Stretch Method

The operating principle of the optical time-stretch technique can be described in three steps (see Figure 2.7).

First, a short laser pulse (duration typically hundreds of femtoseconds) propagates in a dispersive medium, e.g. an optical fiber of length  $L_1$  (see Figure 2.7). With the optical bandwidth of the laser pulse  $\Delta\lambda$  and the dispersion parameter  $D_1$  of the fiber, this results in a chirped laser pulse of the duration

$$T_1 = \Delta\lambda D_1 L_1. \quad (2.3)$$

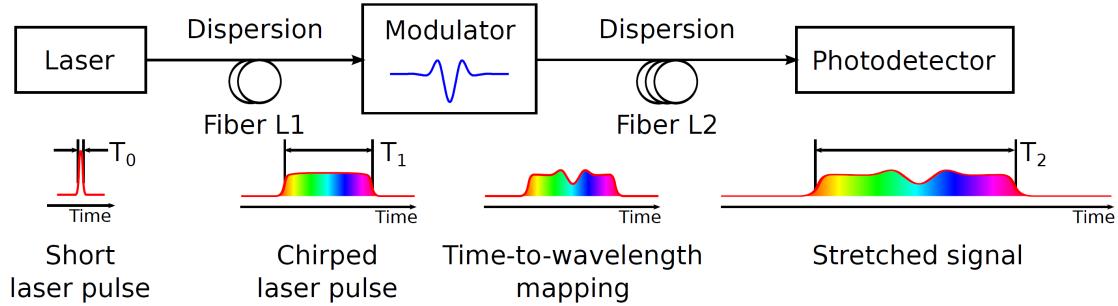
The next step is the time-to-wavelength-mapping, where a temporal intensity modulation is imprinted on the chirped pulse. This happens when the laser pulse co-propagates with another pulse, e.g. a THz pulse from CSR (duration in the range of picoseconds), in an EO crystal. Due to the Pockels effect the THz pulse causes a time-dependent birefringence in the crystal. The Pockels effect describes the phenomenon of occurring and change of existing birefringence in an electric field, which is linearly proportional to the electric field strength. [Gmb]

After that, the modulated chirped pulse propagates through another dispersive medium, a fiber of the length  $L_2$ . In this way, the temporal modulation of the pulse is further stretched to the duration  $T_2$ , which is long enough for detection with photodetectors and the digitizing with ADCs. [Rou14]

The factor  $M$ , by which the pulse is slowed down, is calculated as

$$M = 1 + \frac{L_2}{L_1}. \quad (2.4)$$

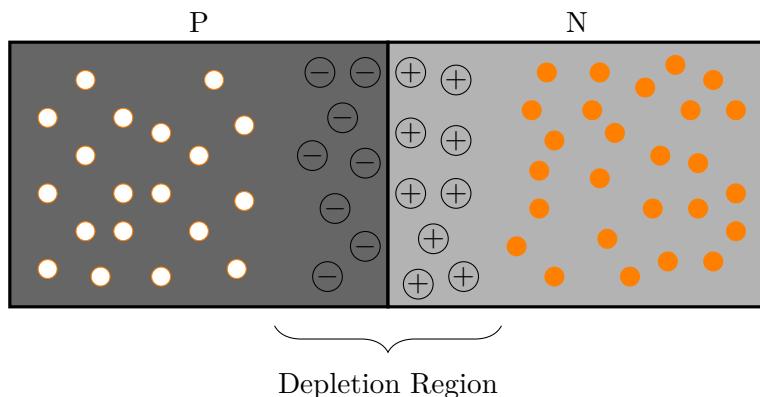
As example, assume the length of the dispersive media as  $L_1 = 10\text{ m}$  and  $L_2 = 2\text{ km}$  and an input signal with the duration  $t_{\text{sig}} = T_1 = 1\text{ ps}$ . With Equation 2.4 the stretching factor for this set-up is  $M \approx 200$ . The input pulse is stretched to  $T_2 = M \cdot T_1 = 200 \cdot 1\text{ ps} = 200\text{ ps} = 0.2\text{ ns}$ . This corresponds to a frequency of 5 GHz which is much easier to handle e.g. for an oscilloscope.



**Figure 2.7.:** Working principle of the electro-optical time-stretch technique [Rou14]

### Photodetector

In order to convert the time-stretched optical signal into an electrical value a photodetector, e.g. a photodiode, is needed. A basic diode photodetector is a photo-diode operated in reverse bias, meaning the *p*-side is connected to the negative terminal and the *n*-side to the positive terminal of the power supply. This enlarges the depletion region (see Figure 2.8) of the *p/n*-junction as the depletion region contains only a very small amount of free charge carriers. Irradiating diode with photons of sufficient energy generates electron-hole pairs due to the photoelectric effect. If the electron-hole pairs are produced in the depleted region of the *p/n*-junction, they are separated by the electric field applied across it, before they can recombine. This creates a so called photo-current which can be measured. [Ele]



**Figure 2.8.:** pn-junction with depleted region [all]

### 2.3. Analog-To-Digital Converter

ADCs are used to translate analog signals, like voltages, into the digital representation of these signals. This *digitized* version can then be stored and processed by information processing, computing, data transmission and control systems. This translation, also called “conversion”, can be seen as encoding a continuous-time analog input  $V_{\text{in}}$  (voltage) into a series of discrete,  $N$ -bit words. This process is also called *sampling*. With the full-scale voltage of the  $V_{\text{FS}}$ , the individual output bits  $b_k$  and the quantization error  $\epsilon$ , the ADC should satisfy the relation

$$V_{\text{in}} = V_{\text{FS}} \sum_{k=0}^{N-1} \frac{b_k}{2^{k+1}} + \epsilon. \quad (2.5)$$

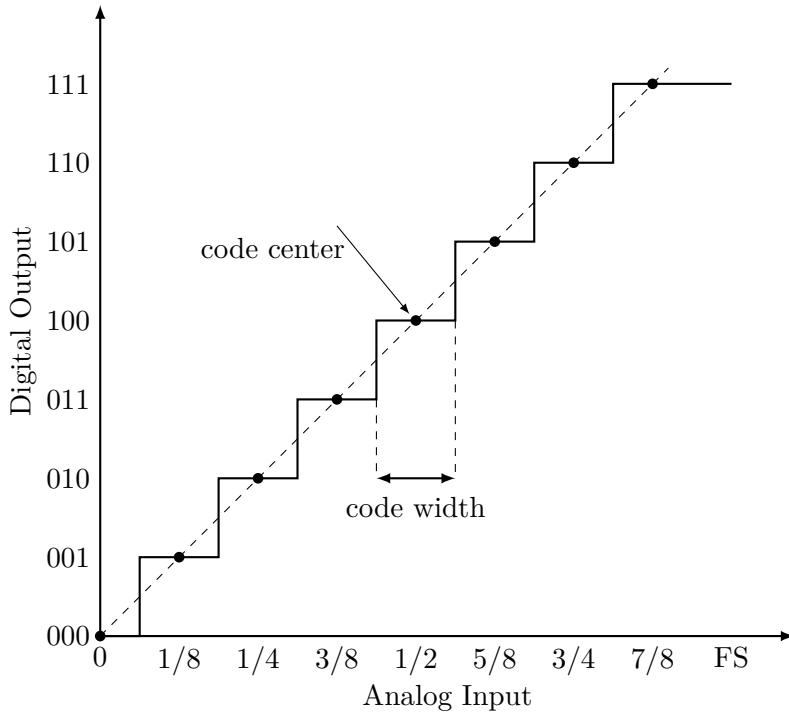
This can also be rewritten in terms of the Least Significant Bit (LSB) or quantum level  $V_Q$

$$1\text{LSB} = \frac{V_{\text{FS}}}{2^N} = V_Q. \quad (2.6)$$

With Equation 2.5 this leads to

$$V_{\text{in}} = V_Q \sum_{k=0}^{N-1} b_k 2^k + \epsilon. \quad (2.7)$$

Figure 2.9 shows the ideal transfer function of a 3-bit ADC. Each digital  $N$ -bit word corresponds to a range of input voltage values (*code width*), which is centered around a *code center*. The input voltage is resolved to the code of the nearest code center.



**Figure 2.9.:** Transfer function of an ideal, 3-bit ADC (redrawn from [LV02])

### Sample-And-Hold-Amplifier

ADCs need a certain amount of time to sample the input signal. If the level of the analog signal changes by more than one LSB during this period, this can result in large errors in the output signal. Therefore so called Sample-And-Hold-Amplifier (SHA) are used in front of the ADC to hold the input level constant for the needed amount of time.

A general block diagram of a SHA is shown in Figure 2.11. It consists of an input and output buffer, a switch controlled by the sampling clock and a capacitor. The analog input is buffered in an input buffer which leads to a switch that is controlled by a sampling clock. During the sample mode, i.e. during the negative sampling clock cycle, the switch is open. At the transition from negative to positive clock cycle, the switch closes, connecting the input signal with the capacitor which is charged in this way.

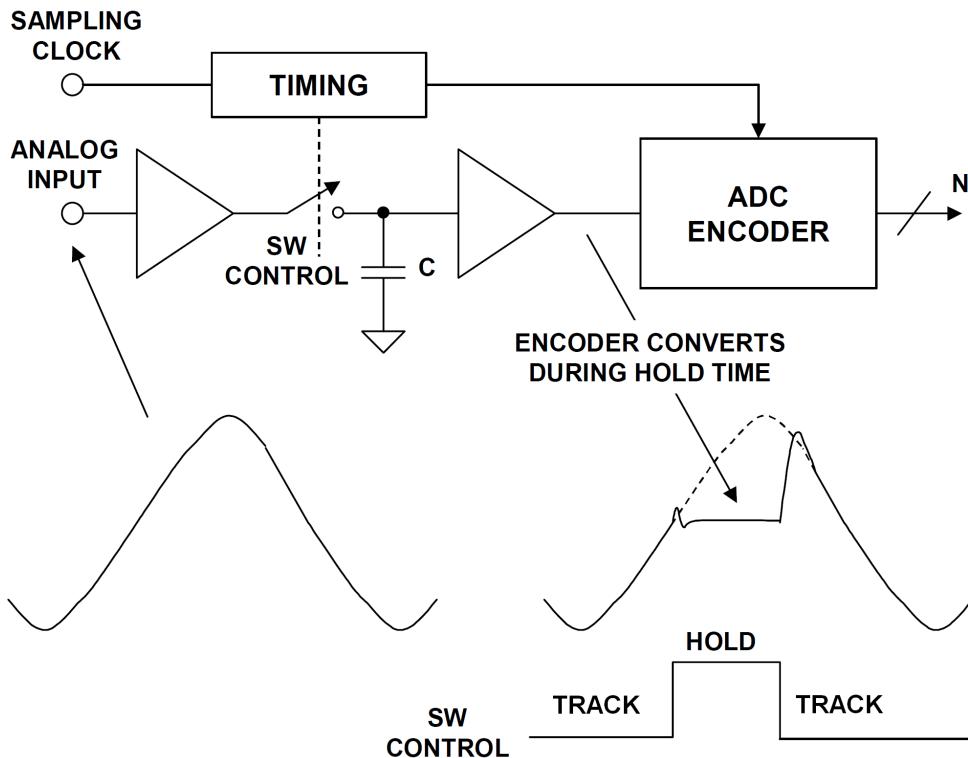
The ADC sampling time needs to be timed in such way, that the whole duration of an analog-to-digital conversion falls into the hold period of the SHA and does not exceed into the sample period. Figure 2.10 shows a qualitative example for proper sample timing. As conclusion, the upper frequency limitation is not determined by the ADC itself, but rather by the aperture jitter, bandwidth, distortion, etc. of the SHA. [Kes05]



**Figure 2.10.:** Example for appropriate sampling timing when using Sample-And-Hold-Amplifier. The sample points of the ADC should be inside the period, where the SHA holds the input value.

### Track-And-Hold Amplifier

Apart from the SHAs there also exists the so called Track-And-Hold-Amplifier (THA). Though the names are often used interchangeably, there exists one fundamental difference between a SHA and a THA. Strictly speaking, the output of a SHA is not defined during the sample period. Only when switching to the hold mode, the output is assigned to a defined value: the voltage level at the input in that moment. Contrary to that, the THA acts as a unity gain amplifier during the sample period, meaning the output is just a replication of the input. The THA “tracks” the input signal (see also Figure 2.10). Therefore, instead of speaking of a “sample” period, the term used here is the “track” period. When switching to hold mode, the instantaneous input level is held over the course of the hold period. This principle allows to improve the sampling rate, as the settling time of an THA is in general smaller than one of a SHA. Settling time denotes the amount of time needed for the output voltage to be at a stable level, after the transition from track/sample to hold mode. This process is quicker, when the output voltage is already in the range of the sampled input at the moment, instead of when the hold capacitor first has to be charged to the input voltage. [Ree17]



**Figure 2.11.:** Track-And-Hold-Amplifier schematic and principle [Kes05]

### 2.3.1. Characteristics of Analog-To-Digital-Converters

For an ideal converter, the number of bits and the sampling rate would be sufficient to fully characterize its performance. Real ADCs however differ from the ideal behavior by introducing static and dynamic imperfections. Different applications have different requirements, which leads to a number of specifications. These can be divided into the categories according to [LV02]:

- Quantization Noise
- Static parameters
- Frequency-domain dynamic parameters
- Time-domain dynamic parameters

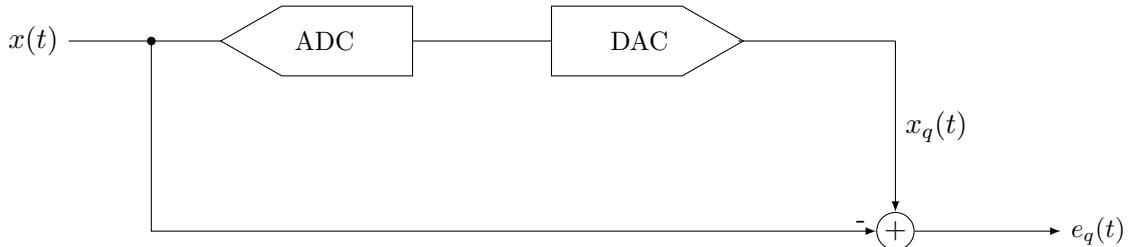
This section provides an overview of these figures of merit. Which of them are needed to specify the necessary performance of the ADC has to be chosen for each application accordingly.

#### 2.3.1.1. Quantization Noise

Even an ideal  $N$ -bit converter has errors resulting from the quantization process which behave like noise. The reason is that each  $N$ -bit word represents a certain range of analog input values, which is 1 LSB wide and centered around a code center (see Figure 2.9). [LV02] The input voltage is assigned to the word of the nearest code center. This means that there will always be a difference between the corresponding voltage of the respective digital code  $x_q(t)$  and the actual analog input voltage  $x(t)$ . This difference is called the *quantization error*. For an equidistant quantization, the quantization error for a code width  $q$  is (see [Pue15])

$$|e_q(t)| = |x(t) - x_q(t)| \leq \frac{q}{2}. \quad (2.8)$$

A setup in order to measure this quantization error is shown in Figure 2.12.



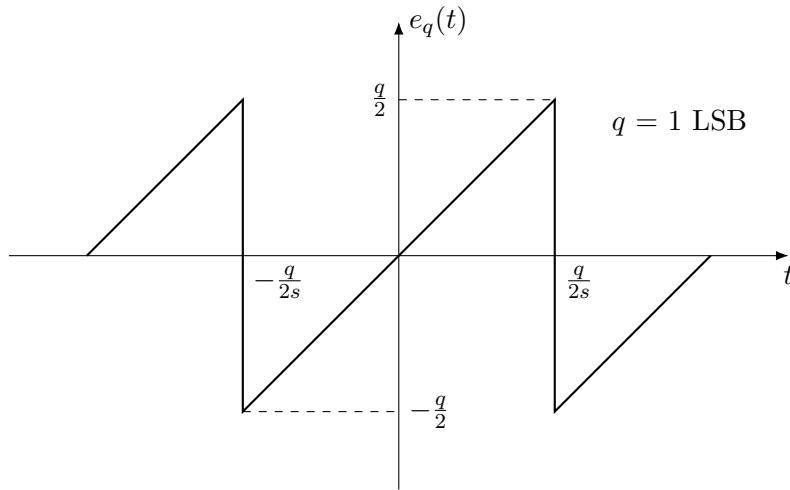
**Figure 2.12.:** Setup for measuring the quantization error of an (ideal) ADC with input signal  $x(t)$

The output of the ADC, the  $N$ -bit code corresponding to the voltage level of the input signal  $x(t)$ , is fed to a Digital-To-Analog-Converter (DAC), which converts this code into a corresponding voltage level  $x_q(t)$ . The difference between  $x(t)$  and  $x_q(t)$  is the quantization error  $e_q(t)$ .

In order to analyze the quantization noise and the resulting theoretical (maximum) Signal-To-Noise-Ratio (SNR) of the ideal ADC, assume a ramp with the slope  $s$  as an input signal. Then, the quantization error  $e_q(t)$  can be approximated with a sawtooth signal in the time domain (see [Kes05]):

$$e_q(t) = st, \quad -\frac{q}{2s} < t < \frac{q}{2s} \quad (2.9)$$

The function in Equation 2.9 is plotted in Figure 2.13.



**Figure 2.13.:** Quantization noise as function of time (redrawn from [Kes05])

The power of this quantization noise can be calculated as the mean-square  $e_{\text{rms}}^2$  of  $e(t)$  (see [Kes05]):

$$P_{QN} = e_{\text{rms}}^2 = \overline{e^2(t)} = \frac{s}{q} \int_{-q/2s}^{+q/2s} (st)^2 dt = \frac{s^3}{q} \left[ \frac{t^3}{3} \right]_{-\frac{q}{2s}}^{+\frac{q}{2s}} = \frac{q^2}{12} \quad (2.10)$$

In order to calculate the maximal SNR of an ideal converter, a full-scale input sine wave is applied to the input:

$$u(t) = u_s \sin(2\pi ft) = \frac{2^N q}{2} \sin(2\pi ft) = 2^{N-1} q \sin(2\pi ft) \quad (2.11)$$

With the effective value of the signal amplitude

$$u_{\text{eff}} = \frac{u_s}{\sqrt{2}} = \frac{2^{N-1} q}{\sqrt{2}} \quad (2.12)$$

the SNR can be calculated as

$$\text{SNR} = \frac{P_{\text{signal}}}{P_{\text{noise}}} = \frac{u_{\text{eff}}^2}{e_{\text{rms}}^2} = \frac{2^{2N-2} q^2 / 2}{q^2 / 12} = 2^{2N} \cdot 1.5. \quad (2.13)$$

In decibel, the SNR is calculated as (see [Pue15, Kes05]):

$$\text{SNR|}_{\text{dB}} = 10 \log (2^{2N} \cdot 1.5) = 6.02N + 1.76 \quad (2.14)$$

### 2.3.1.2. Static parameters

*Static parameters* are specifications, which can be measured at low speed/DC.

#### Accuracy

*Accuracy* is the total error with which an ADC can convert a known voltage, which includes the effects of (see [LV02]):

- Quantization error
- Gain error
- Offset error
- Non-linearities

## Resolution

*Resolution* is the number of bits  $N$  of the ADC. Depending from the resolution are the size of the LSB, which in its turn determines the dynamic range, code widths and quantization error.

## Dynamic Range

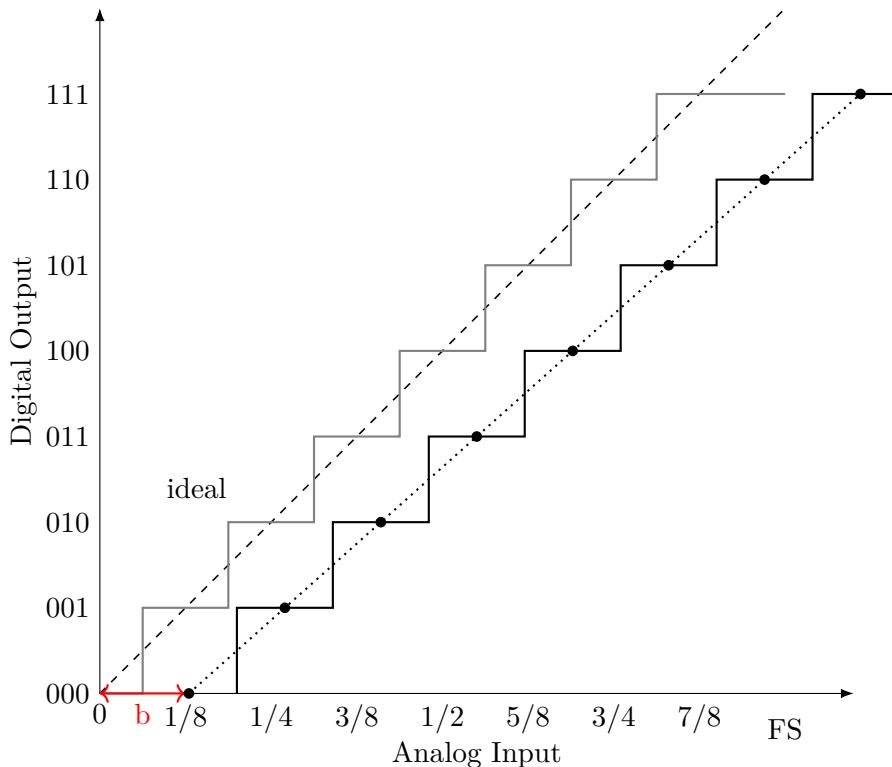
The *dynamic range* represents the ratio between smallest possible output (LSB voltage) and the largest possible output (full-scale voltage). It can be calculated as

$$20 \log 2^N \approx 6N. \quad (2.15)$$

## Offset and Gain Error

The *offset error* is defined as the deviation of the actual ADC transfer function from the ideal ADC transfer function in the point of zero. It is measured in LSB.

*Gain Error* defines the deviation of the slope of the line going through the zero and full-scale point of the transfer function. Figure 2.14 visualizes the effects of both offset and gain error.



**Figure 2.14.:** Offset and Gain Error in the ADC characteristic transfer function. The offset error is indicated with the red arrow. The gain error expresses itself via different slope of the real ADC (dotted) compared to the ideal ADC (dashed)

These errors can easily be corrected by calibration. In order to measure the offset and gain error, two different voltage levels  $V_1$  and  $V_2$  are applied at the ADC input. This results in corresponding bit codes  $b_1$  and  $b_2$ . The slope  $s$  of the transfer function can then be calculated by

$$s = \frac{b_2 - b_1}{V_2 - V_1}. \quad (2.16)$$

From this, the gain error can be determined. In order to obtain the offset error  $b$ , the linear equation

$$b = b_1 - s \cdot V_1 \quad (2.17)$$

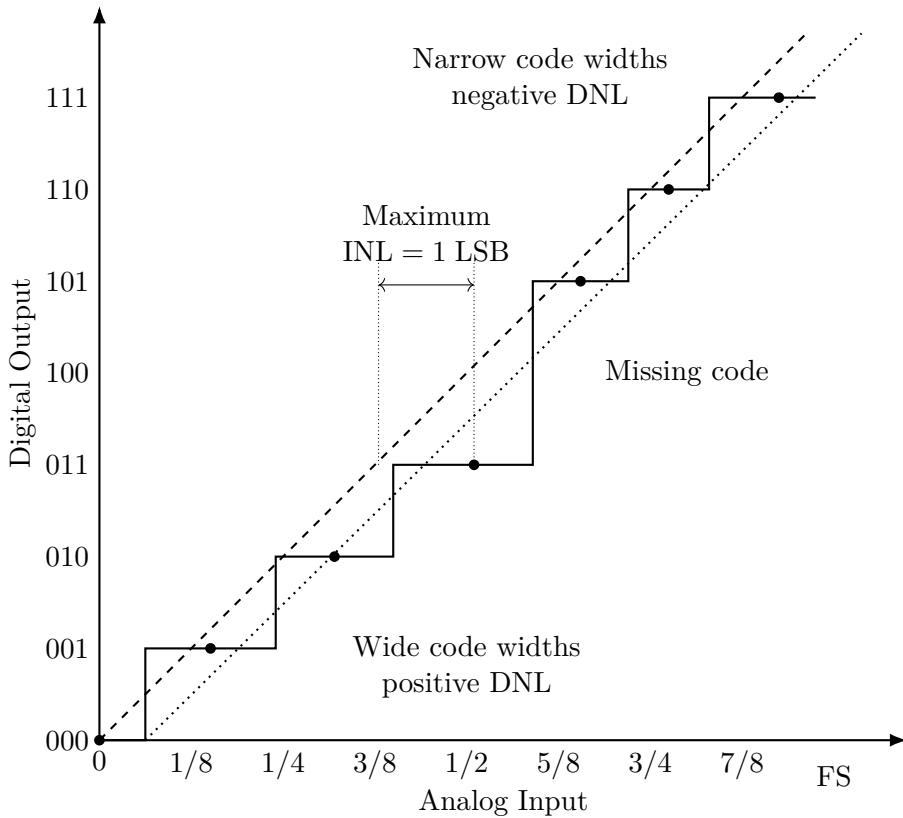
is solved.

### Integral and Differential Non-Linearity Distortion

Integral Nonlinearity (INL) is the distance of the code centers on the actual ADC transfer function from the ideal line (dashed line in Figure 2.15). It results from the integral non-linearities of the front-end, SHA and also the ADC itself [Kes05, LV02].

Differential Nonlinearity (DNL) is the deviation in actual code width from the ideal width of 1 LSB. This non-linearity stems exclusively from the encoding process in the ADC [LV02, Kes05] .

The effect of these errors is shown in Figure 2.15.



**Figure 2.15.:** Transfer function of a real ADC showing DNL and INL.[LV02]

These non-linearities could be measured with a histogram test. A voltage ramp is applied at the input and the number of occurrences of each ADC output code,  $n(\text{code})$ , is measured. With the ramp slope  $s$  an ideal ADC with the sampling frequency  $f_s$  would give

$$n(\text{code}) = \frac{\text{LSB}}{s} \cdot f_s = n_{\text{avg}}, \quad (2.18)$$

which ideally would be constant for the whole input range (except for the first and last code). For a real ADC this is not the case and the DNL and INL are calculated as (see

[Vol])

$$\text{DNL}(\text{code}) = \frac{n(\text{code}) - n_{\text{avg}}}{n_{\text{avg}}} \quad (2.19)$$

$$\text{INL}(\text{code}) = \sum_{i=0}^{\text{code}} \text{DNL}(i). \quad (2.20)$$

### 2.3.1.3. Frequency-Domain Dynamic Parameters

Any real ADC is subject to noise distortion. *Noise* denotes any unwanted random signal, which interferes with the measuring of the desired signal. Examples are quantization noise or random fluctuations due to thermal noise. *Distortion* is the term for alteration of the shape of the original signal. As an example, distortion of the amplitude might result due to not equal amplification of the parts of a signal. [dif]

In an ADC (with built-in SHA) there are a couple of sources, which introduce noise and distortion:

- **Input Stage:** Wideband noise, non-linearity and bandwidth limitation
- **SHA:** Non-linearity, aperture jitter(see paragraph about Time-Domain Dynamic Performances) and bandwidth limitation
- **ADC:** Quantization noise, non-linearity

For quantification of noise and distortion, frequency-domain metrics are used. Therefore the figures of merit described in the following paragraphs are also called frequency-domain dynamic parameters. These parameters are measured with the help of the Fast-Fourier-Transform (FFT) meaning any modern oscilloscope can be used to quickly assess the frequency-domain dynamic performance for a given input at the ADC. As some parameters, such as Spurious-Free Dynamic Range (SFDR), are only defined for one carrier input frequency, several measurements at different input frequencies need to be made in order to fully characterize the ADC.

In the following paragraphs, an overview of the metrics for quantification of the noise and distortion of an ADC is given.

### Signal-to-Noise Ratio

The SNR is defined as the ratio of the input signal power to the power of the noise signal. It is expressed in dB and can be calculated using the Root Mean Square (RMS) value of the signal and noise amplitudes (see [Xila]):

$$\text{SNR} = \frac{\text{Power}_{\text{Signal}}}{\text{Power}_{\text{Noise}}} \quad (2.21)$$

$$= \left( \frac{\text{Amplitude}_{\text{Signal,rms}}}{\text{Amplitude}_{\text{Noise,rms}}} \right)^2 \quad (2.22)$$

$$= 20 \log \left( \frac{V_{\text{in,rms}}}{V_{\text{Q,rms}}} \right) \quad (2.23)$$

Usually, the SNR degrades at higher frequencies due to sampling jitter. [Xila]

### Signal-to-Noise-and-Distortion Ratio

Signal-to-Noise-and-Distortion Ratio (SINAD) (also called SNDR or S/N+D) denotes the ratio between the RMS of the signal amplitude to the mean value of the Root-Sum-Square (RSS) of all other spectral components, including harmonics, but excluding Direct Current (DC) (0 Hz). SINAD is a good indication over the general dynamic performance of the ADC, as it includes all contributions from noise and distortion. The higher the SINAD the stronger the input power is differentiated from noise and spurious components.

SINAD can be calculated from the average power of the input signal  $P_{\text{signal}}$ , noise  $P_{\text{noise}}$  and  $P_{\text{distortion}}$ :

$$\text{SINAD} = 10 \log \left( \frac{P_{\text{signal}}}{P_{\text{noise}} + P_{\text{Distortion}}} \right) \quad (2.24)$$

It is commonly expressed in dB, decibels relative to the carrier (dBc) or decibels relative to full scale (dBFS).

### Effective-Number-Of-Bits

The Effective Number Of Bits (ENOB) expresses the SINAD in terms of bits. It can be calculated as (see [Kes09])

$$\text{ENOB} = \frac{\text{SINAD} - 1.76 \text{ dB}}{6.02 \text{ dB/bit}}. \quad (2.25)$$

This is derived from solving the equation of the “ideal SNR” (Equation 2.14) for the number of bits  $N$  and substituting SNR with SINAD. This however means, that this parameter assumes a full-scale input signal. Expressing the ENOB for a smaller signal amplitude requires measuring the SINAD at this level and a correction factor. [Kes05]

### Spurious-Free Dynamic Range

SFDR indicates the dynamic range of the converter, which can be used, before there is interference or distortion from spurious components with the fundamental signal. [LV02] The SFDR is calculated as the RMS value of the fundamental signal to the RMS value of the worst spurious signal, i.e. the highest spur in the spectrum. It is measured over the whole Nyquist bandwidth from DC to  $f_s/2$ , with  $f_s$  being the ADC sampling rate. The spur may or may not be a harmonic of the fundamental signal. [Kes09, LV02]

The SFDR is an important characteristic in the sense, that it indicates the smallest signal which can still be distinguished from a strong interfering signal. [Kes09]

The SFDR in dBc can be calculated as (see [Xila])

$$\text{SFDR}_{\text{dBc}} = 20 \log \left( \frac{\text{Fundamental Amplitude (RMS)}}{\text{Largest Spur Amplitude (RMS)}} \right). \quad (2.26)$$

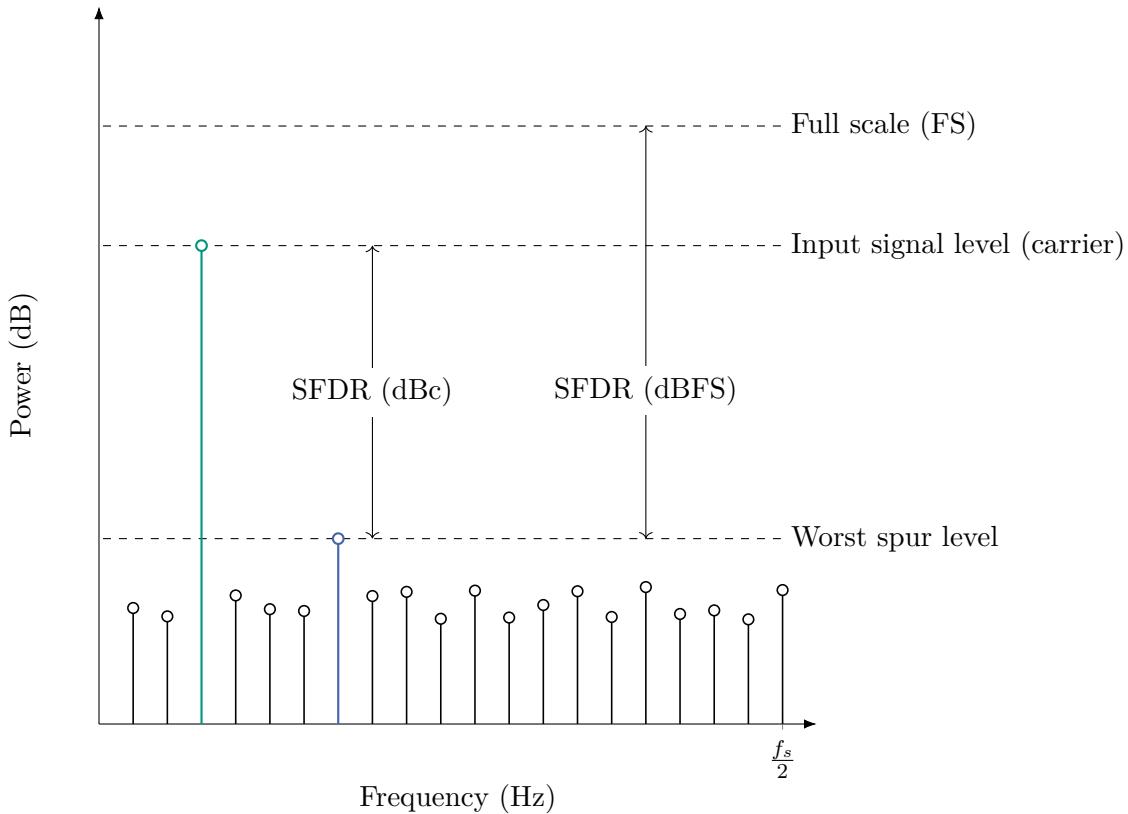
Figure 2.16 illustrates the SFDR in terms of dBFS and dBc.

### Total Harmonic Distortion

The *Total Harmonic Distortion* describes the ratio of the RMS sum of the first five harmonic components (or aliased versions of them) to the RMS of the considered fundamental signal. [LV02]

### Effective Resolution Bandwidth

*Effective Resolution Bandwidth* denotes the frequency of the input signal, at which the SINAD has fallen by 3 dB ( $\cong 0.5$  bit in terms of ENOB) compared to the SINAD at lower frequency range. [LV02]



**Figure 2.16.:** Visualization of the SFDR. It can be indicated either with reference to the carrier frequency in “dBc” or with reference to the Full-Scale Input in “dBFS”. [Kes09]

### Analog Input Bandwidth

*Analog Input Bandwidth* is the analog input frequency at which the power of the fundamental is reduced by 3dB with respect to the low-frequency value. [LV02] It is not to be confused with the maximal analog input frequency which the ADC is able to sample.

### Full-Linear Bandwidth

The *Full-Linear Bandwidth* is defined as the frequency at which the slew-rate of the SHA starts to distort the input signal by a specified value. [LV02] The slew-rate (SR) is defined as the rate of how much the voltage  $v$  changes over time  $t$ :

$$\text{SR} = \frac{dv}{dt} \quad (2.27)$$

A slew-rate of 1 V/ $\mu$ s for example means, that the output of the amplifier can not change more than 1 V over the course of 1  $\mu$ s.[Col21]

### Time-Domain Dynamic Parameters

Time-Domain Dynamic parameters describe the deviation of the converter’s behavior from the ideal one in time domain.

### Aperture Delay

*Aperture Delay* (or *aperture time*) is defined as delay between the triggering of the converter (e.g. rising edge of the sampling clock) and the actual conversion of the input voltage into the digitized value. [LV02]

### Aperture Jitter

*Aperture jitter* describes the sample-to-sample variation in aperture delay. Jitter can cause significant error in the voltage and decreases the overall SNR of a converter. Especially for high-speed ADCs jitter poses a limit in performance.

Assuming a full-scale sinus-wave  $V_{\text{in}}$  as input signal with

$$V_{\text{in}} = V_{\text{FS}} \sin(\omega t) \quad (2.28)$$

the maximal slope of this signal is then

$$\frac{dV_{\text{in}}}{dt} \Big|_{\max} = \omega V_{\text{FS}} \quad (2.29)$$

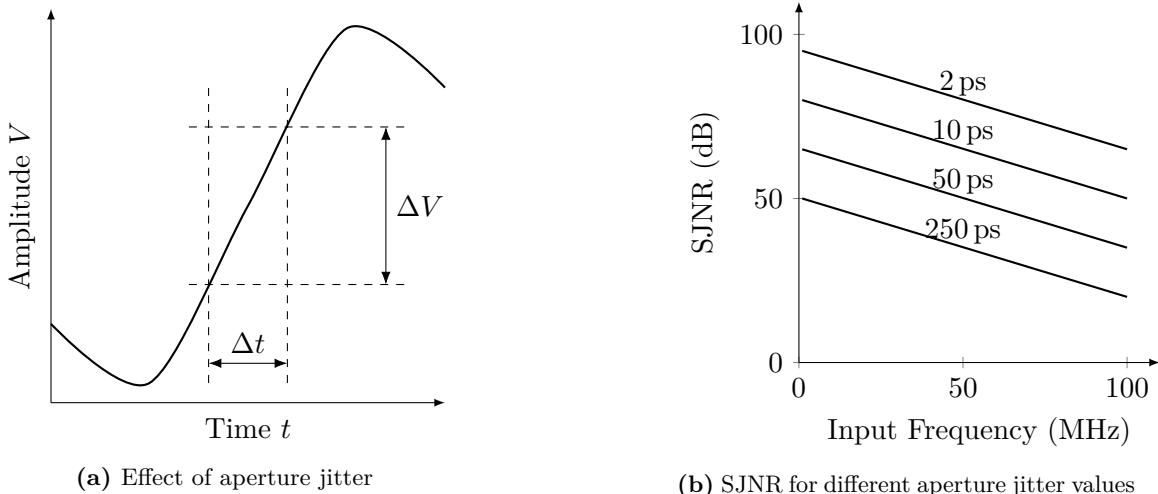
Aperture jitter  $\Delta t_{\text{rms}}$  occurring during the sampling of this maximal slope produces the RMS voltage error

$$\Delta V_{\text{rms}} = \omega V_{\text{FS}} \Delta t_{\text{rms}} = 2\pi f V_{\text{FS}} \Delta t_{\text{rms}}. \quad (2.30)$$

As variations in aperture time occur randomly, these errors behave like a random noise source. This way, a Signal-to-Jitter-Noise-Ratio (SJNR) can be defined as

$$\text{SJNR} = 20 \log \left( \frac{V_{\text{FS}}}{\Delta V_{\text{rms}}} \right) = 20 \log \left( \frac{1}{2\pi f V_{\text{FS}}} \right) \quad (2.31)$$

The voltage error due to jitter and the SJNR for different aperture jitter values are shown in Figure 2.17.



**Figure 2.17.:** Effects of aperture jitter and SJNR. Left: In time domain, Right: SJNR for different aperture jitter [LV02]

### Transient Response

The *transient response* denotes the settling time of an ADC until full accuracy ( $\pm 1/2$  LSB).

#### 2.3.1.4. Sampling Theory

An ADC samples an analog signal with a sample frequency  $f_s$ . This frequency has to be chosen in such way, that the original signal can be fully reconstructed. The *Nyquist criteria* states, that in order to accurately reconstruct continuous signal limited to the bandwidth  $B$

$$y(t) \circledcirc Y(f) \quad \text{with} \quad Y(f) = 0|_{f > B/2} \quad (2.32)$$

it has to be sampled with a frequency  $f_s$  respecting

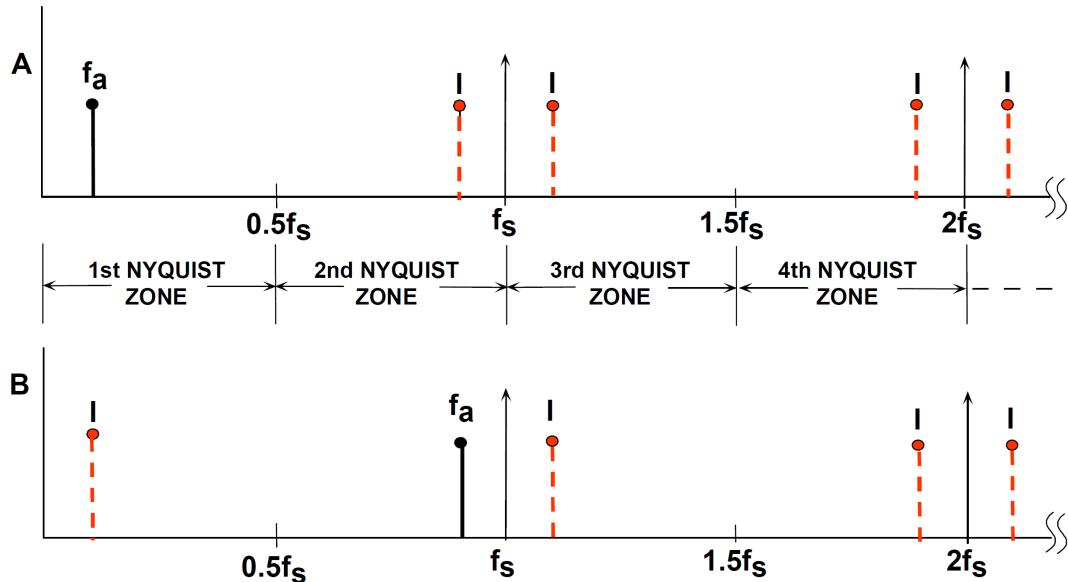
$$f_s > B \quad \text{or} \quad f_s > 2f_a, \quad (2.33)$$

with  $f_a$  being the highest frequency contained in the signal. [Kes05, Pue15] The range from 0 Hz to  $f_s/2$  is also called *Nyquist-Zone* (or “1st Nyquist zone”, see Figure 2.18a).

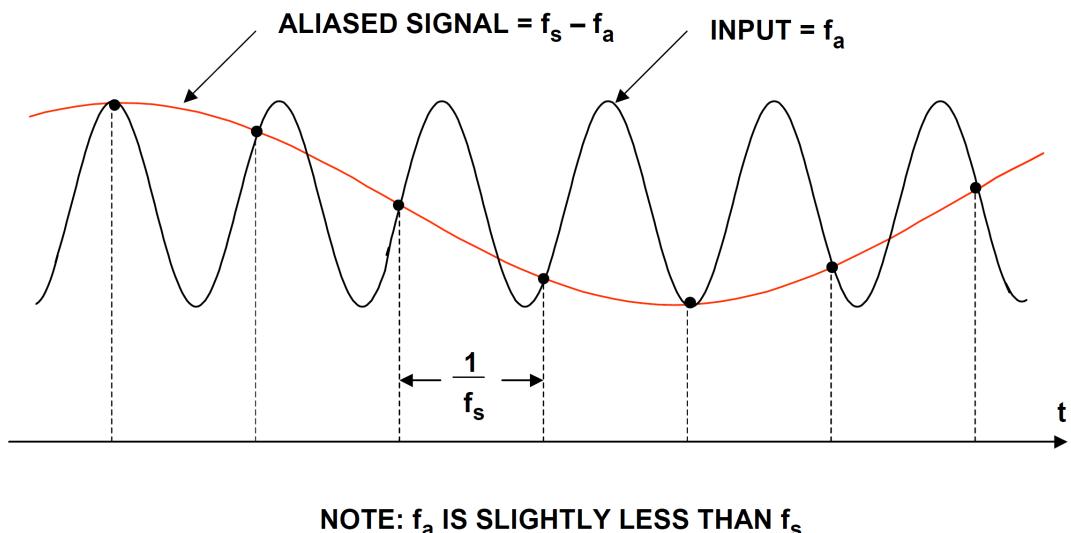
Violation of this rule leads to *aliasing*. The effects of aliasing are shown in Figure 2.18.

When a harmonic wave of the frequency  $f_a$  is sampled with the frequency  $f_s$ , this leads to periodic repetition of the signal spectrum in frequency domain in intervals of  $f_s$ , or “images” (see dashed, red frequency components in Figure 2.18a). If Equation 2.33 is respected, i.e.  $f_a$  lies inside the Nyquist bandwidth, there is no overlap with the images created by the sampling process.

Now assuming a signal frequency  $f_a \approx f_s$ , the sampling process leads to an image falling inside the Nyquist bandwidth. The reconstructed signal then lies at the frequency of this image which is much lower than the original frequency. The result of this *undersampling* is shown in Figure 2.18b.



(a) Sampling process visualized in frequency domain



(b) Effect of aliasing shown in time domain

**Figure 2.18.: Analog signal with frequency  $f_a$  sampled at  $f_s$  respecting (A) and not respecting (B) the Nyquist criteria (see Figure 2.18a). Figure 2.18b shows the effect of case B in time domain. [Kes05]**



### 3. Architecture Of The New Readout-System - THERESA

This section is dedicated to describing the general concept of the new readout-system. The system was given the name THERESA and in the sections to follow this name will be used to denote the new system.

First, a short overview of state of the art systems is given, including commercially available real-time oscilloscopes and Karlsruhe Pulse Taking Ultra-fast Readout Electronics (KAPTURE). This system was developed at Institute for Data Processing and Electronics (IPE) at KIT specifically addressing the needs of THz diagnostics at KARA. The working principle of this system is explained in detail, as the new THERESA system is an evolution of the KAPTURE system.

Then, the architecture of the THERESA system itself is described.

#### 3.1. State Of The Art Readout-Systems

##### Real-Time Oscilloscopes

Real-time oscilloscopes are defined by three key specifications: bandwidth, sample rate, and memory depth. Some examples of currently commercially available oscilloscopes are listed in Table 3.1. The acquisition time is given for the case of maximal sample rate. As can be derived from the table, the acquisition time of such oscilloscopes is quite limited, not allowing for continuous sampling of fast input signals.

**Table 3.1.:** Some example real-time oscilloscopes with (max.) key characteristics

Model	Bandwidth	Sample Rate	Memory Depth	Acquisition time
Keysight MXR608A	6 GHz	16 GS/s	1.6 GS	10 ms
Tektronix DPO70000SX	70 GHz	200 GS/s	1 GS	5 ms
LeCroy LabMaster 10-100Zi	65 GHz	160 GS/s	512 MS	3.2 ms

##### 3.1.1. KAPTURE

KAPTURE (Karlsruhe Pulse Taking Ultra-Fast Readout Electronics) is a fast readout system developed at the IPE for THz diagnostics at KARA. It is designed to digitize the pulses generated by THz detectors at each electron bunch revolution, with a memory-efficient approach to acquire the detector signal on a bunch-by-bunch basis (sampling only

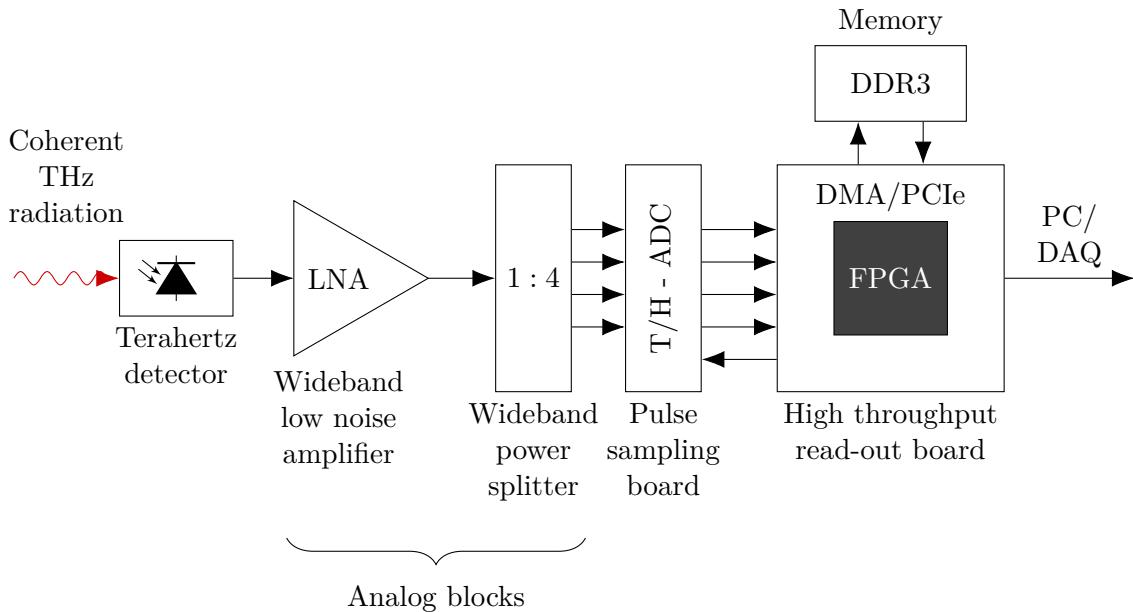
the pulses themselves). The system is able to sample pulses with a Full Width At Half Maximum (FWHM) between a few tens to a hundred picoseconds with a minimal sample time of 3 ps. [CAB<sup>+</sup>17]

To showcase the revolution of this DAQ system, the general architecture and concept is explained with the first version of KAPTURE. Then, the improved version Karlsruhe Pulse Taking Ultra-fast Readout Electronics 2 (KAPTURE-2) is presented. At the end, being a further evolution of these two versions, the architecture of THERESA is explained.

### General Concept

The system consists of two parts: the sampling front-end card and a FPGA readout card. In Figure 3.1 the setup for THz radiation measurements with KAPTURE is shown.

The incoming radiation is fed into a detector, which converts the incident photons into an electrical signal. This signal is then amplified in a wide-band Low-Noise-Amplifier (LNA). A wideband lossless power splitter, developed at IPE, splits the detector signal into four identical signals, which are then propagated to the sampling front-end card. The card consists of four parallel sampling channels with adjustable sampling time. Each channel contains a THA and an ADC. This card is connected to a read-out card by a high-speed and high-density connector. The FPGA sets the sampling time for each individual sampling channel and reads, processes and sends all acquired data to a Central Processing Unit (CPU)/Graphics Processing Unit (GPU) cluster for further processing. [CBC<sup>+</sup>14]



**Figure 3.1.:** THz radiation measurement setup with KAPTURE (redrawn from [CBC<sup>+</sup>14])

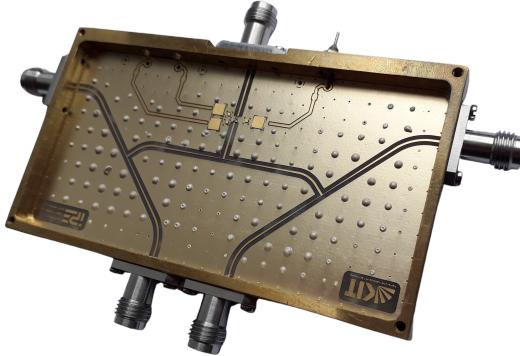
### Analog Front-End

Due to the high bandwidth nature of the detector signal, the analog front-end of the system has to be wideband as well to be able to sample the signal with picosecond resolution.

The used LNA is based on a commercial GaAs Microwave Monolithic Integrated Circuit (MMIC) which operates from DC to 50 GHz. It is needed to compensate the insertion loss<sup>1</sup> of the following power-splitter stage. Classical power-splitters are not intrinsically

<sup>1</sup>Insertion loss is the loss of signal power which occurs, when a signal passes through a component.

wideband ([CBC<sup>+</sup>14]). For that reason, an wideband power-splitter was developed at IPE which fulfills the bandwidth requirements. The designed power-splitter works up to 100 GHz with an insertion loss of 8 dB (at 100 GHz) and a return loss<sup>2</sup> of about 20 dB at 50 GHz. [CBC<sup>+</sup>14] A photo of the power-splitter is shown in Figure 3.2.



**Figure 3.2.:** Photo of the power splitter developed at IPE

### Sampling Board

The architecture of the front-end board with the power-splitter is shown in Figure 3.3.

The power-splitter splits the incoming signal into four identical signals, which are then fed into four parallel channels, consisting of a respective THA unit and a 12-bit ADC sampling at 500 MS/s. The sampling time of each unit can be adjusted individually with a delay chip with a resolution of 3 ps (maximal delay range: 100 ps). The delay chips are programmed with the FPGA on the readout card. The clock signal is provided by KARA, which is cleared from jitter by a Phase-Locked-Loop (PLL). This ensures the synchronization of the ADCs with the RF system. The cleaned clock signal is distributed to the delay chips via fan-out buffer [CAB<sup>+</sup>17]. In this way, the pulse can be “locally sampled” by adjusting the different delay with a maximum rate of 330 GS/s possible. A simplified representation of the local sampling of the signal is shown in Figure 3.4.

### GPU-DAQ System

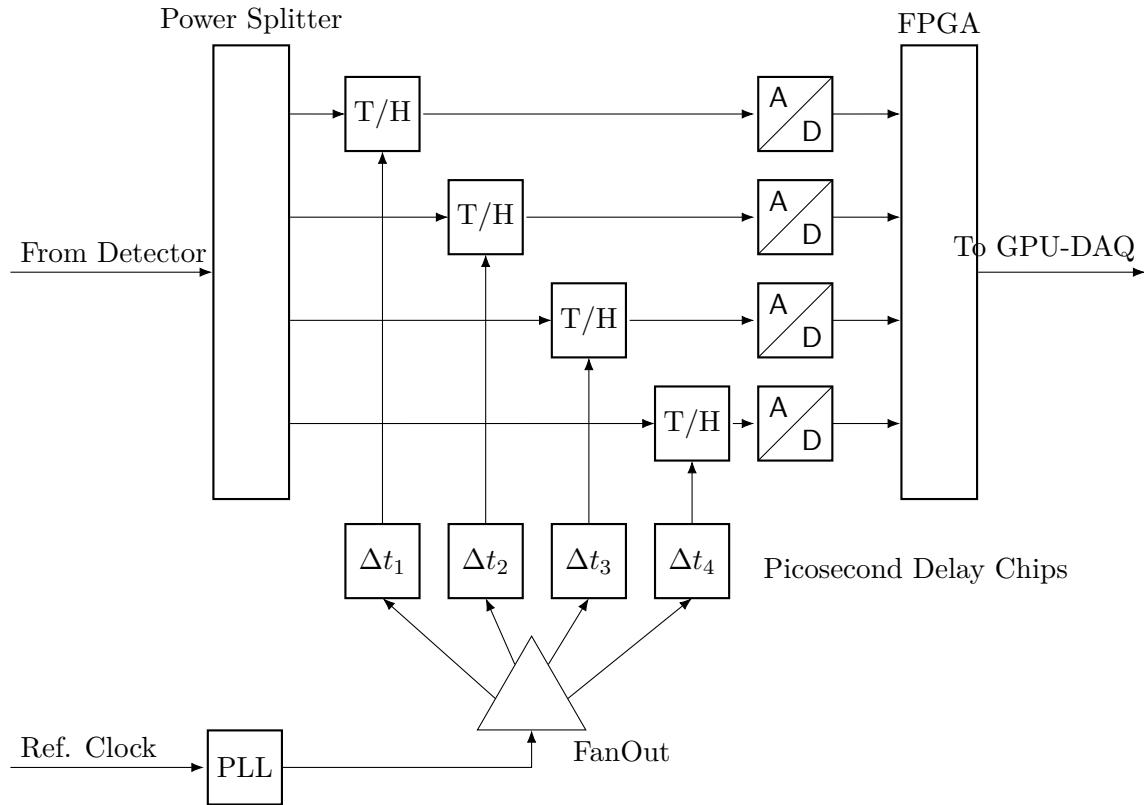
The sampling system produces a large amount of data. In order to keep a continuous data acquisition the necessary bandwidth is

$$12\text{bits} \cdot 8 \text{ samples} \cdot 1 \text{ GHz} = 96 \text{Gb/s} \quad (3.1)$$

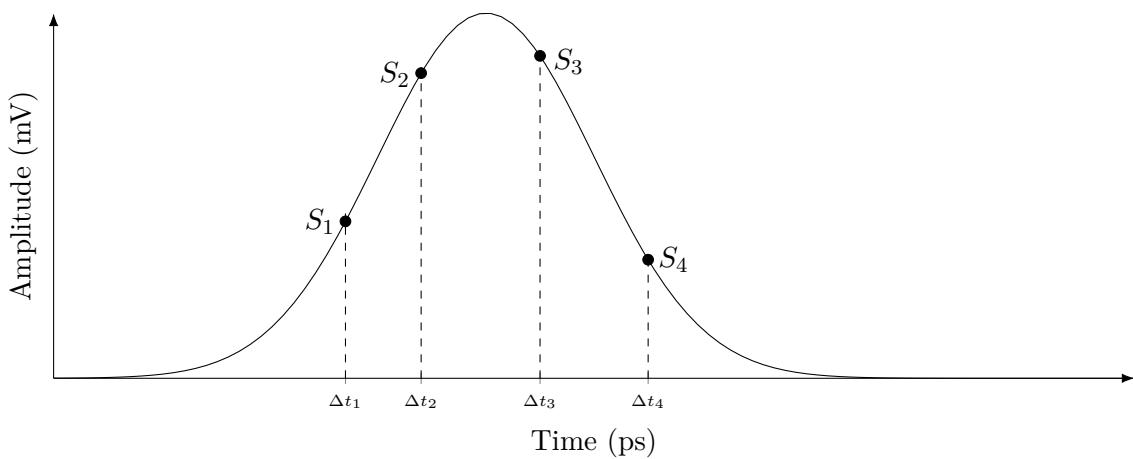
To ensure high data throughput, a high-speed PCI Express (PCIe) readout card was developed (called “High-Flex”) was developed. This card receives the samples and tags them with the respective bunch identification. The data is then sent to a GPU using a PCIe connection based on direct FPGA-GPU direct memory access architecture. The GPU node reconstructs the pulse based on the given sampling points and calculates the amplitude and pulse arrival time. It also performs an online FFT for frequency analysis. To store the data temporary before it is sent to the DAQ system, a large Double Data Rate Gen 3 (DDR3) memory device is used, as seen in Figure 3.3. [CAB<sup>+</sup>17]

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<sup>2</sup>*Return loss* is the loss of signal power due to reflection by a discontinuity in the transmission line.



**Figure 3.3.:** General architecture of the KAPTURE front-end sampling card (cf. [CAB<sup>+</sup>17, p.2])

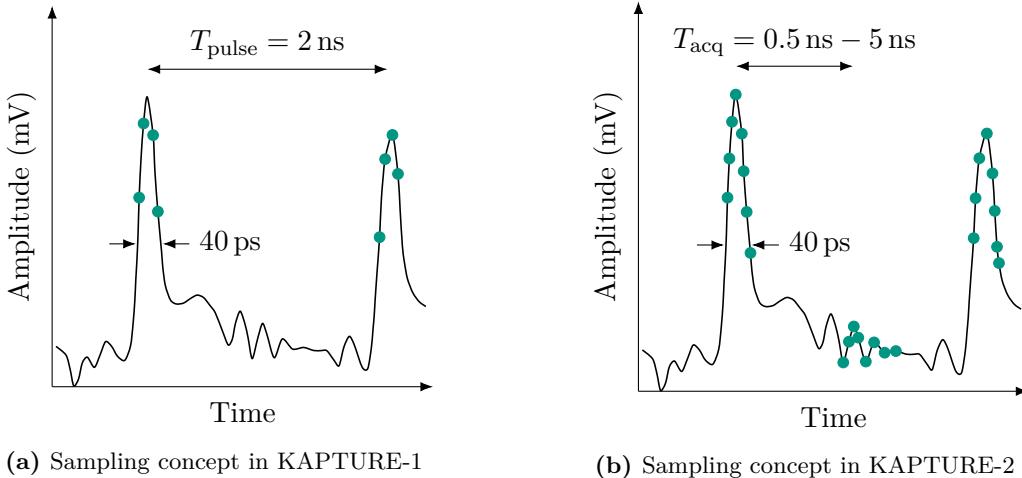


**Figure 3.4.:** Signal and sampled points  $S_1$  to  $S_4$

### 3.1.2. KAPTURE-2

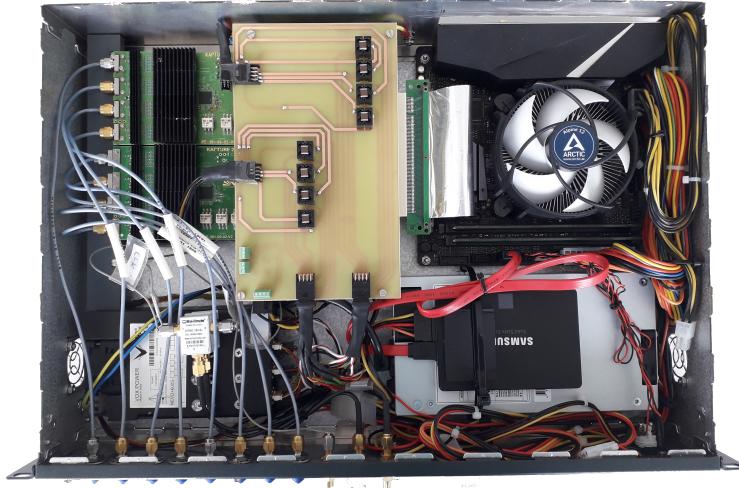
The first version of KAPTURE has a limitation concerning the number of sampling points per pulse and does not allow to sample the baseline of the detector. Analyzing the baseline however is very important, as it is changing slightly and affects the pulse amplitude of the bunch. Due to this distortion, calculating the correlation between bunches was limited. For this reason, a second version of KAPTURE was designed in order to overcome these limitations. The PLL on the sampling board allows for synchronization between two or more PLLs located on different boards. With this feature, the sampling time of two boards can be synchronized and in this way extend the number of sampling points beyond four. A comparison of the sampling concepts is shown in Figure 3.5.

In KAPTURE-2, two front-end boards can be connected to directly sample the pulses with up to eight sampling point at the pulse repetition rate 2 GHz. Alternatively, the system can sample the pulse and the baseline between two consecutive pulses with a constant pulse rate up to 1 GHz (see Figure 3.5b). In this way, the read-out card can calculate the correct amplitude of the pulse and send it to the GPU for further processing [CAB<sup>+</sup>17].



**Figure 3.5.:** Comparison between the sampling concepts of KAPTURE-1 and KAPTURE-2

Figure 3.6 shows a photo of the system setup of KAPTURE-2.



**Figure 3.6.:** Photo of the KAPTURE-2 setup

### 3.2. Proposed Architecture for THERESA

In this section the architecture for the THERESA system is described. The system consists of the optical time-stretch setup, which stretches the analog input signal and the photodetector in order to convert the optical signal into an electrical one. This signal is sampled by a front-end sampling card, which is mounted on a back-end readout card, which processes the acquired samples.

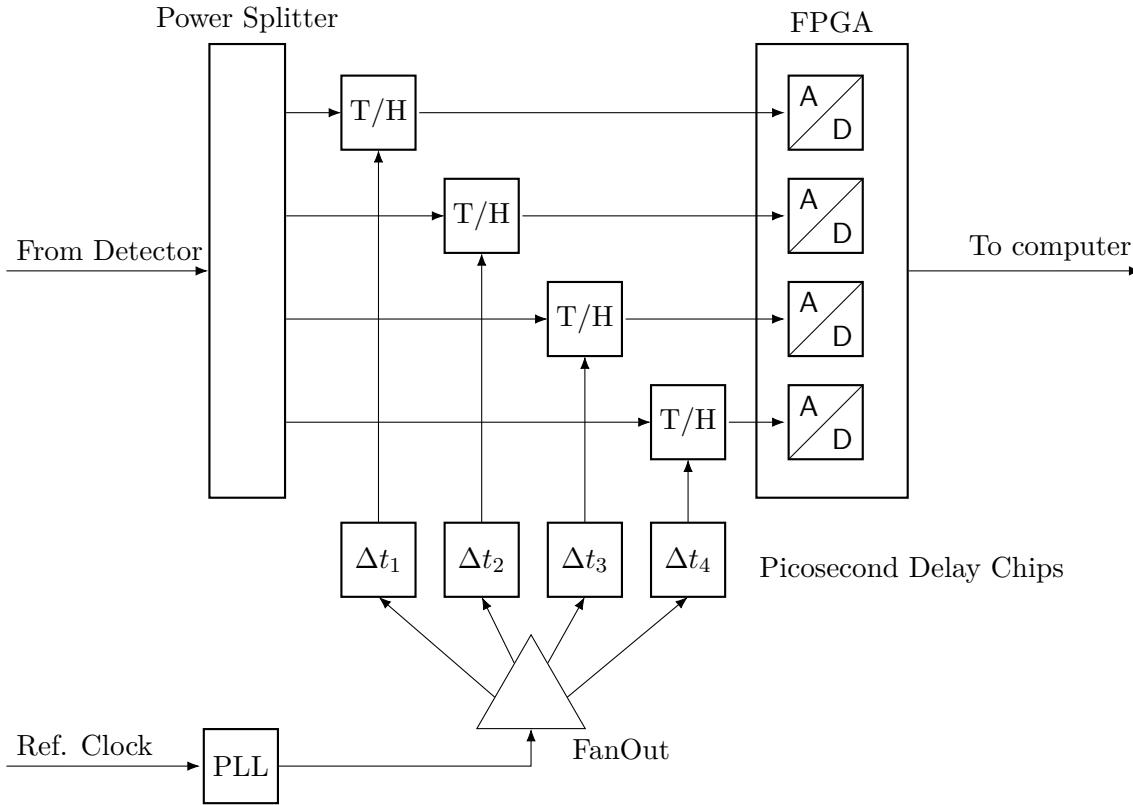
#### Optical Part

For the optical time-stretch setup, a femtosecond Ytterbium-doped fiber laser from *MENLO GmbH* is used. The emitted pulses have a bandwidth of 50 nm and a total output average power of 40 mW. The photodetector used is an InGaAs photodiode from *Discovery Semiconductors* with a 20 GHz bandwidth.

##### 3.2.1. Front-End Sampling Card

The concept of the front-end sampling card is based on and an evolution of the concept used in the KAPTURE system.

The incoming signal is split into 16 identical signals, each leading to the respective sampling channel on the sampling board. These sampling channels consist of a high bandwidth (18 GHz), low noise THA. The sampling clock to these THAs is provided by respective programmable delay chips. In this way, a time interleaving technique (described below) can be implemented by programming the delay chips accordingly. The main clock is provided by a main PLL, which cleans the reference clock coming from the system in which the sampling system is integrated. Figure 3.7 shows the general schema of the sampling system, reduced to four channels for presentation purposes.



**Figure 3.7.:** General architecture of the THERESA sampling card with power splitter and ADCs. For presentation purposes only four of the sixteen channels are shown.

### 3.2.1.1. Time Interleaving

In order to increase the sampling rate, the so called time-interleaving technique is used. In this section, first basic theory about this technique is given. Then, the implementation in the new system is described.

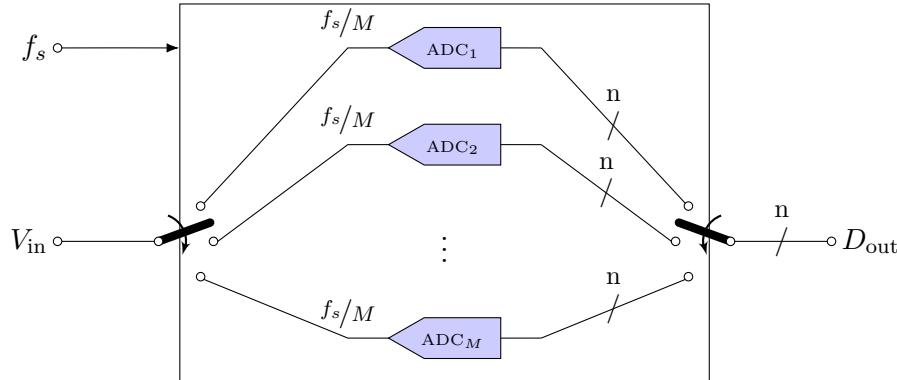
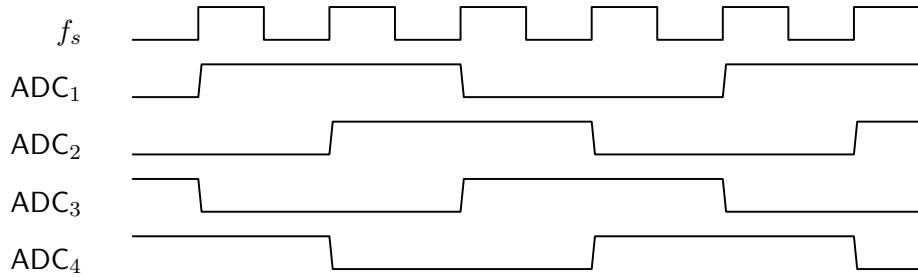
#### Theory

In the *Time Interleaving* technique multiple ADCs are used in such way, that allows to sample data at a faster rate than the respective sample rate of each individual ADC. The principle is based on time-multiplexing an array of  $M$  identical ADCs (see Figure 3.8a), each operating at a sampling rate of  $f_c = f_s/M$  individually. The sampling times of the ADCs are shifted in phase as shown in Figure 3.8b with the example of 4 time-interleaved ADCs. At time  $t_0$  the first ADC starts converting the input signal  $V_i(t_0)$ , after a defined time delay  $\Delta t_i$  the second ADC samples and converts  $V_i(t_0 + t_i)$ , the third converts  $V_i(t_0 + 2t_i)$  and so on. After the  $M$ -th ADC has sampled the signal  $V_i(t_0 + (M - 1)t_i)$ , the whole cycle starts anew with the first ADC [MR15]. An example for such a cycle for 4 ADCs is shown in Figure 3.8b.

#### Challenges

Spurs appear in the spectrum. There are several reasons for this which are described in the following.

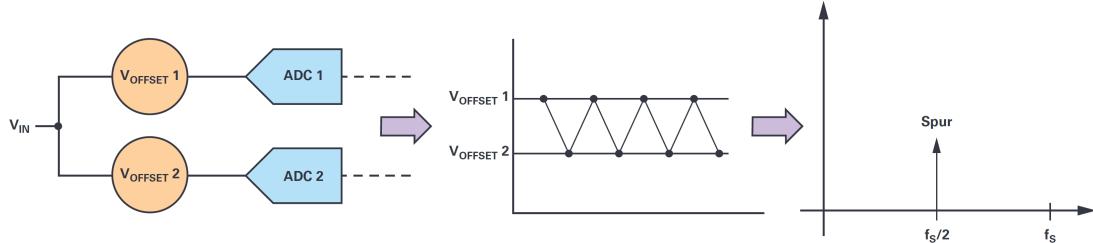
First reason is the *offset mismatch* between the ADCs. Each ADC is characterized by a DC offset. Considering an interleaving structure with two ADCs and a constant input voltage: when the samples are acquired back and forth between the two ADCs, the resulting output will switch back and forth between two levels due to the different offset

(a) An array of  $M$  time interleaved  $N$ -bit ADCs [MR15]

(b) Clocking Scheme for interleaving 4 ADCs

**Figure 3.8.:** Array of  $M$  time interleaved ADCs and clocking example for  $M = 4$ 

levels of the ADCs. This output switches at the frequency  $f_s/2$ . Therefore this introduces spurious harmonic components at the frequency  $f_s/2$  in the spectrum (see Figure 3.9). The magnitude of the spur depends on the offset difference between the ADCs. [Har19]

**Figure 3.9.:** Offset-Mismatch in Interleaving [Har19]

Besides of the offset also the gain of the converters can be mismatched. This *gain mismatch* has a frequency component to it, which in case of an input signal of the frequency  $f_{in}$  results in a spur at  $f_s/2 \pm f_{in}$  (see Figure 3.10). [Har19]

In the time domain, *timing mismatch* due to group delay in the analog circuitry of the ADC and clock skew<sup>3</sup> can occur. The group delay in analog circuitry can vary between the converters. The clock skew has on the one hand an aperture uncertainty component at each of the ADCs. On the other hand it has a component related to the accuracy of the clock phases, which are input to each converter. [Har19] This mismatch also produces a spurious component at  $f_s/2 \pm f_{in}$  (see Figure 3.11).

The last possible mismatch is the *bandwidth mismatch*, which contains both gain and phase/frequency component (see Figure 3.12). Due to bandwidth mismatch, different gain

<sup>3</sup>Difference in arrival time of the clock signal at different components.

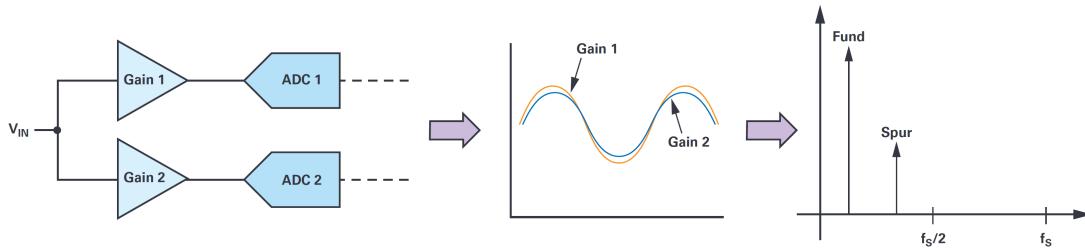


Figure 3.10.: Gain-Mismatch in Interleaving [Har19]

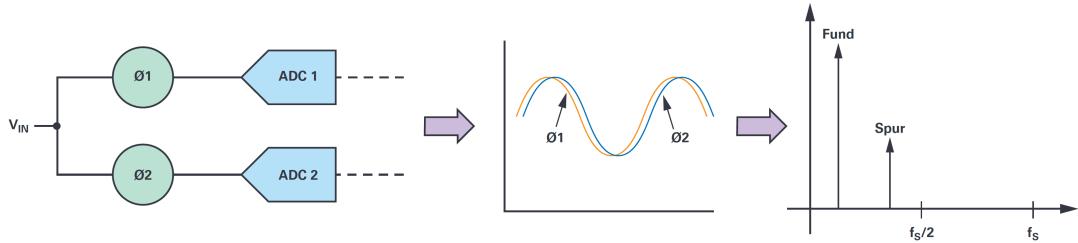


Figure 3.11.: Timing-Mismatch in Interleaving [Har19]

values at different frequencies can be seen. An additional timing component causes different delays for signals at different frequencies through each ADC. Just like gain and timing mismatch, the bandwidth mismatch causes a spur at  $f_s/2 \pm f_{in}$ .

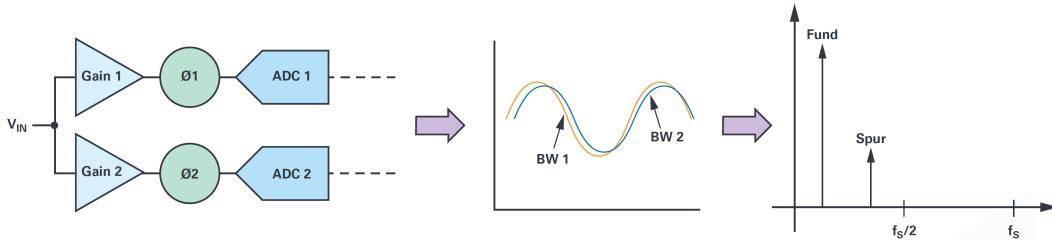


Figure 3.12.: Timing-Mismatch in Interleaving [Har19]

Due to the presented mismatches, a proper characterization of the ADCs. The characterization is required in order to account for all systematical errors in the ADCs and to reduce the spurious components in the spectrum. For this purpose, a circuit on the THERESA sampling board is foreseen, in order to provide the possibility to generate test signals from the readout card.

### 3.2.1.2. Implementation

On the selected readout card for THERESA, 16 ADCs with a sampling rate up to 2.5 GHz are present. In order to implement the time-interleaving method, an appropriate delay step size for the sample time has to be calculated. To calculate the maximal step size possible can be calculated as follows: The ADCs on the read-out card sample at a maximal sample rate of 2.5 GS/s, meaning during the time

$$t_s = \frac{1}{2.5 \text{ GS/s}} = 400 \text{ ps} \quad (3.2)$$

all 16 ADCs have to sample the signal one time. This means, a delay step can not be greater than  $400 \text{ ps}/16 = 25 \text{ ps}$ . With this method, the maximal achievable sampling rate of the card is  $16 \cdot 2.5 \text{ GS/s} = 40 \text{ GS/s}$ .

On the selected readout card, sampling clock signals are not propagated individually to the respective ADCs. The converters are grouped together into tiles, each tile containing four converters. One single reference clock signal is propagated to all tiles. To implement the optimal time-interleaving method with this card, four individual sampling clocks to all tiles shifted by 90° would be necessary. Analyzing the schematic of the readout board revealed however, that only two individual sampling clocks can be provided to the card.

Therefore, another approach needs to be considered. Figure 3.13 shows qualitatively the concept. The main 1 GHz clock is propagated to the THAs, which are in hold-mode when the clock signal is HIGH and in track-mode when the clock signal is LOW. As shown in Figure 3.13 the clock signal to each THA is provided with a respective delay. The maximal delay step size to cover the whole period of the clock is calculated by:

$$\frac{1 \text{ ns}}{16 \text{ channels}} = 62.5 \text{ ps} \quad (3.3)$$

In some way, this implementation can therefore also be regarded as time-interleaving, as each THA holds a different sample point in time, which can then be converted by the ADCs. The two sampling clocks, indicated with “ADC1” and “ADC2”, need to be phase-shifted by 180°. In this way, an alternate clocking of the ADCs is made possible<sup>4</sup>.

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<sup>4</sup>As can be derived from the diagram, only the four respective ADC channels should be considered for signal conversion during one sampling point.

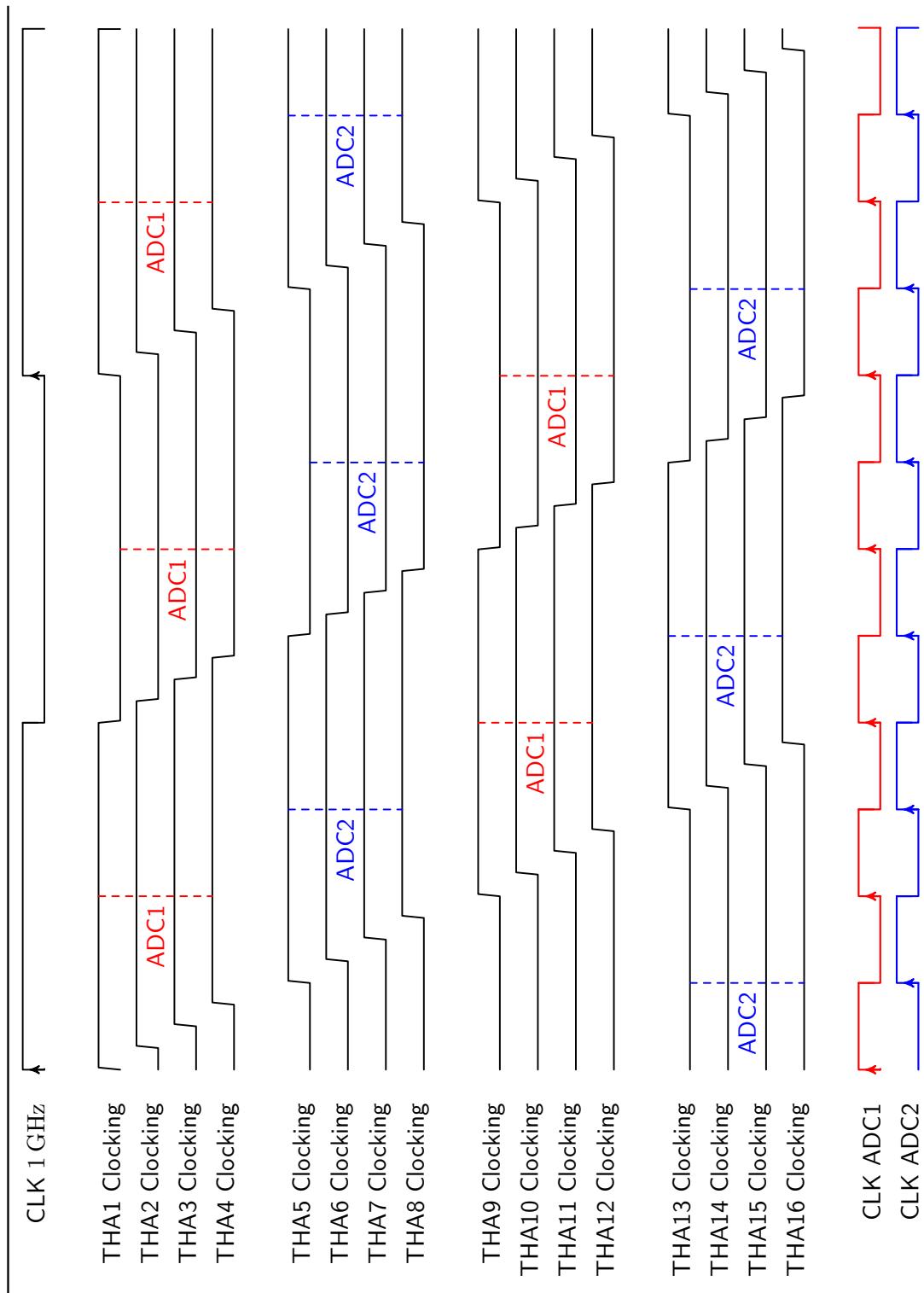


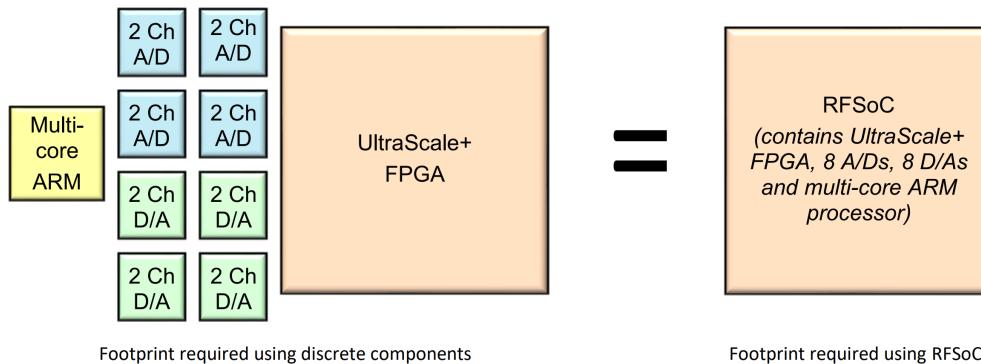
Figure 3.13: THA Timing diagram. Shows the clocking of the THA (HIGH = hold mode, LOW = track mode). Dashed line represents the sampling of the ADC.

### 3.2.2. Readout Card

The most important points to consider when choosing the readout card is its capability to handle high data-throughput, provide the possibility for user-defined firmware and control of the system. This flexibility is provided by FPGA-based System-On-Chips (SoCs), which also integrate the required high-speed peripheral connections for data transfer. An important point for THERESA is also to integrate the ADCs inside the SoC. The reason for this is illustrated in Figure 3.14. In order to fulfill the requirements, the system would need a processing unit, an FPGA and a number of data converters (ADC/DAC). Realizing this in discrete components results in a higher footprint, than integrating every component inside one Integrated Circuit (IC).

Integration of the necessary components inside an IC also drastically reduces the complexity of the sampling board. Implementing the data converters in a discrete way would result in a high number of interfaces/connections, especially for a high ADC resolution, making expensive high pin count connectors necessary. Integrating the converters inside the SoC therefore resolves these challenges.

The currently only commercially available system, meeting the mentioned requirements, is the Xilinx ZU49DR Zynq Ultrascale+ Radio-Frequency System-On-Chip (RFSoC). This SoC integrates 16 high-speed data converters (ADCs and DACs), ARM processor cores and programmable logic (the FPGA). An evaluation card, containing all necessary peripherals (optical interfaces, USB-interface, ...) and integrating the RFSoC, was chosen for the implementation of the THERESA system. The card is described in detail in chapter 5.



**Figure 3.14.:** Footprint of discrete components vs. footprint of IC integrating the components

## **4. Design Of The Front-End Sampling Card**



## 5. Back-End Readout Card and System Integration

The back-end readout card for the system under development, the Zynq UltraScale+ RFSoC ZCU216 Evaluation Card, has been chosen taking into consideration the points described in ???. In this section, the overall architecture and features of the card are presented. A possibility for evaluation of the card is also demonstrated. At last, a design for the read-out firmware is proposed.

### 5.1. Xilinx ZCU216 Evaluation Card

The ZCU216 Evaluation Card is equipped with the ZU49DR Zynq Ultrascale+ RFSoC (Gen 3). It allows for quick evaluation of the on-chip RF data converters and quick prototyping of different user-defined systems.

The features which are important for the designed read-out system are listed in the following:

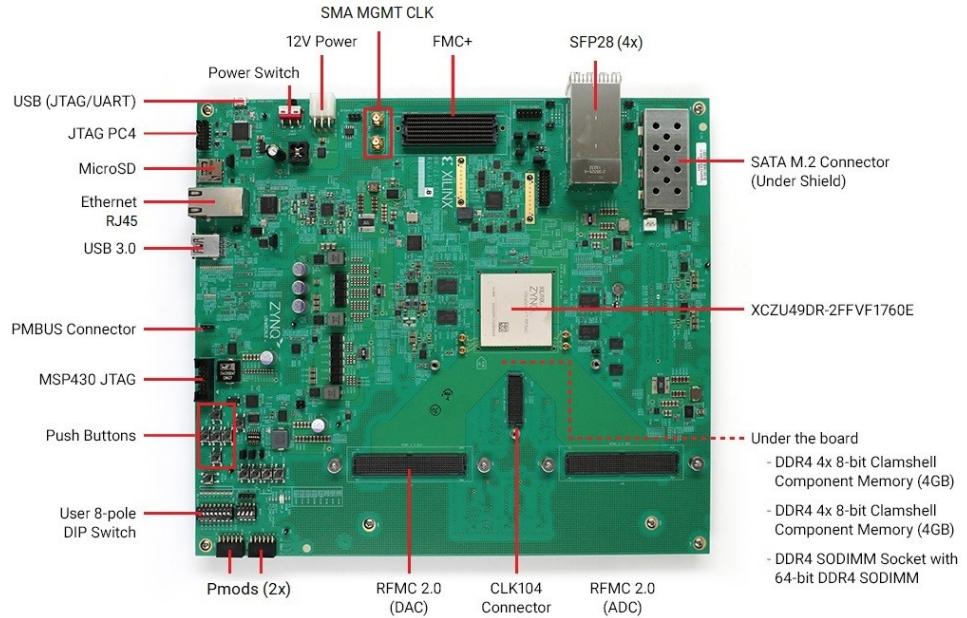
- Sixteen 14-bit, 2.5 GS/s RF-ADC
- Sixteen 14-bit, 10 GS/s RF-DAC
- I/O expansion options: FPGA Mezzanine Card (FPGA Mezzanine Card (FMC)+) interfaces, RFMC 2.0 interfaces, and Pmod (peripheral module) connections
- Double Data Rate Gen 4 (DDR4) Dual In-Line Memory Module (DIMM) – 4 GB, 64-bit, 2.666 MT/s, attached to the programmable logic (PL)
- DDR4 Small Outline Dual In-Line Memory Module (SODIMM) – 4 GB, 64-bit, 2.400 MT/s, attached to the processing system (PS)
- High-speed I/Os: 2x2 Small Form-Factor Pluggable (SFP)/SFP+/zSFP+/SFP28 modules
- Breakout cards for evaluation of the ADC and DAC performance, together with a clock add-on card for internal/external reference clocking

Other peripheral connections and features are shown in the top view of the board in Figure 5.1.

#### ZU49DR RFSoC

Together with an UltraScale+ programmable logic, the ZU49DR RFSoC integrates an ARM®Cortex™-A53 PS. This PS contains a 64-bit quad-core ARM®Cortex™-A53, serving as Application Processing Unit (APU), and a dual core ARM Cortex-R5F, serving as Real-Time Processing Unit (RPU). Furthermore, the system integrates RF data converters, allowing to use the system for RF applications. At the moment of writing, this is the industry's only single-chip, adaptable radio platform. [Xilb] This setup allows to

Figure 5.2 shows the general block diagram of the RFSoC.



**Figure 5.1.:** Topview of ZCU216 evaluation board with labeled components

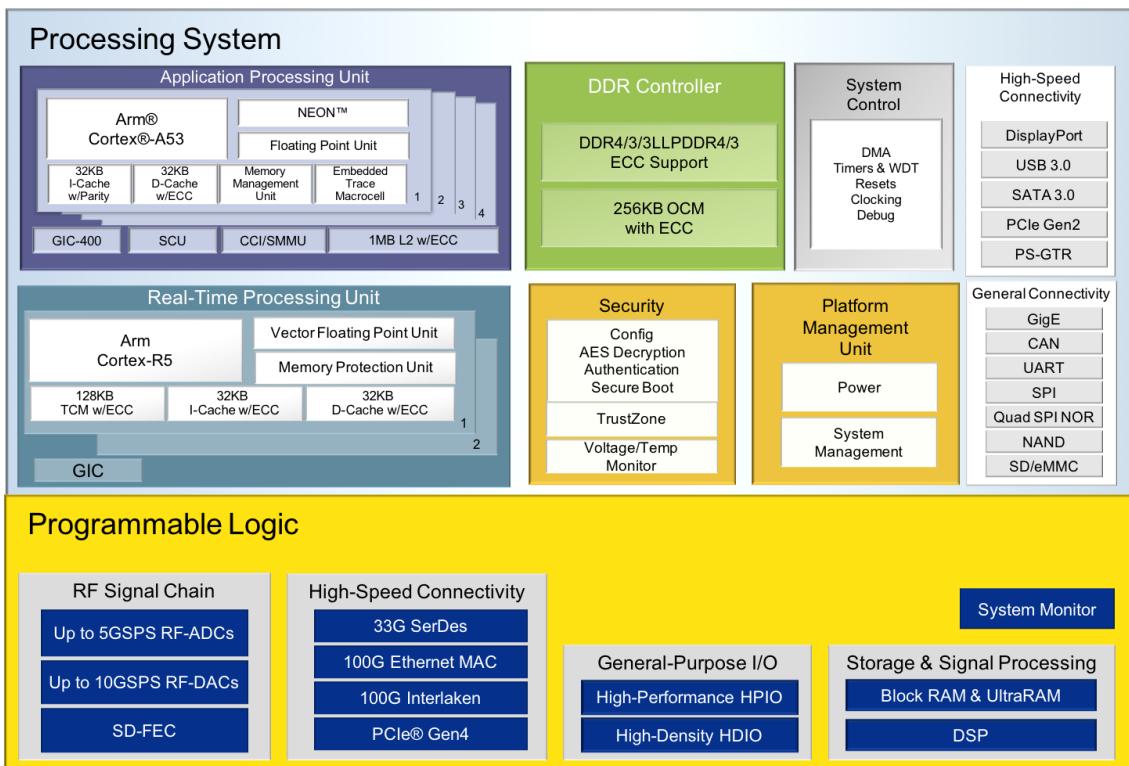
### Evaluation Tool

In order to provide a quick evaluation of data converter performance an evaluation framework from Xilinx can be deployed on the card (see Figure 5.3).

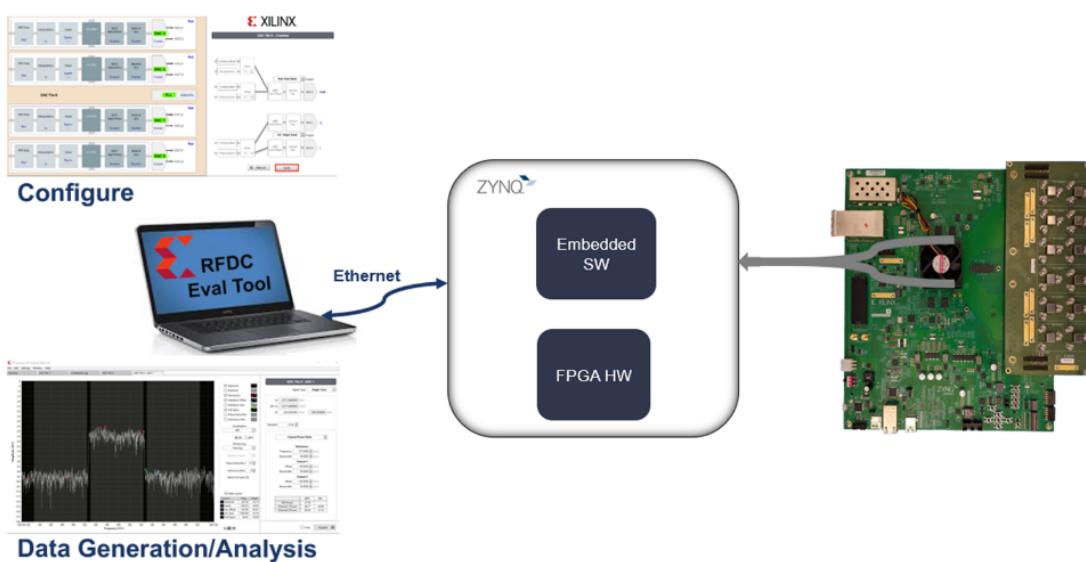
It enables control of the ZCU216 Intellectual Property (IPs) and the associated designs from a host PC. With the tool, different RF configurations can be explored, RF data can be generated and captured and different RF metrics (see subsection 2.3.1) can be observed. For this, the breakout card provided with the board, or any other user-designed board, needs to be attached to the evaluation card via the RFMC connectors.

The RF DC (Data Converter) Evaluation Tool consists of two parts:

- Hardware design on the PL/FPGA, in order to implement the configuration and data generation/capture of the data converters. It is built around the RF Data Converter IP Core from Xilinx, described in section 5.2.
- Software design on the PS and host PC, in order to control the hardware implemented on the FPGA. On the PS a Linux application receives commands from the host PC Graphical User Interface (GUI) over Ethernet. Based on the commands, it performs the according action, e.g. setting the sampling clock or enabling/disabling data converter channels. The GUI provides a convenient possibility to configure the data converters. Data generation via DACs can be started, as well as data capture with the ADCs. Furthermore, the tool provides methods to quickly characterize the performance of the data converters (see Figure 5.4) from which the performance of the plugged break-out board can be derived.



**Figure 5.2.:** Zynq Ultrascale+ RFSoC block diagram, showing in detail the different components of the PS and PL



**Figure 5.3.:** Concept of the Evaluation Tool for the ZCU216, showing the interactions between the host PC and the board

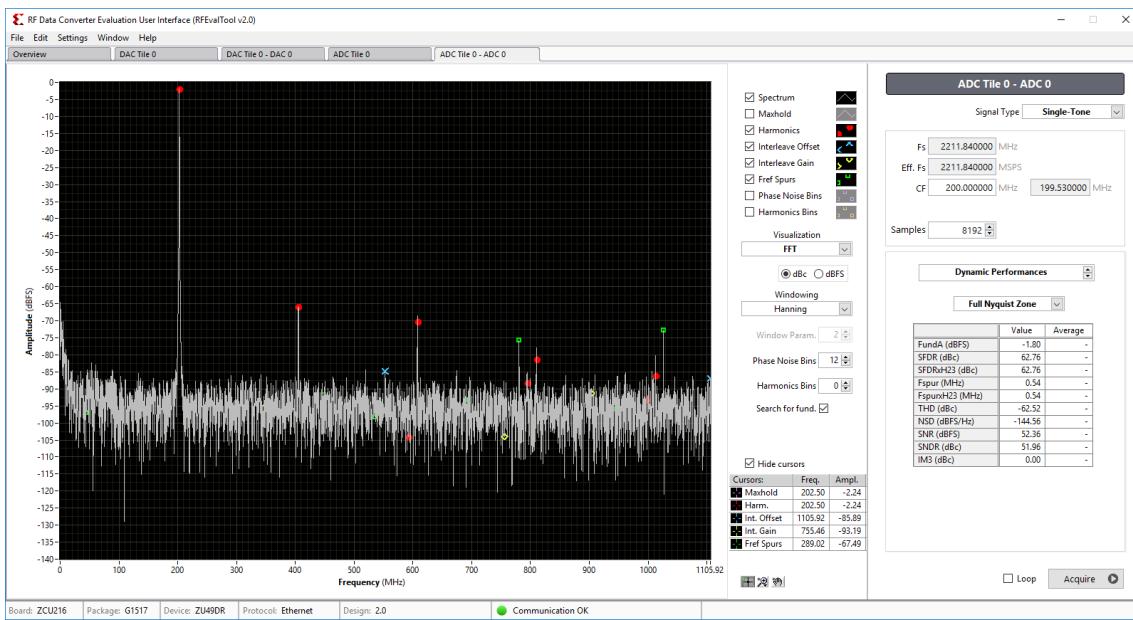
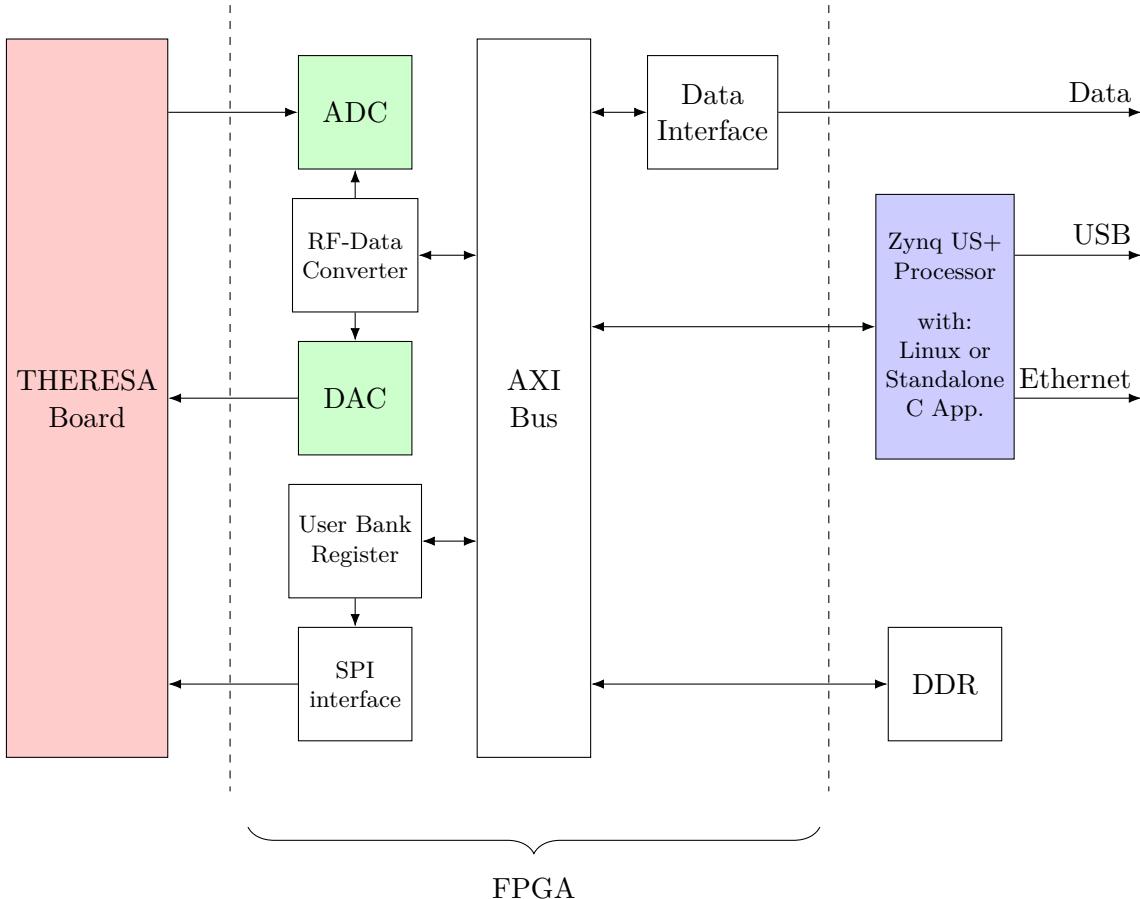


Figure 5.4.: GUI of the RF Data Converter Evaluation Tool

## 5.2. Firmware

Similar to the evaluation tool, the firmware for the readout system should contain a software part on the PS which allows for control and configuration of the data converters. The hardware design part should implement the interface to the sampling board. This means it should provide the necessary interfaces to configure the data converters on the readout card, as well as slow control to the delay chips and PLLs on the sampling board (i.e. through Serial Data Interface (SDI) and Serial Peripheral Interface (SPI)). Furthermore, the high-speed data-throughput interface should be implemented.

Figure 5.5 shows the general schematic of the firmware on the readout card.



**Figure 5.5.:** Schematic of the firmware and processing unit on the readout card

The sampled data is propagated from the sampling card to the ADCs inside the FPGA. This data is written in the Double Data Rate (DDR), from which it is accessible by the data interface, which is responsible for the high-speed data transfer to the following processing node in the DAQ system. A built-in test-loop is implemented with an integrated DAC, in order to produce test signals which are propagated to the sampling board. Configuration of the data converters is done via the Xilinx “RF Data Converter” which is described below.

Components on the sampling board, such as the delay chips, are controlled via SPI interface. This interface is connected to a user bank register, where the user can specify e.g. the desired delay values.

The PS communicates with the PL via Advanced eXtensible Interface (AXI). AXI is a parallel, synchronous, multi-master, multi-slave communication interface. On the PS an operating system, e.g. Linux, or a standalone C application, can run implementing

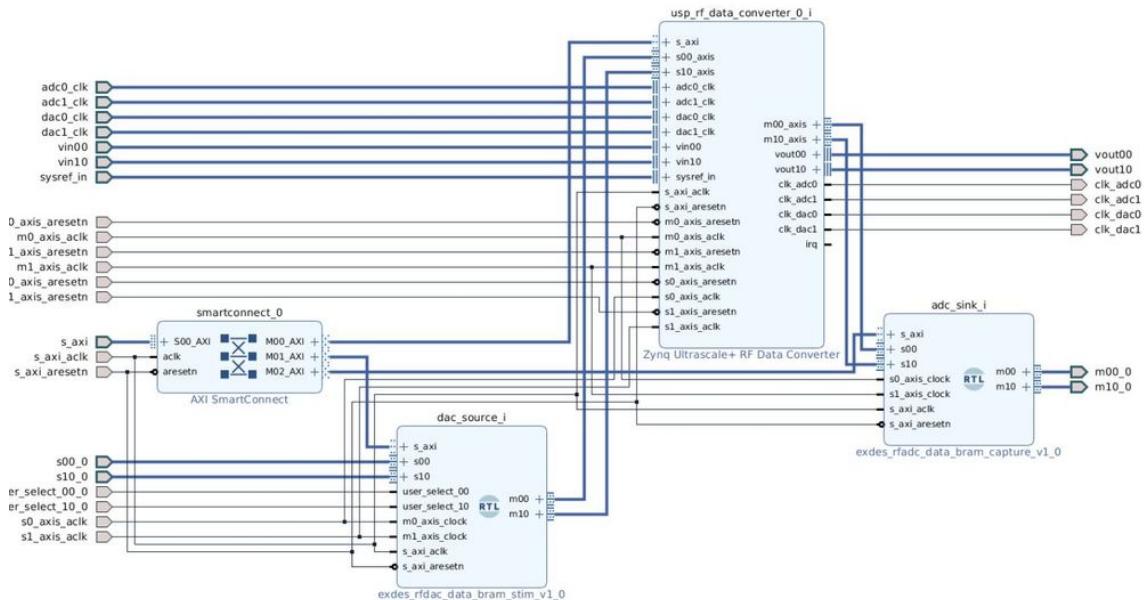
functionalities for the user to be able to control the overall system. Access to the PS is provided by for example via Ethernet or Universal Serial Bus (USB).

### 5.2.1. Programmable Logic - Hardware design

For synthesis and analysis of the Hardware Description Language (HDL) design for the PL, the Integrated Design Environment (IDE) Xilinx Vivado IDE is used. To configure and control the data converters, the RF Data Converter IP Core from Xilinx is used. In order to program the components on the sampling board, appropriate SPI interfaces are implemented, respecting the recommendations in the data sheet.

#### RF Data Converter IP Core

In order to configure the data converters, the HDL design should be based around the Xilinx RF Data Converter IP Core.

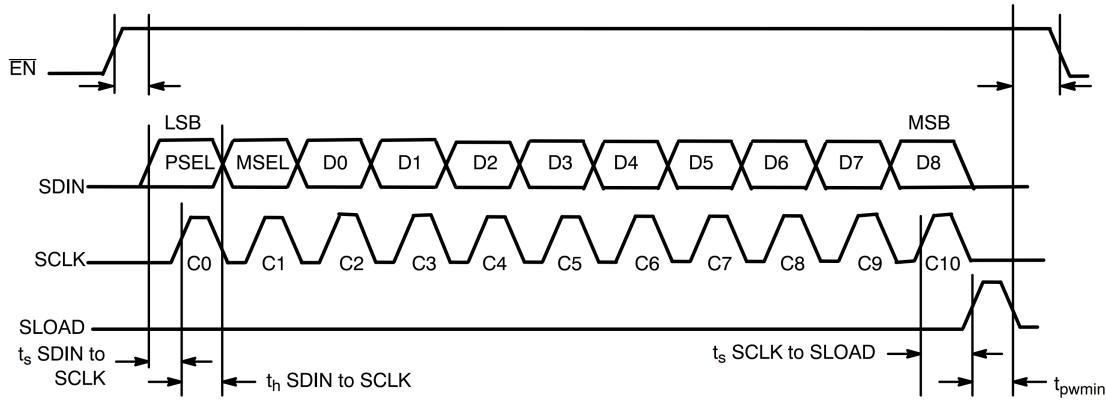


**Figure 5.6.:** Simple example design with the RF Data Converter

#### Slow Control

Components on the sampling board are controlled via a slow control interface. As example, the on-board delay chips are controlled via a SDI interface, consisting of four signals: EN, SDIN, SCLK and SLOAD. In order to program a certain delay, the timing diagram shown in Figure 5.7 has to be respected. The delay chip only accepts data when the EN input is HIGH. Therefore, this signal has to remain high in the course of the whole data transaction. The data pin, SDIN, which is clocked in by the SCLK signal, has to respect the following structure: delay channel select bit, mode select bit, followed by 9 data bits, which represent the desired delay value in binary format. At the end, SLOAD has to be asserted HIGH, in order to signal the chip to load the received data into the chip's internal register. The HDL implementation for this interface is listed in the appendix.

In a similar way, the interface for other components is to be implemented.



**Figure 5.7.: SDI timing diagram for the NB6L295 delay chip [ON ]**

### RDMA over Converged Ethernet (RoCE)

Remote Direct Memory Access (RDMA) is a direct memory access from the memory of one computer into that of another without involving either one's operating system. This permits high-throughput, low-latency networking, which is especially useful in massively parallel computer clusters.

RDMA over Converged Ethernet (RoCE) is a network protocol defined in the InfiniBand Trade Association (IBTA) standard, allowing RDMA over converged Ethernet network. Shortly, it can be regarded as the application of RDMA technology in hyper-converged data centers, cloud, storage, and virtualized environments. It has all the benefits of the RDMA technology and the ease of use and availability of Ethernet.

The ERNIC (Xilinx Embedded RDMA enabled NIC) IP provides an Initiator and Target implementation of RDMA over Converged Ethernet Version 2 (RoCEv2) enabled Network Interface Controller (NIC) functionality. This IP is specifically designed for embedded applications that require reliable transmission over Ethernet networks.

#### 5.2.2. Processing Unit - Software Design

In order for the user to be able to control the whole system, some kind of application has to be implemented for control of the hardware design. For this the PS side of the RFSoC is used. The ARM Cortex processor allows to implement standalone C application, as well as hosting an operating system like Linux. Providing a number of peripheral connections, like Ethernet or USB, the PS can easily be accessed by the user from another host computer, given the necessary drivers and protocols are implemented. The aforementioned evaluation tool for example uses the Linux application *rftool* in order to receive commands and perform the according action.



## **6. Conclusion and Outlook**



## 7. Conclusion and Outlook

Analysis of events occurring in the range of femtoseconds is desired in many scientific experiments. The high temporal resolution needed for measuring such events imposes a great technological challenge for Data Acquisition Systems (DAQs) and Analog-To-Digital-Converters (ADCs). In order to relax the requirements on the acquisition systems, the so-called optical time-stretch technique is used to stretch the analog input signal in time. In this way, data converters at relatively moderate sample rate can be used. Measuring the signal with commercial DAQs, such as real-time oscilloscope, still poses another challenge. Due to the limited acquisition time windows of such systems, continuous measurements at high sampling rate over long time is not possible. In applications, where measurements of long-term evolution of the ultra-fast events is desired, this is a major limitation. Therefore new concepts of DAQ based on the time-stretch method need to be considered in order to overcome this limitation.

In this thesis, a first demonstrator of such a new DAQ system based on the photonic time-stretch method was developed. The system consists of a high bandwidth front-end sampling card, mounted on a back-end card integrating a new generation of Radio-Frequency System-On-Chip (RFSoC) for readout of the acquired samples. The name given to the system is Terahertz Readout Sampling (THERESA).

The front-end sampling card integrates 16 sampling channels, each containing a Track-And-Hold-Amplifier (THA) with individually programmable delay in sampling time. The design of the board allows it to be used in two different modes: with and without the time-stretch setup. In single-channel mode one detector is connected to one sampling channel, therefore allowing sampling of up to 16 detectors at the same time with one sampling point per channel. In the second mode, several channels are connected to one detector via power-splitter, therefore allowing multiple sampling points for one detector/per channel by setting the delay times accordingly.

High-speed ADCs, integrated in the RFSoC, with 14-bit resolution and a sample rate of up to 2.5 GS/s allow continuous sampling of the signal with high time resolution. Using the time-interleaving technique for all sixteen ADCs results in an overall maximal achievable sample rate of 40 GS/s possible. When using in combination with the time-stretch technique and considering typical stretch-factors, these 11 ps are translated into a range of femtoseconds in the original signal.

The sampling card was furthermore designed to fully exploit all the features of the RFSoC, which integrates a processing unit together with a Field Programmable Gate Array (FPGA). An evaluation tool framework is provided for the selected read-out card, allowing for on-board data generation and capture. This tool was also evaluated; allowing for quick set-up and measurement of key data converter characteristics (Signal-to-Noise-and-Distortion Ratio (SINAD), Spurious-Free Dynamic Range (SFDR), ...) it provides an invaluable tool in order to get a first impression of the performance of the sampling card.

The on-chip FPGA provides the possibility to flexibly adjust the firmware to user needs. Slow-control implemented in the FPGA takes care of programming the components on the sampling card, such as the delay chips. High-speed interfaces, allowing speeds over 100 GB/s, are a crucial component for the high throughput of the large amount of data generated by the data converters; with the given resolution and max. sample rate this touches the range of TB/s.

The design of the sampling card was approved and the card has been deployed in production. Quick characterization of the card is possible due to the tool provided for the readout-card and can be carried out using the methods described in subsection 2.3.1. THERESA will then be commissioned and taken into operation, improving the research in various scientific fields, especially beam diagnostics at e.g. at Karlsruhe Research Accelerator (KARA). There it can be used for studying Coherent Synchrotron Radiation (CSR), in the far-field and near-field Electro-Optic (EO) setup, for study of fast laser dynamics and many other applications. The selected FPGA is suitable for deploying Artificial Intelligence (AI) applications (i.e. reinforcement learning). Therefore the system can also be used for interfacing with the Bunch-By-Bunch feedback at KARA. In the context of the Exploration et contrôle ULTRArapide de la dynamique des paquets d'électrons dans les sources de lumière SYNChrotron (ULTRASYNC) project, funded by Agence Nationale de la Recherche (ANR) and Deutsche Forschungsgemeinschaft (DFG), THERESA can be used in order to study the control of electron bunches in accelerators at KARA and Source optimisée de lumière d'énergie intermédiaire du LURE (SOLEIL), therefore being an important step towards new usable Terahertz (THz) sources.

## Acknowledgments



# Appendix

## A. Characteristic Impedance Of Coplanar Waveguides

### Edge-Coupled Coplanar Waveguide

Characteristic impedance[Wad91, p197-198]:

$$Z_{0,o} = \frac{\eta_0}{\sqrt{\epsilon_{\text{eff},o}}} \left( \frac{1.0}{2.0 \frac{K(k_o)}{K'(k_o)} + \frac{K(\beta_1)}{K'(\beta_1)}} \right) \quad (\text{A.1})$$

$$Z_{0,e} = \frac{\eta_0}{\sqrt{\epsilon_{\text{eff},e}}} \left( \frac{1.0}{2.0 \frac{K(k_e)}{K'(k_e)} + \frac{K(\beta_1 k_1)}{K'(\beta_1 k_1)}} \right) \quad (\text{A.2})$$

$$\epsilon_{\text{eff},o} = \frac{2.0 \epsilon_r \frac{K(k_o)}{K'(k_o)} + \frac{K(\beta_1)}{K'(\beta_1)}}{2.0 \frac{K(k_o)}{K'(k_o)} + \frac{K(\beta_1)}{K'(\beta_1)}} \quad (\text{A.3})$$

$$\epsilon_{\text{eff},e} = \frac{2.0 \epsilon_r \frac{K(k_e)}{K'(k_e)} + \frac{K(\beta_1 k_1)}{K'(\beta_1 k_1)}}{2.0 \frac{K(k_e)}{K'(k_e)} + \frac{K(\beta_1 k_1)}{K'(\beta_1 k_1)}} \quad (\text{A.4})$$

with

$$k_o = \Lambda \frac{-\sqrt{\Lambda^2 - t_c^2} + \sqrt{\Lambda^2 - t_B^2}}{t_B \sqrt{\Lambda^2 - t_c^2} + t_c \sqrt{\Lambda^2 - t_B^2}} \quad (\text{A.5})$$

$$k_e = \Lambda' \frac{-\sqrt{\Lambda'^2 - t_c'^2} + \sqrt{\Lambda'^2 - t_B'^2}}{t_B' \sqrt{\Lambda'^2 - t_c'^2} + t_c' \sqrt{\Lambda'^2 - t_B'^2}} \quad (\text{A.6})$$

$$\Lambda = \frac{\sinh^2 \left( \frac{\pi(s/2.0+w+d)}{2.0h} \right)}{2} \quad (\text{A.7})$$

$$t_c = \sinh^2 \left( \frac{\pi(s/2.0+w)}{2.0h} \right) - \Lambda \quad (\text{A.8})$$

$$t_B = \sinh^2 \left( \frac{\pi s}{4.0h} \right) - \Lambda \quad (\text{A.9})$$

$$\Lambda' = \frac{\cosh^2 \left( \frac{\pi(s/2.0+w+d)}{2.0h} \right)}{2} \quad (\text{A.10})$$

$$t'_c = \sinh^2 \left( \frac{\pi(s/2.0 + w)}{2.0h} \right) - \Lambda' + 1.0 \quad (\text{A.11})$$

$$t'_B = \sinh^2 \left( \frac{\pi s}{4.0h} \right) - \Lambda + 1.0 \quad (\text{A.12})$$

The parameters have to be chosen according to

$$s + 2.0w + 2.0d \leq h \quad (\text{A.13})$$

to guarantee coplanar propagation. [Wad91]

### Surface Coplanar Waveguide with Ground

The characteristic impedance of a coplanar waveguide is given as (see [Wad91])

$$Z_0 = \frac{60.0\pi}{\sqrt{\epsilon_{\text{eff}}}} \frac{1.0}{K(k) + K(k_1')} \cdot \quad (\text{A.14})$$

It comprises of the following components, with  $K(k)$  being an elliptical integral of the first kind (see also [BSMM99, p. 430]):

$$k = a/b \quad (\text{A.15})$$

$$k' = \sqrt{1.0 - k^2} \quad (\text{A.16})$$

$$k_1 = \frac{\tanh(\frac{\pi a}{4.0h})}{\tanh(\frac{\pi b}{4.0h})} \quad (\text{A.17})$$

$$k_1' = \sqrt{1.0 - k_1^2} \quad (\text{A.18})$$

$$\epsilon_{\text{eff}} = \frac{1.0 + \epsilon_r \frac{K(k')}{K(k)} \frac{K(k_1)}{K(k_1')}}{1.0 + \frac{K(k')}{K(k)} \frac{K(k_1)}{K(k_1')}} \quad (\text{A.19})$$

## B. Code

```
'timescale 1ns / 1ps

module SDI_Delay_NB6L295(
    input [10:0]           In_1, In_2, In_3, In_4, In_5, In_6, In_7, In_8, // 
                           data for respective delay chips
    input                  Clk,
    input                  Reset,
    output reg [7:0]        EN, // enable signal for delay chips, active LOW
    output reg              SDIN, // configuration data
    output reg              SLOAD, // signals delay chip to load previously sent
                           data
    output                 SCLK // clock for serial communication with delay chips
);

reg                      start_clk;
assign SCLK = start_clk & (!Clk);

reg [21:0]             In_1_reg, In_2_reg, In_3_reg, In_4_reg, In_5_reg,
                       In_6_reg, In_7_reg, In_8_reg; // registers to intermediately store the
                           inputs
```

```

reg [7:0] select; // register used by Priority Encoder to detect
// which input changed

parameter DATA_SHIFT_WIDTH = 11; // number of bits to be shifted
// during transmission, 1 Data word = 11 bits
reg [4:0] clk_cnt;

reg [DATA_SHIFT_WIDTH-1:0] Data_reg; // register for storing data for
state machine

reg data_start; // signal for state machine to start sending
reg is_finished dataSent; // flags if transmission for one delay chip

parameter dly = 1; // delay control

reg delayReady;

always @ (posedge Clk)
begin
  if (select == 'd0) delayReady <= #dly 'b1;
  else delayReady <= #dly 'b0;
end

// Priority Encoder
// Check if any input has changed, select which data should be sent
// accordingly
always @ (posedge Clk)
begin
  if (Reset)
  begin
    In_1_reg <= #dly 'd0;
    In_2_reg <= #dly 'd0;
    In_3_reg <= #dly 'd0;
    In_4_reg <= #dly 'd0;
    In_5_reg <= #dly 'd0;
    In_6_reg <= #dly 'd0;
    In_7_reg <= #dly 'd0;
    In_8_reg <= #dly 'd0;
    Data_reg <= #dly 'd0;

    select <= #dly 'd0;

    start <= #dly 1'b0;;
  end
  else
  begin
    if (~start & delayReady)
    begin
      select[7] <= #dly In_1_reg != In_1;
      select[6] <= #dly In_2_reg != In_2;
      select[5] <= #dly In_3_reg != In_3;
      select[4] <= #dly In_4_reg != In_4;
      select[3] <= #dly In_5_reg != In_5;
      select[2] <= #dly In_6_reg != In_6;
      select[1] <= #dly In_7_reg != In_7;
      select[0] <= #dly In_8_reg != In_8;
    end
    else
    begin

```

```

        if (clk_cnt == 4'd12 & ~start_clk) // = end of
          sequence
            start                      <= #dly 1'b0;
        else
          start                      <= #dly 1'b1;
      end

      casex (select)
        8'b1???????: begin
          if (~dataSent)
            begin
              In_1_reg           <= #dly In_1;
              Data_reg            <= #dly In_1;
              EN                  <= #dly
              8'b01111111;
              start                <= #dly 1'b1;
            end
          else
            begin
              start                <= #dly 1'b0;
              select [7]           <= #dly 1'b0;
            end
          end
        8'b01???????: begin
          if (~dataSent)
            begin
              In_2_reg           <= #dly In_2;
              Data_reg            <= #dly In_2;
              EN                  <= #dly
              8'b10111111;
              start                <= #dly 1'b1;
            end
          else
            begin
              select [6]           <= #dly 1'b0;
              start                <= #dly 1'b0;
            end
          end
        8'b001?????: begin
          if (~dataSent)
            begin
              In_3_reg           <= #dly In_3;
              Data_reg            <= #dly In_3;
              EN                  <= #dly
              8'b11011111;
              start                <= #dly 1'b1;
            end
          else
            begin
              select [5]           <= #dly 1'b0;
              start                <= #dly 1'b0;
            end
          end
        8'b0001?????: begin
          if (~dataSent)
            begin
              In_4_reg           <= #dly In_4;
              Data_reg            <= #dly In_4;
              EN                  <= #dly
              8'b11101111;
            end
          end
        endcase
      end
    end
  end
end

```

```

                start          <= #dly 1'b1;
        end

    else
        begin
            select [4]      <= #dly 1'b0;
            start           <= #dly 1'b0;
        end
    end
8'b00001???: begin
    if (~dataSent)
        begin
            In_5_reg       <= #dly In_5;
            Data_reg        <= #dly In_5;
            EN              <= #dly
            8'b11110111;   start           <= #dly 1'b1;
        end
    end
else
    begin
        select [3]      <= #dly 1'b0;
        start           <= #dly 1'b0;
    end
end
8'b000001??: begin
    if (~dataSent)
        begin
            In_6_reg       <= #dly In_6;
            Data_reg        <= #dly In_6;
            EN              <= #dly
            8'b11111011;   start           <= #dly 1'b1;
        end
    end
else
    begin
        select [2]      <= #dly 1'b0;
        start           <= #dly 1'b0;
    end
end
8'b0000001?: begin
    if (~dataSent)
        begin
            In_7_reg       <= #dly In_7;
            Data_reg        <= #dly In_7;
            EN              <= #dly
            8'b11111101;   start           <= #dly 1'b1;
        end
    end
else
    begin
        select [1]      <= #dly 1'b0;
        start           <= #dly 1'b0;
    end
end
8'b00000001: begin
    if (~dataSent)
        begin
            In_8_reg       <= #dly In_8;
        end
    end

```

```

Data_reg <= #dly In_8;
EN <= #dly
8'b11111110;
start <= #dly 1'b1;
end
else
begin
    select [0] <= #dly 1'b0;
    start <= #dly 1'b0;
end
end
default:
begin
    EN <= #dly
    8'b11111111;
    start <= #dly 1'b0;
end
endcase
end
end

// State Machine for Sending Configuration Data to Delay Chip NB6L295
/*
State Description
-----
RESET Resetting all parameters and registers ->
if (reset): stay; else: to IDLE
IDLE Waiting for start signal from priority
encoder -> if (start): to LOAD_P0; else: stay
LOAD_P0 Load first half of Delay_X - which
corresponds to data for Delay PD0 on delay chip - into
temporary register -> to LOAD_P1
LOAD_P1 Load second half of Delay_X - which
corresponds to data for Delay PD1 on delay chip - into
temporary register -> to SHIFT
SHIFT Shift bits for sending serial bitstream to
SDIN, assert SLOAD -> to END
END End transmission, deassert SLOAD, inform
priority encoder about end of transmission -> to IDLE
*/
parameter RESET = 3'd0;
parameter IDLE = 3'd1;
parameter LOAD = 3'd2;
parameter SHIFT = 3'd3;
parameter END = 3'd4;
reg [2:0] STATE;
reg [DATA_SHIFT_WIDTH-1:0] tmp;

always @ (posedge Clk)
begin
    if (Reset)
        begin
            STATE <= #dly RESET;
            tmp <= #dly 'd0;
            dataSent <= #dly 1'b0;
            start_clk <= #dly 1'b0;
            SLOAD <= #dly 1'b0;
            clk_cnt <= #dly 1'b0;
        end
    else
        begin
            case (STATE)

```

```

RESET:
begin
  if (Reset)
    STATE    <= #dly RESET;
  else
    STATE    <= #dly IDLE;
end // RESET

IDLE:
begin
  SDIN      <= #dly 1'b0;
  clk_cnt   <= #dly 5'd0;
  dataSent  <= #dly 1'b0;
  SLOAD     <= #dly 1'b0;

  if (start & ~dataSent)
    STATE    <= #dly LOAD;
  else
    STATE    <= #dly IDLE;
end // IDLE

LOAD:
begin
  tmp       <= #dly Data_reg;
  STATE    <= #dly SHIFT;
end // LOAD_W1

SHIFT:
begin
  if (clk_cnt < 4'd12) // number of bits to be
  shifted //
  begin
    start_clk      <= #dly 1'b1;
    clk_cnt        <= #dly clk_cnt +1;
    tmp            <= #dly
                  {tmp[DATA_SHIFT_WIDTH-2:0], 1'b0};
    SDIN          <= #dly
                  tmp[DATA_SHIFT_WIDTH-1];
  end
  else
  begin
    SLOAD         <= #dly 1'b1;
    clk_cnt       <= #dly
                  clk_cnt;
    start_clk     <= #dly 1'b0;
    STATE         <= #dly END;
    SDIN          <= #dly 1'b0;
  end
end // SHIFT

END:
begin
  SLOAD         <= #dly 1'b0;
  start_clk     <= #dly 1'b0;
  dataSent      <= #dly 1'b1;
  clk_cnt       <= #dly clk_cnt;
  SDIN          <= #dly 1'b0;
  STATE         <= #dly IDLE;
end // END
default:
  STATE    <= #dly RESET;
endcase
end
endmodule

```



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