DEPARTMENT OF ELECTRICAL ENGINEERING
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Institute for Data Processing and Electronics (IPE)

A Terabit sampling system with a photonics time-stretch ADC

Master Thesis
of

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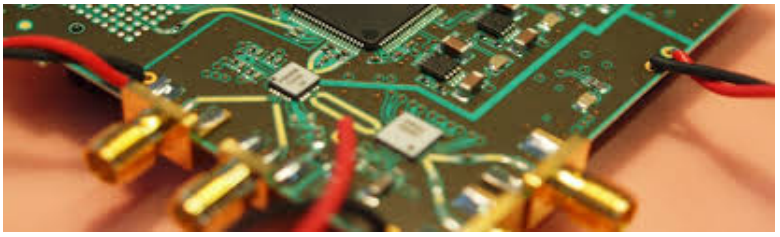

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Abstract

Zusammenfassung

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List of abbreviations

KIT	Karlsruhe Institute of Technology
IPE	Institut für Prozessdatenverarbeitung und Elektronik
KARA	Karlsruhe Research Accelerator
KAPTURE	Karlsruhe Pulse Taking Ultra-fast Readout Electronics
ADC	Analog-To-Digital-Converter
TAH	Track-And-Hold
PLL	Phase-Locked-Loop
DLL	Delay-Locked-Loop
FMC	FPGA Mezzanine Card

1. Introduction

2. Theoretical Background

2.1. Synchrotron

Describe general ideas

2.1.1. Terahertz Radiation

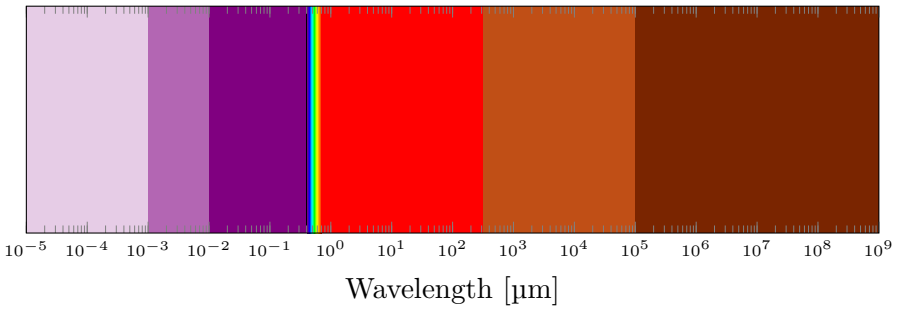

Figure 2.1.: Electro-Magnetic spectrum

Detection/YBCO-Detector?

2.1.2. KARA

- Located at the Karlsruhe Institute of Technology (KIT)
- Up to 184 electron packages (bunches) can be filled with a distance between two adjacent bunches of 2 ns
- Operated by the Institute of Beam Physics and Technology (IBPT)

2.2. Analog-to-Digital-Converter

2.2.1. Theory

Sampling, Quantization, ...

2.2.2. Time-Interleaving

Spectral properties,...

2.2.3. Time-Stretch

2.3. FPGA

2.3.1. Basics

2.3.2. Xilinx Zynq UltraScale+ RFSoC

2.4. State of the art: KAPTURE-2

KAPTURE (**Ka**rlsruhe **P**ulse **T**aking **U**ltra-fast **R**eadout **E**lectronics) is a system – integrated in KARA – designed to continuously sample ultra-short pulses generated by terahertz detectors. The newer version, KAPTURE-2, was designed for more accurate sampling for pulse repetition rates up to 2 GHz. The acquired data is processed by a FPGA and GPU architecture [CAB+17]. The general structure of the board is shown in Figure 2.2.

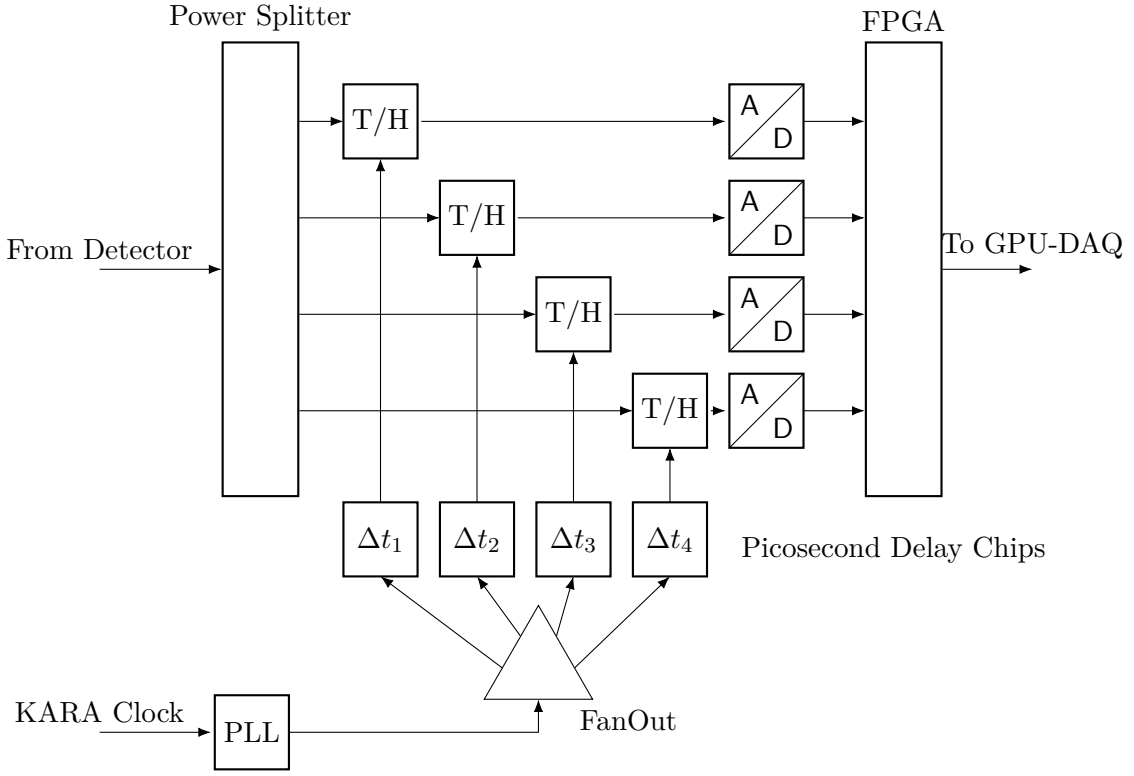

Figure 2.2.: General schema of KAPTURE (cf. [CAB+17, p.2])

The pulse from the THz detector is fed into a power splitter, which splits the signal into four identical pulses and distributes them to four channels, consisting of a respective Track-And-Hold (TAH) unit and a 12-bit ADC@500 MS/s. The sampling time of each unit can be adjusted individually with a Picosecond Delay Chip with a resolution of 3 ps (maximal delay range: 100 ps). The clock signal is provided by KARA, which cleared from jitter by a Phase-Locked-Loop (PLL). The clean clock signal is distributed to the delay chips with a fan-out. [CAB+17]

This results in the sampling of the signal as shown in Figure 2.3.

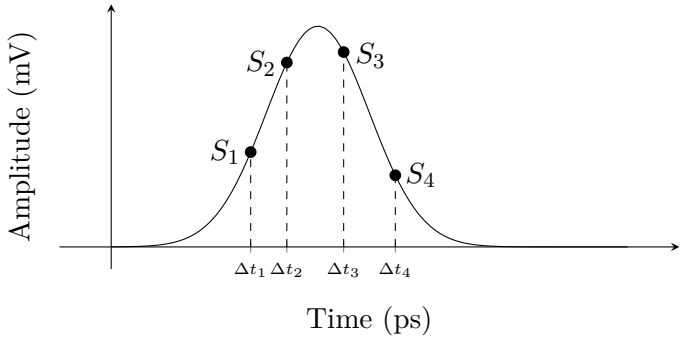

Figure 2.3.: Signal with sample points

2.5. New Boards

On the new boards, up to sixteen ADC, which are integrated in the Xilinx evaluation board, should be used. The two boards cover two modes, one for ultrafast pulse acquistion ("Normalmode") and one for use with the time-stretched signal.

2.5.1. "Normal mode"

PLL provides signal to fan-out and FPGA.

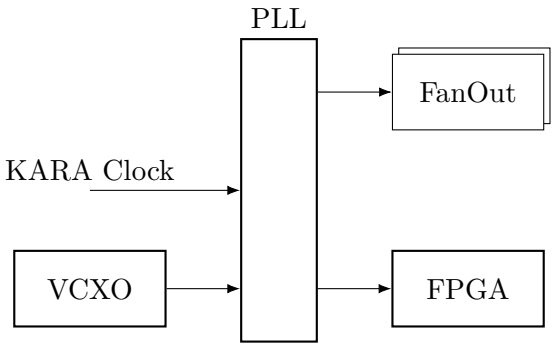

Figure 2.4.: PLL in "KARA-mode"

2.5.2. Mode with time stretch

2.5.3. Requirements

Delay chip

The necessary step size for the delay chips, when using 16 ADC@2 GS/s in time-interleaving mode, is: $\frac{2\,\mathrm{GS/s}}{16} = 31\,\mathrm{ps}$

3. Work

3.1. Front-End Electronics

In a first step, a new front-end board needs to be developed for the new system. This will be plugged into the Xilinx Evaluation Board. As the new system should operate for "normal" and in time-stretch mode, two boards need to be developed to meet the respective requirements.

3.1.1. Power Supply for Track-And-Hold

For the boards to develop a new Power-Supply-Unit for the TAH units – the ADP1741 (Analog Devices) – should be used. It is therefore necessary to think about the quantity of power supply units needed. As a rule of thumb, the power supply should provide twice the maximum power needed by the components which it drives. The power consumption/maximum current for the respective components on the KAPTURE-board is listed in Table 3.1.

Table 3.1.: Power consumption of KAPTURE components (for "KARA-mode")

Component	V_{cc} (V)	I_{max} (A)	P_{max} (W)	$\#_{parts}$	I_{tot}[1] (A)
HMC5649 (T/H-Amplifier)	2	0.221	0.442	16	3.536
	−5	−0.242	1.21		3.872
HMC856 (Delay)	−3.3	0.185	−0.611	16	2.96
HMC987LP5E (Fan-Out)	3.3	0.234[2]	0.772	2	0.468
LMC0480 (PLL)	3.3	0.590[3]	1.947	1	0.590
VCXO	3.3	0.03	0.198	1	0.03

[1] for 16 ADCs
[2] All Outputs and RF-Buffer
[3] All CLKs

The maximal current which the ADP1741 can provide @2 V is 2 A. This means, with the TAH-unit requiring a maximal current of 0.221 A, one ADP1741 can handle four TAH-units ($I_{max\_ADP1741} = 2\,\text{A} > 2 * I_{tot}, I_{tot} = 4 \times 0.221\,\text{A} = 0.884\,\text{A}$).

3.1.2. PLL

For the two modes different PLLs are needed. For "KARA-mode" the already existing PLL-solution can be used, as the clocking is distributed with the help of two fanouts. In "time-stretch mode" however the PLL is used as a Delay-Locked-Loop (DLL) and should drive all 16 delay/TAH-unit respectively, so that a new, fitting component is necessary.

3.1.2.1. "Normal mode"

LMK0480

The LMK0480 feeds into the two fan-out modules and to the FPGA. As the ADCs are now integrated on the FPGA board, it is not necessary to drive them with an external PLL anymore, like in KAPTURE-2.

- Number of CLKOuts: 11
- CLKOuts are grouped together as listed in Table 3.2:

Table 3.2.: CLKOut Groups of PLL LMK0480

Clock Group	Clock Outputs
0	CLKout0, CLKout1
1	CLKout2, CLKout3
2	CLKout4, CLKout5
3	CLKout6, CLKout7
4	CLKout8, CLKout9
5	CLKout10, CLKout11

- Two outputs of the same group provide a clock signal at the same frequency, phase, etc. As the two fan-out modules should be synchronous, they should be connected to the CLKouts of the same group, e.g. CLKout 0 and 1 of Clock Group 0.
- Adjustable delay at CLKouts:
  - **Fine, analog delay**: Step size 25 ps, range from 0 to 475 ps
    → Enabling adds a nominal 500 ps of delay in addition to the programmed value.
  - **Coarse, digital delay**: Delay of 4.5 to 12 clock distribution path cycles (normal mode) or 12.5 to 522 VCO cycles (extended mode) → step as small as half of period of clock distribution path cycle (using `CLKoutX_Y_HS` bit, when output divide value > 1)
- Fixed digital delay is determined by the frequency of distribution path. With an external VCO the resolution (one delay step) is determined by:

$$DD_{Res} = \frac{1}{2 \times VCO\_Frequency} \tag{3.1}$$

  For a desired delay `CLKX_Y_DDLY` and `CLKX_Y_HS` have to be set accordingly, with `X` being the even and `Y` being the odd number of the `CLKout` in the group.

3.1.2.2. For time stretch

NB6L295

Dual Channel Programmable Delay Chip.

- Two individual variable delay channels
- Dual Delay: minimal delay 3.2 ns
- 11 ps in 511 steps
- 100 ps Typical Rise and Fall Times

3.1.3. Delay-Chip (for Time-Stretch-Mode)

3.2. FPGA

4. Conclusions and Outlook

Appendix

A. First Appendix Section

LVCMOS Low voltage complementary metal oxide semiconductor

LVDS Low-voltage differential signaling

LVPECL Low-voltage positive emitter-coupled logic

Bibliography

[CAB+17] Caselle, M., L.E. Ardila Perez, M. Balzer, A. Kopmann, L. Rota, M. Weber, M. Brosi, J. Steinmann, E. Bründermann und A. S. Müller: *KAPTURE-2. A picosecond sampling system for individual THz pulses with high repetition rate.* Journal of Instrumentation, 12, 2017.