DEPARTMENT OF ELECTRICAL ENGINEERING
AND INFORMATION TECHNOLOGY
Institute for Data Processing and Electronics (IPE)

A Terabit sampling system with a photonics time-stretch ADC

Master Thesis
of

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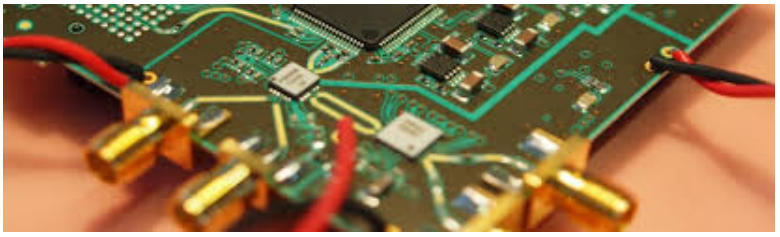
at the Institute for Data Processing and Electronics (IPE)



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Karlsruhe, den 14.05.2021, _____

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Abstract

Zusammenfassung

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List of abbreviations

KIT	Karlsruhe Institute of Technology
IPE	Institut für Prozessdatenverarbeitung und Elektronik
KARA	Karlsruhe Research Accelerator
KAPTURE	Karlsruhe Pulse Taking Ultra-fast Readout Electronics
ADC	Analog-To-Digital-Converter
TAH	Track-And-Hold
PLL	Phase-Locked-Loop
DLL	Delay-Locked-Loop
FMC	FPGA Mezzanine Card

1. Introduction

2. Theoretical Fundamentals

2.1. Synchrotron

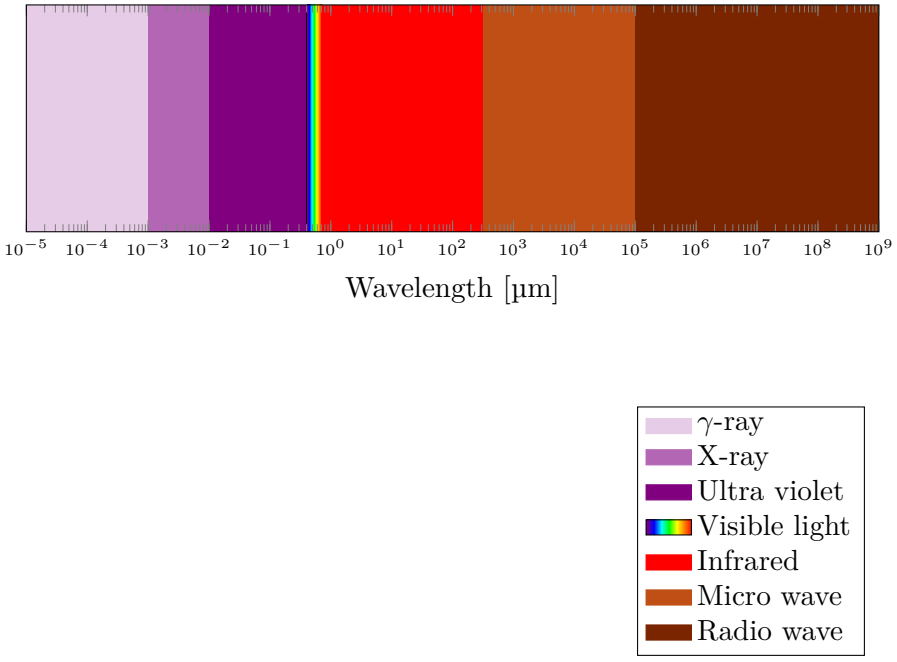

Figure 2.1.: Electro-Magnetic spectrum

2.1.1. KARA

- Located at the Karlsruhe Institute of Technology (KIT)
- Up to 184 electron packages (bunches) can be filled with a distance between two adjacent bunches of 2 ns
- Operated by the Institute of Beam Physics and Technology (IBPT)

2.1.1.1. KAPTURE-2

KAPTURE (**Ka**rlsruhe **P**ulse **T**aking **U**ltra-fast **R**eadout **E**lectronics) is a system – integrated in KARA – designed to continuously sample ultra-short pulses generated by terahertz detectors. The newer version, KAPTURE-2, was designed for more accurate sampling for pulse repetition rates up to 2 GHz. The acquired data is processed by a FPGA and GPU architecture [CAB+17]. The general structure of the board is shown in Figure 2.2.

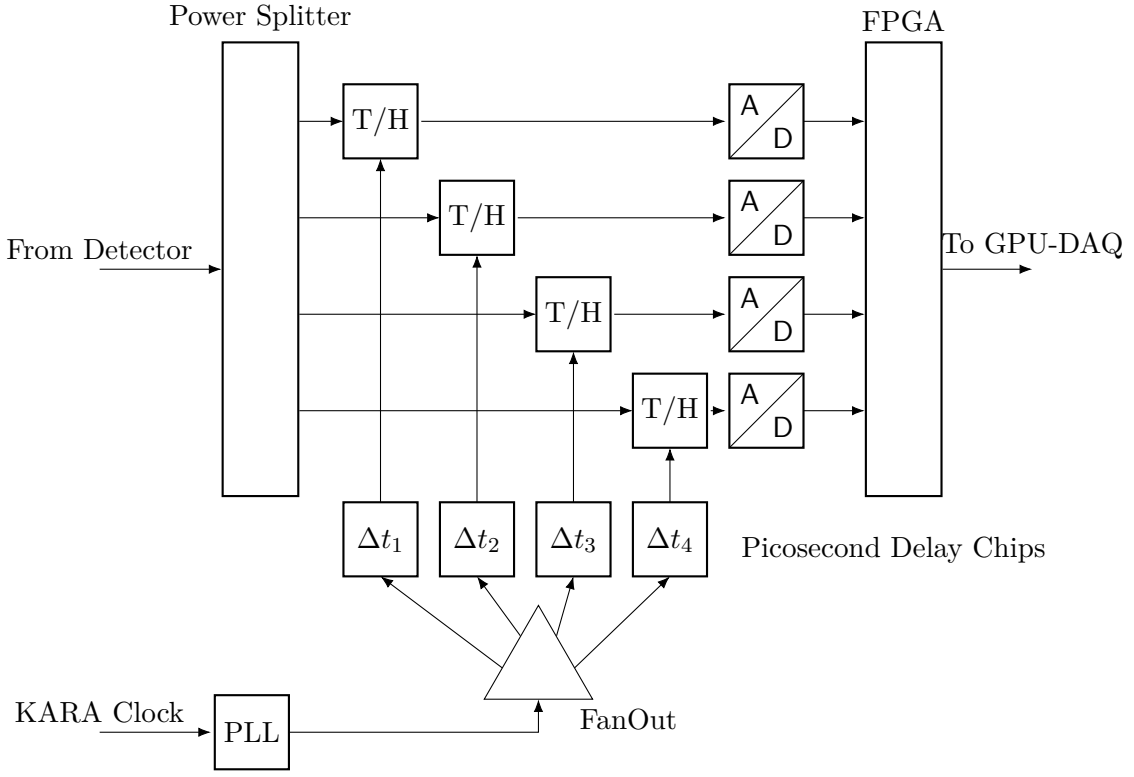

Figure 2.2.: General schema of KAPTURE (cf. [CAB+17, p.2])

The pulse from the THz detector is fed into a power splitter, which splits the signal into four identical pulses and distributes them to four channels, consisting of a respective Track-And-Hold (TAH) unit and a 12-bit ADC@500 MS/s. The sampling time of each unit can be adjusted individually with a Picosecond Delay Chip with a resolution of 3 ps (maximal delay range: 100 ps). The clock signal is provided by KARA, which cleared from jitter by a Phase-Locked-Loop (PLL). The clean clock signal is distributed to the delay chips with a fan-out. [CAB+17]

This results in the sampling of the signal as shown in Figure 2.3.

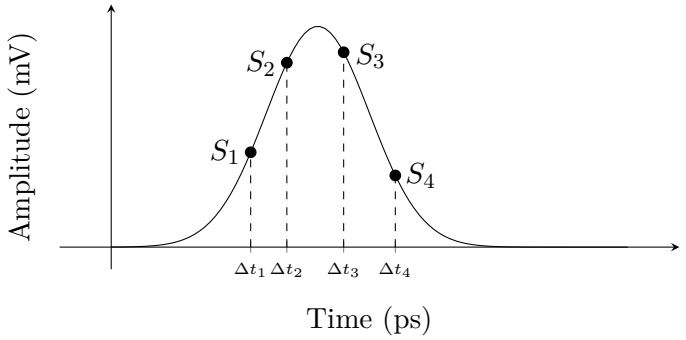

Figure 2.3.: Signal with sample points

2.2. Optical Time Stretching Technique

2.2.1. Applications

2.3. Analog-To-Digital-Converter

2.4. New Readout System

2.4.1. Xilinx Zynq UltraScale+ RFSoC

2.4.2. Requirements

Delay chip

The necessary step size for the delay chips, when using 16 ADC@2 GS/s in time-interleaving mode, is: $\frac{2\,\mathrm{GS/s}}{16} = 31\,\mathrm{ps}$

3. Development of the system

3.1. Architecture

In a first step, a new front-end board needs to be developed for the new system. This will be plugged onto the Xilinx ZCU216 Evaluation Board.

Power Supply for Track-And-Hold amplifiers

For the Track-And-Hold amplifiers a new power supply unit – the ADP1741 (Analog Devices) – should be used. It is necessary to think about the amount of power supply chips needed. As a rule of thumb, the power supply should provide twice the maximum power needed by the components it drives. The power consumption/maximum current for the respective components on the THERESA board is listed in Table 3.1.

Table 3.1.: Power consumption of components on the board

Component	V_{cc} (V)	I_{max} (A)	P_{max} (W)	$\#_{parts}$	I_{tot}[1] (A)
HMC5649 (T/H-Amplifier)	2	0.221	0.442	16	3.536
	−5	−0.242	1.21		3.872
HMC856 (Delay)	−3.3	0.185	−0.611	16	2.96
HMC987LP5E (Fan-Out)	3.3	0.234[2]	0.772	2	0.468
LMC0480 (PLL)	3.3	0.590[3]	1.947	1	0.590
VCXO	3.3	0.03	0.198	1	0.03

[1] for 16 ADCs
[2] All Outputs and RF-Buffer
[3] All CLKs

The maximal current which the ADP1741 can provide @2 V is 2 A. This means, with one Track-And-Hold amplifier requiring a maximal current of 0.221 A, one ADP1741 can handle four units according to the rule mentioned beforehand ($I_{max\_ADP1741} = 2\,\text{A} > 2 * I_{tot}, I_{tot} = 4 \times 0.221\,\text{A} = 0.884\,\text{A}$).

NB6L295

Dual Channel Programmable Delay Chip.

- Two individual variable delay channels
- Dual Delay: minimal delay 3.2 ns
- Total Delay Range: 3.2 ns to 8.8 ns per Delay Channel
- 11 ps Increments in 511 steps
- 100 ps Typical Rise and Fall Times

3.2. PCB-Layout

Surface Coplanar Waveguide with Ground

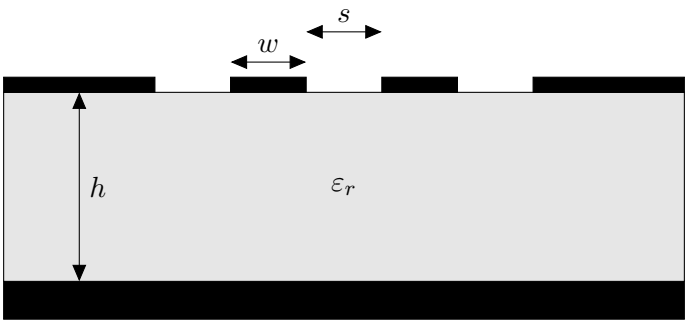

Figure 3.1.: Edge-Coupled Coplanar Waveguide

Surface Coplanar Waveguide with Ground

The characteristic impedance of a coplanar waveguide is given as follows [Wad91]:

$$Z_0 = \frac{60.0\pi}{\sqrt{\epsilon_{eff}}} \frac{1.0}{\frac{K(k)}{K(k')} + \frac{K(k_1)}{K(k_1')}} \tag{3.1}$$

It comprises of the following components, with K(k) being an elliptical integral of the first kind (see also [BSMM99, p. 430]):

$$k = a/b \tag{3.2}$$

$$k' = \sqrt{1.0 - k^2} \tag{3.3}$$

$$k_1' = \sqrt{1.0 - k_1^2} \tag{3.4}$$

$$k_1 = \frac{tanh(\frac{\pi a}{4.0h})}{tanh(\frac{\pi b}{4.0h})} \tag{3.5}$$

$$\epsilon_{eff} = \frac{1.0 + \epsilon_r \frac{K(k')}{K(k)} \frac{K(k_1)}{K(k_1')}}{1.0 + \frac{K(k')}{K(k)} \frac{K(k_1)}{K(k_1')}} \tag{3.6}$$

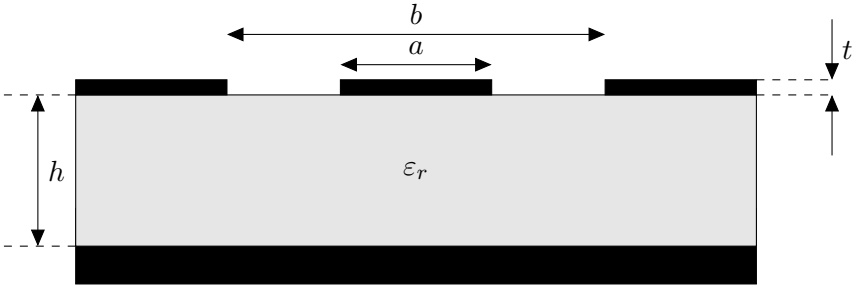

Figure 3.2.: Coplanar Waveguide with Ground

4. Conclusions and Outlook

Appendix

A. First Appendix Section

LVCMOS Low voltage complementary metal oxide semiconductor

LVDS Low-voltage differential signaling

LVPECL Low-voltage positive emitter-coupled logic

Bibliography

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