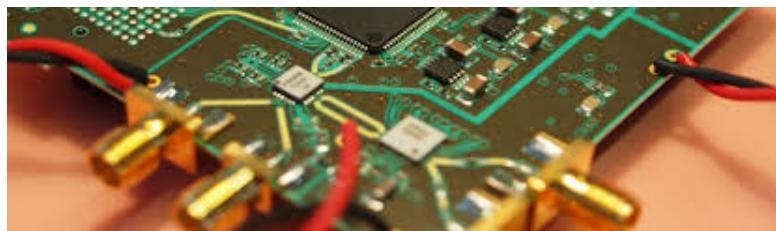


A Terabit sampling system with a photonics time-stretch ADC

Master Thesis
of

Olena Manzhura

at the Institute for Data Processing and Electronics (IPE)



Reviewer: Prof. Dr. Anke-Susanne Müller (LAS)
Second Reviewer: Dr. Michele Caselle (IPE)

15.11.2020 – 13.08.2021

Declaration

I hereby declare that I wrote my master thesis on my own and that I have followed the regulations relating to good scientific practice of the Karlsruhe Institute of Technology (KIT) in its latest form. I did not use any unacknowledged sources or means, and I marked all references I used literally or by content.

Karlsruhe, 13.08.2021, _____
Olena Manzhura

Approved as an exam copy by

Karlsruhe, 13.08.2021, _____
Prof. Dr. Anke-Susanne Müller (LAS)

Abstract

Zusammenfassung

Résumé

Contents

1. Introduction	1
2. Theoretical Fundamentals	3
2.1. Coherent Synchrotron Radiation	3
2.2. Photonic time-stretch analog-to-digital converter	6
2.3. Characteristics of Analog-To-Digital-Converters	7
2.3.1. Sampling Theory	7
2.3.2. AC errors	8
2.3.3. Interleaving	9
2.4. RF/Microwave Design Basics	10
3. Design of the system	11
3.1. General architecture	11
3.1.1. KAPTURE-2	11
3.1.2. THERESA	14
3.1.2.1. Xilinx Zynq UltraScale+ RFSoC ZCU216 Evaluation Kit	14
3.1.3. Requirements	15
3.2. Design of the front-end card	17
3.2.1. Sampling-Channel	17
3.2.2. Clocking	17
3.2.3. Power Supply	17
3.3. PCB-Layout	18
3.3.1. General Techniques/Strategies?	18
3.3.2. Floor Planning	18
3.3.3. Transmission lines	18
3.3.4. Polaris	20
3.4. Firmware	21
3.4.1. Xilinx Designs	21
3.4.2. SPI-firmware for components	21
3.4.3. IPE-AXI IP block	21
3.4.4. GUI	21
4. Characterization	23
4.1. Evaluation of the ZCU216 Board	23
4.1.1. Measurements with Xilinx XM655 add-on card	23
4.2. Measurements with the IPE front-end card	23
5. Conclusions and Outlook	25
Appendix	27
A. QuickStart Guide for Evaluation of ZCU216 Board	27
B. 3D model of front-end card	27

List of Figures

2.1.	Basic scheme of an electron storage ring (redrawn from [Rou14])	3
2.2.	Electromagnetic spectrum	4
2.3.	CSR [Rot18]	4
2.4.	Electrons interact with their own radiation [BBB ⁺ 19]	5
2.5.	Facility [Rot18]	5
2.6.	Electro-Optical Time-Stretch Technique [BBB ⁺ 19]	6
2.7.	Track-And-Hold-Amplifier schematic and principle [Kes05]	8
2.8.	Quantization noise as function of time[Kes05]	8
3.1.	General schema of KAPTURE-2 (cf. [CAB ⁺ 17, p.2])	11
3.2.	12
3.3.	Signal with sample points	12
3.4.	Photo of KAPTURE with highlighted main components. [Bro20, p. 61] . .	13
3.5.	General schema of THERESA. For presentation purposes only four channels are shown.	14
3.6.	ZCU216 evaluation board	15
3.7.	RFSoC block diagram	15
3.8.	Track-And-Hold Timing diagram	16
3.9.	CLK104 Add-on board clocking scheme	17
3.10.	Edge-Coupled Coplanar Waveguide	18
3.11.	Coplanar Waveguide with Ground	19
3.12.	Polaris Solver	20
3.13.	Test Graph	20
4.1.	RF DC Evaluation Tool architecture [Xil20a]	23
4.2.	RF DC Evaluation Tool GUI [Xil20a]	23

List of Tables

2.1. KARA characteristics	5
3.1. Power consumption of components on the board	18

List of abbreviations

KIT	Karlsruhe Institute of Technology
IPE	Institut für Prozessdatenverarbeitung und Elektronik
KARA	Karlsruhe Research Accelerator
KAPTURE	Karlsruhe Pulse Taking Ultra-fast Readout Electronics
ADC	Analog-To-Digital-Converter
TAH	Track-And-Hold
PLL	Phase-Locked-Loop
FMC	FPGA Mezzanine Card
LVCMOS	Low voltage complementary metal oxide semiconductor
LVDS	Low-voltage differential signaling
LVPECL	Low-voltage positive emitter-coupled logic
PCIe	PCI Express
THERESA	Terahertz Readout Sampling
RFSoC	Radio-Frequency System-On-Chip

1. Introduction

Spontaneous formation of small-scale microstructures can have a deleterious effect on electron bunch stability and emission properties, and they are at the same time a tremendous source of coherent radiation in the terahertz domain^{3,4,5,6,7,8,9,10,11,12,13,14,15,16,17}, provided the instability can be mastered. This is the reason why understanding and controlling the interplay between Coherent Synchrotron Radiation (CSR) and the microbunching instability has nowadays become a central open question in the development of synchrotron radiation facilities.

To answer this question, it is essential to develop ultrafast photonic devices for electron bunch shape characterization. The challenges for the photonics community is high, given the need for ultrashort (picosecond or femtosecond) temporal resolution, single-shot operation, at high repetition rates (MHz and more), and given the particularly challenging environment near relativistic electron bunches. Recent advances consequently pushed photonics systems beyond the state of the art. Ultrafast electric-field measurement techniques using femtosecond laser pulses (electro-optic sampling²⁴) have allowed single-shot bunch shape measurements (plural)²⁵, and these techniques have then been extensively investigated and improved this last decade

The ULTRASYNC (Exploration et contrôle ULTRArapide de la dynamique des paquets d'électrons dans les sources de lumière SYNChrotron, ANG-DFG) aims to study and control coherent synchrotron radiation (CSR) and microbunching instability. The goal is to obtain a high power and stable coherent emission (KARA and SOLEIL) by feedback control. At SOLEIL, this was already successfully achieved, still there is a significant limit to the range, where this concept works. One possible way would be to calculate the necessary feedback from a whole THz CSR pulse shape, which would require to record an electro-optical signal (time-stretch). This leads to a possible approach by combining time-stretch and FPGA.

For the moment, the only experimental test has been made using a relatively simple feedback: - a bolometer signal as the feedback loop input - a low-cost FPGA (redpitaya) that sends the feedback on the accelerating voltage There are limitations in the maximal bunch charge in the accelerator. So an open question is whether measuring each THz pulse using EO sampling + time-stretch may help to solve this open problem. In clear: - EO sampling + time-stretch as in Eléonore's thesis -> association with the new FPGA-based system -> finding adequate feedback that is programmed in the FPGA may solve the problem, and allow the control to succeed at the highest currents in SOLEIL. Target would be 15 mA for 1 bunch (and feedback control presently works to a little more than 10 mA).

At 1 micron wavelength, the maximum stretch is limited due to fiber glass properties (at this wavelength). The maximum length achieved are 2-4 ns (SOLEIL and KARA). For this reason, a fast ADC is critical, to get a good ENOB/number of sampling points. A relevant figure of merit (that characterizes the effective number of points) is – we think: FOM=electronic bandwidth x stretch time. There is some bottleneck concerning time-

stretch at this wavelength, and one way to solve the issue is to try pushing the bandwidth of ADCs.

At 1550 nm wavelength, it is possible to stretch the signal up to tens of nanoseconds. Therefore, a relatively cheap ADC would already be sufficient and allow an effective number of samples at around 100. Applications still need to be investigated.

As potential applications for the new system would be applications for accelerators in the 1 micron wavelength (best concerning EO sampling SNR and bandwidth).

2. Theoretical Fundamentals

2.1. Coherent Synchrotron Radiation

Synchrotron radiation (SR) is produced in synchrotron radiation facilities (like electron storage rings) by accelerating relativistic electrons. Emission of SR occurs, when bending/deflecting the electrons in dipole magnets or undulators¹.

Figure 2.1 shows a general scheme of an electron storage ring. Electrons, or rather electron bunches, are generated with an electron gun and are accelerated to almost speed of light by a linear accelerator (LINAC). The bunches are injected into the storage ring, after reaching their nominal energy in a booster. In the ring, the path of the electron bunches is altered by bending magnets, leading them on a circular trajectory. Due to emission of SR at each bending, the electrons lose energy, which has to be compensated. This is done in an accelerating radiofrequency (RF) cavity. Not shown in the scheme are the beamlines, which lead the SR radiation, or rather chosen wavelength regions of it, through an optical system to the respective user experiments.[Rou14] [Rot18]

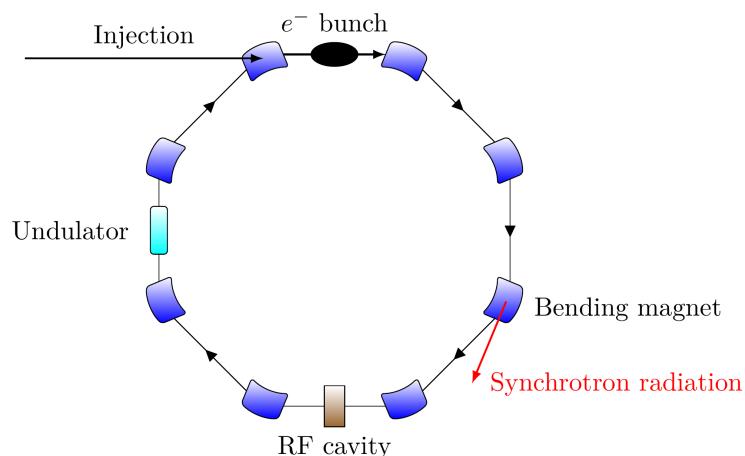


Figure 2.1.: Basic scheme of an electron storage ring (redrawn from [Rou14])

The range of SR reaches from hard X-rays down to the infrared region of the electromagnetic spectrum (see Figure 2.2). In contrast to other sources, it has properties like:

- high intensity
- high collimation
- polarisation
- well-defined timing of pulses

¹Undulators are used to make the electrons oscillate by generating a periodic magnetic field

Due to this properties, synchrotrons are used for microscopy, spectroscopy, and time-resolved experiments in such fields like condensed matter physics, biology, material science and many more.

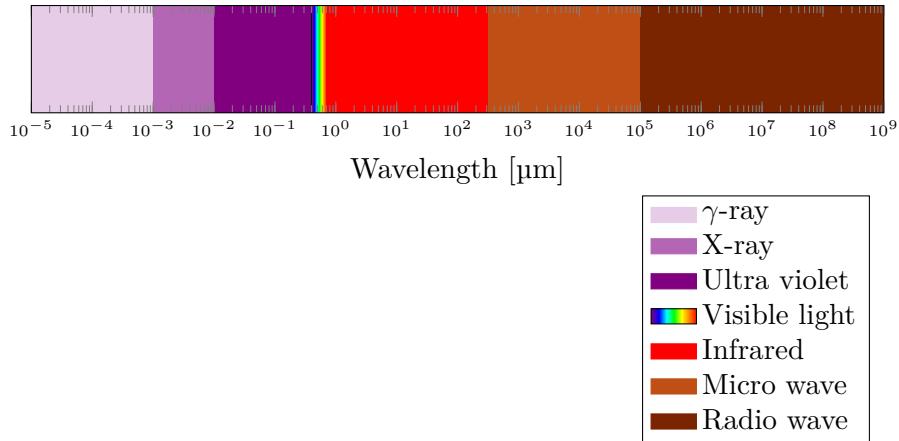


Figure 2.2.: Electromagnetic spectrum

As demands in these fields are ever-increasing, electron accelerators need to provide higher brilliance (or brightness). This is achieved by increased photon flux and reduction of the transverse emittance. For longitudinal coherence, the electron bunches are shortened, which results in emission of coherent synchrotron radiation (CSR) at frequencies up to the THz range. However, this introduces complex dynamics, as the electrons interact with their own radiation. This manifests into the so called microbunching instability: the formation of microstructures (in the sub-millimeter to centimeter range) in the longitudinal density profile of the electron bunches. Being on the one side a limitation to the stable operation of the overall system at high current density/short bunch length mode. On the other side, these instabilities can be potential sources of brilliant THz radiation. A thorough understanding of these dynamics is necessary to control the emission in this spectral domain which enables usage in experiments. [Rot18] [Bro20]

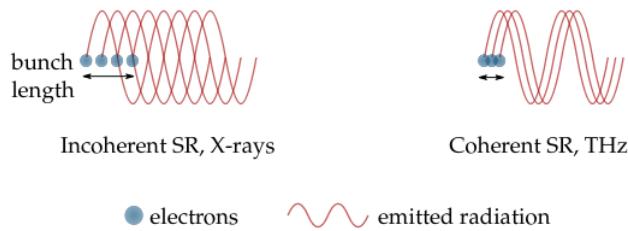


Figure 2.3.: CSR [Rot18]

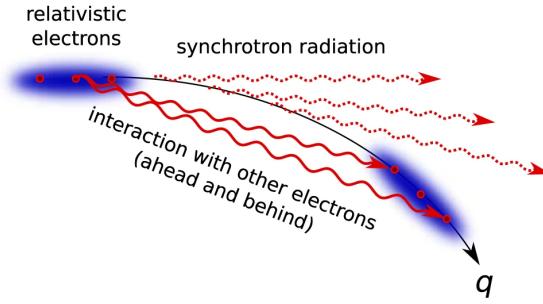


Figure 2.4.: Electrons interact with their own radiation [BBB⁺19]

KARA

- Located at the Karlsruhe Institute of Technology (KIT)
- Up to 184 electron packages (bunches) can be filled with a distance of 2 ns (500 MHz) between two adjacent bunches
- Operated by the Institute of Beam Physics and Technology (IBPT)
- Microtron, Booster Synchrotron, and Storage Ring

Table 2.1.: KARA characteristics

Beam energy	2.5 GeV
Circumference	110 m
RF frequency	499.7 MHz
Harmonic number	184
Number of RF stations	2
Number of cavities per station	2
Accelerating voltage	1.4 MeV

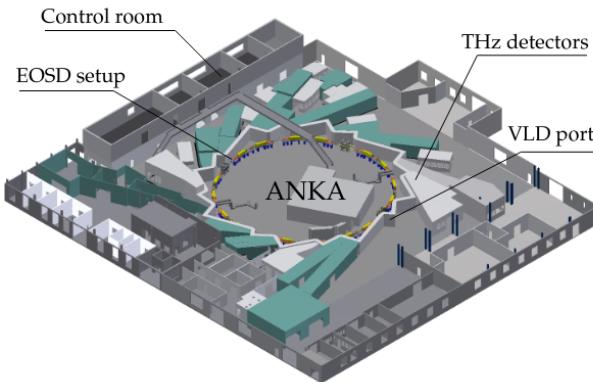


Figure 2.5.: Facility [Rot18]

2.2. Photonic time-stretch analog-to-digital converter

" In recent and future synchrotron radiation facilities, relativistic electron bunches with increasingly high charge density are needed for producing brilliant light at various wavelengths, from X-rays to terahertz. In such conditions, interaction of electron bunches with their own emitted electromagnetic fields leads to instabilities and spontaneous formation of complex spatial structures. Understanding these instabilities is therefore key in most electron accelerators. However, investigations suffer from the lack of non-destructive recording tools for electron bunch shapes. In storage rings, most studies thus focus on the resulting emitted radiation. Here, we present measurements of the electric field in the immediate vicinity of the electron bunch in a storage ring, over many turns. For recording the ultrafast electric field, we designed a photonic time-stretch analog-to-digital converter with terasamples/second acquisition rate. We could thus observe the predicted link between spontaneous pattern formation and giant bursts of coherent synchrotron radiation in a storage ring. "' [BBB⁺19]

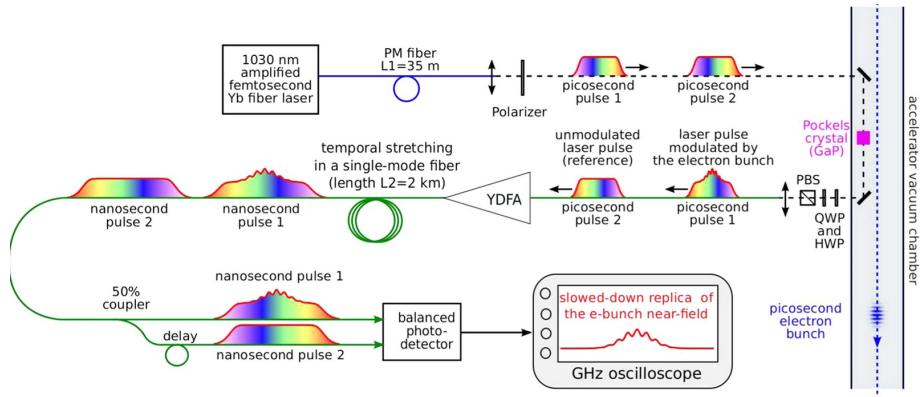


Figure 2.6.: Electro-Optical Time-Stretch Technique [BBB⁺19]

2.3. Characteristics of Analog-To-Digital-Converters

Analog-to-digital converters (ADCs) are used to translate analog quantities into digital signals, which can be processed by information processing, computing, data transmission and control systems. This section covers the different characteristics of an ADC, which are needed to evaluate the performance of the converter in the developed system.

2.3.1. Sampling Theory

Nyquist-Criteria

An ADC samples an analog signal with a frequency f_s . This frequency has to be chosen in such way, that the original signal can be fully reconstructed. The Nyquist criteria states, that in order to accurately represent a bandlimited, continuous signal

$$y(t) \circ= Y(f) \quad \text{with} \quad Y(f) = 0, |f| \geq \frac{B}{2} \quad (2.1)$$

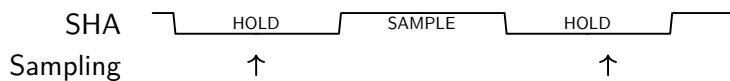
it has to be sampled with a frequency f_s respecting

$$f_s \geq B \quad \text{or} \quad f_s \geq 2f_a \quad (2.2)$$

with f_a being the highest frequency contained in the signal. [Kes05] [Pue15]
In other words, f_a must be inside of the *Nyquist bandwidth*, which is the spectrum from DC to $f_s/2$. Violation of this rule leads to *aliasing*

Sample-And-Hold-Amplifier

ADCs need a certain amount of time to sample the input signal. If the value of the signal changes by more than one Least-Significant-Bit (LSB) during this period, this can result in large errors in the output signal. Therefore, so called Sample-And-Hold-Amplifiers (SHA) are used in front of ADCs to hold the input value for the needed amount of time. The ADC sampling time needs to be timed in such way, that the analog-to-digital conversion falls into the hold period of the SHA and doesn't exceed into the sample period, for example like shown schematically in the diagram below. Thus, the upper frequency limitation is not determined by the ADC itself, but rather by the aperture jitter, bandwidth, distortion, etc. of the SHA. [Kes05]



In addition to the SHA, there is also the Track-And-Hold-Amplifier (THA). Instead of a sample period, the THA has a track period, where the output of the amplifier tracks the input signal (see also Figure 2.7). When switching to hold mode, the signal at this instant is held. This is opposed to the SHA, where the output during sample mode is actually not defined and is set to the value of the input signal, only when switching into hold mode.

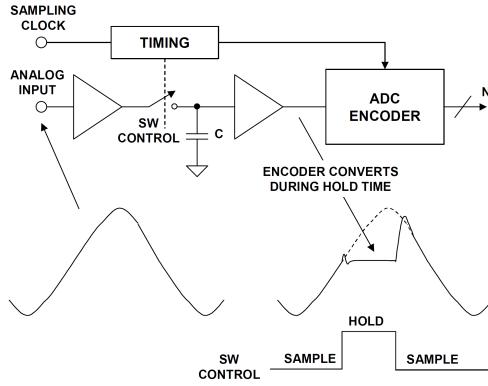


Figure 2.7.: Track-And-Hold-Amplifier schematic and principle [Kes05]

2.3.2. AC errors

In this section, the most important AC errors are briefly described.

Quantization Noise

An ideal N-bit converter has errors occurring during sampling and quantization. For an equidistant quantization the **quantization error** is:

$$|e_q(t)| = |x_q(t) - x(t)| \leq \frac{q}{2} \quad (2.3)$$

with $x_q(t)$ being the quantized/discrete signal, $x(t)$ the input signal and q the width of the quantisation stage. [Pue15] In time domain, can be approximated with a sawtooth signal:

$$e(t) = st, \quad -\frac{q}{2s} < t < \frac{q}{2s} \quad (2.4)$$

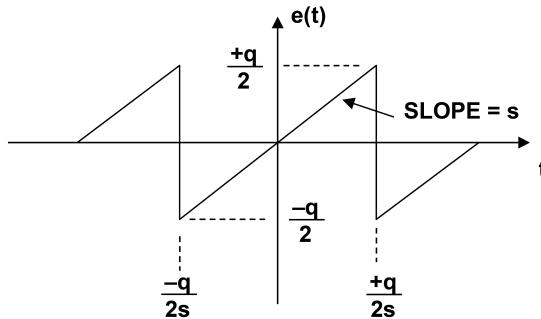


Figure 2.8.: Quantization noise as function of time[Kes05]

The power of the quantization noise can be calculated as the mean-square of $e(t)$:

$$P_{QN} = e_{rms}^2 = \overline{e^2(t)} = \frac{s}{q} \int_{-q/2s}^{+q/2s} (st)^2 dt = \frac{q^2}{12} \quad (2.5)$$

The rms quantization error is then:

$$e_{rms} = \frac{q}{\sqrt{12}} \quad (2.6)$$

Assuming a full-scale input sinewave, the theoretical Signal-To-Noise-Ratio (SNR) of the ideal converter can be calculated as follows:

$$\text{Sine wave: } u(t) = u_s \sin(2\pi ft) = \frac{2^N q}{2} \sin(2\pi ft) \quad (2.7)$$

$$u_{\text{eff}} = \frac{u_s}{\sqrt{2}} = \frac{2^{N-1} q}{2} \sin(2\pi ft) \quad (2.8)$$

$$\text{SNR} = \frac{P_{\text{signal}}}{P_{\text{noise}}} = \frac{u_{\text{eff}}^2}{e_{\text{rms}}^2} \quad (2.9)$$

- Equivalent Input Referred Noise
- Noise-Free Code Resolution

Integral and Differential Nonlinearity Distortion

Dynamic Performance

- Harmonic Distortion, Worst Harmonic, Total Harmonic Distortion (THD), Total Harmonic Distortion + Noise (THD + N)
- Signal-to-Noise-and-Distortion Ratio (SINAD, or S/N + D), Signal-to-Noise ratio (SNR), Effective Number of Bits (ENOB)
- Analog Bandwidth (Full-Power, Small-Signal)
- Spurious Free Dynamic Range (SFDR)
- Two-Tone Intermodulation Distortion, Multi-Tone Intermodulation Distortion
- Noise Power Ratio (NPR)
- Adjacent Leakage Ratio (ACLR)
- Noise Figure
- Setting Time, Overvoltage Recovery Time

[Kes05]

2.3.3. Interleaving

- Net sample rate
- Interleaving Spurs

[MR15]

2.4. RF/Microwave Design Basics

3. Design of the system

This chapter covers the architecture and design of the system.

3.1. General architecture

In this section the general architecture of the THERESA system is described. The idea for the new system is to reuse the concept of the already existing sampling system KAPTURE (**K**arlsruhe **P**ulse **T**aking **U**ltra-fast **R**eadout **E**lectronics), which is using four ADCs, and expanding it to 16. Therefore, also the architecture of the latter is explained briefly.

3.1.1. KAPTURE-2

KAPTURE, which was developed at IPE, is a system designed to continuously sample ultra-short pulses generated by Terahertz detectors. It consists of a daughter card, holding four sampling channels, mounted on a FPGA . The FPGA is connected to a computer via PCIe for further processing of the acquired data. [Bro20] The newer version, KAPTURE-2, was designed for more accurate sampling for pulse repetition rates up to 2 GHz. The acquired data is processed with a FPGA and GPU architecture. [CAB⁺17]

The general structure of the board is shown in Figure 3.1.

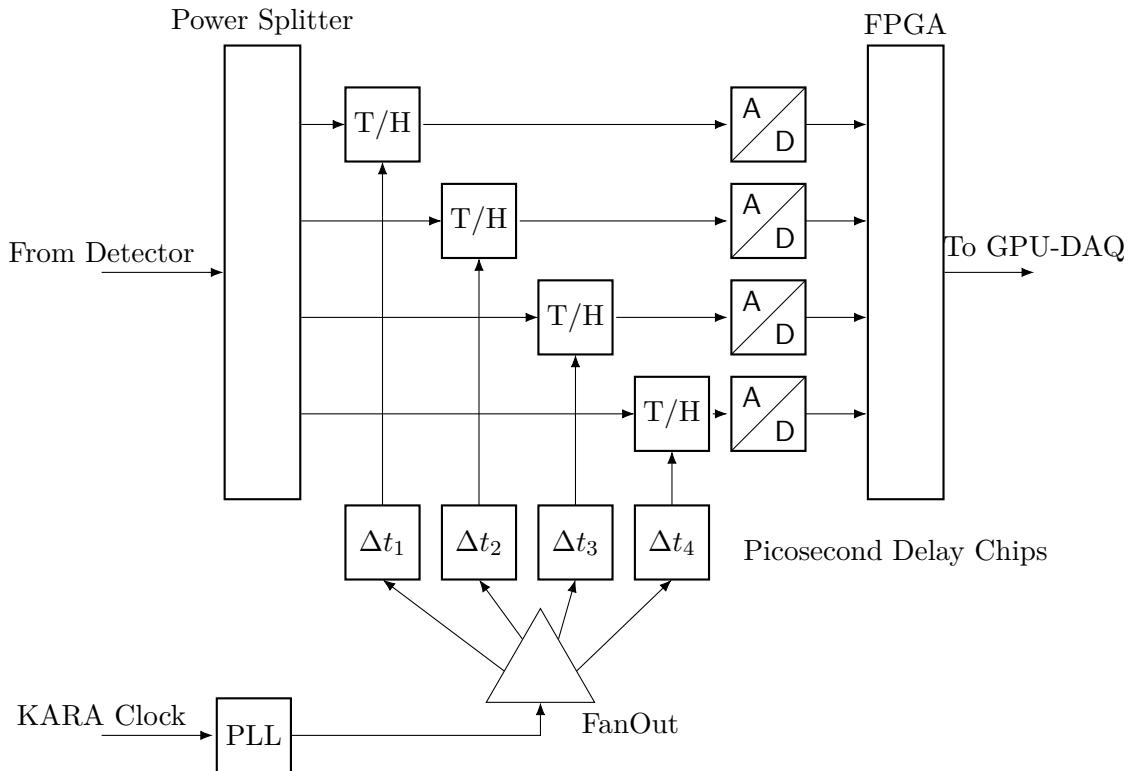
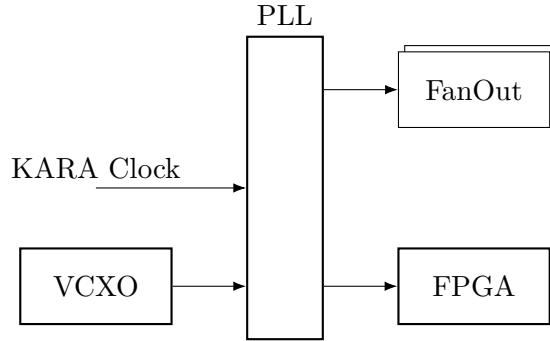
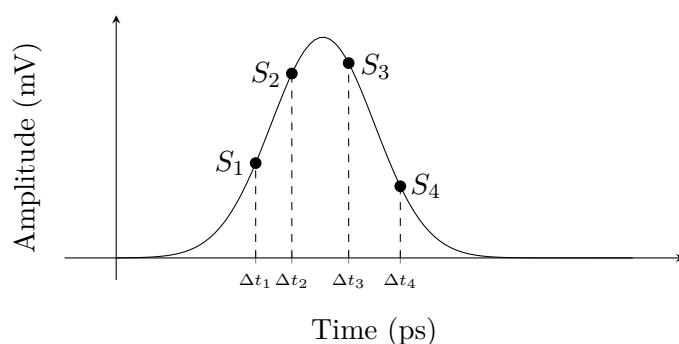


Figure 3.1.: General schema of KAPTURE-2 (cf. [CAB⁺17, p.2])

**Figure 3.2.**

The pulse from the THz detector is fed into a power splitter, which splits the signal into four identical pulses and distributes them to four channels, consisting of a respective Track-And-Hold-Amplifier (THA) unit and a 12-bit ADC@500 MS/s. The sampling time of each unit can be adjusted individually with a Picosecond Delay Chip with a resolution of 3 ps (maximal delay range: 100 ps). The clock signal is provided by KARA, which cleared from jitter by a Phase-Locked-Loop (PLL). This ensures the synchronization of the ADCs with the RF system. The clean clock signal is distributed to the delay chips via fan-out. [CAB⁺17]

The resulting sampling of the detector signal is shown Figure 3.3 (simplified representation).

**Figure 3.3.: Signal with sample points**

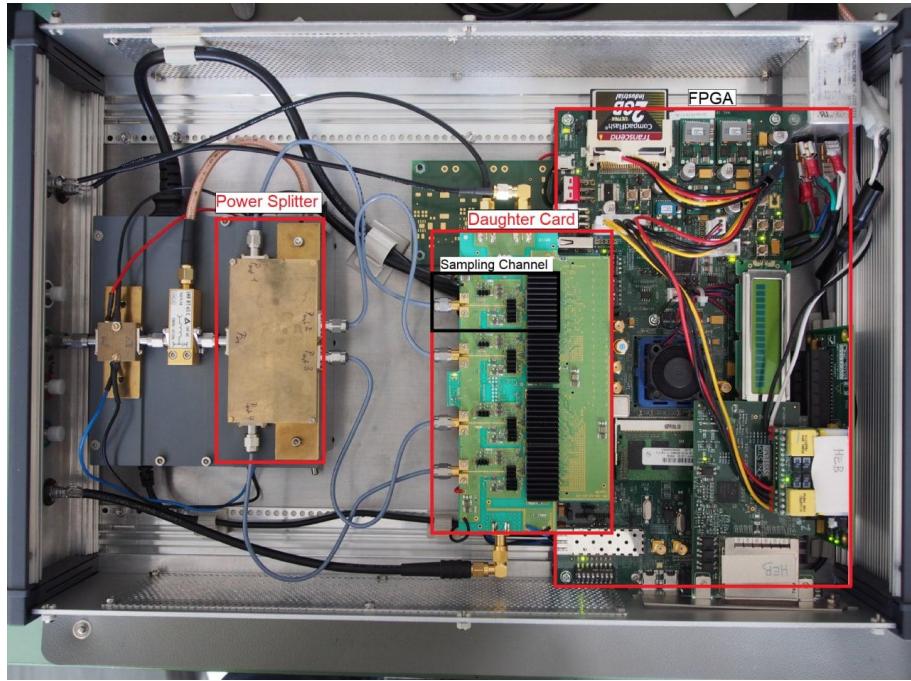


Figure 3.4.: Photo of KAPTURE with highlighted main components. [Bro20, p. 61]

3.1.2. THERESA

In principle, the new system has the same structure, as KAPTURE. Notable differences are firstly the number of ADCs, which is increased up to 16. Secondly, the latter are not located on the daughter card anymore, but inside the Xilinx Zynq UltraScale+ RFSoC ZU49DR on the ZCU216 Evaluation Kit on which the front-end card is mounted. Figure 3.5 shows the general schema of the sampling system, reduced to four channels for presentation purposes.

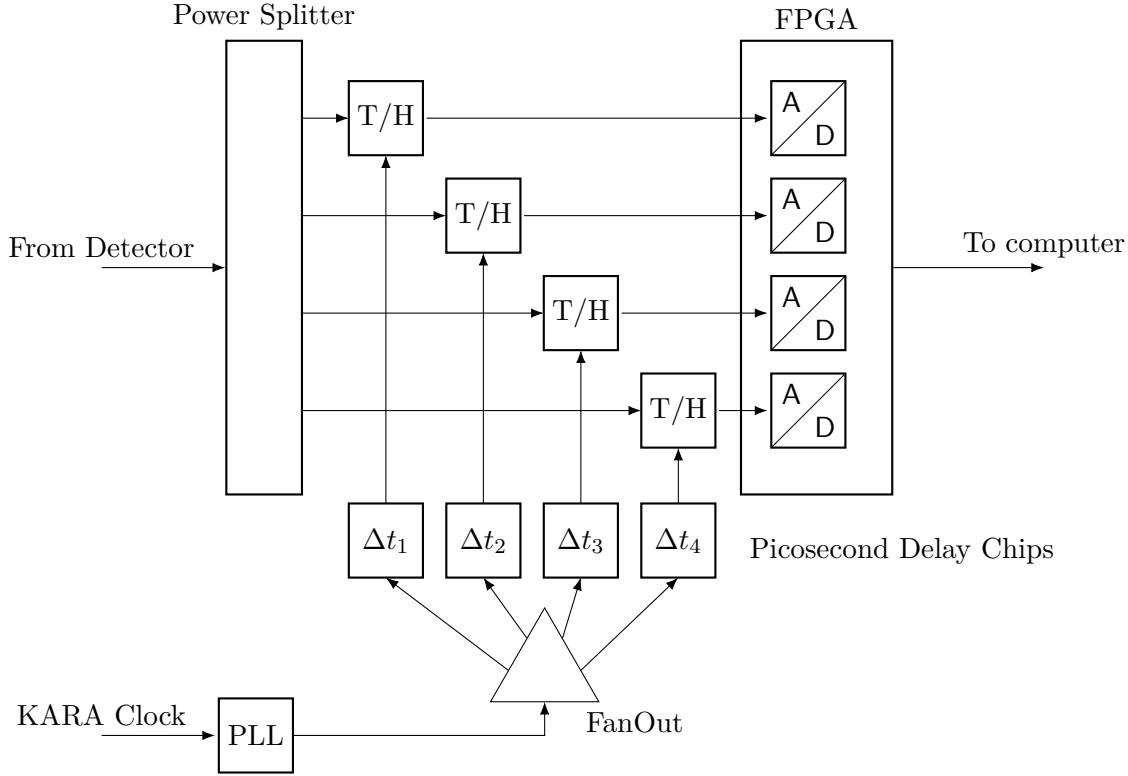


Figure 3.5.: General schema of THERESA. For presentation purposes only four channels are shown.

3.1.2.1. Xilinx Zynq UltraScale+ RFSoC ZCU216 Evaluation Kit

The card, holding the sampling channels, should be mounted on a ZCU216 evaluation board. This board is the newest generation of Xilinx' evaluation cards, which has features suitable for the purpose at hand.

- Sixteen 14-bit, 2.5GSPS RF-ADC
- Sixteen 14-bit, 10GSPS RF-DAC
- I/O expansion options – FPGA Mezzanine Card (FMC+) interfaces, RFMC 2.0 interfaces, and Pmod connections

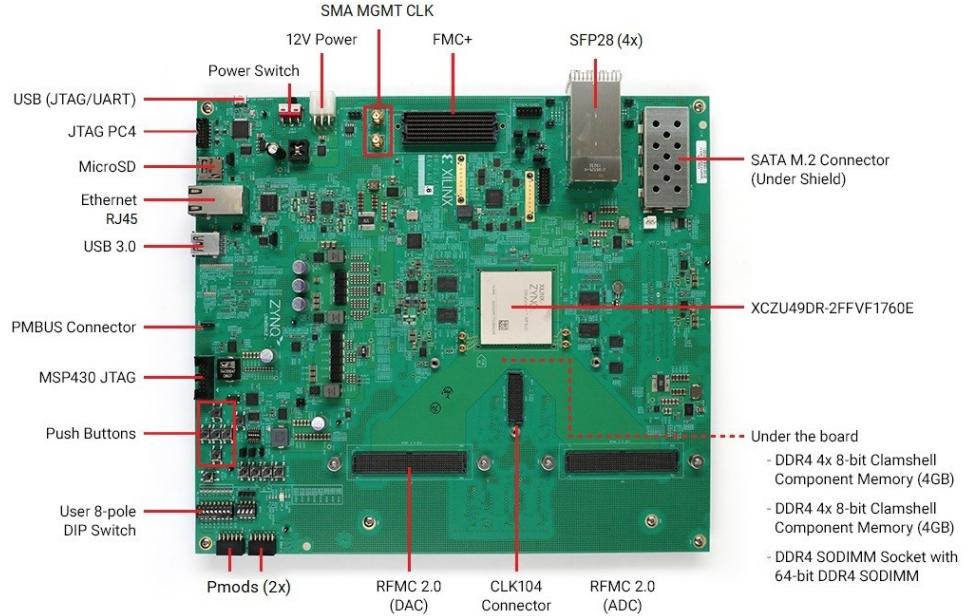


Figure 3.6.: ZCU216 evaluation board

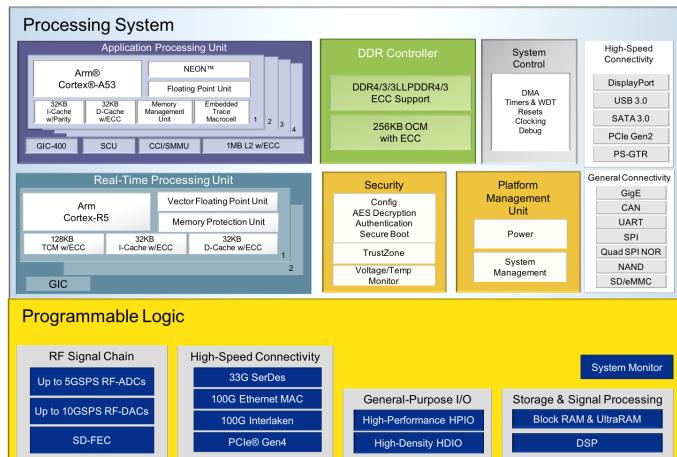


Figure 3.7.: RFSoC block diagram

3.1.3. Requirements

Step size delay chip

The necessary step size for the delay chips, when using 16 ADC@2 GS/s in time-interleaving mode, is: $\frac{2 \text{ GS/s}}{16} = 31 \text{ ps}$

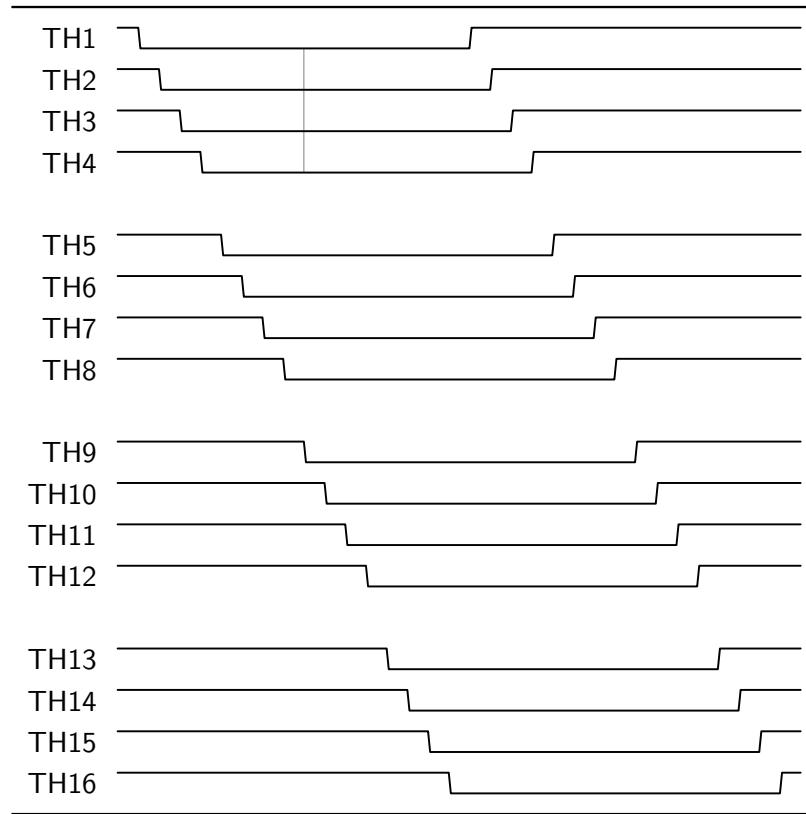
Frequency

Figure 3.8.: Track-And-Hold Timing diagram

Data Rate**Visualization/GUI**

3.2. Design of the front-end card

In this section, the design of the front-end card is covered.

3.2.1. Sampling-Channel

Delay Chip NB6L295

Dual Channel Programmable Delay Chip.

- Two individual variable delay channels
 - Dual Delay: minimal delay 3.2 ns
 - Total Delay Range: 3.2 ns to 8.8 ns per Delay Channel
 - 11 ps Increments in 511 steps
 - 100 ps Typical Rise and Fall Times

3.2.2. Clocking

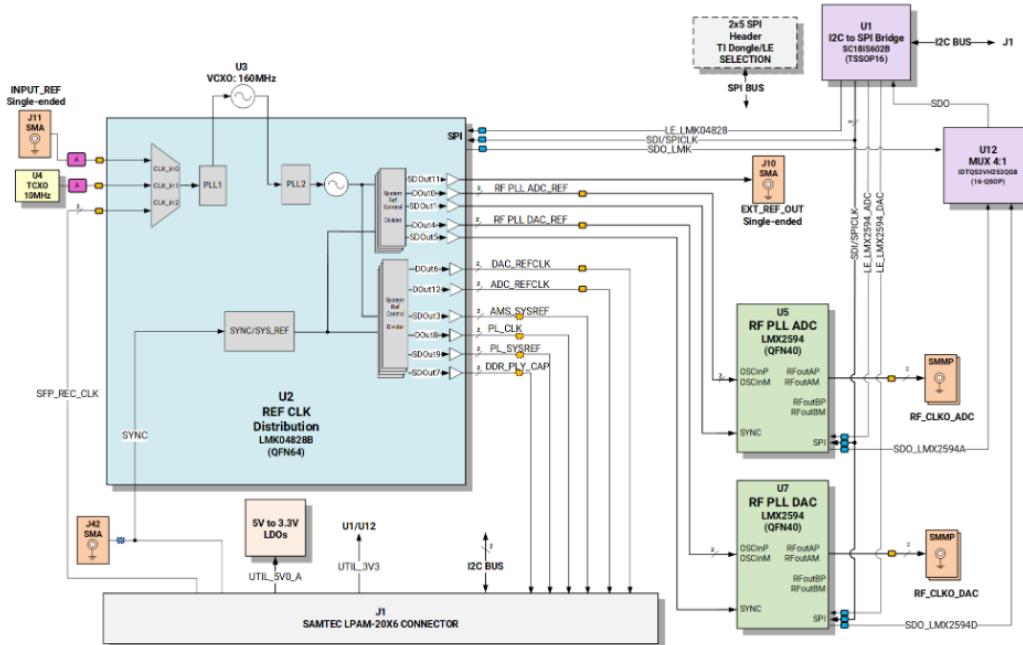


Figure 3.9.: CLK104 Add-on board clocking scheme

3.2.3. Power Supply

For the Track-And-Hold amplifiers a new power supply unit – the ADP1741 (Analog Devices) – should be used. It is necessary to think about the amount of power supply chips needed. As a rule of thumb, the power supply should provide twice the maximum power needed by the components it drives. The power consumption/maximum current for the respective components on the THERESA board is listed in Table 3.1.

The maximal current which the ADP1741 can provide @2 V is 2 A. This means, with one Track-And-Hold amplifier requiring a maximal current of 0.221 A, one ADP1741 can handle four units according to the rule mentioned beforehand ($I_{max_ADP1741} = 2 \text{ A} > 2 * I_{tot}$, $I_{tot} = 4 \times 0.221 \text{ A} = 0.884 \text{ A}$).

Table 3.1.: Power consumption of components on the board

Component	V_{cc} (V)	I_{max} (A)	P_{max} (W)	#parts	I_{tot}^1 (A)
HMC5649 (T/H-Amplifier)	2	0.221	0.442	16	3.536
	-5	-0.242	1.21		3.872
HMC856 (Delay)	-3.3	0.185	-0.611	16	2.96
HMC987LP5E (Fan-Out)	3.3	0.234 ²	0.772	2	0.468
LMC0480 (PLL)	3.3	0.590 ³	1.947	1	0.590
VCXO	3.3	0.03	0.198	1	0.03

¹for 16 ADCs²All Outputs and RF-Buffer³All CLKS

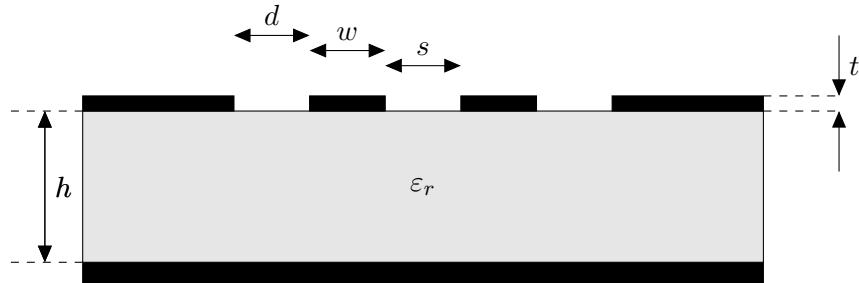
3.3. PCB-Layout

3.3.1. General Techniques/Strategies?

3.3.2. Floor Planning

3.3.3. Transmission lines

Surface Coplanar Waveguide with Ground

**Figure 3.10.:** Edge-Coupled Coplanar Waveguide

The corresponding equations are [Wad91, p197-198]:

$$Z_{0,o} = \frac{\eta_0}{\sqrt{\epsilon_{eff,o}}} \left(\frac{1.0}{2.0 \frac{K(k_o)}{K'(k_o)} + \frac{K(\beta_1)}{K'(\beta_1)}} \right) \quad (3.1)$$

$$Z_{0,e} = \frac{\eta_0}{\sqrt{\epsilon_{eff,e}}} \left(\frac{1.0}{2.0 \frac{K(k_e)}{K'(k_e)} + \frac{K(\beta_1 k_1)}{K'(\beta_1 k_1)}} \right) \quad (3.2)$$

$$\epsilon_{eff,o} = \frac{2.0 \epsilon_r \frac{K(k_o)}{K'(k_o)} + \frac{K(\beta_1)}{K'(\beta_1)}}{2.0 \frac{K(k_o)}{K'(k_o)} + \frac{K(\beta_1)}{K'(\beta_1)}} \quad (3.3)$$

$$\epsilon_{eff,e} = \frac{2.0 \epsilon_r \frac{K(k_e)}{K'(k_e)} + \frac{K(\beta_1 k_1)}{K'(\beta_1 k_1)}}{2.0 \frac{K(k_e)}{K'(k_e)} + \frac{K(\beta_1 k_1)}{K'(\beta_1 k_1)}} \quad (3.4)$$

Where

$$k_o = \Lambda \frac{-\sqrt{\Lambda^2 - t_c^2} + \sqrt{\Lambda^2 - t_B^2}}{t_B \sqrt{\Lambda^2 - t_c^2} + t_c \sqrt{\Lambda^2 - t_B^2}} \quad (3.5)$$

$$k_e = \Lambda' \frac{-\sqrt{\Lambda'^2 - t_c'^2} + \sqrt{\Lambda'^2 - t_B'^2}}{t_B' \sqrt{\Lambda'^2 - t_c'^2} + t_c' \sqrt{\Lambda'^2 - t_B'^2}} \quad (3.6)$$

$$\Lambda = \frac{\sinh^2 \left(\frac{\pi(s/2.0+w+d)}{2.0h} \right)}{2} \quad (3.7)$$

$$t_c = \sinh^2 \left(\frac{\pi(s/2.0+w)}{2.0h} \right) - \Lambda \quad (3.8)$$

$$t_B = \sinh^2 \left(\frac{\pi s}{4.0h} \right) - \Lambda \quad (3.9)$$

$$\Lambda' = \frac{\cosh^2 \left(\frac{\pi(s/2.0+w+d)}{2.0h} \right)}{2} \quad (3.10)$$

$$t_c' = \sinh^2 \left(\frac{\pi(s/2.0+w)}{2.0h} \right) - \Lambda' + 1.0 \quad (3.11)$$

$$t_B' = \sinh^2 \left(\frac{\pi s}{4.0h} \right) - \Lambda + 1.0 \quad (3.12)$$

The parameters have to be chosen according to

$$s + 2.0w + 2.0d \leq h \quad (3.13)$$

to guarantee coplanar propagation. [Wad91]

Surface Coplanar Waveguide with Ground

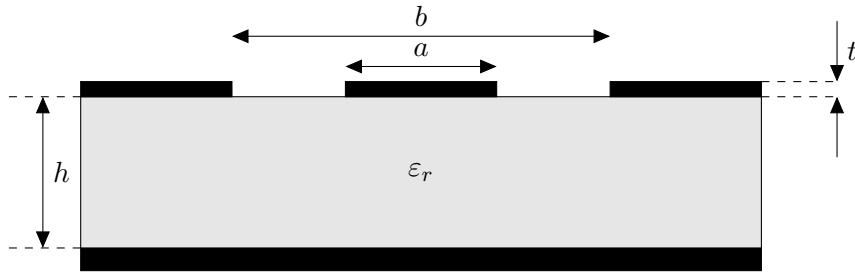


Figure 3.11.: Coplanar Waveguide with Ground

The characteristic impedance of a coplanar waveguide is given as follows [Wad91]:

$$Z_0 = \frac{60.0\pi}{\sqrt{\epsilon_{eff}}} \frac{1.0}{\frac{K(k)}{K(k')} + \frac{K(k_1)}{K(k'_1)}} \quad (3.14)$$

It comprises of the following components, with $K(k)$ being an elliptical integral of the first kind (see also [BSMM99, p. 430]):

$$k = a/b \quad (3.15)$$

$$k' = \sqrt{1.0 - k^2} \quad (3.16)$$

$$k'_1 = \sqrt{1.0 - k_1^2} \quad (3.17)$$

$$k_1 = \frac{\tanh(\frac{\pi a}{4.0 h})}{\tanh(\frac{\pi b}{4.0 h})} \quad (3.18)$$

$$\epsilon_{eff} = \frac{1.0 + \epsilon_r \frac{K(k')}{K(k)} \frac{K(k_1)}{K(k'_1)}}{1.0 + \frac{K(k')}{K(k)} \frac{K(k_1)}{K(k'_1)}} \quad (3.19)$$

3.3.4. Polaris

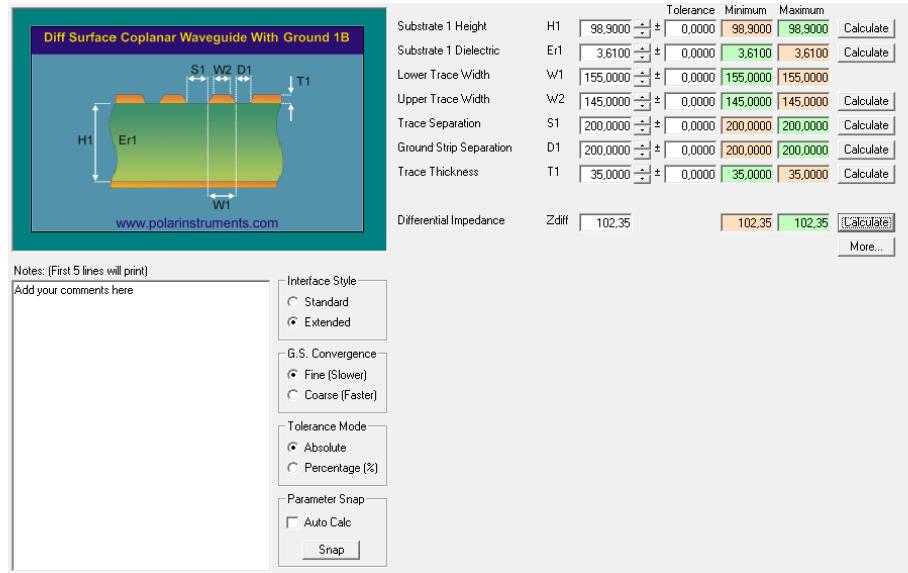


Figure 3.12.: Polaris Solver

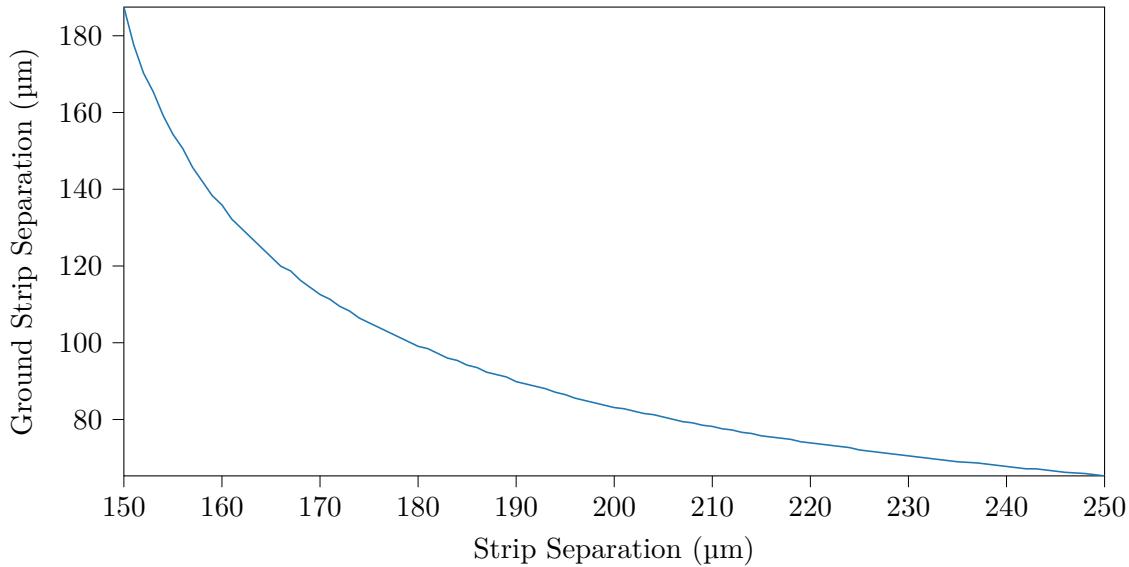


Figure 3.13.: Test Graph

3.4. Firmware

3.4.1. Xilinx Designs

3.4.2. SPI-firmware for components

3.4.3. IPE-AXI IP block

3.4.4. GUI

4. Characterization

4.1. Evaluation of the ZCU216 Board

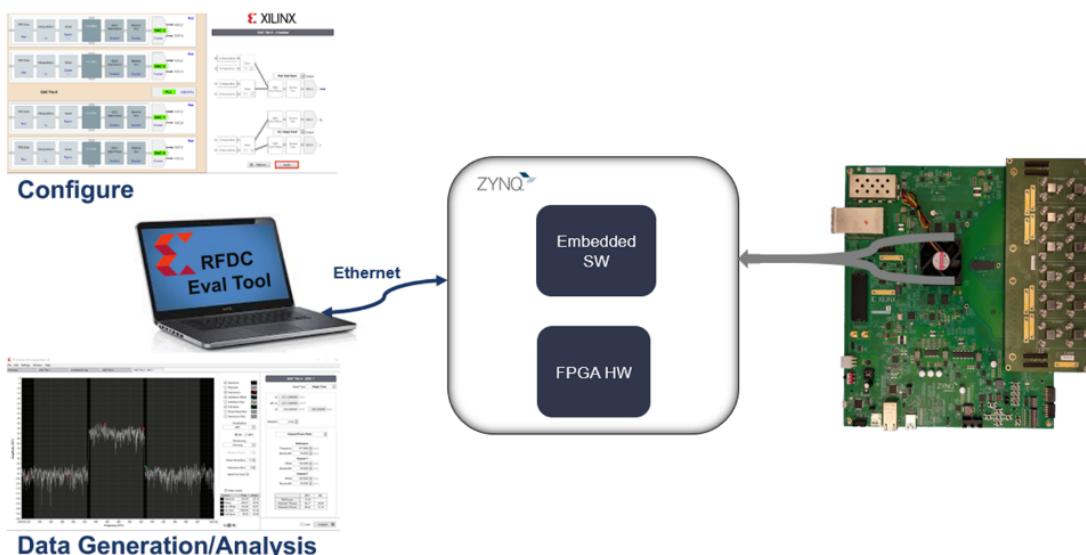


Figure 4.1.: RF DC Evaluation Tool architecture [Xil20a]

4.1.1. Measurements with Xilinx XM655 add-on card

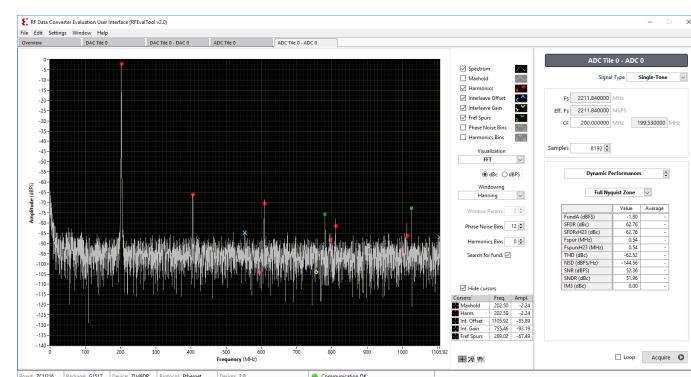


Figure 4.2.: RF DC Evaluation Tool GUI [Xil20a]

4.2. Measurements with the IPE front-end card

5. Conclusions and Outlook

Appendix

A. QuickStart Guide for Evaluation of ZCU216 Board

B. 3D model of front-end card

Bibliography

- [BBB⁺19] Bielawski, Serge, Edmund Blomley, Miriam Brosi, Erik Bründermann, Eva Burkard, Clément Evain, Stefan Funkner, Nicole Hiller, Michael Nasse, Gundrun Niehues und et al.: *From self-organization in relativistic electron bunches to coherent synchrotron light: observation using a photonic time-stretch digitizer*. Scientific Reports, 9(1), July 2019. <http://dx.doi.org/10.1038/s41598-019-45024-2>.
- [Bro20] Brosi, Miriam: *In-Depth Analysis of the Micro-Bunching Characteristics in Single and Multi-Bunch Operation at KARA*. Dissertation, Karlsruher Institut für Technologie (KIT), 2020. 54.01.01; LK 01.
- [BSMM99] Bronstein, Semendjajew, Musiol und Mühlig: *Taschenbuch der Mathematik*. Verlag Harri Deutsch, 1999.
- [CAB⁺17] Caselle, M., L.E. Ardila Perez, M. Balzer, A. Kopmann, L. Rota, M. Weber, M. Brosi, J. Steinmann, E. Bründermann und A. S. Müller: *KAPTURE-2. A picosecond sampling system for individual THz pulses with high repetition rate*. Journal of Instrumentation, 12, 2017.
- [Kes05] Kester, Walt: *The Data Conversion Handbook*. Newnes, 2005.
- [MR15] Manganaro, Gabriele und Dave Robertson: *Interleaving ADCs: Unraveling the Mysteries*. Analog Dialogue, 2015.
- [Pue15] Puente León, Fernando: *Messtechnik - Systemtheorie für Ingenieure und Informatiker*. Vieweg Verlag, 10. aufl. Auflage, 2015, ISBN 978-3-662-44820-5.
- [Rot18] Rota, Lorenzo: *KALYPSO, a novel detector system for high-repetition rate and real-time beam diagnostics*. Dissertation, Karlsruher Institut für Technologie (KIT), 2018. 54.02.02; LK 01.
- [Rou14] Roussel, Eleonore: *Spatio-temporal dynamics of relativistic electron bunches during the microbunching instability: study of the Synchrotron SOLEIL and UVSOR storage rings*. Dissertation, September 2014.
- [Wad91] Wadell, Brian C.: *Transmission Line Design Handbook*. Artech House, 1991.
- [Xil20a] Xilinx: *UG1433 - Zynq UltraScale+ RFSoCZCU208 and ZCU216 RFData Converter Evaluation Tool User Guide*. https://www.xilinx.com/support/documentation/boards_and_kits/zcu216/ug1433-zcu216-rfsoc-eval-tool.pdf, June 2020.
- [Xil20b] Xilinx: *UG1437 - CLK104 RF Clock Add-onCard User Guide*. https://www.xilinx.com/support/documentation/boards_and_kits/zcu216/ug1437-clk104.pdf, March 2020.