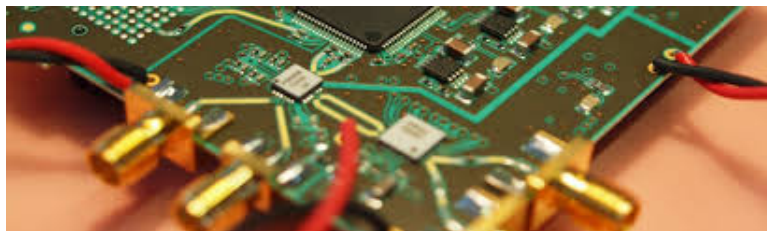


A Terabit sampling system with a photonics time-stretch ADC

Master Thesis
of

Olena Manzhura

at the Institute for Data Processing and Electronics (IPE)



Reviewer: Prof. Dr. Anke-Susanne Müller (LAS)
Second Reviewer: Dr. Michele Caselle (IPE)

15.11.2020 – 14.05.2021

Erklärung zur Selbstständigkeit

Ich versichere, dass ich diese Arbeit selbstständig verfasst habe und keine anderen als die angegebenen Quellen und Hilfsmittel benutzt habe, die wörtlich oder inhaltlich übernommenen Stellen als solche kenntlich gemacht und die Satzung des KIT zur Sicherung guter wissenschaftlicher Praxis in der gültigen Fassung vom 24.05.2018 beachtet habe.

Karlsruhe, den 14.05.2021, _____
Olena Manzhura

Als Prüfungsexemplar genehmigt von

Karlsruhe, den 14.05.2021, _____
Prof. Dr. Anke-Susanne Müller (LAS)

Abstract

Zusammenfassung

Résumé

Contents

1. Introduction	1
2. Theoretical Background	3
2.1. Synchrotron/Terahertz radiation/Electron bunch?	3
2.2. YBCO detector?	4
2.3. Time-Stretch Analog-to-Digital-Converter	4
2.4. State of the art: KAPTURE-2	4
2.5. New Board	5
3. Work	7
3.1. Power Supply	7
4. Conclusions	9
Appendix	11
A. First Appendix Section	11

List of Figures

2.1.	Electro-Magnetic spectrum	3
2.2.	General schema of KAPTURE-2	4
2.3.	Signal with sampled points	4
3.1.	Schema with PLL. Red: only in "time-stretch-mode"	8

List of Tables

3.1. Power consumption of KAPTURE-2 components	7
3.2. CLKOut Groups of PLL LMK0480	7

List of abbreviations

LVC MOS Low voltage complementary metal oxide semiconductor

LVDS Low-voltage differential signaling

LVPECL Low-voltage positive emitter-coupled logic

1. Introduction

2. Theoretical Background

2.1. Synchrotron/Terahertz radiation/Electron bunch?

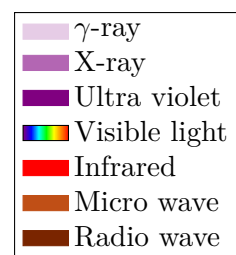
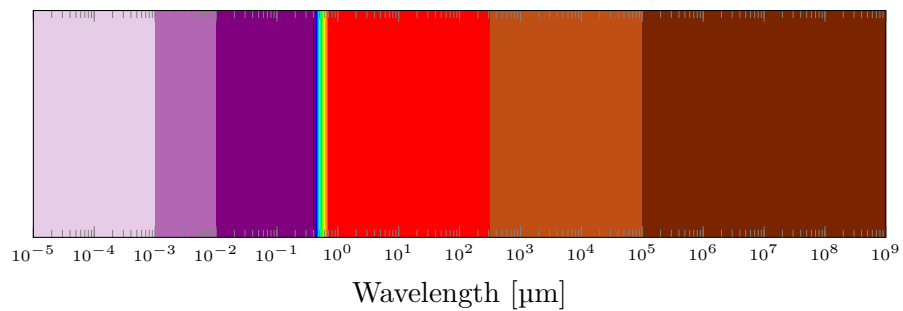


Figure 2.1.: Electro-Magnetic spectrum

2.2. YBCO detector?

2.3. Time-Stretch Analog-to-Digital-Converter

2.4. State of the art: KAPTURE-2

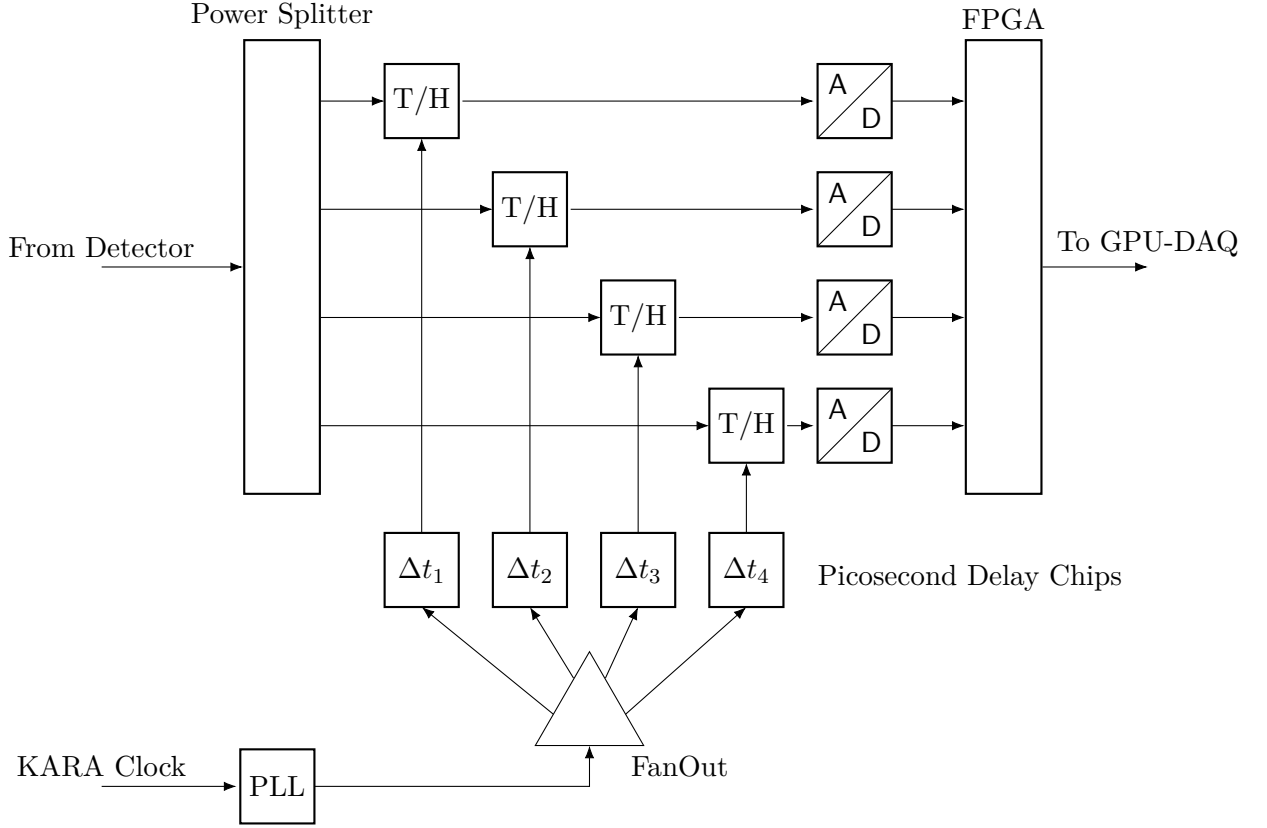


Figure 2.2.: General schema of KAPTURE-2

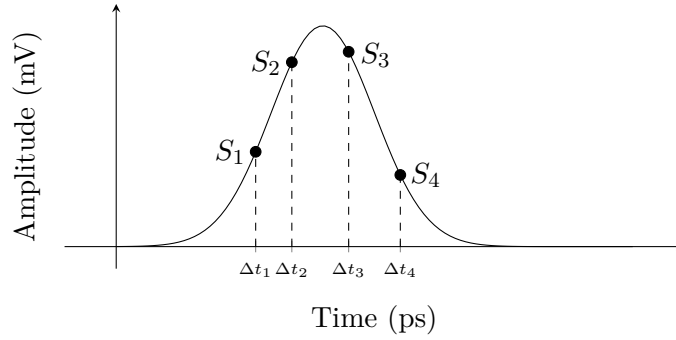


Figure 2.3.: Signal with sampled points

2.5. New Board

3. Work

3.1. Power Supply

Table 3.1.: Power consumption of KAPTURE-2 components

Component	V_{cc} (V)	I_{max} (A)	P_{max} (W)	$\#_{parts}$	I_{tot}^1 (A)
HMC5649 (T/H-Amplifier)	2	0.221	0.442	16	3.536
	-5	-0.242	1.21		3.872
HMC856 (Delay)	-3.3	0.185	-0.611	16	2.96
HMC987LP5E (Fan-Out)	3.3	0.234 ²	0.772	2	0.468
LMC0480 (PLL)	3.3	0.590 ³	1.947	?	???
VCXO	3.3	0.03	0.198	?	???

¹for 16 ADCs

²All Outputs and RF-Buffer

³All CLKs

PLL LMK0480

The LMK0480 is used for jitter cleaning of the clock signal coming from KARA. It feeds to the FanOut, FPGA and – in KAPTURE-2 – to the ADCs.

- Number of CLKOuts: 11
- CLKOuts are grouped together as follows

Table 3.2.: CLKOut Groups of PLL LMK0480

Clock Group	Clock Outputs
0	CLKout0, CLKout1
1	CLKout2, CLKout3
2	CLKout4, CLKout5
3	CLKout6, CLKout7
4	CLKout8, CLKout9
5	CLKout10, CLKout11

- Adjustable delay at CLKouts:
 - **Fine, analog delay:** Step size 25 ps, range from 0 to 475 ps
 → Enabling adds a nominal 500 ps of delay in addition to the programmed value.

- **Coarse, digital delay:** Delay of 4.5 to 12 clock distribution path cycles (normal mode) or 12.5 to 522 VCO cycles (extended mode) → step as small as half of period of clock distribution path cycle (using `CLKoutX_Y_HS` bit, when output divide value > 1)
- Fixed digital delay is determined by the frequency of distribution path. With an external VCO the resolution (one delay step) is determined by:

$$DD_{Res} = \frac{1}{2 \times VCO_Frequency} \quad (3.1)$$

For a desired delay `CLKX_Y_DDLY` and `CLKX_Y_HS` have to be set accordingly, with **X** being the even and **Y** being the odd number of the `CLKout` in the group.

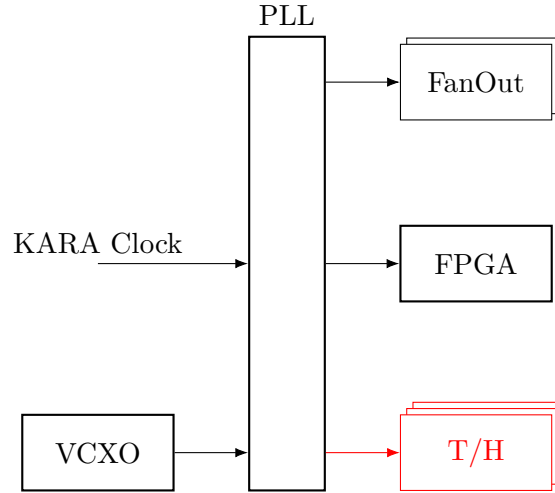


Figure 3.1.: Schema with PLL. Red: only in "time-stretch-mode"

4. Conclusions

Appendix

A. First Appendix Section