Karlsruher Institut für Technologie

Université de Lille 1 SCIENCES ET TECHNOLOGIES

PhLAM

ATP Accelerator Technology Platform @ KIT

IPE

THERESA (TeraHErtz REadout Sampling)

A Terabit sampling system with a photonics time-stretch ADC

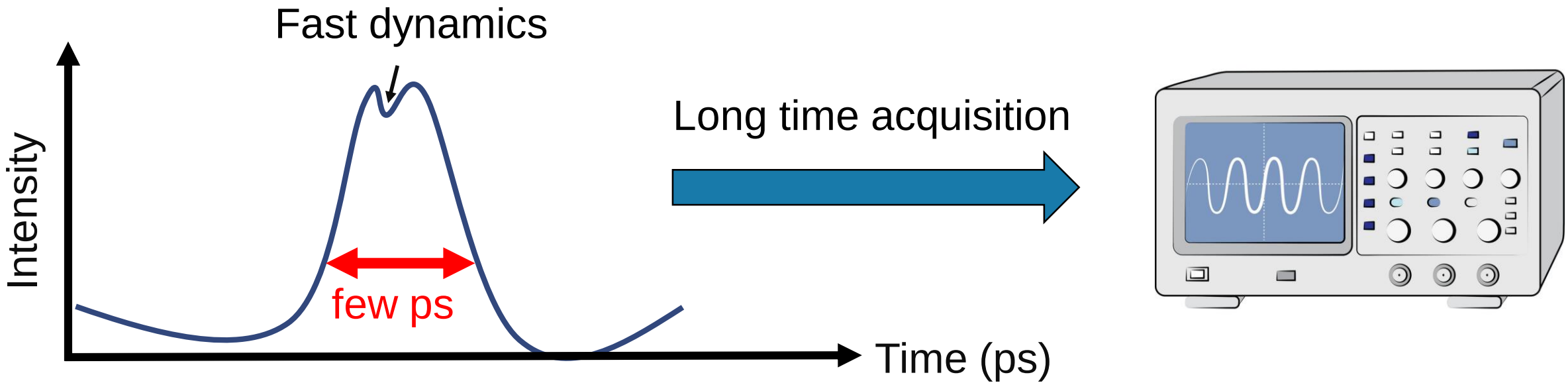
Olena Manzhura

Advisor: *Prof. Anke-Susanne Müller*

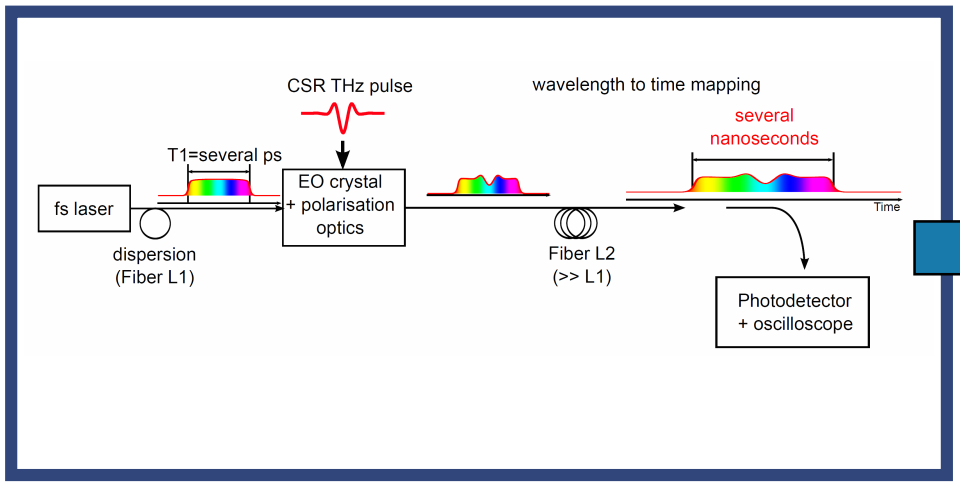
Scientific advisor: *Dr. Michele Caselle*

Motivation: Realizing Ultra-Fast Measurements

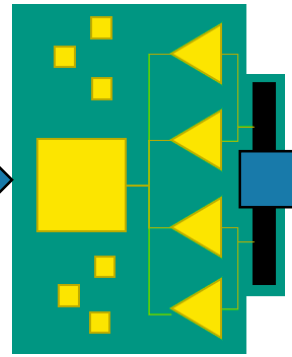
- Study of complex dynamics is crucial for understanding numerous physical processes (e.g. in beam diagnostics, laser dynamics, …)
- Time scale of dynamics: 10 fs to hundreds of ps
- Long time continuous acquisition (1 s to several hours) required



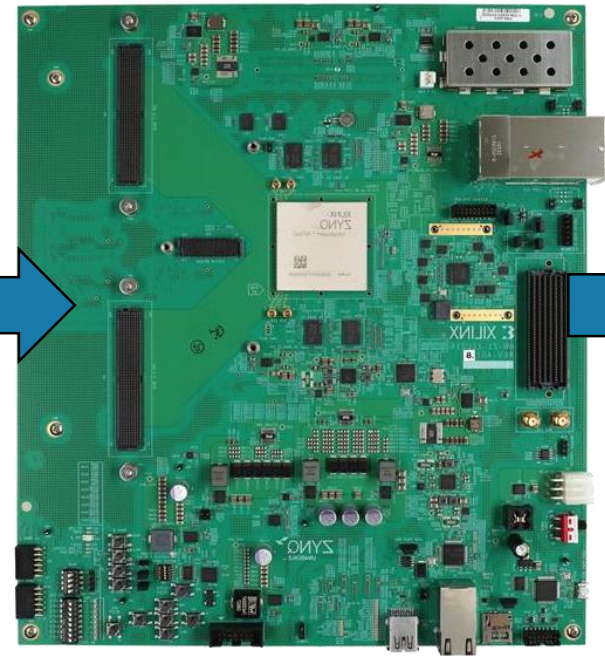
THERESA (TeraHErtz REadout SAmpling)



Front-End
Sampling Card

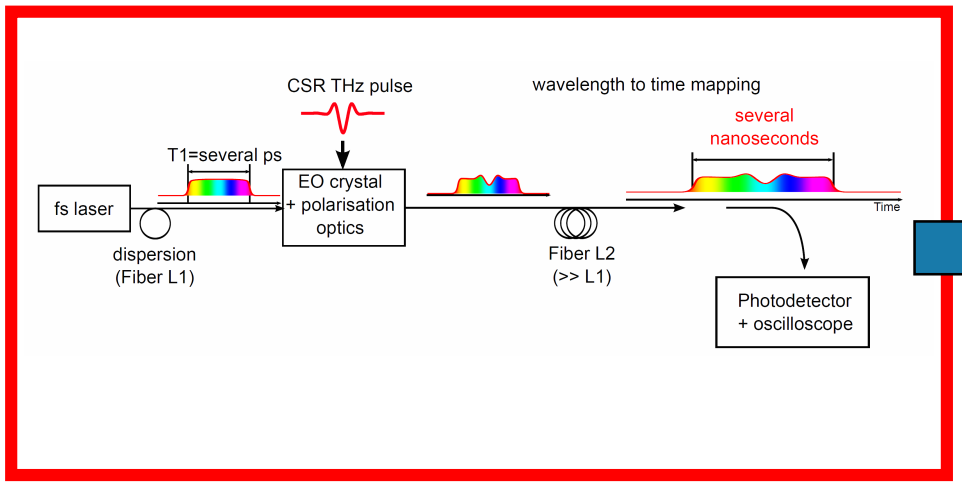


Back-End
Readout Card

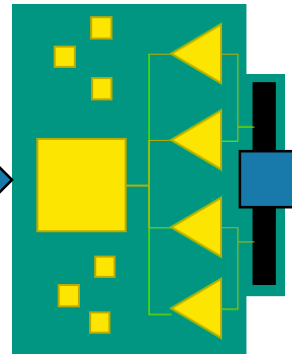


DATA

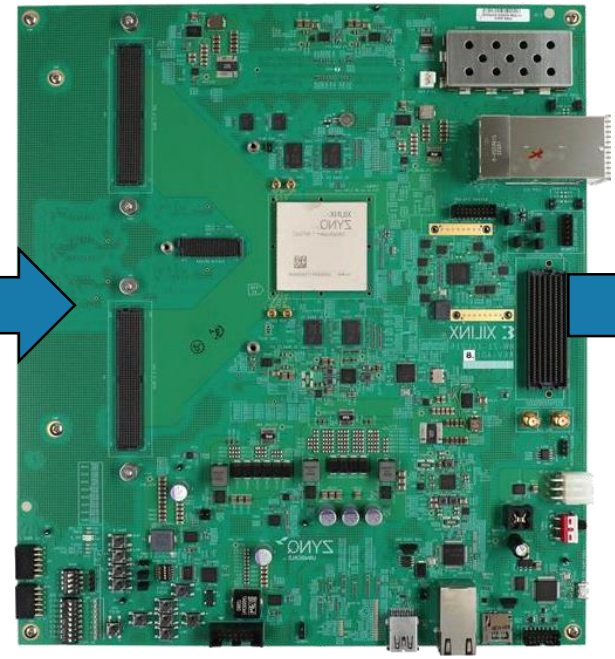
THERESA (TeraHErtz REadout SAmpling)



Front-End
Sampling Card



Back-End
Readout Card



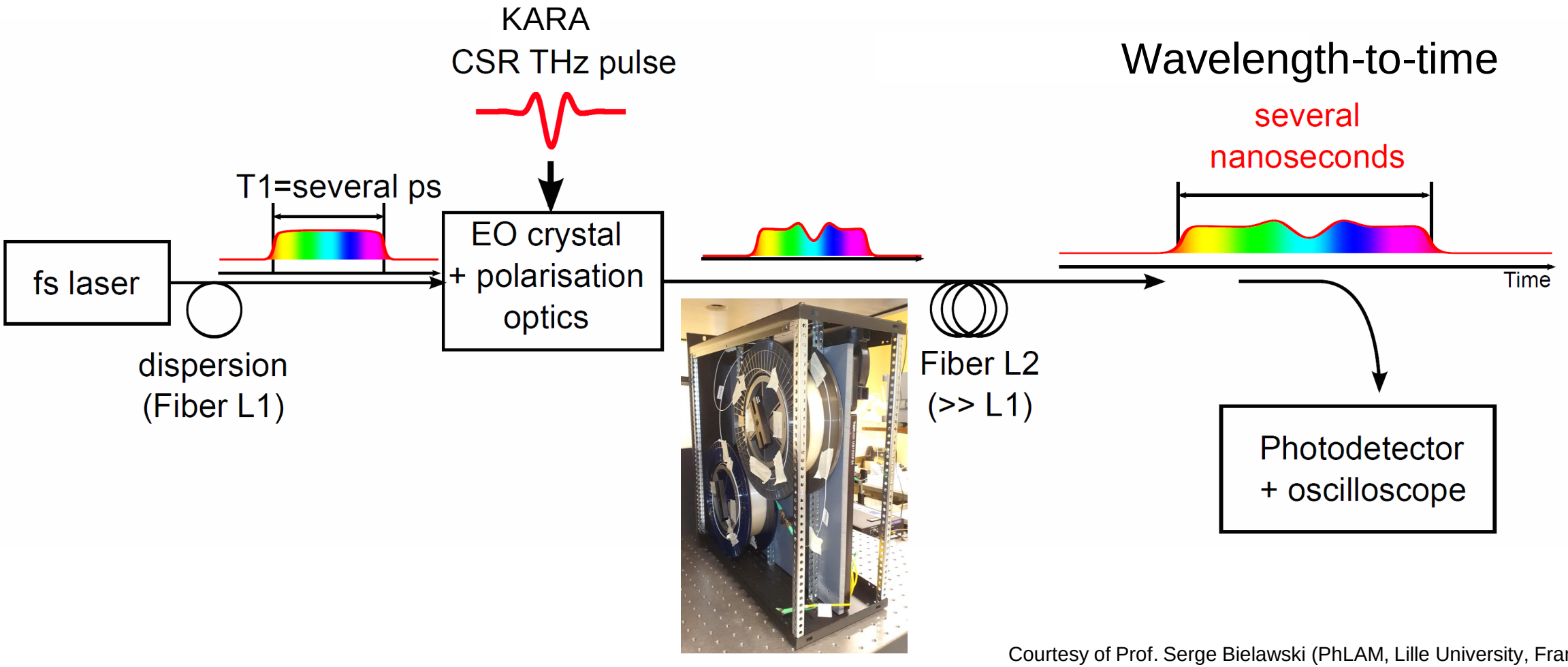
DATA

My contribution

PhLAM

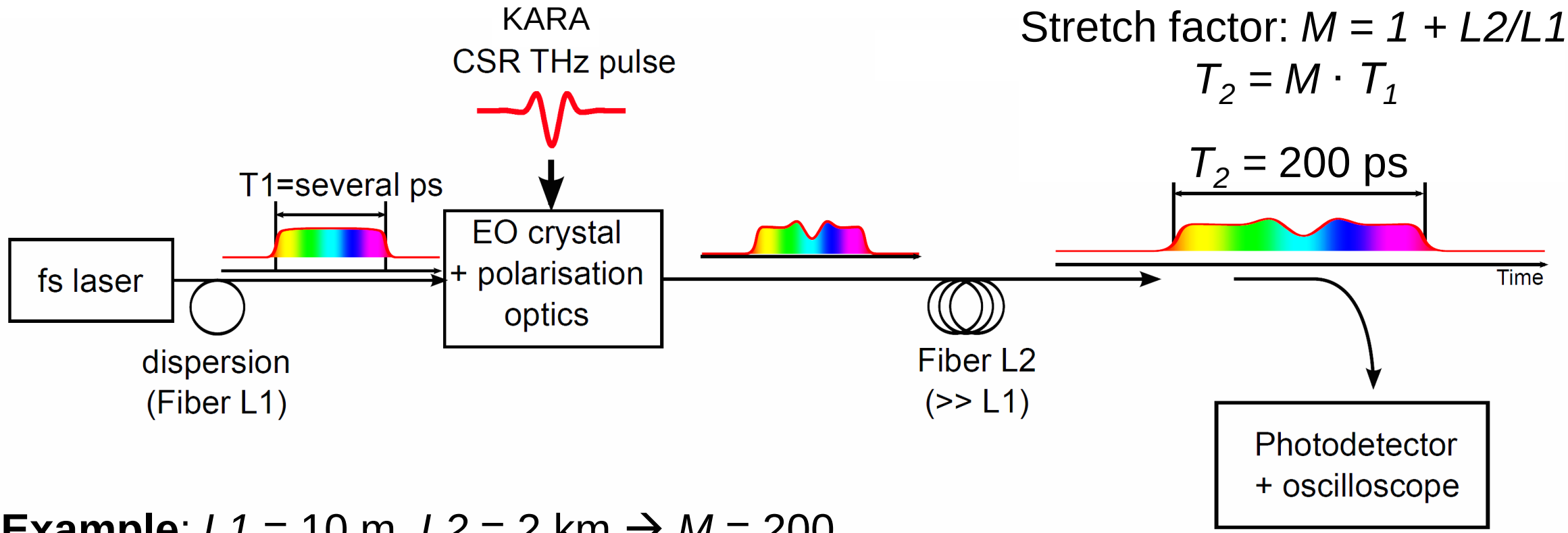
Collaboration with
Prof. S. Bielawski
(Lille University)

Photonic Time-Stretch Method



Courtesy of Prof. Serge Bielawski (PhLAM, Lille University, France)

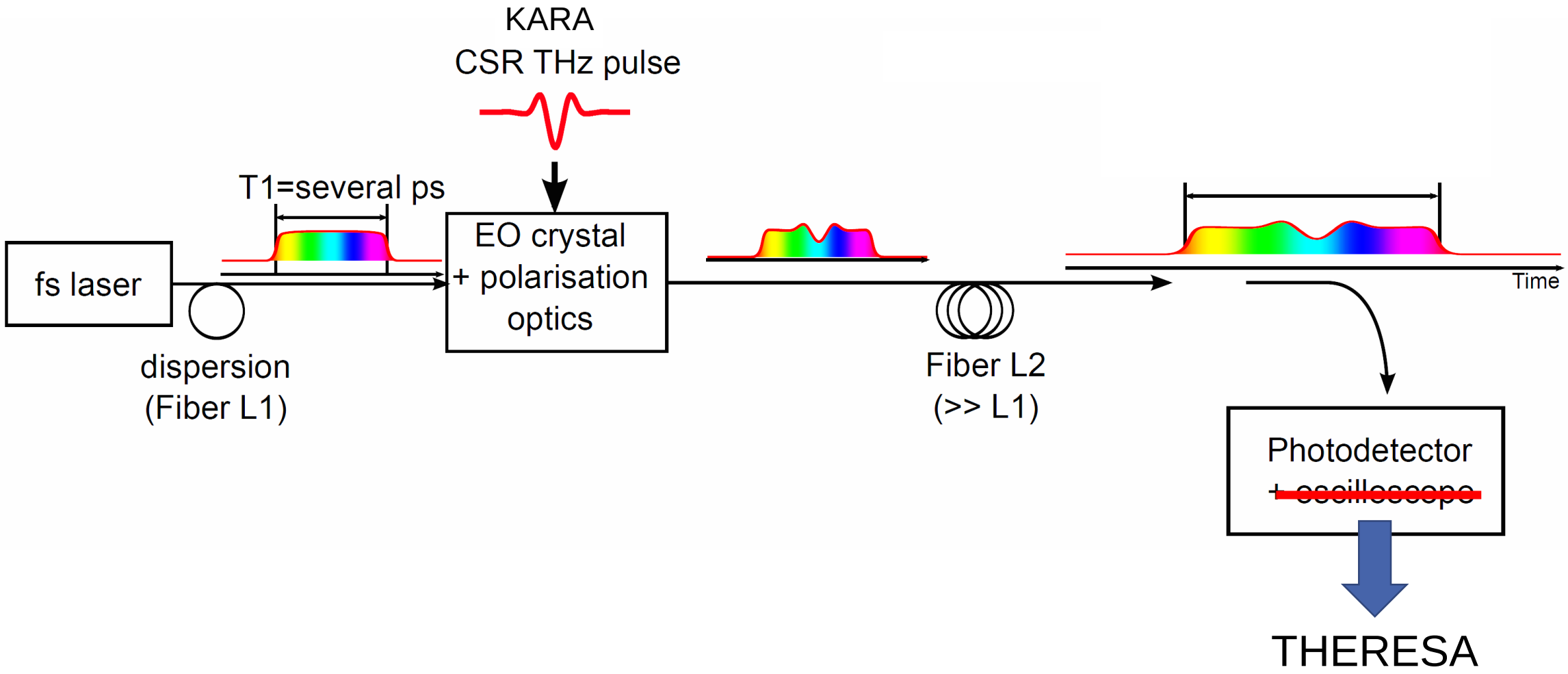
Photonic Time-Stretch Method



Example: *L1* = 10 m, *L2* = 2 km → *M* = 200

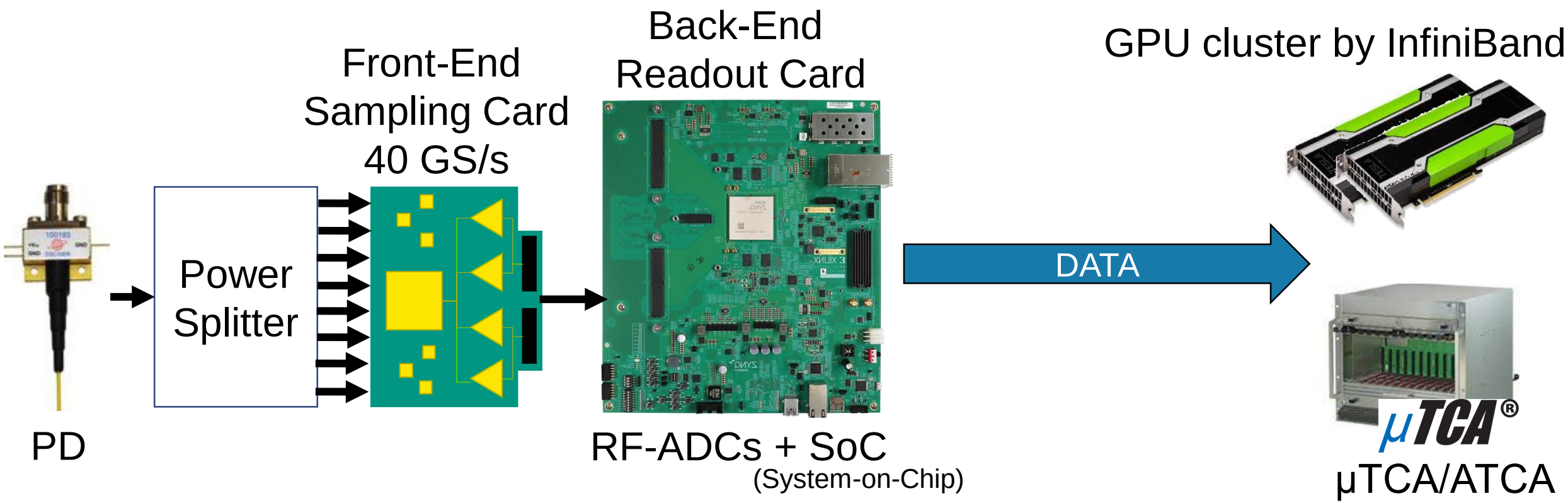
T_1 = 1 ps ≙ 1 THz → T_2 = 200 ps ≙ 5 GHz

Photonic Time-Stretch Method

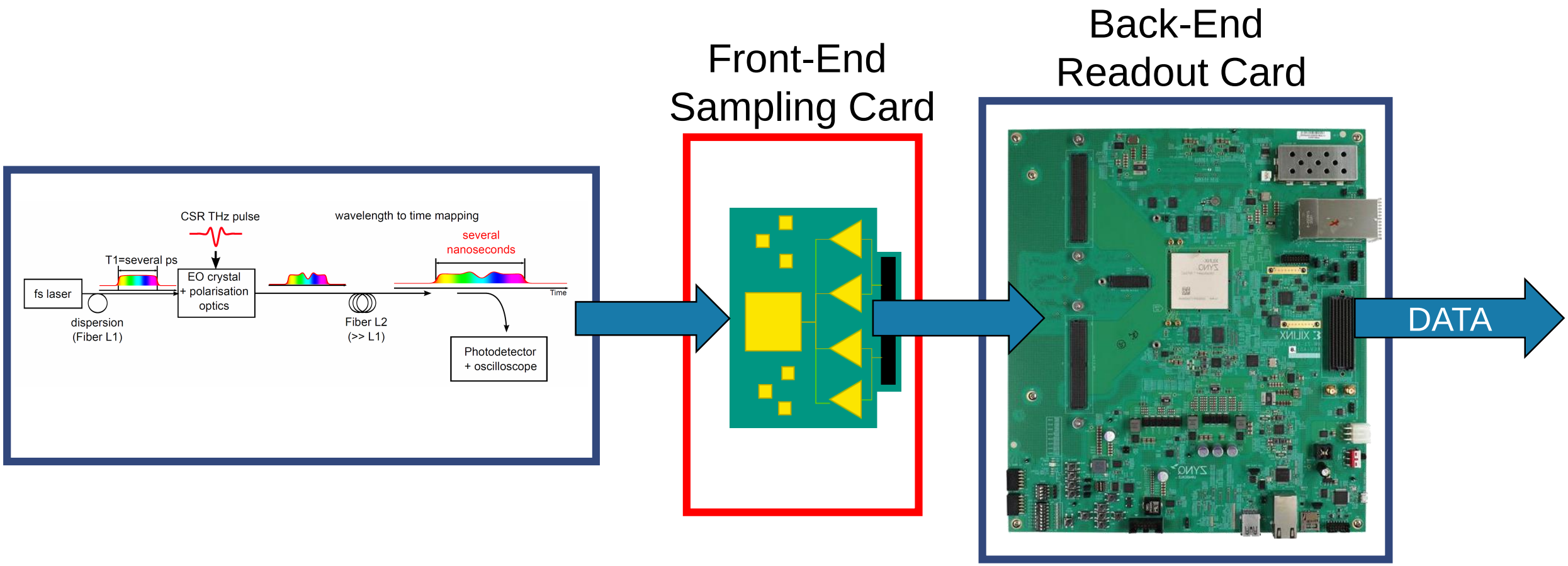


Thesis Objective

- Design a DAQ system, operating in continuous acquisition mode, to sample the photodetector (PD) signal and overcome memory limitation

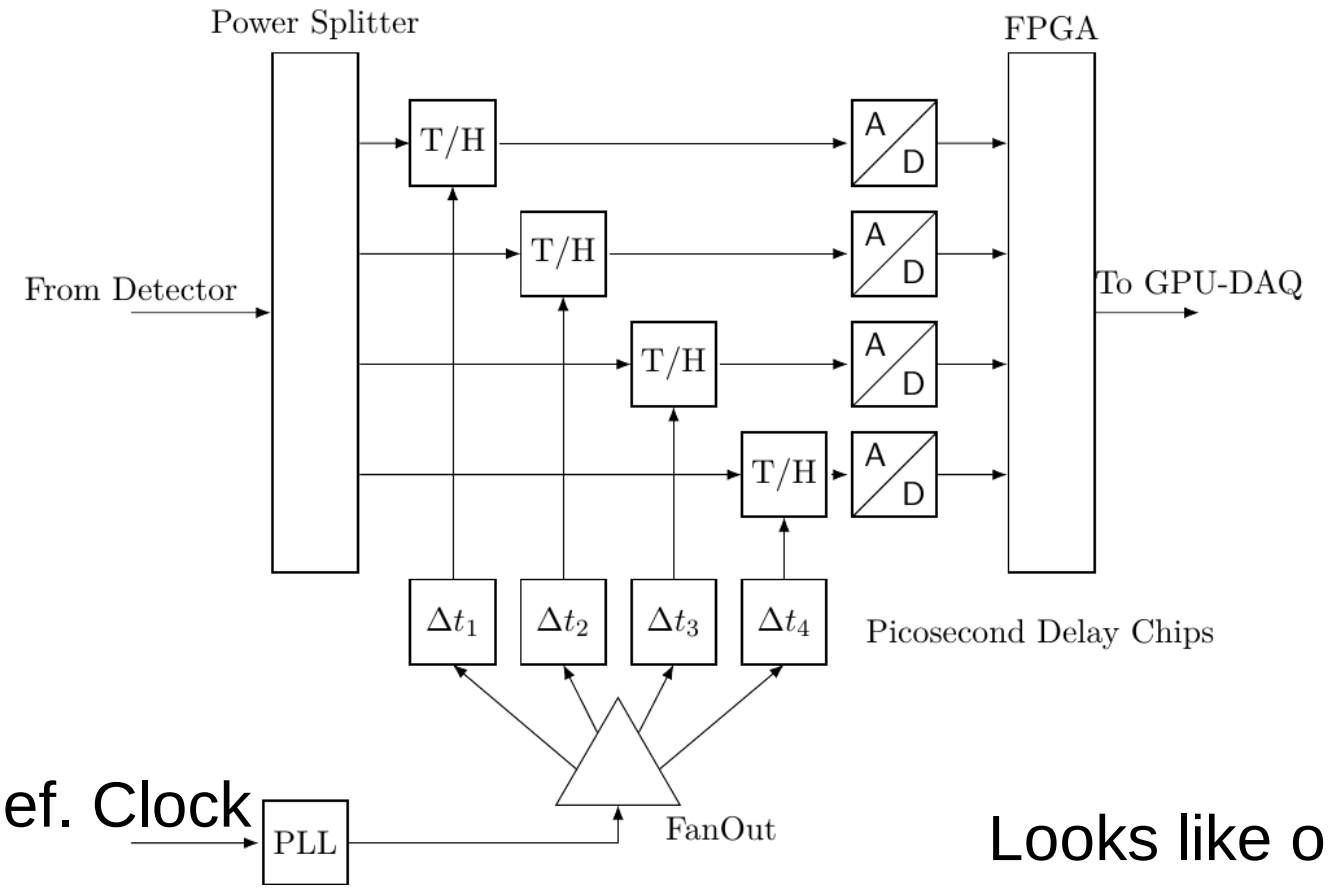


THERESA (TeraHErtz REadout SAmpling)

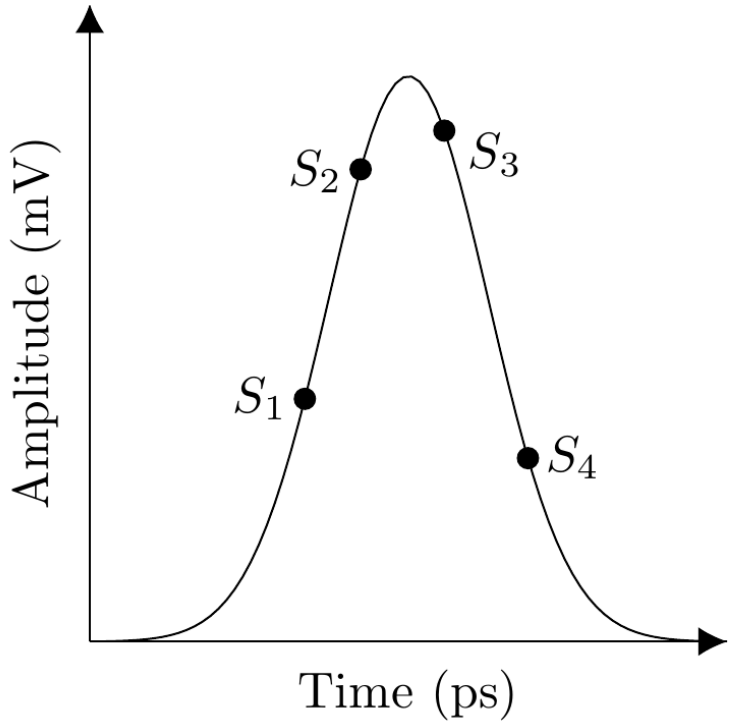


Sampling Concept: Programmable Time Delay

KAPTURE Concept



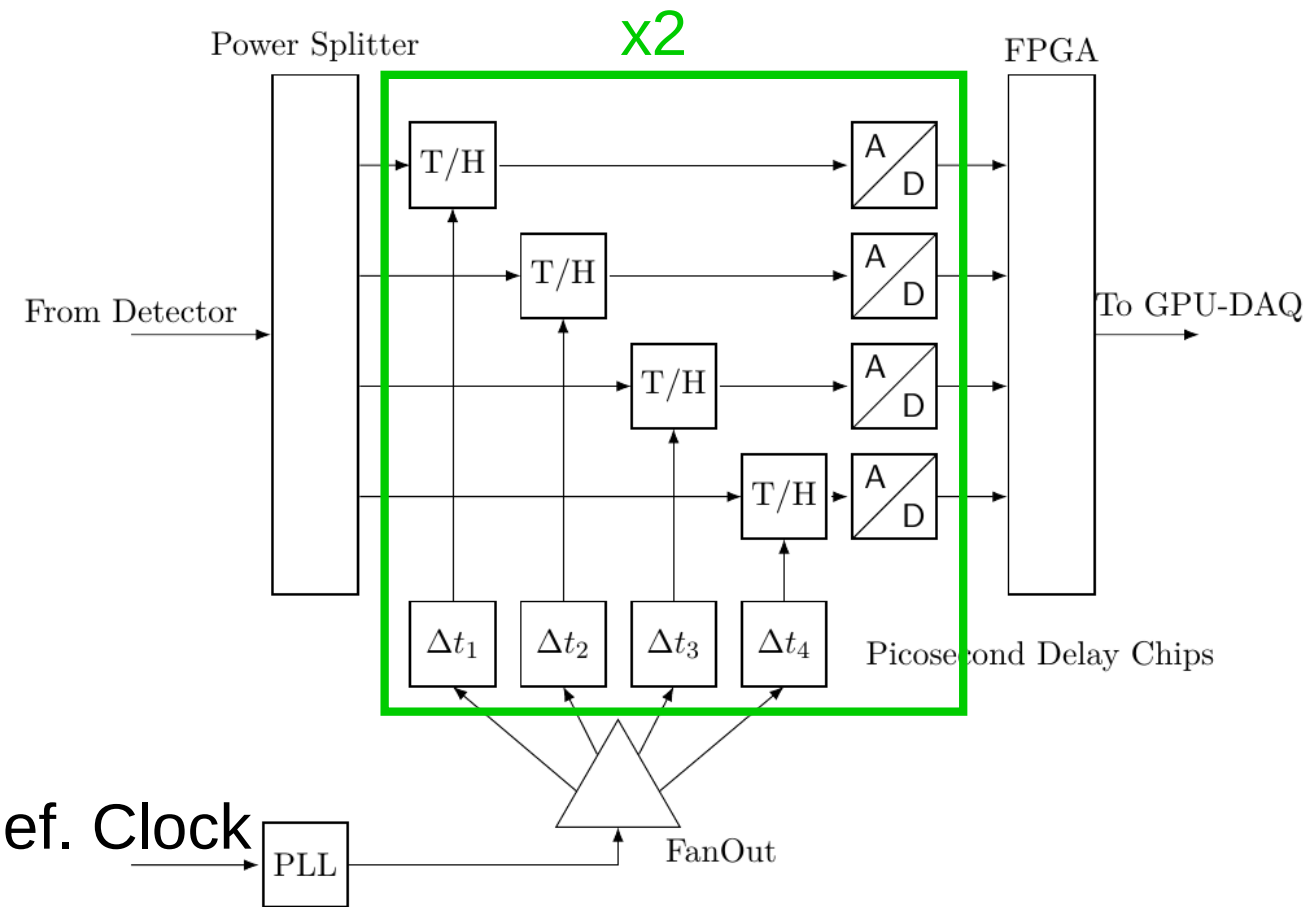
4 Samples



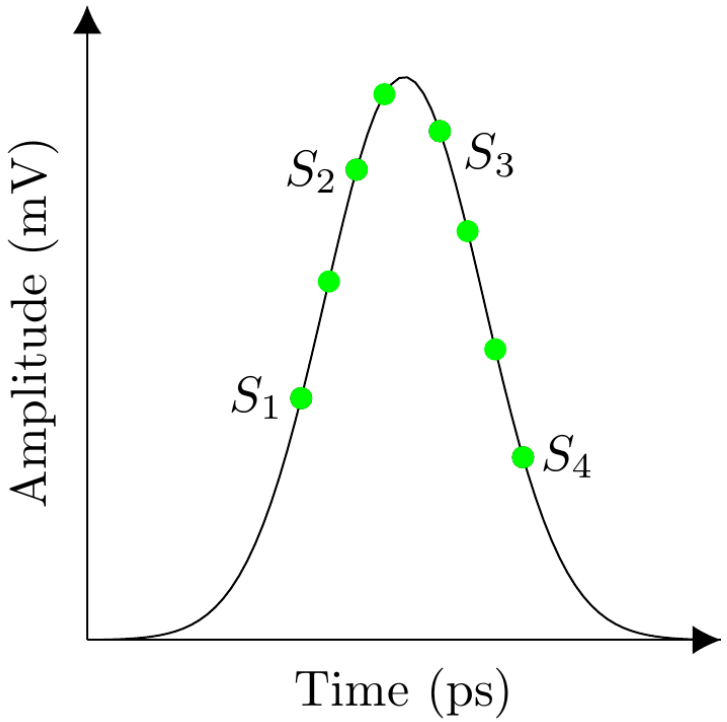
Looks like one ADC sampling at fast sample rate

Sampling Concept: Programmable Time Delay

KAPTURE v2 Concept

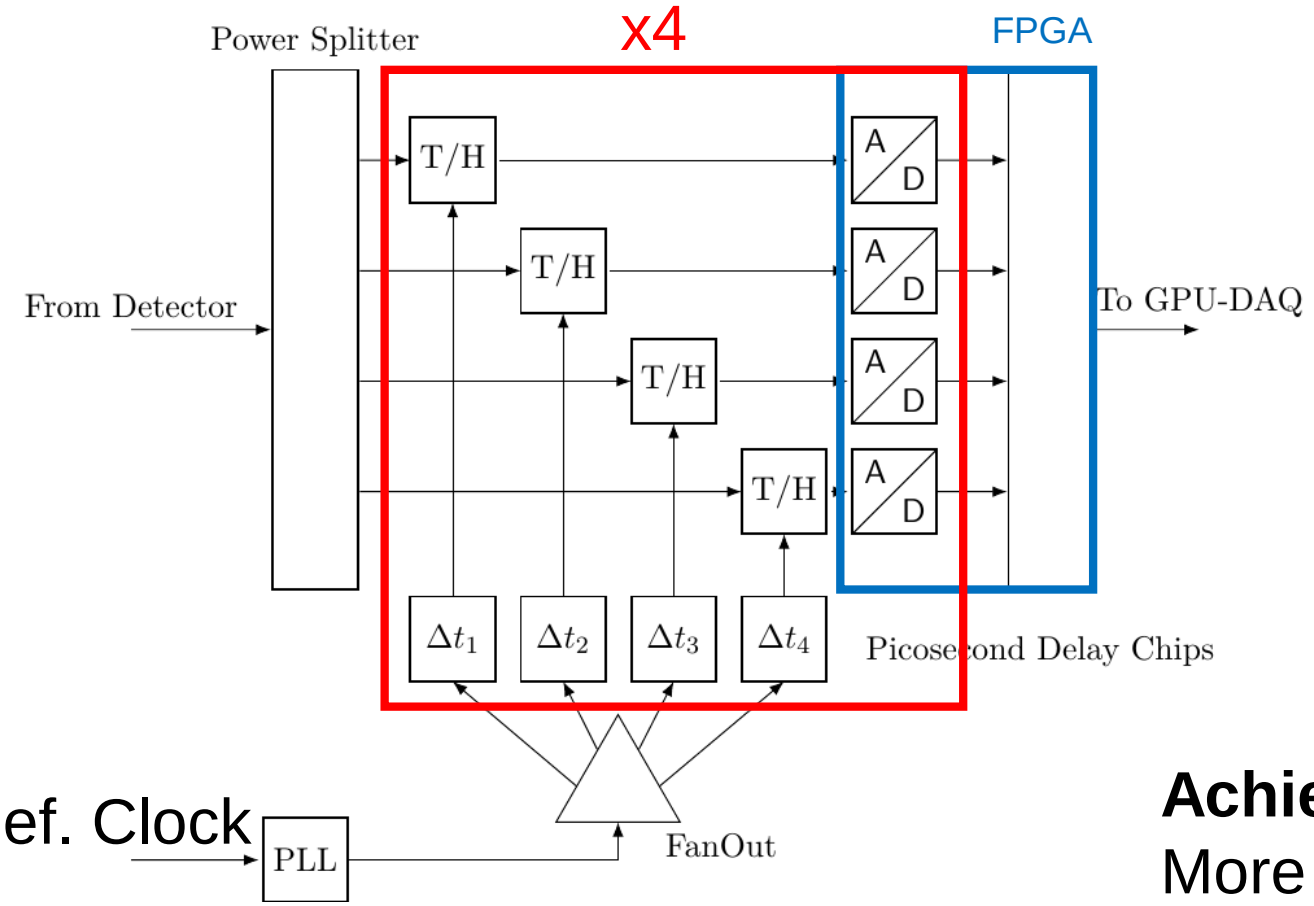


8 Samples

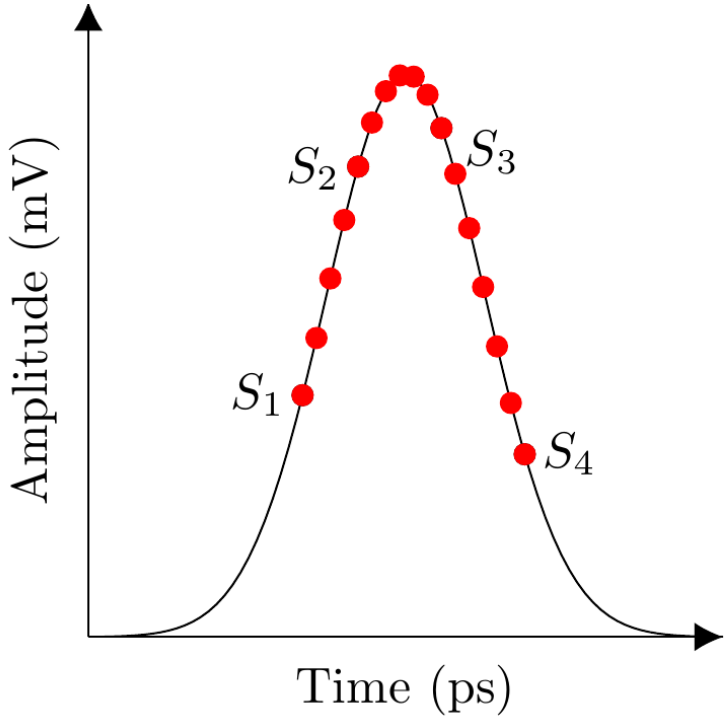


Sampling Concept: Programmable Time Delay

THERESA Concept



16 Samples



Achievements:
More samples + reduced board complexity

Characteristics of THERESA

Features	KAPTURE v2	THERESA
# Channels	8	**16**
Sampling rate per channel	1.8 GS/s per channel	**2.5 GS/s** per channel
Max. sampling rate (time-interleaved)	4 channels: up to 7.2 GS/s 8 channels: up to 14.4 GS/s	Up to **40 GS/s** (16 x 2.5 GS/s)
Operation modes	• Single channel → 1sample/channel • Multiple sampling points (up to 8)	• Photonic Time-Stretch ADC (TS-ADC)
Expected time resolution	3 ps	**125 fs** (e.g.: stretch factor M=200)
Delay range	3 - 100 ps (→ not suitable for time-stretch)	0 - **11.2 ns** (with 511 programmable steps)

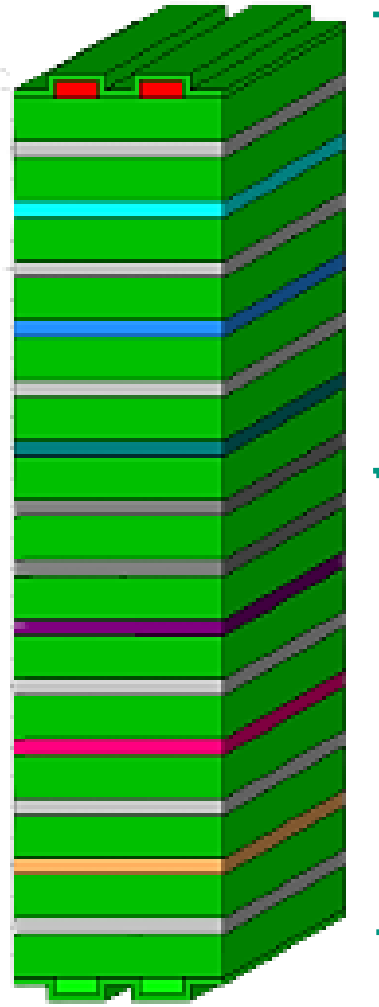
Design Challenges in Front-End Card

- Wide bandwidth (Track-and-Hold-Amplifier(THA) limits to 18 GHz)
- Very low-noise conditions (THA limits to 60 dB SINAD[1], ENOB[2] ≈ 10 bits)
- HF PCB dielectric, metal layer stack-up, RF components/filters, impedance matching, etc.
- High-speed and time skew controlled transmission lines
- Slow-control and calibration circuits

[1] Signal-to-Noise-and-Distortion ratio

[2] Effective-Number-of-Bits

PCB Design : Substrate & Metal Layer Stackup

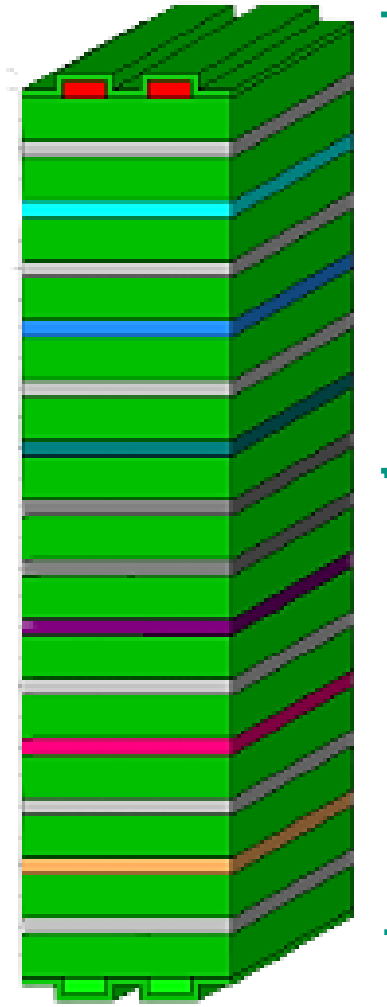


Separate analog from digital:

Digital part

Analog part

PCB Design : Substrate & Metal Layer Stackup



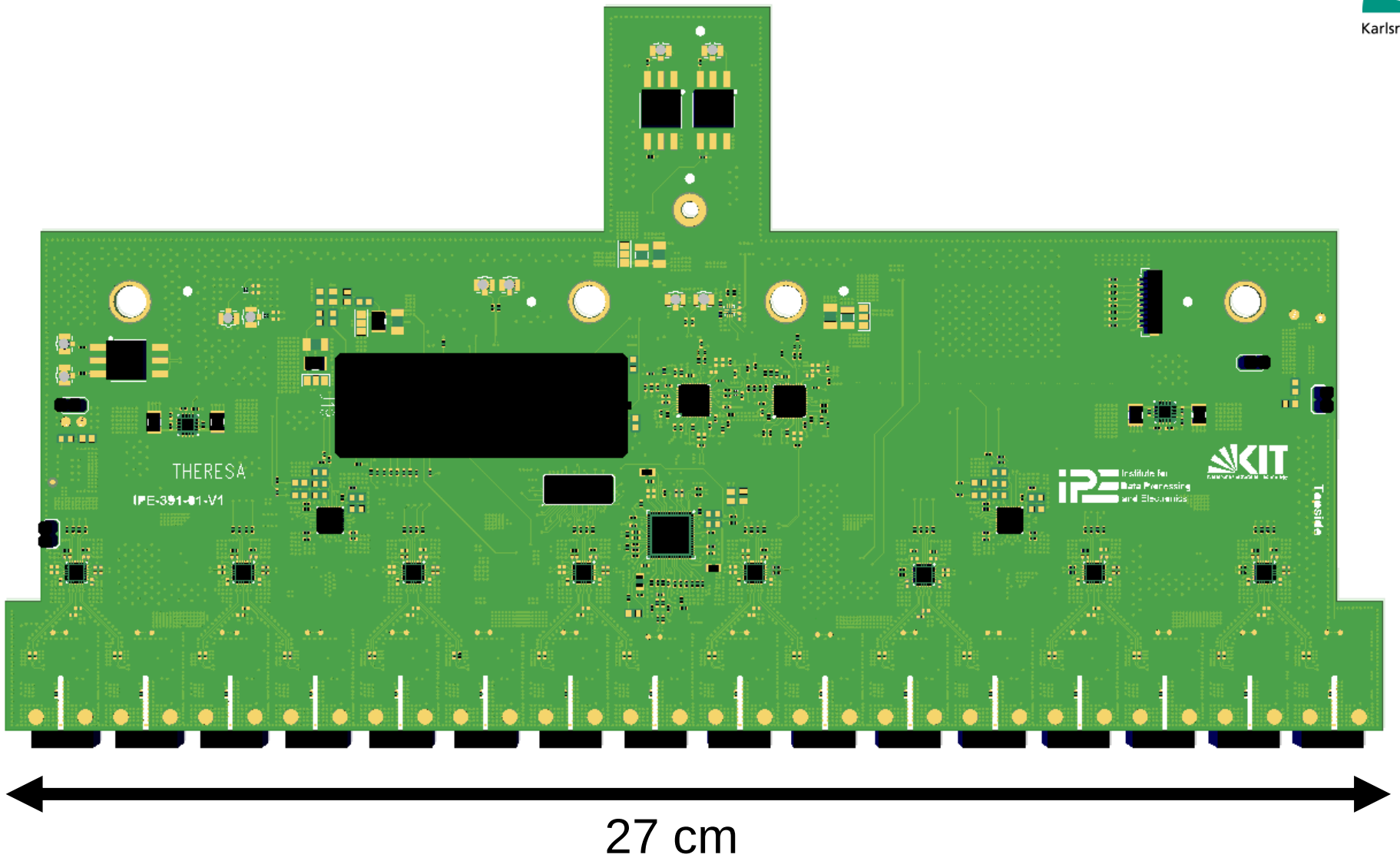
Separate analog from digital:

Digital part:

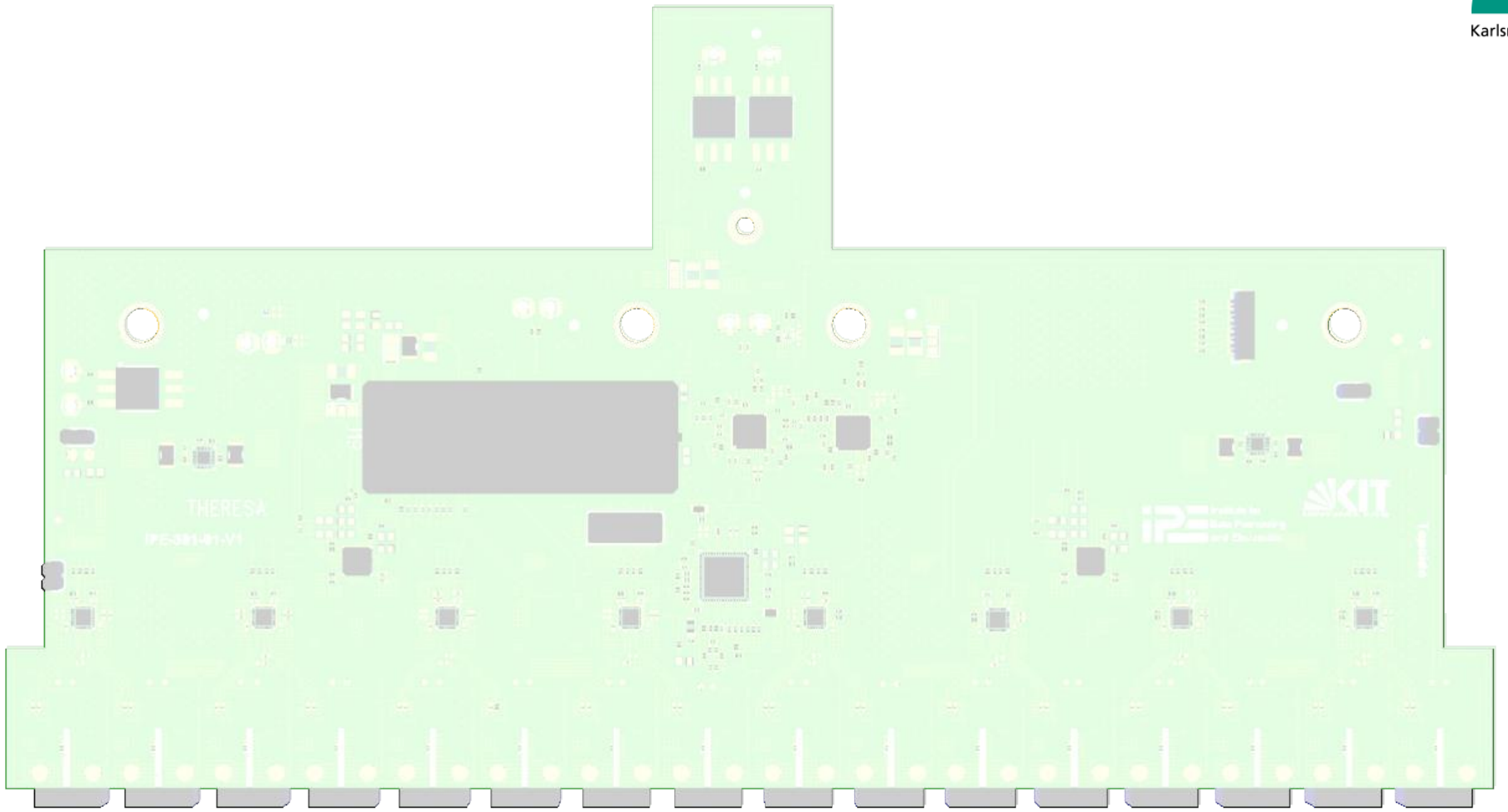
- Clocking distribution
- Delay chips
- Slow control lines

Analog part

Digital Component Placement (Top)

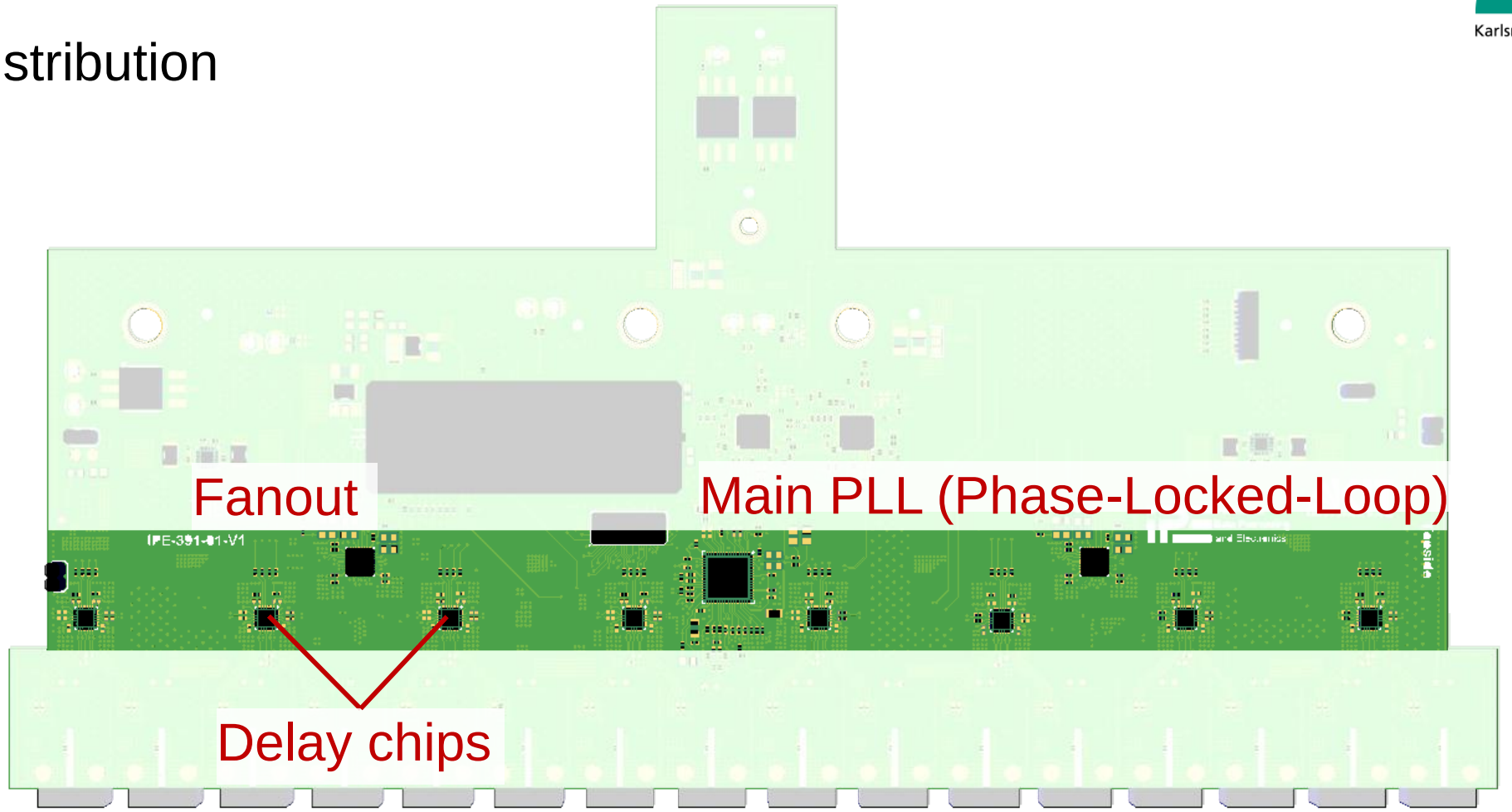


Digital Component Placement (Top)



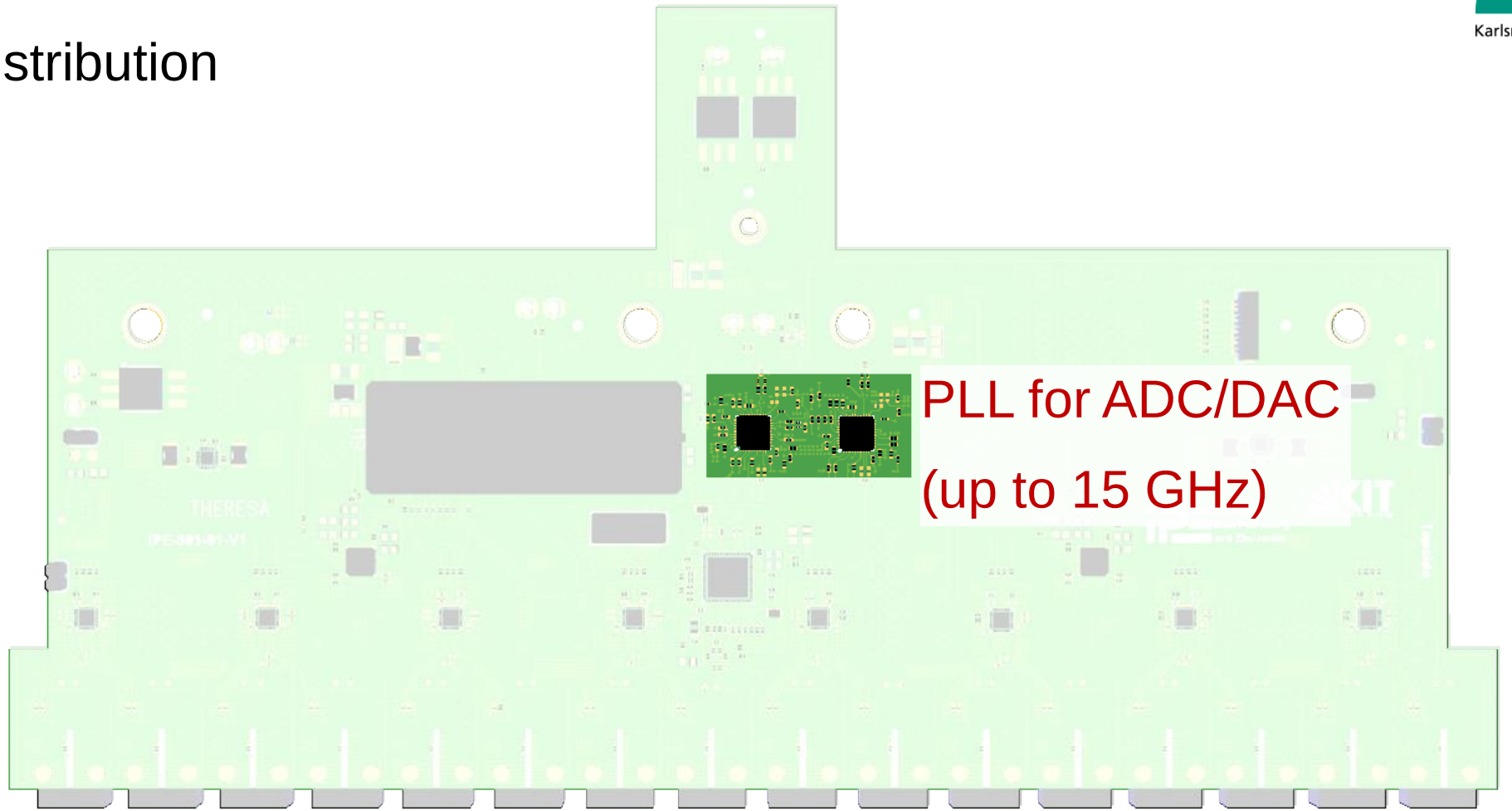
Digital Component Placement (Top)

Clock Distribution

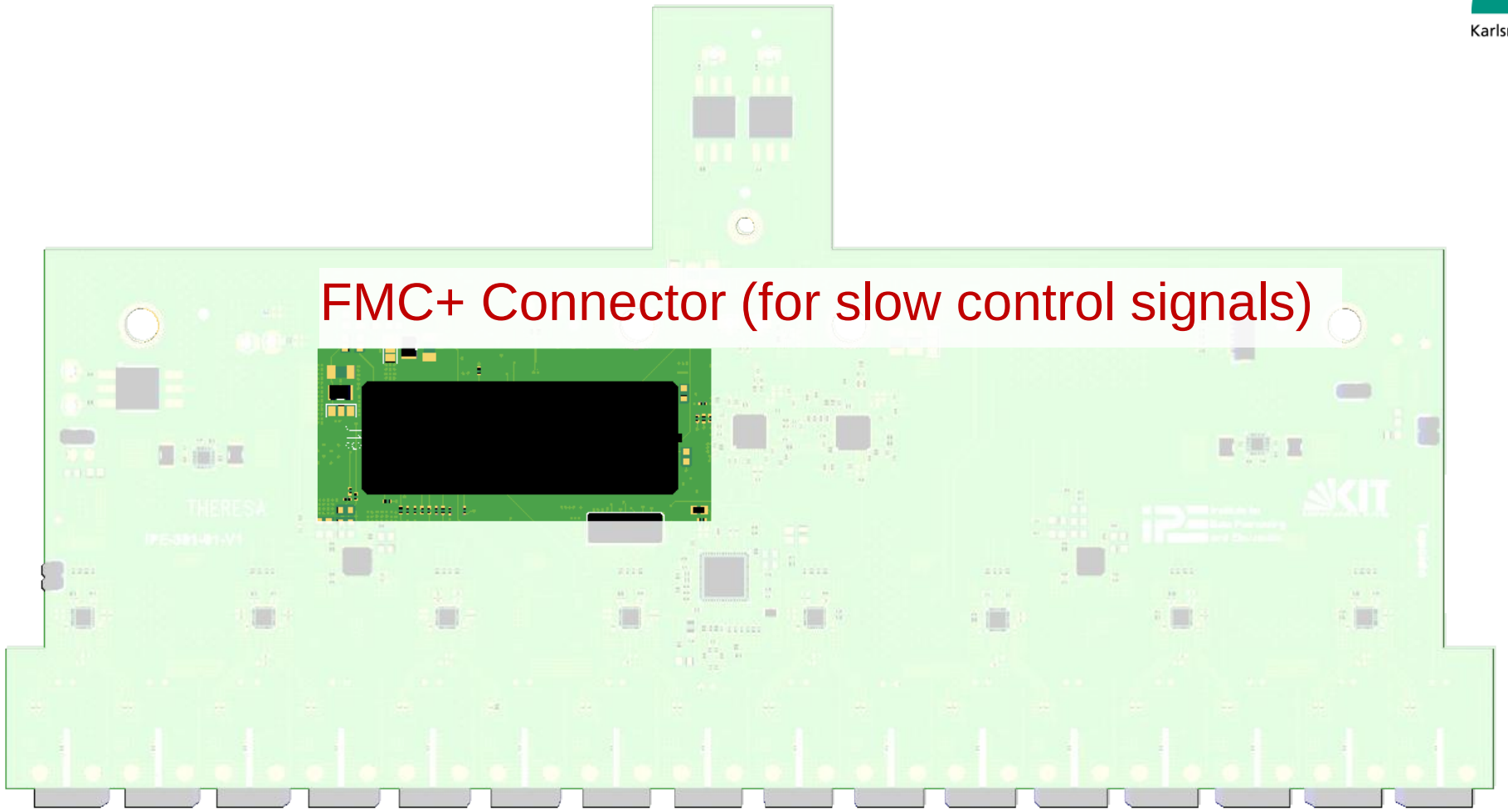


Digital Component Placement (Top)

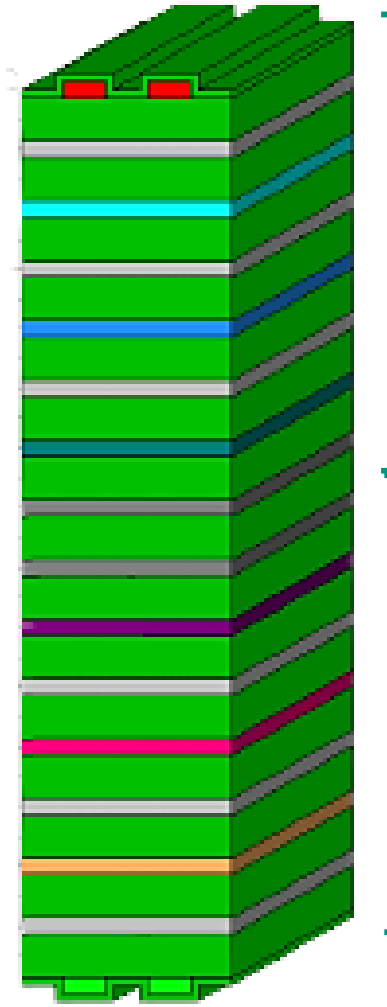
Clock Distribution



Digital Component Placement (Top)



PCB Design : Substrate & Metal Layer Stackup



Separate analog from digital:

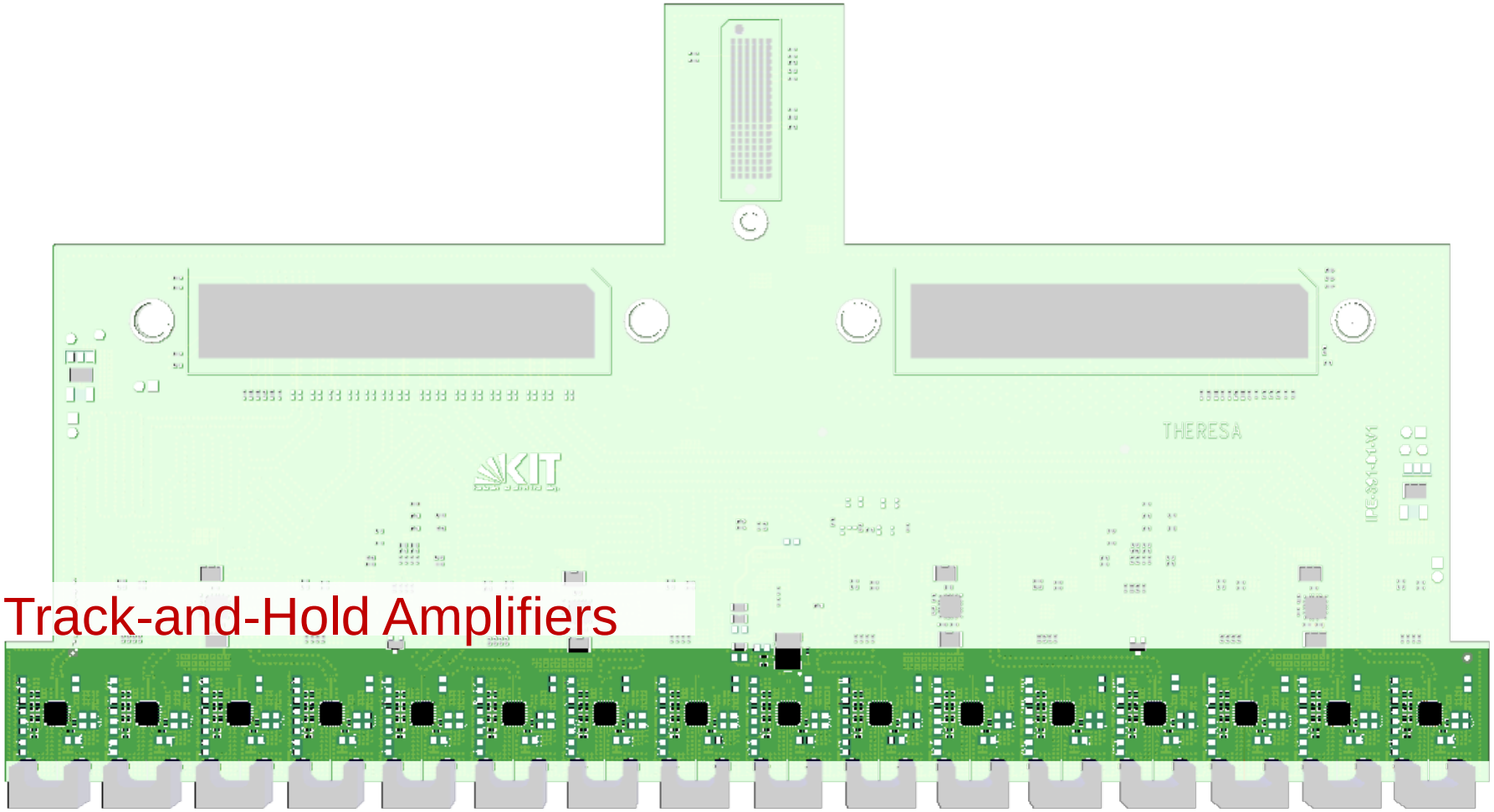
Digital part:

- Clocking distribution
- Delay chips
- Slow control lines

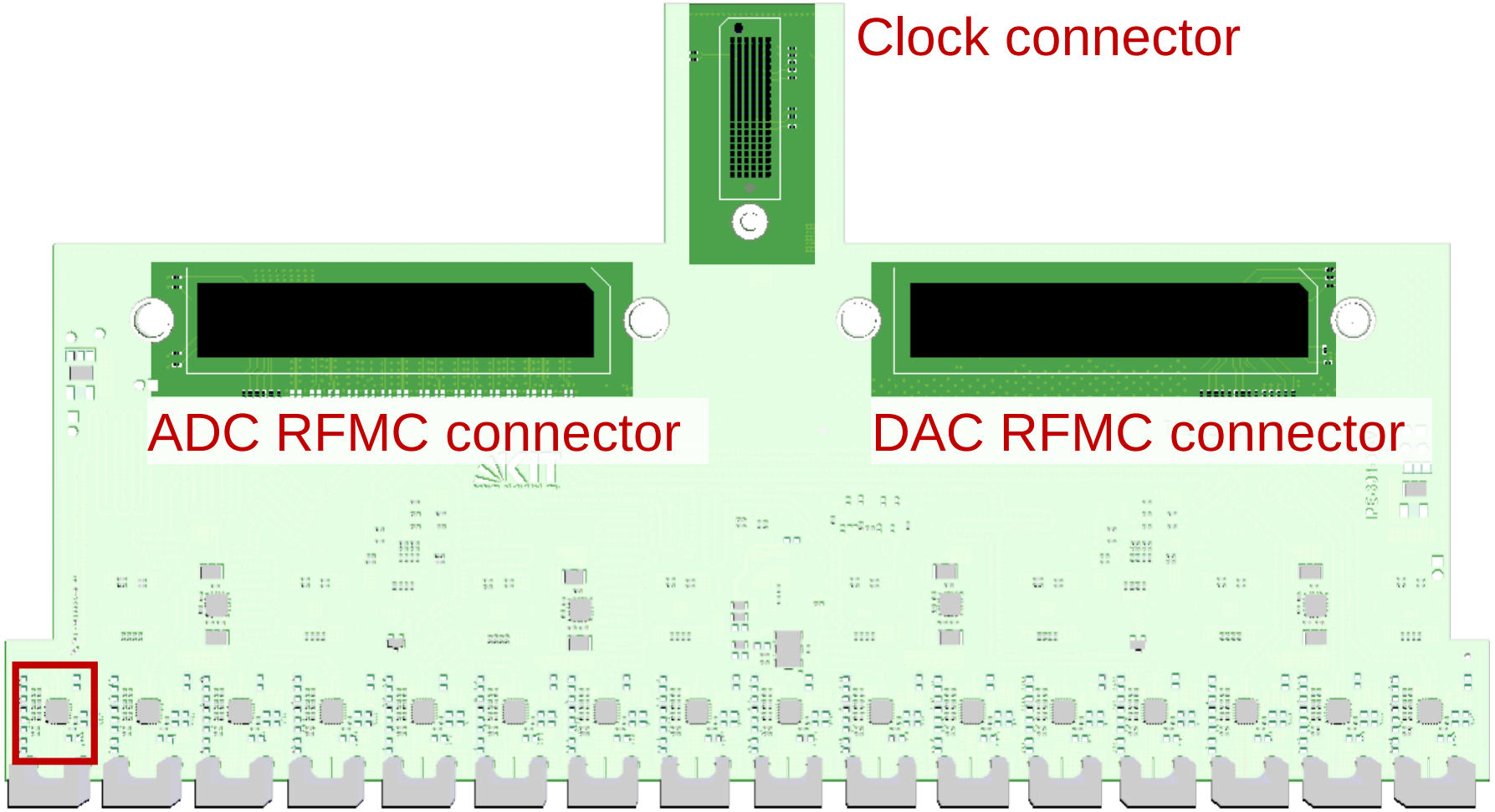
Analog part:

- Track-and-Hold amplifiers
- HF transmission lines
- Analog power supplies

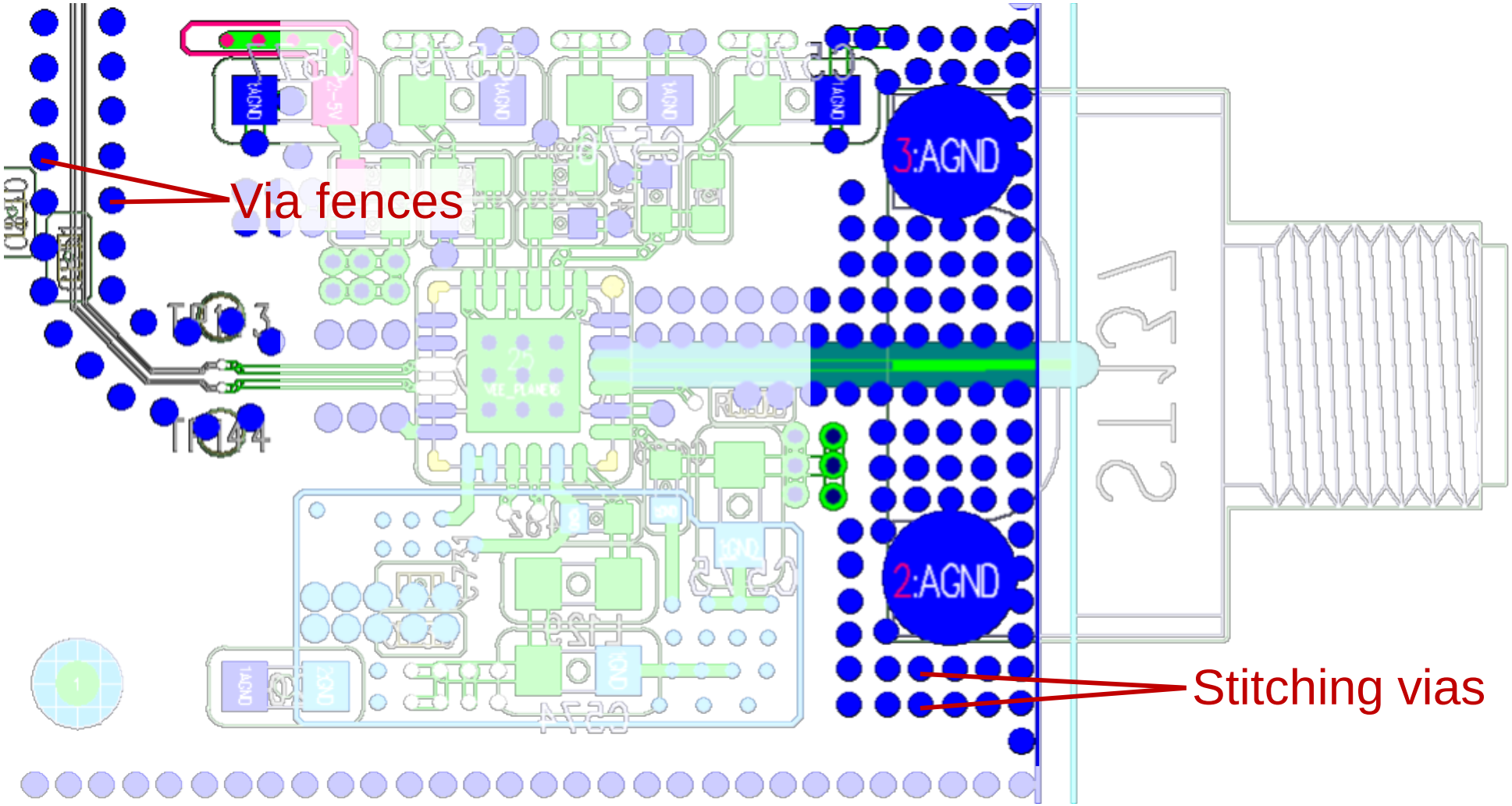
Analog Component Placement (Bottom)



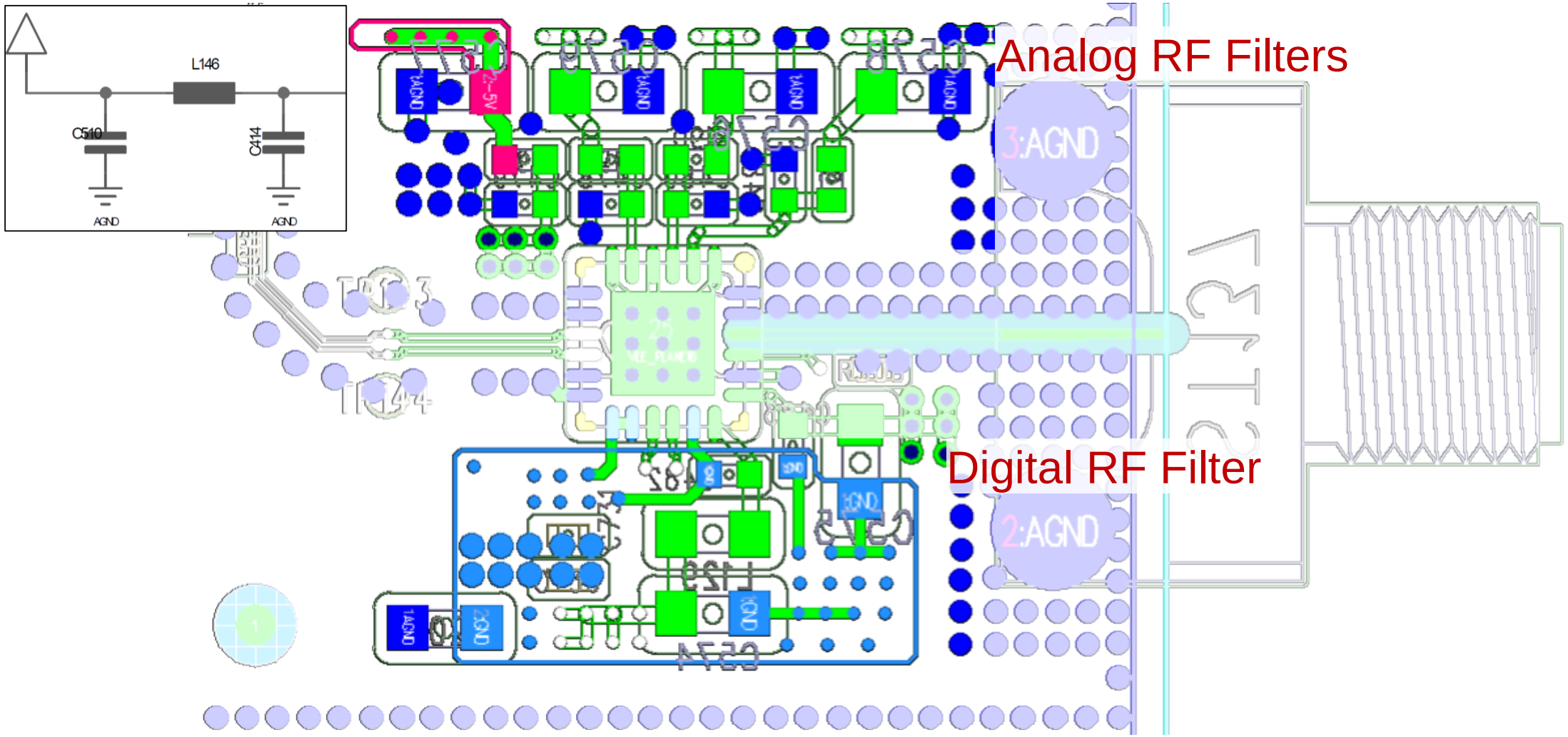
Analog Component Placement (Bottom)



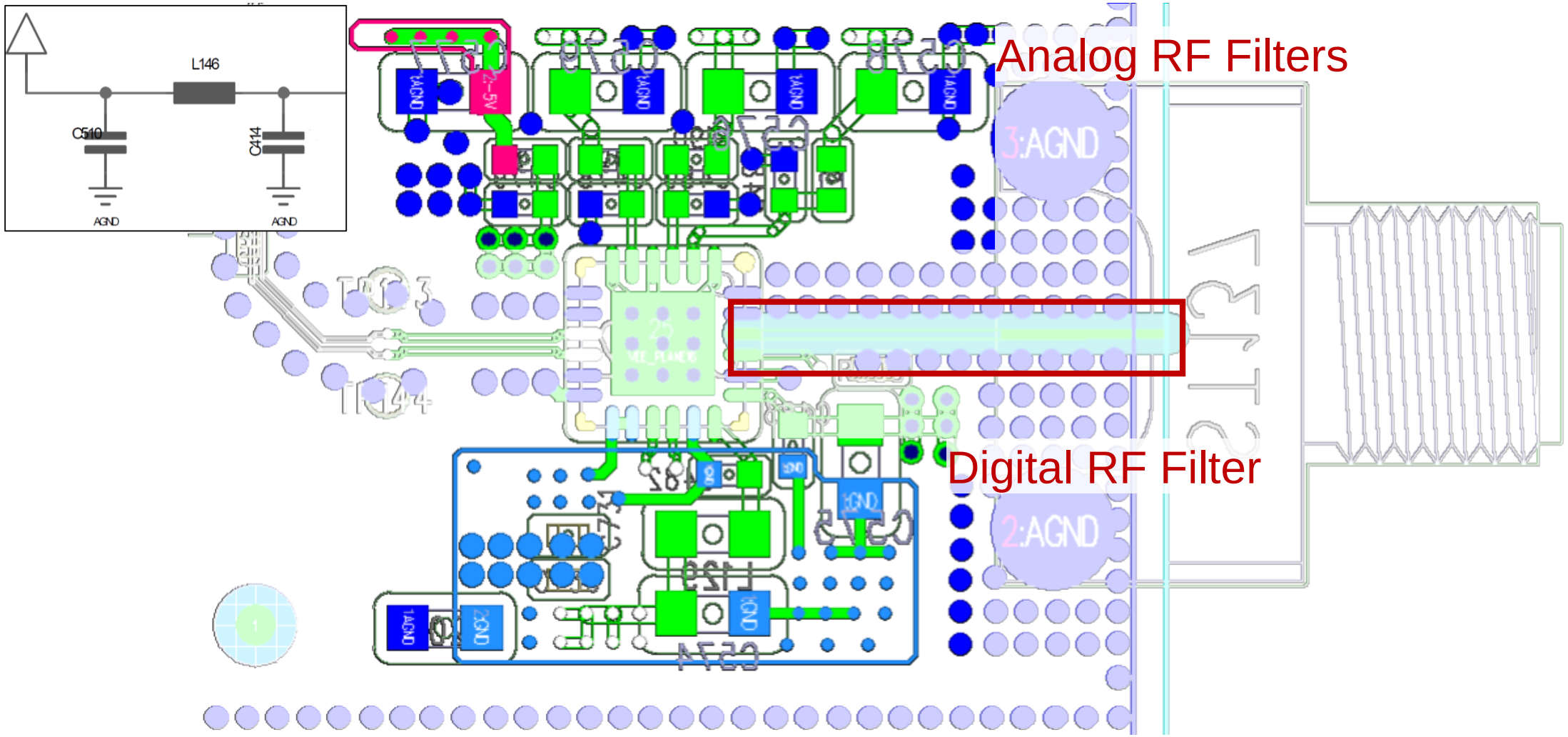
Design: Low Noise



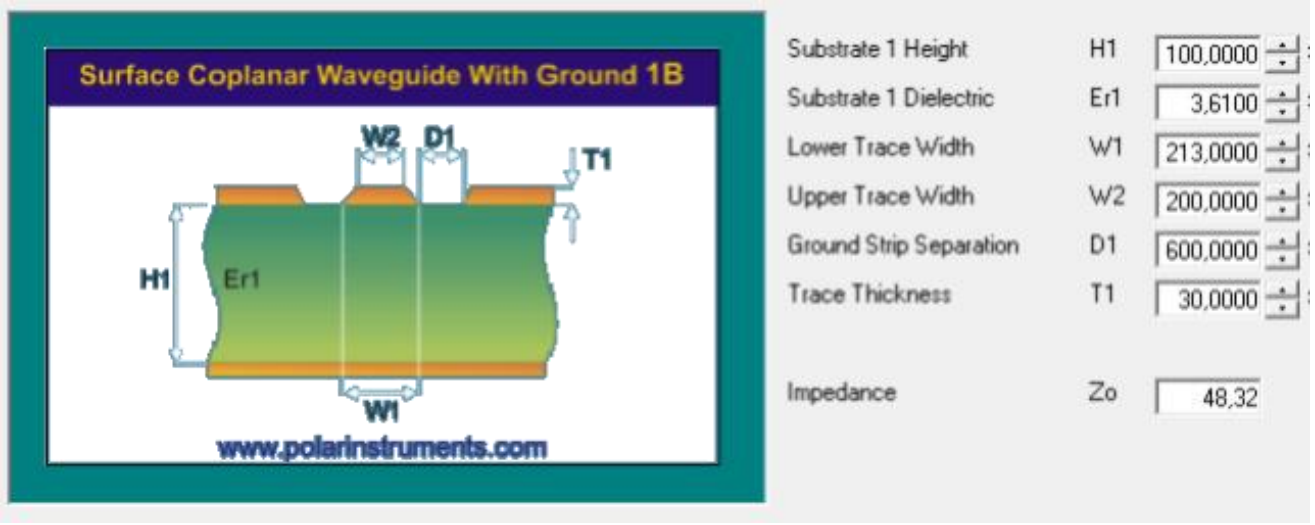
Design: Low Noise

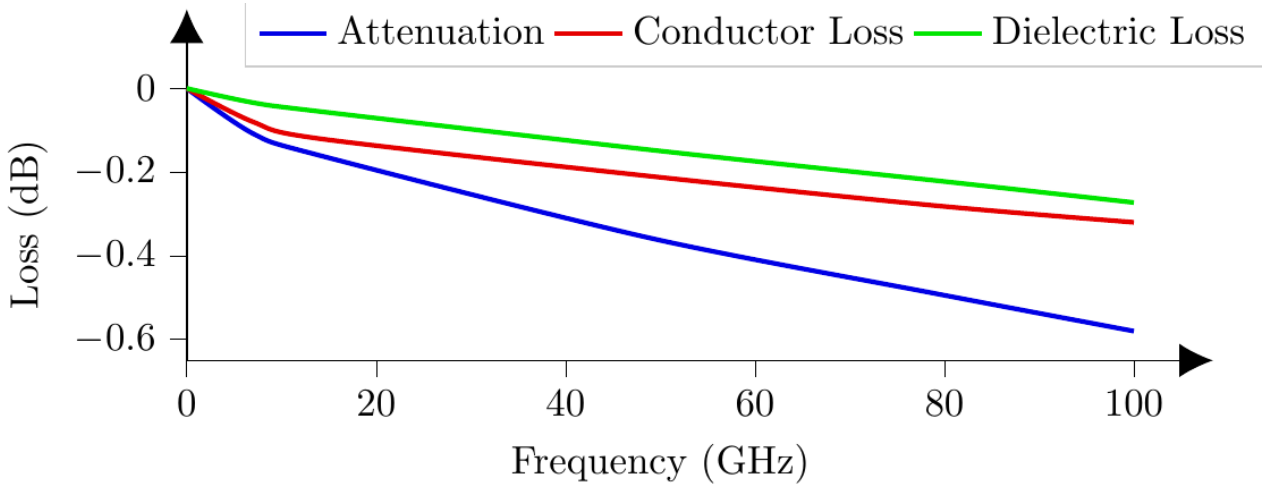


Design: Low Noise



Design: Transmission Lines





$$Z_0 = \frac{60.0\pi}{\sqrt{\epsilon_{\text{eff}}}} \frac{1.0}{\frac{K(k)}{K(k')} + \frac{K(k_1)}{K(k_1')}}$$

$$k = W1/(2D1 + W1)$$

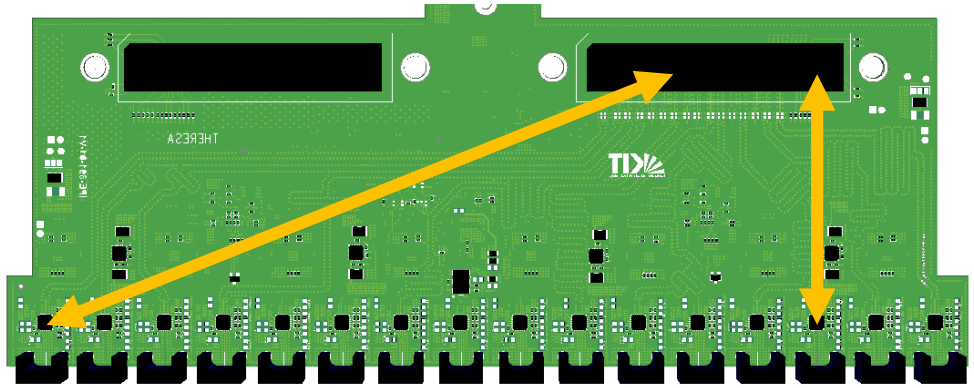
$$k' = \sqrt{1.0 - k^2}$$

$$k_1 = \frac{\tanh(\frac{\pi W1}{4.0H1})}{\tanh(\frac{\pi(2D1+W1)}{4.0H1})}$$

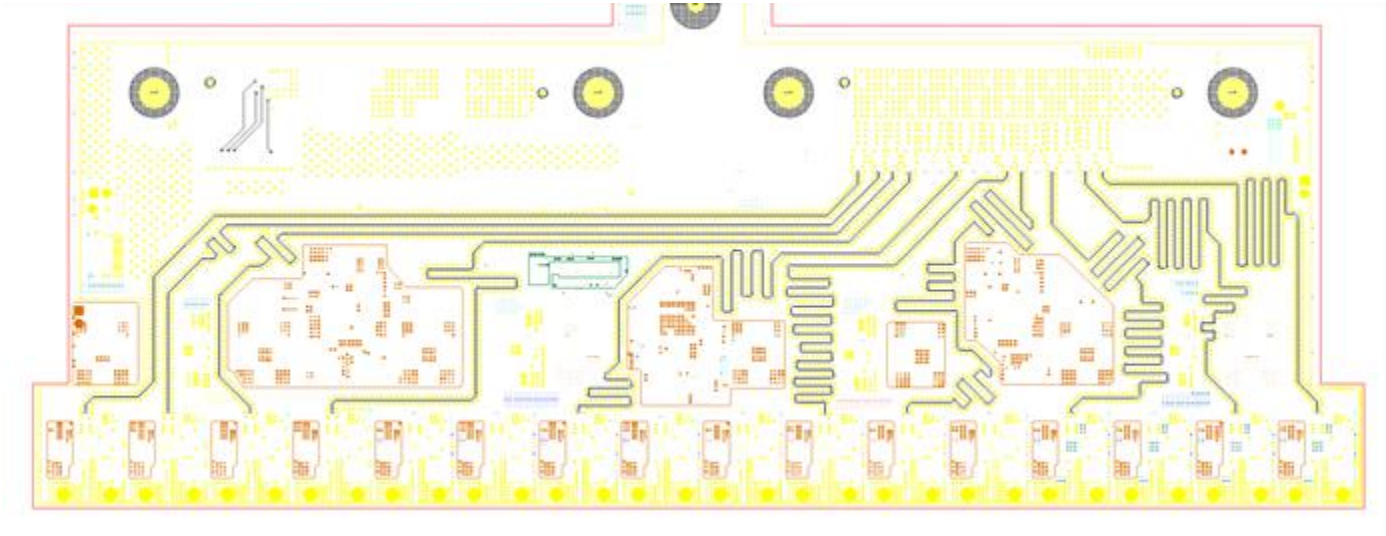
$$k_1' = \sqrt{1.0 - k_1^2}$$

$$\epsilon_{\text{eff}} = \frac{1.0 + \epsilon_r \frac{K(k')}{K(k)} \frac{K(k_1)}{K(k_1')}}{1.0 + \frac{K(k')}{K(k)} \frac{K(k_1)}{K(k_1')}}$$

Design: Time Skew

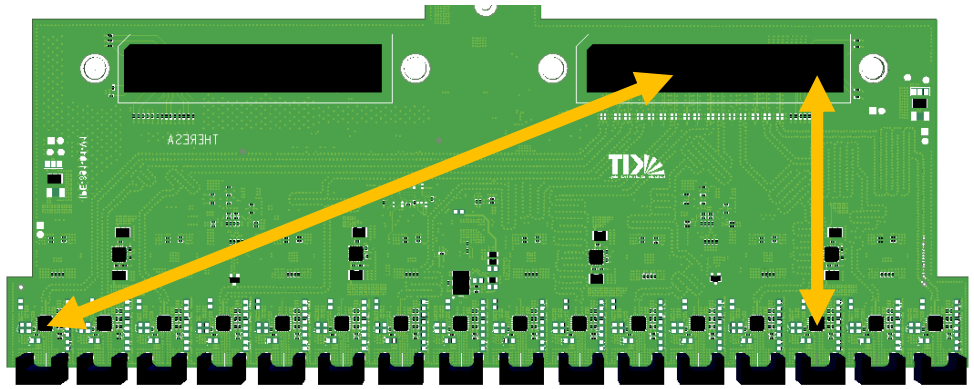


Signal path lengths differ between THA_3 and THA_{16}



RF traces from Track-and-Hold to RF-ADC via RF-connector

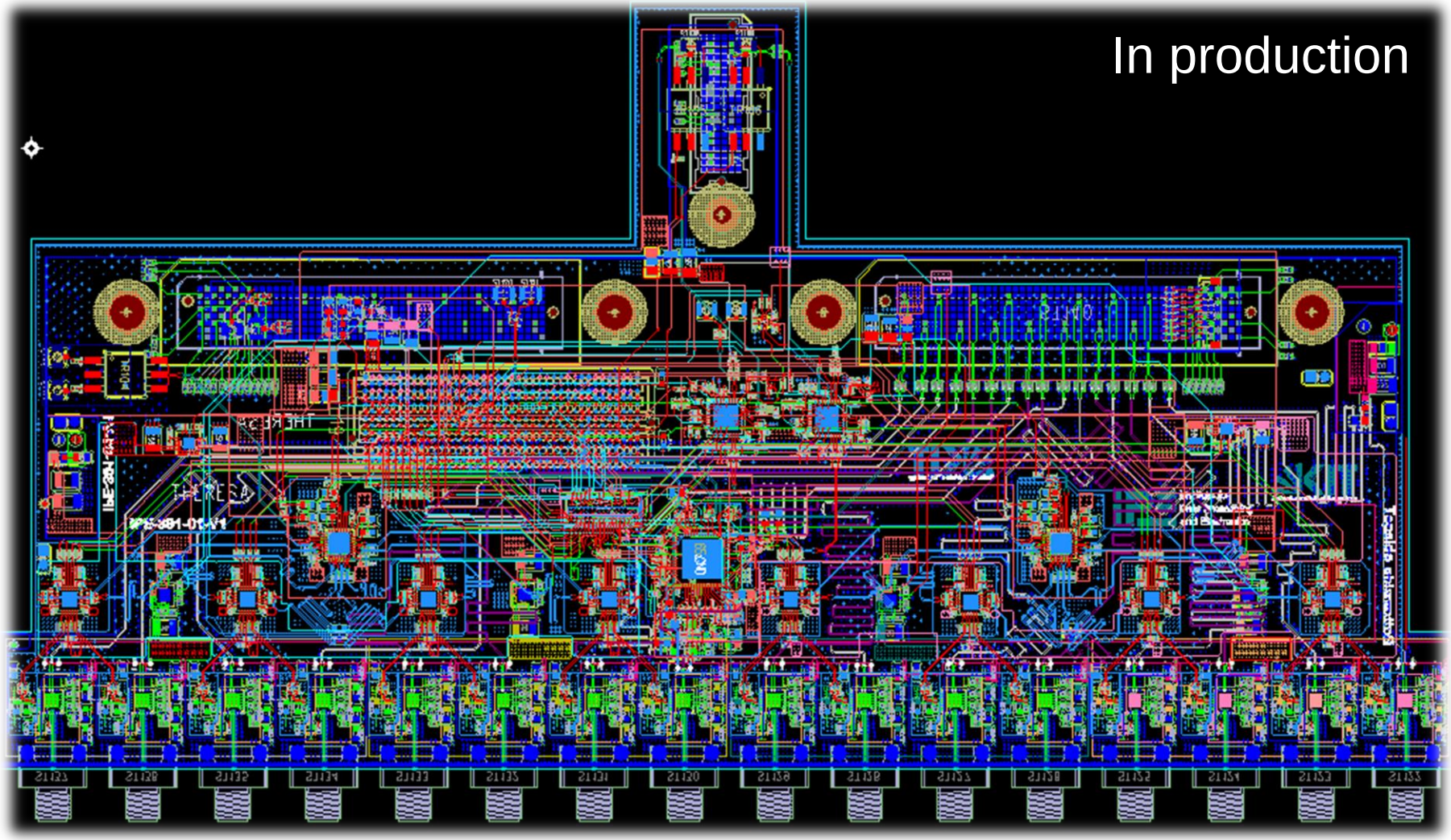
Design: Time Skew



Signal path lengths differ between THA_3 and THA_{16}

Name	Estimated length	Routed length	Tolerance
OUT_TH_1_P	197.35682	197.35682	1
OUT_TH_2_N	197.48659	197.48659	1
OUT_TH_2_P	197.58522	197.58522	1
OUT_TH_3_N	197.44362	197.44362	1
OUT_TH_3_P	197.42569	197.42569	1
OUT_TH_4_N	197.4959	197.4959	1
OUT_TH_4_P	197.49939	197.49939	1

Final PCB Layout



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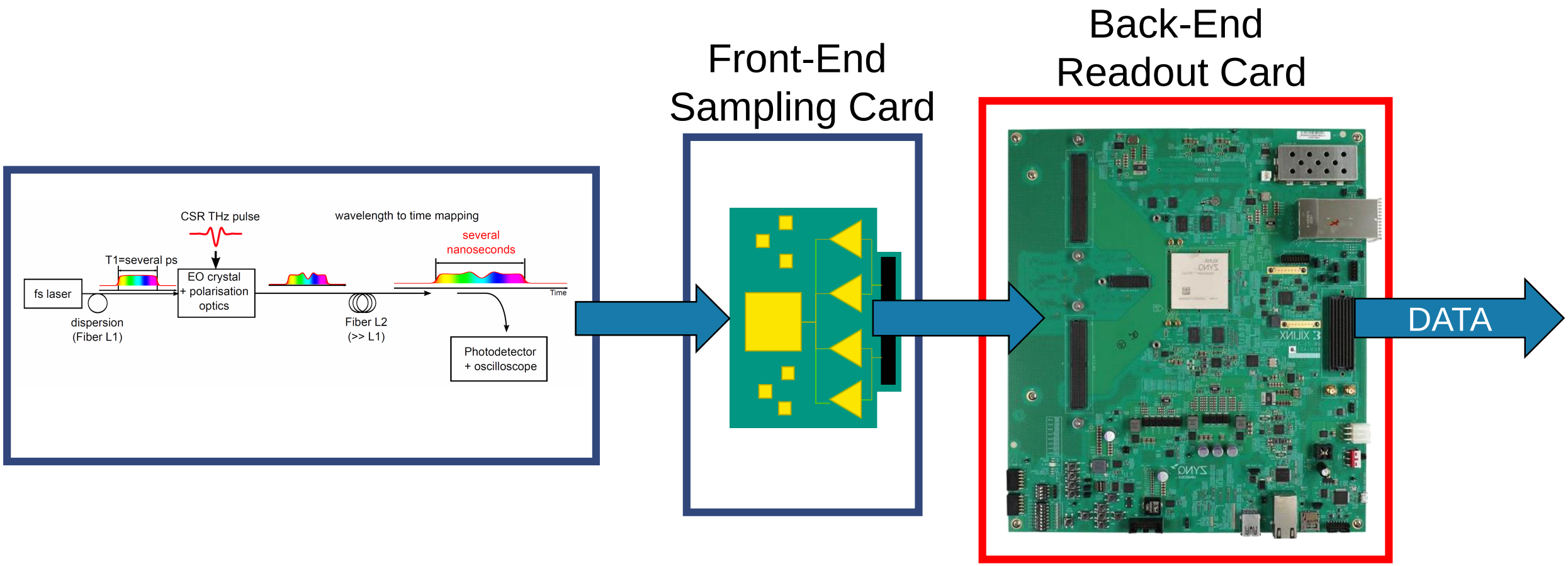
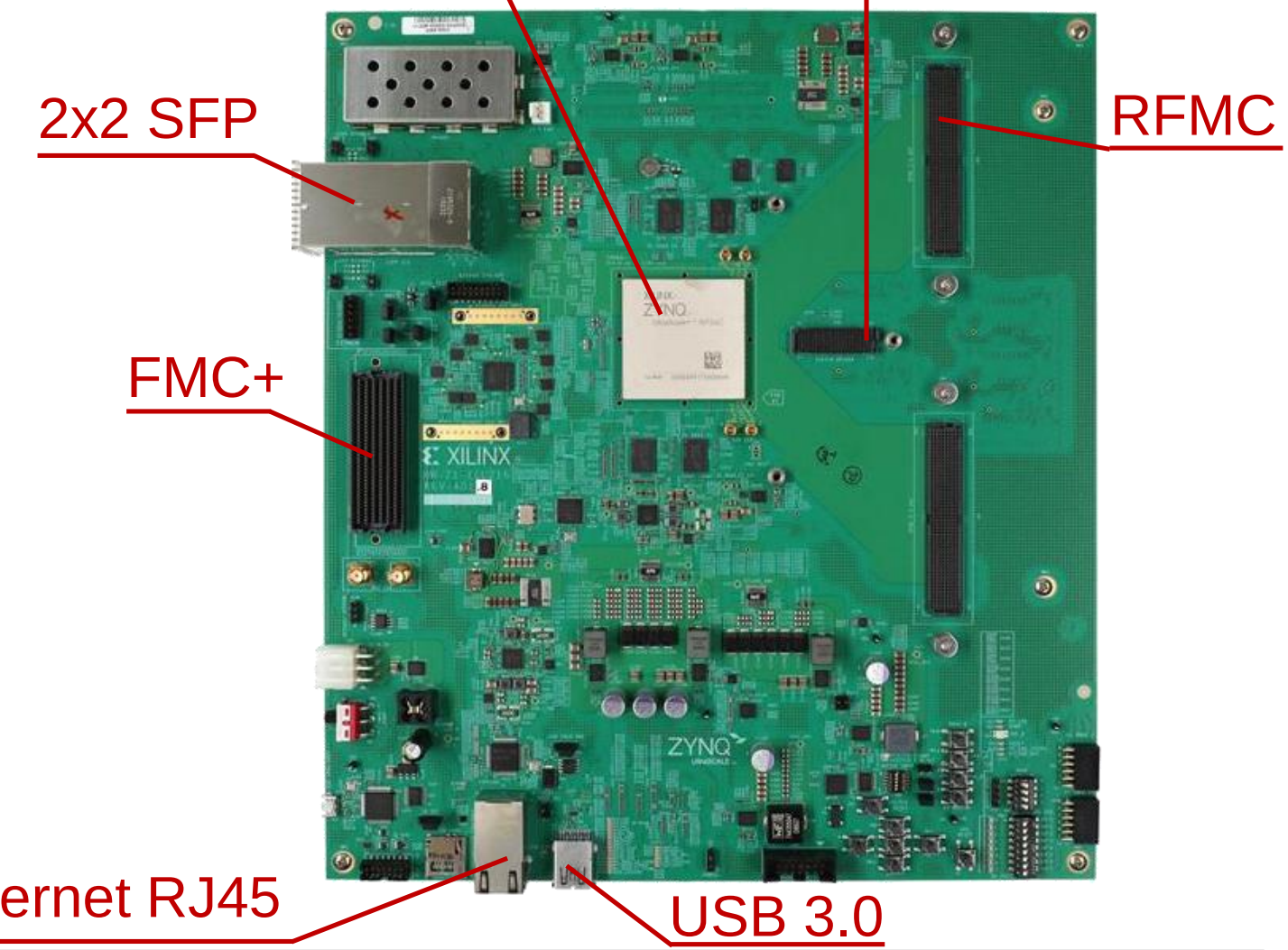
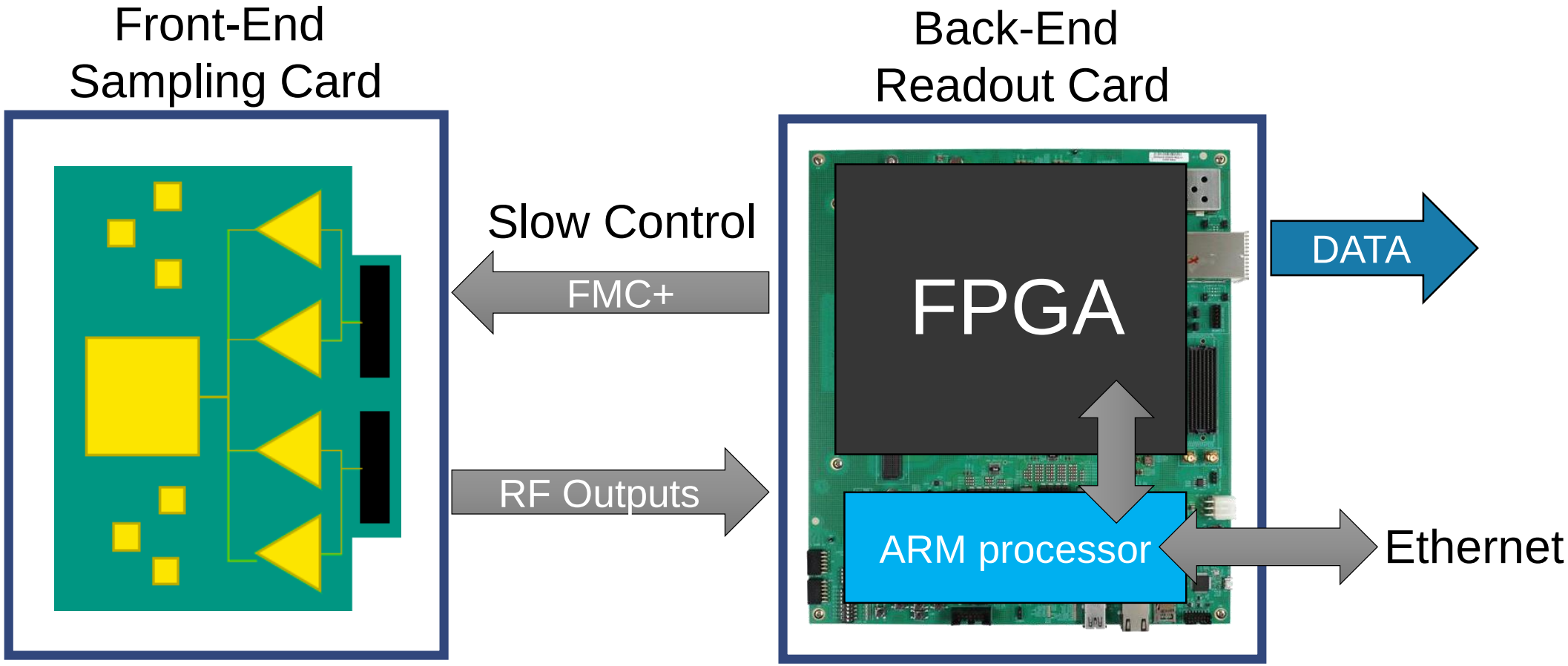


Back-End Readout Card

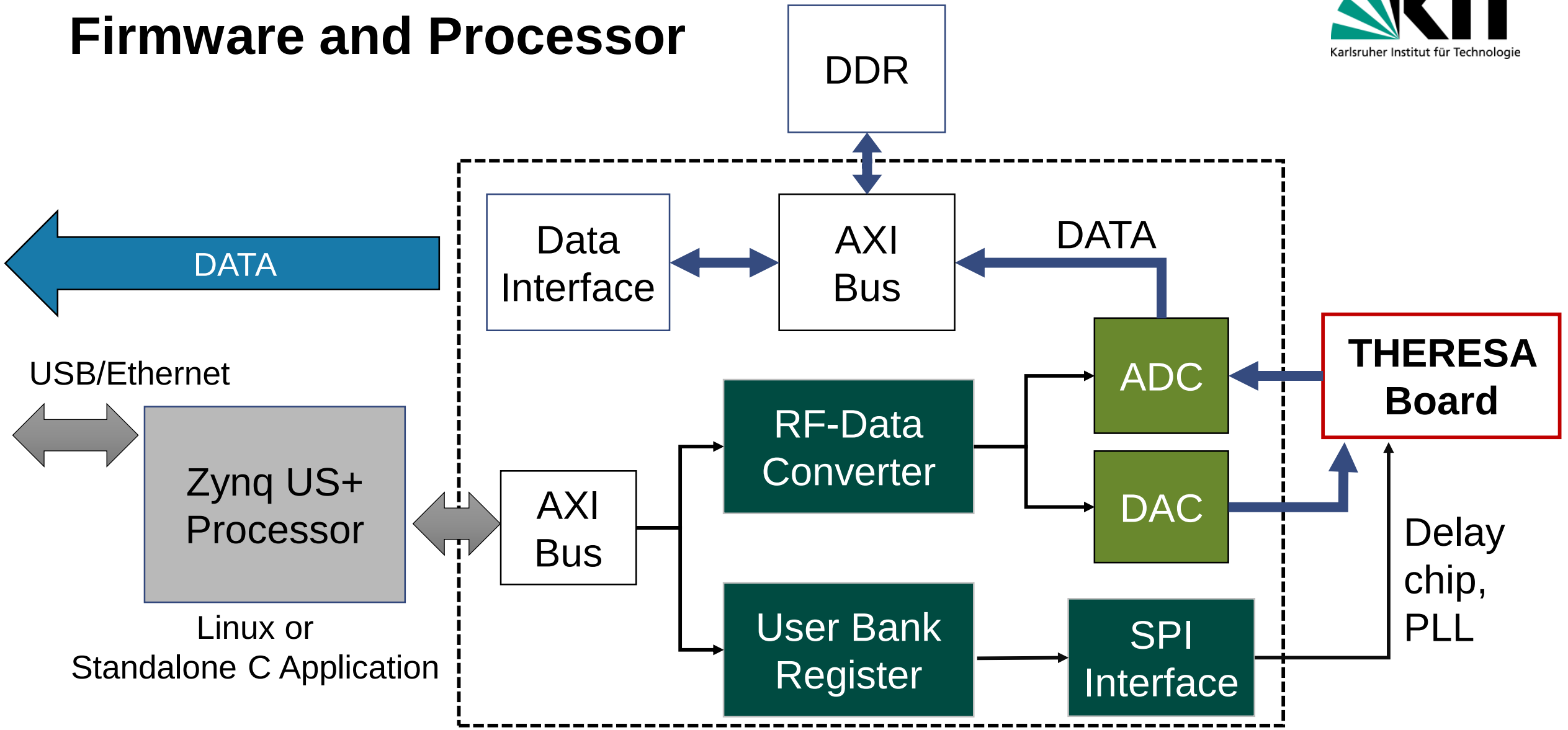
- Xilinx Evaluation Card (ZCU216)
- Zynq UltraScale+ RF-SoC
  - ARM CPU
  - FPGA
- 14-bit, 2.5 GSPS RF-ADC (16x)
- 14-bit, 10 GSPS RF-DAC (16x)
- 112 Gbps optical connections



Firmware and Integration with ARM Processor

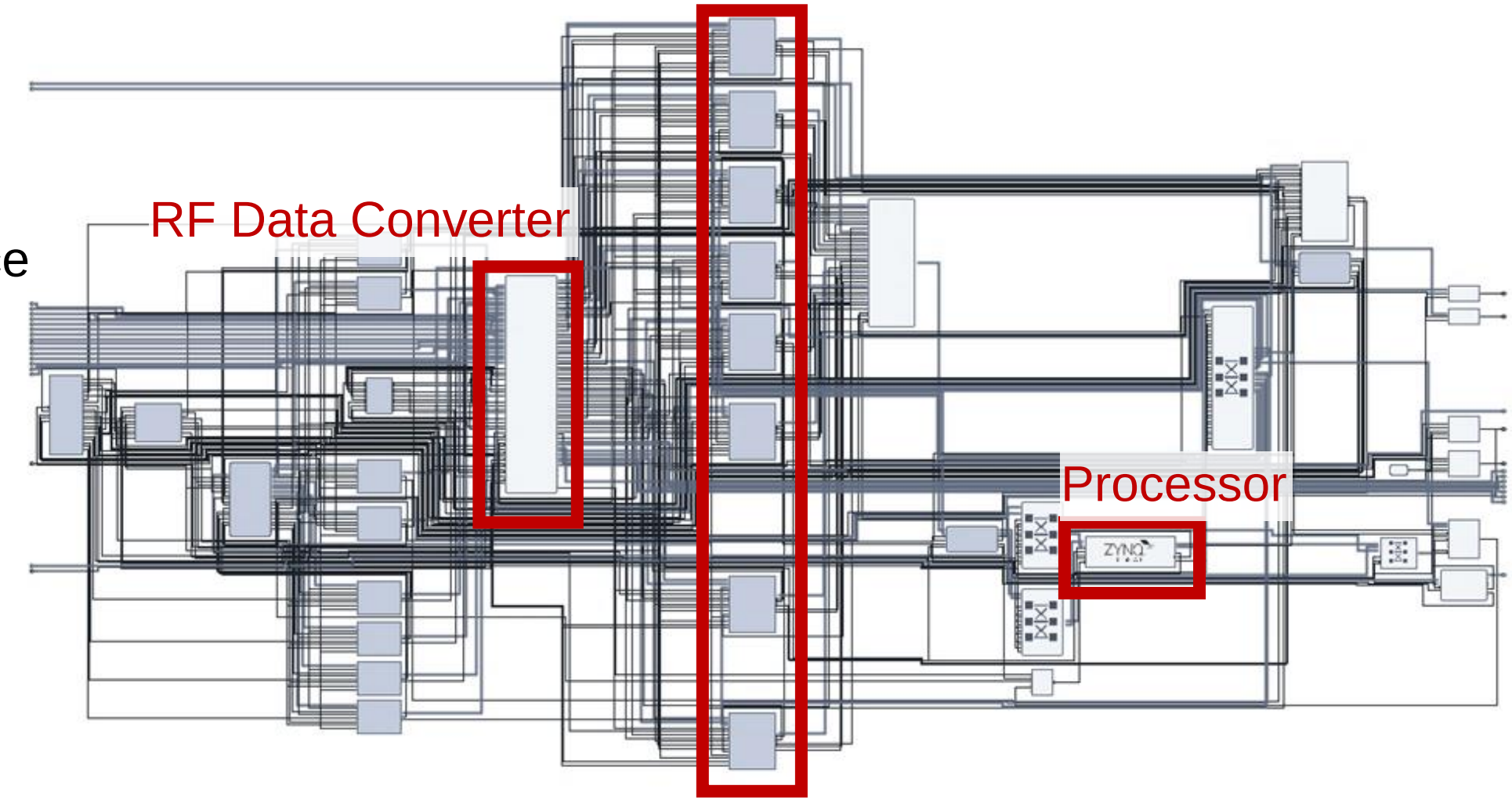


Firmware and Processor



Xilinx Firmware

Interface



Results

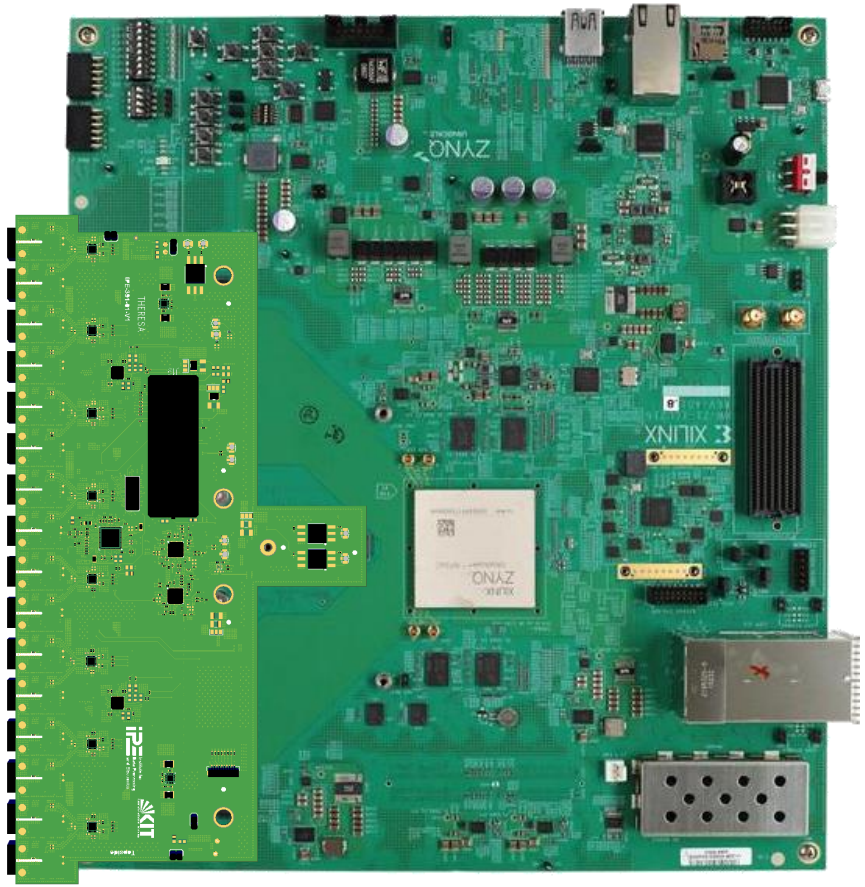
- Front-end sampling card successfully designed
- Currently under production (ETA mid-Sept. 2021)
- Continuous sampling up to 40 GS/s
- Evaluation of a novel readout RF-SoC system + Xilinx Design Tool (Vitis)
- Firmware and slow-control developed

Conclusions & Outlook

- THERESA is suitable for several applications at KARA
- DAQ infrastructure and firmware suitable for next generation of beam diagnostics instrumentations
- Selected FPGA is compatible with AI (i.e. Reinforcement-Learning) and interfacing with the BBB-feedback at KARA

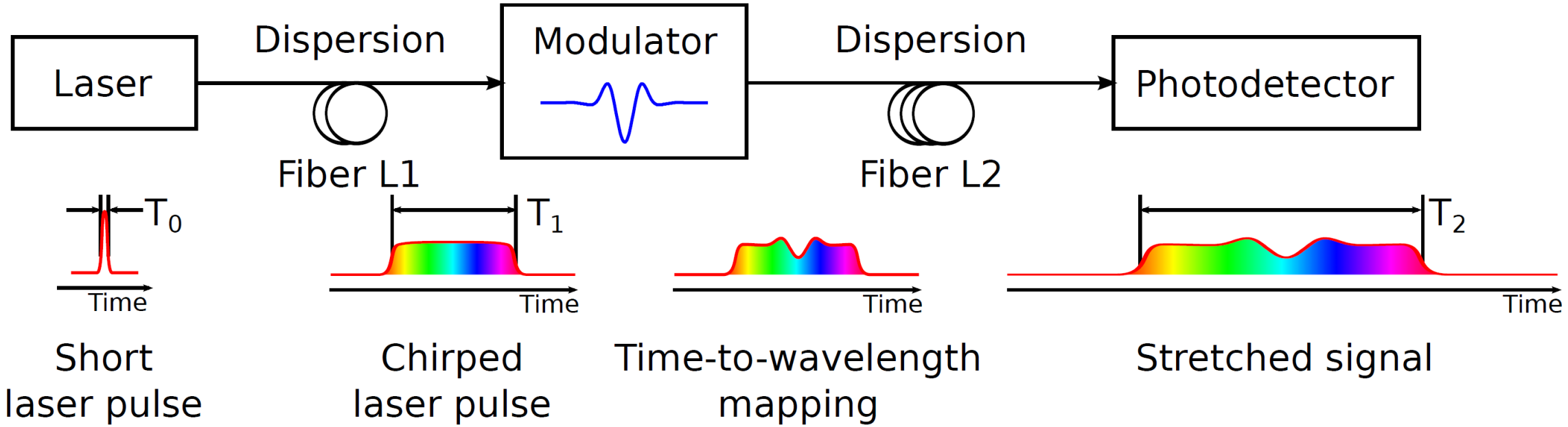
- Characterization & integration with optical time-stretch setup in collaboration with Lille University
- Final commissioning at KARA

Thank you for your attention!



BACKUP

Photonic Time-Stretch Method



$T_2 = M \cdot T_1$

$M = 1 + L2/L1$

Example: L1 = 10m, L2 = 2km → M=200

T_1 = 1 ps ≙ 1 THz → T_2 = 200 ps ≙ 5 GHz

PhD thesis, Eléonore Roussel, Lille University

Table 117: **RF-ADC Electrical Characteristics for ZU4xDR Devices**

Parameter	Comments/Conditions[1]	Min	Typ[2]	Max	Units
Analog inputs					
Resolution		14	–	–	Bits
Sample Rate	Devices using quad ADC tile channel	0.5	–	2.5	GS/s
	Devices using dual ADC tile channel	1	–	5	GS/s
Full-scale input	Input 100Ω on-die termination when DSA attenuation = 0 dB	–	1	–	V_{PPD}
		–	1	–	dBm
Maximum allowed input power	Input 100Ω on-die termination when DSA attenuation ≥ 15 dB	–	4.8	–	V_{PPD}
		–	14.6	–	dBm
Digital Attenuation Range		0	–	27	dB
Attenuator step size		–	1	–	dB
Auto attenuation	Automatically set when amplitude over-voltage is asserted	–	15	–	dB
Analog input bandwidth	Full-power bandwidth (–3 dB)	–	6	–	GHz
Return loss (R_L)[3]	Up to 4 GHz	–	–12	–	dB
	Up to 6 GHz	–	–10	–	dB
Optimized common mode voltage range	Performance optimized range. AC and DC coupling modes[4]	0.68	0.7	0.72	V
Maximum common mode voltage range	Available range before triggering over-voltage protection. AC and DC coupling modes[4]	0.4	0.7	1	V
Crosstalk isolation between channels[5]	F_{IN} = 0–4 GHz	–	–75	–	dBc
	F_{IN} = 0–6 GHz	–	–70	–	dBc

SFDR	Spurious free dynamic range excluding second- and third-order harmonic distortion, and including OIS and GTIS spurs.	F_{IN} = 240 MHz	72.0	84.0	–	82.0	dBc
		F_{IN} = 1.9 GHz	–	83.0	–	81.0	dBc
		F_{IN} = 2.4 GHz	–	82.0	–	80.0	dBc
		F_{IN} = 3.5 GHz	72.0	80.0	–	79.0	dBc
		F_{IN} = 3.5 GHz, CW at –10 dBFS	64.0	77.0	–	74.0	dBc
		F_{IN} = 3.5 GHz, CW at –20 dBFS	–	66.0	–	65.0	dBc
		F_{IN} = 4.9 GHz	67.0	77.0	–	76.0	dBc
		F_{IN} = 4.9 GHz, CW at –10 dBFS	66.0	75.0	–	74.0	dBc
		F_{IN} = 4.9 GHz, CW at –20 dBFS	–	66.0	–	65.0	dBc
		F_{IN} = 5.9 GHz	66.0	75.0	–	75.0	dBc
		F_{IN} = 5.9 GHz, CW at –10 dBFS	65.0	74.0	–	73.0	dBc
		F_{IN} = 5.9 GHz, CW at –20 dBFS	–	66.0	–	65.0	dBc

HMC5640BLC4B

DC - 18 GHz ULTRA-WIDEBAND, 4 GS/s TRACK-AND-HOLD AMPLIFIER

Features

18 GHz Input bandwidth (1 Vp-p Full Scale)

4 GS/s Maximum Sampling Rate

68 dB SFDR (4 GHz / 0.5 Vp-p Input, CLK = 1 GS/s)

57 dB SFDR (4 GHz / 1 Vp-p Input, CLK = 1 GS/s)

Direct-Coupled I/O

Ultra-Clean Output Waveforms, Minimal Glitching

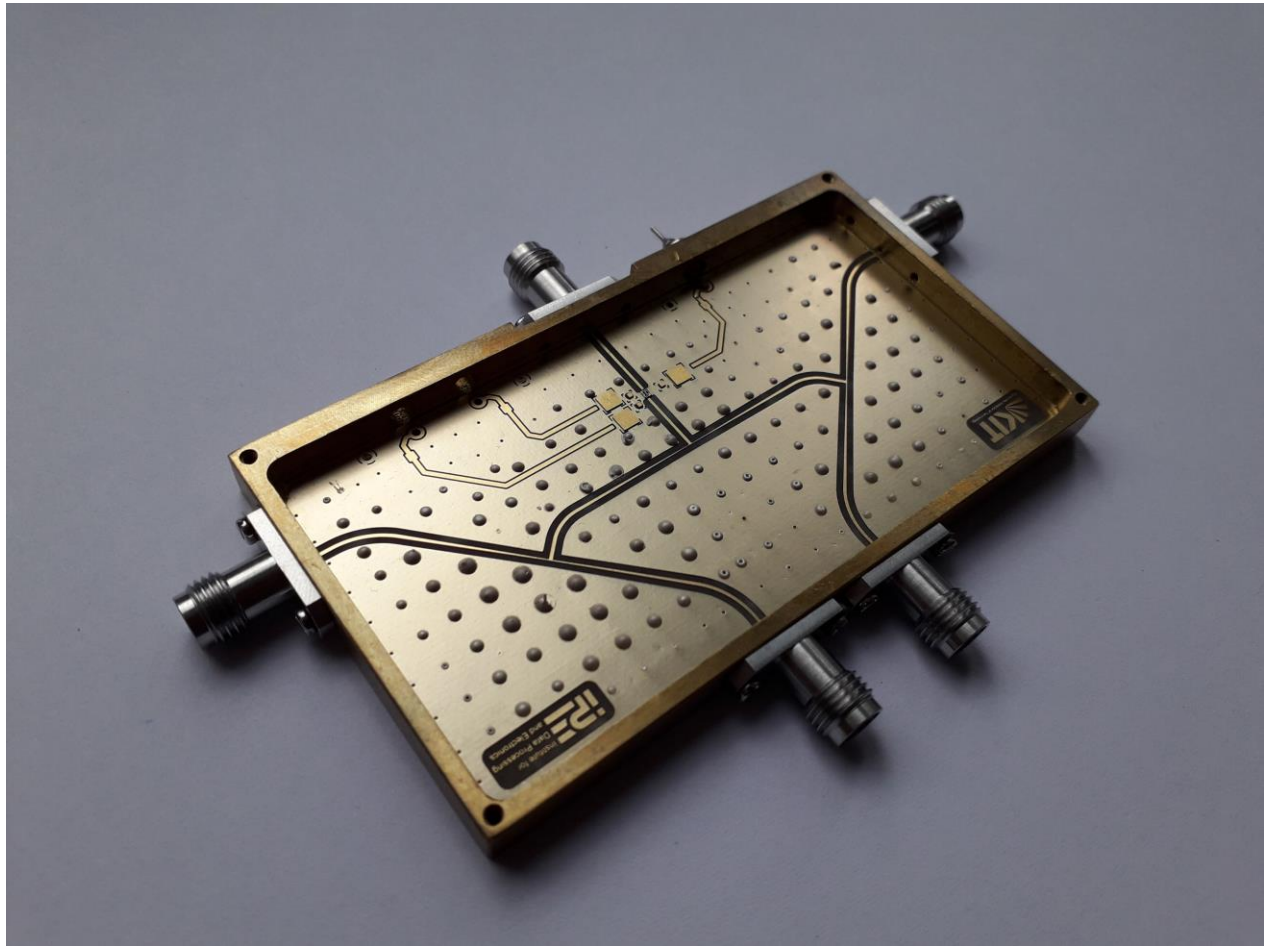
>60 dB Hold Mode Feedthrough Rejection

1.05 mV RMS Hold Mode Output Noise

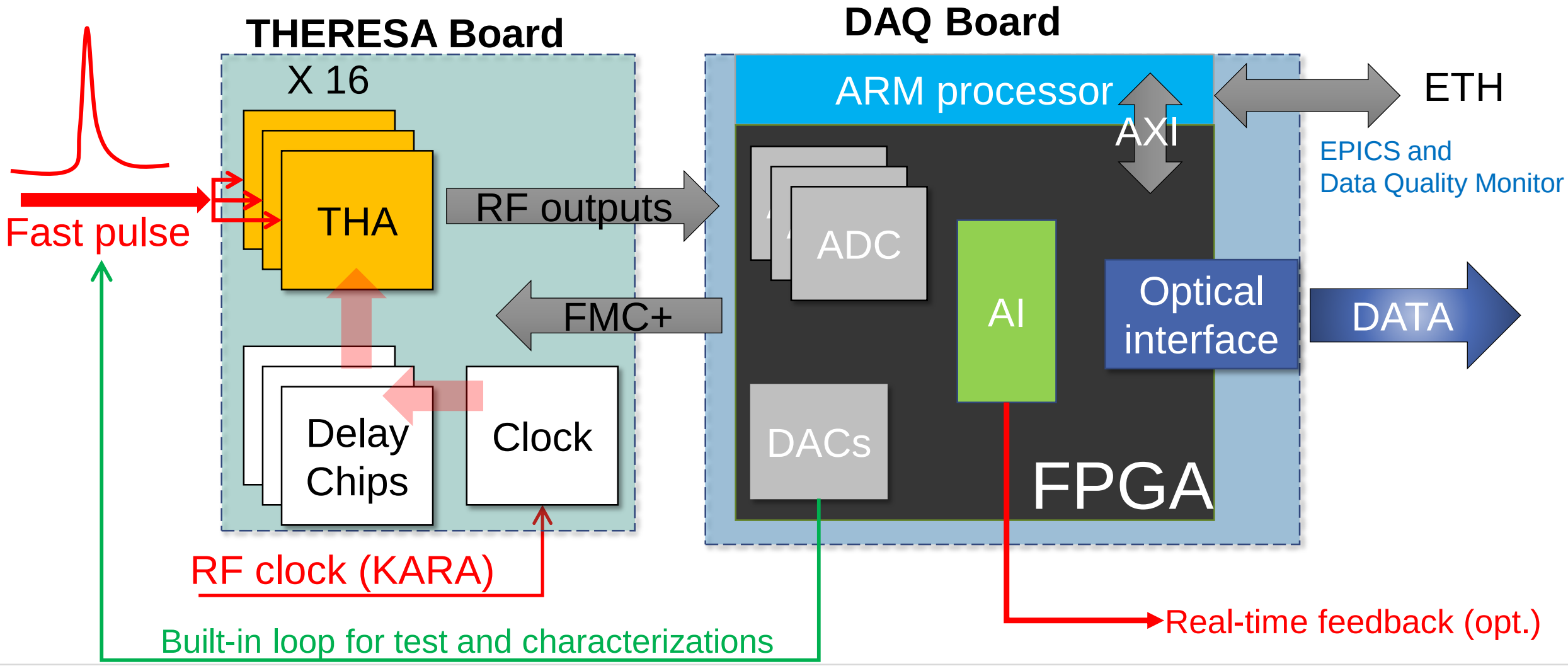
Single / Dual Rank Evaluation Boards are Available

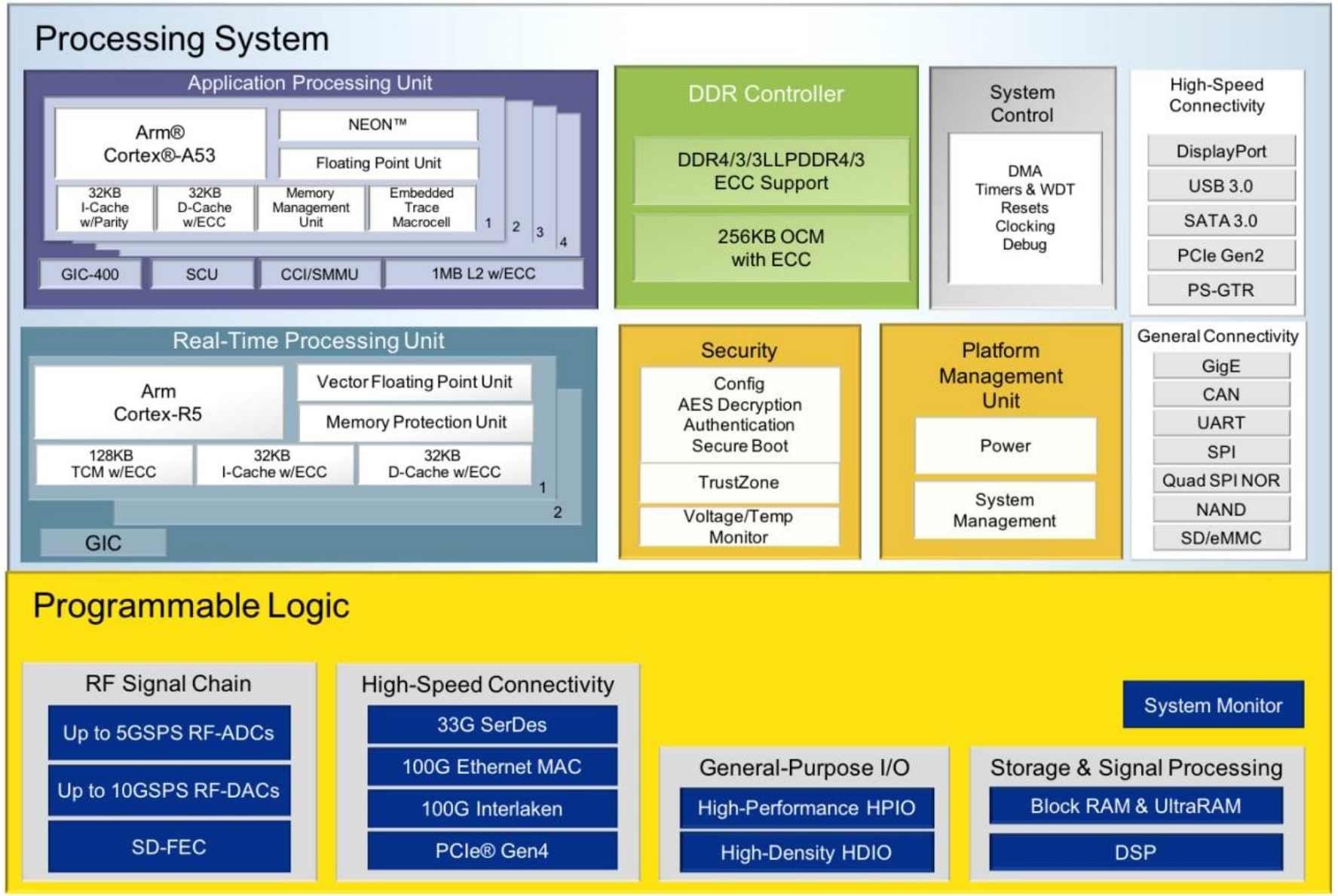
RoHS Compliant 4x4 mm SMT Package

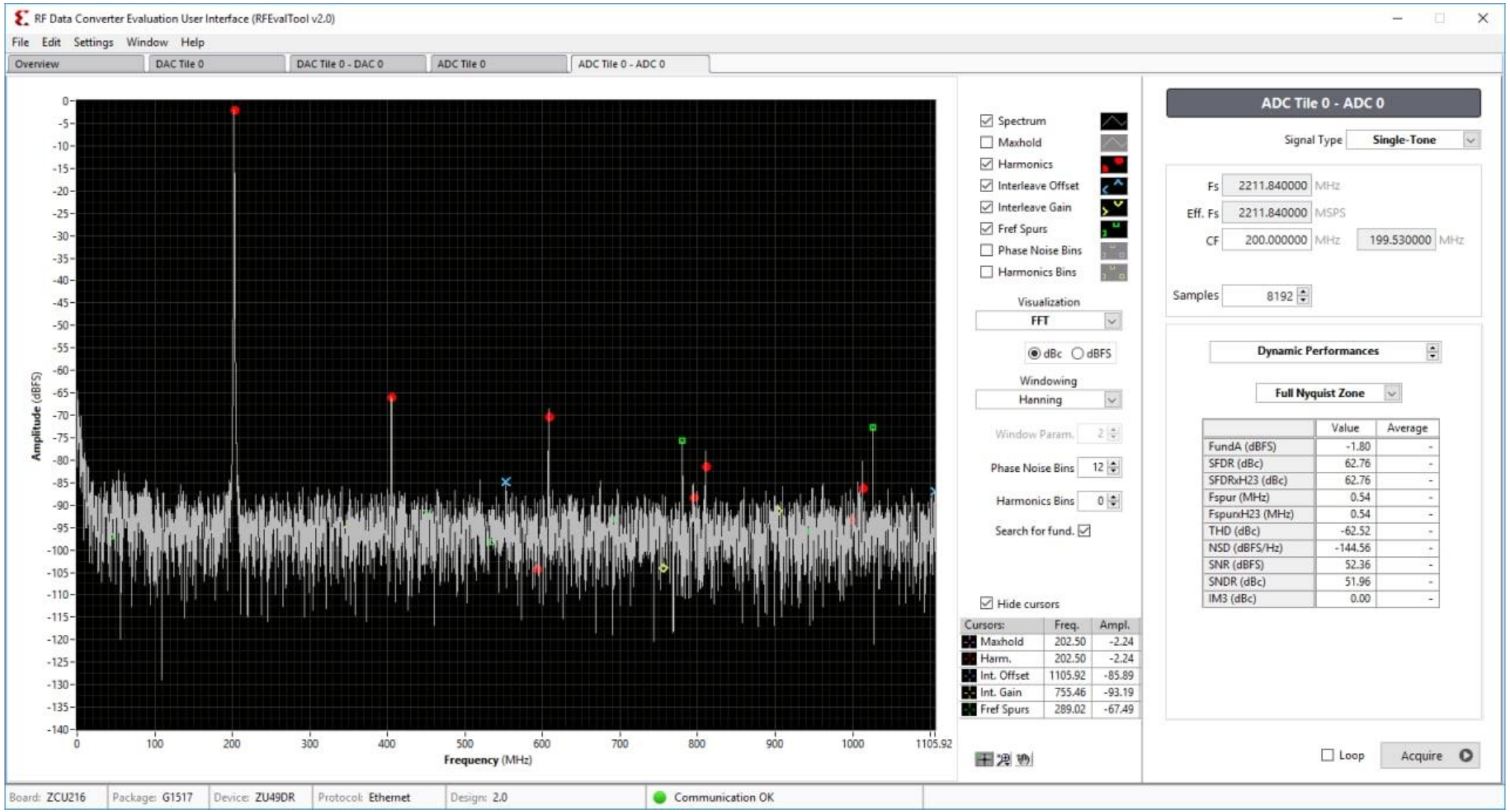
Backup slides



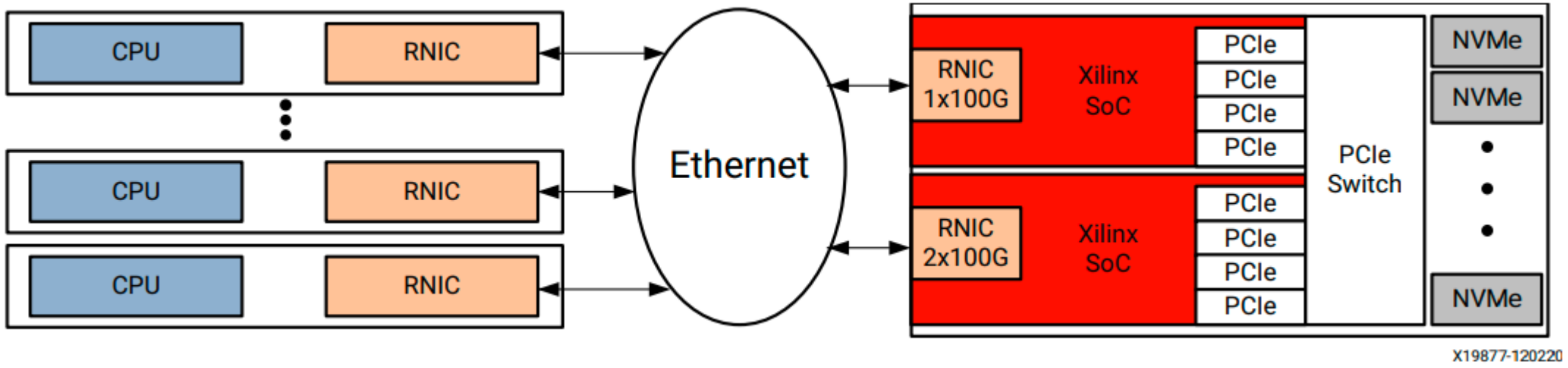
Back-End Readout Card (2)




Processing System
Application Processing Unit
Arm®
Cortex®-A53
NEON™
Floating Point Unit
32KB
I-Cache
w/Parity
32KB
D-Cache
w/ECC
Memory
Management
Unit
Embedded
Trace
Macrocell
1
2
3
4
GIC-400
SCU
CCI/SMMU
1MB L2 w/ECC
DDR Controller
DDR4/3/3LLPDDR4/3
ECC Support
256KB OCM
with ECC
System
Control
DMA
Timers & WDT
Resets
Clocking
Debug
High-Speed
Connectivity
DisplayPort
USB 3.0
SATA 3.0
PCIe Gen2
PS-GTR
Real-Time Processing Unit
Arm
Cortex-R5
Vector Floating Point Unit
Memory Protection Unit
128KB
TCM w/ECC
32KB
I-Cache w/ECC
32KB
D-Cache w/ECC
1
2
GIC
Security
Config
AES Decryption
Authentication
Secure Boot
TrustZone
Voltage/Temp
Monitor
Platform
Management
Unit
Power
System
Management
General Connectivity
GigE
CAN
UART
SPI
Quad SPI NOR
NAND
SD/eMMC
Programmable Logic
RF Signal Chain
Up to 5GSPS RF-ADCs
Up to 10GSPS RF-DACs
SD-FEC
High-Speed Connectivity
33G SerDes
100G Ethernet MAC
100G Interlaken
PCIe® Gen4
System Monitor
General-Purpose I/O
High-Performance HPIO
High-Density HDIO
Storage & Signal Processing
Block RAM & UltraRAM
DSP


RF Data Converter Evaluation User Interface (RFEvalTool v2.0)
File Edit Settings Window Help
Overview
DAC Tile 0
DAC Tile 0 - DAC 0
ADC Tile 0
ADC Tile 0 - ADC 0
Amplitude (dBFS)
Frequency (MHz)
Spectrum
Maxhold
Harmonics
Interleave Offset
Interleave Gain
Fref Spurs
Phase Noise Bins
Harmonics Bins
Visualization
FFT
dBc dBFS
Windowing
Hanning
Window Param.
Phase Noise Bins 12
Harmonics Bins 0
Search for fund.
Hide cursors
Cursors: Freq. Ampl.
Maxhold 202.50 -2.24
Harm. 202.50 -2.24
Int. Offset 1105.92 -85.89
Int. Gain 755.46 -93.19
Fref Spurs 289.02 -67.49
ADC Tile 0 - ADC 0
Signal Type Single-Tone
Fs 2211.840000 MHz
Eff. Fs 2211.840000 MSPS
CF 200.000000 MHz 199.530000 MHz
Samples 8192
Dynamic Performances
Full Nyquist Zone
Value Average
FundA (dBFS) -1.80 -
SFDR (dBc) 62.76 -
SFDRxH23 (dBc) 62.76 -
Fspur (MHz) 0.54 -
FspurxH23 (MHz) 0.54 -
THD (dBc) -62.52 -
NSD (dBFS/Hz) -144.56 -
SNR (dBFS) 52.36 -
SNDR (dBc) 51.96 -
IM3 (dBc) 0.00 -
Loop
Acquire
Board: ZCU216
Package: G1517
Device: ZU49DR
Protocol: Ethernet
Design: 2.0
Communication OK

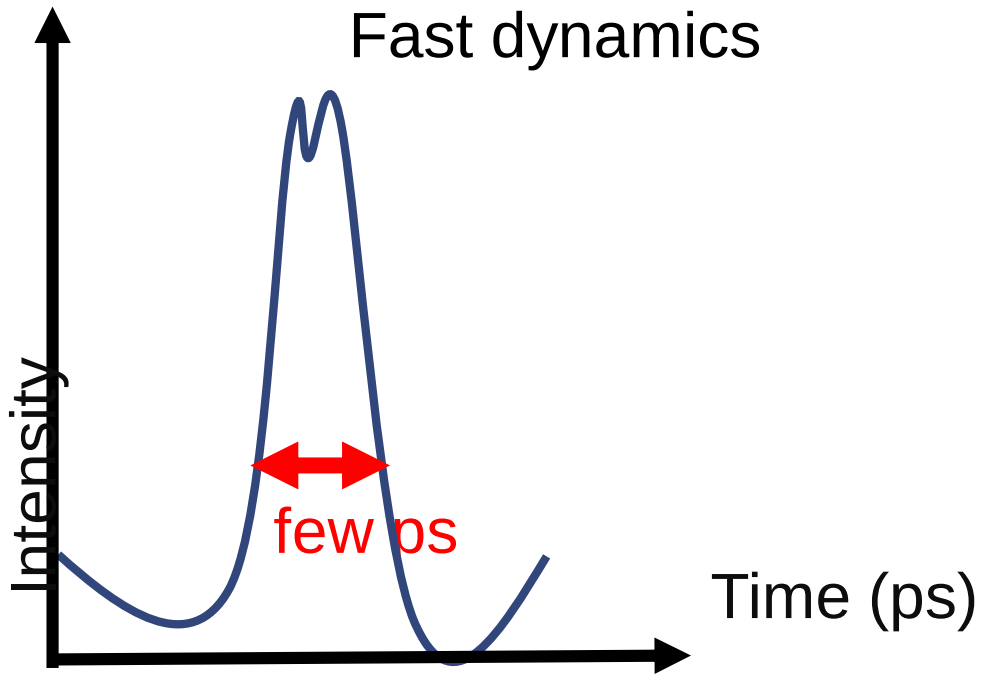
Backup slides



Backup slides

- Given: fs pulse
- Task: Measuring the pulse
- How to measure such a short pulse?
  - Requires sampling rate in THz range
    - Problem

- Idea/Solution: Photonic Time-Stretch



$$\mathrm{ENOB} = \frac{\mathrm{SINAD} - 1.76}{6.02}, \qquad \mathrm{SINAD} = \frac{P_{\mathrm{signal}} + P_{\mathrm{noise}} + P_{\mathrm{distortion}}}{P_{\mathrm{noise}} + P_{\mathrm{distortion}}}.$$