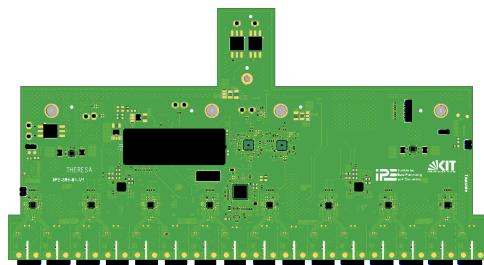


# A Terabit Sampling System with a Photonics Time-Stretch ADC

Master Thesis  
of

Olena Manzhura

at the Institute for Data Processing and Electronics (IPE)



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Second Reviewer: Dr. Michele Caselle (IPE)

15.11.2020 – 13.08.2021



# Declaration

I hereby declare that I wrote my master thesis on my own and that I have followed the regulations relating to good scientific practice of the Karlsruhe Institute of Technology (KIT) in its latest form. I did not use any unacknowledged sources or means, and I marked all references I used literally or by content.

Karlsruhe, 13.08.2021, \_\_\_\_\_  
Olena Manzhura

Approved as an exam copy by

Karlsruhe, 13.08.2021, \_\_\_\_\_  
Prof. Dr. Anke-Susanne Müller (LAS)



# **Abstract**



# Zusammenfassung



# Résumé



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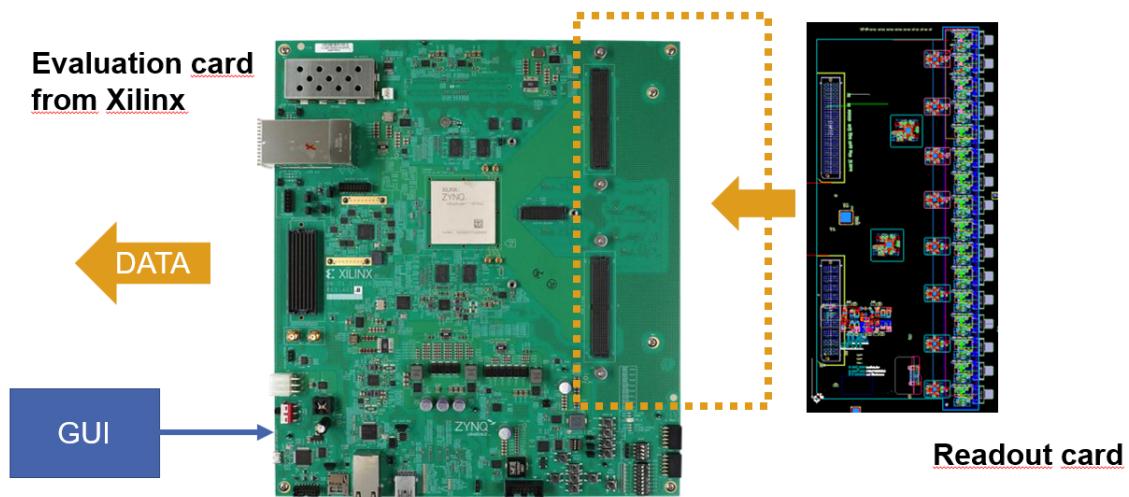
# **1. Introduction**



## **2. State Of The Art Read-Out-Systems**



### 3. Architecture Of The New Read-Out-System



**Figure 3.1.:** General concept of the new readout system

**TODO:** Picture of the WHOLE system, i.e. with the optical front end + power splitter + theresa + zcu216

#### 3.1. Optical part

#### 3.2. Optical Part

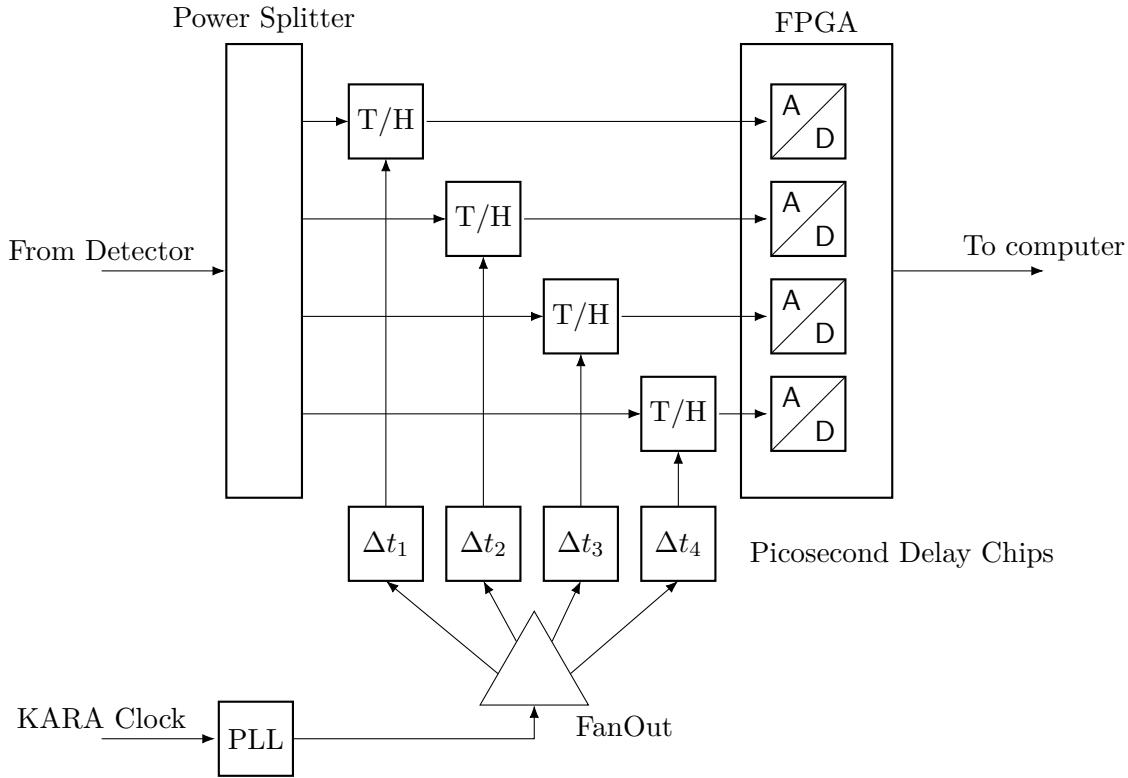
”femtosecond Ytterbium-doped fiber laser (Orange) from MENLO GmbH. The emitted pulses have a spectral bandwidth of 50 nm, and the total output average power is 40 mW. The repetition rate is chosen at 88 MHz, which corresponds to 1/4 th of the RF frequency of Synchrotron SOLEIL and 104 times the electron revolution frequency.”

#### Photodetector

The detection and subtraction between the two stretched signals is performed using a amplified balanced photodetector (photoreceiver) from Discovery Semiconductors, with 20 GHz bandwidth and 2800 V/W gain (specified at 1500 nm).

#### 3.3. Front-End Card

Figure 3.2 shows the general schema of the sampling system, reduced to four channels for presentation purposes.



**Figure 3.2.:** General architecture of THERESA with power splitter and Analog-To-Digital-Converters (ADCs). For presentation purposes only four of the sixteen channels are shown.

### 3.3.1. Time Interleaving

In order to increase the sampling rate, the so called time-interleaving technique is used. In this section, first basic theory about this technique is given. Then, the implementation in the new system is described.

#### 3.3.1.1. Theory

In the *Time Interleaving* technique multiple ADCs are used in such way, that allows to sample data at a faster rate, than the respective sample rate of each individual ADC. The principle is based on time-multiplexing an array of  $M$  identical ADCs (see Figure 3.3), each sampling at  $f_c = f_s/M$  individually. This means, the ADCs are clocked in such a way, that they start their respective conversion cycle shortly one after another. At time  $t_0$  the first ADC starts converting the input signal  $V_i(t_0)$ , after a time delay  $\Delta t_i$  the second starts converting the signal  $V_i(t_0 + t_i)$ , the third converts  $V_i(t_0 + 2t_i)$  and so on. After the  $M$ -th ADC has sampled the signal  $V_i(t_0 + (M - 1)t_i)$ , the whole cycle starts anew with the first converter. [MR15]

#### Challenges

Spurs appear in the spectrum. There are several reasons for this.

First reason is the *offset mismatch* between the ADCs. Each ADC has an DC offset value. Considering as example an interleaving structure with two ADCs and a constant input voltage: when the samples are acquired back and forth between the two ADCs, the resulting output will switch back and forth between two levels due to the different offset levels. This output switches at the frequency  $f_s/2$  and therefore introduces an additional frequency

component in the spectrum (see Figure 3.4). The magnitude of the spur depends on the offset difference between the ADCs. [Har19]

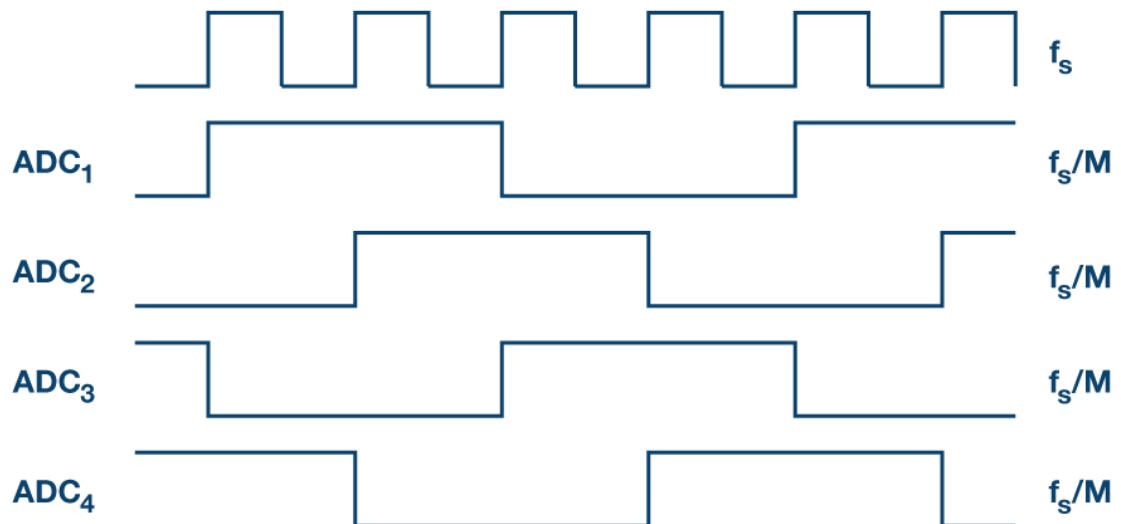
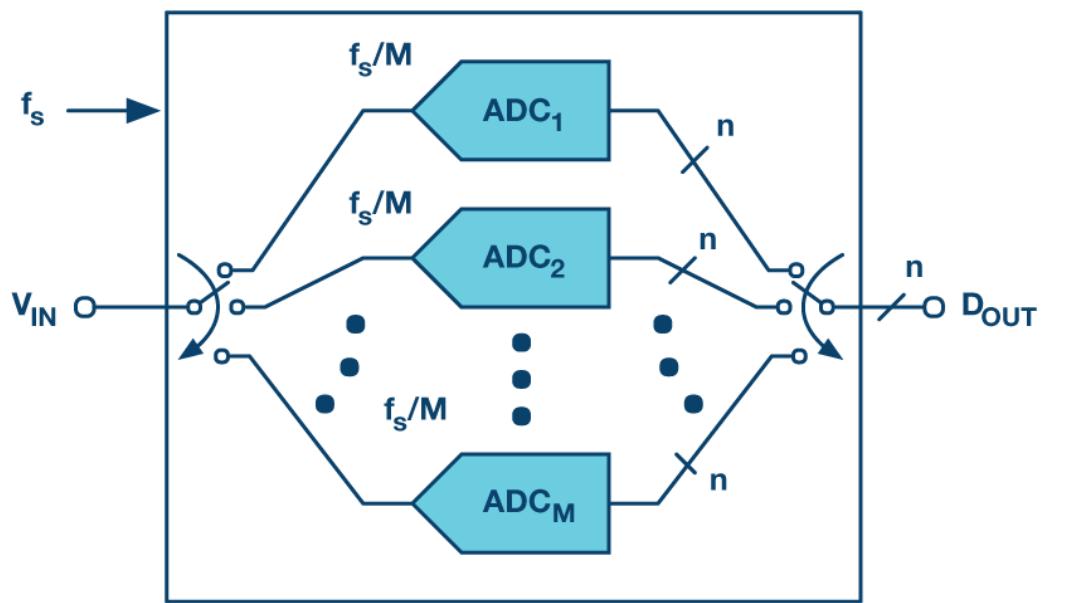
Besides of the offset also the gain of the converters can be mismatched. This *gain mismatch* has a frequency component to it, which in case of an input signal of the frequency  $f_{\text{in}}$  results in a spur at  $f_s/2 \pm f_{\text{in}}$  (see Figure 3.5). [Har19]

In the time domain, *timing mismatch* due to group delay in the analog circuitry of the ADC and clock skew<sup>1</sup> can occur. The group delay in analog circuitry can vary between the converters. Furthermore, the clock skew has on the one hand an aperture uncertainty component at each of the ADCs and on the other hand a component related to the accuracy of the clock phases, which are input to each converter. [Har19] This mismatch also produces a spur at  $f_s/2 \pm f_{\text{in}}$  (see Figure 3.6).

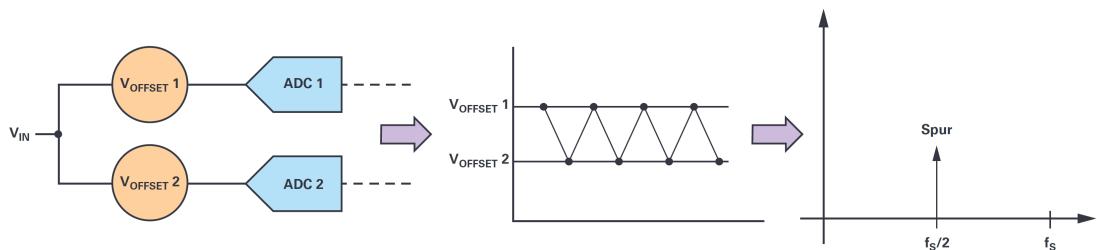
The last possible mismatch is the *bandwidth mismatch*, which contains both gain and phase/frequency component (see Figure 3.7). Due to bandwidth mismatch, different gain values at different frequencies can be seen. An additional timing component causes different delays for signals at different frequencies through each ADC. Just like gain and timing mismatch, the bandwidth mismatch causes a spur at  $f_s/2 \pm f_{\text{in}}$ .

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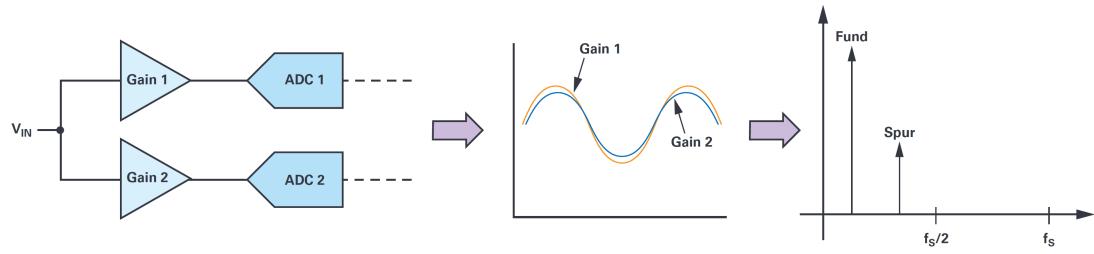
<sup>1</sup>Difference in arrival time of the clock signal at different components.



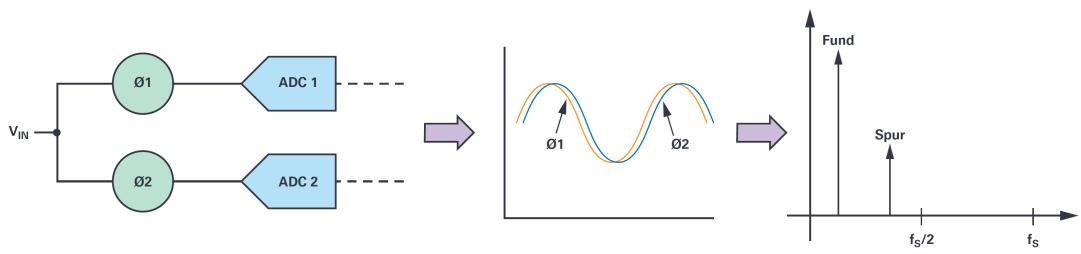
**Figure 3.3.:** Placeholder: An array of  $M$  time interleaved  $N$ -bit ADCs with example of clocking scheme for the case of  $M = 4$  [MR15]



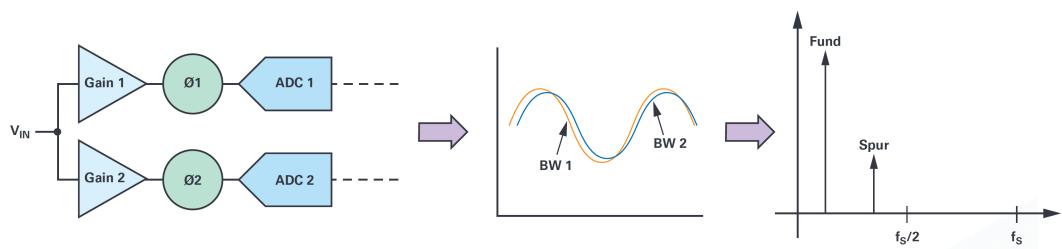
**Figure 3.4.:** Placeholder: Offset-Mismatch in Interleaving [Har19]



**Figure 3.5.:** Placeholder: Gain-Mismatch in Interleaving [Har19]



**Figure 3.6.:** Placeholder: Timing-Mismatch in Interleaving [Har19]



**Figure 3.7.:** Placeholder: Timing-Mismatch in Interleaving [Har19]

### 3.3.1.2. Implementation

The delay step size must be small enough, such that the ADC interleaving technique subsection 3.3.1 can be implemented. The ADCs on the read-out card sample at a maximal sample rate of 2.5 GS/s, meaning during the time

$$t_s = \frac{1}{2.5 \text{ GS/s}} = 400 \text{ ps} \quad (3.1)$$

all 16 ADCs have to be clocked one time. This means, a delay step can not be greater than  $400 \text{ ps}/16 = 25 \text{ ps}$ .

Clock to THA: 500 MHz

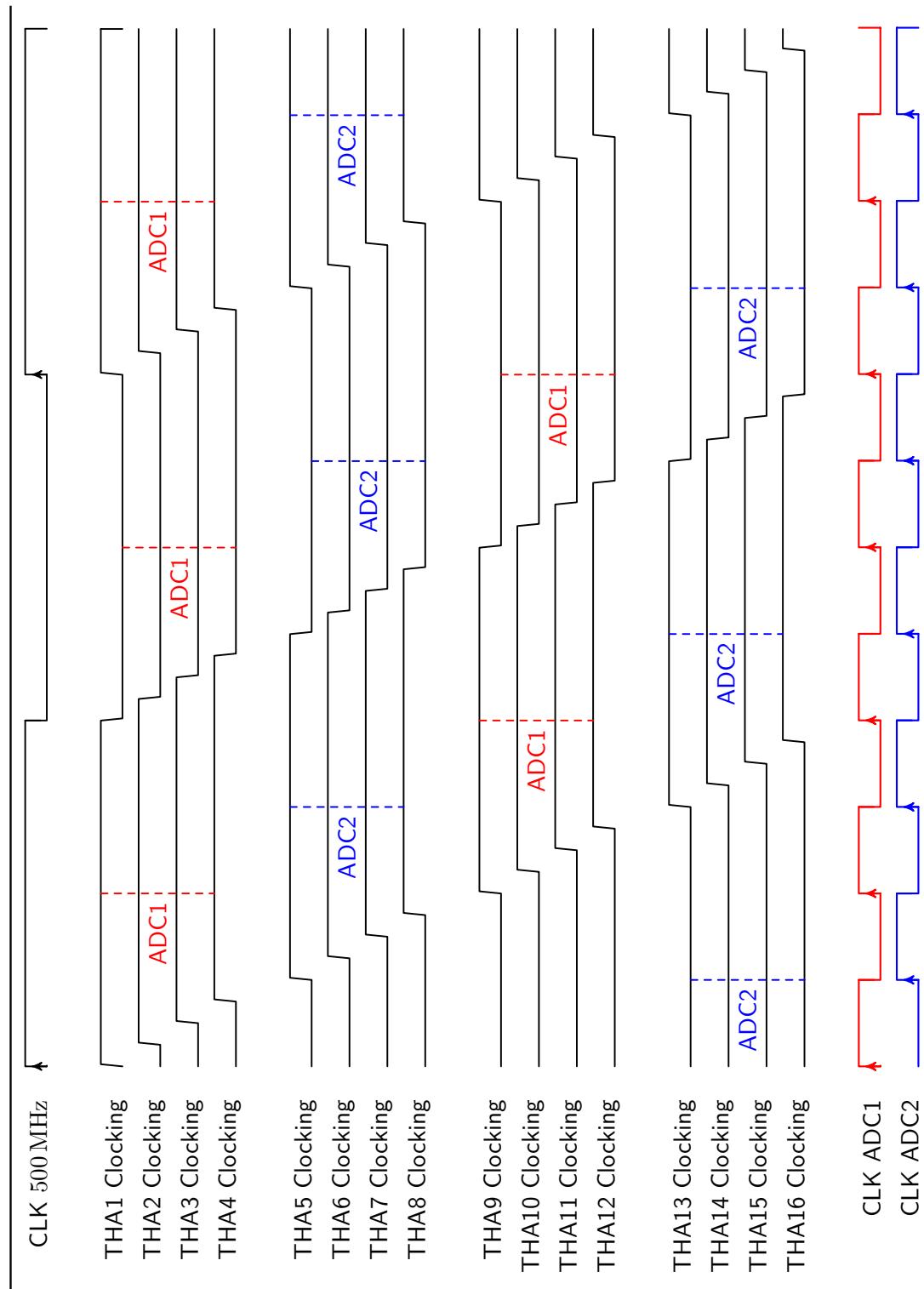
Total Hold time: 1 ns

→ Step size for delay:

$$\frac{1 \text{ ns}}{16 \text{ channels}} = 62.5 \text{ ps} \quad (3.2)$$

Aperture delay, jitter, need to be taken into account to determine the max. sampling frequency.

The necessary step size for the delay chips, when using 16 ADC@2 GS/s in time-interleaving mode, is:  $\frac{2 \text{ GS/s}}{16} = 31 \text{ ps}$  However, providing individual clocks to the ADCs is not possible on the ZCU216 card. ADCs are grouped together into tiles, each tile containing four converters. One single reference clock signal is propagated to all tiles. Sampling clock is adjusted at each tile individually, however this clocking signal is the same for all of the four converters in the tile. Normally, only one reference clock can be provided. Analyzing the schematic of the ZCU216 board revealed however, that there are pins leading to the FPGA banks (224 to 227), labeled as clocks for the individual tiles. Two of the clocks are not connected (224 and 227). 225 is provided via SMA cable, the other comes from the LPAM clock connector.



**Figure 3.8:** Track-And-Hold-Amplifier (THA) Timing diagram. Shows the clocking of the THA (HIGH = hold mode, LOW = track mode). Dashed line represents the sampling of the ADC.

### 3.4. Readout Card

#### TODO

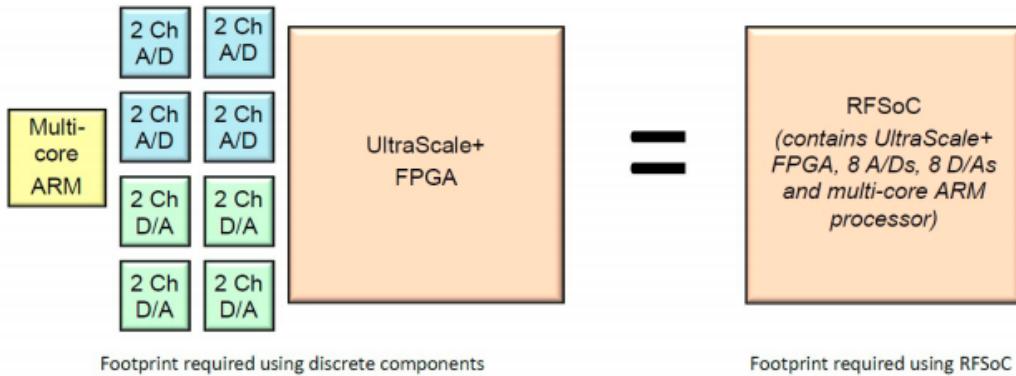
##### 3.4.1. Selection Of The Card

When selecting the Readout Card, following criteria need to be considered:

- Integrated ADCs
- Number, resolution and bandwidth of ADCs
- Peripheral connections
- Flexibility/Customization
- Suitable connectivity for high-data-throughput

Footprint of using all discrete components is, as one can imagine, higher, than if you integrate all the parts into one Integrated Circuit (IC). Not only the footprint is a concern, but also the number of connections. ADCs with high resolution, a high number of ADCs therefore explodes the necessary amount of connections. High number of ADCs also means

**Figure 2.** Discrete component versus RFSoC solution size comparison



**Figure 3.9.: Placeholder: Discrete vs IC**

## 4. Design Of The Front-End Sampling Card

In this chapter, the process of designing the front-end sampling card is described. Designing a PCB is a two step process: circuit design and layout design. In this thesis, the software used to cover both of these steps is PADS xDx Designer (for schematic capture) and PADS Layout/Router (for PCB layout design) from Mentor Graphics (subsidiary of Siemens).

### 4.1. Schematics

Without knowing which components are needed and how they are interconnected, it is impossible to manufacture any board, no matter how high or low the level of complexity is. The main purpose of a schematic is thus to provide a documentation about the necessary components and in which way they should be connected to another. Furthermore, a schematic provides a starting point for automatic placement and routing, i.e. where the components are placed and how they are connected on the physical PCB, which is done with the layout design tool. During the creation of the schematics, the following points have to be taken into consideration:

- Deciding which components are needed and what the performance requirements are. Especially for high-speed components carefully considering specifications like signal rise and fall times, jitter, skew, etc. is crucial to achieve the overall expected performance.
- Keeping in mind how many pins are available for peripheral connection, control signals, etc. Many components have an interface for programming (e.g. Serial Peripheral Interface (SPI)) which requires several pins. Especially for boards with a lot of components this can quickly become an issue.
- Checking the signaling interfaces of the components. Additional circuitry might be needed for interfacing between two different components. Some signaling interfaces, like Low Voltage Differential Signaling (LVDS), require a specific voltage level, which might result in the need of voltage level translators.
- Keep in mind the different common mode voltages at input/output pins of different components and placing decoupling capacitors if needed.
- Consider placing additional filtering for power supplies, as well as recommended filters from manufacturers of the components.
- Choose suitable type and amount of power supplies/voltage regulators.
- Packaging/Size of the components. Obviously the size matters, as space on the board is limited. But the package also introduces additional capacitance/inductance, which can be a problem for precise filtering circuits.

- Power dissipation of the components. Especially voltage regulators might need coolers. This might not pose any problems for components which are located on the top side of the board. However, components on the bottom side might create an issue, if the designed PCB should be mounted on another board.
- For mixed-signal boards, i.e. boards containing digital and analog signal paths, analog and digital ground should be separated. For ICs like THAs or ADCs, where both analog and digital signals are present, connecting the grounds via appropriate components needs to be considered.
- Check if the components are still available and if they can be delivered in the given project time.

This list is certainly not complete, but provides an overview over the most important points which need to be taken into account during design. Decoupling techniques and separation of analog and digital ground are explained a bit more detailed, being very important and crucial steps for design of high-performance PCB.

### Decoupling techniques

Probably the most important part in schematics design is proper decoupling of power supplies, as ICs require a stable voltage on the power supply pin for optimal performance. Any ripple<sup>1</sup> or noise can substantially degrade the performance of the ICs, i.e. by decreasing the noise margin. *Noise margin* defines the difference between the useful signal and noise. A sufficient noise margin is necessary to guarantee that the output signal will still be correctly interpreted, even if some noise is added to the signal. Usually, manufacturers give information about proper decoupling circuits for their component in the data sheet. If this is not the case, there are basic rules of thumb which can be followed to ensure good decoupling. [Anab]

Basically, two types of voltage variations on the power supply pin can be distinguished: low frequency and high frequency variation. Low frequency variation occurs for example due to devices (or parts of them) being enabled/disabled or in the event of data traffic or data processing. The current draw during these occurrences can not be compensated immediately by the voltage regulator providing the supply voltage, which leads to drops in the voltage levels. Time frames of this variation vary in the range of milliseconds up to days. High frequency variation results from switching events in the device, occurring in the range of the clock frequency and the corresponding harmonics up to about 5 GHz. Spikes due to Electro-Magnetic Interference (EMI) are also a source of high frequency variation and need to be compensated for. [Xil]

Ideally, one capacitor, which acts as a low-pass filter, should be enough to mitigate these variations. A real capacitor however has parasitics and thus can in general not be modeled by a “pure” capacitive behavior, especially for high-frequency applications. Additional resistances and inductance need to be considered [Anab]:

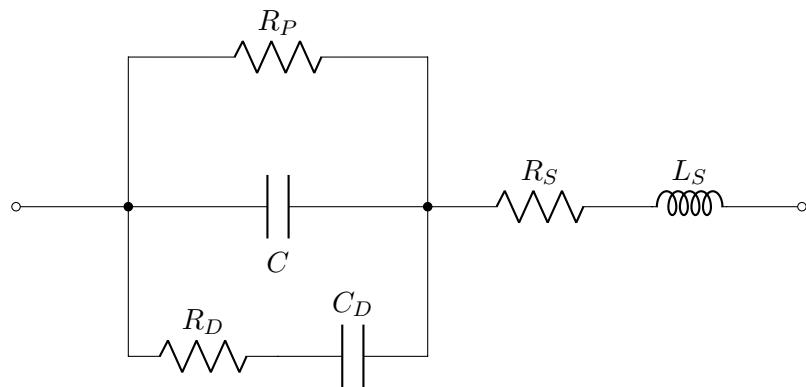
- A parallel resistance  $R_P$ , which shunts the nominal capacitance ( $C$ ), representing insulation resistance or leakage.
- A series resistance  $R_S$ , or Equivalent-Series-Resistance (ESR), which represents the plates and the leads of the capacitor.
- A series inductance  $L_S$ , or Equivalent-Series-Inductance (ESL), that models the inductance of the plates and leads of the capacitor.

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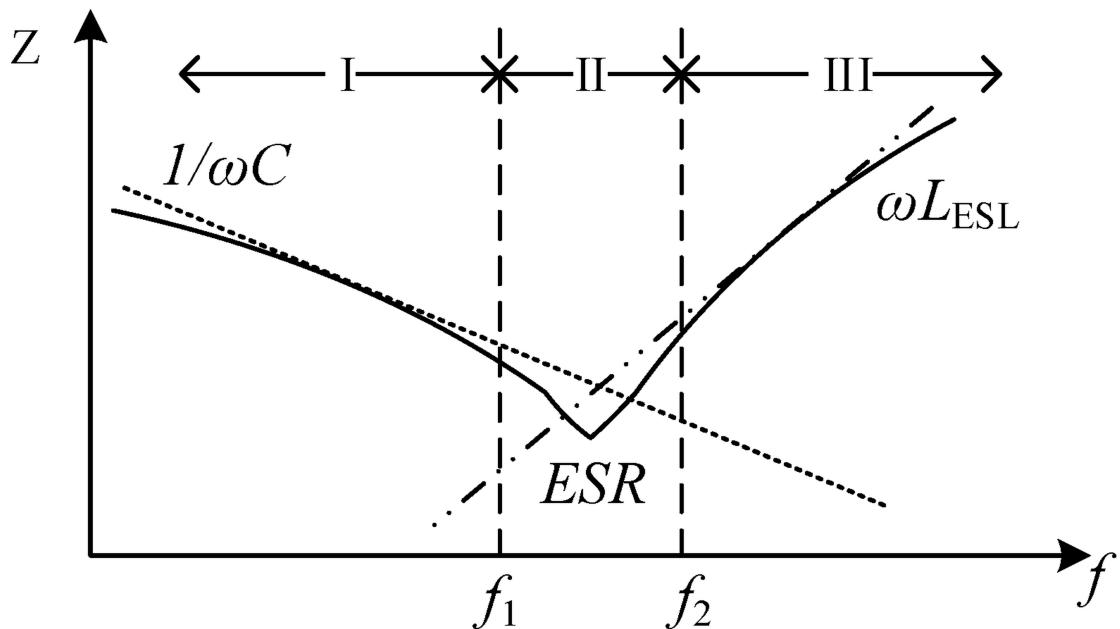
<sup>1</sup>*Ripple* is the Alternating Current (AC)-voltage superimposed on an otherwise Direct Current (DC)-voltage.

- A parallel resistance and capacitance,  $R_D$  and  $C_D$ , which model the effect called dielectric absorption. This denotes the phenomenon, that a capacitor which has been charged for a long time, doesn't fully discharge when briefly discharged. Dielectric absorption can be detrimental for high-precision use-cases, for power supply decoupling this effect doesn't have to be considered.

Consideration of all these effects leads to the equivalent circuit shown in Figure 4.1. It can be seen that this forms a RLC circuit, meaning the capacitor will not have the ideal behavior over the whole frequency range. In fact, a real capacitor shows an impedance response as seen in Figure 4.2, which resembles one of a band stop, rather than a low pass. Typical capacitive behavior is seen in region (I). Region (II) shows the influence of the ESR, which is why there is a residual impedance at the lowest point. Region (III) showcases the effect of the ESL. To extend the capacitive behavior over a wider frequency range, at least two capacitors are placed.



**Figure 4.1.:** Equivalent circuit of a real capacitance (redrawn from [Anab])



**Figure 4.2.:** Qualitative impedance response of a real capacitance [DK20]

To deal with the low frequency variation, a large capacitor (typical values: 10  $\mu\text{F}$  to 100  $\mu\text{F}$ ) is placed next to the component, not more than 5 cm ( $\approx$  2 inch.) away. The role of this capacitor is to be a charge supply for the instantaneous needs of the device, i.e. keeping a constant voltage level until the slower control loop of the voltage regulator can compensate

for the changed current draw. [Anab]

A small capacitor (typical values: 0.01  $\mu$ F to 0.1  $\mu$ F), placed as close as possible to the power pins of the component. This capacitor should bypass the high frequency variation on the power supply line. [Anab]

To cover a larger frequency range, multiple capacitors can be used.

All capacitors should be connected through vias or short traces to a large area, low impedance ground plane. Vias on a PCB are used to connect different layers, a plane is an uninterrupted area of metal covering the whole (or part) of a PCB layer (basic PCB structures are also explained in subsection 4.2.1). Connecting capacitors in this way minimizes the inductance due to connection traces. [Anab]

An optional ferrite bead in series with the supply pin keeps external high frequency from the device and the noise generated inside the component from the rest of the board. [Anab]

## Separating Analog and Digital Ground

TODO

### 4.1.1. Connectors

The number and type of connectors is primarily defined by the read-out card, on which the sampling board is mounted. The different connector types serve different purposes, which can be organized into three categories.

#### Digital Control Signals

For digital control signals (i.e. SPI, enable signals, ...) and clocking a VITA 57.4 FMC+ connector from *SAMTEC* is used (see Figure 4.3).

FPGA Mezzanine Card (FMC) is a standard defined by VMEbus International Trade Association (VITA) to provide a standard mezzanine card<sup>2</sup> form factor, connectors, and modular interface to a Field Programmable Gate Array (FPGA) located on a base board (carrier card). [See09] The FMC+ standard extends the pin count and throughput of the present high-speed interfaces.

This connector provides 560 pins arranged in a  $14 \times 40$  array, 80 of which are additional high-speed interfaces, located on either side of the connector (therefore this connector type is also called High Serial Pin Count Extension (HSPCe) connector, as opposed to the HSPC connector which doesn't have additional rows). For user-defined purpose 160 pins are available. They can be used as single-ended or differential pins. Clocking capable pins can be used to propagate clock signals from the mezzanine to the carrier board.

Furthermore, the connector provides pins for power supply from carrier board to mezzanine card. [FMC] The voltage levels provided are listed in Table 4.1.

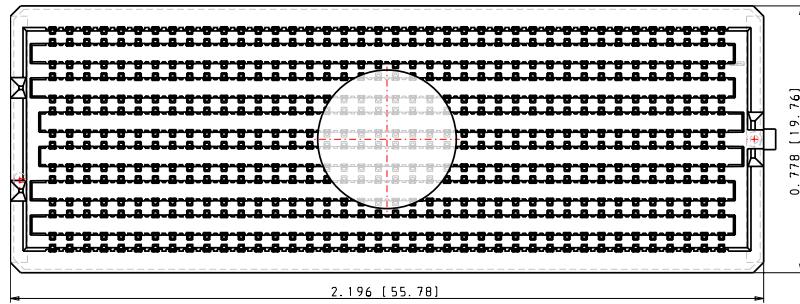
**Table 4.1.:** Voltage levels for power supply provided by the FMC+

Voltage	Max. current	Max. capacitive load
$V_{ADJ}$ , 0 V to 3.3 V	4 A	1000 $\mu$ F
3.3 V	3 A	1000 $\mu$ F
12 V	1 A	1000 $\mu$ F

An assembly drawing of the FMC+ connector is shown in Figure 4.3.

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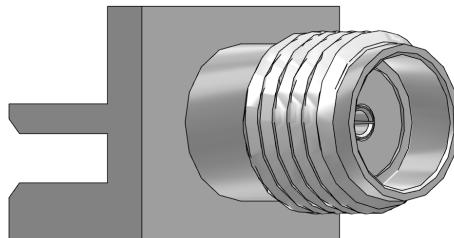
<sup>2</sup>A PCB which is plugged on a plug-in board. [PCM]



**Figure 4.3.:** Part drawing of FMC+ connector [SAM]

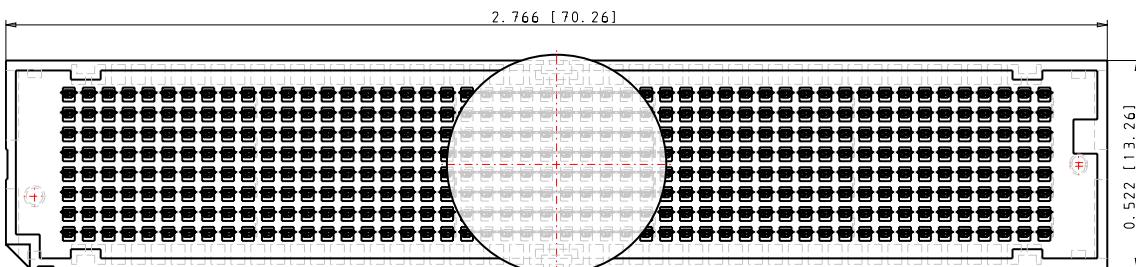
### Analog Signals

The signal from the detector is provided to the THAs through SubMiniature version A (SMA)<sup>3</sup> RF connectors from *molex*, which are mounted at the edge of the board. Figure 4.4 shows a 3D model of this connector type.



**Figure 4.4.:** 3D model of the edge-mount RF SMA connector from *molex* [mol]

On the read-out board two RFMC 2.0 (RF Mezzanine Card) interface connectors are provided. The connectors used are Low Profile Array, Female (LPAF) connectors from *SAMTEC* with 400 pins arranged in a  $8 \times 50$  array. One connector is dedicated for transmitting signals from the mezzanine card to the on-board ADCs. The other provides the analog output from the on-board Digital-To-Analog-Converters (DACs)<sup>4</sup> to the mezzanine card. On the sampling board, the male counterpart of the connectors, Low Profile Array, Male (LPAM), is used (see Figure 4.5).



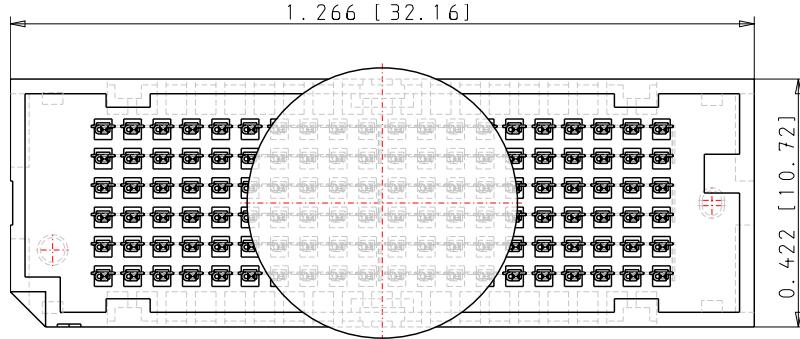
**Figure 4.5.:** Part drawing of a LPAM 8  $\times$  50 connector

<sup>3</sup>Coaxial Radio Frequency (RF) connector

<sup>4</sup>A DAC translates digital values into an analog signal.

## Clock Signals

The clock signals from the Phase-Locked-Loops (PLLs) on the sampling board are propagated in different ways. The reference clock for the FPGA is propagated through the FMC+ connector. Clocking for the ADCs and the DACs is provided through a  $6 \times 20$  LPAM connector (see Figure 4.6).



**Figure 4.6.:** Part drawing of LPAM  $6 \times 20$  connector

The clock coming from Karlsruhe Research Accelerator (KARA) is provided through RF SMA connectors directly to the PLL.

### 4.1.2. Sampling-Channel

The sampling channel consists of the THA, which is driven by a delay chip.

#### Track-And-Hold-Amplifier

The THA used is the same as in Karlsruhe Pulse Taking Ultra-fast Readout Electronics (KAPTURE). The component was chosen such that jitter lies in the range of hundreds of femtoseconds. [CBC<sup>+</sup>13] According to the data sheet [Anac], the component shows the characteristics shown in Table 4.2.

As the analog input to the THA is single-ended, a  $50\Omega$  termination on the unused input pin has been added, as recommended in the data sheet.[Anac]

At the power pins, decoupling capacitors and a ferrite bead were placed. The THA is a crucial component, as it samples the detector signal, therefore any possible noise should be reduced to a minimum.

#### Delay Chip

The delay chip is used to create a delay in the clocking signal, which then goes to the THA chip. For the selection of the delay chip, the most important characteristic, apart from jitter, is the delay step size and delay range.

As indicated in subsubsection 3.3.1.2, the step-size of the delay chip must not exceed 25 ps to use the technique with ADCs sampling at 2.5 GHz.

With the HMC856 programmable delay chip from *Analog Devices*, which is also used for the KAPTURE sampling board, a minimal step size of 3 ps [Anaa] is possible. This is much less than 25 ps and thus the chip could be potentially used for the intended purpose. However, one drawback is the maximal delay range of 100 ps. Considering a signal, which is stretched over several nanoseconds, this range limits the possibility to freely chose the overall timing resolution. Another problem is the programming interface of the chip, which consists of five differential Current Mode Logic (CML) inputs. This means, one chip already

**Table 4.2.:** Specifications of the HMC5640 THA

Parameter	Min	Typ.	Max	Unit
<b>Analog Inputs</b>				
Differential FS Range		1		V <sub>pp</sub> <sup>1</sup>
Common mode voltage	-0.1	0	0.1	V
<b>Clock Inputs</b>				
DC Differential High Voltage (Track Mode)	20	40	2000	mV
DC Differential Low Voltage (Hold Mode)	-2000	-40	-20	mV
Common mode voltage	-0.5	0	0.5	V
<b>Analog Outputs</b>				
Differential FS Range		1		V <sub>pp</sub>
Common mode voltage		0		V
<b>Track-to-Hold/Hold-to-Track Switching</b>				
Aperture Delay		-6		ps
Random Aperture Jitter (FS, 1 GHz)		< 70		fs
Settling time <sup>2</sup> (to 1 mV)		116		ps

<sup>1</sup>Volt peak-to-peak

<sup>2</sup>*Settling time* is the interval between the internal track-hold transition and the time when the output signal is settled within the specified value.

takes up 10 pins only for control signals. For in total 16 necessary delay chips, this results in 160 pins used only for control of the delay chips. This occupies all pins of the FMC+ connector (see subsection 4.1.1) available for the user.

A better candidate is the dual channel programmable delay chip NB6L295 from *ON Semiconductor*. This chip provides two separately programmable delay channels. This has the benefit of reducing the total chip count by half, as now two THAs can be connected to one delay chip.

The minimal delay step size of 11 ps lies under the maximal 25 ps. Therefore the chip is suitable for the targeted interleaving method, covering a total delay range from 3.2 ns to 8.8 ns per delay channel.

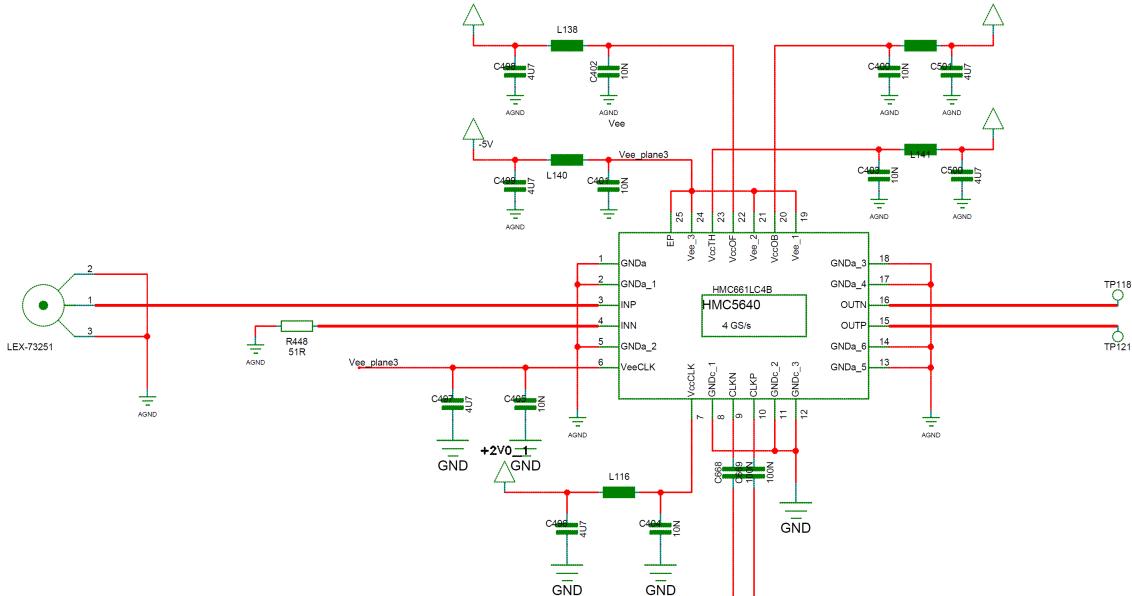
The chip is programmed via Serial Data Interface (SDI), which only requires 4 pins (enable pin, data pin, clock pin, load pin). Thus, the total number of digital control pins used by the delay chips is  $4 \cdot 8 = 32$ , which is a significant reduction compared to the 160 control pins needed by the HMC856 chips.

## Inputs

The inputs of the delay chip are driven by the preceding PLL, the outputs of which are Low-Voltage Positive Emitter-Coupled Logic (LVPECL) drivers. According to the data sheet, when driving the inputs with a LVPECL driver, the VT<sub>x</sub> and  $\overline{VT_x}$  pins of the delay chip need to be connected to  $V_{cc} - 2$  V (see Figure 4.9). In case of  $V_{cc} = 2.5$  V, this results in a voltage level of  $VT_x = \overline{VT_x} = 0.5$  V.

To avoid using an additional voltage regulator, this voltage level is achieved by using a resistive voltage divider connected to  $V_{cc}$ . Choosing the resistor values  $43\text{ k}\Omega$  and  $11\text{ k}\Omega$  results in a voltage of

$$V_{cc} \frac{11\text{ k}\Omega}{11\text{ k}\Omega + 43\text{ k}\Omega} = 0.5093\text{ V} \approx 0.5\text{ V} \quad (4.1)$$



**Figure 4.7.:** HMC5640 THA schematic

A 100 nF capacitor is put in parallel for power supply decoupling.

**Table 4.3.:** Specifications of the NB6L295 delay chip [ON ]

Parameter	Min	Typ.	Max	Unit
<b>Outputs</b>				
Output HIGH Voltage	$V_{cc} - 1075$	$V_{cc} - 950$	$V_{cc} - 825$	mV
Output LOW Voltage	$V_{cc} - 1825$	$V_{cc} - 1725$	$V_{cc} - 1625$	mV
Common mode voltage	-0.1	0	0.1	V
<b>AC Characteristics</b>				
Random Clock Jitter RMS		3	10	ps
Output Rise/Fall Times (@50 MHz)	85	120	170	ps
Serial Clock Input Frequency (50% Duty Cycle <sup>1</sup> )			20	MHz
Minimum Pulse width SLOAD	1			ns

<sup>1</sup>Percentage of the ratio of pulse width and total period of the waveform.

## Outputs

The output of the delay chip is using a LVPECL signaling interface, which is based on an open-emitter topology (see Figure 4.10). This requires a path to DC, which is achieved by adding 140  $\Omega$  resistors.

As the output will be connected to the THA, it is necessary to check the compatibility of the maximum amplitude and common-mode of the pins.

According to the data sheet [ON ], the voltage level of the output can vary between  $V_{cc} - 1825$  mV and  $V_{cc} - 825$  mV (see Table 4.3). Maximal voltage amplitude acceptable by the THA inputs is 2000 mV (see Table 4.2). When using a supply voltage of  $V_{cc} = 3.3$  V, provided e.g. by the read-out card through the FMC+ connector, this leads to a maximum output level of 2475 mV. This exceeds the limit given by the THA. Therefore, for  $V_{cc}$  a smaller voltage should be considered. In this design a voltage of  $V_{cc} = 2.5$  V is chosen, which guarantees that the amplitude falls within the range 675 mV to 1675 mV.

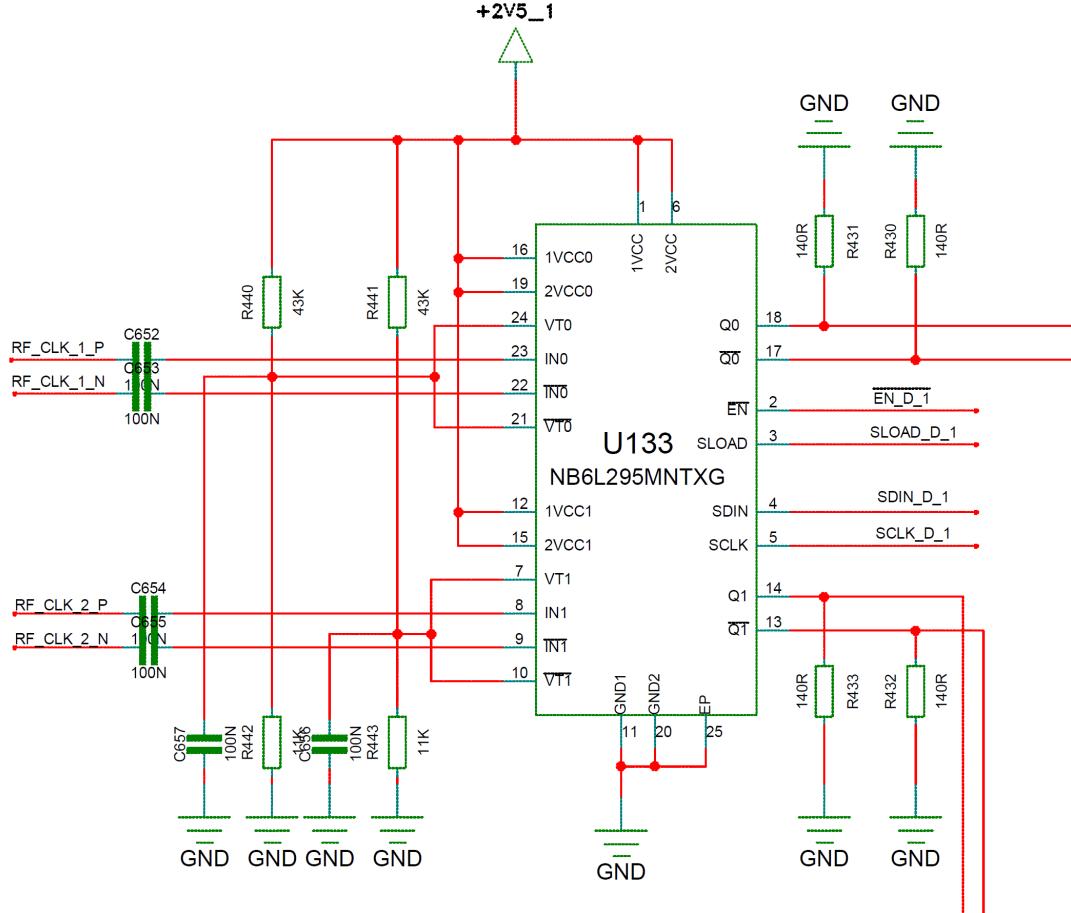


Figure 4.8.: NB6L295 schematic

The second point to consider is the common mode voltages. According to the data sheet of the THA, the common mode voltage of the input clock pins is 0.1 V (see Table 4.2). The common mode voltage of the delay chip is not explicitly mentioned in the data sheet, thus it has to be calculated. The common mode voltage  $V_{CM}$  is just the mean value between the high level and the low level voltage of the output pins:

$$V_{CM} = \frac{V_{out, LOW} + V_{out, HIGH}}{2}. \quad (4.2)$$

According to this, the common mode voltage  $V_{CM}$  of the delay chip output, when taking the minimum/maximum voltage level values, is

$$V_{CM} = \frac{675 \text{ mV} + 1675 \text{ mV}}{2} = 1175 \text{ mV}. \quad (4.3)$$

This is higher than the maximal input common mode voltage of the THA. AC coupling is therefore necessary in this case.

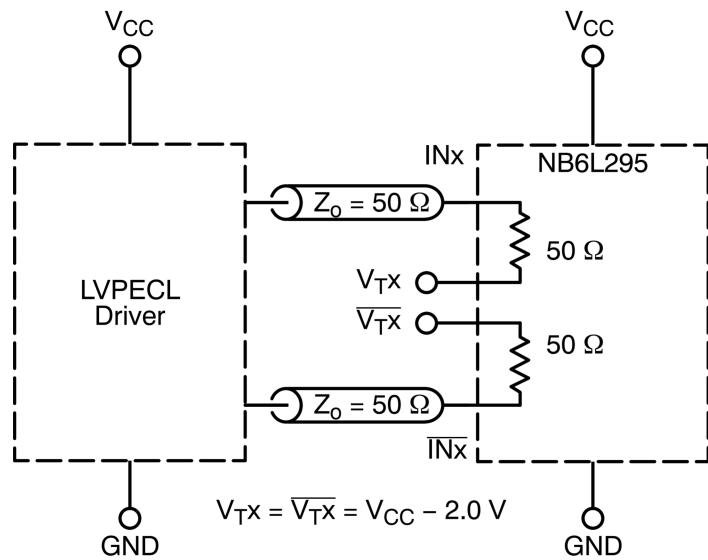


Figure 4.9.: LVPECL recommendations for NB6L295 [ON ]

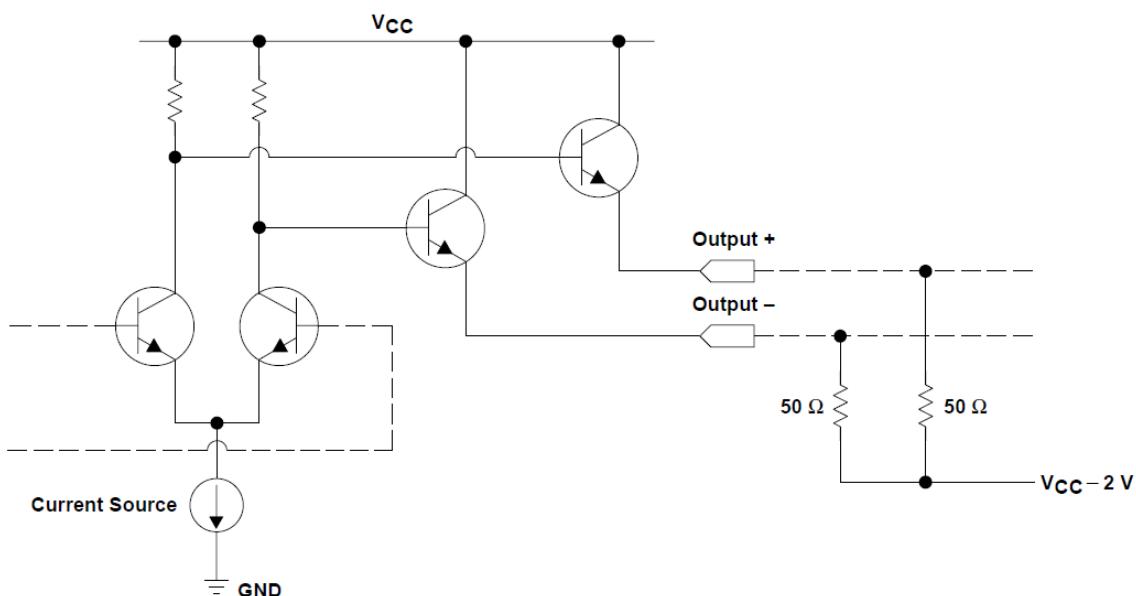


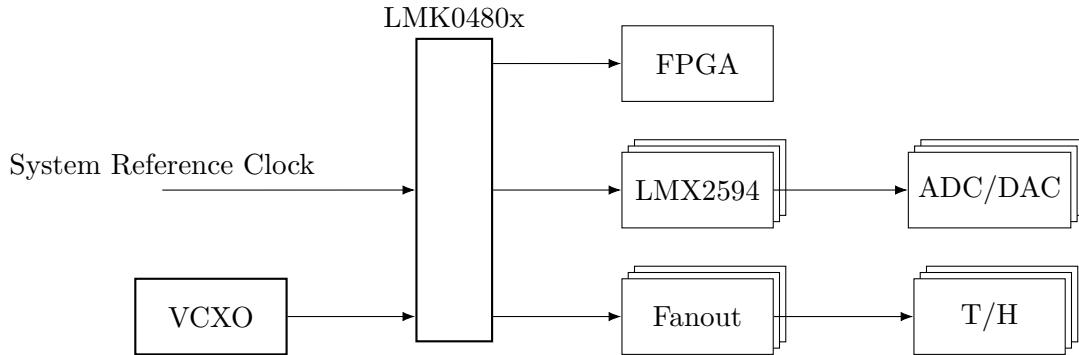
Figure 4.10.: LVPECL driver topology. Left side shows the emitter-follower based driver. On the right, an example biasing with resistors is shown. [Mik]

#### 4.1.3. Level Translator

TODO

#### 4.1.4. Clock Distribution

The clock distribution is designed as shown in Figure 4.11. The LMK04808B low-noise clock



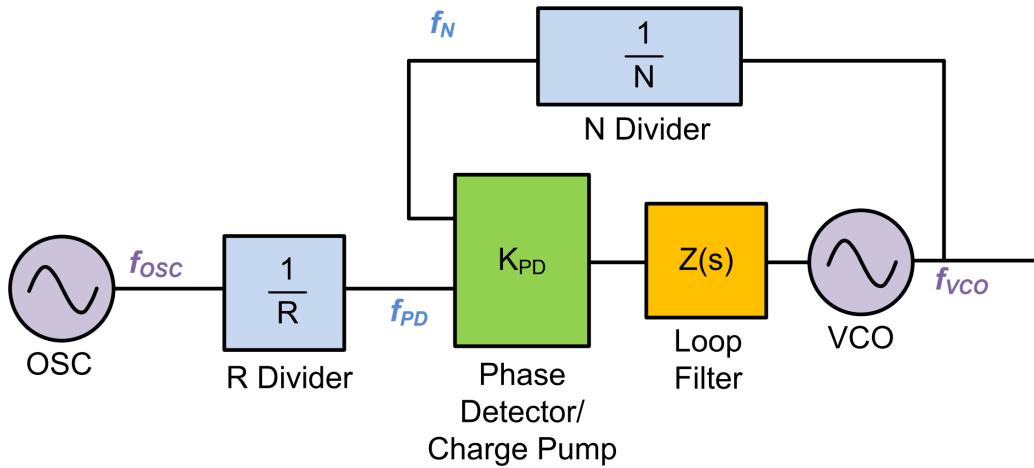
**Figure 4.11.:** Overview of the clocking paths on the sampling board

jitter cleaner with dual-loop PLLs from *Texas Instruments* cleans the incoming reference clock provided from the system (e.g. from KARA) for high temporal accuracy [CBC<sup>+</sup>13]. It is used with an external Voltage-Controlled Crystal Oscillator (VCXO) from *ABRACON*.

The LMK04808B contains two PLLs (therefore called “dual-loop”). The first PLL is used to clean the jitter from the reference clock. The second is then used to create a higher frequency clocking signal out of the cleaned clock.

For proper functioning/best performance, a properly designed loop filter (see Figure 4.12) for both PLLs is needed. *Texas Instruments* provides the *PLLatinum Sim* tool, with which an appropriate loop filter can be calculated, given the device, desired loop bandwidth, phase margin and frequency. The LMK04808B has only 12 outputs which is not enough for the 16 THAs and additional clock signals needed for FPGA, ADCs and DAC. Furthermore, the outputs are divided into six groups à two outputs. Outputs in one group have the same configuration (frequency, phase, ...), which means that effectively only six different outputs are available. Therefore, a low noise clock distribution fan-out buffer, the HMC987LP5E from *Analog Devices*, is used for distributing the clock signal to the delay chips. As one fan-out buffer has eight outputs, two chips are needed to cover all 16 channels. These chips get the output clock signal from two pins of the LMK04808B. To ensure exactly identical clocking signals, both of the pins are chosen to be in one output group. One output of the PLL is propagated to the FMC+ connector as reference clock for the FPGA. Up until this part, this clocking distribution architecture is not different from the one on the KAPTURE sampling board.

As Figure 4.11 shows, the LMK04808B also provides a clocking signal to another PLL, the LMX2594 from *Texas Instruments*. The maximum output frequency of the LMK04808B is 1536 MHz, not enough to clock the ADCs at maximum sampling rate (2.5 GS/s). A second PLL is therefore needed.



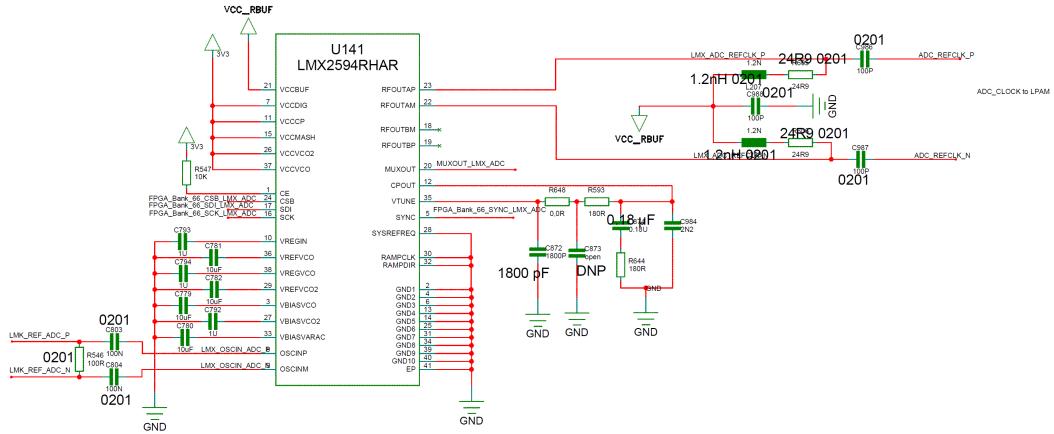
**Figure 4.12.:** General block diagram of a PLL

The LMX2594 provides clocking signal frequencies up to 15 GHz and is therefore a fitting candidate. To calculate the loop filter, the *Texas Instruments PLLatinum Sim* tool is used. The parameters of the used third order loop filter are as shown in Table 4.4. In order to provide the flexibility to enlarge the filter order, some of the components are considered in the schematics, but are either not placed or put to zero. In this way, a placeholder on the board is created. The schematic of the LMX2594 is shown in Figure 4.13.

Due to the ADC clocking limitations on the read-out card explained in subsubsection 3.3.1.2, two of the PLLs are needed. The reference clock signal is provided by outputs from different output groups of the LMK04808B. This way, the phase of each reference clock can be programmed individually, which allows to implement the ADC clocking technique described in subsubsection 3.3.1.2.

**Table 4.4.:** Filter characteristics

Parameter	Value
VCO Gain	239 MHz/V
Loop Bandwidth	32.7 kHz
Phase Margin	69°
Effective Charge Pump Gain	3 mA
Phase Detector Frequency	24.576 MHz
VCXO Frequency	Designed for 15 GHz
<b>Loop filter components</b>	
$C_{1,LF}$	2200 pF
$C_{2,LF}$	180 nF
$C_{3,LF}$	1800 pF
$R_2$	160 Ω
$R_{3,LF}$	180 Ω



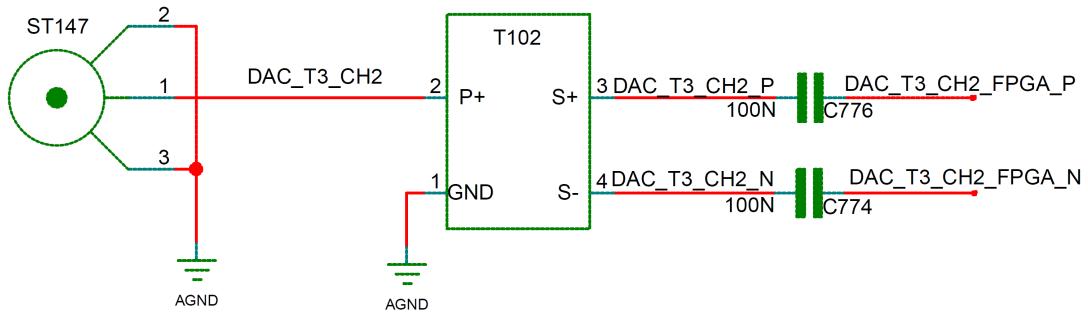
**Figure 4.13.:** Schematics of the LMX2594

#### 4.1.5. Digital-To-Analog-Converter Channels

For test purposes, two DAC channels from the read-out card are routed on the sampling board. In this way, test signals can be generated right on the read-out card, without the need for an external signal generator. The differential inputs from the DACs are transformed into single ended outputs with dedicated baluns<sup>5</sup>. the BD3150N50100AHFa and the BD4859N50100AHF from *Anaren*. These are used for the signal frequency range 3.1 GHz to 5.0 GHz and 4.8 GHz to 5.9 GHz respectively.

The single-ended output is connected to a miniature RF connector from *Hirose Electric*.

The schematic of a DAC channel is shown in Figure 4.14.



**Figure 4.14.:** DAC-channel with balun. Signal propagates from right to left.

#### 4.1.6. Power Supply

Stable power supply is the key for best performance of the components. Especially high-performance ICs, such as THAs, highly rely on a stable voltage level for correct functionality.

<sup>5</sup>balanced to unbalanced

Therefore, proper power supply design is an important step which needs to be handled with care. This step includes choosing the right type and amount of voltage regulators, as well as providing appropriate filtering.

Table 4.5 lists the power supply requirements of all the components used on the board.

**Table 4.5.: Power consumption of components on the board**

Component	$V_{cc}$ (V)	$I_{max}$ (A)	$P_{max}$ (W)	#parts	$I_{tot}^1$ (A)
HMC5649 (THA)	2	0.221	0.442	16	3.536
	-5	-0.242	1.21		3.872
NB6L295 (Delay chip)	2.5	0.170	0.425	8	1.36
HMC987LP5E (Fanout buffer)	3.3	0.234 <sup>2</sup>	0.772	2	0.468
LMK04808B (PLL)	3.3	0.590 <sup>3</sup>	1.947	1	0.590
LMX2594 (PLL)	3.3	0.340	1.122	2	2.244
VCXO	3.3	0.03	0.198	1	0.03

<sup>1</sup>for 16 ADCs

<sup>2</sup>All Outputs and RF-Buffer

<sup>3</sup>All CLKs

For general components, there are two power supply sources

- Voltage coming from FMC+ connector
- External power supplies (-5V)

An EMI filter needs to be placed in order to keep noise of the power supply and read-out card from the sampling board. This is not stable enough for the sensitive THA, therefore voltage regulators are needed. These are able to regulate the voltage to be stable.

### Power Supply for Track-and-Hold-Amplifiers

The THAs need a constant voltage level for optimal operation. To guarantee a stable voltage level, linear voltage regulators which are capable to maintain a stable output voltage, are to be used with the THAs.

On the KAPTURE sampling board, the Low Dropout Voltage Regulator (LDO) ADP1708 from *Analog Devices* is used to provide a power supply for the THAs. A LDO is able to operate at a low potential difference between the input and output voltage. This low potential difference has also the benefit of low power dissipation, which also This power supply can provide at maximum 1 A to the load. In order to minimize the amount of components needed on the board, i.e. to save space, a component which can provide higher currents should be used. This way, one single voltage regulator can be used for more components.

For the new board, the ADP1741 low-dropout voltage regulator from *Analog Devices* is used. This voltage regulator has adjustable output voltage from 1.6 V to 3.6 V and a maximum output current of 2 A.

With the given characteristics, it is now necessary to think about the amount of voltage regulators needed. As a rule of thumb, the power supply should provide twice the maximum power needed by the components it drives. [Mic] The power consumption/maximum current for the respective components on the sampling board is listed in ??.

It is necessary to think about the amount of voltage regulators needed. As a rule of thumb, the power supply should provide twice the maximum current (i.e. power) needed by the

components it drives. [Mic] The power consumption/maximum current for the THAs on is listed in ??.

The maximal current which the ADP1741 can provide @2 V is 2 A. This means, with one THA amplifier requiring a maximal current of 0.221 A, one ADP1741 can handle four units according to the rule mentioned beforehand:

$$I_{\max, \text{ADP1741}} = 2 \text{ A} > 2 * I_{\text{tot}} \quad (4.4)$$

$$I_{\text{tot}} = 4 \cdot 0.221 \text{ A} = 0.884 \text{ A} \quad (4.5)$$

## Delay Chips

The delay chips require 2.5 V. They carry sensitive clock signals, therefore also needs stable voltage levels. Two other voltage regulators are used, they are an easy way to generate the voltage and keep it stable. Two chips because of max. current draw from the chips.

## 4.2. Layout

The next step after schematic capture is the design of the layout. In this step, the board outline (“form”) is defined, the components are placed and traces between them are routed.

- Define layer number
- Choose substrate
- Calculate transmission line geometries for high frequency signals
- Place components following proper decoupling techniques
- Route traces, taking care that traces of the same group have same length. For sensitive signals take care that these are shielded by ground planes on the layers above and below.
- Places additional structures to reduce cross-talk, EMI, etc. (via fences, stitching vias)
- Create proper power distribution by placing copper planes at appropriate places.

For better understanding, first a general overview over PCB structures is given. Then the steps mentioned above are described.

### 4.2.1. PCB Structures Overview

In this section an overview over the basic structures on a PCB is given.

#### Traces

A *trace* is a strip of metal, which establishes an electrical connection and carries signals between two (or more) points in the horizontal plane of a PCB. [Xil]

#### Planes

*Plane* denotes an uninterrupted area of metal, which covers the whole PCB layer. If this area only covers a part of the layer, it is called a *planelet*. These areas provide power distribution across the PCB and present an important transmission medium for the return current<sup>6</sup>. [Xil]

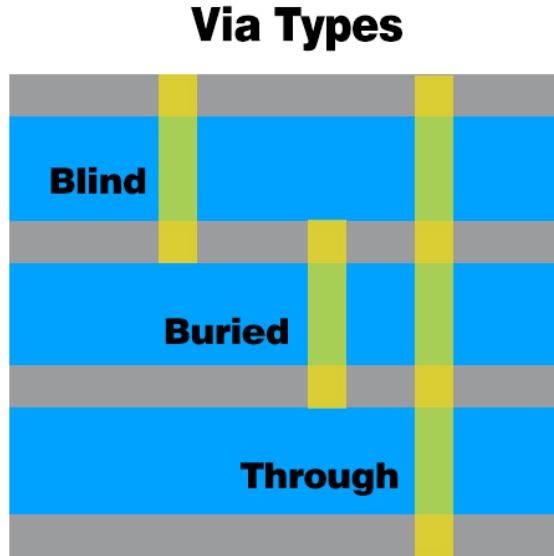
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<sup>6</sup>Any current, which is injected into the components/boards, needs a return path, as otherwise there is no closed circuit.

## Vias

A via is metal-plated hole, which is used to route a trace in vertical direction, i.e. from the PCB outer layer to the inner layers. They carry signals and power. Three types of vias are [our]:

- Blind via: A blind via connects the surface layers with at most three layers below.
- Buried via: A buried via only connects internal layers.
- Through via: A through via goes from one PCB surface to another and is used to connect any layer.



**Figure 4.15.:** Visualization of via types [our]

## TODO:

- Via fences
- Pads

In this design only blind and through vias are used.

### 4.2.2. PCB Substrate Selection and

TODO Megtron6 Laminate R-5775 Prepreg R-5670

$\epsilon_r = 3.61$  at 10 GHz,  $\epsilon_r = 3.71$  at 1 GHz

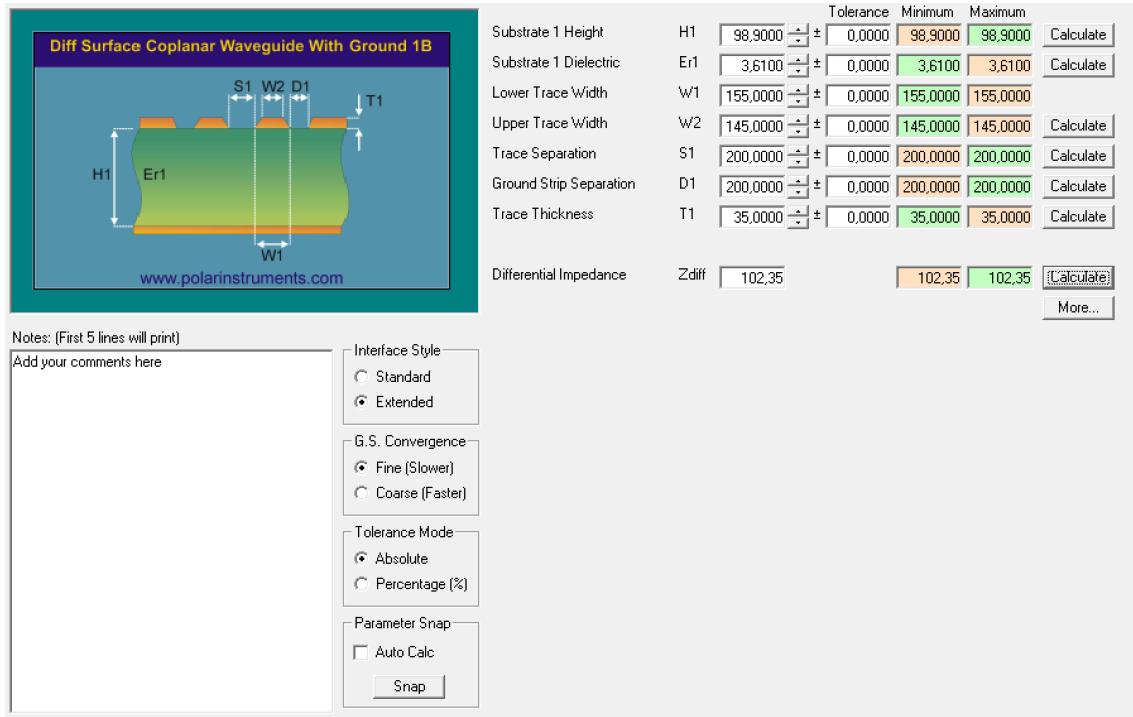
### 4.2.3. Transmission lines

TODO

Transmission lines carry high-frequency signals, therefore the geometry of them is important, as this affects the impedance. For single-ended the waveguide characteristic impedance should be  $50 \Omega$ , for differential signals  $100 \Omega$ . For slow signals not that crucial, but for sensitive, high-speed signals, e.g. clocking signals, proper calculation is very important to ensure signal integrity and reduce reflection and damping.

For PCBs usually coplanar waveguides are used for signal propagation. The characteristic impedance depends on the dielectric, the trace width, separation between traces and

separation between the signal traces and the ground planes/traces. Formulas to calculate the characteristic impedance are quite lengthy and not easy to solve. Luckily, tools<sup>7</sup> exist to quickly calculate the geometric values needed for appropriate impedance. For the design, the Si9000e PCB field solver from *Polar* (see Figure 4.16) is used to calculate the necessary trace widths, separations, etc.



**Figure 4.16.:** Screenshot of the Polaris Si9000e, showing calculation of characteristic impedance

Three geometries of waveguides are used in this design which are described in the following. Furthermore, geometric dimensions calculated with the Si9000e tool are presented. In principle, the geometries can be taken from the design of the sampling card of KAPTURE system. As the dielectric constant of the substrate is slightly different (KAPTURE: 3.52, here: 3.61), the impedance has to be recalculated to check whether the characteristic value impedance still lies in the 10 % tolerance.

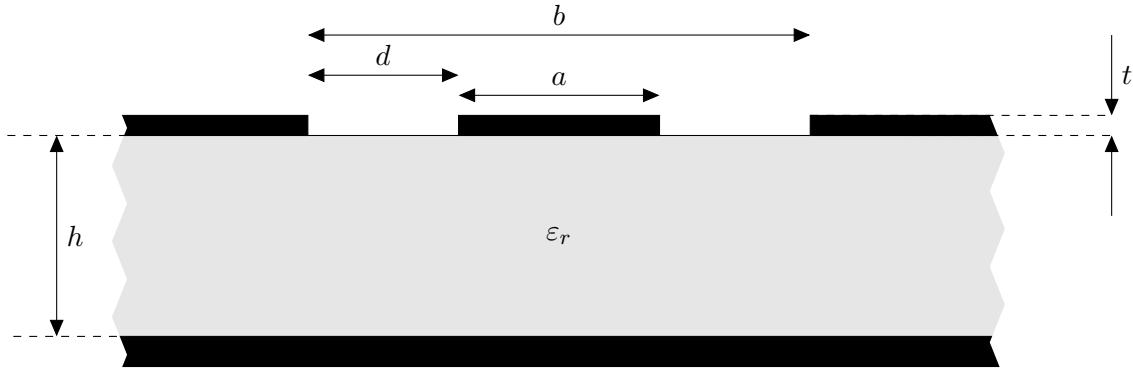
### Surface Coplanar Waveguide with Ground

The surface coplanar waveguide has the geometry shown in Figure 4.17. The single trace of thickness  $t$  and width  $a$  lies between two ground planes on a dielectric of thickness  $h$  and the effective dielectric constant  $\epsilon_r$ . Another ground plane is located at the bottom of the dielectric. Separation between trace and ground plane is defined as  $(b - a)/2 := d$ .

Trace width is assumed to be  $a = 180 \mu\text{m}$ . In the tool, an upper and a lower trace width can be specified, therefore taking into account manufacturing processes. As the exact upper trace width is not known, both are assumed to be  $180 \mu\text{m}$ . Trace-To-Ground Separation, or "Ground Strip Separation", is defined by the manufacturing technology of the PCB process:  $d = 250 \mu\text{m}$  With  $h = 98.9 \mu\text{m}$ ,  $\epsilon_r = 3.61$  (at 10 GHz) this results in a characteristic impedance of  $52.90 \Omega$ . This lies well in the tolerance area.

Over the frequency range, the value of the effective dielectric constant changes from 3.71 (at 1 GHz) to 3.61 (at 10 GHz). As the tool provides the possibility to calculate the impedance

<sup>7</sup>which are quite expensive though, if a high variety of geometries is necessary



**Figure 4.17.:** Coplanar Waveguide with Ground

versus a changing parameter, the influence of a changing dielectric was calculated. As can be seen in ??, with higher effective dielectric constant, the characteristic impedance decreases (see ??).

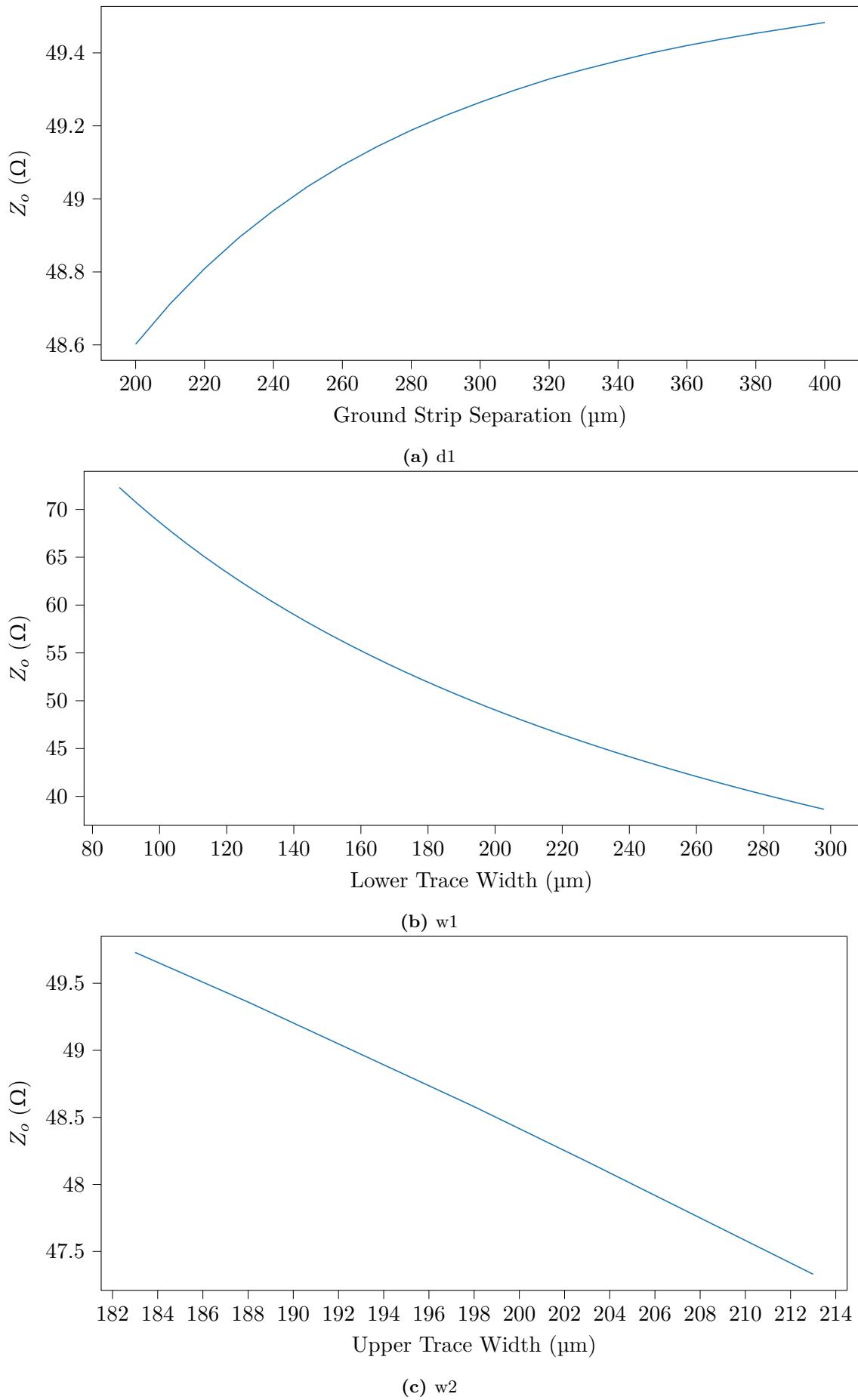
The only parameters, which are not defined by the manufacturing process and therefore can be altered, are the ground strip separation  $d$  and the trace width  $a$ . When altering the trace width, the tool automatically assumes an upper trace width, which is 25  $\mu\text{m}$ .

### Differential Pairs on Surface

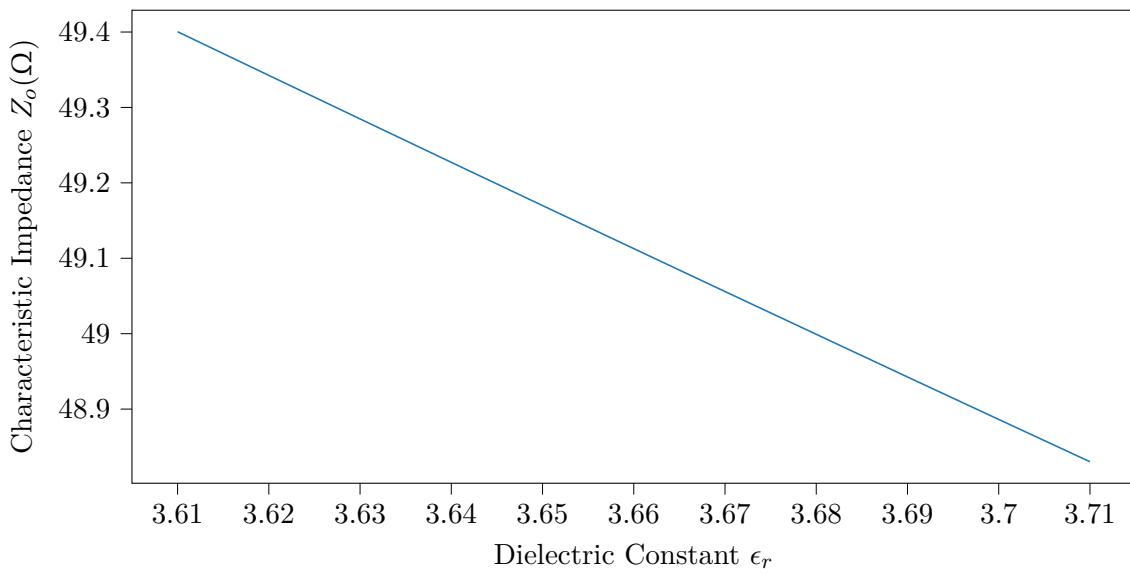
Some signals are propagated as differential pair traces on the PCB surface. Together with the surrounding ground plane and the ground plane on the layer below, these traces thus form the geometry of an edge-coupled coplanar waveguide (see Figure 4.20). The formulas to calculate the characteristic impedance of this waveguide type is listed in section A.

### Differential Pairs between Layers

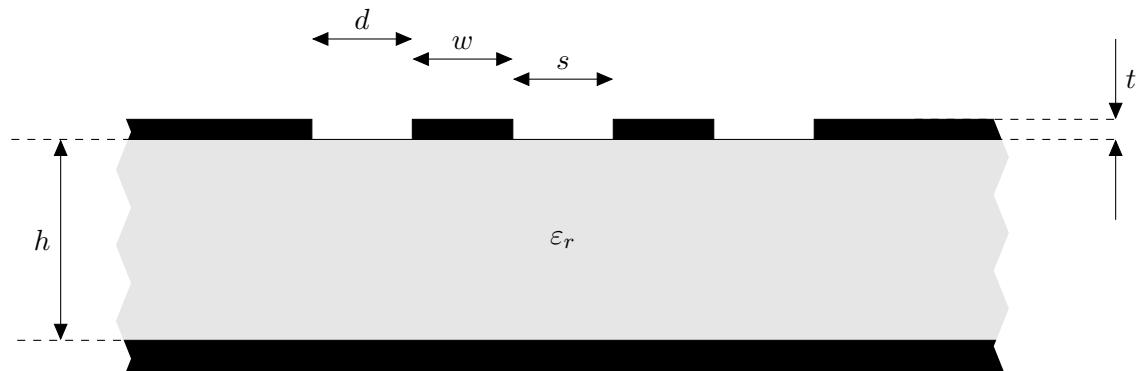
The analog signals from the THAs, as well as the clock signals, are propagated through differential pair traces on the inner layers of the PCB. This forms an offset coplanar waveguide as seen in Figure 4.21.



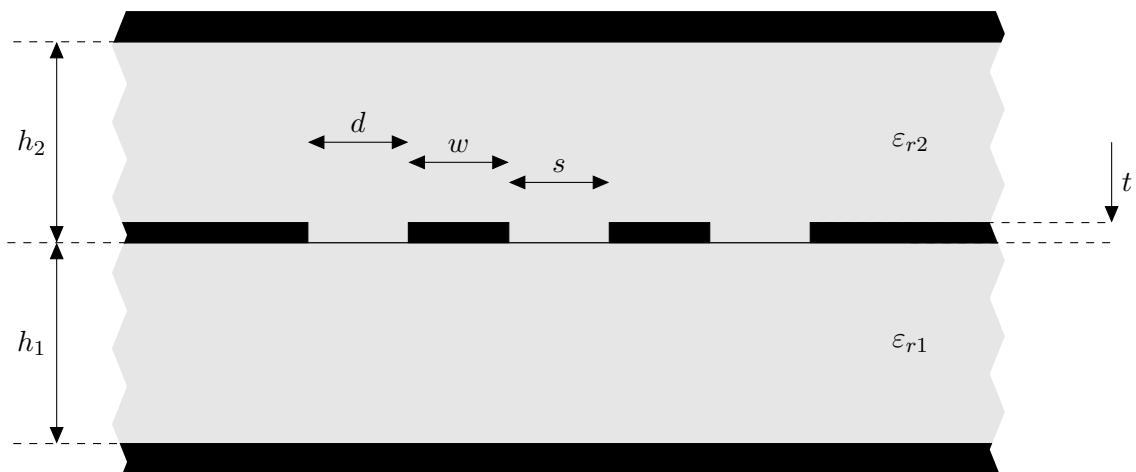
**Figure 4.18.:** Characteristic impedance of surface coplanar waveguide versus different parameters



**Figure 4.19.:** Characteristic impedance  $Z_o$  of a coplanar waveguide versus dielectric constant  $\epsilon_r$



**Figure 4.20.:** Edge-Coupled Coplanar Waveguide



**Figure 4.21.:** Offset Differential Coplanar waveguide

#### 4.2.4. Component Placement and Routing

## **5. Analyzing the Back-End Readout Card**



## 6. Results



## 7. Conclusion and Outlook

There is a disturbing lack of benches in Ramset Park Campus North. I want to sit more!



### 7.1. Expectation vs. Reality

At least I wrote more than 273 words.



(a) How you think you will feel like at the end of your master studies.



(b) How you actually feel like.

**Figure 7.1.:** Expectation vs. Reality

## 7.2. The board

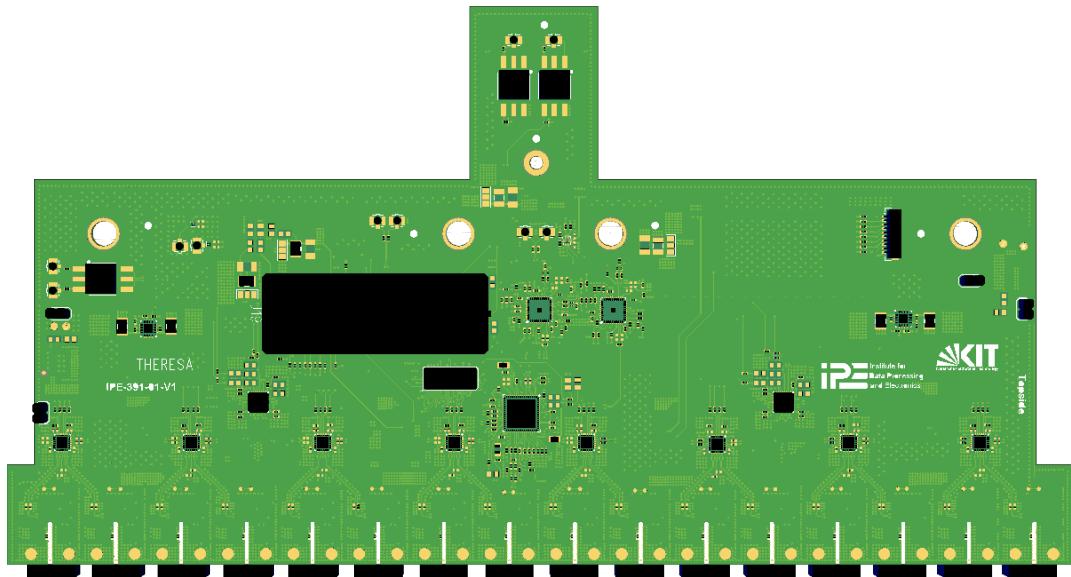


Figure 7.2.: THERESA



## Acknowledgments



# Appendix

## A. Characteristic Impedance Of Coplanar Waveguides

### Edge-Coupled Coplanar Waveguide

Characteristic impedance[Wad91, p197-198]:

$$Z_{0,o} = \frac{\eta_0}{\sqrt{\epsilon_{\text{eff},o}}} \left( \frac{1.0}{2.0 \frac{K(k_o)}{K'(k_o)} + \frac{K(\beta_1)}{K'(\beta_1)}} \right) \quad (\text{A.1})$$

$$Z_{0,e} = \frac{\eta_0}{\sqrt{\epsilon_{\text{eff},e}}} \left( \frac{1.0}{2.0 \frac{K(k_e)}{K'(k_e)} + \frac{K(\beta_1 k_1)}{K'(\beta_1 k_1)}} \right) \quad (\text{A.2})$$

$$\epsilon_{\text{eff},o} = \frac{2.0 \epsilon_r \frac{K(k_o)}{K'(k_o)} + \frac{K(\beta_1)}{K'(\beta_1)}}{2.0 \frac{K(k_o)}{K'(k_o)} + \frac{K(\beta_1)}{K'(\beta_1)}} \quad (\text{A.3})$$

$$\epsilon_{\text{eff},e} = \frac{2.0 \epsilon_r \frac{K(k_e)}{K'(k_e)} + \frac{K(\beta_1 k_1)}{K'(\beta_1 k_1)}}{2.0 \frac{K(k_e)}{K'(k_e)} + \frac{K(\beta_1 k_1)}{K'(\beta_1 k_1)}} \quad (\text{A.4})$$

with

$$k_o = \Lambda \frac{-\sqrt{\Lambda^2 - t_c^2} + \sqrt{\Lambda^2 - t_B^2}}{t_B \sqrt{\Lambda^2 - t_c^2} + t_c \sqrt{\Lambda^2 - t_B^2}} \quad (\text{A.5})$$

$$k_e = \Lambda' \frac{-\sqrt{\Lambda'^2 - t_c'^2} + \sqrt{\Lambda'^2 - t_B'^2}}{t_B' \sqrt{\Lambda'^2 - t_c'^2} + t_c' \sqrt{\Lambda'^2 - t_B'^2}} \quad (\text{A.6})$$

$$\Lambda = \frac{\sinh^2 \left( \frac{\pi(s/2.0+w+d)}{2.0h} \right)}{2} \quad (\text{A.7})$$

$$t_c = \sinh^2 \left( \frac{\pi(s/2.0+w)}{2.0h} \right) - \Lambda \quad (\text{A.8})$$

$$t_B = \sinh^2 \left( \frac{\pi s}{4.0h} \right) - \Lambda \quad (\text{A.9})$$

$$\Lambda' = \frac{\cosh^2 \left( \frac{\pi(s/2.0+w+d)}{2.0h} \right)}{2} \quad (\text{A.10})$$

$$t'_c = \sinh^2 \left( \frac{\pi(s/2.0 + w)}{2.0h} \right) - \Lambda' + 1.0 \quad (\text{A.11})$$

$$t'_B = \sinh^2 \left( \frac{\pi s}{4.0h} \right) - \Lambda + 1.0 \quad (\text{A.12})$$

The parameters have to be chosen according to

$$s + 2.0w + 2.0d \leq h \quad (\text{A.13})$$

to guarantee coplanar propagation. [Wad91]

### Surface Coplanar Waveguide with Ground

The characteristic impedance of a coplanar waveguide is given as (see [Wad91])

$$Z_0 = \frac{60.0\pi}{\sqrt{\epsilon_{\text{eff}}}} \frac{1.0}{\frac{K(k)}{K(k')} + \frac{K(k_1)}{K(k'_1)}}. \quad (\text{A.14})$$

It comprises of the following components, with  $K(k)$  being an elliptical integral of the first kind (see also [BSMM99, p. 430]):

$$k = a/b \quad (\text{A.15})$$

$$k' = \sqrt{1.0 - k^2} \quad (\text{A.16})$$

$$k_1 = \frac{\tanh(\frac{\pi a}{4.0h})}{\tanh(\frac{\pi b}{4.0h})} \quad (\text{A.17})$$

$$k'_1 = \sqrt{1.0 - k_1^2} \quad (\text{A.18})$$

$$\epsilon_{\text{eff}} = \frac{1.0 + \epsilon_r \frac{K(k')}{K(k)} \frac{K(k_1)}{K(k'_1)}}{1.0 + \frac{K(k')}{K(k)} \frac{K(k_1)}{K(k'_1)}} \quad (\text{A.19})$$

## B. QuickStart Guide for Evaluation of ZCU216 Board

### C. 3D model of front-end card

### D. Code

```
'timescale 1ns / 1ps

module SDI_Delay_NB6L295(
    input [10:0]           In_1, In_2, In_3, In_4, In_5, In_6, In_7, In_8, // 
                           data for respective delay chips
    input                  Clk,
    input                  Reset,
    output reg [7:0]        EN, // enable signal for delay chips, active LOW
    output reg              SDIN, // configuration data
    output reg              SLOAD, // signals delay chip to load previously sent
                           data
    output                 SCLK // clock for serial communication with delay chips
);

reg                      start_clk;
assign SCLK = start_clk & (!Clk);
```

```

reg [21:0] In_1_reg, In_2_reg, In_3_reg, In_4_reg, In_5_reg,
In_6_reg, In_7_reg, In_8_reg; // registers to intermediately store the
inputs

reg [7:0] select; // register used by Priority Encoder to detect
which input changed

parameter DATA_SHIFT_WIDTH = 11; // number of bits to be shifted
during transmission, 1 Data word = 11 bits
reg [4:0] clk_cnt;

reg [DATA_SHIFT_WIDTH-1:0] Data_reg; // register for storing data for
state machine

reg start; // signal for state machine to start sending
reg data
reg dataSent; // flags if transmission for one delay chip
is finished

parameter dly = 1; // delay control

reg delayReady;

always @ (posedge Clk)
begin
    if (select == 'd0) delayReady <= #dly 'b1;
    else delayReady <= #dly 'b0;
end

// Priority Encoder
// Check if any input has changed, select which data should be sent
accordingly
always @ (posedge Clk)
begin
    if (Reset)
        begin
            In_1_reg <= #dly 'd0;
            In_2_reg <= #dly 'd0;
            In_3_reg <= #dly 'd0;
            In_4_reg <= #dly 'd0;
            In_5_reg <= #dly 'd0;
            In_6_reg <= #dly 'd0;
            In_7_reg <= #dly 'd0;
            In_8_reg <= #dly 'd0;
            Data_reg <= #dly 'd0;

            select <= #dly 'd0;

            start <= #dly 1'b0;;
        end
    else
        begin
            if (~start & delayReady)
                begin
                    select[7] <= #dly In_1_reg != In_1;
                    select[6] <= #dly In_2_reg != In_2;
                    select[5] <= #dly In_3_reg != In_3;
                    select[4] <= #dly In_4_reg != In_4;
                    select[3] <= #dly In_5_reg != In_5;
                    select[2] <= #dly In_6_reg != In_6;
                    select[1] <= #dly In_7_reg != In_7;
                    select[0] <= #dly In_8_reg != In_8;
                end
        end
    end

```

```

        end
    else
        begin
            if (clk_cnt == 4'd12 & ~start_clk) // = end of
                sequence
                    start          <= #dly 1'b0;
            else
                start          <= #dly 1'b1;
        end

    casex (select)
        8'b1???????: begin
            if (~dataSent)
                begin
                    In_1_reg      <= #dly In_1;
                    Data_reg       <= #dly In_1;
                    EN             <= #dly
                        8'b01111111;
                    start          <= #dly 1'b1;
                end
            else
                begin
                    start          <= #dly 1'b0;
                    select [7]     <= #dly 1'b0;
                end
        end
        8'b01???????: begin
            if (~dataSent)
                begin
                    In_2_reg      <= #dly In_2;
                    Data_reg       <= #dly In_2;
                    EN             <= #dly
                        8'b10111111;
                    start          <= #dly 1'b1;
                end
            else
                begin
                    select [6]     <= #dly 1'b0;
                    start          <= #dly 1'b0;
                end
        end
        8'b001?????: begin
            if (~dataSent)
                begin
                    In_3_reg      <= #dly In_3;
                    Data_reg       <= #dly In_3;
                    EN             <= #dly
                        8'b11011111;
                    start          <= #dly 1'b1;
                end
            else
                begin
                    select [5]     <= #dly 1'b0;
                    start          <= #dly 1'b0;
                end
        end
        8'b0001????: begin
            if (~dataSent)
                begin
                    In_4_reg      <= #dly In_4;

```

```

Data_reg          <= #dly In_4;
EN               <= #dly
8'b11101111;    <= #dly 1'b1;
start            <= #dly 1'b1;
end

else
begin
  select [4]      <= #dly 1'b0;
  start           <= #dly 1'b0;
end
end
8'b00001???: begin
if (~dataSent)
begin
  In_5_reg        <= #dly In_5;
  Data_reg         <= #dly In_5;
  EN               <= #dly
  8'b11110111;    <= #dly 1'b1;
  start            <= #dly 1'b1;
end

else
begin
  select [3]      <= #dly 1'b0;
  start           <= #dly 1'b0;
end
end
8'b000001???: begin
if (~dataSent)
begin
  In_6_reg        <= #dly In_6;
  Data_reg         <= #dly In_6;
  EN               <= #dly
  8'b11111011;    <= #dly 1'b1;
  start            <= #dly 1'b1;
end

else
begin
  select [2]      <= #dly 1'b0;
  start           <= #dly 1'b0;
end
end
8'b0000001?: begin
if (~dataSent)
begin
  In_7_reg        <= #dly In_7;
  Data_reg         <= #dly In_7;
  EN               <= #dly
  8'b11111101;    <= #dly 1'b1;
  start            <= #dly 1'b1;
end

else
begin
  select [1]      <= #dly 1'b0;
  start           <= #dly 1'b0;
end
end
8'b00000001: begin

```

```

        if (~dataSent)
        begin
            In_8_reg           <= #dly In_8;
            Data_reg           <= #dly In_8;
            EN                 <= #dly
                                8'b11111110;
            start              <= #dly 1'b1;
        end
        else
            begin
                select [0]      <= #dly 1'b0;
                start             <= #dly 1'b0;
            end
        end
    default:
        begin
            EN                 <= #dly
                                8'b11111111;
            start              <= #dly 1'b0;
        end
    endcase
end
/*
// State Machine for Sending Configuration Data to Delay Chip NB6L295
/*
   State          Description
   -----
RESET           Resetting all parameters and registers ->
               if (reset): stay; else: to IDLE
IDLE            Waiting for start signal from priority
               encoder -> if (start): to LOAD_P0; else: stay
LOAD_P0          Load first half of Delay_X - which
               corresponds to data for Delay PD0 on delay chip - into
               temporary register -> to LOAD_P1
LOAD_P1          Load second half of Delay_X - which
               corresponds to data for Delay PD1 on delay chip - into
               temporary register -> to SHIFT
SHIFT            Shift bits for sending serial bitstream to
               SDIN, assert SLOAD -> to END
END              End transmission, deassert SLOAD, inform
               priority encoder about end of transmission -> to IDLE
*/
parameter RESET      = 3'd0;
parameter IDLE       = 3'd1;
parameter LOAD        = 3'd2;
parameter SHIFT       = 3'd3;
parameter END         = 3'd4;
reg [2:0] STATE;
reg [DATA_SHIFT_WIDTH-1:0]     tmp;

always @ (posedge Clk)
begin
    if (Reset)
        begin
            STATE      <= #dly RESET;
            tmp        <= #dly 'd0;
            dataSent   <= #dly 1'b0;
            start_clk  <= #dly 1'b0;
            SLOAD      <= #dly 1'b0;
            clk_cnt    <= #dly 1'b0;
        end
end

```

```

else
begin
  case (STATE)
    RESET:
      begin
        if (Reset)
          STATE    <= #dly RESET;
        else
          STATE    <= #dly IDLE;
      end // RESET
    IDLE:
      begin
        SDIN      <= #dly 1'b0;
        clk_cnt   <= #dly 5'd0;
        dataSent  <= #dly 1'b0;
        SLOAD     <= #dly 1'b0;

        if (start & ~dataSent)
          STATE    <= #dly LOAD;
        else
          STATE    <= #dly IDLE;
      end // IDLE
    LOAD:
      begin
        tmp       <= #dly Data_reg;
        STATE    <= #dly SHIFT;
      end // LOAD_W1
    SHIFT:
      begin
        if (clk_cnt < 4'd12) // number of bits to be
        shifted //
        begin
          start_clk    <= #dly 1'b1;
          clk_cnt      <= #dly clk_cnt +1;
          tmp         <= #dly
                      {tmp[DATA_SHIFT_WIDTH-2:0], 1'b0};
          SDIN        <= #dly
                      tmp[DATA_SHIFT_WIDTH-1];
        end
        else
          begin
            SLOAD      <= #dly 1'b1;
            clk_cnt    <= #dly
                        clk_cnt;
            start_clk  <= #dly 1'b0;
            STATE      <= #dly END;
            SDIN        <= #dly 1'b0;
          end
      end // SHIFT
    END:
      begin
        SLOAD      <= #dly 1'b0;
        start_clk  <= #dly 1'b0;
        dataSent   <= #dly 1'b1;
        clk_cnt    <= #dly clk_cnt;
        SDIN        <= #dly 1'b0;
        STATE      <= #dly IDLE;
      end // END
    default:
      STATE    <= #dly RESET;
  endcase
end

```

**endmodule**

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