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AND INFORMATION TECHNOLOGY
Institute for Data Processing and Electronics (IPE)

A Terabit Sampling System with a Photonics Time-Stretch ADC

Master Thesis
of

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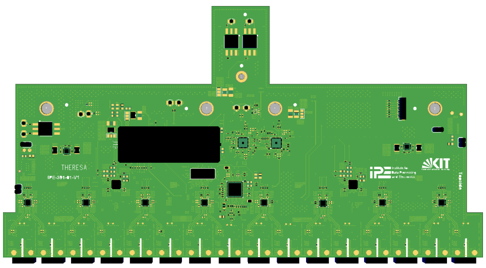
at the Institute for Data Processing and Electronics (IPE)



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Declaration

I hereby declare that I wrote my master thesis on my own and that I have followed the regulations relating to good scientific practice of the Karlsruhe Institute of Technology (KIT) in its latest form. I did not use any unacknowledged sources or means, and I marked all references I used literally or by content.

Karlsruhe, 13.08.2021, ____________________________

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Prof. Dr. Anke-Susanne Müller (LAS)

Abstract

Zusammenfassung

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Acronyms

AC Alternating Current. 32, 42

ADC Analog-To-Digital-Converter. 1–5, 7–12, 18, 20, 24–29, 32, 35, 39, 44, 50, 73

CML Current Mode Logic. 39

CSR Coherent Synchrotron Radiation. 1, 2, 15, 16

DAC Digital-To-Analog-Converter. 35, 44, 49

DAQ Data Acquisition System. 1, 2, 18, 19, 21, 73

dBc decibels relative to the carrier. 9

dBFS decibels relative to full scale. 9

DC Direct Current. 41

DDR Double Data Rate. 21

DMA Direct-Memory-Access. 21

DNL Differential Nonlinearity. 7

EMI Electro-Magnetic Interference. 32, 47, 50, 54, 64

ENOB Effective-Number-Of-Bits. 1, 8–10

EO Electro-Optic. 2, 16, 17

ESL Equivalent-Series-Inductance. 33

ESR Equivalent-Series-Resistance. 32, 33

FMC FPGA Mezzanine Card. 34, 35, 39–41, 44, 47, 49, 50, 53

FPGA Field Programmable Gate Array. 2, 18–20, 34, 35, 44, 67, 73

FS Full-Scale. 37

FWHM Full Width At Half Maximum. 19

HSPCe High Serial Pin Count Extension. 34

IC Integrated Circuit. 29, 32, 50, 64

INL Integral Nonlinearity. 7

IPE Institute for Data Processing and Electronics. 19, 20

KAPTURE Karlsruhe Pulse Taking Ultra-fast Readout Electronics. xi, 19, 20, 37, 39, 44, 51, 56, 57

KARA Karlsruhe Research Accelerator. 15, 19, 20, 36, 44

LDO Low Dropout Voltage Regulator. 51, 52

LINAC linear accelerator. 14

LNA Low-Noise-Amplifier. 19, 20

LPAF Low Profile Array, Female. 35

LPAM Low Profile Array, Male. 35, 37

LSB Least Significant Bit. 3, 4, 6, 7, 12

LVDS Low Voltage Differential Signaling. 31

LVPECL Low-Voltage Positive Emitter-Coupled Logic. 39, 41, 48

MMIC Microwave Monolithic Integrated Circuit. 20

PCB Printed Circuit Board. xi, 31, 32, 34, 38, 53–57, 60

PCIe PCI Express. 21

PLL Phase-Locked-Loop. 20, 35, 36, 39, 44–48, 50, 64

RF Radio Frequency. 14, 20, 34–36, 49, 64

RFSoC Radio-Frequency System-On-Chip. 73

RMS Root-Mean-Square. 8, 9, 11, 42

SDI Serial Data Interface. 39

SFDR Spurious-Free Dynamic Range. 9, 10

SHA Sample-And-Hold-Amplifier. 4, 5, 7, 8, 10

SINAD Signal-to-Noise-and-Distortion Ratio. 8–10

SJNR Signal-to-Jitter-Noise-Ratio. 11

SMA SubMiniature version A. 34, 35

SNR Signal-To-Noise-Ratio. 6, 9, 11

SoC System-On-Chip. 18, 73

SPI Serial Peripheral Interface. 31, 34, 48, 49

SR Synchrotron Radiation. xiii, 14, 16

THA Track-And-Hold-Amplifier. 4, 5, 19, 20, 28, 32, 34, 37–39, 41, 42, 44, 48, 50–54, 56, 60, 64, 65

THz Tera Hertz. 1, 2, 14, 16, 19, 20

VCO Voltage-Controlled Oscillator. 45

VCXO Voltage-Controlled Crystal Oscillator. 44

VITA VMEbus International Trade Association. 34

1. Introduction

In many scientific applications and experiments the observation of non-repetitive, statistically rare occurrences is desired to gather valuable information about the system producing these events. As these events occur on a time range of femtoseconds, real-time measurement systems with fine temporal resolution and long record lengths are necessary. This imposes high technological challenges on Analog-To-Digital-Converters (ADCs) and Data Acquisition Systems (DAQs) in general.

One bottleneck in acquisition of ultra-fast events is the limited performance of the ADCs. The limitation posed by the converters is the trade-off between the dynamic range (Effective-Number-Of-Bits (ENOB)) and sampling rate of the converters. As the sample rate increases, comparator ambiguity and sampling errors due to clock jitter become the major limitation factors on the overall performance. [MCB$^+$17]

A first demonstration of a concept to overcome these limitations was done in 1999 by F. Coppinger, A. S. Bhushan and B. Jalali. The idea is to stretch the signal in time before digitizing it in the converter and in this way relaxing the demands on the ADCs performance. This time-stretch accomplished by using chirped optical pulses and dispersion in optical fibers. The concept is therefore called "photonic time-stretch" and was successfully tested in combination with an ADC. [CBJ99]

Since then, the time-stretch method was continuously studied and improved and has found potential usage in many application fields. For example in biomedical diagnostics, a first demonstration of an artificial intelligence facilitated high-speed phase microscope has been done. It uses the time-stretch quantitative phase imaging (TS-QPI), a technique based on the time-stretch concept which enables simultaneous measurement of phase and spatial intensity profiles. This allows label-free classification of cells essential to cancer diagnostics and drug development.

The time-stretch concept is also very interesting for particle accelerator applications. Relativistic electron bunches interact with their own radiation which leads to spatial microstructures inside of the bunches, also called micro-bunching instabilities. They are a source of intense pulses of Tera Hertz (THz) radiation (Coherent Synchrotron Radiation (CSR)) and therefore an important field of study. A first demonstration of direct observation of these instabilities was done at the synchrotron facility SOLEIL[1] using the time-stretch method together with a real-time oscilloscope. [RELP$^+$15]

While the integration of the time-stretch method in different applications has given the possibility to measure events in femtosecond resolution, one major limitation still exists. Commercially available real-time measurement equipment is limited in memory space, i.e. it is not possible to measure data continuously over a large range of time. This creates a problem in applications where a long observation time is important, e.g. in accelerator application where the turn-by-turn analysis of the electron bunches is desired.

[1]Source optimisée de lumière d'énergie intermédiaire du LURE

This challenge creates a stimulus for the design of novel ultra-fast acquisition systems based on the photonic time-stretch ADC principle. Paired with next generation, Field Programmable Gate Array (FPGA)-based systems with integrated high-performance ADCs, this gives rise to a new concept of DAQ, the photonic time-stretch DAQ. A photonic time-stretch DAQ consists of a photonic part, which covers the time-stretching method and conversion of photons into electrical values with a photo-detector. Furthermore, such a system has an ADC (or multiple ADCs) which converts the analog values into digital signals that can be processed by a computing unit. This unit should have a sufficient memory depth and be capable of high data-throughput.

In this thesis, a first demonstrator of a DAQ-system based on the time-stretch concept is developed.

This system should enable high-speed measurement of ultrafast event with a resolution in the range of femtoseconds. The input signal should be continuously sampled by high-speed ADCs with a temporal resolution which can be defined by the user. In order to guarantee a large memory depth and high data-throughput, the system should be based on a new generation of System-On-Chip (SoC) paired with an FPGA. The SoC should have high-speed peripherals in order to guarantee high-speed data-throughput. The use with FPGA should enable flexible adjustment of the system for the user-defined application.

Furthermore, the system should be compatible with already existing high-speed DAQ frameworks and be easily integrable into the system of the user application. The DAQ should provide the flexibility to be also used without the time-stretch method. One use case of the system (see Figure 1.1) is to replace commercial oscilloscopes which are currently used for measurements.

Potential use of the DAQ system in the industry should also be considered.

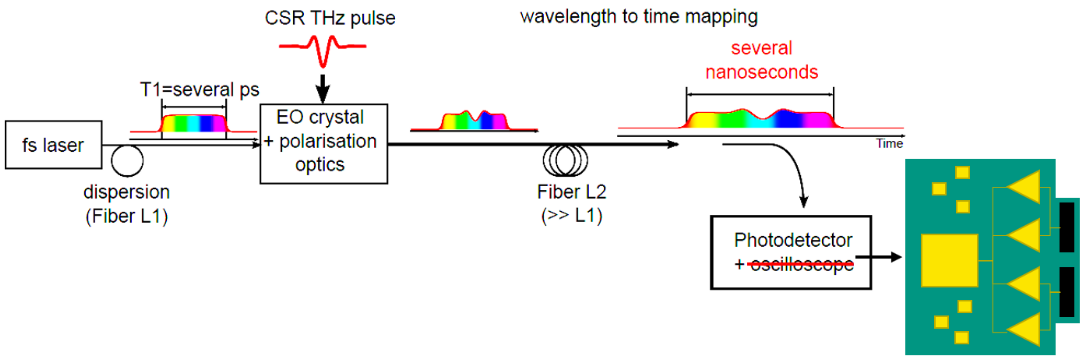


Figure 1.1.: Use case of the time-stretch photonic DAQ. The system should replace commercially available oscilloscopes and improve the performance in terms of resolution and memory depth.

The following section covers the general architecture and basic theory of a photonic time-stretch DAQ. First, the basic working principle of the time-stretch concept is explained. Then, a short overview of the basic ADC-theory is given, together with the most prominent figures of merit. Knowledge and understanding of ADC-characteristics is necessary to define and/or evaluate the overall performance of the converter.

As the main aspired use case of the newly developed time-stretch DAQ lies in accelerator applications, especially in THz science e.g. at the Karlsruhe Research Accelerator (KARA), a brief introduction into this topic is given at the end.

1.1. Photonic Time-Stretch Method

The working principle of the optic time-stretch technique can be described in three steps (see Figure 1.2).

First, a short laser pulse (duration typically hundreds of femtoseconds) propagates in a dispersive medium, e.g. an optical fiber of length L_1 (see Figure 1.2). With the optical bandwidth of the laser pulse $\Delta\lambda$ and the dispersion parameter D_1 of the fiber this results in a chirped laser pulse of the duration

$$T_1 = \Delta\lambda D_1 L_1. \tag{1.1}$$

The next step is the time-to-wavelength-mapping, where a temporal intensity modulation is imprinted on the chirped pulse. This happens when the laser pulse co-propagates with another pulse, e.g. a Tera Hertz (THz) pulse from Coherent Synchrotron Radiation (CSR) (duration in the range of picoseconds), in an Electro-Optic (EO) crystal. Due to the Pockels effect the THz pulse causes a time-dependent birefringence in the crystal. The Pockels effect describes the phenomenon of occurring and change of existing birefringence in an electric field, which is linearly proportional to the electric field strength.[Gmb]

After that, the modulated chirped pulse propagates through another dispersive medium, a fiber of the length L_2. In this way, the temporal modulation of the pulse is further stretched to the duration T_2, which is long enough for detection with photodetectors and the digitizing with Analog-To-Digital-Converters (ADCs). [Rou14]

The factor M, by which the pulse is slowed down, is calculated as

$$M = 1 + \frac{L_2}{L_1}. \tag{1.2}$$

As example, assume the length of the dispersive media as $L_1 = 10\,\text{m}$ and $L_2 = 2\,\text{km}$ and an input signal with the duration $t_{\text{sig}} = T_1 = 1\,\text{fs}$. With Equation 1.2 the stretching factor for this set-up is $M \approx 200$. The input pulse is stretched to $T_2 = M \cdot T_1 = 200 \cdot 1\,\text{fs} = 200\,\text{fs} = 0.2\,\text{ns}$. This corresponds to a frequency of 5 GHz which is much easier to handle e.g. for an oscilloscope.

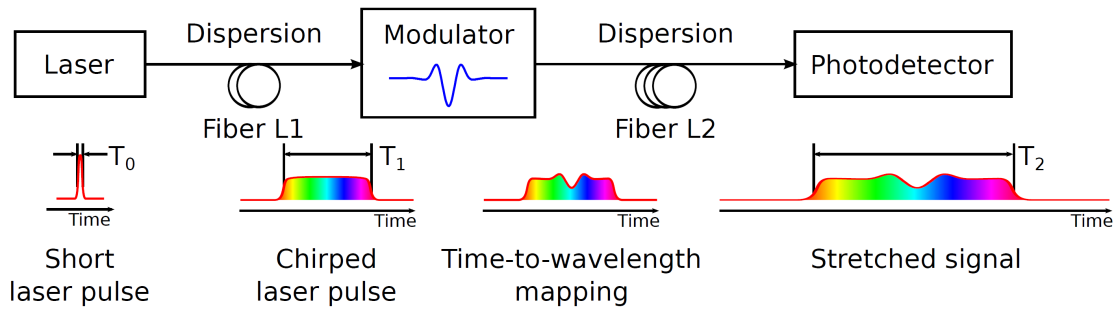


Figure 1.2.: Working principle of the electro-optical time-stretch technique [Rou14]

In order to convert the time-stretched optical signal into an electrical value a photodetector, or photodiode, is needed. A basic photodiode is a diode, which is operated in reverse bias, meaning the p-side is connected to the negative terminal and the n-side to the positive terminal of the power supply. This enlarges the depletion region of the p/n-junction (the depletion region contains only a very small amount of free charge carriers). Irradiating photons generate electron-hole pairs due to the photoelectric effect. The photoelectric effect denotes the phenomenon of emission of electrons when photons of a sufficient energy hits a material. If the electron-hole pairs are produced in the depleted region of the p/n-junction, they are separated by the electric field applied across the diode, before they can recombine. This creates a so called photo-current which can be measured. [Ele]

1.2. Analog-To-Digital Converter

ADCs are used to translate analog signals, like voltages, into the digital representation of these signals. This *digitized* version can then be stored and processed by information processing, computing, data transmission and control systems. This translation, also called "conversion", can be seen as encoding a continuous-time analog input V_{in} (voltage) into a series of discrete, N-bit words. This process is also called *sampling.* With the full-scale voltage of the V_{FS}, the individual output bits b_k and the quantization error ϵ, the ADC should satisfy the relation

$$V_{\text{in}} = V_{\text{FS}} \sum_{k=0}^{N-1} \frac{b_k}{2^{k+1}} + \epsilon. \tag{1.3}$$

This can also be rewritten in terms of the Least Significant Bit (LSB) or quantum level V_Q

$$1\text{LSB} = \frac{V_{\text{FS}}}{2^N} = V_Q. \tag{1.4}$$

With Equation 1.3 this leads to

$$V_{\text{in}} = V_Q \sum_{k=0}^{N-1} b_k 2^k + \epsilon. \tag{1.5}$$

Figure 1.3 shows the ideal transfer function of a 3-bit ADC. As one can see, each digital N-bit word corresponds to a range of input voltage values (*code width*), which is centered around a *code center.* The input voltage is resolved to the code of the nearest code center.

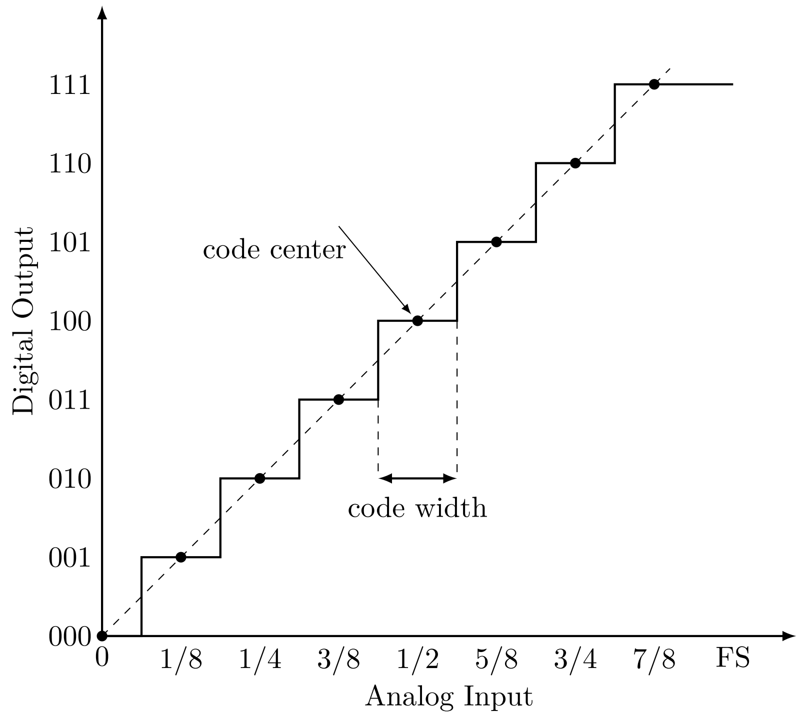


Figure 1.3.: Transfer function of an ideal, 3-bit ADC (redrawn from [LV02])

Sample-And-Hold-Amplifier

ADCs need a certain amount of time to sample the input signal. If the level of the analog signal changes by more than one LSB during this period, this can result in large errors in the output signal. Therefore, so called Sample-And-Hold-Amplifier (SHA) are used in front of the ADC to hold the input level constant for the needed amount of time.

A general block diagram of a SHA is shown in Figure 1.5. It consists of an input and output buffer, a switch controlled by the sampling clock and a capacitor. The analog input is buffered in an input buffer which leads to a switch that is controlled by a sampling clock. During the sample mode, i.e. during the negative sampling clock cycle, the switch is open. At the transition from negative to positive clock cycle, the switch closes, connecting the input signal with the capacitor which is charged in this way.

The ADC sampling time needs to be timed in such way, that the whole duration of an analog-to-digital conversion falls into the hold period of the SHA and does not exceed into the sample period. Figure 1.4 shows a qualitative example for proper sample timing. As conclusion, the upper frequency limitation is not determined by the ADC itself, but rather by the aperture jitter, bandwidth, distortion, etc. of the SHA. [Kes05]

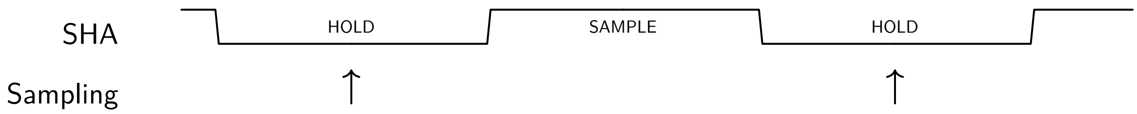


Figure 1.4.: Example for appropriate sampling timing when using Sample-And-Hold-Amplifier. The sample points of the ADC should be inside the period, where the SHA holds the input value.

Apart from the SHAs there also exists the so called Track-And-Hold-Amplifier (THA). Though the names are often used interchangeably, there exists one fundamental difference between a SHA and a THA. Strictly speaking, the output of a SHA is not defined during the sample period. Only when switching to the hold mode, the output is assigned to a defined value: the voltage level at the input in that moment. Contrary to that, the THA acts as a unity gain amplifier during the sample period, meaning the output is just a replication the input. The THA “tracks” the input signal (see also Figure 1.4). Therefore, instead of speaking of a “sample” period, the term used here is the “track” period. When switching to hold mode, the instantaneous input level is held over the course of the hold period. This principle allows to improve the sampling rate, as the settling time of an THA is in general smaller than one of a SHA. Settling time denotes the amount of time needed for the output voltage to be at a stable level, after the transition from track/sample to hold mode. This process is quicker, when the output voltage is already in the range of the sampled input at the moment, instead of when the capacitor first has to be charged up to the input voltage. [Ree17]

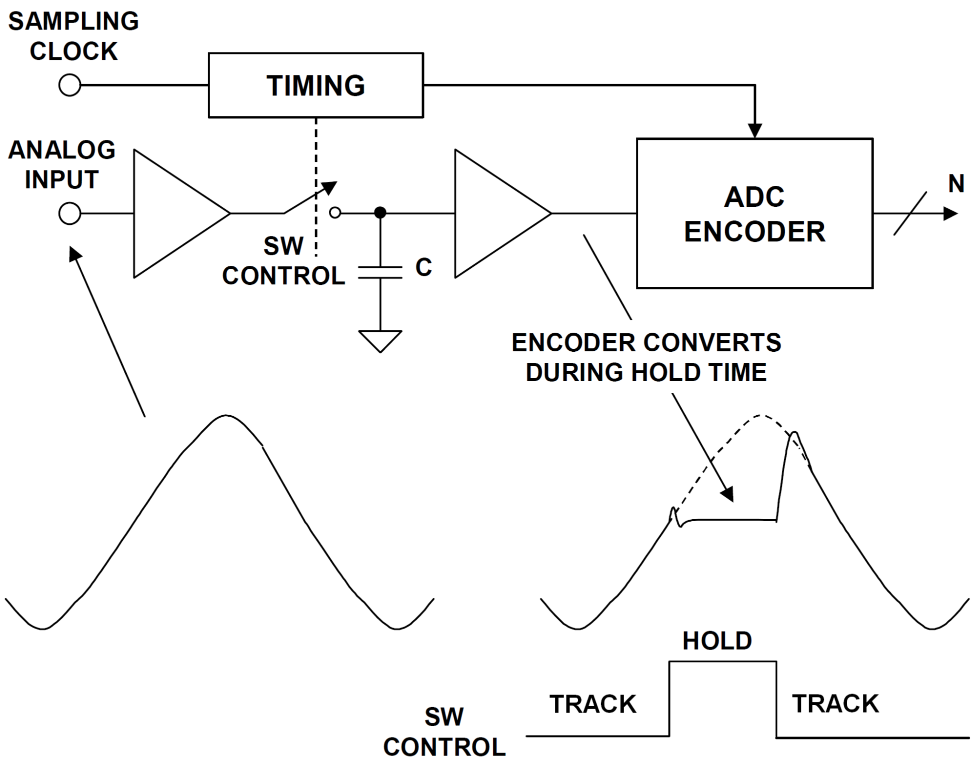


Figure 1.5.: Track-And-Hold-Amplifier schematic and principle [Kes05]

Characteristics of Analog-To-Digital-Converters

For an ideal converter, the number of bits and the sampling rate would be sufficient to fully characterize its performance. Real ADCs however differ from the ideal behavior by introducing static and dynamic imperfections. Different applications have different requirements, which leads to a number of specifications. These can be divided into the following categories [LV02]:

- Quantization Noise
- Static parameters
- Frequency-domain dynamic parameters
- Time-domain dynamic parameters

This section provides an overview of these figures of merit. Which of them are needed to specify the necessary performance of the ADC has to be chosen for each application accordingly.

Quantization Noise

Even in an ideal N-bit converter there will be errors during the quantization, which behave like noise. The reason is that each N-bit word represents a certain range of analog input values, which is 1 LSB wide and centered around a code center (see Figure 1.3) [LV02]. The input voltage is assigned to the word of the nearest code center. This means that there will always be a difference between the corresponding voltage of the respective digital code $x_q(t)$ and the actual analog input voltage $x(t)$. This difference is called the *quantization error*. For an equidistant quantization, the quantization error for a code width q is (see [Pue15])

$$|e_q(t)| = |x(t) - x_q(t)| \leq \frac{q}{2}. \tag{1.6}$$

A setup in order to measure this quantization error is shown in Figure 1.6. The output of the ADC, the N-bit code corresponding to the voltage level of the input signal $x(t)$, is fed to a Digital-To-Analog-Converter (DAC), which converts this code into a corresponding voltage level $x_q(t)$. The difference between $x(t)$ and $x_q(t)$ is then the quantization error $e_q(t)$.

In order to analyze the quantization noise and the resulting theoretical (maximum) Signal-To-Noise-Ratio (SNR) of the ideal ADC, assume a ramp with the slope s as an input signal. In the time domain, the quantization error $e_q(t)$ can then be approximated with a sawtooth signal:

$$e_q(t) = st, \quad -\frac{q}{2s} < t < \frac{q}{2s} \tag{1.7}$$

The function Equation 1.7 is plotted in Figure 1.6.

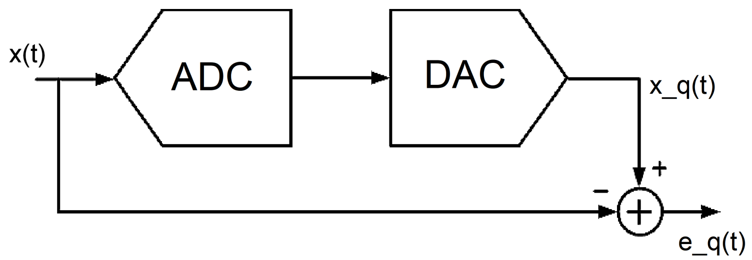


Figure 1.6.: Setup for measuring the quantization error of an (ideal) ADC

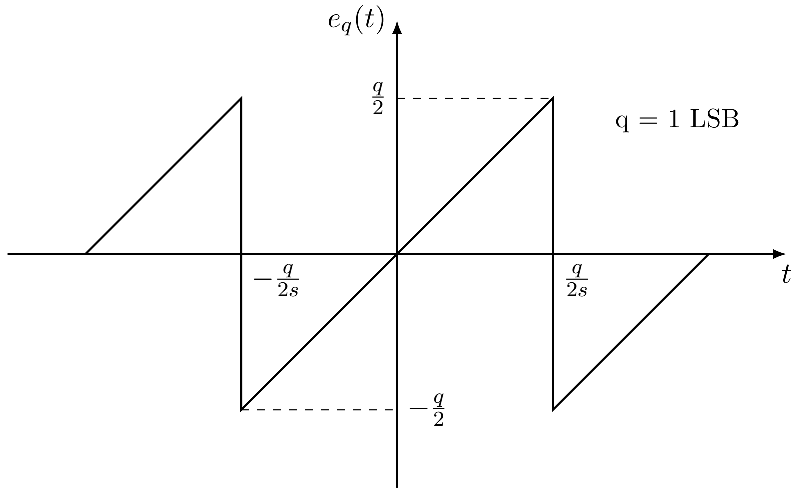


Figure 1.7.: Quantization noise as function of time (redrawn from [Kes05])

The power of this quantization noise can be calculated as the mean-square $e^2_{\text{rms}}$of $e(t)$ [Kes05]:

$$P_{QN} = e^2_{\text{rms}} = \overline{e^2(t)} = \frac{s}{q}\int_{-q/2s}^{+q/2s}(st)^2 dt = \frac{s^3}{q}\left[\frac{t^3}{3}\right]_{-\frac{q}{2s}}^{+\frac{q}{2s}} = \frac{q^2}{12} \tag{1.8}$$

In order to calculate the maximal SNR of an ideal converter, a full-scale input sine wave is applied to the input:

$$u(t) = u_s \sin(2\pi ft) = \frac{2^N q}{2}\sin(2\pi ft) = 2^{N-1}q\sin(2\pi ft) \tag{1.9}$$

With the effective value of the signal amplitude

$$u_{\text{eff}} = \frac{u_s}{\sqrt{2}} = \frac{2^{N-1}q}{\sqrt{2}} \tag{1.10}$$

SNR

$$\text{SNR} = \frac{P_{\text{signal}}}{P_{\text{noise}}} = \frac{u_{\text{eff}}^2}{e_{\text{rms}}^2} = \frac{2^{2N-2}q^2/2}{q^2/12} = 2^{2N} \cdot 1.5. \tag{1.11}$$

In decibel:

$$\text{SNR}|_{\text{dB}} = 10 \log \left(2^{2N} \cdot 1.5\right) = 6.02N + 1.76 \tag{1.12}$$

[Pue15] [Kes05]

Static parameters

Static parameters are specifications, which can be measured at low speed/DC.

Accuracy

Accuracy is the total error with which an ADC can convert a known voltage, which includes the effects of:

- Quantization error
- Gain error
- Offset error
- Nonlinearities

[LV02]

Resolution

Resolution is the number of bits N of the ADC. Depending from the resolution are the size of the LSB, which in its turn determines the dynamic range, code widths and quantization error.

Dynamic Range

The *dynamic range* represents the ratio between smallest possible output (LSB voltage) and the largest possible output (full-scale voltage). It can be calculated as

$$20 \log 2^N \approx 6N. \tag{1.13}$$

Offset and Gain Error

The *offset error* is defined as the deviation of the actual ADC transfer function from the ideal ADC transfer function in the point of zero. It is measured in LSB.

Gain Error defines the deviation of the slope of the line going through the zero and full-scale point of the transfer function. Figure 1.8 visualizes the effects of both offset and gain error.

These errors can easily be corrected by calibration. In order to measure the offset and gain error, two different voltage levels V_1 and V_2 are applied at the ADC input. This results in corresponding bit codes b_1 and b_2. The slope s of the transfer function can then be calculated by

$$s = \frac{b_2 - b_1}{V_2 - V_1}. \tag{1.14}$$

From this, the gain error can be determined. In order to obtain the offset error b, the linear equation

$$b = b_1 - s \cdot V_1 \tag{1.15}$$

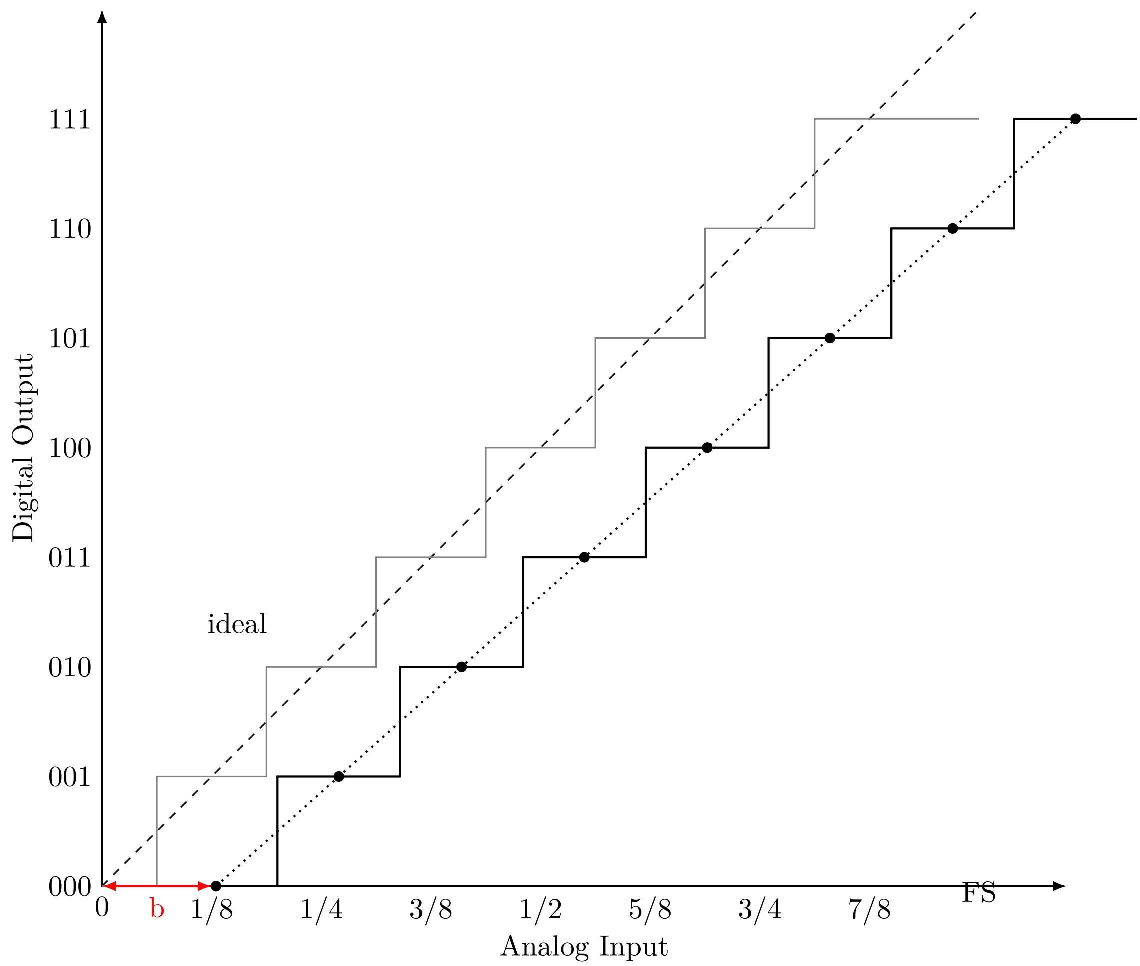


Figure 1.8.: Offset and Gain Error in the ADC characteristic transfer function. The offset error is indicated with the red arrow. The gain error expresses itself via different slope of the real ADC (dotted) compared to the ideal ADC (dashed)

Integral and Differential Non-linearity Distortion

Integral Nonlinearity (INL) is the distance of the code centers on the actual ADC transfer function from the ideal line (dashed line in Figure 1.9). It results from the integral non-linearities of the front-end, SHA and also the ADC itself. [Kes05, LV02]

Differential Nonlinearity (DNL) is the deviation in actual code width from the ideal width of 1 LSB. This nonlinearity stems exclusively from the encoding process in the ADC. [LV02, Kes05]

The effect of these errors is shown in Figure 1.9.

These nonlinearities could be measured with a histogram test. A voltage ramp is applied at the input and the number of occurrences of each ADC output code, $n(\text{code})$, is measured. With the ramp slope s am ideal ADC with the sampling frequency f_s would give

$$n(\text{code}) = \frac{\text{LSB}}{s} \cdot f_s = n_{\text{avg}} \tag{1.16}$$

which ideally would be constant for the whole input range (except for the first and last

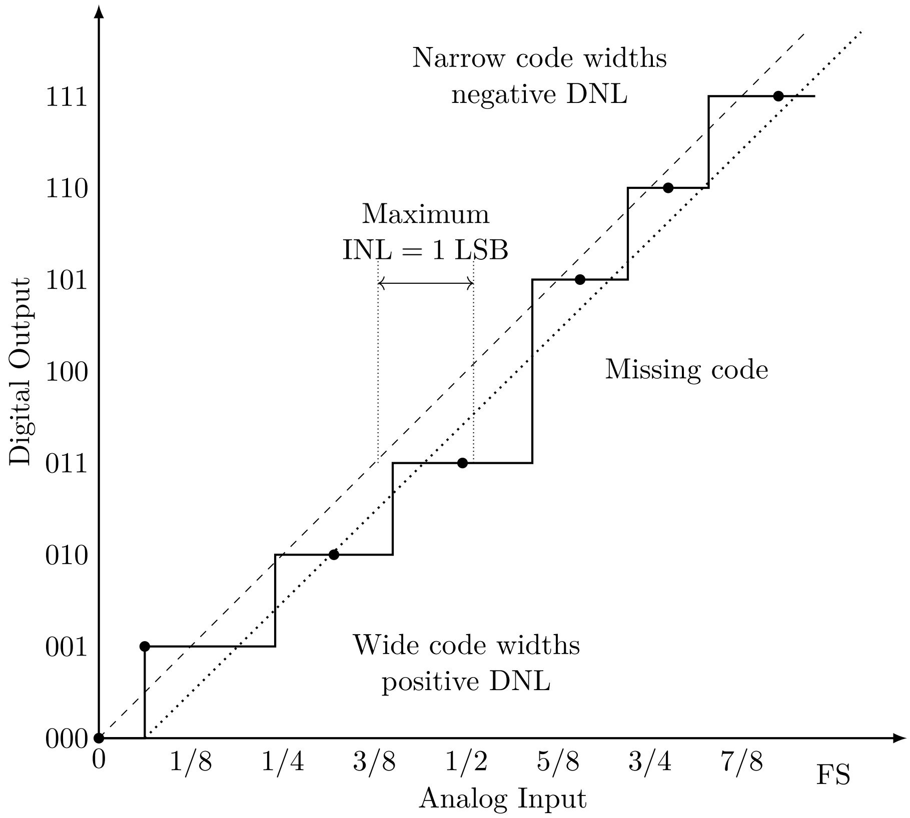


Figure 1.9.: Transfer function of a real ADC showing DNL and INL.[LV02]

code). For a real ADC this is not the case and the DNL and INL are calculated as

$$\text{DNL(code)} = \frac{n(\text{code}) - n_{\text{avg}}}{n_{\text{avg}}} \tag{1.17}$$

$$\text{INL(code)} = \sum_{i=0}^{\text{code}} \text{DNL}(i). \tag{1.18}$$

[Vol]

Frequency-Domain Dynamic Parameters

Any real ADC is subject to noise distortion. *Noise* denotes any unwanted random signal, which interferes with the measuring of the desired signal. Examples are quantization noise or random fluctuations due to thermal noise. *Distortion* is the term for alteration of the shape of the original signal. As an example, distortion of the amplitude might result due to not equal amplification of the parts of a signal. [dif]

In an ADC (with built-in SHA) there are a couple of sources, which introduce noise and distortion:

- **Input Stage:** Wideband noise, non-linearity and bandwidth limitation
- **SHA:** Non-linearity, aperture jitter(see paragraph about Time-Domain Dynamic Performances) and bandwidth limitation
- **ADC:** Quantization noise, non-linearity

For quantification of noise and distortion, frequency-domain metrics are used. Therefore the in the following paragraph described figures of merit are also called frequency-domain dynamic parameters. These parameters are measured with the help of the Fast-Fourier-Transform (FFT) meaning any modern oscilloscope can be used to quickly assess the frequency-domain dynamic performance for a given input at the ADC. As some parameters, such as SFDR (Spurious-Free Dynamic Range), are only defined for one carrier input frequency, several measurements at different input frequencies need to be made in order to fully characterize the ADC.

In the following, an overview of the metrics for quantification of the noise and distortion of an ADC is given.

Signal-to-Noise-and-Distortion Ratio

Signal-to-Noise-and-Distortion Ratio (SINAD) (also called SNDR or S/N+D) denotes the ratio between the Root-Mean-Square (RMS) of the signal amplitude to the mean value of the Root-Sum-Square (RSS) of all other spectral components, including harmonics, but excluding DC (0 Hz). SINAD is a good indication over the general dynamic performance of the ADC, as it includes all contributions from noise and distortion.

Effective-Number-Of-Bits

The *Effective-Number-Of-Bits (ENOB)* expresses the SINAD in terms of bits. It can be calculated as

$$\mathrm{ENOB} = \frac{\mathrm{SINAD} - 1.76\,\mathrm{dB}}{6.02\,\mathrm{dB/bit}}. \quad \text{[Kes09]} \tag{1.19}$$

This is derived from solving the equation of the ”ideal SNR” Equation 1.12 for the number of bits N and substituting SNR with SINAD. This however means, that this parameter assumes a full-scale input signal. Expressing the ENOB for a smaller signal amplitude requires measuring the SINAD at this level and a correction factor. [Kes05]

Spurious-Free Dynamic Range

Spurious-Free Dynamic Range (SFDR) indicates the dynamic range of the converter, which can be used, before there is interference or distortion from spurious components with the fundamental signal. [LV02] The SFDR is calculated as the RMS value of the fundamental signal to the RMS value of the worst spurious signal, i.e. the highest spur in the spectrum. It is measured over the whole Nyquist-Bandwidth (DC (0 Hz) to $f_s/2$, f_s being the ADC sampling rate). The spur may or may not be a harmonic of the fundamental signal. [Kes09] [LV02]

The SFDR is an important characteristic in the sense, that it indicates the smallest signal which can still be distinguished from a strong interfering signal. [Kes09]

Figure 1.10 illustrates the SFDR in terms of decibels relative to full scale (dBFS) and decibels relative to the carrier (dBc).

Total Harmonic Distortion

The *Total Harmonic Distortion* describes the ratio of the RMS sum of the first five harmonic components (or aliased versions of them) to the RMS of the considered fundamental signal. [LV02]

Effective Resolution Bandwidth

Effective Resolution Bandwidth denotes the frequency of the input signal, at which the SINAD has fallen by 3 dB ($\widehat{=}$ 0.5 bit in terms of ENOB) compared to the SINAD at lower frequency range. [LV02]

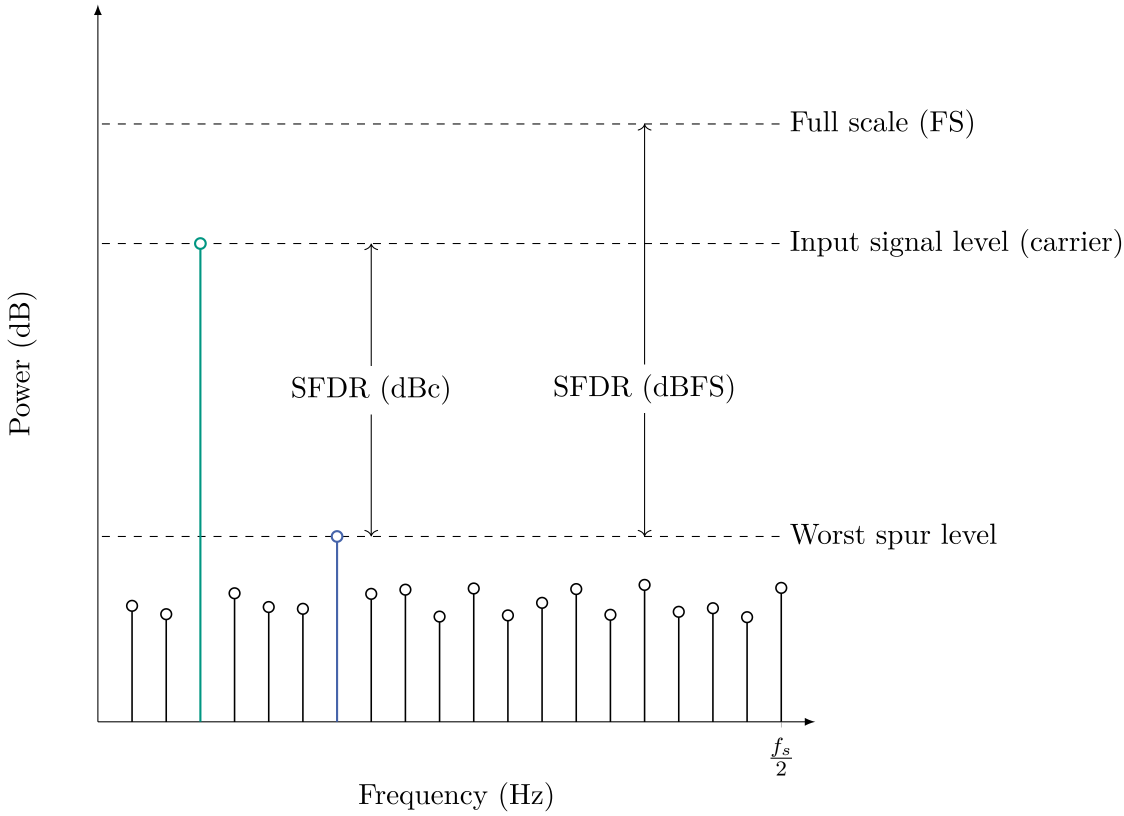


Figure 1.10.: Visualization of the SFDR. It can be indicated either with reference to the carrier frequency in “dBc” or with reference to the Full-Scale Input in “dBFS”. [Kes09]

Analog Input Bandwidth

Analog Input Bandwidth is the analog input frequency at which the power of the fundamental is reduced by 3dB with respect to the low-frequency value. [LV02] It is not to be confused with the maximal analog input frequency which the ADC is able to sample.

Full-Linear Bandwidth

The *Full-Linear Bandwidth* is defined as the frequency at which the slew-rate (SR) of the SHA starts to distort the input signal by a specified value. [LV02] The slew-rate is defined as the rate of how much the voltage v changes against time t:

$$\mathrm{SR} = \frac{dv}{dt} \tag{1.20}$$

A SR of 1 V/µs for example means, that the output of the amplifier can not change more than 1 V over the course of 1 µs.[Col21]

Time-Domain Dynamic Parameters

Time-Domain Dynamic parameters describe the deviation of the converter’s behavior from the ideal one in time domain.

Aperture Delay

Aperture Delay (or *aperture time*) is defined as delay between the triggering of the converter (e.g. rising edge of the sampling clock) and the actual conversion of the input voltage into the digitized value. [LV02]

Aperture Jitter

Aperture jitter describes the sample-to-sample variation in aperture delay. Jitter can cause significant error in the voltage and decreases the overall SNR of a converter. Especially for high-speed ADCs jitter poses a limit in performance.

Assuming a full-scale sinus-wave V_{in} as input signal with

$$V_{\text{in}} = V_{\text{FS}} \sin(\omega t) \tag{1.21}$$

the maximal slope of this signal is then

$$\left.\frac{dV_{\text{in}}}{dt}\right|_{\text{max}} = \omega V_{\text{FS}} \tag{1.22}$$

Aperture jitter Δt_{rms} occurring during the sampling of this maximal slope produces the RMS voltage error

$$\Delta V_{\text{rms}} = \omega V_{\text{FS}} \Delta t_{\text{rms}} = 2\pi f V_{\text{FS}} \Delta t_{\text{rms}}. \tag{1.23}$$

As variations in aperture time occur randomly, these errors behave like a random noise source. This way, a Signal-to-Jitter-Noise-Ratio (SJNR) can be defined as

$$\text{SJNR} = 20 \log \left(\frac{V_{\text{FS}}}{\Delta V_{\text{rms}}} \right) = 20 \log \left(\frac{1}{2\pi f V_{\text{FS}}} \right) \tag{1.24}$$

The voltage error due to jitter and the SJNR for different aperture jitter values are shown in Figure 1.11.

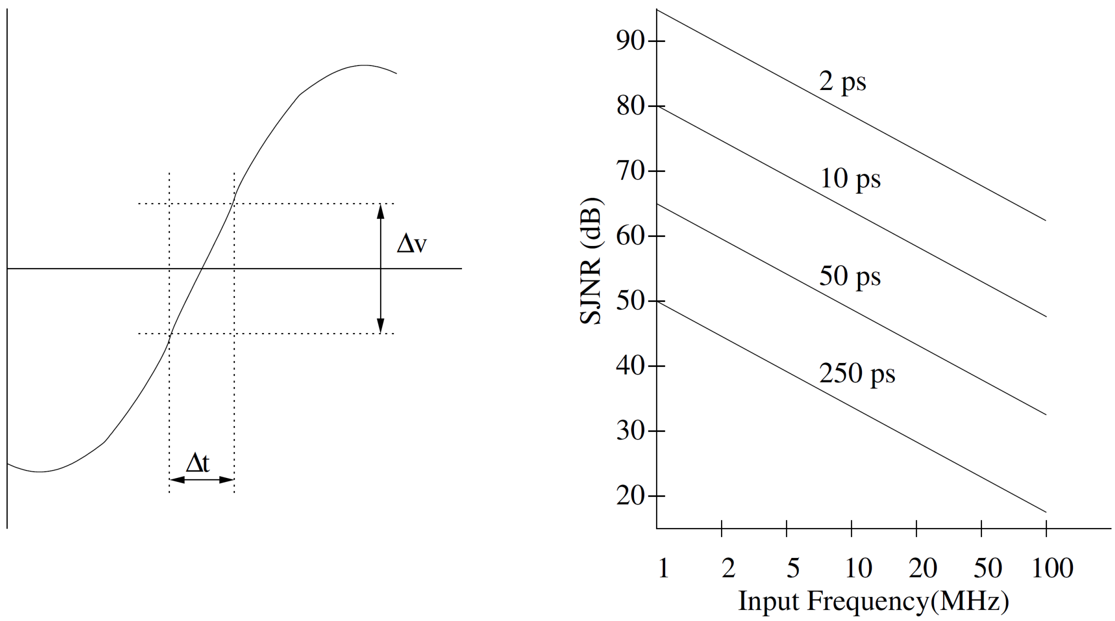


Figure 1.11.: Placeholder: Effects of aperture jitter and SJNR [LV02]

Transient Response

The *transient response* denotes the settling time of an ADC until full accuracy (± 1/2 LSB).

Sampling Theory

An ADC samples an analog signal with a sample frequency f_s. This frequency has to be chosen in such way, that the original signal can be fully reconstructed. The *Nyquist criteria* states, that in order to accurately reconstruct a band-limited, continuous signal

$$y(t) \circ\!\!-\!\!\!-\, Y(f) \quad \text{with} \quad Y(f) = 0|_{f>B/2} \tag{1.25}$$

it has to be sampled with a frequency f_s respecting

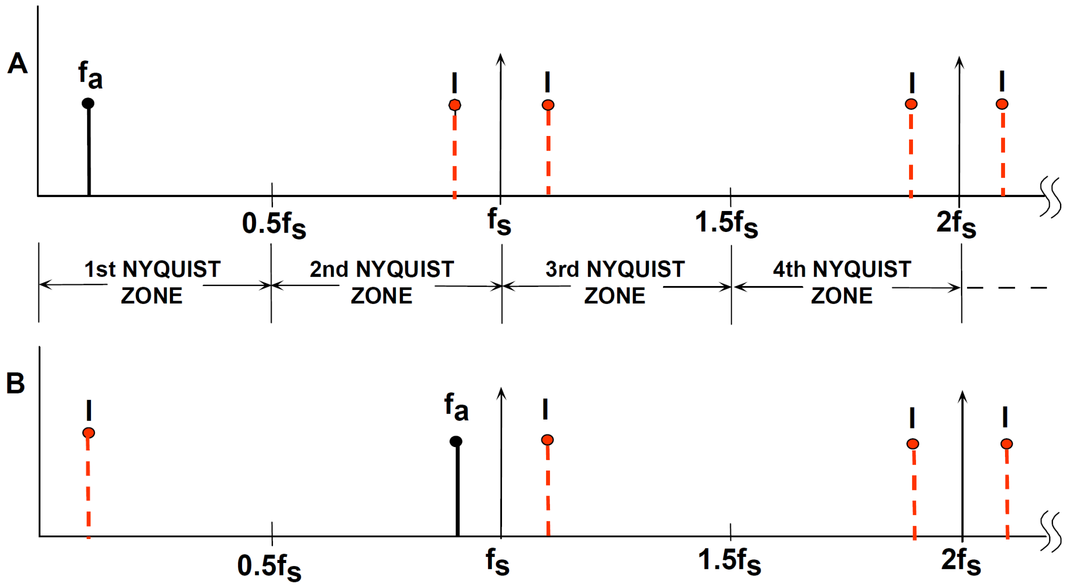
$$f_s > B \quad \text{or} \quad f_s > 2f_a \tag{1.26}$$

with f_a being the highest frequency contained in the signal. [Kes05, Pue15] The range from 0 Hz to $f_s/2$ is also called *Nyquist-Zone* (or "1st Nyquist zone", see Figure 1.12a).

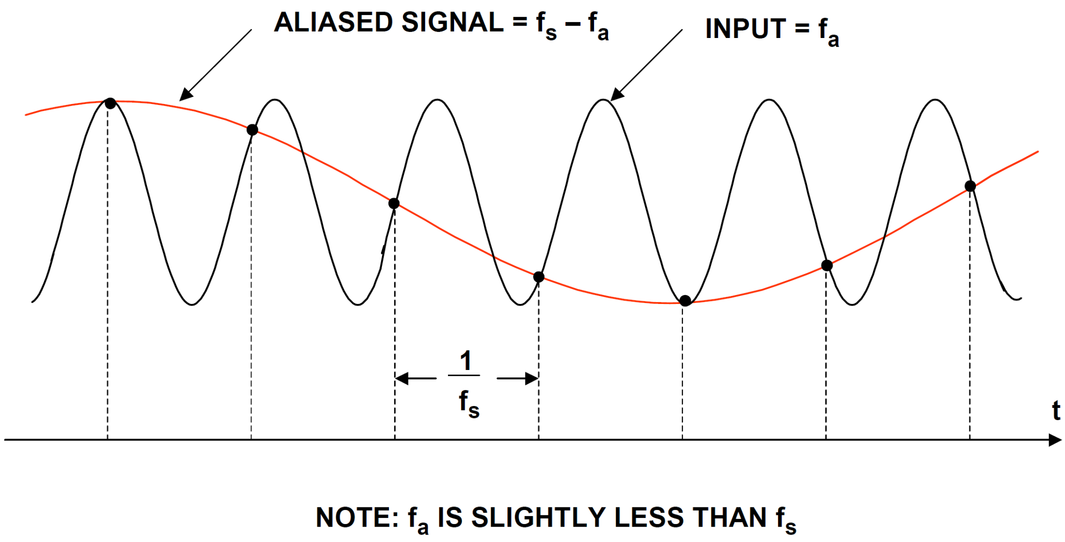
Violation of this rule leads to *aliasing*. The effects of aliasing are shown in Figure 1.12.

When a sine wave of the frequency f_a is sampled with the frequency f_s, this leads to periodic repetition of the signal spectrum in frequency domain in intervals of f_s, or "images" (see dashed, red frequency components in Figure 1.12a). If Equation 1.26 is respected, i.e. f_a lies inside the Nyquist bandwidth, there is no overlap with the images created by the sampling process.

Now assuming a signal frequency $f_a \approx f_s$, the sampling process leads to an image falling inside the Nyquist bandwidth. The reconstructed signal then lies at the frequency of this image which is much lower than the original frequency. The result of this *undersampling* is shown in Figure 1.12b



(a) Sampling process visualized in frequency domain



(b) Effect of aliasing shown in time domain

Figure 1.12.: Analog signal with frequency f_a sampled at f_s respecting (A) and not respecting (B) the Nyquist criteria (see Figure 1.12a). Figure 1.12b shows the effect of case B in time domain. [Kes05]

1.3. THz Science

Recent years have seen an increasing interest in THz radiation (ranging from 3 THz up to 30 THz), as it allows non-destructive analysis of organic material. This is possible because unlike e.g. X-Rays, THz radiation is not ionizing. It is therefore of great interest to use THz radiation in such fields like biology, medicine or material science. However, until recently the usage of THz radiation was very limited, as generation of such radiation has proven to be difficult.

Electron storage rings, also called synchrotrons, are studied as a potential source of THz-radiation. The emission of THz radiation is closely linked to instabilities of the particles which are accelerated in the synchrotron. These instabilities occur in the range of femtoseconds and cause bursts of THz radiation. The periodicity of these bursts depends on multiple parameters of the synchrotron and therefore imposes a challenge on controlling the emission of THz radiation. Studying the dynamics of these instabilities is an important step towards the applicability of synchrotrons as source of THz radiation. [Rot18]

Coherent Synchrotron Radiation

In synchrotron radiation facilities (like electron storage rings) Synchrotron Radiation (SR) is produced by accelerating relativistic electrons. Emission of SR occurs, when electron beams are bent or deflected with dipole magnets or using undulators. The latter are used to make the electrons oscillate by generating a periodic magnetic field. Figure 1.13 shows the general scheme of an electron storage ring.

Electrons, which are grouped to "electron bunches", are generated with an electron gun and accelerated to relativistic speeds[2] by a linear accelerator (LINAC). After being brought up to their nominal energy[3], the bunches are injected into the storage ring. In the ring, the path of the electron bunches is altered by bending magnets, guiding them on a circular trajectory. Due to emission of SR at each bend, the electrons lose energy, which has to be compensated for. This is done by accelerating them with an electric field inside a Radio Frequency (RF) cavity. Not shown in the drawing are the beamlines, which lead the SR radiation, or rather chosen wavelength ranges, through an optical system to the respective user experiments. [Rou14] [Rot18]

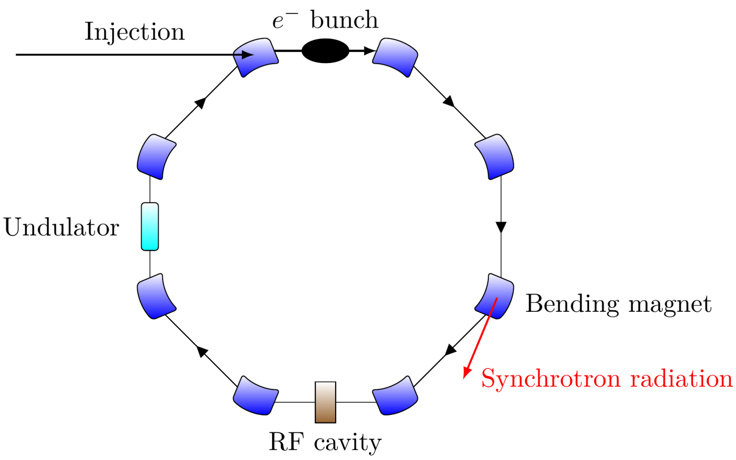


Figure 1.13.: Basic scheme of an electron storage ring (redrawn from [Rou14])

The range of SR reaches from hard X-rays down to the infrared region of the electromagnetic spectrum (see Figure 1.14). In contrast to other sources, it has properties like:

[2]almost speed of light
[3]in a booster

- high intensity
- high collimation
- polarisation
- well-defined timing of pulses

Due to this properties, synchrotrons are used for microscopy, spectroscopy, and time-resolved experiments in such fields like condensed matter physics, biology, material science and many more.

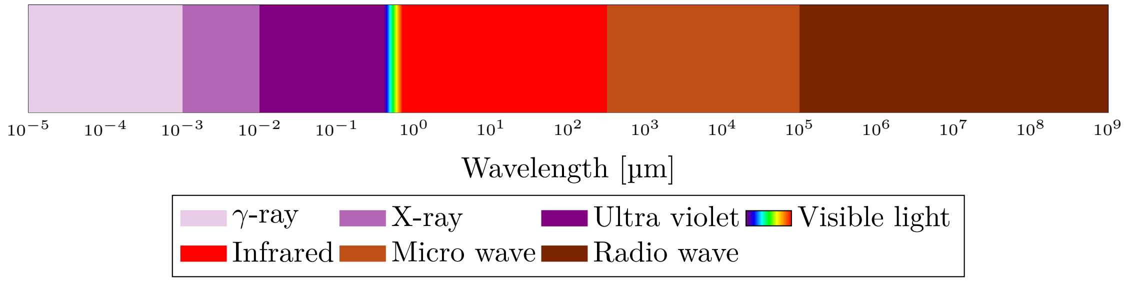


Figure 1.14.: Electromagnetic spectrum

Karlsruhe Research Accelerator

At the synchrotron light source Karlsruhe Research Accelerator (KARA), the possibility to utilize the synchrotron as a source of THz is actively researched. The photonic time-stretch Data Acquisition System (DAQ), which is developed in this thesis, should also be integrated into the beam diagnostics system at KARA. Therefore, a short overview of some parameters of this facility is given.

- Located at the Karlsruhe Institute of Technology (KIT)
- Up to 184 electron bunches can be filled into the storage ring with a distance of 2 ns (500 MHz) between two adjacent bunches
- Operated by the Institute of Beam Physics and Technology (IBPT)
- Microtron, Booster Synchrotron, and Storage Ring

Table 1.1.: Some KARA parameters [Rot18]

Parameter	**Value**
Beam energy	2.5 GeV
Circumference	110 m
Revolution Frequency (one electron)	2.7 MHz
Minimum bunch spacing	
multi-bunch	2 ns
single-bunch	368 ns
Bunch length	
normal operation	45 ps
short bunch	2 ps

Micro-Bunching Instabilities

Increasing demands in current and future accelerators applications call for higher brilliance of the emitted radiation. This is achieved by shortening the electron bunches are shortened. This results in emission of CSR, shown in Figure 1.15, at frequencies up to the THz range.

Due to this CSR the bunches interact with their own radiation (see Figure 1.16).

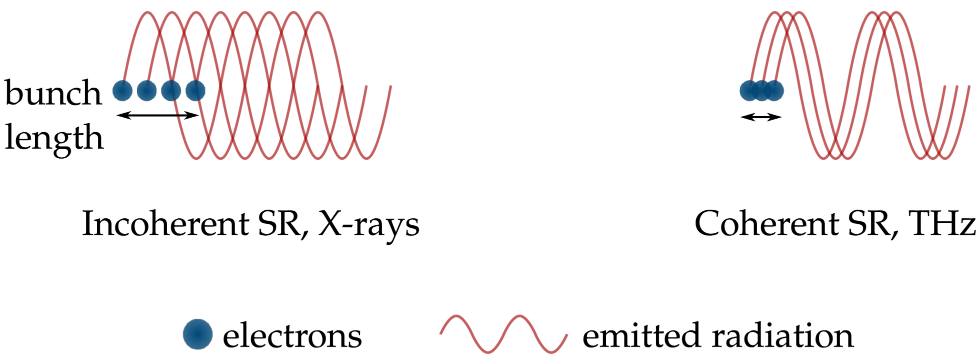


Figure 1.15.: Incoherent SR and coherent SR due to shorter electron bunch length [Rot18]

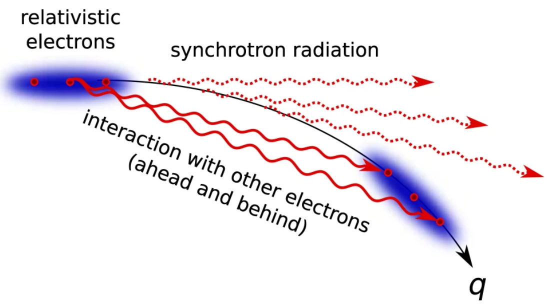


Figure 1.16.: Electrons interact with their own radiation [BBB+19]

This introduces complex dynamics, as the electrons interact with their own radiation. This manifests into the so called micro-bunching instability, the formation of micro-structures (in the sub-millimeter range) in the longitudinal density profile of the electron bunches. These instabilities occur in bursts and are hard to control, as they depend from a number of system parameters. This imposes on one side a great limitation to the stable operation of the overall system at high current density/short bunch length mode. On the other side, these instabilities themselves emit brilliant THz radiation. Therefore, a control of these instability bursts could potentially make them a source of THz for user-applications. A thorough understanding and studying of these beam dynamics is therefore an important step towards providing an applicable THz source. [Rot18, Bro20] In order to make such investigations possible, appropriate beam diagnostic systems are required.

Longitudinal Bunch Profile Diagnostics

Methods for analyzing the longitudinal profile of electron bunches are based on a similar, if not the same, concept as the time-stretch method. Two most prominent methods are briefly described.

Scanning-Type Electro-Optic Sampling

The scanning-type electro-optic sampling (EOS) samples one point of the THz pulse, emitted e.g. from an electron bunch, at the time at each acquisition, hence the naming of this method. A short laser pulse (duration typically hundreds of femtoseconds) co-propagates with a THz pulse from CSR (range of picoseconds) in an EO crystal. Due to the Pockels effect. The THz pulse causes a time dependent birefringence in the crystal. This modulates the polarization of the laser pulse.

To sample the pulse, the delay between the laser and the THz pulse is varied. To detect the changing polarization, the polarization of the laser pulse is transformed into an intensity modulation. This is done by using polarizers, e.g. quarter-wave plates (QWP) and Wollaston prism (WP) (as shown in Figure 1.17). A general scheme of the system is shown in Figure 1.17. For this technique a stable emission of the THz pulses is crucial, as they are not measured in one acquisition. [Rou14]

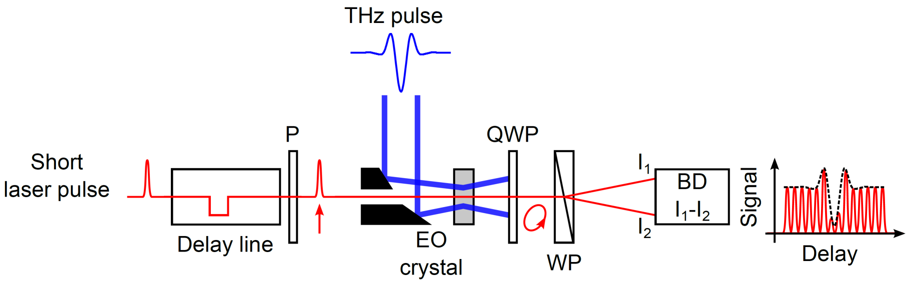


Figure 1.17.: Scheme of Scanning-Type Electro-Optical Sampling System [Rou14]

Spectrally Resolved Electro-Optic Detection

In contrast to the EOS, single-acquisition is possible with the spectrally resolved electro-optic detection technique. The short laser pulse is first stretched to a duration similar to the THz pulse in a dispersive material (stretcher). In this way the pulse is chirped, meaning the instantaneous frequency of the pulse varies over time. Together with the THz pulse, the laser pulse propagates in a EO crystal. Again, the induced birefringence modulates the laser pulse, not only in time, but also in the optical spectrum. The polarization state of the pulse is converted into an amplitude/intensity modulation. This is done with a series of quarter-wave plate (QWP), half-wave plate (HWP) and a polarizer (P) (as shown in Figure 1.18). To retrieve the THz pulse shape in time, the spectrum of the laser pulse is measured with a spectrometer. A general scheme of the system is shown in Figure 1.18. [Rou14]

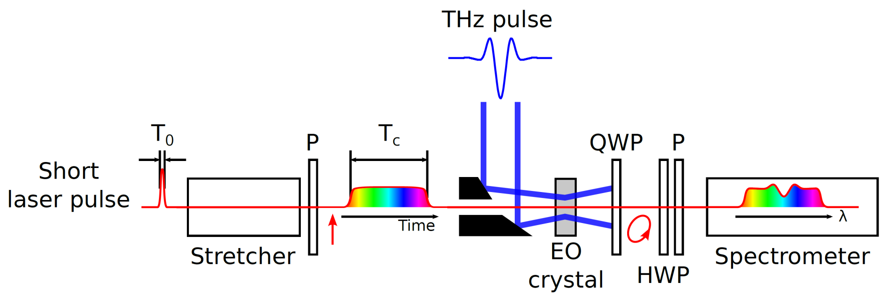


Figure 1.18.: Scheme of Spectrally Encoded Electro-Optical Detection System [Rou14]

The temporal resolution of this method is limited due to the finite chirp rate

$$\text{chirp rate} = \frac{\text{laser bandwidth}}{\text{laser pulse duration after stretcher}}. \tag{1.27}$$

The resolution T_{min} is determined as

$$T_{\text{min}} = \sqrt{T_0 T_c} \tag{1.28}$$

with the bandwidth-limited pulse duration (before stretcher) T_0 and the duration of the chirped laser pulse T_c.

Potential Usage: ANR-DFG ULTRASYNC project?

From Serge's email:

For accelerator applications, we have also a project (ANR-DFG ULTRASYNC project) with KARA and SOLEIL. There is the question of control (i.e., suppression) of the bursts occuring during the microbunching instability. The objective is to obtain a high power and stable coherent emission (at SOLEIL and KARA). For the moment, the only experimental test has been made using a relatively simple feedback:

- a bolometer signal as the feedback loop input
- a low-cost FPGA (redpitaya) that sends the feedback on the accelerating voltage

There are limitations in the maximal bunch charge in the accelerator. So an open question is whether measuring each THz pulse using EO sampling + time-stretch may help to solve this open problem. In clear:

- EO sampling + time-stretch as in Eléonore's thesis
- association with the new FPGA-based system
- finding adequate feedback that is programmed in the FPGA

may solve the problem, and allow the control to succeed at the highest currents in SOLEIL. Target would be ca. 15 mA for 1 bunch (and feedback control presently works to a little more than ca. 10 mA).

2. Architecture Of The New Readout-System - THERESA

2.1. State Of The Art Readout-Systems

This section describes commercially available real-time oscilloscopes, as well as the Karlsruhe Pulse Taking Ultra-fast Readout Electronics (KAPTURE) system, which is in use at KARA for THz diagnostics. Understanding the architecture of the latter will help for the development of the new system, as the basic concept of KAPTURE is reused there.

Real-Time Oscilloscope

TODO: Overview over the current commercially available oscilloscopes.

- KeySight Infiniium MXR-Series Real-Time Oscilloscopes
- Rohde&Schwarz DPO70000SX
- LeCroy LabMaster 10-100Zi

KAPTURE

KAPTURE is a fast readout system developed at the Institute for Data Processing and Electronics (IPE) for THz diagnostics at KARA. It is designed to digitize the pulses generated by THz detectors at each revolution, only sampling the pulse shapes without the "empty" signal in between. The system is able to sample pulses with a Full Width At Half Maximum (FWHM) between a few tens to a hundred picoseconds with a minimal sample time of 3 ps. [CAB+17]

General Architecture

The system consists of two parts: the sampling front-end card and a Field Programmable Gate Array (FPGA) readout card. In Figure 2.1 the setup for THz radiation measurements with KAPTURE is shown.

The incoming radiation is fed into a detector, which converts the incident photons into an electrical signal. This signal is then amplified in a wide-band Low-Noise-Amplifier (LNA). The latter splits the detector signal into four identical signals, which are then propagated to the sampling front-end card. The card consists of four parallel sampling channels with adjustable sample time, each containing a THA and an ADC. This card is connected to a read-out card, which has two tasks: programming the components on the front-end card (FPGA-part) and sending the acquired data to a PC/DAQ system. [CBC+14]

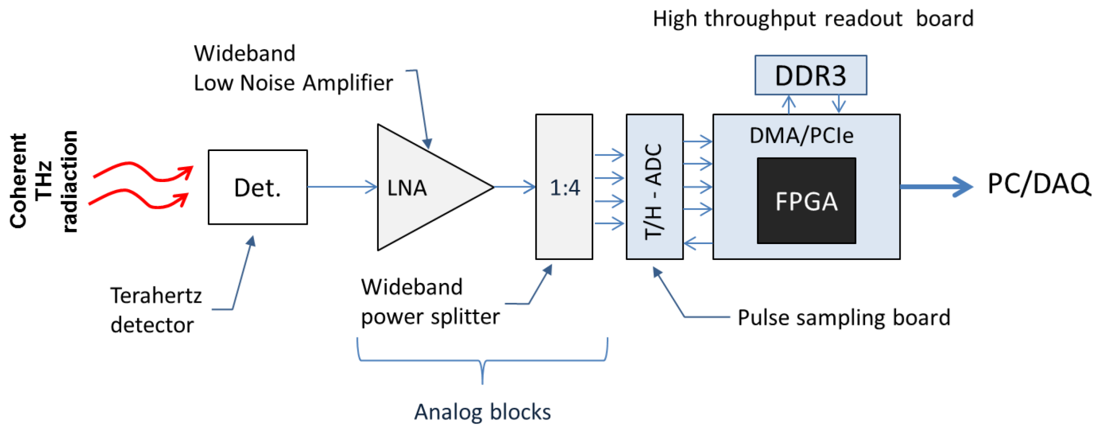


Figure 2.1.: THz radiation measurement setup with KAPTURE(cf. [CBC+14])

Analog Front-End

Due to the high bandwidth nature of the detector signal, the analog front-end of the system has to be wideband as well to be able to sample the signal with picosecond resolution.

The used LNA is based on a commercial GaAs Microwave Monolithic Integrated Circuit (MMIC) which operates from DC to 50 GHz. It is needed to compensate the insertion loss[1] due to the following power splitter.

Classical power-splitters are not intrinsically wideband ([CBC+14]). For that reason, an wideband power-splitter was developed at IPE which fulfills the bandwidth requirements. The designed power-splitter works up to 100 GHz with an insertion loss of 8 dB and a return loss[2] of about 20 dB at 50 GHz.[CBC+14]

Sampling Board

The general structure of the board with the power splitter is shown in Figure 2.2.

Four identical signals from the power-splitter are fed into four channels, consisting of a respective THA unit and a 12-bit ADC sampling at 500 MS/s. The sampling time of each unit can be adjusted individually with a delay chip with a resolution of 3 ps (maximal delay range: 100 ps). The delay chips are programmed with the FPGA on the readout card. The clock signal is provided by KARA, which is cleared from jitter by a Phase-Locked-Loop (PLL). This ensures the synchronization of the ADCs with the RF system. The cleaned clock signal is distributed to the delay chips via fan-out buffer. [CAB+17] In this way, the pulse can be "locally sampled" by adjusting the different delay with a maximum rate of 330 GS/s possible. A simplified representation of the local sampling of the signal is shown in Figure 2.3.

Figure 2.4 shows a photo of the system setup at KARA

PC/Data-Acquisition System

In order to keep a continuous data acquisition the necessary bandwidth is

$$12\text{bits} \cdot 4\,\text{samples} \cdot 500\,\text{MHz} = 24\text{Gb/s} \tag{2.1}$$

[1] *Insertion loss* is the loss of signal power which occurs, when a signal passes through a component.
[2] *Return loss* is the loss of signal power due to reflection by a discontinuity in the transmission line.

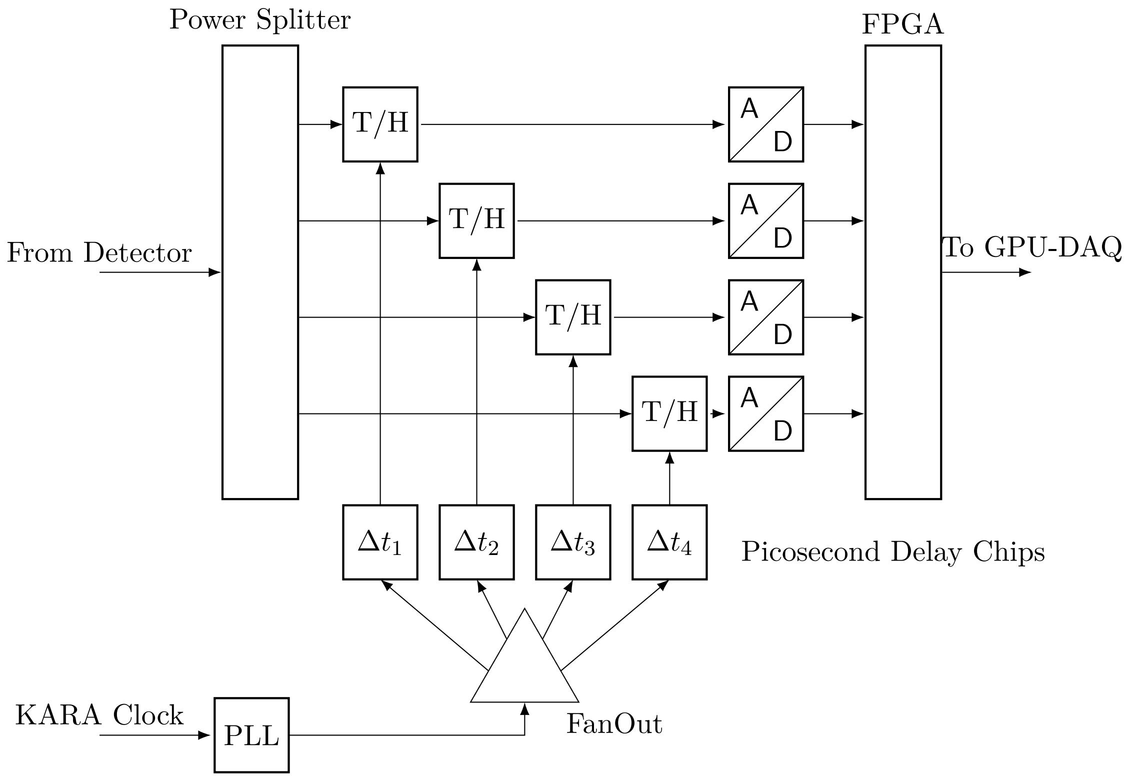


Figure 2.2.: General architecture of the KAPTURE front-end sampling card (cf. [CAB+17, p.2])

To ensure high data throughput, the readout board is based on a bus master Direct-Memory-Access (DMA) architecture which is connected to PCI Express (PCIe) end-point logic. This ensures a throughput of up to 2 GByte/s. To store the data temporary before it is sent to the DAQ system, a large Double Data Rate (DDR)3 memory device is used, as seen in Figure 2.2. [CAB+17]

TODO: briefly explain newer DAQ system with GPU architecture

Briefly mention KAPTURE-2 also?

TODO: Picture of the WHOLE system, i.e. with the optical front end + power splitter + theresa + zcu216

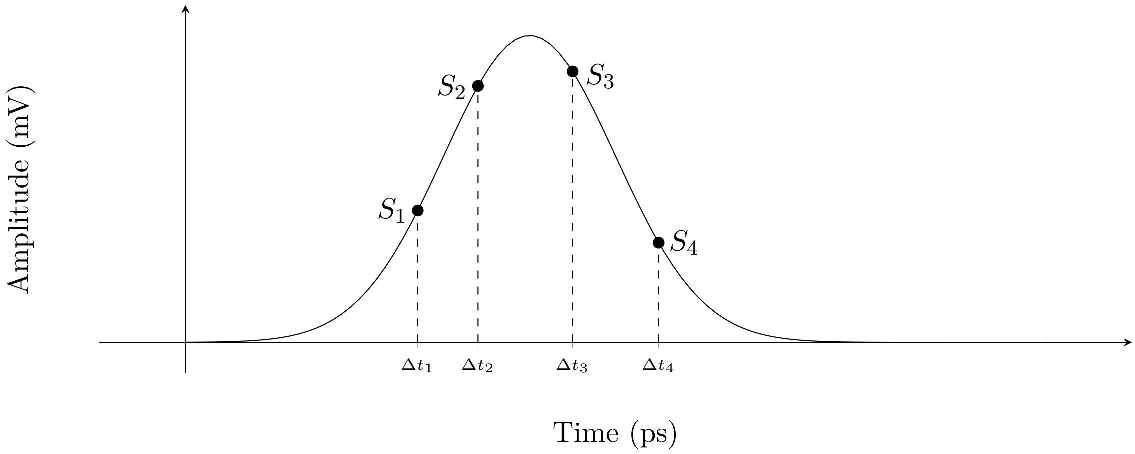


Figure 2.3.: Signal and sampled points S_1 to S_4

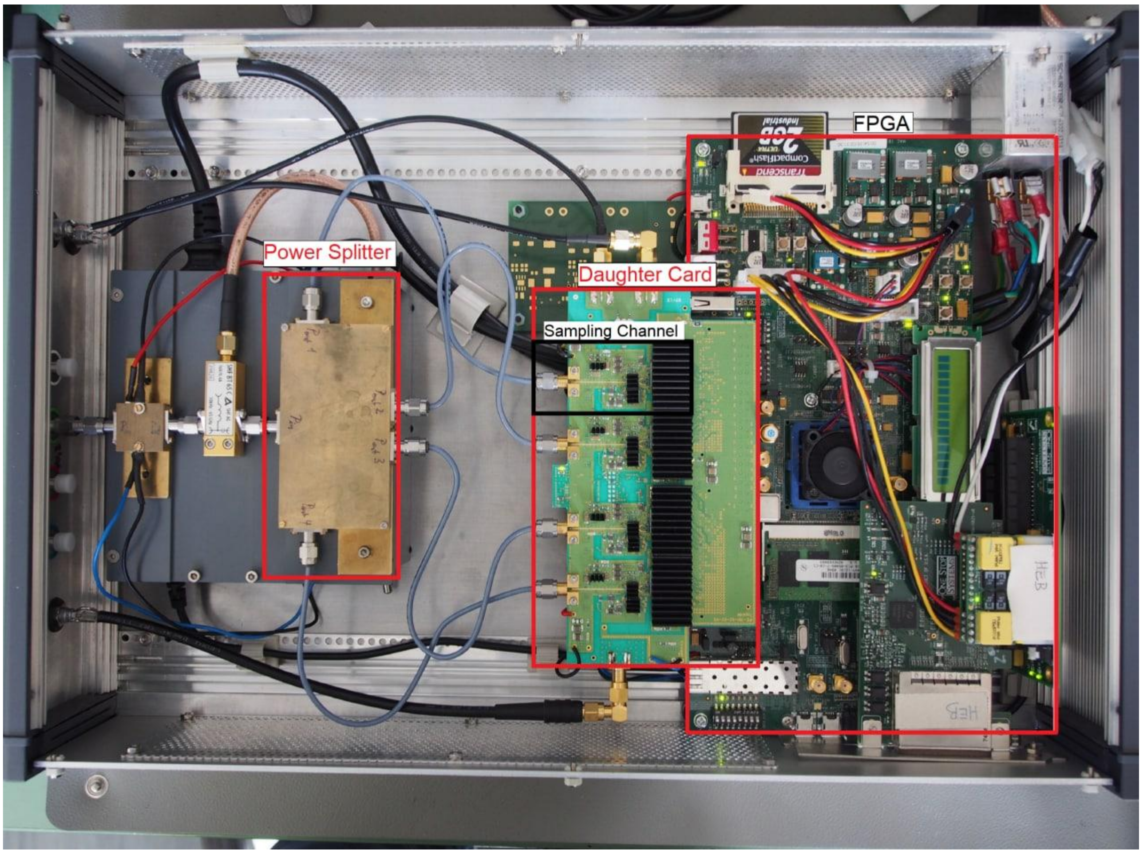


Figure 2.4.: Photo of KAPTURE with highlighted main components. [Bro20, p. 61]

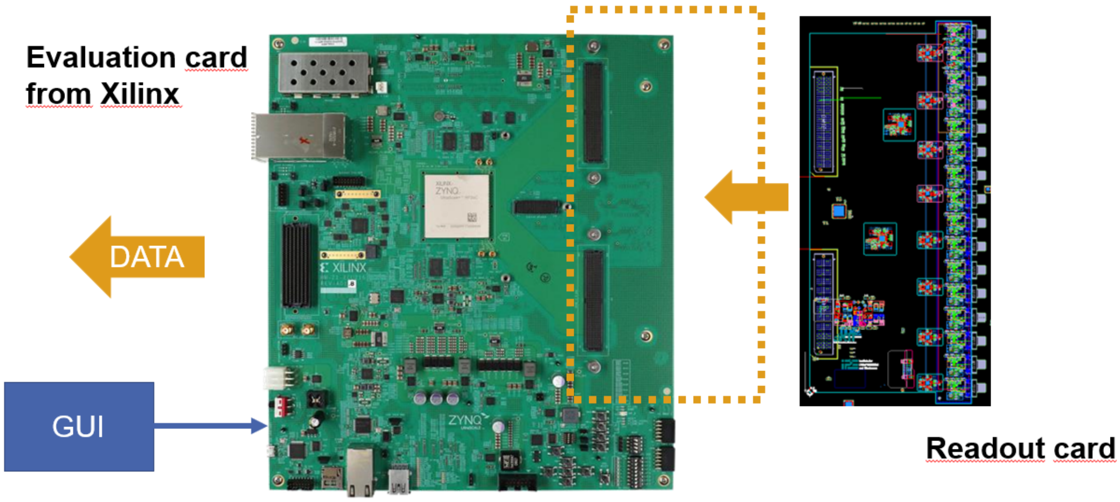


Figure 2.5.: General concept of the new readout system

2.2. New System

Optical Part

"femtosecond Ytterbium-doped fiber laser (Orange) from MENLO GmbH. The emitted pulses have a spectral bandwidth of 50 nm, and the total output average power is 40 mW. The repetition rate is chosen at 88 MHz, which corresponds to 1/4 th of the RF frequency of Synchrotron SOLEIL and 104 times the electron revolution frequency."

Photodetector

The detection and subtraction between the two stretched signals is performed using a amplified balanced photodetector (photoreceiver) from Discovery Semiconductors, with 20 GHz bandwidth and 2800 V/W gain (specified at 1500 nm).

Front-End Card

Figure 2.6 shows the general schema of the sampling system, reduced to four channels for presentation purposes.

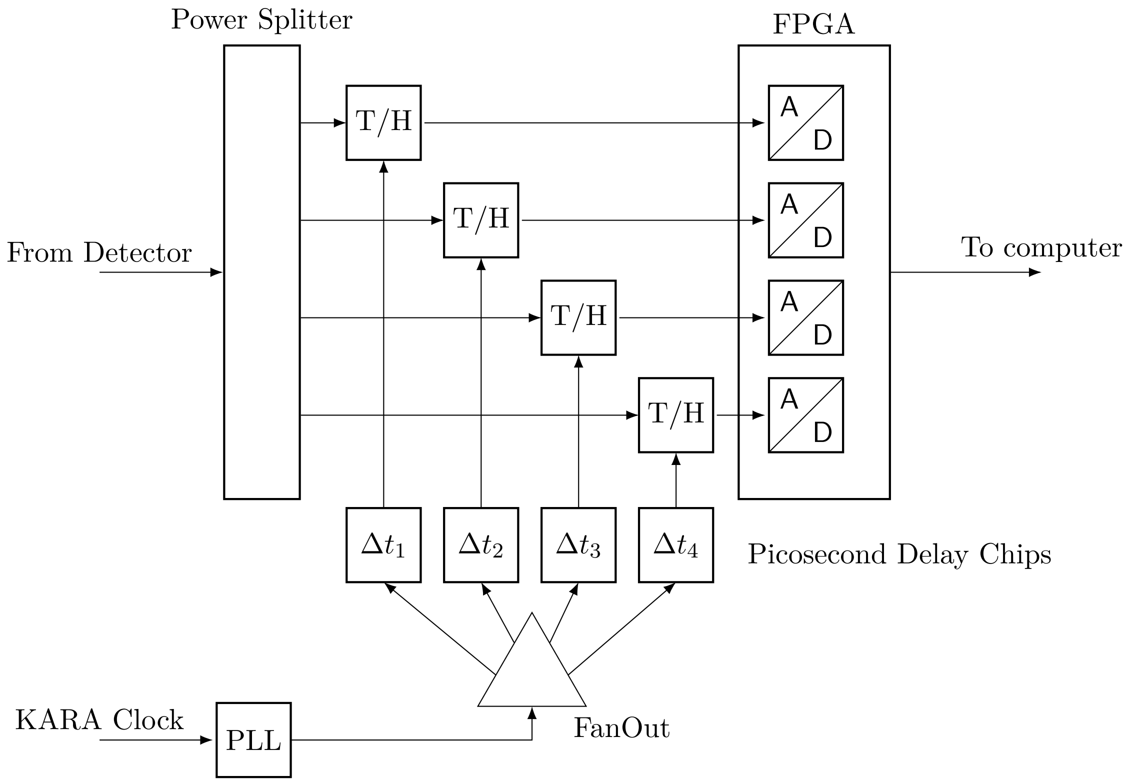


Figure 2.6.: General architecture of THERESA with power splitter and ADCs. For presentation purposes only four of the sixteen channels are shown.

Time Interleaving

In order to increase the sampling rate, the so called time-interleaving technique is used. In this section, first basic theory about this technique is given. Then, the implementation in the new system is described.

Theory

In the *Time Interleaving* technique multiple ADCs are used in such way, that allows to sample data at a faster rate, than the respective sample rate of each individual ADC. The principle is based on time-multiplexing an array of M identical ADCs (see Figure 2.7), each sampling at $f_c = f_s/M$ individually. This means, the ADCs are clocked in such a way, that they start their respective conversion cycle shortly one after another. At time t_0 the first ADC starts converting the input signal $V_i(t_0)$, after a time delay Δt_i the second starts converting the signal $V_i(t_0 + t_i)$, the third converts $V_i(t_0 + 2t_i)$ and so on. After the M-th ADC has sampled the signal $V_i(t_0 + (M-1)t_i)$, the whole cycle starts anew with the first converter. [MR15]

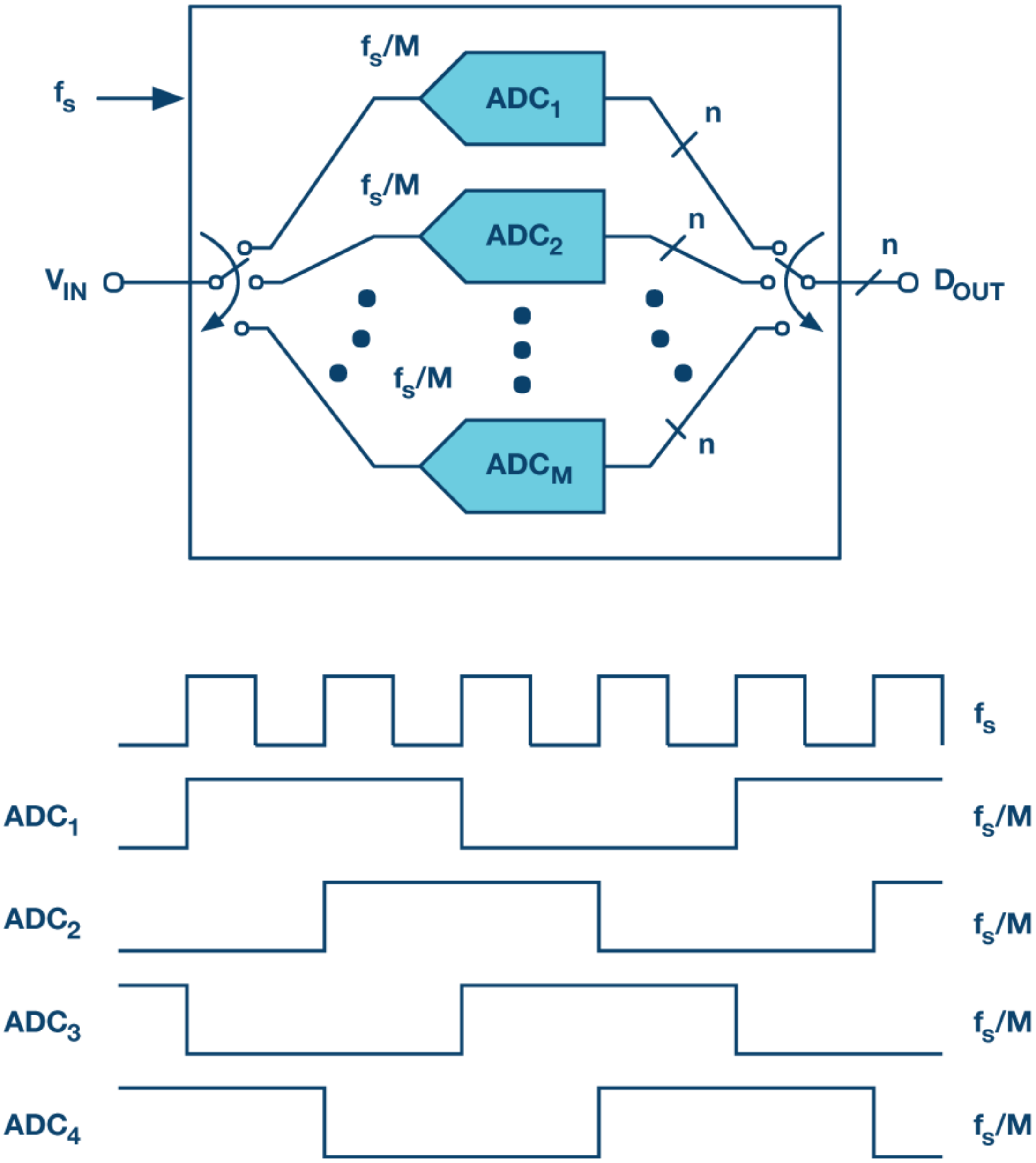


Figure 2.7.: Placeholder: An array of M time interleaved N-bit ADCs with example of clocking scheme for the case of $M = 4$ [MR15]

Challenges

Spurs appear in the spectrum. There are several reasons for this.

First reason is the *offset mismatch* between den ADCs. Each ADC has an DC offset value. Considering as example an interleaving structure with two ADCs and a constant input voltage: when the samples are acquired back and forth between the two ADCs, the resulting output will switch back and forth between two levels due to the different offset levels. This output switches at the frequency $f_s/2$ and therefore introduces an additional frequency component in the spectrum (see Figure 2.8). The magnitude of the spur depends on the offset difference between the ADCs. [Har19]

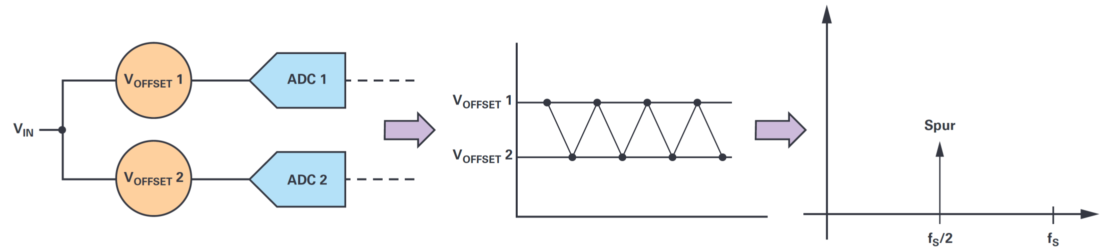


Figure 2.8.: Placeholder: Offset-Mismatch in Interleaving [Har19]

Besides of the offset also the gain of the converters can be mismatched. This *gain mismatch* has a frequency component to it, which in case of an input signal of the frequency f_{in} results in a spur at $f_s/2 \pm f_{\text{in}}$ (see Figure 2.9). [Har19]

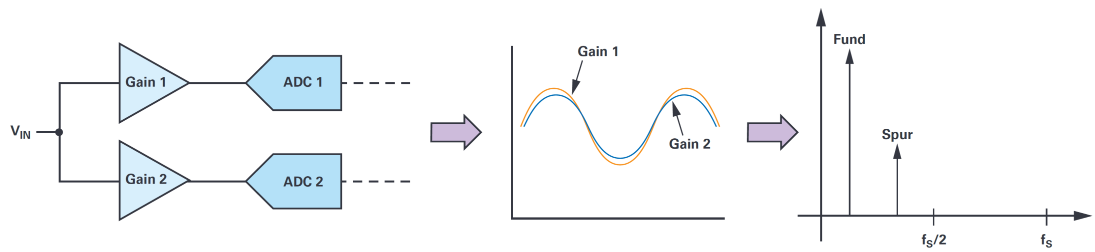


Figure 2.9.: Placeholder: Gain-Mismatch in Interleaving [Har19]

In the time domain, *timing mismatch* due to group delay in the analog circuitry of the ADC and clock skew[3] can occur. The group delay in analog circuitry can vary between the converters. Furthermore, the clock skew has on the one hand an aperture uncertainty component at each of the ADCs and on the other hand a component related to the accuracy of the clock phases, which are input to each converter. [Har19] This mismatch also produces a spur at $f_s/2 \pm f_{\text{in}}$ (see Figure 2.10).

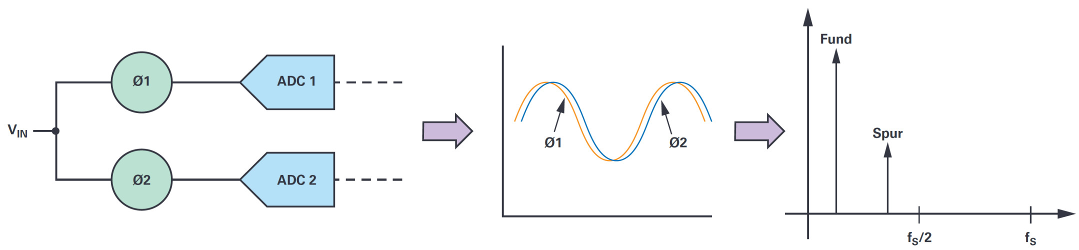


Figure 2.10.: Placeholder: Timing-Mismatch in Interleaving [Har19]

[3]Difference in arrival time of the clock signal at different components.

The last possible mismatch is the *bandwidth mismatch*, which contains both gain and phase/frequency component (see Figure 2.11). Due to bandwidth mismatch, different gain values at different frequencies can be seen. An additional timing component causes different delays for signals at different frequencies through each ADC. Just like gain and timing mismatch, the bandwidth mismatch causes a spur at $f_s/2 \pm f_{\text{in}}$.

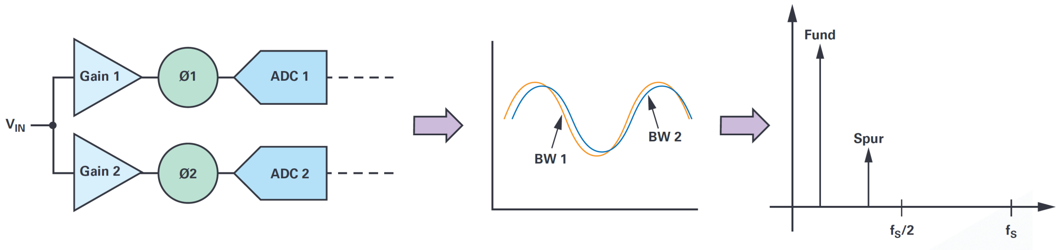


Figure 2.11.: Placeholder: Timing-Mismatch in Interleaving [Har19]

Implementation

The delay step size must be small enough, such that the ADC interleaving technique section 2.2 can be implemented. The ADCs on the read-out card sample at a maximal sample rate of 2.5 GS/s, meaning during the time

$$t_s = \frac{1}{2.5\,\mathrm{GS/s}} = 400\,\mathrm{ps} \tag{2.2}$$

all 16 ADCs have to be clocked one time. This means, a delay step can not be greater than ${}^{400\,\mathrm{ps}}/_{16} = 25\,\mathrm{ps}$.

Clock to THA: 2 GHz $\rightarrow$ Step size for delay:

$$\frac{1\,\mathrm{ns}}{16\,\mathrm{channels}} = 62.5\,\mathrm{ps} \tag{2.3}$$

Aperture delay, jitter, need to be taken into account to determine the max. sampling frequency.

The necessary step size for the delay chips, when using 16 ADC@2 GS/s in time-interleaving mode, is: $\frac{2\,\mathrm{GS/s}}{16} = 31\,\mathrm{ps}$ However, providing individual clocks to the ADCs is not possible on the ZCU216 card. ADCs are grouped together into tiles, each tile containing four converters. One single reference clock signal is propagated to all tiles. Sampling clock is adjusted at each tile individually, however this clocking signal is the same for all of the four converters in the tile. Normally, only one reference clock can be provided. Analyzing the schematic of the ZCU216 board revealed however, that there are pins leading to the FPGA banks (224 to 227), labeled as clocks for the individual tiles. Two of the clocks are not connected (224 and 227). 225 is provided via SMA cable, the other comes from the LPAM clock connector.

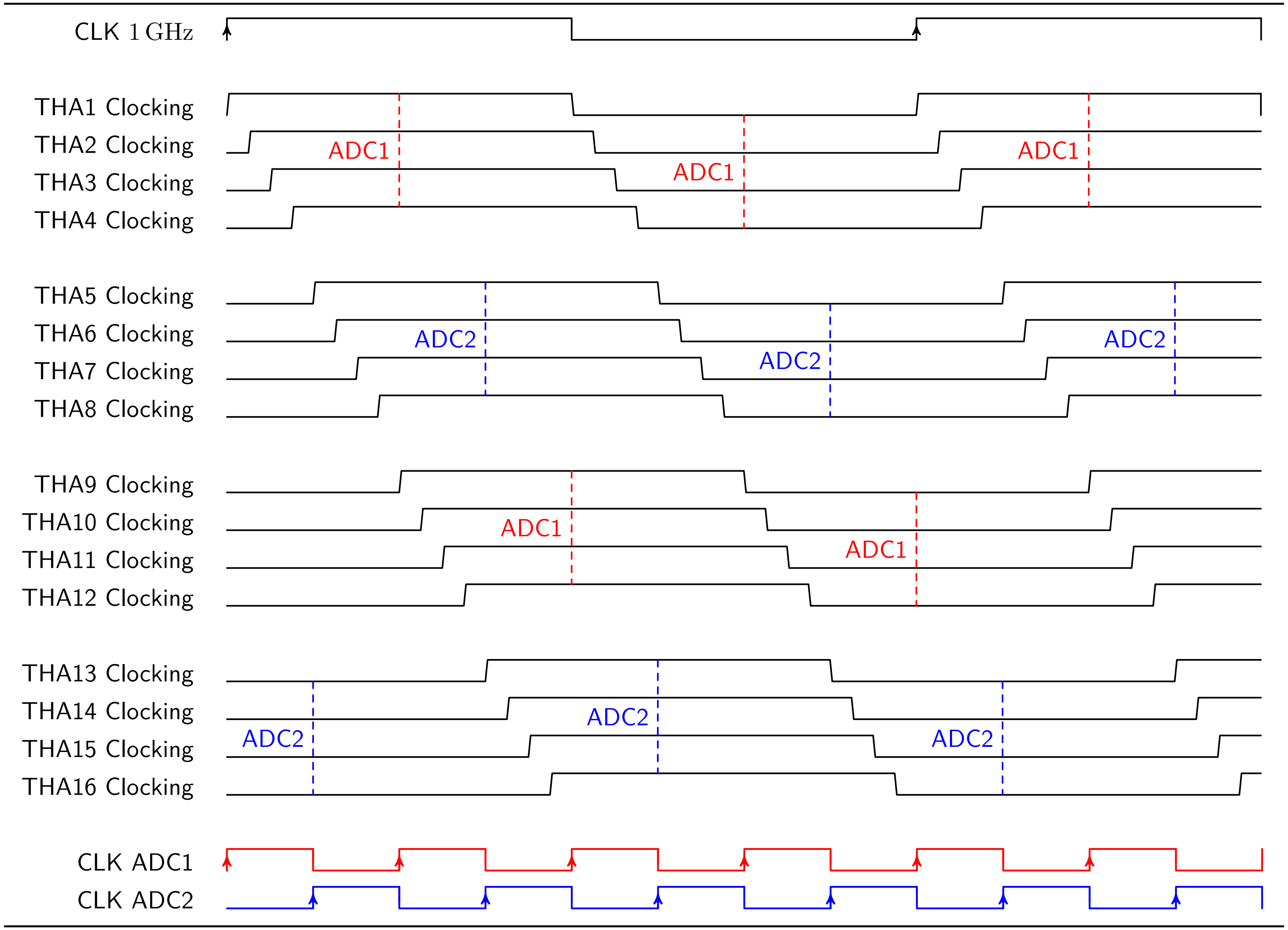


Figure 2.12.: THA Timing diagram. Shows the clocking of the THA (HIGH = hold mode, LOW = track mode). Dashed line represents the sampling of the ADC.

Readout Card

TODO

Selection Of The Card

When selecting the Readout Card, following criteria need to be considered:

- Integrated ADCs
- Number, resolution and bandwidth of ADCs
- Peripheral connections
- Flexibility/Customization
- Suitable connectivity for high-data-throughput

Footprint of using all discrete components is, as one can imagine, higher, than if you integrate all the parts into on Integrated Circuit (IC). Not only the footprint is a concern, but also the number of connections. ADCs with high resolution, a high number of ADCs therefore explodes the necessary amount of connections. High number of ADCs also means

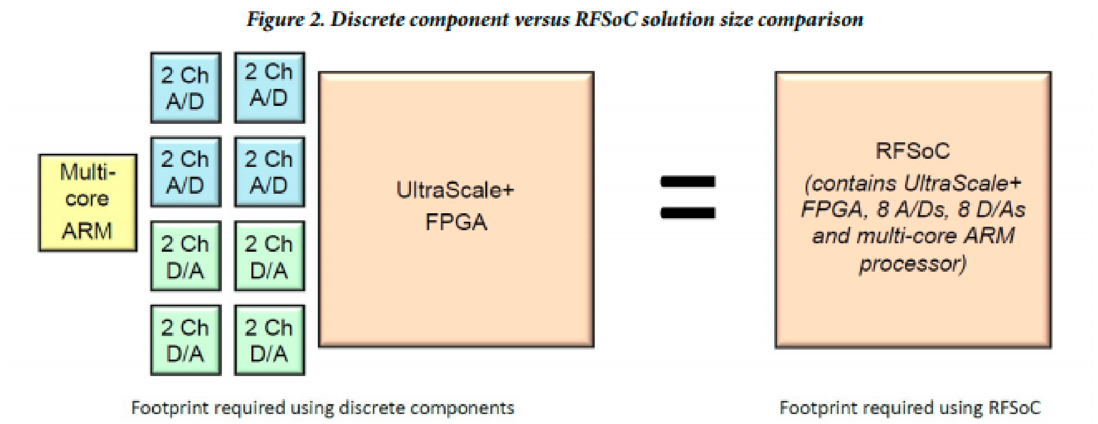


Figure 2.13.: Placeholder: Discrete vs IC

3. Design Of The Front-End Sampling Card

In this chapter, the process of designing the front-end sampling card is described. Designing a Printed Circuit Board (PCB) is a two step process: circuit design and layout design. In this thesis, the software used to cover both of these steps is PADS xDx Designer (for schematic capture) and PADS Layout/Router (for PCB layout design) from Mentor Graphics (subsidiary of Siemens).

3.1. Schematics

Without knowing which components are needed and how they are interconnected, it is impossible to manufacture any board, no matter how high or low the level of complexity is. The schematic is a graphical documentation of an electrical circuit, showing the needed components and their interconnections using standardized symbols. Furthermore, a schematic provides a starting point for automatic placement and routing, i.e. where the components are placed and how they are connected on the physical PCB, which is done with the layout design tool. During the creation of the schematics, the following points have to be considered:

- Deciding which components are needed and what the performance requirements are. Especially for high-speed components carefully considering specifications like signal rise and fall times, jitter, skew, etc. is crucial to achieve the overall expected performance.
- Keeping in mind how many pins are available for high- and low-speed peripheral connections, control signals, etc. Many components have an interface for programming (e.g. Serial Peripheral Interface (SPI)) which requires several pins that need to be connected to the controlling unit. Especially for boards with a lot of components this can quickly become an issue.
- Checking the signaling interfaces of the components. Additional circuitry might be needed for interfacing between two different components. Some signaling interfaces, like Low Voltage Differential Signaling (LVDS), require a specific voltage level, which might result in the need of voltage level translators.
- Keep in mind the different common mode voltages at input/output pins of different components and placing decoupling capacitors if needed.
- Consider placing additional filtering for power supplies in order to reduce noise and PCB, as well as recommended filters from manufacturers of the components.
- Choose suitable type and amount of power supplies/voltage regulators.
- Keep in mind the packaging/Size of the components. The size of the component is important, as space on the board is limited. The package introduces additional capacitive/inductive parasitics, which can be a problem for precise filtering circuits.

- Consider the power dissipation of the components. Components like for example voltage regulators might need coolers or heat sinks. These additional elements might not pose any problems for components which are located on the top side of the board. However, components on the bottom side might create a space issue, if the designed PCB should be mounted on another board.
- For mixed-signal boards, i.e. boards containing digital and analog signal paths, analog and digital ground should be separated. For ICs like THAs or ADCs, where both analog and digital signals are present, connecting the grounds via appropriate components needs to be considered.
- Check if the components are still available and if they can be delivered in the given project time.

This list is certainly not complete, but provides an overview over the most important points which need to be taken into account during design. Decoupling techniques and separation of analog and digital ground are explained a bit more detailed, being very important and crucial steps for design of high-performance PCB.

Decoupling techniques

Probably the most important part in schematics design is proper decoupling of power supplies, as ICs require a stable voltage on the power supply pins for optimal performance. Any ripple[1] or noise can substantially degrade the performance of the ICs, i.e. by decreasing the noise margin. *Noise margin* defines the difference between the useful signal and noise. A sufficient noise margin is necessary to guarantee that the output signal will still be correctly interpreted, even if some noise is added to the signal. Variation on the power supply produces also a variation on the signal and can therefore lead to a smaller difference between signal and noise.

Usually, manufacturers give information about proper power supply decoupling circuits for their component in the data sheet. If this is not the case, there are basic rules of thumb which can be followed to ensure proper decoupling. [Anac]

Basically, two types of voltage variations on the power supply pin can be distinguished: low frequency and high frequency variation. Low frequency variation occurs for example due to devices (or parts of them) being enabled/disabled or in the event of data traffic or data processing. The current draw during these occurrences can not be compensated immediately by the voltage regulator providing the supply voltage, which leads to drops in the voltage level. Time frames of this variation vary in the range of milliseconds up to days. High frequency variation results from switching events in the device, occurring in the range of the clock frequency and the corresponding harmonics up to about 5 GHz. Spikes due to Electro-Magnetic Interference (EMI) are also a source of high frequency variation and need to be compensated for. [Xil]

Ideally, one capacitor, which acts as a low-pass filter, should be enough to mitigate these variations. A real capacitor however has parasitics and thus can in general not be modeled by a “pure” capacitive behavior. This reduces the filtering performace Additional resistances and inductance need to be considered [Anac]:

- A parallel resistance R_P, which shunts the nominal capacitance (C), representing insulation resistance or leakage.
- A series resistance R_S, or Equivalent-Series-Resistance (ESR), which represents the plates and the leads of the capcitor.

[1] *Ripple* is additional Alternating Current (AC)-voltage (of small amplitude) superimposed on a the general voltage level.

- A series inductance L_S, or Equivalent-Series-Inductance (ESL), that models the inductance of the plates and leads of the capacitor.
- A parallel resistance and capacitance, R_D and R_C, which model the effect called dielectric absorption. This denotes the phenomenon, that a capacitor which has been charged for a long time, doesn't fully discharge when briefly discharged. Dielectric absorption can be detrimental for high-precision use-cases, for power supply decoupling this effect doesn't have to be considered.

Consideration of all these effects leads to the equivalent circuit shown in Figure 3.1. It can be seen that this forms a RLC circuit, meaning the capacitor will not have the ideal behavior over the whole frequency range. In fact, a real capacitor shows an impedance response as seen in Figure 3.2, which resembles one of a band stop, rather than a low pass. Typical capacitive behavior is seen in region (I). Region (II) shows the influence of the ESR, which is why there is a residual impedance at the lowest point. Region (III) showcases the effect of the ESL. To extend the capacitive behavior over a wider frequency range, at least two capacitors are placed.

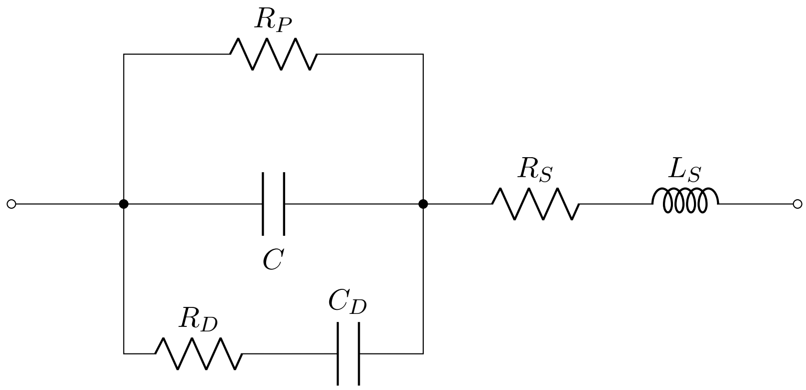


Figure 3.1.: Equivalent circuit of a real capacitance (redrawn from [Anac])

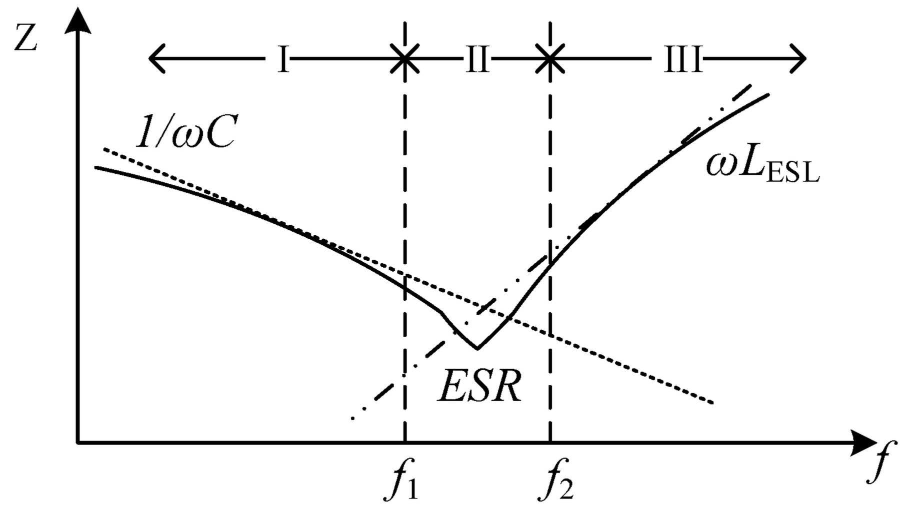


Figure 3.2.: Qualitative impedance response of a real capacitance [DK20]

To deal with the low frequency variation, a large capacitor (typical values: 10 µF to 100 µF) is placed next to the component, not more than 5 cm away. The role of this capacitor is to be a charge supply for the instantaneous needs of the device, i.e. keeping a constant voltage level until the slower control loop of the voltage regulator can compensate for the changed current draw. [Anac] This capacitor is also called *decoupling capacitor*.

Another, small capacitor (typical values: 0.01 µF to 0.1 µF) is placed as close as possible to the power pins of the component. This capacitor should bypass (therefore also called *bypass capacitor*) the high frequency variation on the power supply line. [Anac]

To cover a larger frequency range, multiple capacitors can be used.

All capacitors should be connected through vias or short traces to a large area, low impedance ground plane. Vias on a PCB are used to connect different layers, a plane is an uninterrupted area of metal covering the whole (or part) of a PCB layer (basic PCB structures are also explained in section 3.2). Connecting capacitors in this way minimizes the inductance due to connection traces. [Anac]

An optional ferrite bead in series with the supply pin keeps external high frequency from the device and the noise generated inside the component from the rest of the board. [Anac]

3.1.1. Connectors

The number and type of connectors is primarily defined by the read-out card, on which the sampling board is mounted. The different connector types serve different purposes, which can be organized into three categories.

Digital Control Signals

For digital control signals (i.e. SPI, enable signals, …) and clocking a VITA 57.4 FMC+ connector from *SAMTEC* is used (see Figure 3.3).

FPGA Mezzanine Card (FMC) is a standard defined by VMEbus International Trade Association (VITA) to provide a standard mezzanine card[2] form factor, connectors, and modular interface to a FPGA located on a base board (carrier card). [See09] The FMC+ standard extends the pin count and throughput of the present high-speed interfaces.

This connector provides 560 pins arranged in a 14×40 array, 80 of which are additional high-speed interfaces, located on either side of the connector (therefore this connector type is also called High Serial Pin Count Extension (HSPCe) connector, as opposed to the HSPC connector which doesn't have additional rows). For user-defined purpose 160 pins are available. They can be used as single-ended or differential pins. Clocking capable pins can be used to propagate clock signals from the mezzanine to the carrier board.

Furthermore, the connector provides pins for power supply from carrier board to mezzanine card. [FMC] The voltage levels provided are listed in Table 3.1.

Table 3.1.: Voltage levels for power supply provided by the FMC+

Voltage	Max. current	Max. capacitive load
V_{ADJ}, 0 V to 3.3 V	4 A	1000 µF
3.3 V	3 A	1000 µF
12 V	1 A	1000 µF

An assembly drawing of the FMC+ connector is shown in Figure 3.3.

Analog Signals

The signal from the detector is provided to the THAs through SubMiniature version A (SMA)[3] RF connectors from *molex*, which are mounted at the edge of the board. Figure 3.4 shows a 3D model of this connector type.

[2] A PCB which is plugged on a plug-in board. [PCM]
[3] Coaxial RF connector

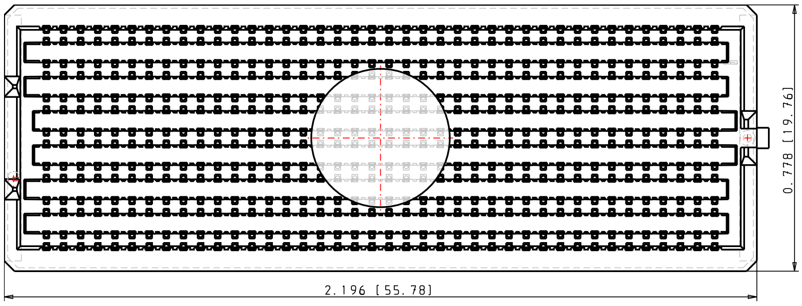


Figure 3.3.: Part drawing of FMC+ connector [SAM]

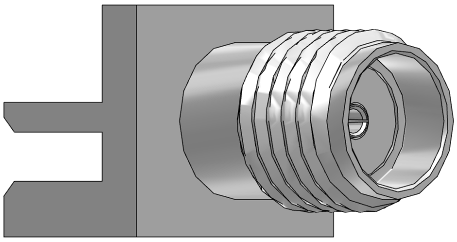


Figure 3.4.: 3D model of the edge-mount RF SMA connector from *molex* [mol]

On the read-out board two RFMC 2.0 (RF Mezzanine Card) interface connectors are provided. The connectors used are Low Profile Array, Female (LPAF) connectors from *SAMTEC* with 400 pins arranged in a 8×50 array. One connector is dedicated for transmitting signals from the mezzanine card to the on-board ADCs. The other provides the analog output from the on-board DACs[4] to the mezzanine card. On the sampling board, the male counterpart of the connectors, Low Profile Array, Male (LPAM), is used (see Figure 3.5).

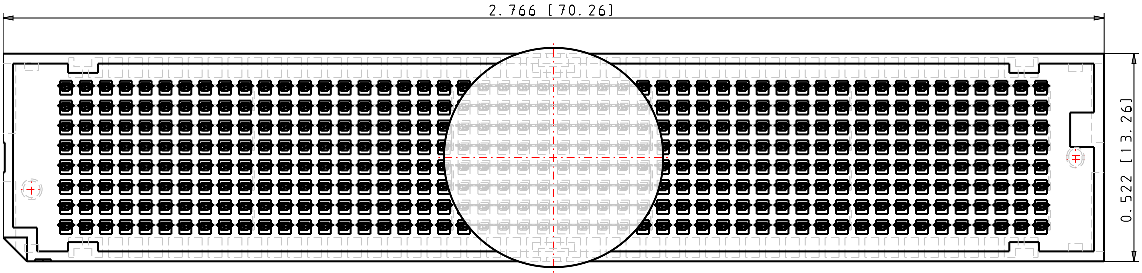


Figure 3.5.: Part drawing of a LPAM 8×50 connector

Clock Signals

The clock signals from the PLLs on the sampling board are propagated in different ways. The reference clock for the FPGA is propagated through the FMC+ connector. Clocking for the ADCs and the DACs is provided through a 6×20 LPAM connector (see Figure 3.6).

[4] A DAC translates digital values into an analog signal.

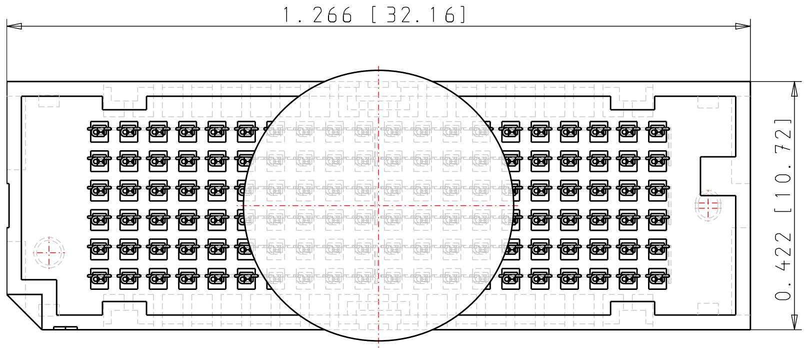


Figure 3.6.: Part drawing of LPAM 6 × 20 connector

The clock coming from KARA is provided through RF SMA connectors directly to the PLL.

3.1.2. Sampling-Channel

The sampling channel consists of the THA, which is driven by a delay chip.

Track-And-Hold-Amplifier

The THA used is the same as in KAPTURE. The component was chosen due to its high bandwidth (4 GHz) and low jitter(range of hundreds of femtoseconds). [CBC+13] Therefore it is also a good candidate for the new system.

According to the data sheet [Anad], the component shows the characteristics listed in Table 3.2. These input specifications are important for later connection with the delay chip. Switching characteristics are important for estimation of the maximal sample frequency possible and overall performance of the system.

Table 3.2.: Specifications of the HMC5640 THA

Parameter	Min	Typ.	Max	Unit
Analog Inputs				
Differential FS Range		1		Vpp[1]
Common mode voltage	-0.1	0	0.1	V
Clock Inputs				
DC Differential High Voltage (Track Mode)	20	40	2000	mV
DC Differential Low Voltage (Hold Mode)	-2000	-40	-20	mV
Common mode voltage	-0.5	0	0.5	V
Analog Outputs				
Differential FS Range		1		Vpp
Common mode voltage		0		V
Track-to-Hold/Hold-to-Track Switching				
Aperture Delay		-6		ps
Random Aperture Jitter (FS, 1 GHz)		< 70		fs
Settling time[2] (to 1 mV)		116		ps

[1] Volt peak-to-peak
[2] *Settling time* is the interval between the internal track-hold transition and the time when the output signal is settled within the specified value.

As the analog input to the THA is single-ended, a 50 Ω termination on the unused input pin has been added, as recommended in the data sheet.[Anad]

The differential outputs are connected to the corresponding RFMC LPAM 8x50 connector pins.

At the power pins, decoupling capacitors and a ferrite bead were placed. The THA is a crucial component, as it samples the detector signal, therefore any possible noise should be reduced to a minimum.

The schematics of the THA is shown in Figure 3.7.

Separating Analog and Digital Ground

TODO: more explanation?

Digital ground is more noisy than analog ground due to switching of the digital components. Analog components are more susceptible to noise (due to e.g. lower amplitudes) than

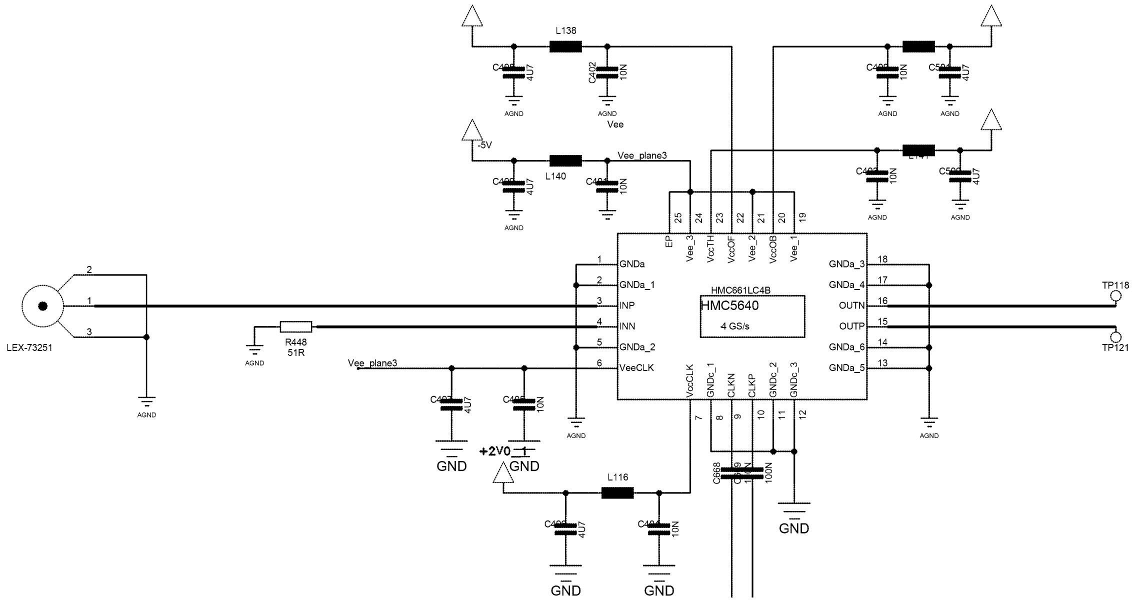


Figure 3.7.: HMC5640 THA schematic

digital components (as they operate with discrete voltage/thresholds representing "high" and "low" states) and need a clean ground. In a mixed-signal (having both analog and digital signals) PCBs analog and digital ground should be therefore well separated. For some mixed-signal components, such as THAs, where separate analog and digital ground pins are provided, it is however recommended to connect both grounds directly at the component. For the THAs in this design, this is done by connecting the ground pins via ferrite bead at each THA (see Figure 3.8). The ferrite bead mitigates any high-frequency components and therefore protects the analog ground from noise.

Current through the bead creates a voltage which could potentially lead to electrical breakdown. Two back-to-back diodes Figure 3.8) are placed in parallel in order to limit this voltage to 0.6 V to 0.7 V (diodes become conducting in this voltage range).

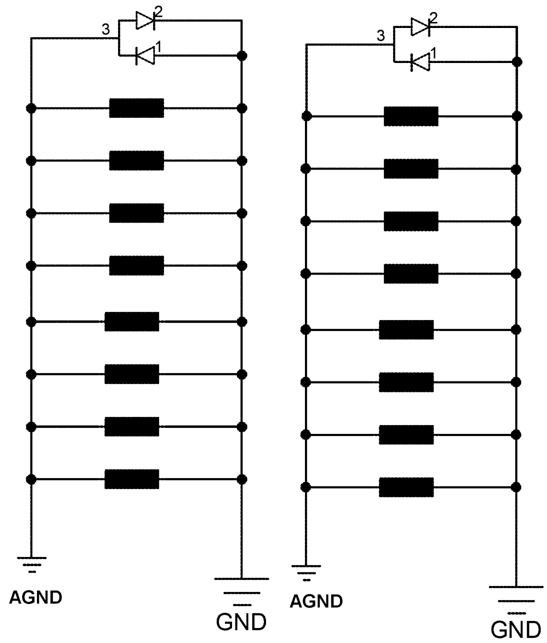


Figure 3.8.: Connection of the analog and digital grounds at the THAs

Delay Chip

The delay chips are used to create a delay in the clocking signals which go to the THA chip. For the selection of the delay chip, the most important characteristic, apart from jitter, is the delay step size and delay range.

As indicated in paragraph 2.2, the step-size of the delay chip must not exceed 25 ps to use the technique with ADCs sampling at 2.5 GHz.

With the HMC856 programmable delay chip from *Analog Devices*, which is also used for the KAPTURE sampling board, a minimal step size of 3 ps [Anab] is possible. This is much less than 25 ps and thus the chip could be potentially used for the intended purpose. However, one drawback is the maximal delay range of 100 ps. Considering a signal, which is stretched over several nanoseconds, this range limits the possibility to freely chose the overall timing resolution. Another problem is the programming interface of the chip, which consists of five differential Current Mode Logic (CML) inputs. This means, one chip already takes up 10 pins only for control signals. For in total 16 necessary delay chips, this results in 160 pins used only for control of the delay chips. This uses up all pins of the FMC+ connector (see subsection 3.1.1) available for user-defined purpose.

A better candidate is the dual channel programmable delay chip NB6L295 from *ON Semiconductor*. This chip provides two separately programmable delay channels. This has the benefit of reducing the total chip count by half, as now two THAs can be connected to one delay chip.

The minimal delay step size of 11 ps lies under the maximal allowed 25 ps. Therefore the chip is suitable for the targeted interleaving method, covering a total delay range from 3.2 ns to 8.8 ns per delay channel.

The chip is programmed via Serial Data Interface (SDI), which only requires 4 pins (enable pin, data pin, clock pin, load pin). Thus, the total number of digital control pins used by the delay chips is $4 \cdot 8 = 32$, which is a significant reduction compared to the 160 control pins needed by the HMC856 chips. This number can be even more reduced, by propagating the same data, clock and load pins to the chips and providing the enable signal on individual lines to the respective chip (see Figure 3.9). In this way, only 11 pins (8 enable pins and 3 pins for data, clock and load) are needed in total for programming all delay chips.

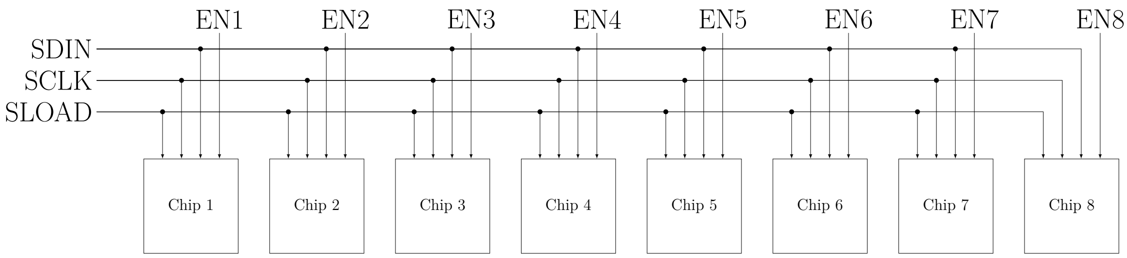


Figure 3.9.: Diagram of the SDI control pins for the NB6L295 delay chip. The data (SDIN), clock (SCLK) and load (SLOAD) pins are shared by all chips. Only the enable (ENx) signals are routed individually.

The schematic of the delay chips is shown in Figure 3.10.

Inputs

The inputs of the delay chip are driven by the preceding PLL, the outputs of which are Low-Voltage Positive Emitter-Coupled Logic (LVPECL) drivers. According to the data sheet, when driving the inputs with a LVPECL driver, the VTx and $\overline{\text{VTx}}$ pins of the delay

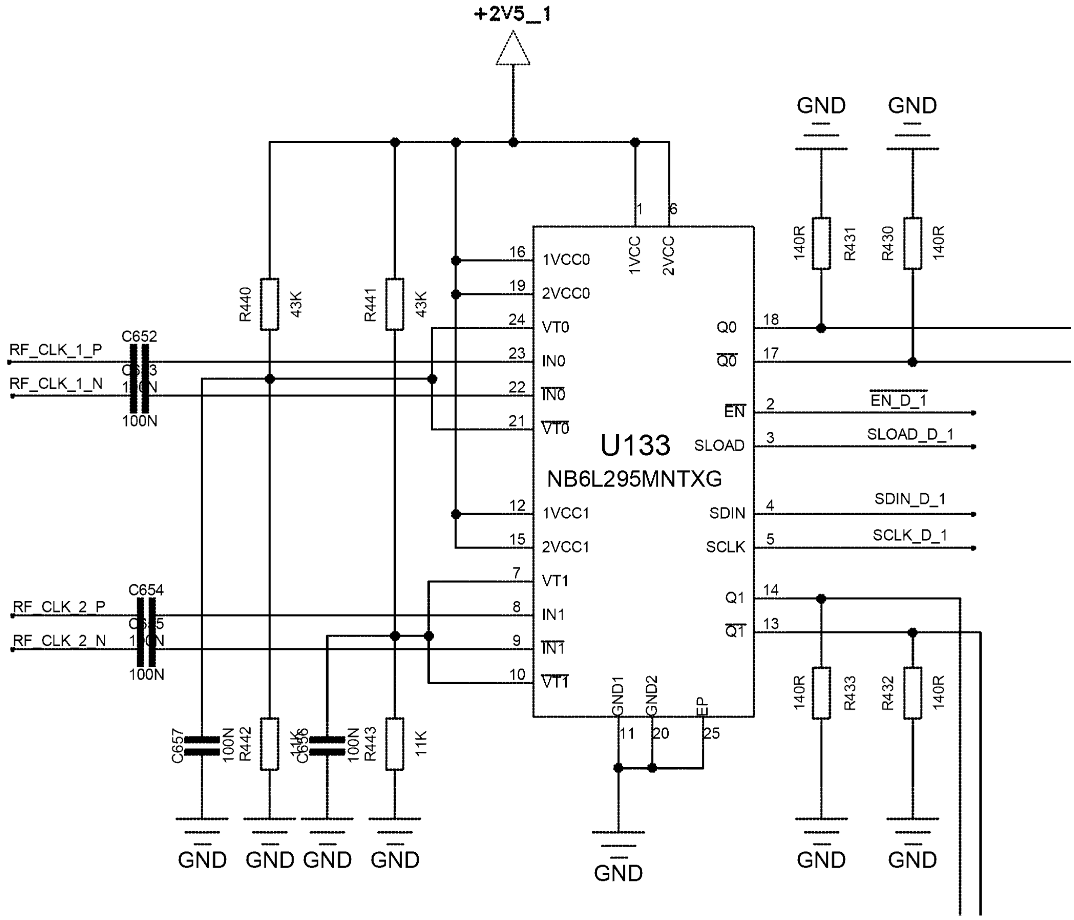


Figure 3.10.: NB6L295 delay chip schematic

chip need to be connected to $V_{cc} - 2\,\text{V}$ (see Figure 3.12). In case of $V_{cc} = 2.5\,\text{V}$, this results in a voltage level of $\text{VTx} = \overline{\text{VTx}} = 0.5\,\text{V}$.

To avoid using an additional voltage regulator, this voltage level is achieved by using a resistive voltage divider connected to V_{cc}. A voltage divider with the resistors R_1 and R_2 (see Figure 3.11) produces a voltage V_{out} which is a fraction of the input voltage V_{in}. V_{out} is calculated as

$$V_{\text{out}} = \frac{R_2}{R_1 + R_2} V_{\text{in}} \tag{3.1}$$

The resistor values are chosen to be $R_1 = 43\,\text{k}\Omega$ and $R_2 = 11\,\text{k}\Omega$. According to Equation 3.1 this results in a voltage of

$$V_{\text{cc}} \frac{11\,\text{k}\Omega}{11\,\text{k}\Omega + 43\,\text{k}\Omega} = 0.5093\,\text{V} \approx 0.5\,\text{V} \tag{3.2}$$

at the VTx and $\overline{\text{VTx}}$ pins. Resistor values are chosen high to minimize current flow. A 100 nF capacitor is put in parallel for V_{cc} decoupling.

According to the data sheet [ON], the digital control pins need an input HIGH voltage of at least 2 V. Directly connecting to the FMC+ connector pins is therefore not possible, as the maximal level on these pins can be 1.8 V. The SN74AVC32T245 bus transceiver from *Texas Instruments* is able to shift signals from one voltage level to another. In this design, the bus transceiver is configured to propagate signals from the "A" ports (coming from the FMC+ connector) to the "B" ports (going to the delay chips), shifting the signals from the 1.8 V of the FMC+ connector (V_{ADJ}) to 2.5 V (see Figure 3.13). Furthermore, resistors are

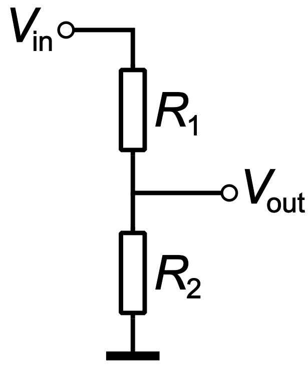


Figure 3.11.: Schematic of a resistive voltage divider

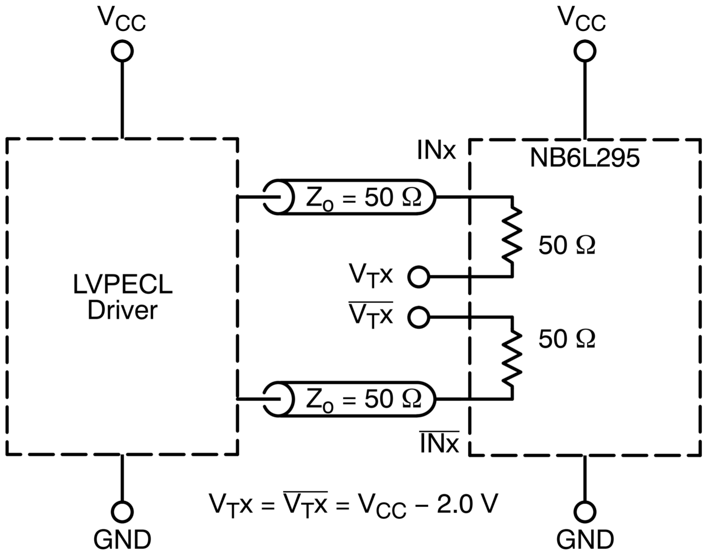


Figure 3.12.: LVPECL recommendations for NB6L295 [ON]

place at the pins to reduce possible voltage overshootings which result from reflections on the line.

Outputs

The output of the delay chip is using a LVPECL signaling interface, which is based on an open-emitter topology (see Figure 3.14). This requires a path to Direct Current (DC), which is achieved by adding 140 Ω resistors.

As the output will be connected to the THA, it is necessary to check the compatibility of the maximum amplitude and common-mode of the pins.

According to the data sheet [ON], the voltage level of the output can vary between $V_{cc} - 1825\,\mathrm{mV}$ and $V_{cc} - 825\,\mathrm{mV}$ (see Table 3.3). Maximal voltage amplitude acceptable by the THA inputs is 2000 mV (see Table 3.2). When using a supply voltage of $V_{cc} = 3.3\,\mathrm{V}$, provided e.g. by the read-out card through the FMC+ connector, this leads to a maximum output level of 2475 mV. This exceeds the limit given by the THA. Therefore, for V_{cc} a smaller voltage should be considered. In this design a voltage of $V_{cc} = 2.5\,\mathrm{V}$ is chosen, which guarantees that the amplitude falls within the range 675 mV to 1675 mV.

The second point to consider is the common mode voltages. According to the data sheet of the THA, the common mode voltage of the input clock pins is 0.1 V (see Table 3.2). The

Table 3.3.: Specifications of the NB6L295 delay chip [ON]

Parameter	Min	Typ.	Max	Unit
Outputs				
Output HIGH Voltage	$V_{cc} - 1075$	$V_{cc} - 950$	$V_{cc} - 825$	mV
Output LOW Voltage	$V_{cc} - 1825$	$V_{cc} - 1725$	$V_{cc} - 1625$	mV
Common mode voltage	-0.1	0	0.1	V
AC Characteristics				
Random Clock Jitter RMS		3	10	ps
Output Rise/Fall Times (@50 MHz)	85	120	170	ps
Serial Clock Input Frequency (50% Duty Cycle[1])			20	MHz
Minimum Pulse width SLOAD	1			ns

[1]Percentage of the ratio of pulse width and total period of the waveform.

common mode voltage of the delay chip is not explicitly mentioned in the data sheet, thus it has to be calculated.

The common mode voltage V_{CM} is just the mean value between the high level and the low level voltage of the output pins:

$$V_{\mathrm{CM}} = \frac{V_{\mathrm{out,\ LOW}} + V_{\mathrm{out,\ HIGH}}}{2}. \tag{3.3}$$

According to this, the common mode voltage V_{CM} of the delay chip output, when taking the minimum/maximum voltage level values, is

$$V_{\mathrm{CM}} = \frac{675\,\mathrm{mV} + 1675\,\mathrm{mV}}{2} = 1175\,\mathrm{mV}. \tag{3.4}$$

This is higher than the maximal input common mode voltage of the THA. AC coupling is therefore necessary in this case, i.e. connecting the pins via capacitors.

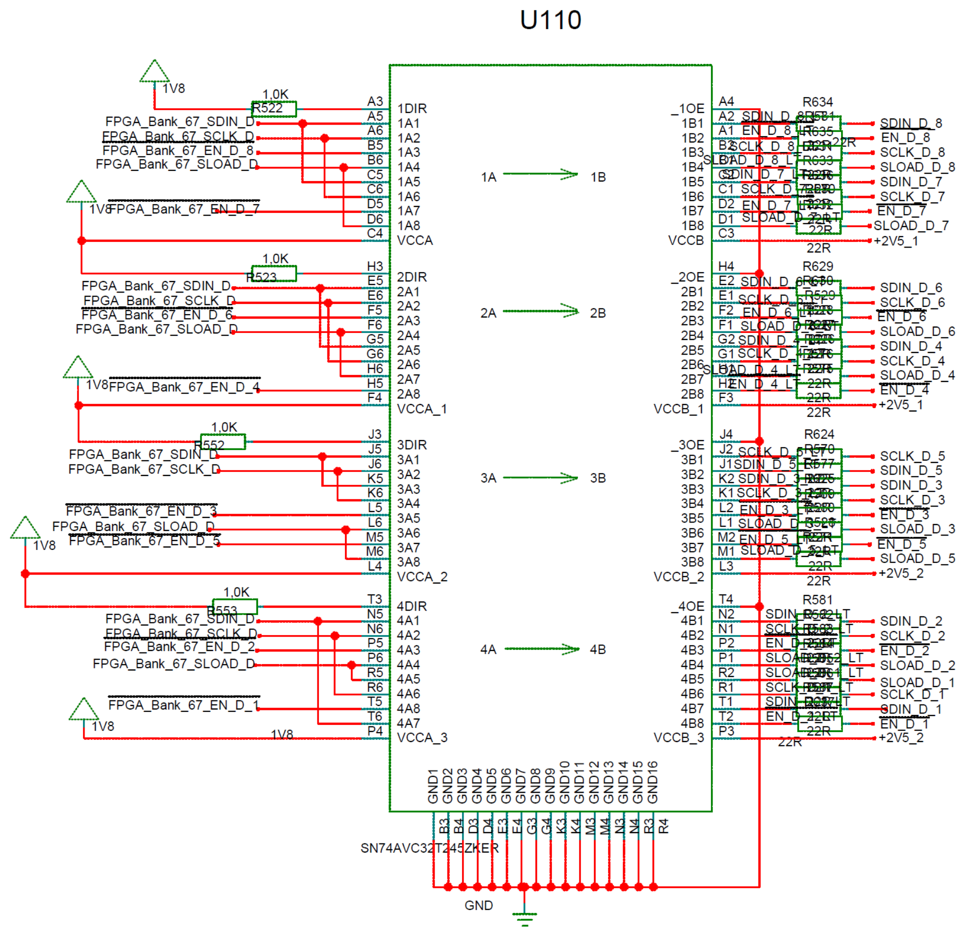


Figure 3.13.: Picture to be replaced. Schematic of the SN74AVC32T245 bus transceiver

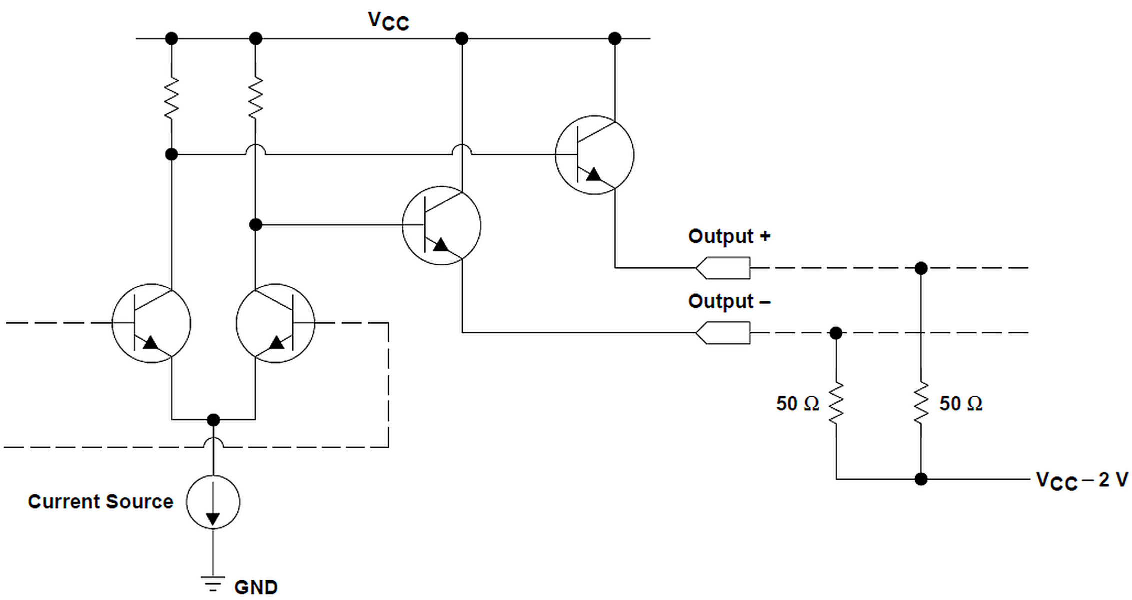


Figure 3.14.: LVPECL driver topology. Left side shows the emitter-follower based driver. On the right, an example biasing with resistors is shown. [Mik]

3.1.3. Clock Distribution

The clock distribution is designed as shown in Figure 3.15.

The LMK04808B low-noise clock jitter cleaner with dual-loop PLLs from *Texas Instruments* cleans the incoming reference clock provided from the system (e.g. from KARA) for high temporal accuracy [CBC+13]. It is used with an external Voltage-Controlled Crystal Oscillator (VCXO) from *ABRACON*.

The LMK04808B contains two PLLs (therefore called “dual-loop”). The first PLL is used to clean the jitter from the reference clock. The second is then used to create a higher frequency clocking signal out of the cleaned clock.

The LMK04808B has only 12 outputs which is not enough for the 16 THAs and additional clock signals needed for FPGA, ADCs and DAC. Furthermore, the outputs are divided into six groups à two outputs. Outputs in one group have the same configuration (frequency, phase, ...), which means that effectively only six different outputs are available.

Therefore, a low noise clock distribution fan-out buffer, the HMC987LP5E from *Analog Devices*, is used for distributing the clock signal to the delay chips. As one fan-out buffer has eight outputs, two chips are needed to cover all 16 channels. These chips get the output clock signal from two pins of the LMK04808B. To ensure exactly identical clocking signals, both of the pins are chosen to be in one output group.

One output of the PLL is propagated to the FMC+ connector as reference clock for the FPGA. Up until this part, this clocking distribution architecture is not different from the one on the KAPTURE sampling board.

The maximum output frequency of the LMK04808B is 1536 MHz, not enough to clock the ADCs at maximum sampling rate (2.5 GS/s). A second PLL is therefore needed. As Figure 3.15 shows, the LMK04808B also provides a clocking signal to other PLLs, the LMX2594 from *Texas Instruments*. This PLL is able of clocking signal frequencies up to 15 GHz.

Due to the ADC clocking limitations on the read-out card explained in paragraph 2.2, two of the PLLs are needed. The reference clock signal is provided by outputs from different output groups of the LMK04808B. This way, the phase of each reference clock can be programmed individually, which allows to implement the ADC clocking technique described in paragraph 2.2.

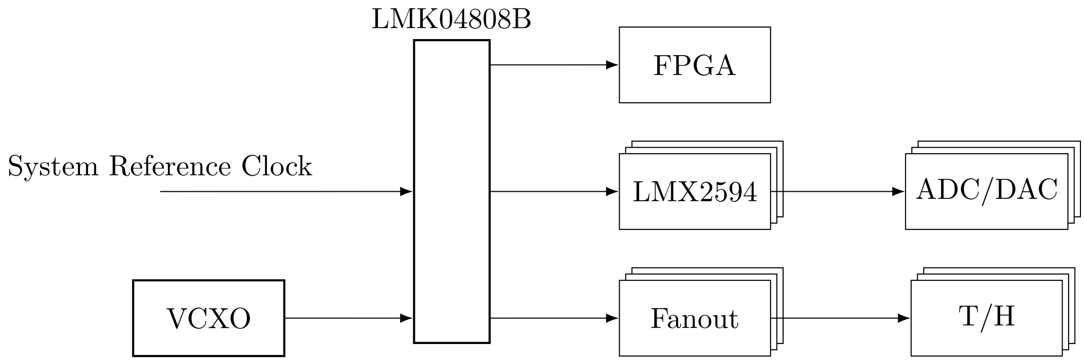


Figure 3.15.: Overview of the clocking paths on the sampling board

PLLs

For proper functioning/best performance, a properly designed loop filter (see Figure 3.16) for both PLLs is needed. The output of the loop filter is the voltage for controlling the Voltage-Controlled Oscillator (VCO), the output of which is a frequency, f_{VCO}, proportional to that voltage. f_{VCO} is divided by the *N Divider* to the frequency f_n and then compared to the phase detector frequency f_{PD} in the phase detector. f_{PD} results from dividing the reference frequency f_{OSC} with an *R divider*. The phase detector produces current correction pulses (with magnitude K_{PD}) with a duty cycle proportional to the phase error between f_{PD} and f_n. These pulses pass through the low pass loop filter, which basically converts these pulses into a voltage. [Ban] The loop filter is therefore the key component to

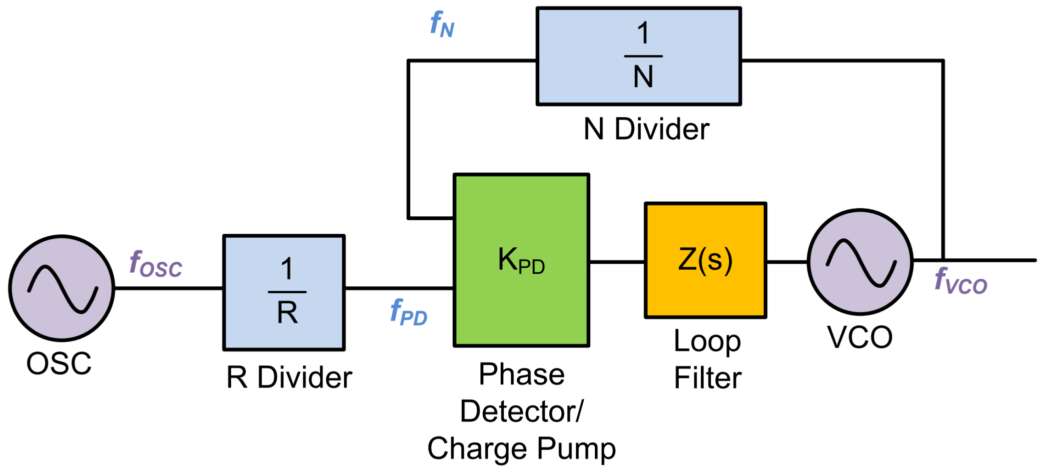


Figure 3.16.: General block diagram of a PLL [Ban]

To calculate the loop filter, the *Texas Instruments PLLatinum Sim* tool is used (see Figure 3.17). This tool provides a convenient way to calculate the necessary loop filter components, given the VCO characteristics, desired filter order, charge pump current and desired performance (e.g. optimize jitter). For the names of the filter components refer to

Figure 3.18.

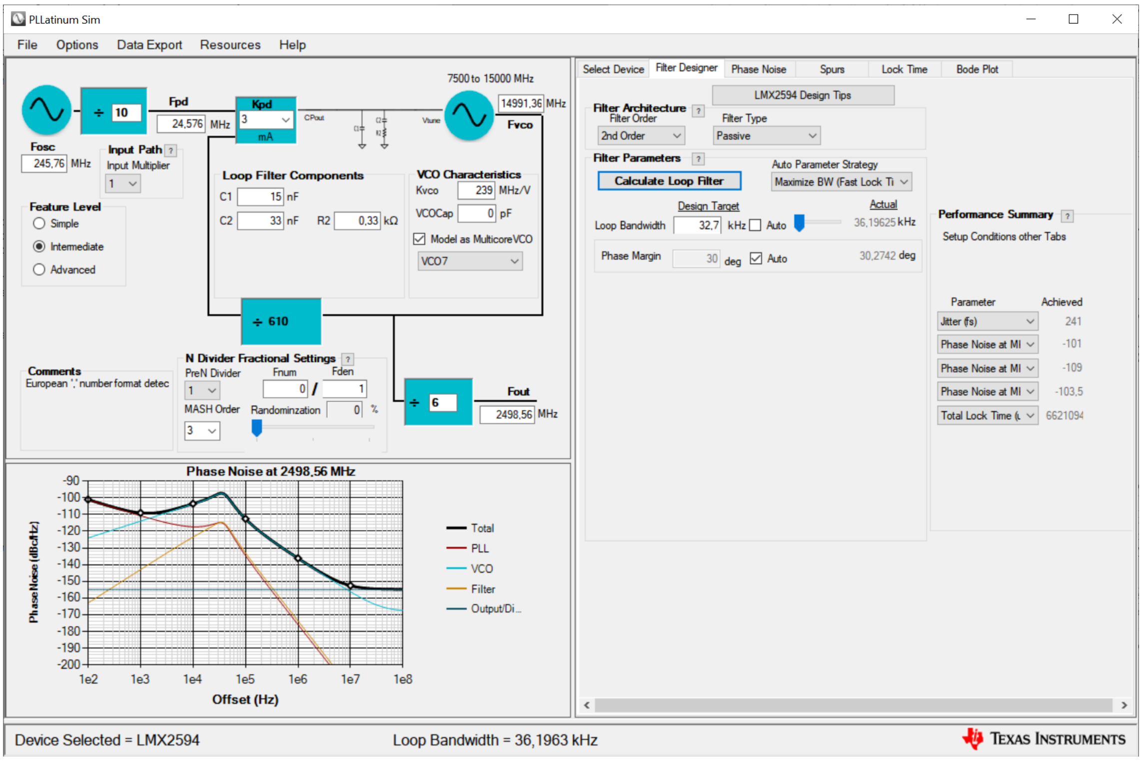


Figure 3.17.: Screenshot of the TI PLLatinum Sim tool for loop filter design and PLL performance simulation

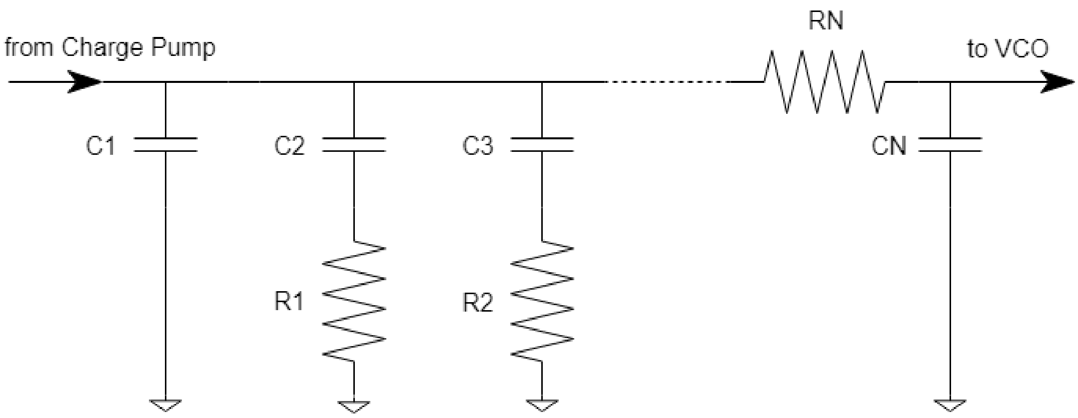


Figure 3.18.: Picture to be replaced. General n-th order passive loop filter for PLL. To reduce the order leave components out.

The LMK04808B has two PLLs inside (PLL1 and PLL2), for both the loop filter has to be calculated separately. The parameters/values are shown in Table 3.4. The filters are implemented as second order filters, note that PLL2 has already a partially integrated loop filter.

The loop filter for the LMX2594 is designed in the same way, the values are shown in Table 3.5. The filter is implemented as a third order passive filter. In order to provide the flexibility to enlarge the filter order (for performance adjustment), some of the components are considered in the schematics, but are either not placed or put to zero. In this way, a placeholder on the board is created. The schematic of the LMX2594 is shown in Figure 3.19.

Table 3.4.: Loop filter characteristics of the LMK04808B

Parameter	Value
PLL1 parameters	
VCO Gain	0.15 MHz/V
Loop Bandwidth	0.2578 kHz
Phase Margin	70°
Effective Charge Pump Gain	0.4 mA
Phase Detector Frequency	25 MHz
VCO Frequency	200 MHz
Loop filter components for PLL1	
C_1	39 nF
C_2	1800 nF
R_2	2.2 kΩ
PLL2 parameters	**Value**
VCO Gain	30 MHz/V
Loop Bandwidth	390.9624 kHz
Phase Margin	70°
Effective Charge Pump Gain	1.6 mA
Phase Detector Frequency	50 MHz
VCO Frequency	3000 MHz
Loop filter components for PLL2	
C_1	22 pF
C_2	2.2 nF
R_2	3.3 kΩ

Both PLLs are connected to the digital 3.3 V coming from the FMC+ connector. For the output buffer supply (`VCC_RFBUF`) of the LMX2594, an additional EMI filter is used to provide a very clean voltage level. The output pins are pulled-up via ferrite bead to `VCC_RFBUF` as recommended in the data sheet.

Table 3.5.: Loop filter characteristics of the LMX3594

Parameter	**Value**
VCO Gain	239 MHz/V
Loop Bandwidth	32.7 kHz
Phase Margin	69°
Effective Charge Pump Gain	3 mA
Phase Detector Frequency	24.576 MHz
VCXO Frequency	Designed for 15 GHz
Loop filter components	
C_1	2200 pF
C_2	180 nF
C_3	1800 pF
R_2	160 Ω
R_3	180 Ω

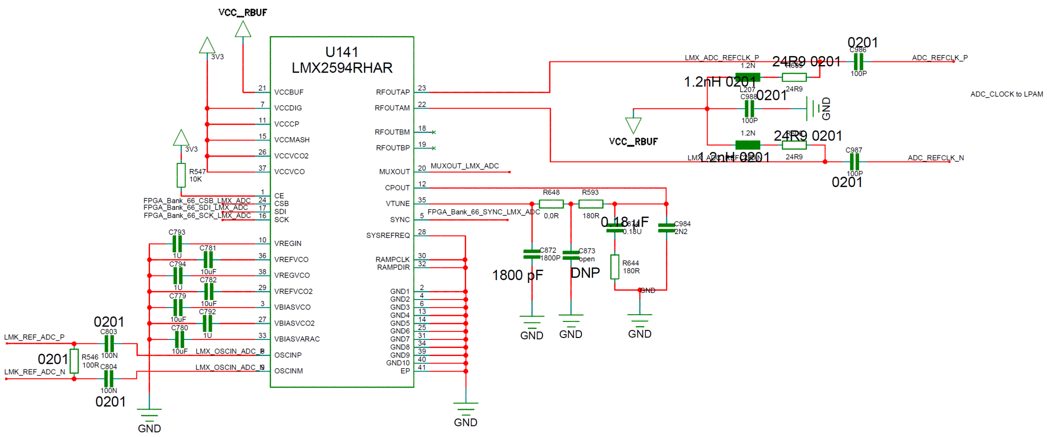


Figure 3.19.: Schematics of the LMX2594

Fanout Buffer

The fanout buffer takes as input the clock signal from the PLL and distributes it to the THAs chips. In this design, the HMC987LP5E from *Analog Devices* is chosen due to its low jitter and low skew performance. The schematics of the chip is shown in Figure 3.20.

Decoupling capacitors are placed at all power supply pins in order to guarantee a clean and stable voltage level.

The outputs of the fanout buffer use LVPECL signaling interfaces and therefore need to be connected to ground via resistor. They can be enabled or disabled either via SPI (setting pin `PMODE_SEL` to ’0’) or by using parallel pin control (setting pin `PMODE_SEL` to ’1’).

In parallel pin control the SPI pins `SCLK`, `SDI` and `SEN` are reinterpreted as a 3-bit control bus. In this mode, the pins are either pulled up to V_{CC} or tied to ground to represent a logic ’1’ or ’0’. For the design, the parallel pin control mode is chosen, therefore the `PMODE_SEL` pin is pulled up to V_{CC} ($\widehat{=}$ logic ’1’). In order to have the opportunity to enable the SPI mode in later usage, a jumper is placed at this pin so that it can be tied to ground ($\widehat{=}$ logic ’0’, enabling SPI mode). For the eventual use SPI mode, the `SCLK`, `SDI` and `SEN`

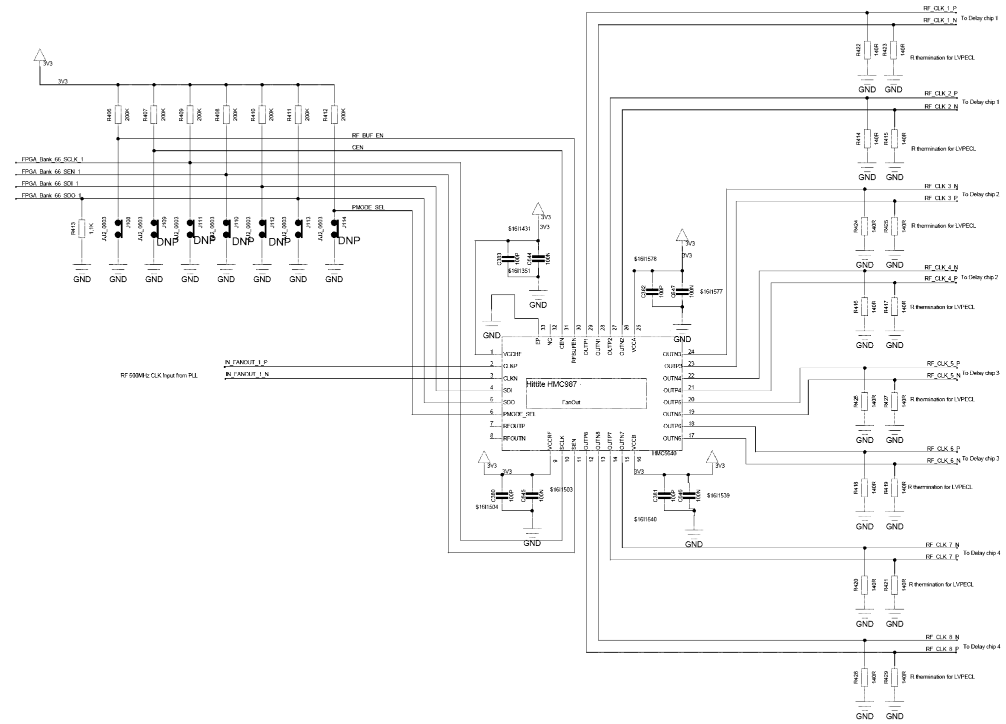


Figure 3.20.: Schematic of the fanout.

pins are connected to the FMC+ connector. To enable all outputs, the SPI pins need to be set to '111' according to the datasheet, i.e. pulled-up to V_{CC}. Here, jumpers are foreseen as well, to allow enabling/disabling in later usage.

3.1.4. Digital-To-Analog-Converter Channels

For test purposes, two DAC channels from the read-out card are routed on the sampling board. In this way, test signals can be generated right on the read-out card, without the need for an external signal generator. The differential inputs from the DACs are transformed into single ended outputs with dedicated baluns[5]. the BD3150N50100AHFa and the BD4859N50100AHF from *Anaren*. These are used for the signal frequency range 3.1 GHz to 5.0 GHz and 4.8 GHz to 5.9 GHz respectively.

The single-ended output is connected to a miniature RF connector from *Hirose Electric*.

The schematic of a DAC channel is shown in Figure 3.21.

[5]**bal**anced to **un**balanced

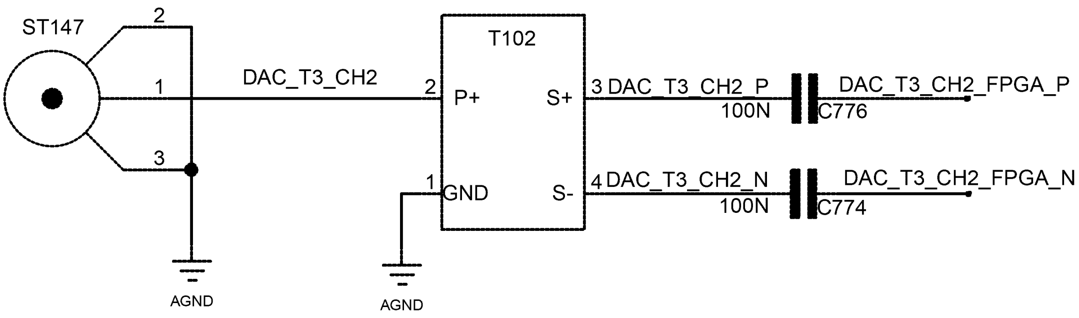


Figure 3.21.: DAC-channel with balun. Signal propagates from right to left.

3.1.5. Power Supply

Stable power supply is the key for best performance of the components. Especially high-performance ICs, such as THAs, highly rely on a stable voltage level for correct functionality. Therefore, proper power supply design is an important step which needs to be handled with care. This step includes choosing the right type and amount of voltage regulators, as well as providing appropriate filtering.

Table 3.6 lists the power supply requirements of all the components used on the board.

Table 3.6.: Power consumption of components on the board

Component	V_{cc} (V)	I_{max} (A)	P_{max} (W)	$\#_{parts}$	$I_{tot, max}$[1] (A)
HMC5649 (THA)	2	0.221	0.442	16	3.536
	-5	-0.242	1.21		3.872
NB6L295 (Delay chip)	2.5	0.170	0.425	8	1.36
HMC987LP5E (Fanout buffer)	3.3	0.234[2]	0.772	2	0.468
LMK04808B (PLL)	3.3	0.590[3]	1.947	1	0.590
LMX2594 (PLL)	3.3	0.340	1.122	2	2.244
VCXO	3.3	0.03	0.198	1	0.03

[1]for 16 ADCs
[2]All Outputs and RF-Buffer
[3]All CLKs

In general, there are three different voltage levels provided by different components:

- 1.8 V for digital components coming from FMC+ connector
- 3.3 V for digital components coming from FMC+ connector
- 3.3 V and −5 V for analog devices from external power supplies

An EMI filter needs to be placed in order to keep noise of the power supply and read-out card from the sampling board (see Figure 3.22).

For the sensitive components like THA, voltage regulators are needed, to guarantee a stable voltage level.

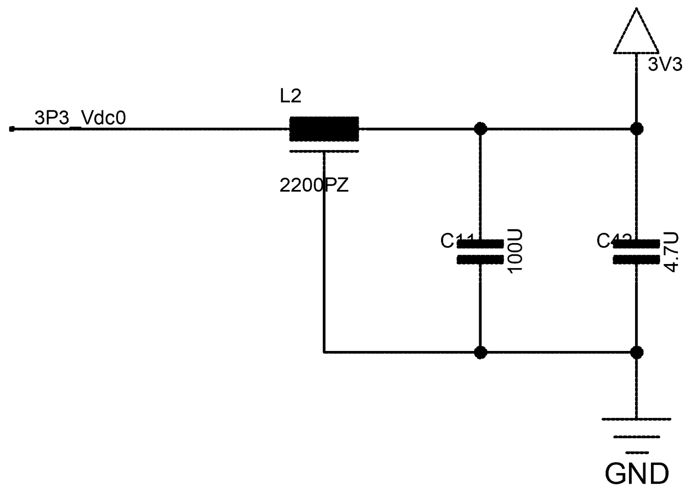


Figure 3.22.: EMI-filter used for power supply

Voltage Regulator for Track-and-Hold-Amplifiers

The THAs need a constant voltage level for optimal operation. Linear voltage regulators are capable to maintain a stable output voltage and are therefore to be used with the THAs.

On the KAPTURE sampling board, the Low Dropout Voltage Regulator (LDO) ADP1708 from *Analog Devices* is used to provide a power supply for the THAs. A LDO is able to operate at a low potential difference between the input and output voltage. This low potential difference has also the benefit of low power dissipation, which also reduces the This power supply can provide at maximum 1 A to the load. In order to minimize the amount of components needed on the board, i.e. to save space, a component which can provide higher currents should be used. This way, one single voltage regulator can be used for more components.

For the new board, the ADP1741 low-dropout voltage regulator from *Analog Devices* is used. This voltage regulator has adjustable output voltage from 1.6 V to 3.6 V and a maximum output current of 2 A.

It is now necessary to think about the amount of voltage regulators needed. As a rule of thumb, the power supply should provide twice the maximum power needed by the components it drives. [Mic] The power consumption/maximum current for the respective components on the sampling board is listed in Table 3.6.

It is necessary to think about the amount of voltage regulators needed. As a rule of thumb, the power supply should provide at least twice the maximum current (i.e. power) needed by the components it drives. [Mic] The power consumption/maximum current for the THAs on is listed in Table 3.6.

The maximal output current $I_{\text{max, LDO}}$ from the ADP1741 is 2 A. With the rule mentioned above and the maximal current draw $I_{\text{m, THA}} = 0.221\,\text{A}$ from the THA, the maximal number N of components which the LDO can handle is calculated as

$$
\begin{aligned}
I_{\text{max, LDO}} &> 2 \cdot N \cdot I_{\text{m, THA}} \\
I_{\text{max, LDO}}/(2 \cdot I_{\text{m, THA}}) &> N \\
2\,\text{A}/(2 \cdot 0.221\,\text{A}) &> N \\
4.52 &> N \quad \rightarrow N = 4
\end{aligned}
$$

This means, 4 LDOs are needed to cover 16 THAs.

The output voltage level of the regulator is set by an external divider with the resistors R_1 and R_2 (refer to Figure 3.23). According to the datasheet [Anaa] the voltage V_{OUT} is determined by

$$
V_{\text{OUT}} = 0.5\,\text{V}\left(1 + \frac{R_1}{R_2}\right) \tag{3.5}
$$

In order to achieve the required 2 V, the values of the resistors are chosen to $R_1 = 30\,\text{k}\Omega$ and $R_2 = 10\,\text{k}\Omega$.

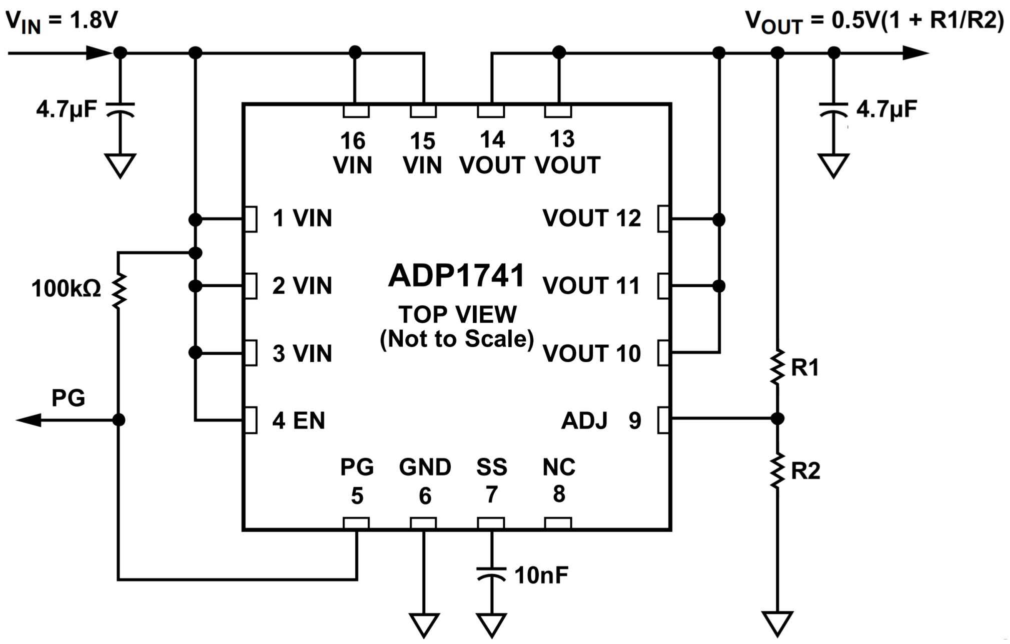


Figure 3.23.: Recommended schematic of the ADP1741 voltage regulator [Anaa]

As input voltage, the 3.3 V from the external power supply is provided.

Capacitors and resistors are placed as recommended in the datasheet[Anaa](see Figure 3.23).

Voltage Regulator for Delay Chips

The delay chips require a voltage level of 2.5 V. As they propagate the sensitive clock signals they also need stable voltage levels. The number N of delay chips with a maximal current draw $I_{\text{m, Delay}}$, which one LDO can handle, can be again calculated as:

$$
\begin{aligned}
I_{\text{max, LDO}} &> 2 \cdot N \cdot I_{\text{m, Delay}} \\
I_{\text{max, LDO}}/(2 \cdot I_{\text{m, Delay}}) &> N \\
2\,\text{A}/(2 \cdot 0.170\,\text{A}) &> N \\
5.88 &> N \quad \rightarrow N = 5
\end{aligned}
$$

Therefore, two regulators are needed to cover the 8 delay chips. In order to keep the current draw evenly distributed among the regulators, 4 chips are assigned to one regulator respectively.

In order to set the output voltage of the regulator to 2.5 V, the resistor values $R_1 = 12\,\mathrm{k\Omega}$ and $R_1 = 3\,\mathrm{k\Omega}$ are chosen (refer to Figure 3.23 and Equation 3.5).

The 2.5 V are also used as input for the bus transceiver which acts as a level translator. The current draw from this component lies in the range of µA and can thus be neglected.

As input voltage these regulators receive the 3.3 V from the FMC+ connector. The ground pins are connected to the digital ground of the PCB. This is important, as the

Power Dissipation of the Voltage Regulators

According to the data sheet of the ADP1741 [Anaa], the power dissipation P_D of the regulator can be calculated with the input and output voltage V_{IN} and V_{OUT}, load current I_{LOAD} and ground current I_{GND}[6]:

$$P_D = (V_{\mathrm{IN}} - V_{\mathrm{OUT}}) \cdot I_{\mathrm{LOAD}} + (V_{\mathrm{IN}} \cdot I_{\mathrm{GND}}) \tag{3.6}$$

I_{GND} is very small (range of µA), thus the power dissipation due to this current can be neglected. Therefore the equation above can be simplified to:

$$P_D = (V_{\mathrm{IN}} - V_{\mathrm{OUT}}) \cdot I_{\mathrm{LOAD}} \tag{3.7}$$

The power dissipation $P_{\mathrm{D,\ THA}}$ of one voltage regulator for the THAs is therefore

$$P_{\mathrm{D,\ THA}} = (3.3\,\mathrm{V} - 2\,\mathrm{V}) \cdot (4 \cdot 0.221\,\mathrm{A}) = 1.149\,\mathrm{W}. \tag{3.8}$$

The power dissipation $P_{\mathrm{D,\ Delay}}$ of one voltage regulator for the delay chips is

$$P_{\mathrm{D,\ Delay}} = (3.3\,\mathrm{V} - 2.5\,\mathrm{V}) \cdot (4 \cdot 0.17\,\mathrm{A}) = 0.544\,\mathrm{W}. \tag{3.9}$$

3.2. Layout

After completing the schematic capture, the following step is the PCB layout design. During this process, the following points need to be considered:

- An appropriate PCB substrate has to be chosen. The most important parameter of a substrate is its dielectric constant. For high-frequency circuits, a low dielectric constant is necessary.
- Generally, complex PCBs consist of a number of layers. In order to be able to route all the signals, it is necessary to think about the number of layers needed.
- Closely linked to the dielectric constant are the transmission lines. The geometry of these lines has to be calculated in order to meet the desired characteristic impedance (single-ended: 50 Ω, differential pair: 100 Ω). As this impedance also is defined by the dielectric constant, this step is closely linked to the selection of the substrate.
- Components need to be placed in a way that minimizes traces and routing. Sensitive components, like THAs have to be placed first

[6] difference between input and output current

- Route traces, taking care that traces of the same group (e.g. clock signals distributed to the THAs) have the same length. For sensitive signals take care that these are shielded by ground planes on the layers above and below.
- Places additional structures to reduce cross-talk, EMI, etc. (via fences, stitching vias, ...)
- Create proper power distribution by placing planes at appropriate places, i.e. reducing overlapping with traces carrying signals that could induce noise on the power plane.

For better understanding, first a general overview over PCB structures is given. Then the steps mentioned above are described.

PCB Structures Overview

In this section an overview over the basic structures on a PCB is given for better understanding.

Traces

A *trace* is a strip of metal, which establishes an electrical connection and carries signals between two (or more) points in the horizontal plane of a PCB. [Xil]

Planes

Plane denotes an uninterrupted area of metal, which covers the whole PCB layer. If this area only covers a part of the layer, it is called a *planelet*. These areas provide power distribution across the PCB and present an important transmission medium for the return current[7]. [Xil]

Vias

A via is metal-plated hole, which is used to route a trace in vertical direction, i.e. from the PCB outer layer to the inner layers. They carry signals and power. Three types of vias are [our]:

- Blind via: A blind via connects the surface layers with at most three layers below.
- Buried via: A buried via only connects internal layers.
- Through via: A through via goes from one PCB surface to another and is used to connect any layer.

In this design only blind and through vias are used due to manufacturing limitations.

[7] Any current, which is injected into the components/boards, needs a return path, as otherwise there is no closed circuit.

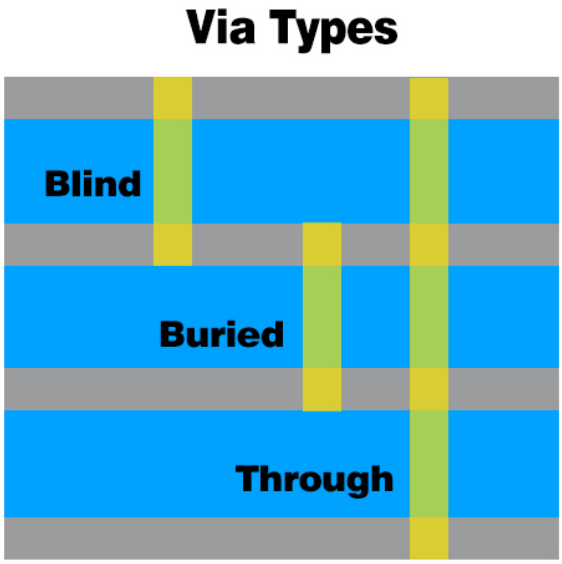


Figure 3.24.: Visualization of via types [our]

3.2.1. PCB Substrate Selection and Metal Layer Stackup

Proper substrate material has to be selected in according to the use-case. The MEGTRON 6 from *Panasonic* is designed for high-speed/high frequency applications. Characteristics of this material are:

- Low dielectric constant: $\varepsilon_r = 3.61$ at 10 GHz, 3.71 at 1 GHz
- Low dielectric dissipation factor: 0.002 at 10 GHz, 0.004 at 1 GHz
- Low transmission loss
- High heat resistance: Decomposition temperature $T_d = 410\,°\mathrm{C}$

Another important step is deciding the number of layers. The complexity of the board implies that a lot of layers are needed. For this design a number of 16 layers is chosen.

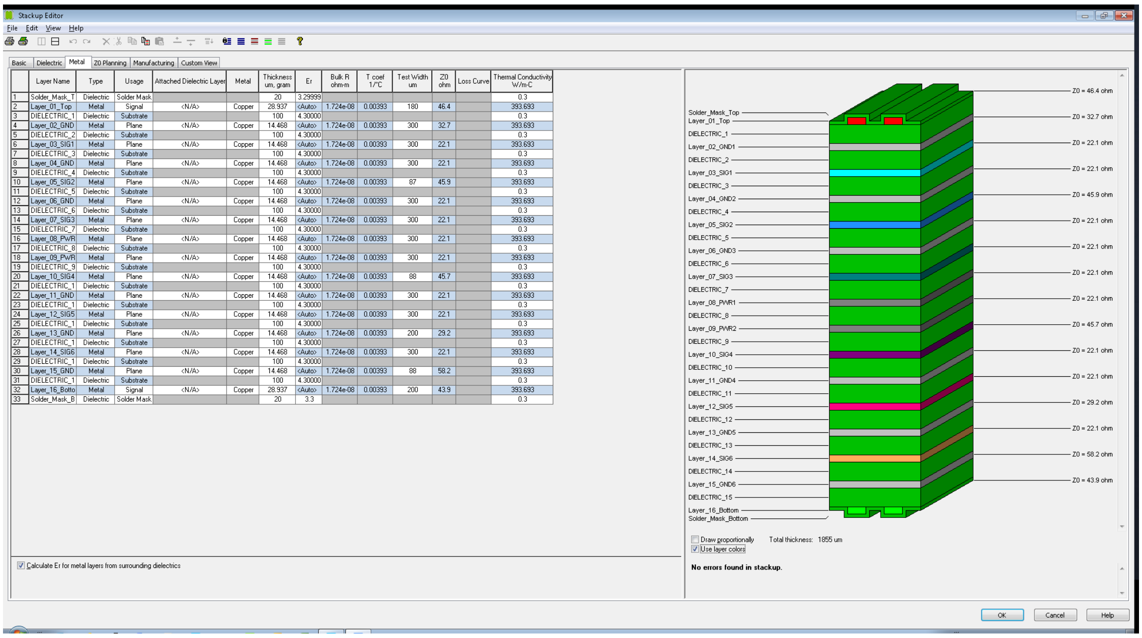


Figure 3.25.: Metal Layer stackup showing 16 layers.

3.2.2. Transmission Lines

Transmission lines guide electromagnetic waves from one point to another. They have a characteristic impedance which is determined by parameters like width of the trace, separation from ground plane, etc. Not matching correctly can lead to reflections and damping. For single-ended signals the waveguide characteristic impedance should be 50 Ω, for differential pairs 100 Ω. The impedance has to be matched especially for sensitive, high-speed signals, e.g. clock signals. Proper calculation of the geometrical parameters is therefore very important to ensure signal integrity and reduce reflection and damping.

Formulas to calculate the characteristic impedance are quite lengthy and not easy to solve. To make the design of transmission lines easier, tools exist to quickly calculate the geometric values needed for appropriate impedance. For this design, the Si9000e tool for modeling PCB transmission lines from *Polar* (see Figure 3.26) is used to calculate the necessary trace widths, trace separations, etc.

As there are a lot of parameters which can be tuned, as a starting point the geometrical parameters from the KAPTURE system are applied. These were carefully designed for optimal signal transmission. However, the substrate used in the KAPTURE system, has a different dielectric constant than the Megtron6 substrate used for the new design. Therefore, the impedance has to be recalculated to check whether it is still acceptable. A deviation of 10% from the ideal 50 Ω and 100 Ω is still regarded as acceptable, as tolerances during manufacturing need to be considered. The change in impedance/parameters is assumed to be negligible, as the difference in dielectric constans between the two boards is not large (KAPTURE: $\varepsilon_r = 3.52$, new board: $\varepsilon_r = 3.61$)

Three types of waveguides are used in this design:

- Surface coplanar waveguide with ground for analog input to the THAs
- Differential surface coplanar waveguide with ground for output from the delay chips to the THAs
- Offset differential coplanar waveguide for clock signals and signals coming from the THAs

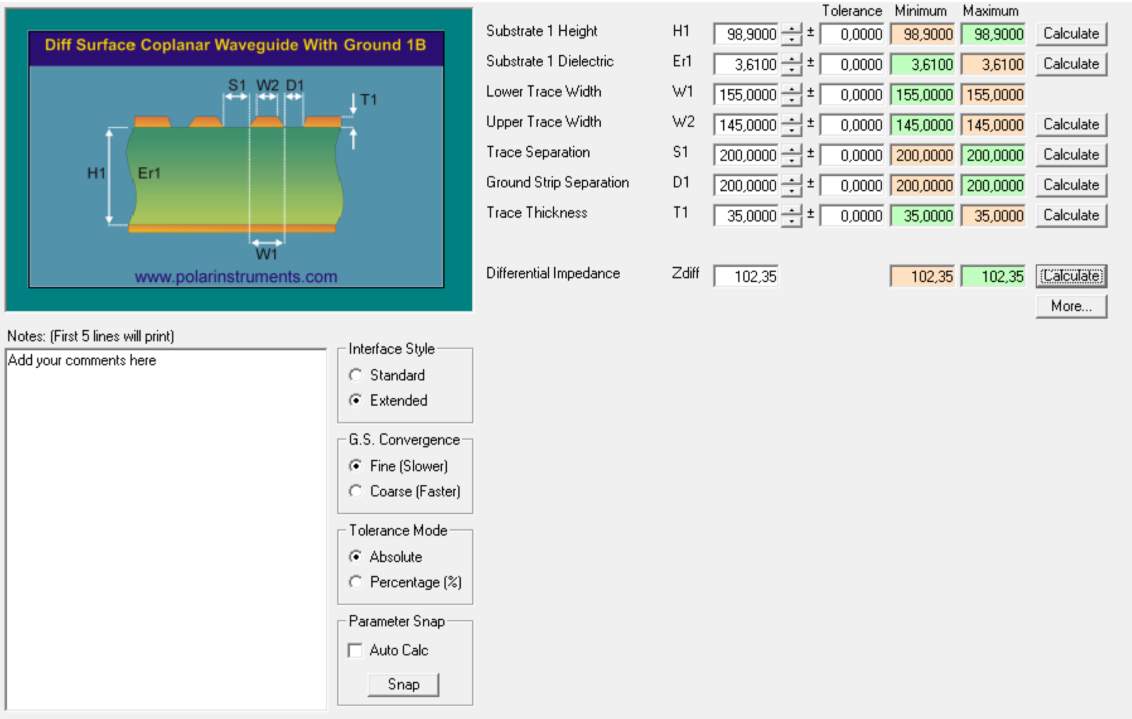


Figure 3.26.: Screenshot of the Polaris Si9000e tool for modeling PCB transmission lines, showing calculation of characteristic impedance of a coplanar waveguide

These waveguide types are presented and the geometric dimensions calculated with the Si9000e tool are presented.

Surface Coplanar Waveguide with Ground

The surface coplanar waveguide has the geometry shown in Figure 3.27. The single trace of thickness t and width a lies between two ground planes on a dielectric of thickness h and the effective dielectric constant ε_r. Another ground plane is located at the bottom of the dielectric. Separation between trace and ground plane is defined as $(b - a)/2 := d$.

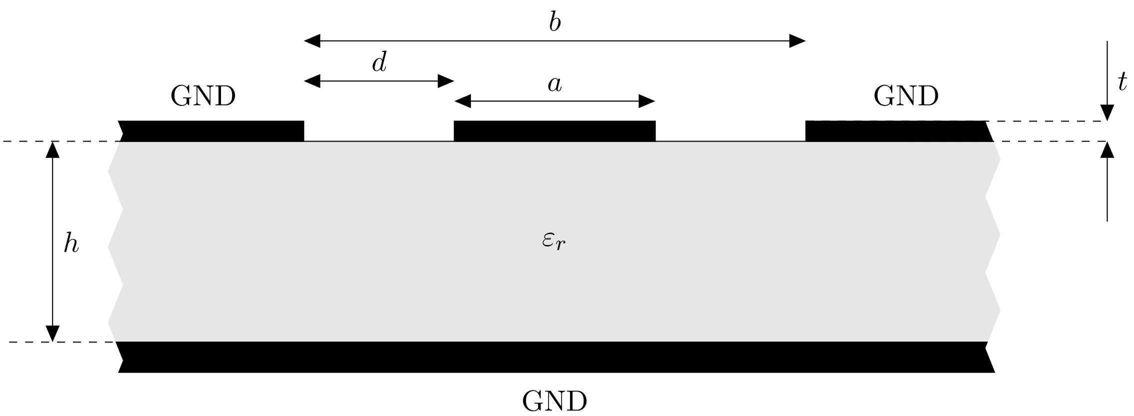


Figure 3.27.: Coplanar Waveguide with Ground

To have a rough starting point of the dimensions of the parameters, the following widths are taken from the KAPTURE board:

- $a = 213\,\mu m$
- $d = 250\,\mu m$

In the Si9000e tool, an upper and a lower trace width can be specified, therefore taking into account the etching process during manufacturing. As the exact upper trace width is not known, both widths are assumed to be of the same value if not stated otherwise. The thickness t of the trace and the thickness h of the dielectric is defined by the used substrate. For Megtron6 it is

- $t = 30\,\mu m$
- $h = 100\,\mu m$

With all these parameters, the value for the characteristic impedance is calculated to $Z_o = 47.33\,\Omega$. This lies well in the 10% tolerance range of $45\,\Omega$ to $55\,\Omega$.

According to the datasheet of the Megtron6, the dielectric constant ε_r changes over frequency (see subsection 3.2.1). As the dielectric constant ε_r of the Megtron6 substrate varies between 3.61 and 3.71 depending on the frequency, the effect of the changing ε_r should also be studied. The Si9000e tool provides the possibility to simulate the characteristic impedance versus a changing parameter. In Figure 3.28 the characteristic impedance Z_o is plotted against ε_r. It can be seen that with higher effective dielectric constant the characteristic impedance decreases. The lowest values lies around $47\,\Omega$, a change of 0.7 %, which is still inside the 10% tolerance range.

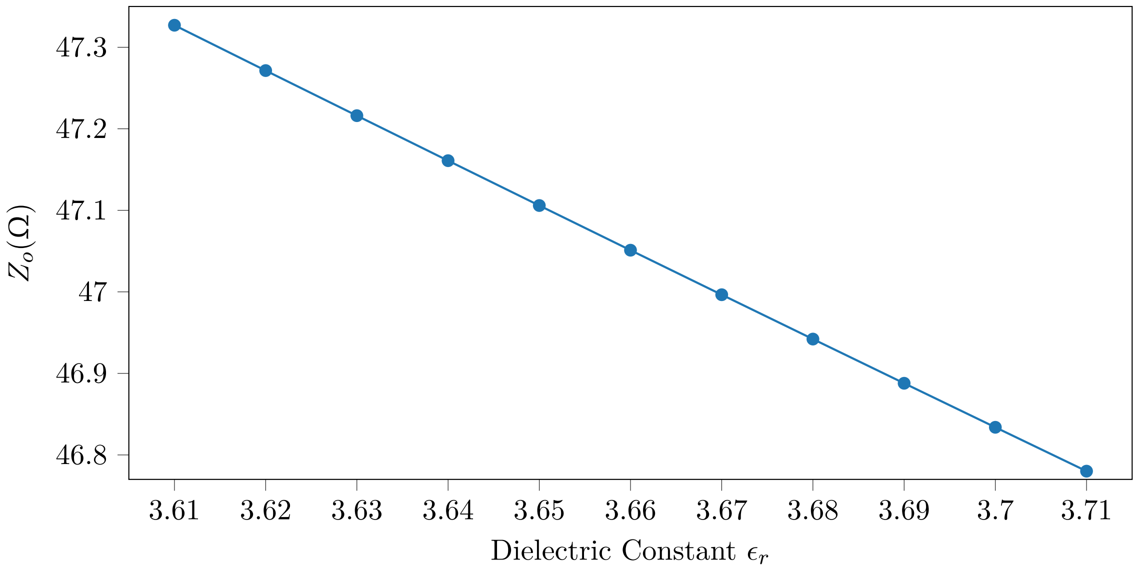


Figure 3.28.: Characteristic impedance Z_o of a coplanar waveguide versus dielectric constant ε_r assuming $a = 213\,\mu m$

Furthermore, the effect of changing the trace width on Z_o is studied and shown in Figure 3.29. This plot shows that for best matching of the impedance a trace thickness of around $200\,\mu m$ is the best choice. This result however does not take into account the real upper tracewidth.

For an estimation of the effect of the upper trace width on the impedance, a constant lower trace width of $213\,\mu m$ and $\varepsilon_r = 3.61$ is assumed, while varying the upper trace width from $183\,\mu m$ to $213\,\mu m$. The result is shown in Figure 3.30. With decreasing width the characteristic impedance approaches $50\,\Omega$, meaning the matching can potentially become better due to manufacturing.

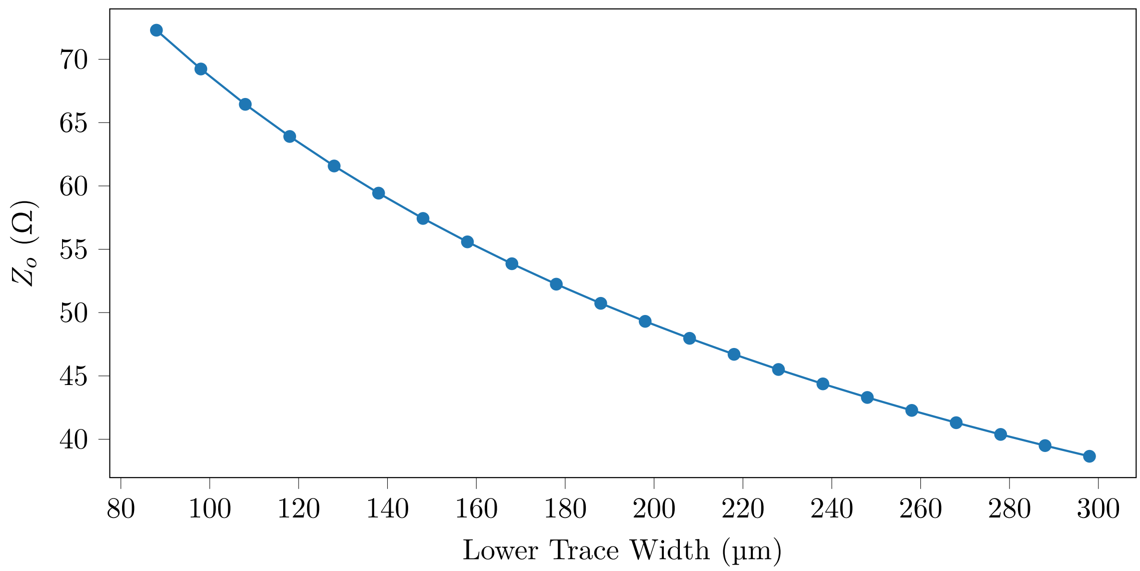


Figure 3.29.: Z_o vs. lower trace thickness a, assuming $\varepsilon_r = 3.61$

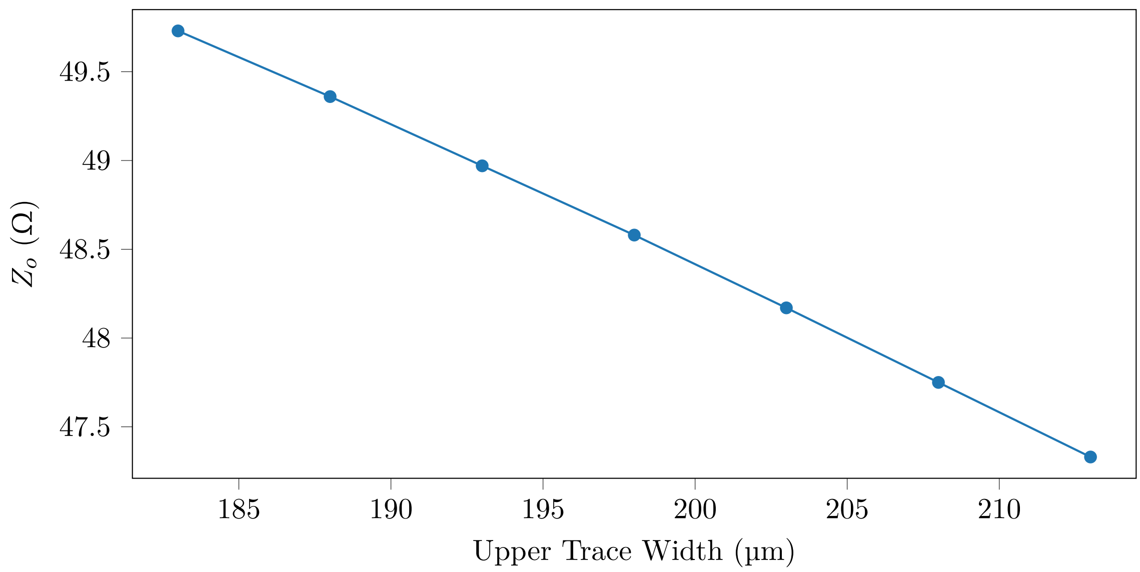


Figure 3.30.: Z_o vs. lower trace thickness

Differential Pairs on Surface

The geometry of the differential surface is similar to the waveguide type before, with the difference of having a pair of traces instead of one single trace (see page 62). The characteristic differential impedance Z_{diff} of this transmission line type is determined by the trace width w, the trace separation s, the trace-to-ground-separation d, the thickness of the trace t and thickness of the dielectric h.

The parameters t and h have the same value, as for the coplanar waveguide described below. For the other parameters first the following values are assumed:

- Trace width $w = 180\,\mu\text{m}$
- Trace separation $s = 150\,\mu\text{m}$
- Trace-to-ground separation $d = 600\,\mu\text{m}$

For these parameters and an $\varepsilon_r = 3.61$ an impedance of $92.35\,\Omega$ is calculated with the Si9000e tool. This is still inside the tolerance band, but can potentially be improved.

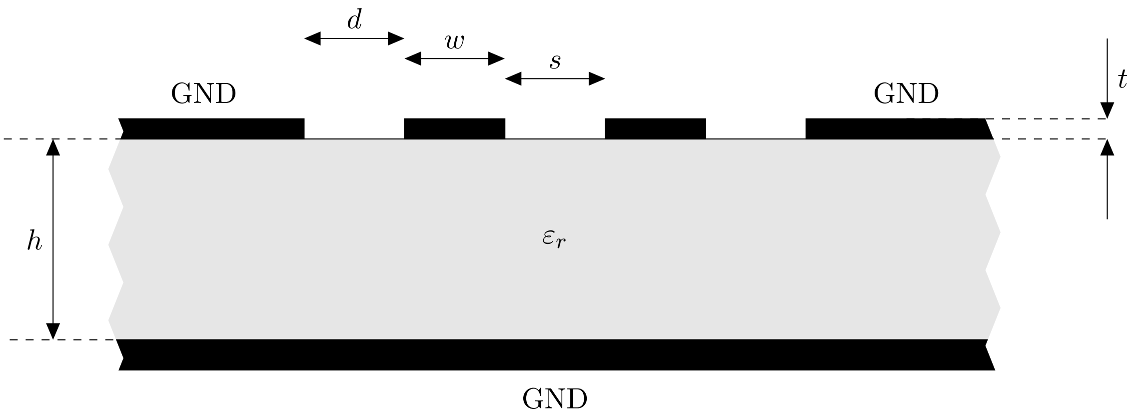


Figure 3.31.: Edge-Coupled Coplanar Waveguide

In Figure 3.32 a the characteristic impedance Z_{diff} is plotted against the trace width[8]. The impedance Z_{diff} lies around $100\,\Omega$ for a trace width $w \approx 155\,\mu\text{m}$.

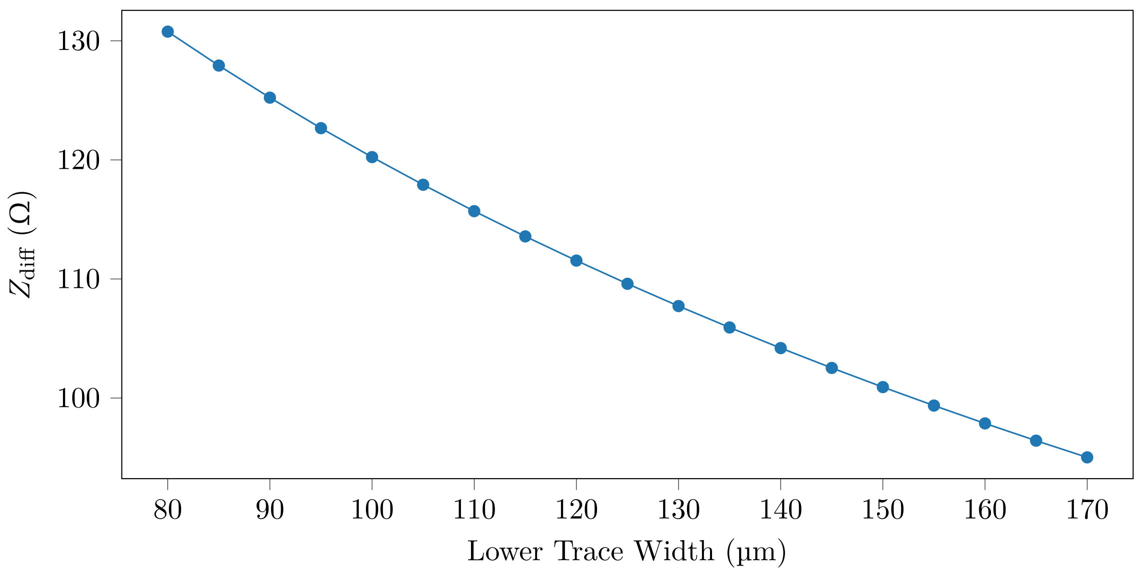


Figure 3.32.: Z_{diff} vs. lower trace width w, assuming $\varepsilon_r = 3.61$

Setting the width to $155\,\mu\text{m}$ indeed gives an impedance of $Z_{\text{diff}} = 99.37\,\Omega$. The influence of the changing dielectric constant ε_r is studied in this case as well (see Figure 3.33). At the maximal value of $\varepsilon_r = 3.71$, the impedance lies around $98.4\,\Omega$ corresponding to a change of $0.88\,\%$ compared to the value at $\varepsilon_r = 3.61$.

Furthermore, assuming $\varepsilon_r = 3.61$ and a lower trace width $w = 155\,\mu\text{m}$, the impedance over a varying upper trace width is plotted in page 63.

Differential Pairs between Layers

The analog signals from the THAs, as well as the clock signals, are propagated through differential pair traces on the inner layers of the PCB. This forms an offset coplanar waveguide as seen in Figure 3.35. The impedance of this waveguide type depends on the trace width w, the trace separation s, the trace-to-ground separation d, the thickness t of

[8] Assuming lower and upper trace width are equal.

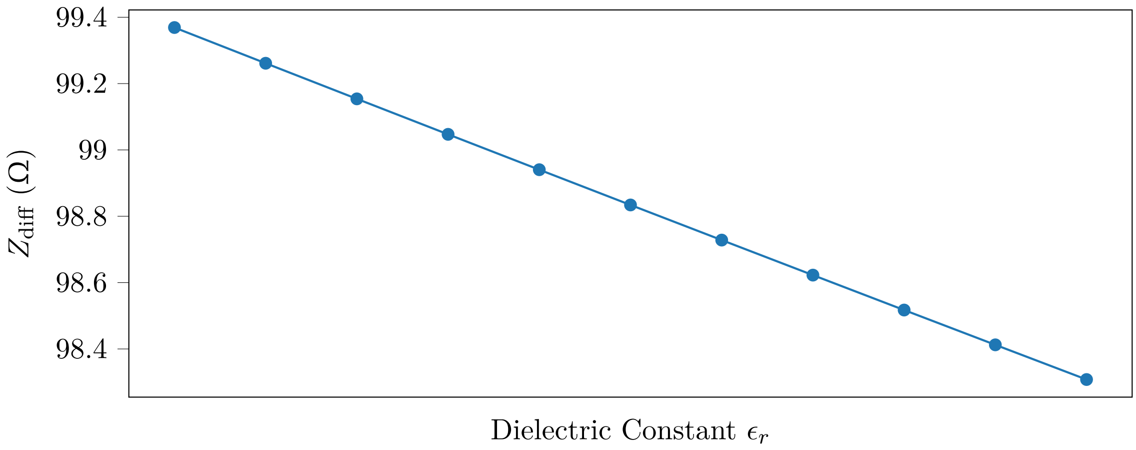


Figure 3.33.: Z_{diff} vs. dielectric constant ε_r

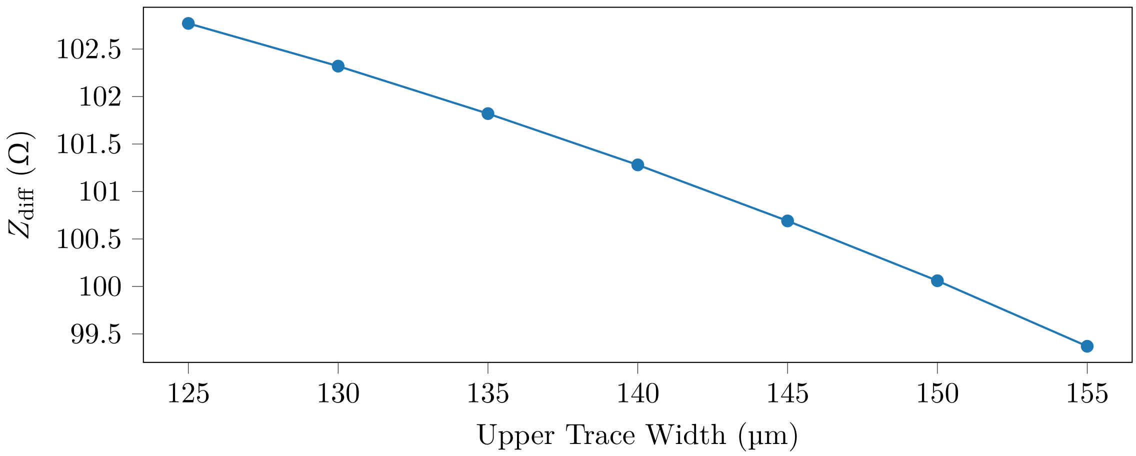


Figure 3.34.: Z_{diff} vs. upper trace width, assuming lower trace width $w = 155\,\mu\text{m}$ and$\varepsilon_r = 3.61$

the trace, as well as the thickness of the dielectrics h_1 and h_2 and their respective dielectric constant ε_1 and ε_2.

The parameters are assumed as

- Trace width $w = 88\,\mu\text{m}$
- Trace separation $s = 150\,\mu\text{m}$
- Trace-to-ground separation $d = 250\,\mu\text{m}$

Thickness of the dielectrics is $h_1 = h_2 = 150\,\mu\text{m}$ and the dielectric constant is equal for both ($\varepsilon_1 = \varepsilon_2 = \varepsilon_r = 3.61$.) With these parameters the impedance is calculated as $Z_{\text{diff}} = 90.40\,\Omega$. In Figure 3.36 Z_{diff} is plotted against the trace width w (assuming upper trace width equal to w). It can be seen, that in order to improve the impedance, one should decrease the trace width. Due to the manufacturing technology the minimal trace width possible is 88 µm. Therefore this option is not feasible.

Keeping the trace width constant at $w = 88\,\mu\text{m}$ the trace separation could also be changed. Figure 3.37 shows Z_{diff} plotted against the trace separation s. It can be seen that Z_{diff} does not change significantly over a large range of s. For a trace separation of around 300 µm (more than 3 times larger than the trace width itself) $Z_{\text{diff}} \approx 94\,\Omega$ and not significantly improved. Taking this into consideration, as well as the space on the board, the parameters are left as is.

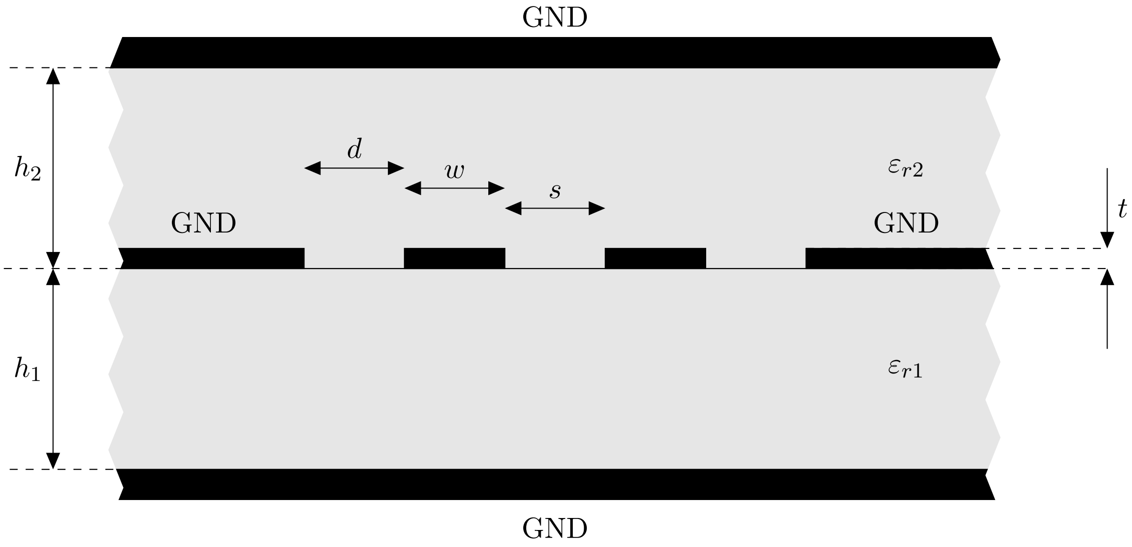


Figure 3.35.: Offset Differential Coplanar waveguide

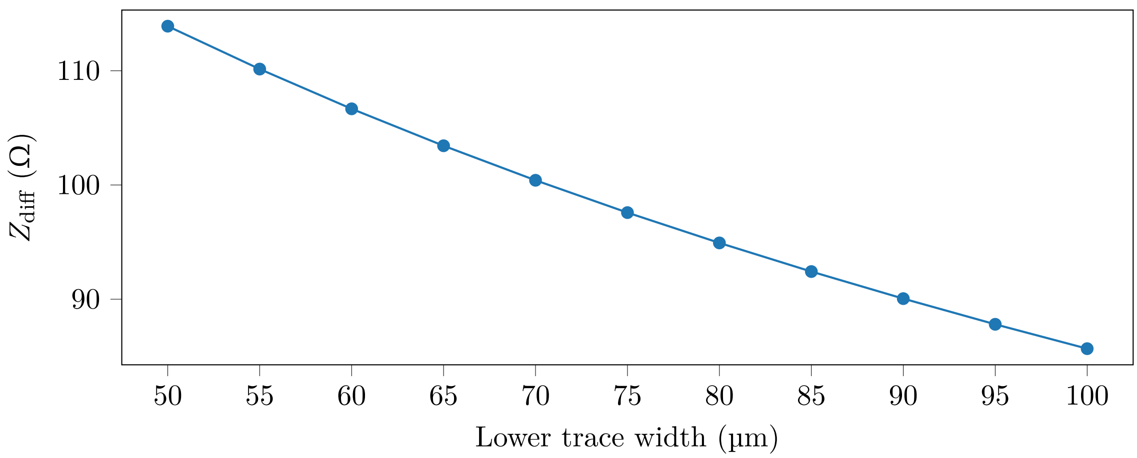


Figure 3.36.: Z_{diff} vs. lower trace width w, assuming upper trace width equals to w

The influence of the dielectric constant ε_r is shown in Figure 3.38. Z_{diff} decreases with higher value of ε_r and even get below $90\,\Omega$, exceeding the $10\,\%$ tolerance. However, the upper trace width has also to be taken into account, which is in any case smaller than the lower trace width due to the etching process during manufacturing. As Figure 3.39 shows, the impedance is potentially higher than calculated by assuming both width equal. Therefor the impedance can still be regarded as falling into the tolerance band.

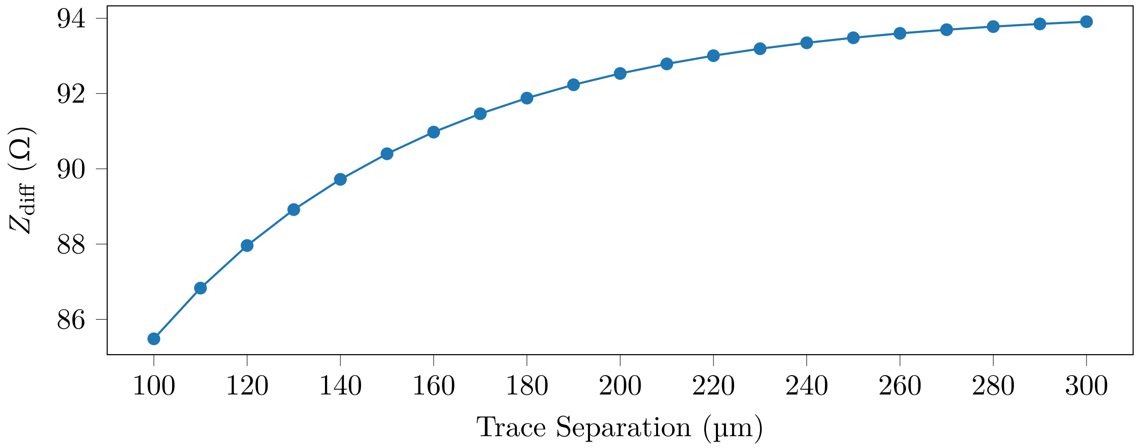


Figure 3.37.: Z_{diff} vs. trace separation s, assuming trace width $w = 88\,\mu\text{m}$

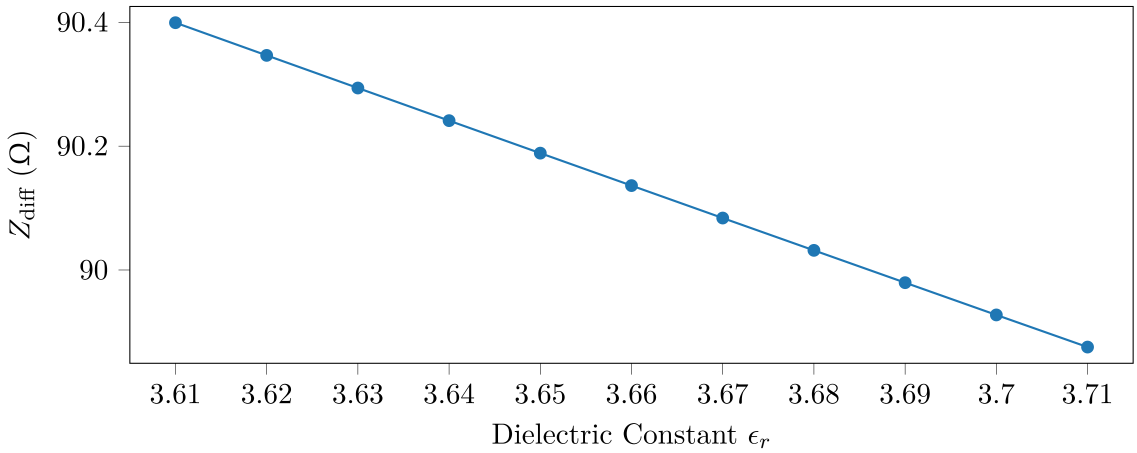


Figure 3.38.: Z_{diff} vs. dielectric constant ε_r, assuming lower trace width $w = 88\,\mu\text{m}$ and $\varepsilon_r = 3.61$

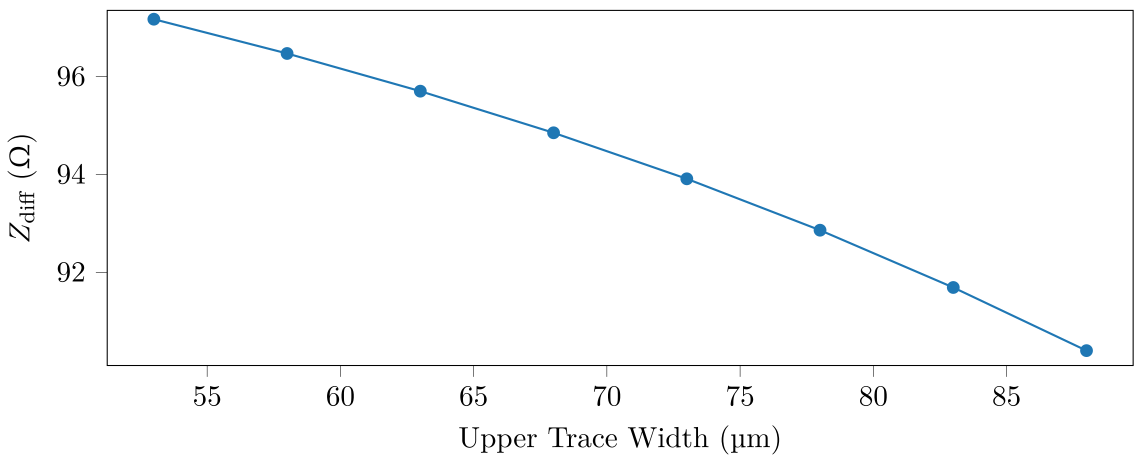


Figure 3.39.: Z_{diff} vs. upper trace width, assuming lower trace width $w = 88\,\mu\text{m}$ and $\varepsilon_r = 3.61$

3.2.3. Component Placement and Routing

During component placement and routing, several rules need to be followed in order to guarantee proper signal propagation and signal integrity.

Component placement

- The board geometry, or board outline, need to match the readout card, i.e. the connectors need to be placed exactly to match their counterpart on the board
- Analog and digital components need to be separated. In order to accomplish this, the board is divided into two parts: the top eight layers are assigned to carry digital signals and ground. The other half of the layers is dedicated to analog components.
- Layers carrying signals are "sandwiched" between two ground layers. This is important for differential pairs, as they should GND right below/above, because this serves as a return path. Furthermore, the ground layers serve as shielding from noise.
- Power planes are placed in such a way, that no or only few signal traces are routed above/below, as any switching events may introduce noise on the power plane.
- Components, especially sensitive ones, have to be placed in dedicated "islands" .
- High-frequency components need to be placed first. This is done on order to minimize the routing length of the RF traces.
- Stitching vias are used to shield the sensitive ICs as much as possible from EMI (see Figure 3.40 for an example).
- Decoupling capacitors are placed in such way, that the large capacitor is connected to the power plane of the external power supply or voltage regulator. The filtered voltage level after the capacitor is propagated to a power plane located on an inner layer. The smaller bypass capacitor is connected to this layer by a via and then to the power supply pin of the respective chip. The small capacitor connects the component to the clean power plane and bypasses high frequency variations. The bypass capacitor is closed as close as possible to the power supply pin.
- THAs have been placed on the edge.
- Delay chips have been arranged evenly so no further delay is introduced due to misplaced components.
- Fanout buffers have been placed in the middle of two groups à 8 THAs for even distribution of the signal.
- LMK04808B is placed right in the middle to evenly distribute clocking to the fanout buffers and the other to PLLs.
- Voltage regulators are placed symmetrically, this makes it easier to provide power planes in an efficient way.

Routing

During routing, take care of the high frequency, sensitive signals first. This guarantees on the one hand the shortest possible connection for these signals. On the other hand this defines the routing for the slower, less critical signals. In order to minimize cross-talk, these signals need to be routed around the high-frequency lines and must not cross these (in the layer directly above or below).

Some pins form a "group", e.g. clock signals from the fanout to the delay chips. Trace length of the same group need to be matched as close as possible to reduce any skew between signals.

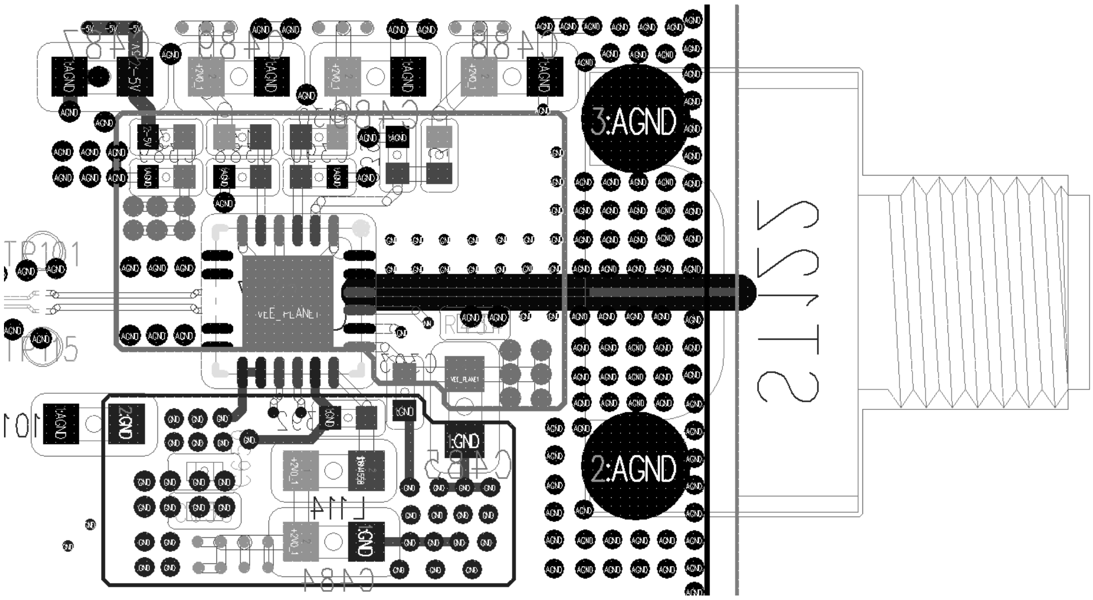


Figure 3.40.: Example for stitching vias at the THA. An area is filled up with (blind) vias connected to analog or digital ground. This way, they protect the trace or component from external (and internal) noise.

- Keep routes confined to the section they are assigned to, i.e. digital traces have to be in digital.
- Connectors need to be placed exactly to match the connectors on the board. The connectors therefore define the geometry of the board in a large way.

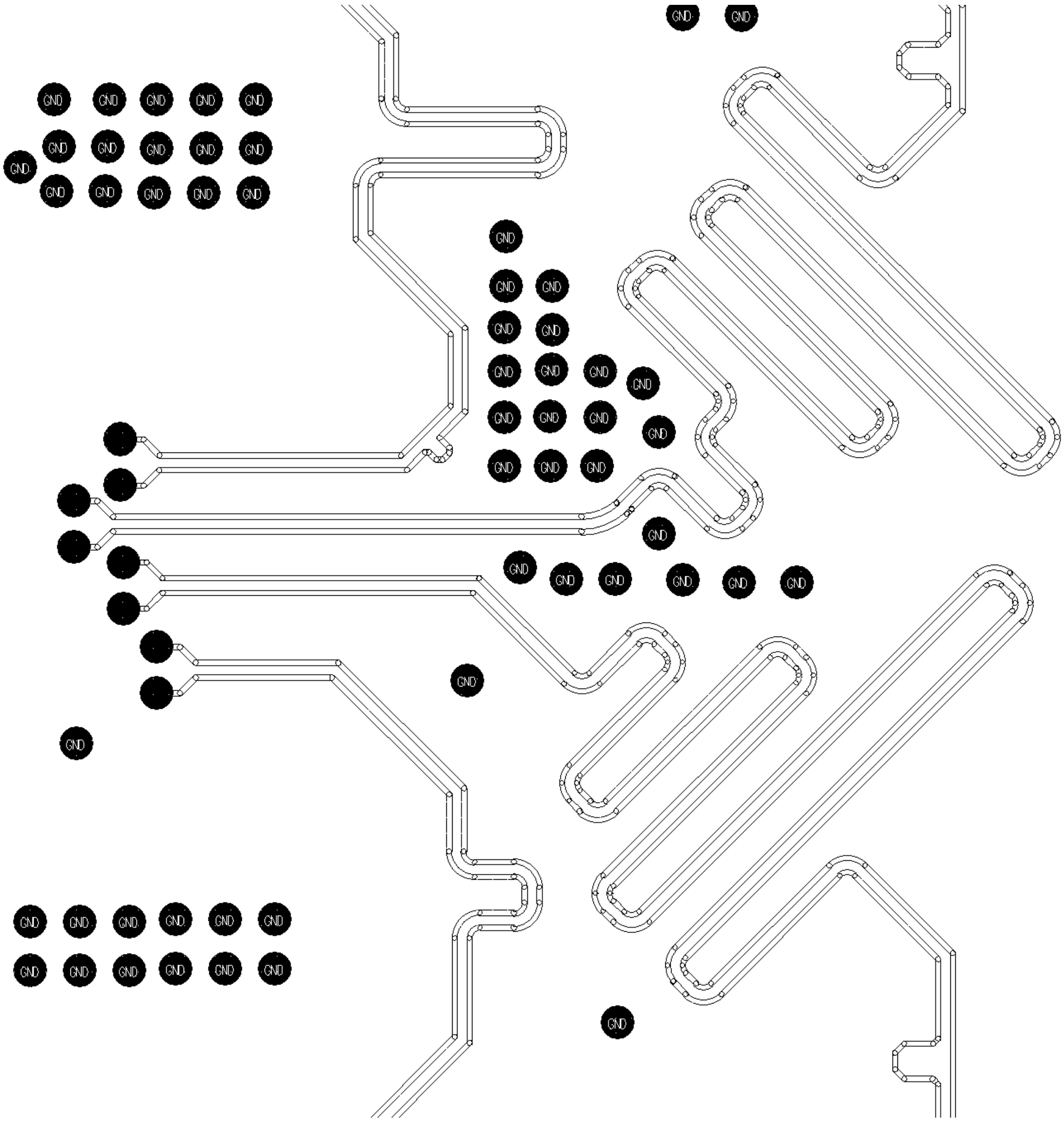


Figure 3.41.: Example for trace accordions which are used to enlarge the trace length when little space is available

4. Back-End Readout Card and System Integration

The back-end readout card for the system under development, the Zynq UltraScale+ RFSoC ZCU216 Evaluation Card, was chosen taking into consideration the points described in section 2.2. In this section, the overall architecture and features of the card are presented. A possibility for evaluation of the card is also demonstrated. At last, a design for the read-out firmware is proposed.

4.1. Xilinx Zynq UltraScale+ RFSoC ZCU216 Evaluation Card

Zynq UltraScale+ RFSoCs: Combine RF data converter subsystem and forward error correction with industry-leading programmable logic and heterogeneous processing capability. Integrated RF-ADCs, RF-DACs, and soft decision FECs (SD-FEC) provide the key subsystems for multiband, multi-mode cellular radios and cable infrastructure

With the data converters integrated directly into the FPGA using parallel interfaces, they do not require the prohibitively high-pin-count external connections needed for discrete parallel interface converters, allowing more converter

- Sixteen 14-bit, 2.5GSPS RF-ADC
- Sixteen 14-bit, 10GSPS RF-DAC
- I/O expansion options – FPGA Mezzanine Card (FMC+) interfaces, RFMC 2.0 interfaces, and Pmod connections

Evaluation Tool

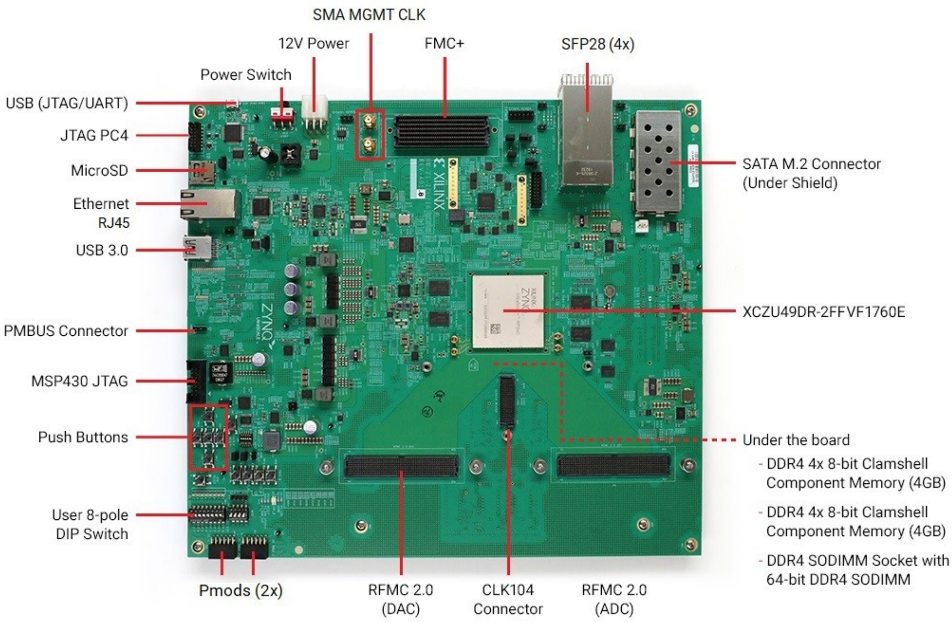


Figure 4.1.: ZCU216 evaluation board

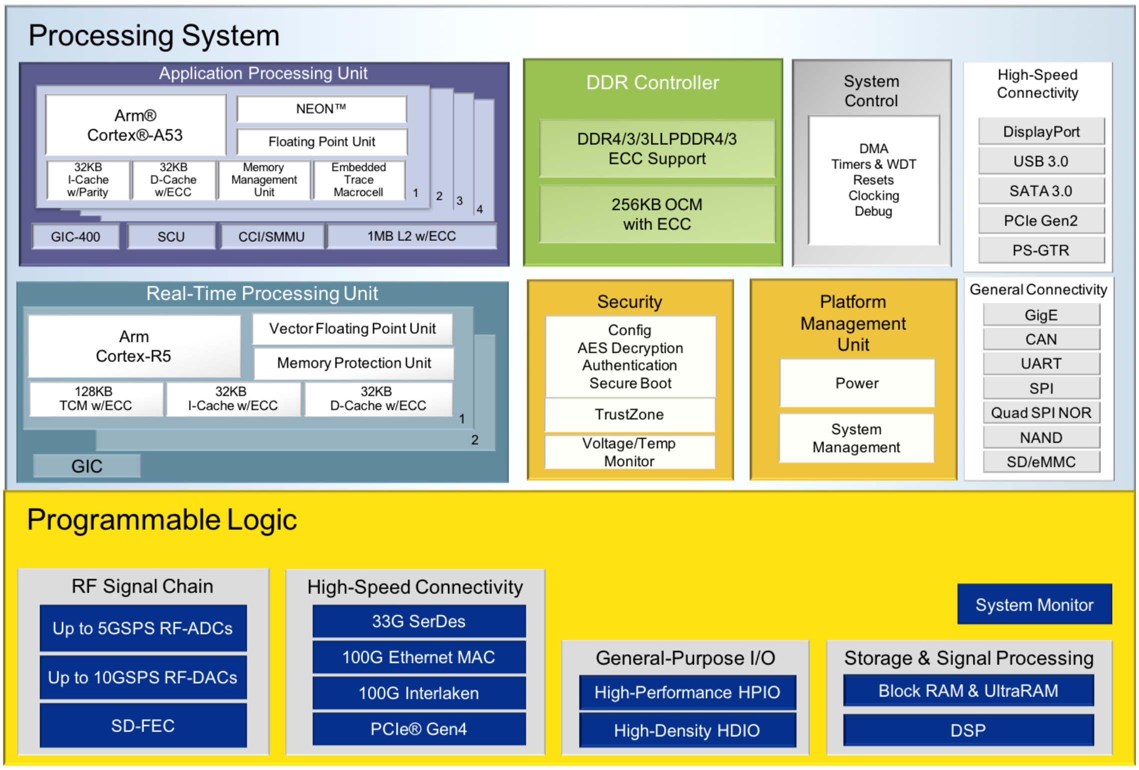


Figure 4.2.: RFSoC block diagram

4.2. Firmware

4.2.1. RF Data Converter

4.2.2. SoC

4.2.3. RDMA over Converged Ethernet (RoCE)

4.2.4. System Integration

5. Conclusion and Outlook

In this thesis, a first demonstrator of a new DAQ system based on the photonic time-stretch method was developed. The system consists of a high bandwidth front-end sampling card, mounted on a new generation of Radio-Frequency System-On-Chip (RFSoC) for readout of the acquired samples. The sampling card was designed to fully exploit all the features of the RFSoC.

- Integrated high-speed ADCs with 14-bit resolution and a sample rate up to 2.5 GS/s. With the sixteen available converters and using a time-interleaving method, the system is capable of a sample rate of 40 GS/s, allowing a continuous sampling with high temporal resolution.
- On-chip FPGA provides high-speed control and the flexibility adjust the firmware to user needs.
- On-chip memory to intermediately store acquired data.
- The System-On-Chip (SoC) high-speed connections (e.g. 100G-Ethernet) in order to guarantee the high-speed throughput of the data (range of TeraBits!)
- Use of the provided framework in order to quickly characterize system performance

The system can be used to assist research in important scientific topics, e.g. improving quality of beam diagnostics or the research of laser dynamic. Potential industrialization of the DAQ is also foreseen.

Acknowledgments

Appendix

A. Characteristic Impedance Of Coplanar Waveguides

Edge-Coupled Coplanar Waveguide

Characteristic impedance[Wad91, p197-198]:

$$Z_{0,o} = \frac{\eta_0}{\sqrt{\epsilon_{\text{eff},o}}} \left(\frac{1.0}{2.0\frac{K(k_o)}{K'(k_o)} + \frac{K(\beta_1)}{K'(\beta_1)}} \right) \tag{A.1}$$

$$Z_{0,e} = \frac{\eta_0}{\sqrt{\epsilon_{\text{eff},e}}} \left(\frac{1.0}{2.0\frac{K(k_e)}{K'(k_e)} + \frac{K(\beta_1 k_1)}{K'(\beta_1 k_1)}} \right) \tag{A.2}$$

$$\epsilon_{\text{eff},o} = \frac{2.0\epsilon_r \frac{K(k_o)}{K'(k_o)} + \frac{K(\beta_1)}{K'(\beta_1)}}{2.0\frac{K(k_o)}{K'(k_o)} + \frac{K(\beta_1)}{K'(\beta_1)}} \tag{A.3}$$

$$\epsilon_{\text{eff},e} = \frac{2.0\epsilon_r \frac{K(k_e)}{K'(k_e)} + \frac{K(\beta_1 k_1)}{K'(\beta_1 k_1)}}{2.0\frac{K(k_e)}{K'(k_e)} + \frac{K(\beta_1 k_1)}{K'(\beta_1 k_1)}} \tag{A.4}$$

with

$$k_o = \Lambda \frac{-\sqrt{\Lambda^2 - t_c^2} + \sqrt{\Lambda^2 - t_B^2}}{t_B\sqrt{\Lambda^2 - t_c^2} + t_c\sqrt{\Lambda^2 - t_B^2}} \tag{A.5}$$

$$k_e = \Lambda' \frac{-\sqrt{\Lambda'^2 - t_c'^2} + \sqrt{\Lambda'^2 - t_B'^2}}{t_B'\sqrt{\Lambda'^2 - t_c'^2} + t_c'\sqrt{\Lambda'^2 - t_B'^2}} \tag{A.6}$$

$$\Lambda = \frac{\sinh^2\left(\frac{\pi(s/2.0+w+d)}{2.0h}\right)}{2} \tag{A.7}$$

$$t_c = \sinh^2\left(\frac{\pi(s/2.0+w)}{2.0h}\right) - \Lambda \tag{A.8}$$

$$t_B = \sinh^2\left(\frac{\pi s}{4.0h}\right) - \Lambda \tag{A.9}$$

$$\Lambda' = \frac{\cosh^2\left(\frac{\pi(s/2.0+w+d)}{2.0h}\right)}{2} \tag{A.10}$$

$$t'_c = \sinh^2\left(\frac{\pi(s/2.0+w)}{2.0h}\right) - \Lambda' + 1.0 \tag{A.11}$$

$$t'_B = \sinh^2\left(\frac{\pi s}{4.0h}\right) - \Lambda + 1.0 \tag{A.12}$$

The parameters have to be chosen according to

$$s + 2.0w + 2.0d \leq h \tag{A.13}$$

to guarantee coplanar propagation. [Wad91]

Surface Coplanar Waveguide with Ground

The characteristic impedance of a coplanar waveguide is given as (see [Wad91])

$$Z_0 = \frac{60.0\pi}{\sqrt{\epsilon_{\text{eff}}}} \frac{1.0}{\frac{K(k)}{K(k')} + \frac{K(k_1)}{K(k_1')}}. \tag{A.14}$$

It comprises of the following components, with $K(k)$ being an elliptical integral of the first kind (see also [BSMM99, p. 430]):

$$k = a/b \tag{A.15}$$

$$k' = \sqrt{1.0 - k^2} \tag{A.16}$$

$$k_1 = \frac{\tanh(\frac{\pi a}{4.0h})}{\tanh(\frac{\pi b}{4.0h})} \tag{A.17}$$

$$k_1' = \sqrt{1.0 - k_1^2} \tag{A.18}$$

$$\epsilon_{\text{eff}} = \frac{1.0 + \epsilon_r \frac{K(k')}{K(k)} \frac{K(k_1)}{K(k_1')}}{1.0 + \frac{K(k')}{K(k)} \frac{K(k_1)}{K(k_1')}} \tag{A.19}$$

B. QuickStart Guide for Evaluation of ZCU216 Board

C. 3D model of front-end card

D. Code

```
`timescale 1ns / 1ps

module SDI_Delay_NB6L295(

    input [10:0]        In_1, In_2, In_3, In_4, In_5, In_6, In_7, In_8,  //
        data for respective delay chips
    input               Clk,
    input               Reset,
    output reg          [7:0] EN, // enable signal for delay chips, active LOW
    output reg          SDIN, // configuration data
    output reg          SLOAD, // signals delay chip to load previously sent
        data
    output              SCLK // clock for serial communication with delay chips
    );

    reg                 start_clk;
    assign SCLK = start_clk & (!Clk);
```

```
reg [21:0]          In_1_reg, In_2_reg, In_3_reg, In_4_reg, In_5_reg,
    In_6_reg, In_7_reg, In_8_reg; // registers to intermediately store the
    inputs

reg [7:0]           select; // register used by Priority Encoder to detect
    which input changed

parameter           DATA_SHIFT_WIDTH = 11; // number of bits to be shifted
    during transmission, 1 Data word = 11 bits
reg [4:0]           clk_cnt;


reg [DATA_SHIFT_WIDTH-1:0]  Data_reg;  // register for storing data for
    state machine

reg                 start; // signal for state machine to start sending
    data
reg                 dataSent; // flags if transmission for one delay chip
    is finished

parameter           dly = 1; // delay control

reg                 delayReady;


always @ (posedge Clk)
begin
    if (select == 'd0)      delayReady <= #dly 'b1;
    else                    delayReady <= #dly 'b0;
end

// Priority Encoder
// Check if any input has changed, select which data should be sent
    accordingly
always @ (posedge Clk)
    begin
        if (Reset)
            begin
                In_1_reg        <= #dly 'd0;
                In_2_reg        <= #dly 'd0;
                In_3_reg        <= #dly 'd0;
                In_4_reg        <= #dly 'd0;
                In_5_reg        <= #dly 'd0;
                In_6_reg        <= #dly 'd0;
                In_7_reg        <= #dly 'd0;
                In_8_reg        <= #dly 'd0;
                Data_reg        <= #dly 'd0;

                select          <= #dly 'd0;

                start           <= #dly 1'b0;;
            end
        else
            begin
                if (~start & delayReady)
                    begin
                        select[7]   <= #dly In_1_reg != In_1;
                        select[6]   <= #dly In_2_reg != In_2;
                        select[5]   <= #dly In_3_reg != In_3;
                        select[4]   <= #dly In_4_reg != In_4;
                        select[3]   <= #dly In_5_reg != In_5;
                        select[2]   <= #dly In_6_reg != In_6;
                        select[1]   <= #dly In_7_reg != In_7;
                        select[0]   <= #dly In_8_reg != In_8;
```

```
        end
    else
      begin
          if (clk_cnt == 4'd12 & ~start_clk) // = end of
              sequence
                start                   <= #dly 1'b0;
              else
                start                   <= #dly 1'b1;
        end

      casex (select)
          8'b1???????:
              begin
                if (~dataSent)
                  begin
                        In_1_reg            <= #dly In_1;
                        Data_reg            <= #dly In_1;
                        EN                  <= #dly
                            8'b01111111;
                        start               <= #dly 1'b1;
                        end
                  else
                    begin
                        start               <= #dly 1'b0;
                        select[7]           <= #dly 1'b0;
                    end
              end
          8'b01??????:
              begin
                if (~dataSent)
                  begin
                        In_2_reg            <= #dly In_2;
                        Data_reg            <= #dly In_2;
                        EN                  <= #dly
                            8'b10111111;
                        start               <= #dly 1'b1;
                    end
                  else
                    begin
                        select[6]           <= #dly 1'b0;
                        start               <= #dly 1'b0;
                    end
              end
          8'b001?????:
              begin
              if (~dataSent)
                  begin
                      In_3_reg              <= #dly In_3;
                      Data_reg              <= #dly In_3;
                      EN                    <= #dly
                          8'b11011111;
                      start                 <= #dly 1'b1;
                  end
                else
                        begin
                            select[5]       <= #dly 1'b0;
                            start           <= #dly 1'b0;
                          end
              end
          8'b0001????:
              begin
              if (~dataSent)
                  begin
                      In_4_reg              <= #dly In_4;
```

```
                Data_reg                    <= #dly  In_4;
                EN                          <= #dly
                    8'b11101111;
                start                       <= #dly  1'b1;
            end

        else
                begin
                    select[4]               <= #dly  1'b0;
                    start                   <= #dly  1'b0;
                end
    end
8'b00001???:
    begin
    if (~dataSent)
        begin
            In_5_reg                        <= #dly  In_5;
            Data_reg                        <= #dly  In_5;
            EN                              <= #dly
                8'b11110111;
            start                           <= #dly  1'b1;
        end

        else
                begin
                    select[3]               <= #dly  1'b0;
                    start                   <= #dly  1'b0;
                end
    end
8'b000001??:
    begin
    if (~dataSent)
        begin
            In_6_reg                        <= #dly  In_6;
            Data_reg                        <= #dly  In_6;
            EN                              <= #dly
                8'b11111011;
            start                           <= #dly  1'b1;
        end

        else
                begin
                    select[2]               <= #dly  1'b0;
                    start                   <= #dly  1'b0;
                end
    end
8'b0000001?:
    begin
     if (~dataSent)
        begin
            In_7_reg                        <= #dly  In_7;
            Data_reg                        <= #dly  In_7;
            EN                              <= #dly
                8'b11111101;
            start                           <= #dly  1'b1;
        end
      else
                begin
                    select[1]               <= #dly  1'b0;
                    start                   <= #dly  1'b0;
                end
    end
8'b00000001:
    begin
```

```
                        if (~dataSent)
                          begin
                            In_8_reg          <= #dly In_8;
                            Data_reg          <= #dly In_8;
                            EN                <= #dly
                                8'b11111110;
                            start             <= #dly 1'b1;
                          end
                        else
                            begin
                              select[0]       <= #dly 1'b0;
                              start           <= #dly 1'b0;
                            end
                      end
                    default:
                      begin
                        EN                    <= #dly
                            8'b11111111;
                        start                 <= #dly 1'b0;
                      end
                endcase
            end
  end


// State Machine for Sending Configuration Data to Delay Chip NB6L295
/*
    State                   Description
    ------------------------------------------------------------
    RESET                   Resetting all parameters and registers ->
        if (reset): stay; else: to IDLE
    IDLE                    Waiting for start signal from priority
        encoder -> if (start): to LOAD_P0; else: stay
    LOAD_P0                 Load first half of Delay_X - which
        corresponds to data for Delay PD0 on delay chip - into
        temporary register -> to LOAD_P1
    LOAD_P1                 Load second half of Delay_X - which
        corresponds to data for Delay PD1 on delay chip - into
        temporary register -> to SHIFT
    SHIFT                   Shift bits for sending serial bitstream to
        SDIN, assert SLOAD -> to END
    END                     End transmission, deassert SLOAD, inform
        priority encoder about end of transmission -> to IDLE

*/
parameter RESET        = 3'd0;
parameter IDLE     = 3'd1;
parameter LOAD     = 3'd2;
parameter SHIFT    = 3'd3;
parameter END      = 3'd4;
reg [2:0] STATE;
reg [DATA_SHIFT_WIDTH-1:0]       tmp;

always @ (posedge Clk)
begin
    if (Reset)
        begin
            STATE        <= #dly RESET;
            tmp          <= #dly 'd0;
            dataSent     <= #dly 1'b0;
            start_clk    <= #dly 1'b0;
            SLOAD        <= #dly 1'b0;
            clk_cnt      <= #dly 1'b0;
        end
```

```
        else
            begin
                case (STATE)
                    RESET:
                        begin
                            if (Reset)
                                STATE    <= #dly RESET;
                            else
                                STATE    <= #dly IDLE;
                        end // RESET
                    IDLE:
                        begin
                            SDIN        <= #dly 1'b0;
                            clk_cnt     <= #dly 5'd0;
                            dataSent    <= #dly 1'b0;
                            SLOAD       <= #dly 1'b0;

                            if (start & ~dataSent)
                                STATE    <= #dly LOAD;
                            else
                                STATE    <= #dly IDLE;
                        end // IDLE
                    LOAD:
                        begin
                            tmp         <= #dly Data_reg;
                            STATE       <= #dly SHIFT;
                        end // LOAD_W1
                    SHIFT:
                        begin
                            if (clk_cnt < 4'd12) // number of bits to be
                                shifted //
                                begin
                                    start_clk      <= #dly 1'b1;
                                    clk_cnt        <= #dly clk_cnt +1;
                                    tmp            <= #dly
                                        {tmp[DATA_SHIFT_WIDTH-2:0], 1'b0};
                                    SDIN           <= #dly
                                        tmp[DATA_SHIFT_WIDTH-1];
                                end
                            else
                                begin
                                    SLOAD          <= #dly 1'b1;
                                    clk_cnt                    <= #dly
                                        clk_cnt;
                                    start_clk      <= #dly 1'b0;
                                    STATE          <= #dly END;
                                    SDIN           <= #dly 1'b0;
                                end
                        end // SHIFT
                    END:
                        begin
                            SLOAD           <= #dly 1'b0;
                            start_clk       <= #dly 1'b0;
                            dataSent        <= #dly 1'b1;
                            clk_cnt             <= #dly clk_cnt;
                            SDIN            <= #dly 1'b0;
                            STATE           <= #dly IDLE;
                        end // END
                    default:
                        STATE    <= #dly RESET;
                endcase
            end
    end
```

endmodule

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