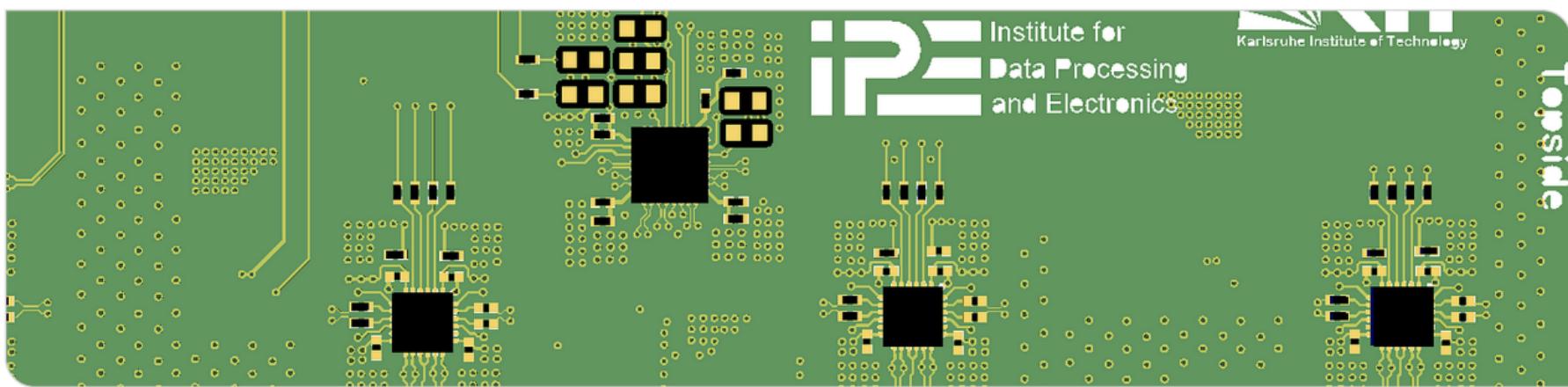


# A Terabit-Sampling System with a Photonics Time-Stretch ADC

Master Thesis Presentation

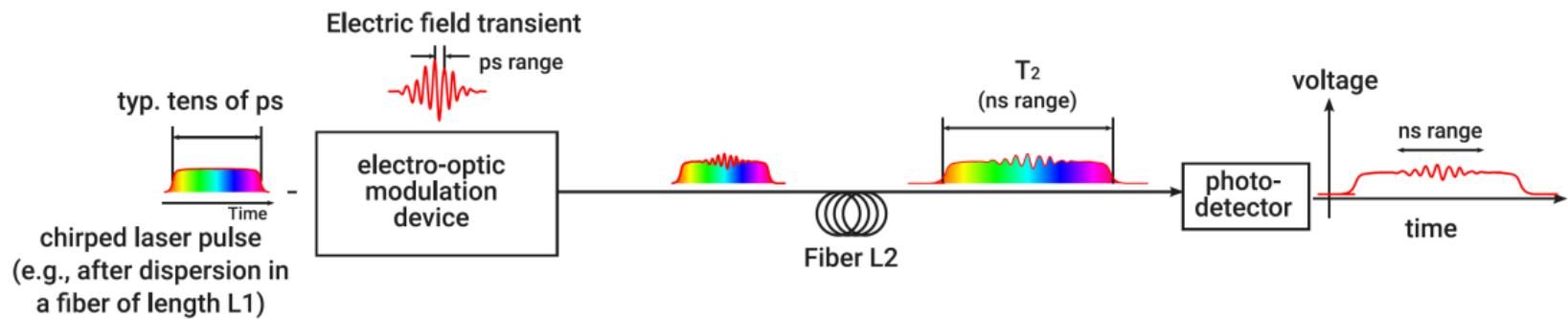
Olena Manzhura | July 20, 2021



# Agenda

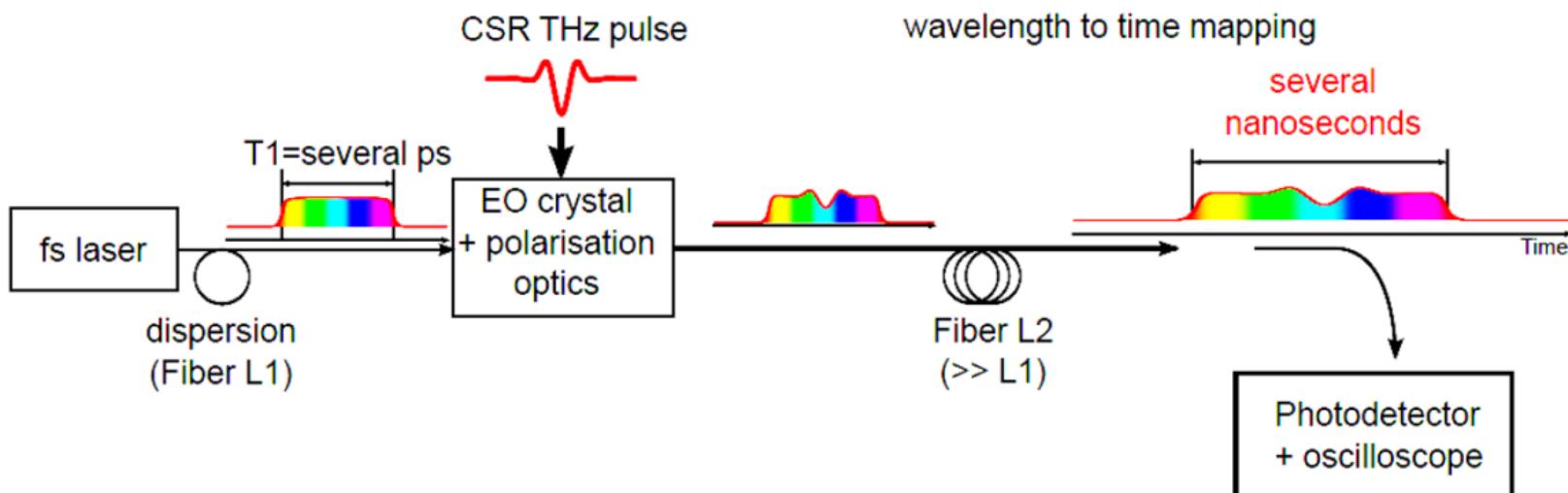
- 1. Introduction**
- 2. Motivation And Objective**
- 3. Architecture**
- 4. Schematics & Layout**
- 5. Outlook**

# Introduction

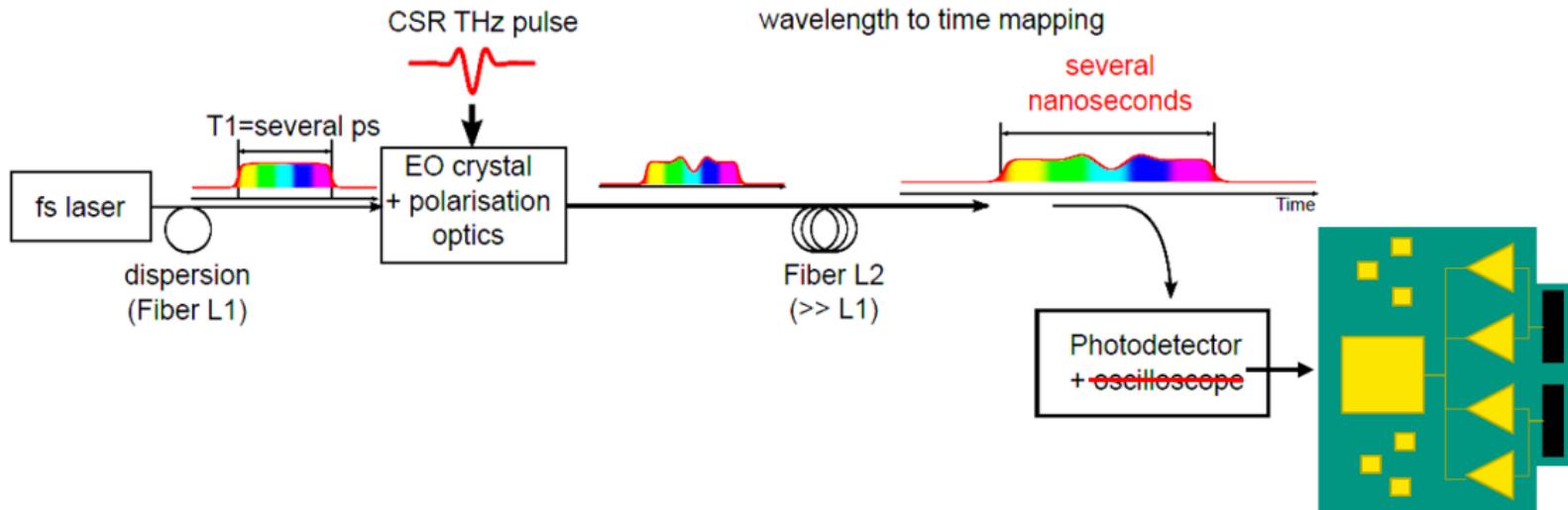


- Brief explanation of principle

# Motivation and Objectives



# Motivation and Objectives



# Motivation and Objectives

- Optical part is done at Lille University
- Work @IPE: Design appropriate read-out system

## Objectives

- Continuously sample ns pulse
- Using time-interleaving method for ADCs
- Compatibility with KARA

# Architecture

- Briefly explain KAPTURE
- ...

# Architecture

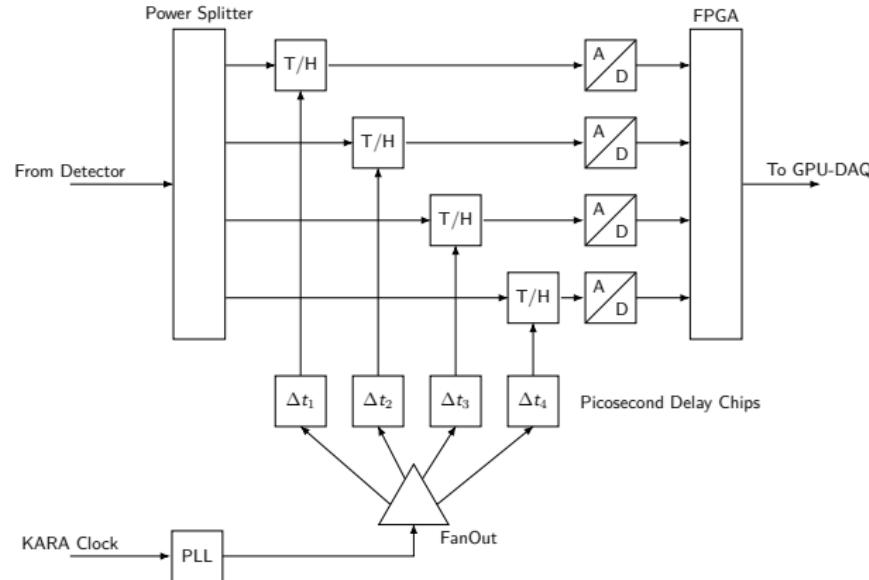


Figure: KAPTURE general principle

# Architecture

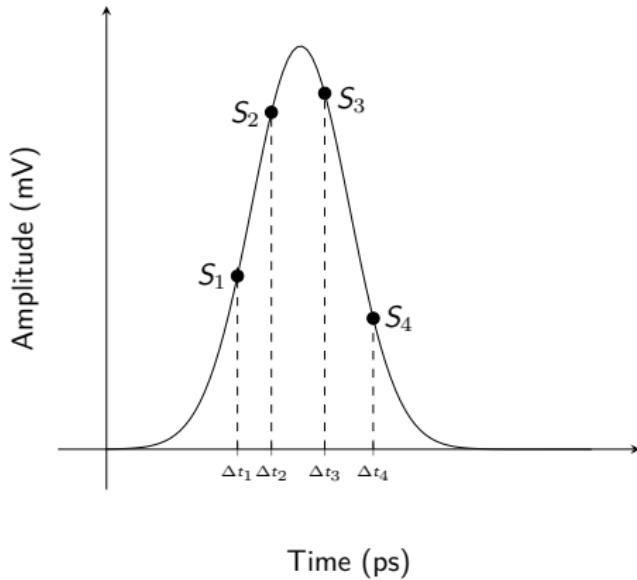
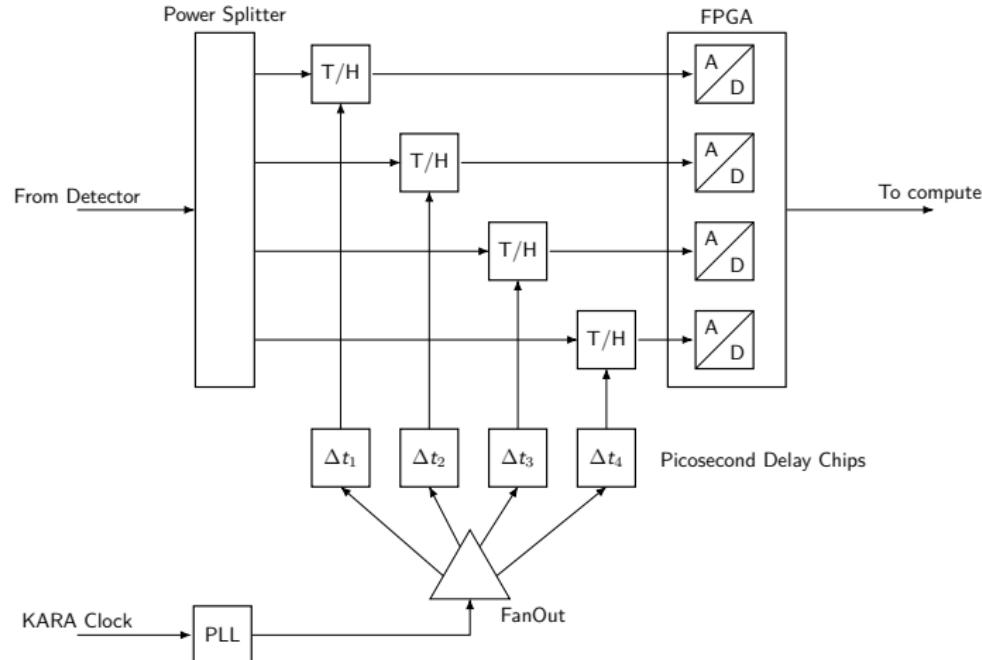
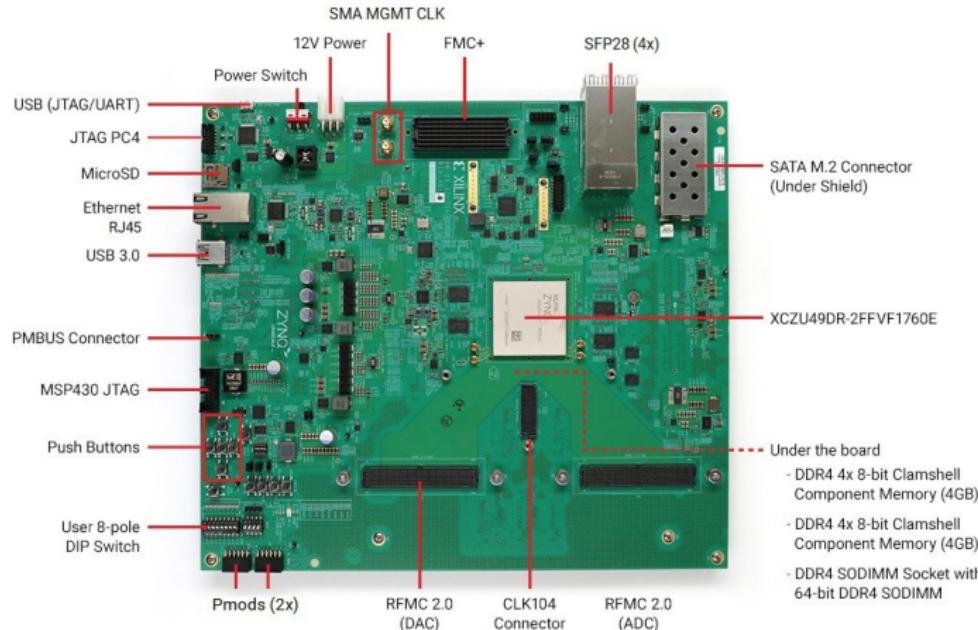


Figure: Sampled pulse

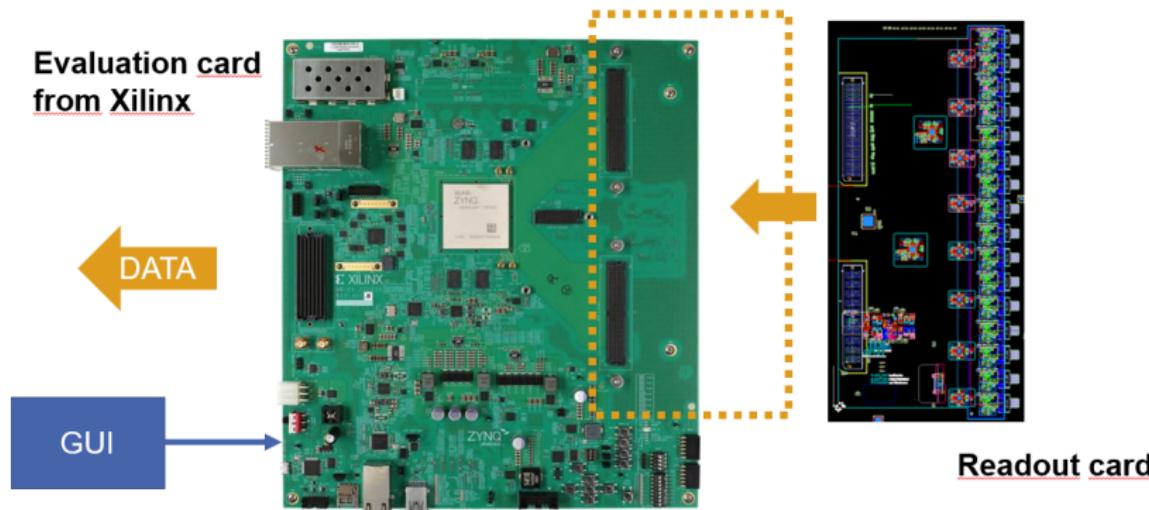
# Architecture



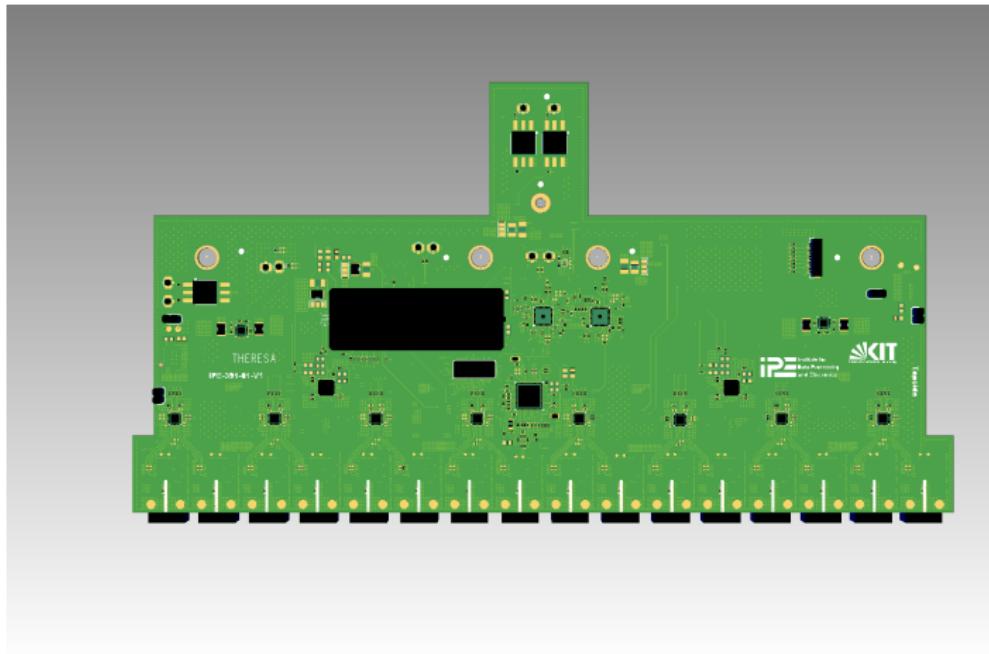
# Architecture



# Architecture



# Schematics & Layout



# Outlook

- Firmware: Xilinx example designs, IPE-own solutions
- Show picture of example design

# Outlook

- Board in production
- Characterization of sampling board → e.g. with Evaluation Tool
- Firmware development for system integration
- Use in experiments, e.g. KARA

# Sources

# Backup (1)

- May help if someone asks