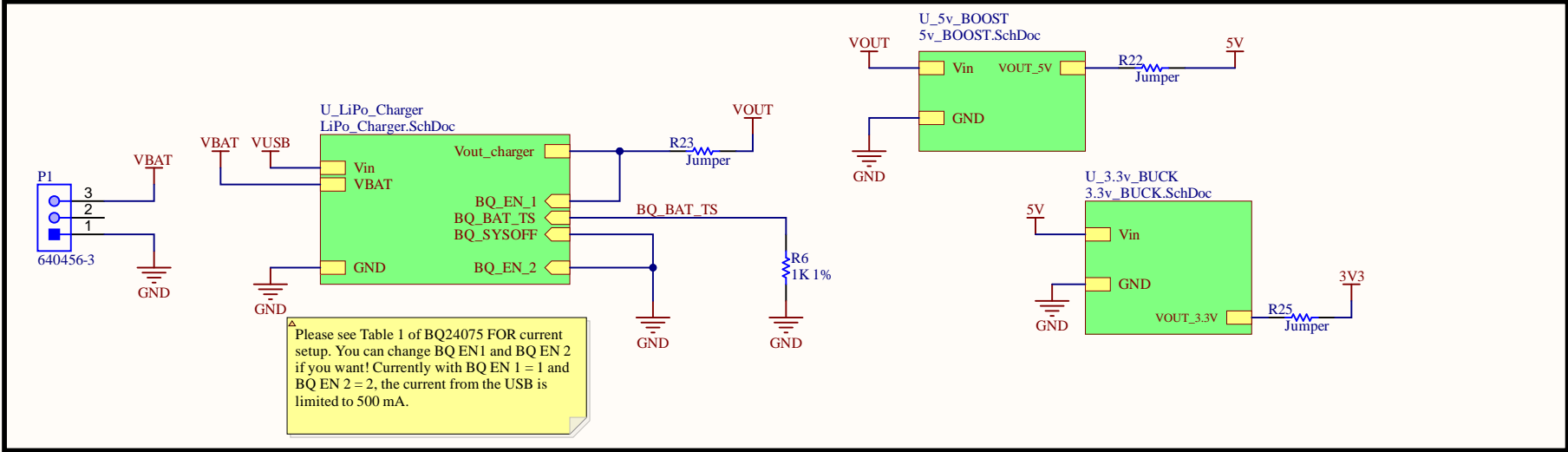


REVISION	DESCRIPTION	DATE	APPROVED

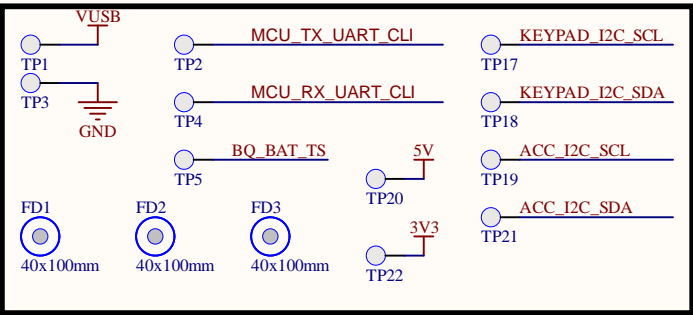
## POWER SUPPLY



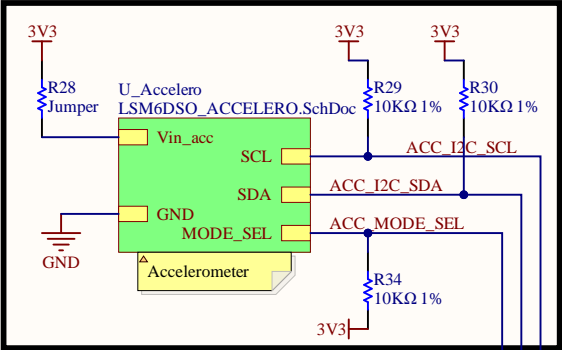
## NOTES

Section to add version notes or any other general information

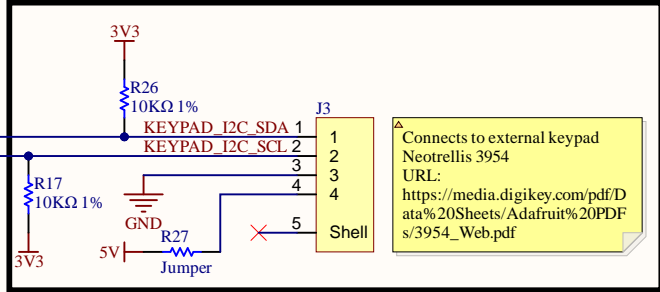
## TEST POINTS AND FIDUCIALS



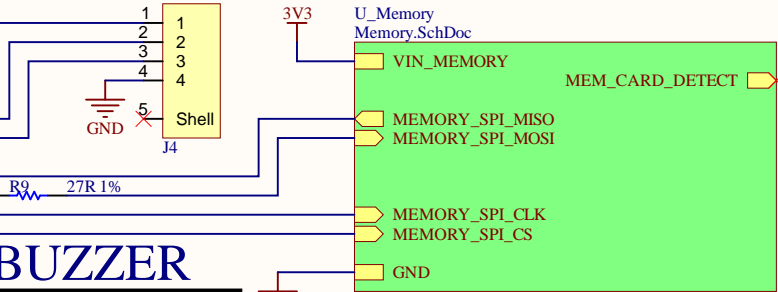
## ACCELEROMETER



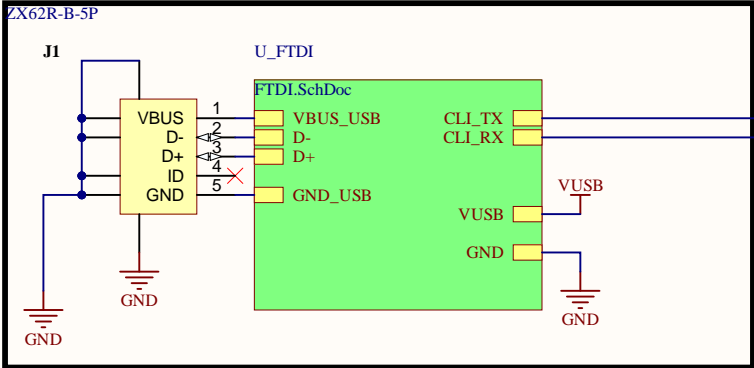
## KEYPAD



## SD CARD MEMORY

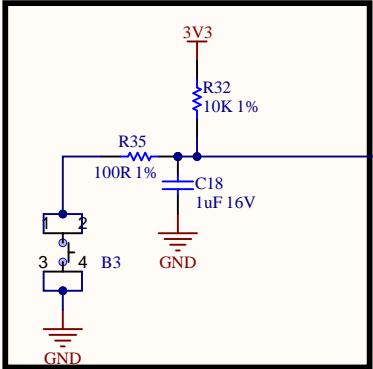


## USB CONNECTOR + FTDI

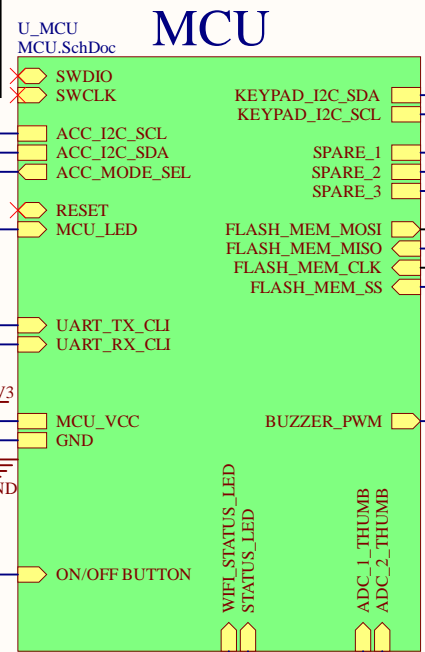


NOTE:  
The FTDI Chip is an useful chip that allows us to convert USART cmessages into USB signals. It allows us to connect the MCU directly to the USB port of a computer and use the serial terminal (it is the same bridge used on the SAMW25 Xplained Board).The FTDI device also contains protection circuitry for the USB.

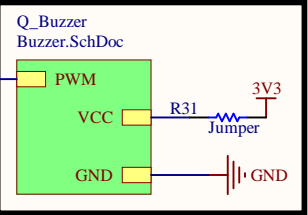
## ON/OFF BUTTON



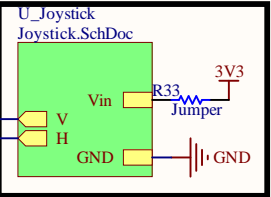
## MCU



## BUZZER



## JOYSTICK



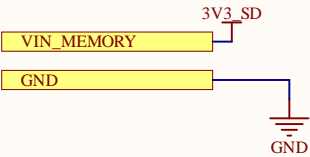
APPROVALS	DATE	PROJECT	260 S 33rd Street Detkin Lab Philadelphia PA 19104	
ENG: SP, PS		Shipwars		
DSN: SP, PS		PROJECT REVISION:	DOCUMENT REVISION:	DESIGN ITEM:
CHK: SP, PS		TITLE		
REFERENCE DOCUMENTS				
BOM:				
ASSY DWG:				
FAB DWG:				
PCB DWG:				
SIZE		CAGE CODE	DWG NO.	REV
B				1.0.0
SCALE:		FILE NAME	SHEET 1 OF 10	
		MAIN.SchDoc		

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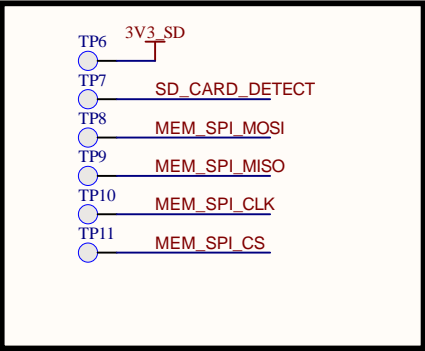
DWG. NO. 1.020  
REV. SMT

REVISION	DESCRIPTION	DATE	APPROVED

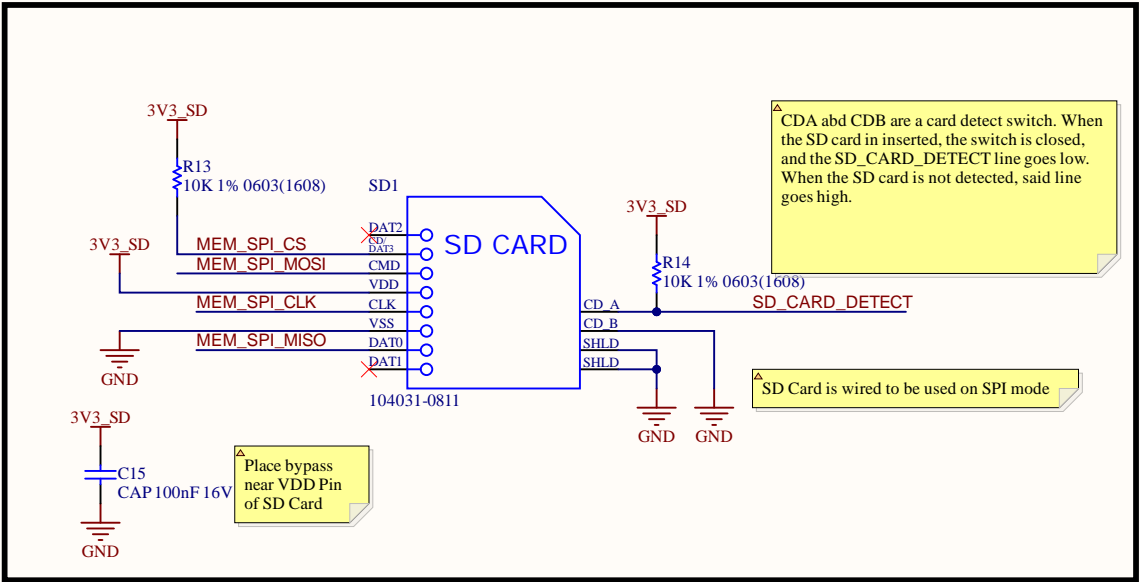
MEMORY_SPI_MOSI	MEM_SPI_MOSI
MEMORY_SPI_MISO	MEM_SPI_MISO
MEMORY_SPI_CLK	MEM_SPI_CLK
MEMORY_SPI_CS	MEM_SPI_CS
MEM_CARD_DETECT	SD_CARD_DETECT




## TESTPOINTS



## SD CARD

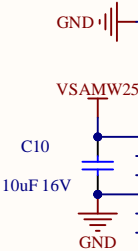
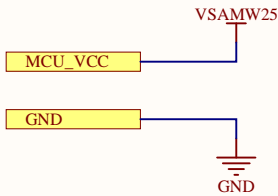


APPROVALS		DATE		PROJECT		 290 S 33rd Street Detkin Lab Philadelphia PA 19104	
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DSN:	SP, PS			PROJECT REVISION:		DOCUMENT REVISION:	
CHK:	SP, PS					DESIGN ITEM:	
REFERENCE DOCUMENTS				TITLE			
				Shipwars Memory Schematic			
BOM:				SIZE		CAGE CODE	
ASSY DWG:				B		DWG NO.	
FAB DWG:						REV	
PCB DWG:				SCALE:		FILE NAME	
						Memory.SchDoc	
				SHEET		2 OF 10	

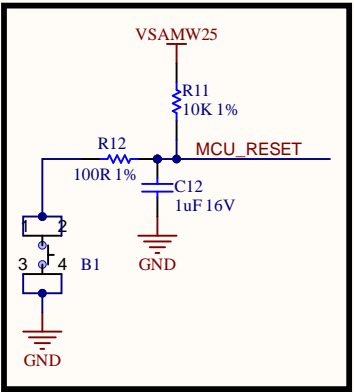
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DWG. NO. 1.030  
REV. SHI

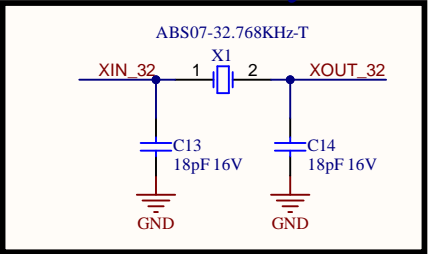
REVISION	DESCRIPTION	DATE	APPROVED



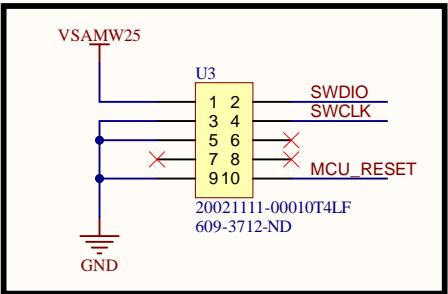
## Reset Button



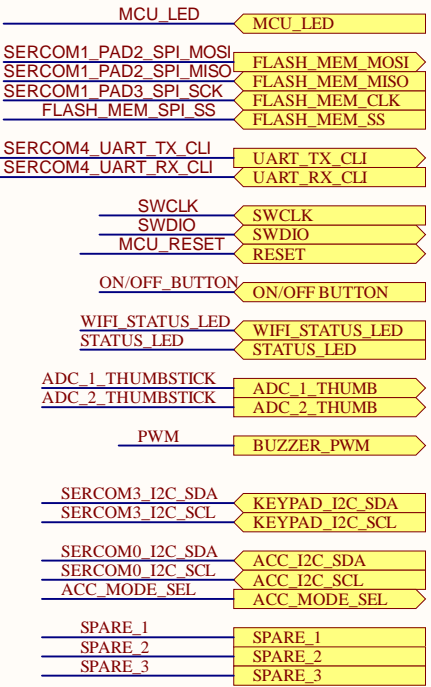
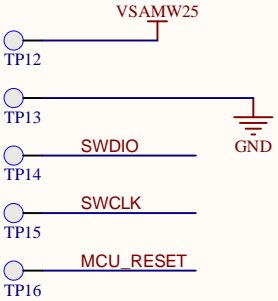
## 32.768 Crystal



<sup>a</sup> Calculation of crystal load capacitors:  
 $C_{ext} = 2 \times (C_{crystal} - C_{para} - C_{pcb})$   
  
Crystal = 12.5pF (from crystal datasheet)  
Cpara = 3.15pF (from MCU datasheet)  
Cpcb = 0.5pF (estimate)  
  
 $C_{ext} = 2 \times (12.5pF - 3.15pF - 0.5pF) = 17.7pF$



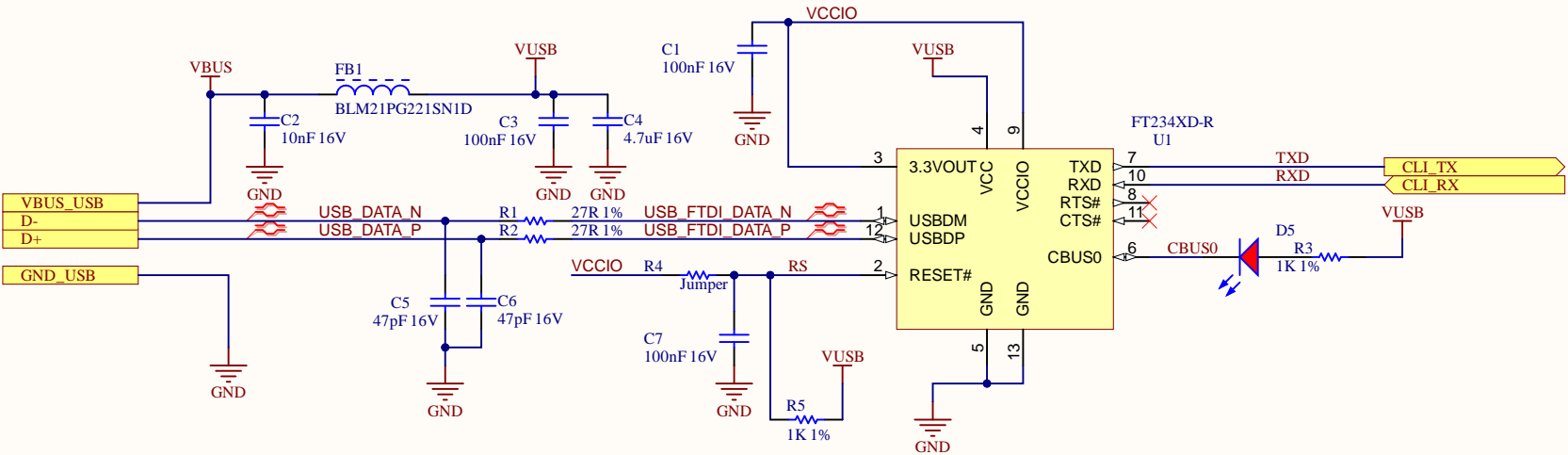
## DEBUGGER PORT



APPROVALS	DATE	PROJECT	200 S 33rd Street Detkin Lab Philadelphia PA 19104		
ENG: SP, PS		Shipwars	Penn Engineering		
DSN: SP, PS		PROJECT REVISION:	DOCUMENT REVISION:	DESIGN ITEM:	
CHK: SP, PS		TITLE			
REFERENCE DOCUMENTS		Shipwars MCU Schematic			
BOM:		SIZE	CAGE CODE	DWG NO.	REV
ASSY DWG:		B			.1.0.0
FAB DWG:		SCALE:	FILE NAME	MCU.SchDoc	
PCB DWG:				SHEET	3 OF 10

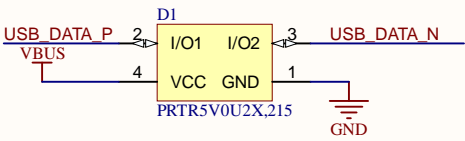
REVISION	DESCRIPTION	DATE	APPROVED


# FTDI CHIP



△ Schematics follows Fig. 6.1 of Datasheet

## USB ESD PROTECTION

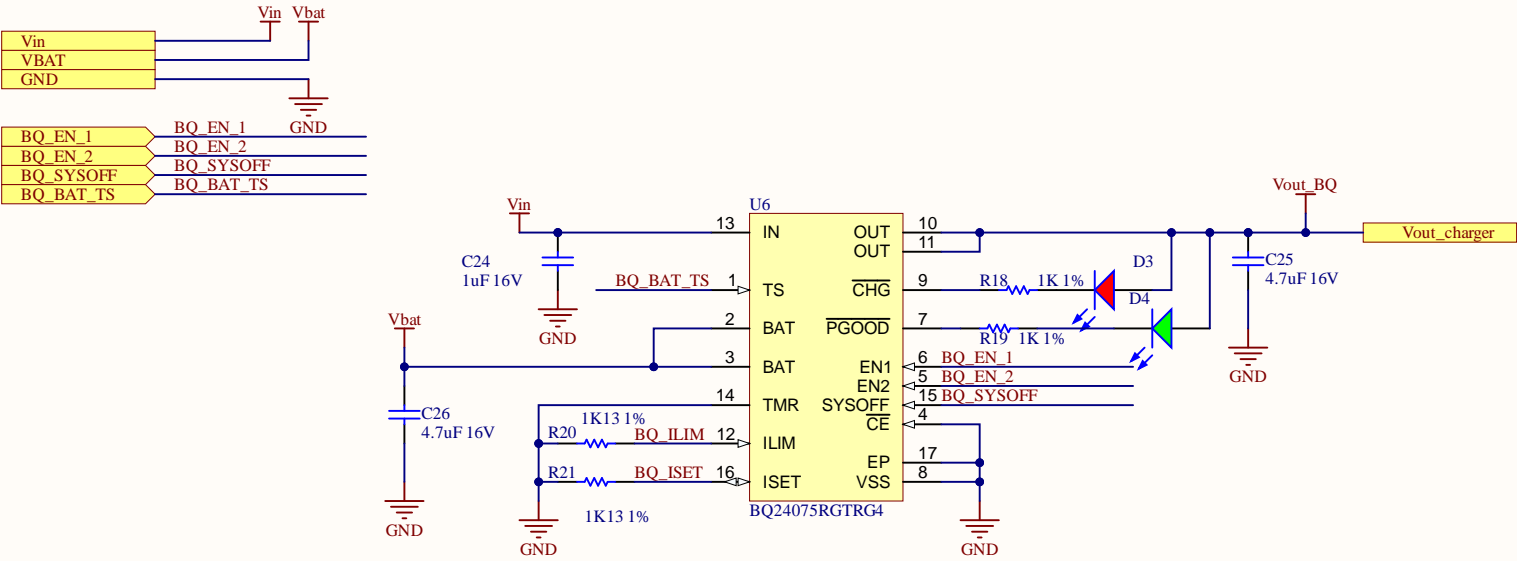


APPROVALS		DATE		PROJECT		 <div> <div>290 S 33rd Street</div> <div>Detkin Lab</div> <div>Philadelphia</div> <div>PA 19104</div> </div>	
ENG:	SP, PS			Shipwars			
DSN:	SP, PS			PROJECT REVISION:		DOCUMENT REVISION:	
CHK:	SP, PS					DESIGN ITEM:	
REFERENCE DOCUMENTS				TITLE			
BOM:				Shipwars FTDI Schematic			
ASSY DWG:				SIZE	CAGE CODE	DWG NO.	REV
FAB DWG:				B			1.0.0
PCB DWG:				SCALE:	FILE NAME	SHEET	OF
					FTDI.SchDoc	4	10

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REV.1 SHIT

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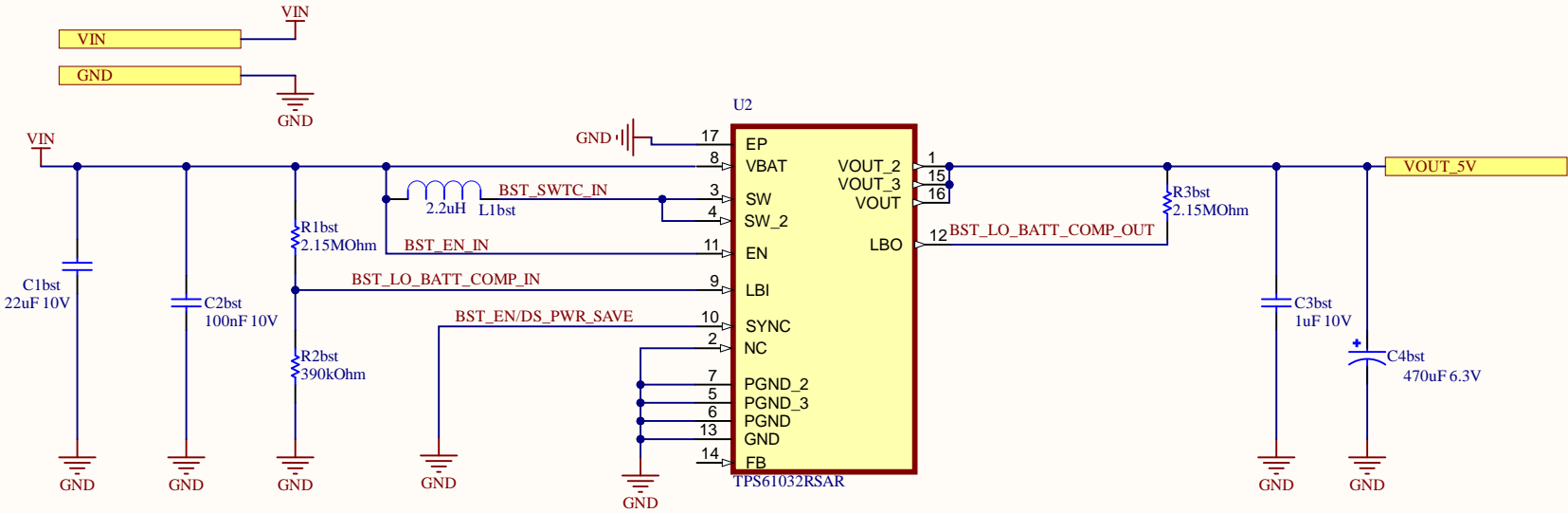


ilim = Kilim/Rilim => 1610/1130 = 1.42A  
(if EN2=1, EN1=0)

ISET = KISET/RISET => 890/1130 = 0.788A

APPROVALS	DATE	PROJECT	Shipwars		
ENG: SP, PS		PROJECT REVISION:	DOCUMENT REVISION:	DESIGN ITEM:	
DSN: SP, PS		TITLE			
CHK: SP, PS		Shipwars Charger Shematic			
REFERENCE DOCUMENTS		SIZE	CAGE CODE	DWG NO.	REV
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ASSY DWG:		SCALE:	FILE NAME	SHEET	OF
FAB DWG:			LiPo_Charger.SchDoc	5	10
PCB DWG:					


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TPS61032  
VIN: 3.3V to 5V  
OUT: 5V up to 2A  
REF: <https://webench.ti.com/appinfo/webench/scripts/SDP.cgi?ID=0929BF869665908F>

DWG. NO. 1.0.0

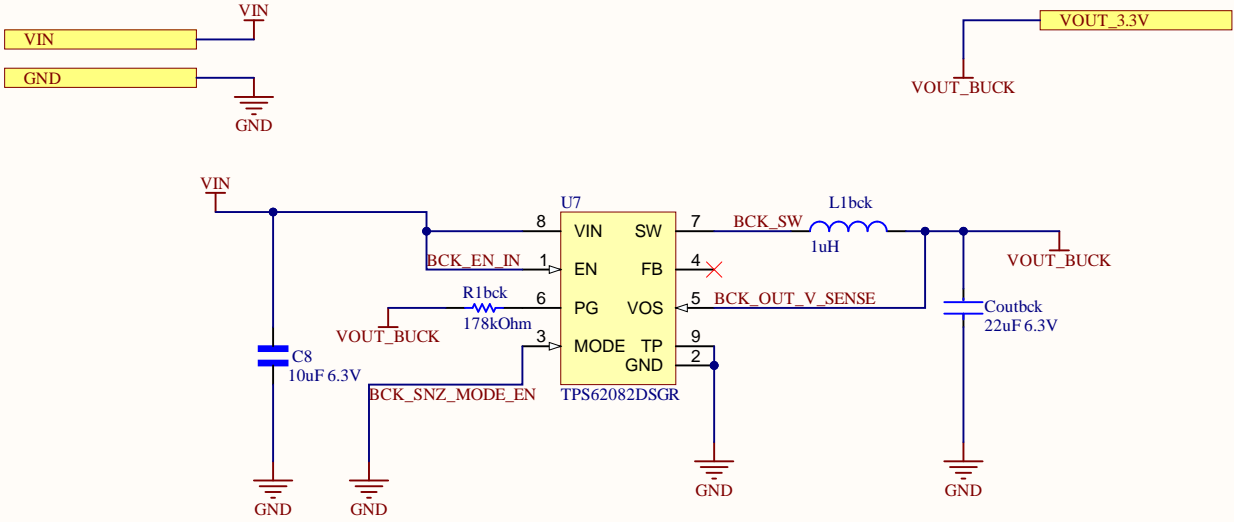
REVISION	DESCRIPTION	DATE	APPROVED

APPROVALS		DATE	PROJECT		 <div>Penn Engineering <small>PHILADELPHIA, PA</small></div>		200 S 33rd Street Detkin Lab Philadelphia PA 19104							
ENG:	SP, PS		Shipwars				PROJECT REVISION:		DOCUMENT REVISION:		DESIGN ITEM:			
DSN:	SP, PS													
CHK:	SP, PS													
REFERENCE DOCUMENTS			TITLE											
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FAB DWG:			B								.1.0.0			
PCB DWG:			SCALE:	FILE NAME		5v BOOST.SchDoc					SHEET	6	OF	10


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DWG. NO. 1.0.0  
REV. SHT.

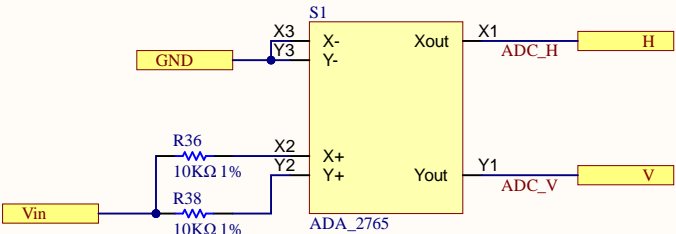
REVISION	DESCRIPTION	DATE	APPROVED



TPS62082  
VIN: 4.5V to 5.5V  
OUT: 3.3V up to 1.2A  
REF: <https://webench.ti.com/appinfo/webench/scripts/SDP.cgi?ID=769E7FCD3E8DDF5A>  
TP = thermal pad -> connect to GND according to Datasheet

APPROVALS		DATE	PROJECT  Shipwars	 <b>Penn Engineering</b> <small>PHILADELPHIA, PENNSYLVANIA</small>	200 S 33rd Street Detkin Lab Philadelphia PA 19104	
ENG:	SP, PS					
DSN:	SP, PS					
CHK:	SP, PS					
REFERENCE DOCUMENTS					Shipwars Buck Schematic	
BOM:						
ASSY DWG:						
FAB DWG:						
PCB DWG:			SCALE:	FILE NAME	3.3v_BUCK.SchDoc	SHEET 7 OF 10

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Sparkfun COM-09032 Thumb Joystick

REF:  
<http://cdn.sparkfun.com/datasheets/BreakoutBoards/Joystick-Breakout-v12b.pdf>

pin reference in :

REVISION	DESCRIPTION	DATE	APPROVED

APPROVALS		DATE	PROJECT		<div><div><div></div><div>Penn Engineering</div><div>UNIVERSITY OF PENNSYLVANIA</div></div><div>200 S 33rd Street Detkin Lab Philadelphia PA 19104</div></div>					
ENG:	SP, PS		Shipwars							
DSN:	SP, PS		PROJECT REVISION:		DOCUMENT REVISION:		DESIGN ITEM:			
CHK:	SP, PS		TITLE							
REFERENCE DOCUMENTS			Shipwars Joystick Schematic							
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					SHEET		8	OF 10		

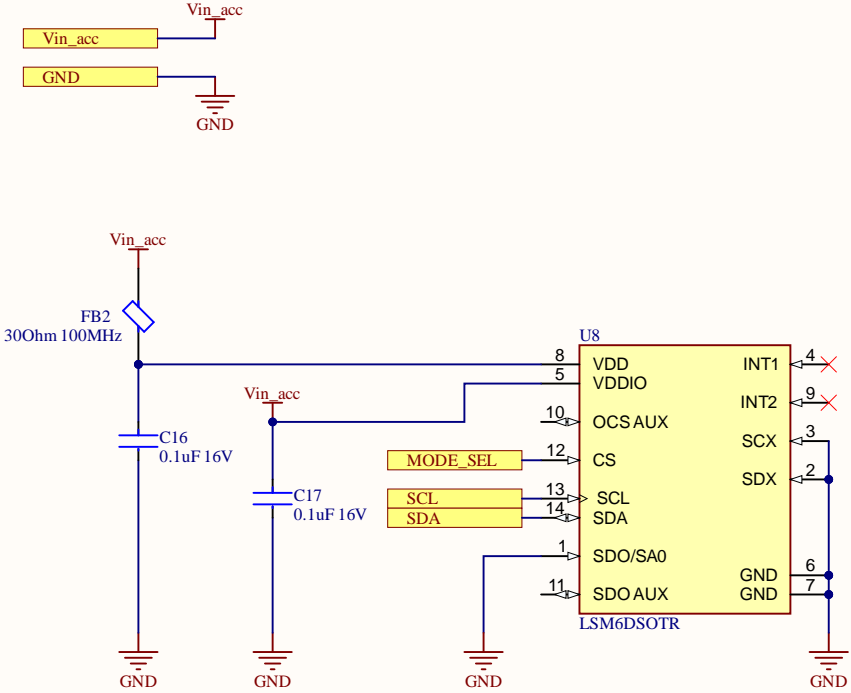


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Text



SLM6DSOTR ACCELEROMETER

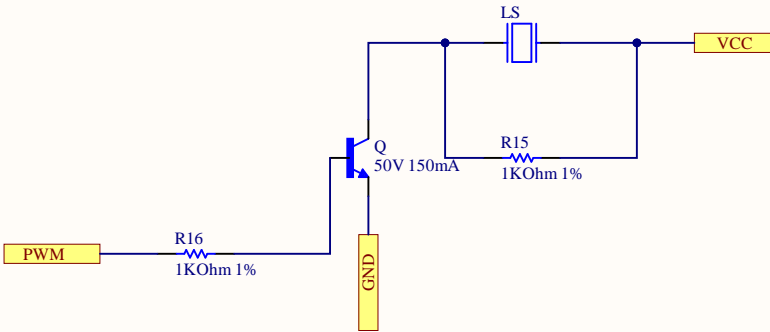
REF: [https://cdn.sparkfun.com/assets/3/1/6/b/c/SparkFun\\_Qwiic\\_6DoF\\_LSM6DSO\\_Schematic.pdf](https://cdn.sparkfun.com/assets/3/1/6/b/c/SparkFun_Qwiic_6DoF_LSM6DSO_Schematic.pdf)

OR

REF: <https://www.st.com/resource/en/datasheet/lsm6dso.pdf> (Page35)

APPROVALS	DATE	PROJECT	200 S 33rd Street Detkin Lab Philadelphia PA 19104		
ENG: SP, PS		Shipwars	Penn Engineering		
DSN: SP, PS		PROJECT REVISION:	DOCUMENT REVISION:	DESIGN ITEM:	
CHK: SP, PS		TITLE			
REFERENCE DOCUMENTS		Shipwars Accelerometer Schematic			
BOM:		SIZE	CAGE CODE	DWG NO.	REV
ASSY DWG:		B			.1.0.0
FAB DWG:		SCALE:	FILE NAME	SHEET	OF
PCB DWG:			LSM6DSO_ACCELERO.SchDoc	9	10


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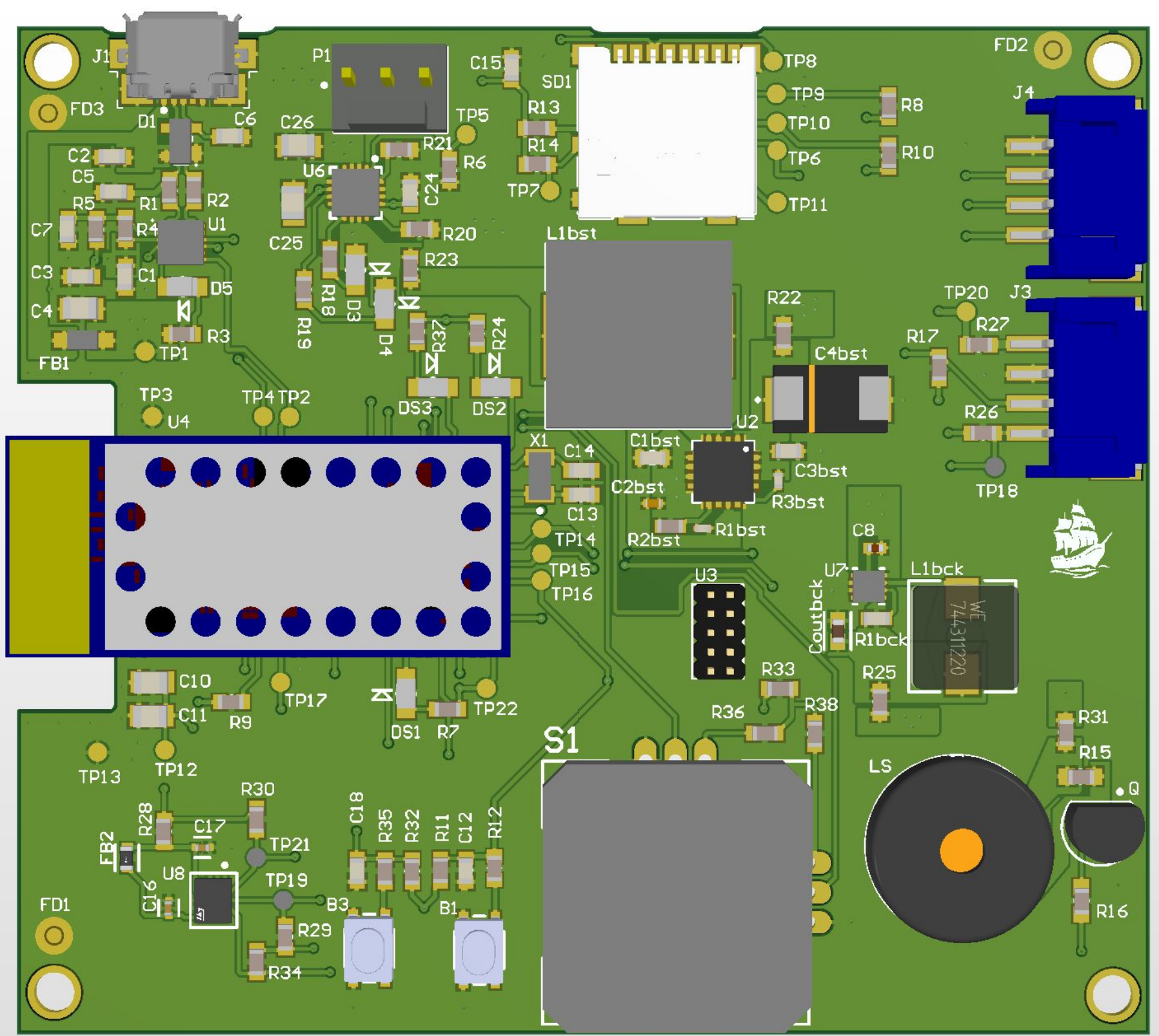


PS1240P02BT 3V 4kHz buzzer  
REF:  
<https://www.snapeda.com/parts/PS1240P02BT/TDK%20Corporation/datasheet/> (page 2)

DWG. NO. 1.0.0  
REV. SHI

REVISION	DESCRIPTION	DATE	APPROVED

APPROVALS		DATE	PROJECT		 <div>Penn Engineering <small>UNIVERSITY OF PENNSYLVANIA</small></div>		200 S 33rd Street Detkin Lab Philadelphia PA 19104		
ENG:	SP, PS		Shipwars						
DSN:	SP, PS		PROJECT REVISION:		DOCUMENT REVISION:		DESIGN ITEM:		
CHK:	SP, PS		TITLE						
REFERENCE DOCUMENTS			Shipwars Buzzer Schematic						
BOM:			SIZE	CAGE CODE	DWG NO.			REV	
ASSY DWG:			B					.1.0.0	
FAB DWG:									
PCB DWG:			SCALE:		FILE NAME				SHEET
			Buzzer.SchDoc						

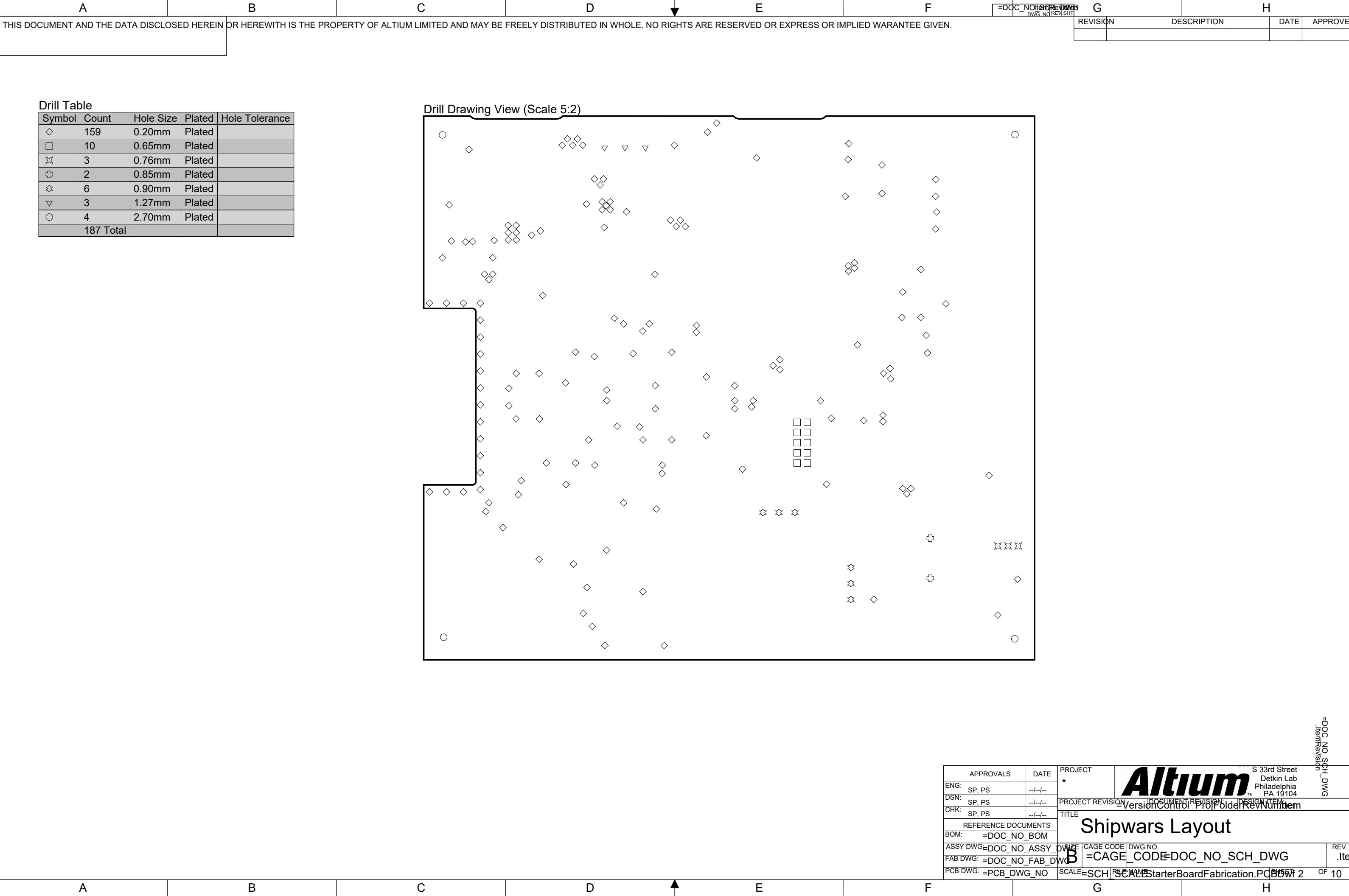


View from Top side (Scale 2:1)




Total thickness: 1.53mm

APPROVALS		DATE		PROJECT		S 33rd Street Detkin Lab Philadelphia PA 19104		SCH_DWG	
ENG: SP, PS		--/--/--		*		<b>Altium</b>			
DSN: SP, PS		--/--/--		PROJECT REVISION		DOCUMENT REVISION		DESIGN ITEM	
CHK: SP, PS		--/--/--		TITLE		Version Control		Proj Older Rev Number	
REFERENCE DOCUMENTS				Shipwars Layout					
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ASSY DWG: =DOC_NO_ASSY				DWG NO.					
FAB DWG: =DOC_NO_FAB_DWG				=CAGE CODE		=DOC_NO_SCH_DWG			
PCB DWG: =PCB_DWG_NO				SCALE		OF 10			





APPROVALS	DATE	PROJECT	S 33rd Street Detkin Lab Philadelphia PA 19104		PH_DWG
ENG: SP, PS	--/--/--	*			
DSN: SP, PS	--/--/--				
CHK: SP, PS	--/--/--	PROJECT REVISION: 1	DOCUMENT REVISION: 1	DESIGN: 1	ITEM
REFERENCE DOCUMENTS		TITLE			
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FAB DWG: =DOC_NO_FAB_DWG	DWG	=CAGE	CODE=DOC_NO_SCH_DWG	.ltd	
PCB DWG: =PCB_DWG_NO	SCH	PCB DWG		OF 10	





PROJECT	<b>Altium</b>		S 33rd Street Detkin Lab Philadelphia PA 19104	CH_DWG
PROJECT REVISION	DOCUMENT REVISION	DESIGN REVISION	Version Control Proj Folder Rev Number Item	
E Shipwars Layout				
E	CAGE CODE =CAGE	DWG NO. CODE=DOC_NO_SCH_DWG	REV .lter	
E	SCH / SCALE StarterBoardFabrication.PCBDFW 5			OF 10







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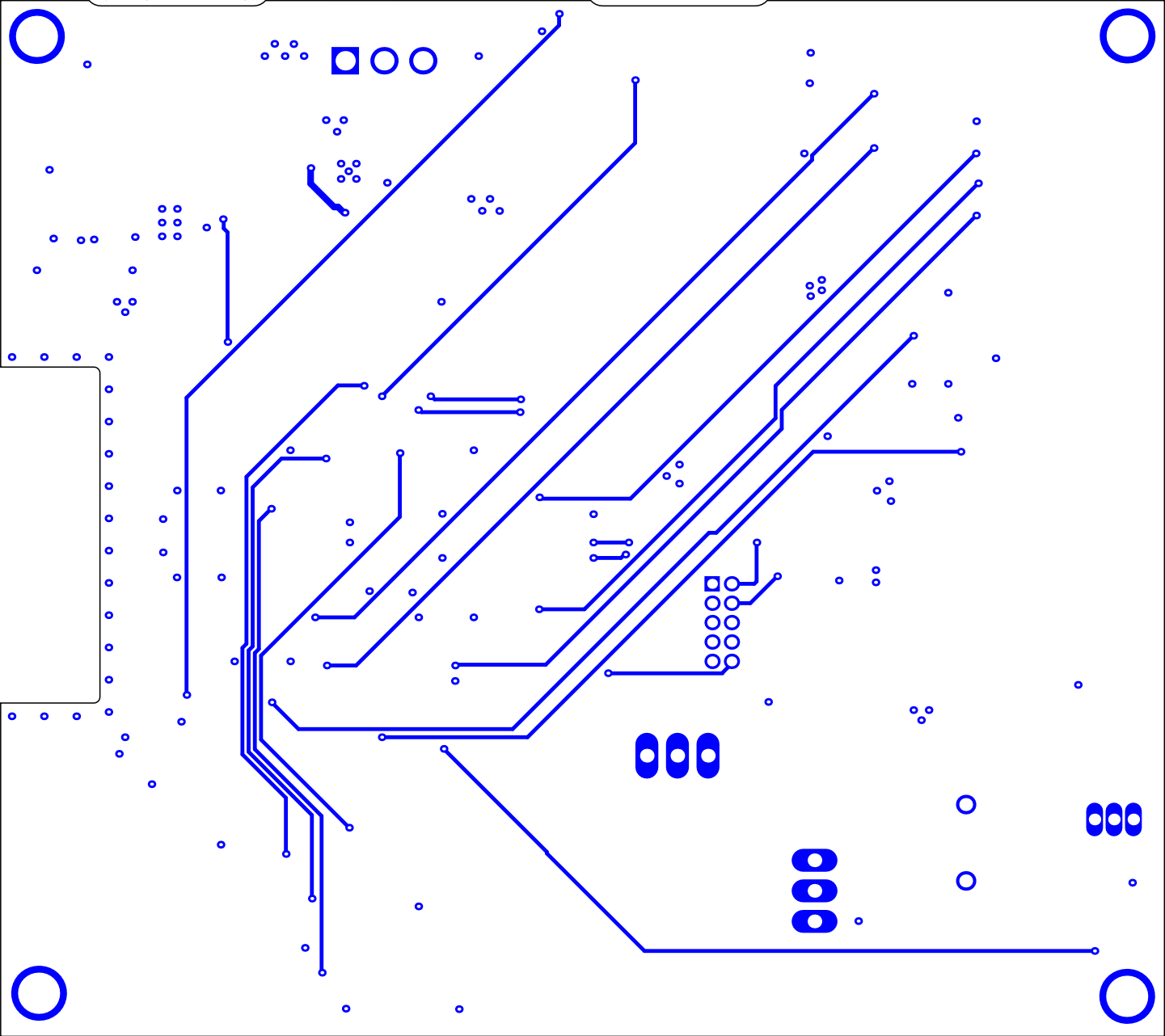
F

G

H

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Bottom Layer (Scale 5:2)



APPROVALS	DATE	PROJECT
ENG: SP, PS	--/--/--	*
DSN: SP, PS	--/--/--	PROJECT REVISION
CHK: SP, PS	--/--/--	DOCUMENT REVISION
REFERENCE DOCUMENTS		DESIGN ITEM
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ASSY DWG: =DOC_NO_ASSY_DWG	SIZE	CAGE CODE
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PCB DWG: =PCB_DWG_NO	SCALE	FILE NAME

Altium

S 33rd Street  
Detkin Lab  
Philadelphia  
PA 19104

Version Control

ProjFolderRevNumberItem

Shipwars Layout

REV 8 OF 10

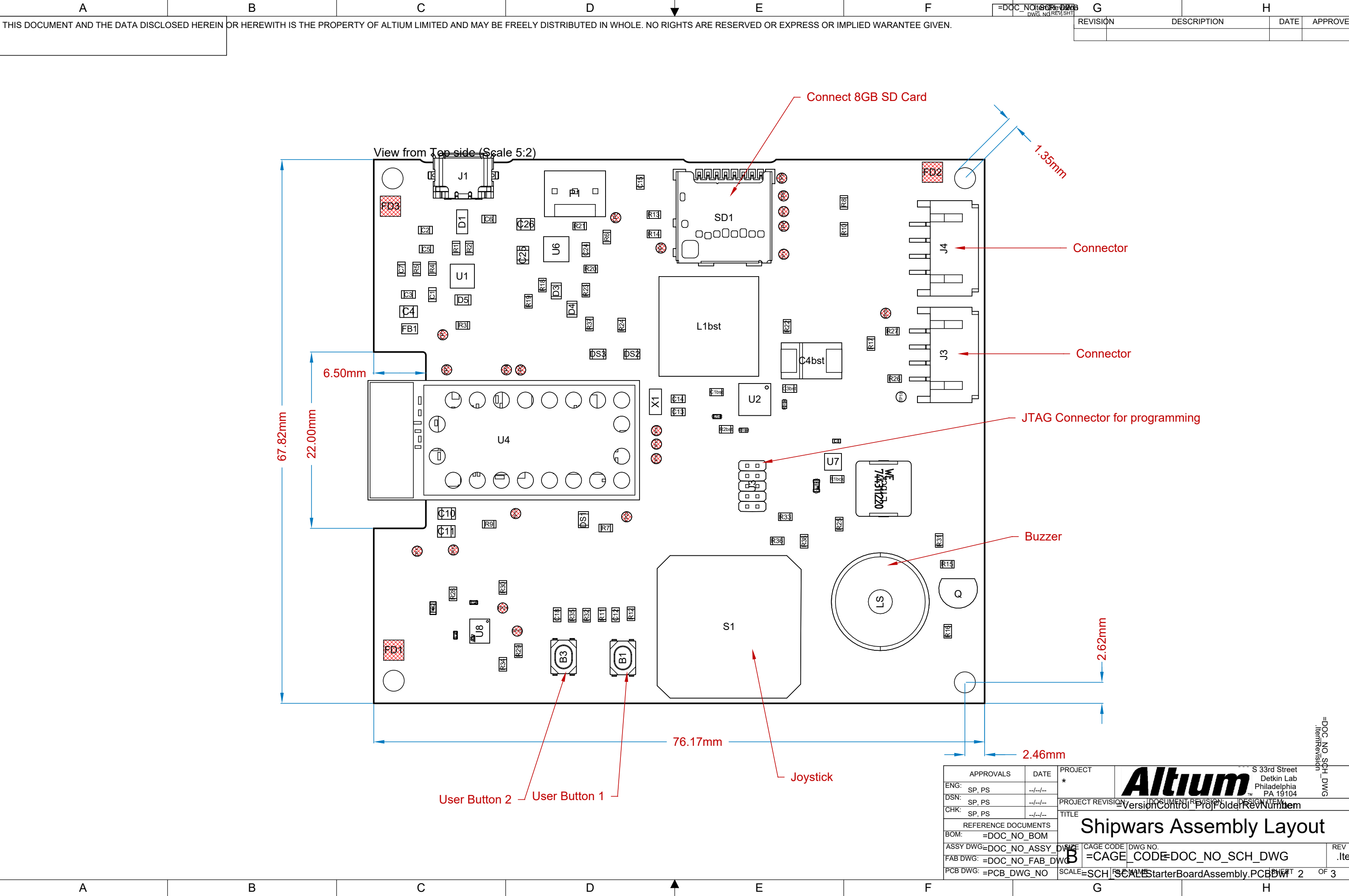
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.ItemR









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View from Bottom side (Scale 5:2)

APPROVALS

DATE

PROJECT

ENG: SP, PS

--/--/--

\*

DSN: SP, PS

--/--/--

PROJECT REVISION

CHK: SP, PS

--/--/--

DOCUMENT REVISION

REFERENCE DOCUMENTS

TITLE

DESIGN ITEM

BOM: =DOC\_NO\_BOM

ASSY DWG: =DOC\_NO\_ASSY\_DWG

FAB DWG: =DOC\_NO\_FAB\_DWG

PCB DWG: =PCB\_DWG\_NO

SIZE

CAGE CODE

DWG NO.

REV

B

=CAGE\_CODE

=DOC\_NO\_SCH\_DWG

.ItemR

SCALE

=SCH\_SCALE

STARTERBOARDASSEMBLY.PCB.DWG

3

OF 3

Altium

S 33rd Street  
Detkin Lab  
Philadelphia  
PA 19104

=DOC\_NO\_SCH\_DWG

.ItemR

REVISION

DESCRIPTION

DATE

APPROVED