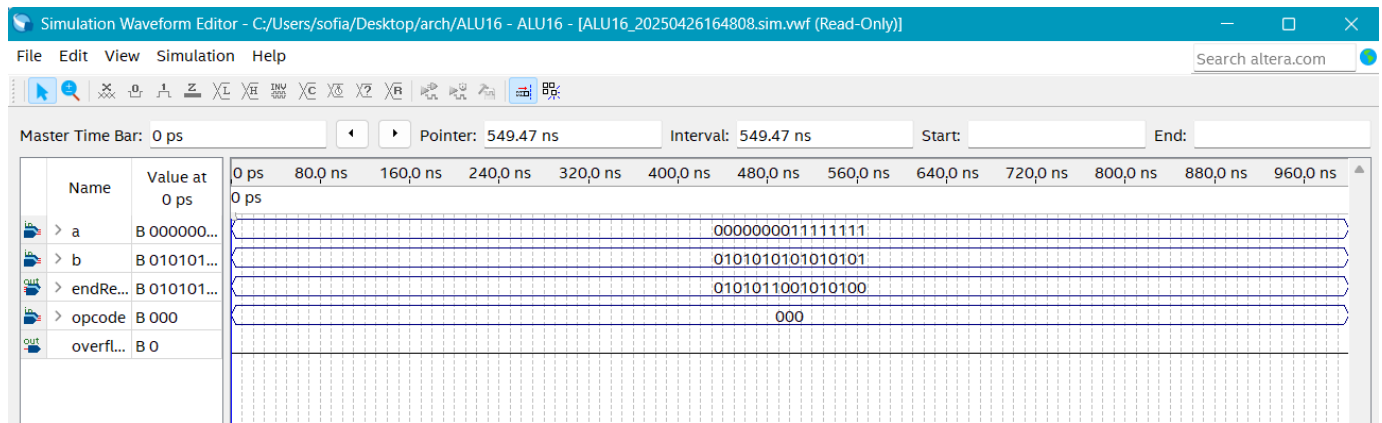
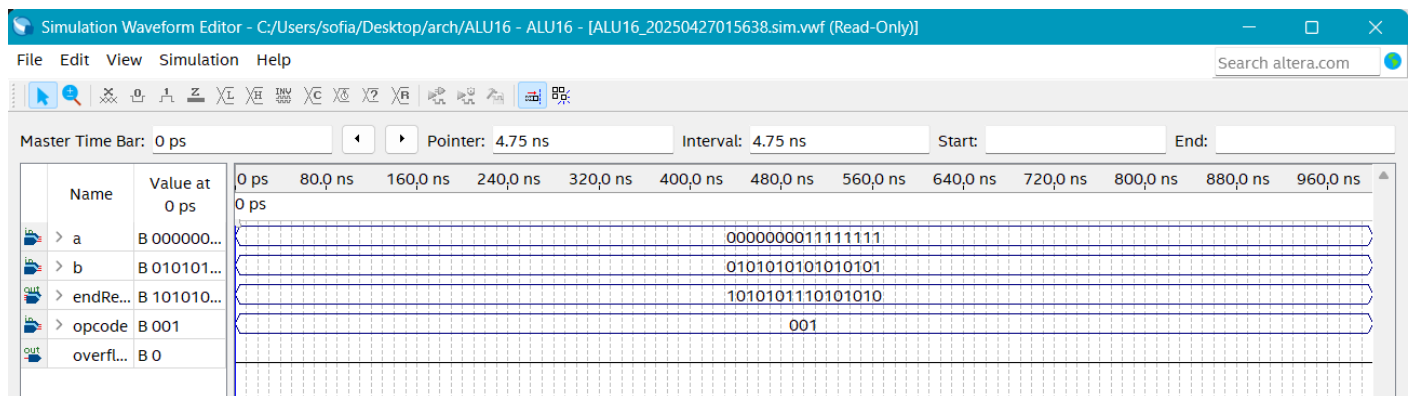


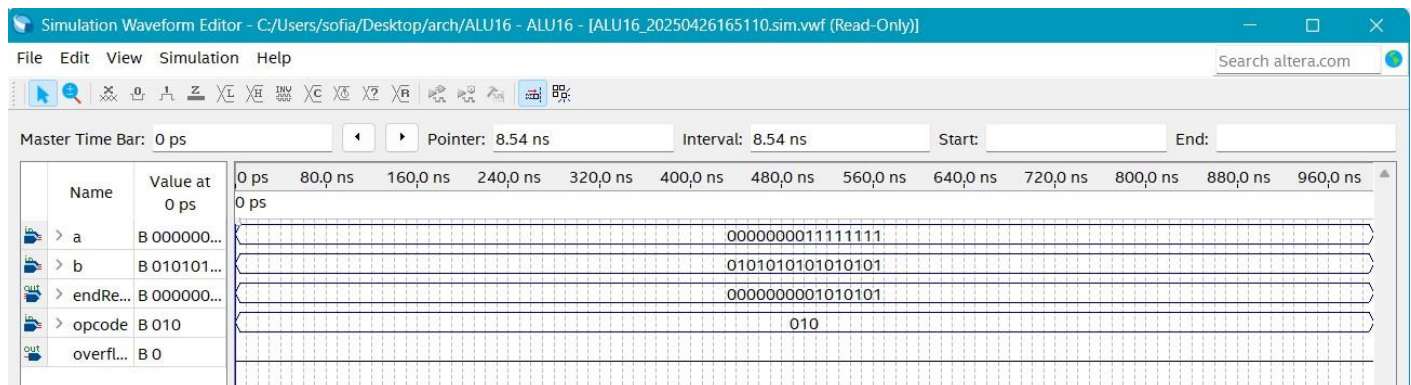
# Arithmetic Addition (ADD)



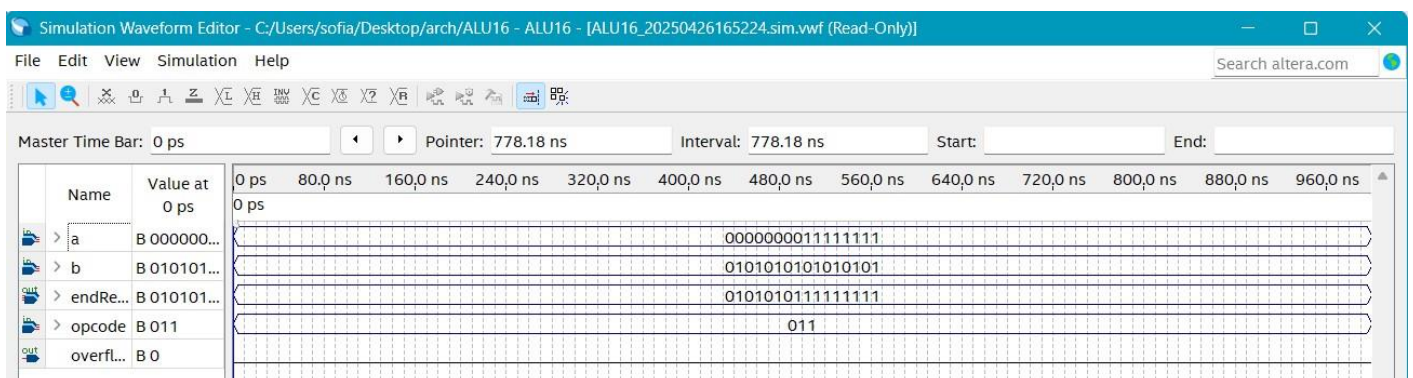
# Arithmetic Subtraction (SUB)



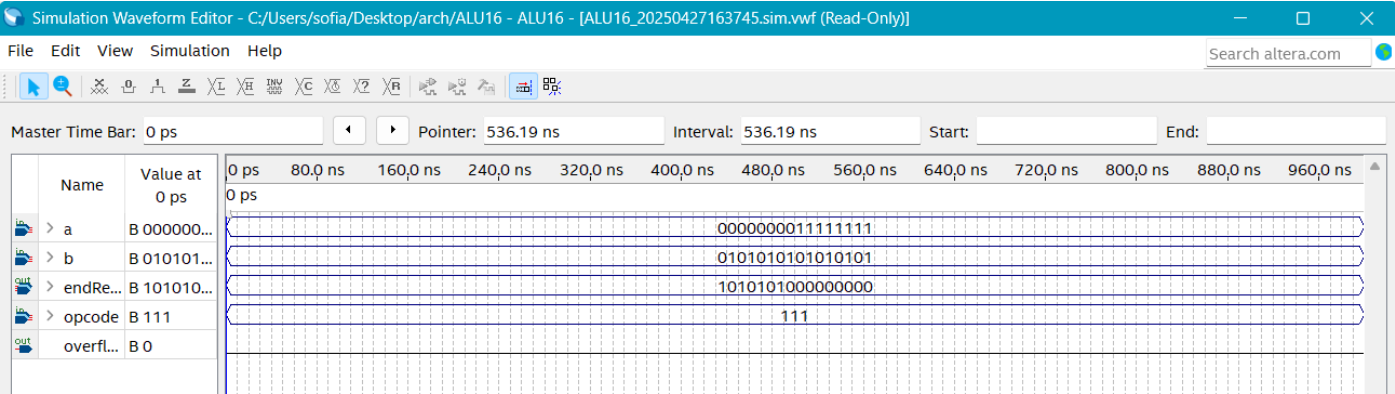
# Logical AND



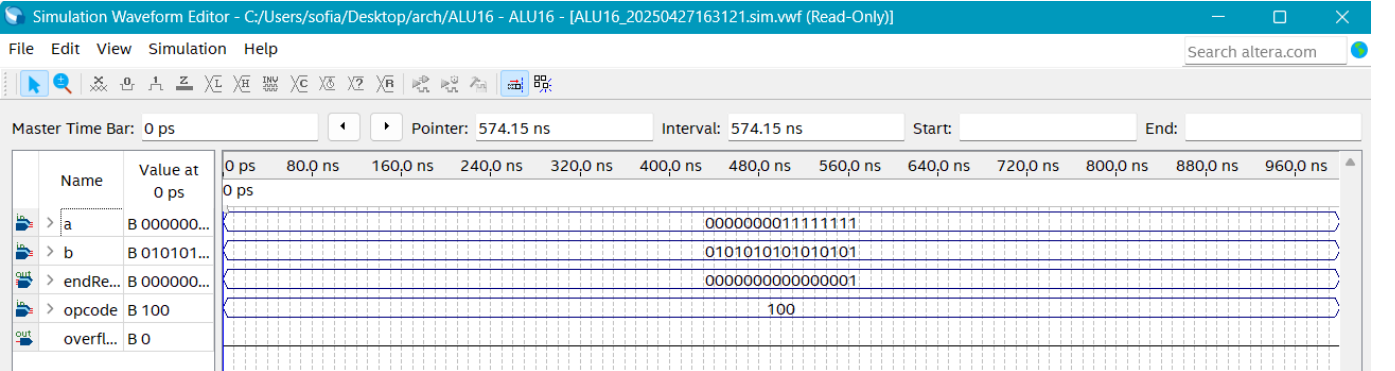
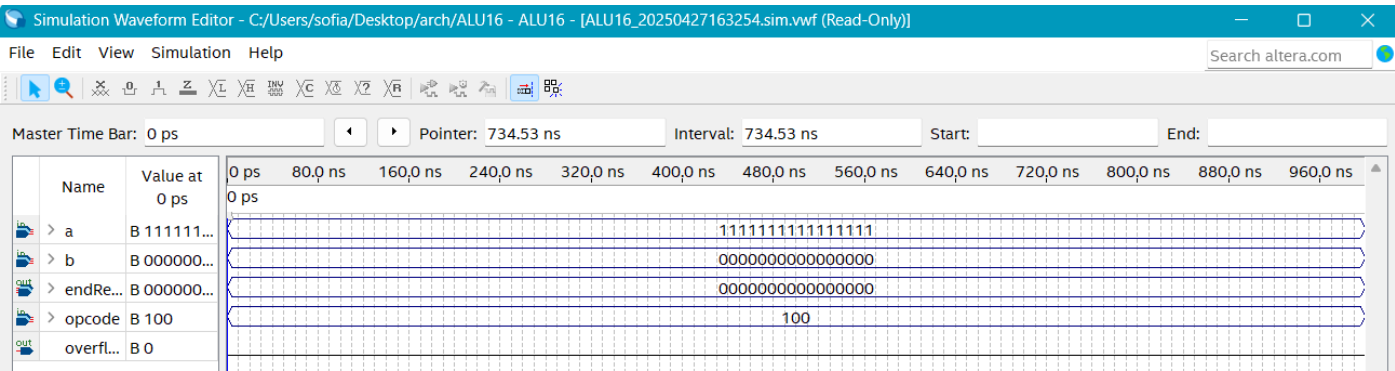
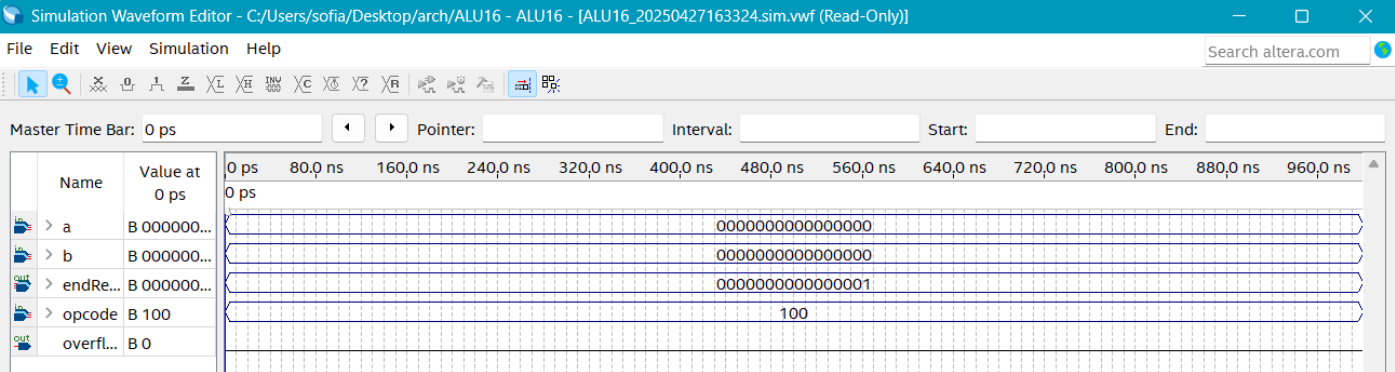
# Logical OR



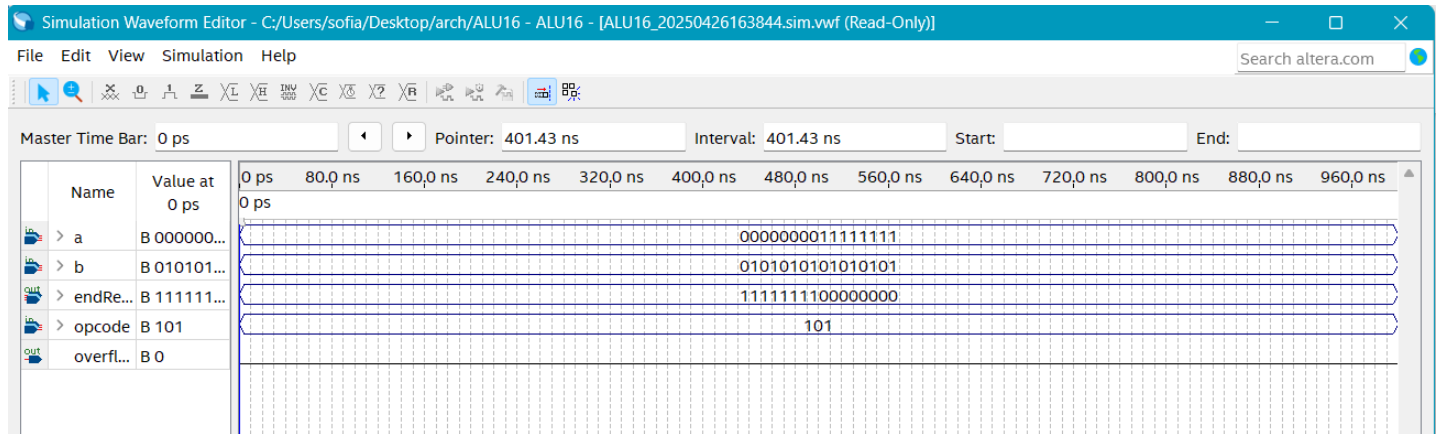
# Logical NOR



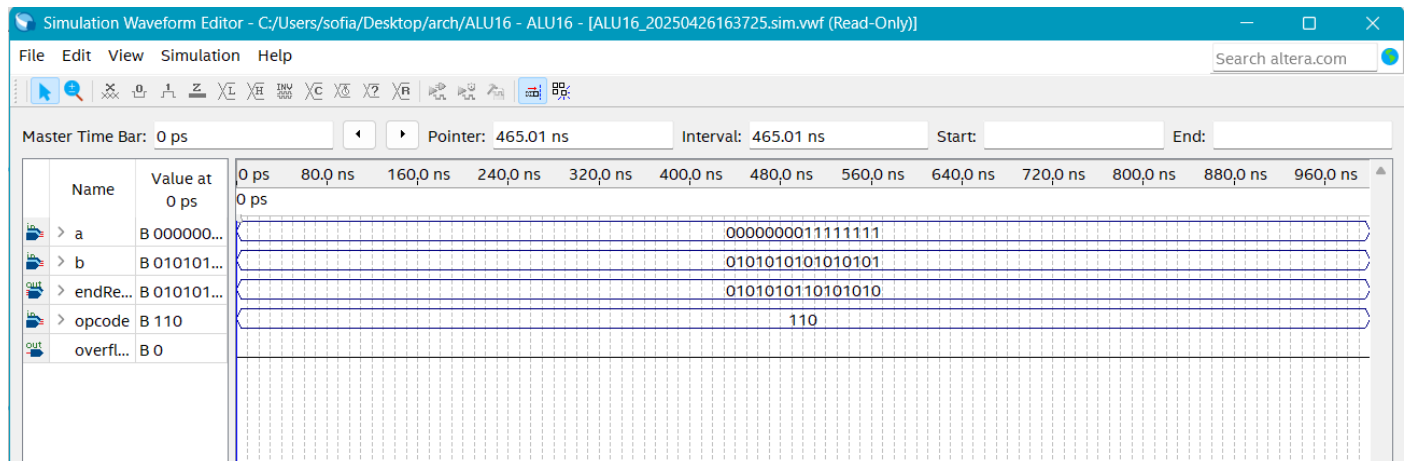
# Logical GEQ



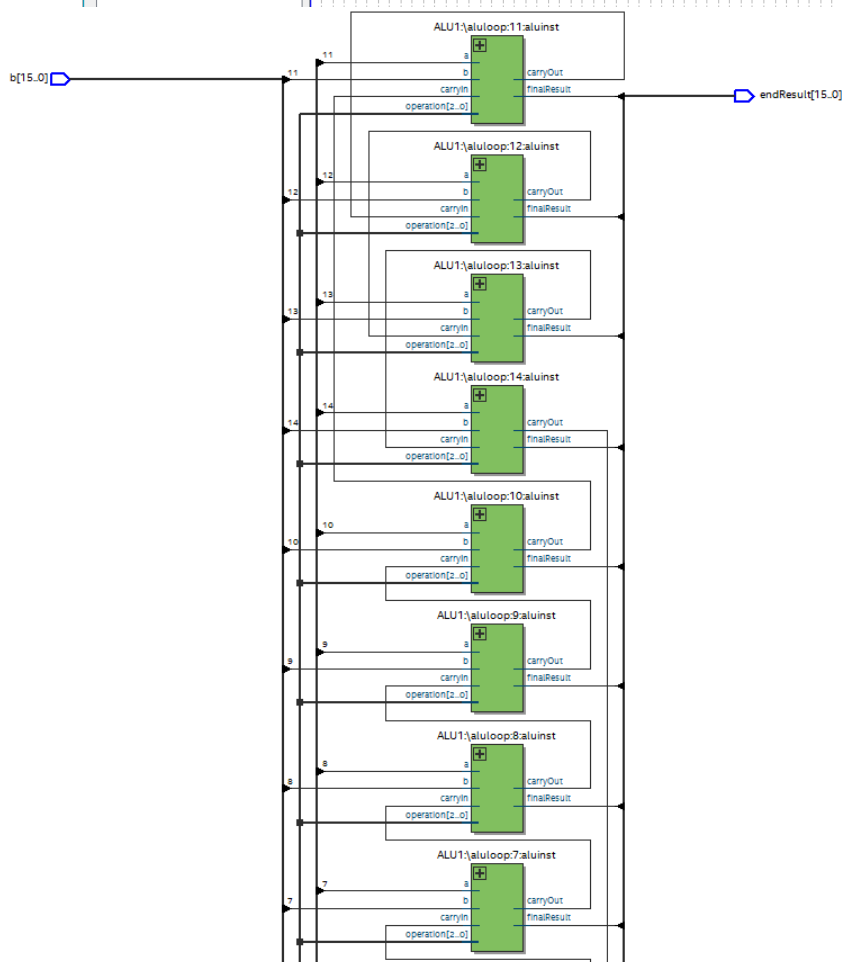
# Logical NOT



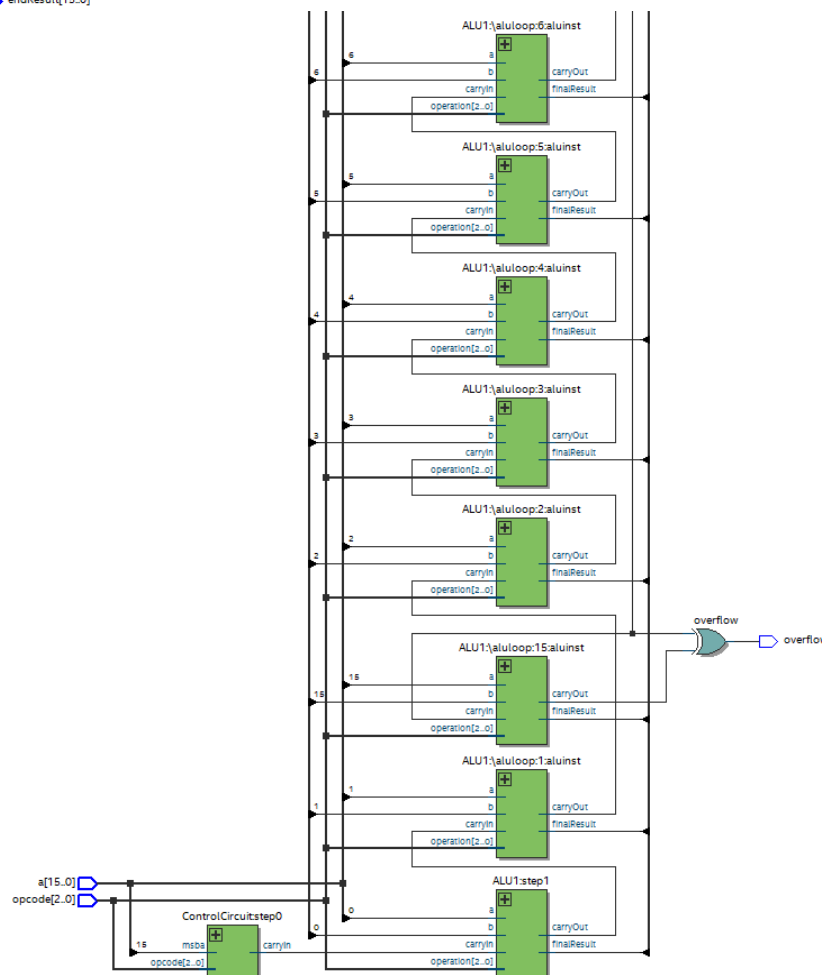
# Exclusive OR (XOR)

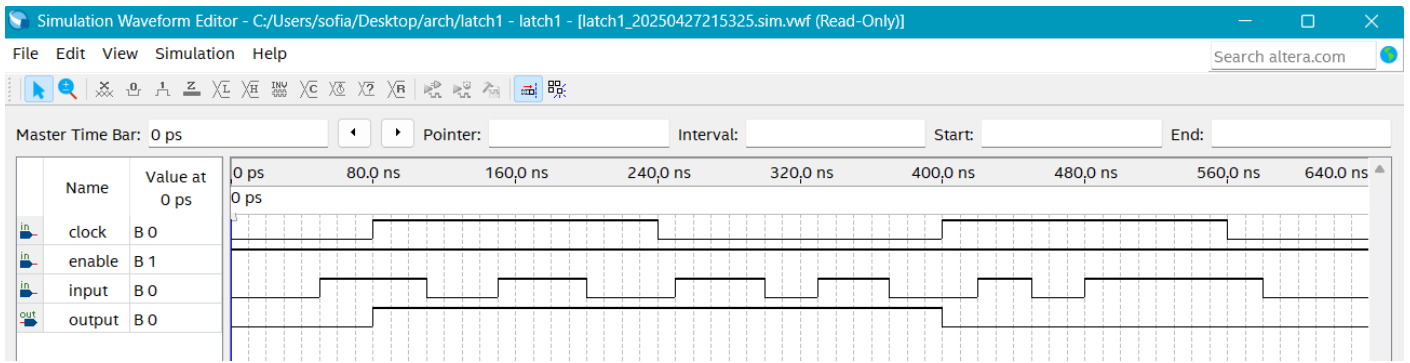


## 16-bit ALU RTL Schema

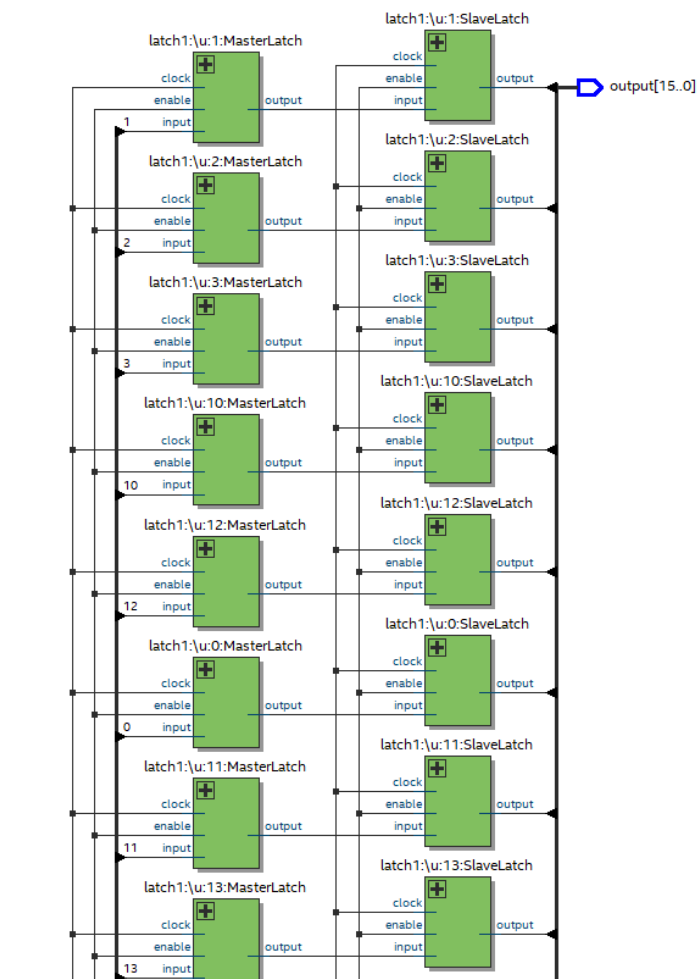
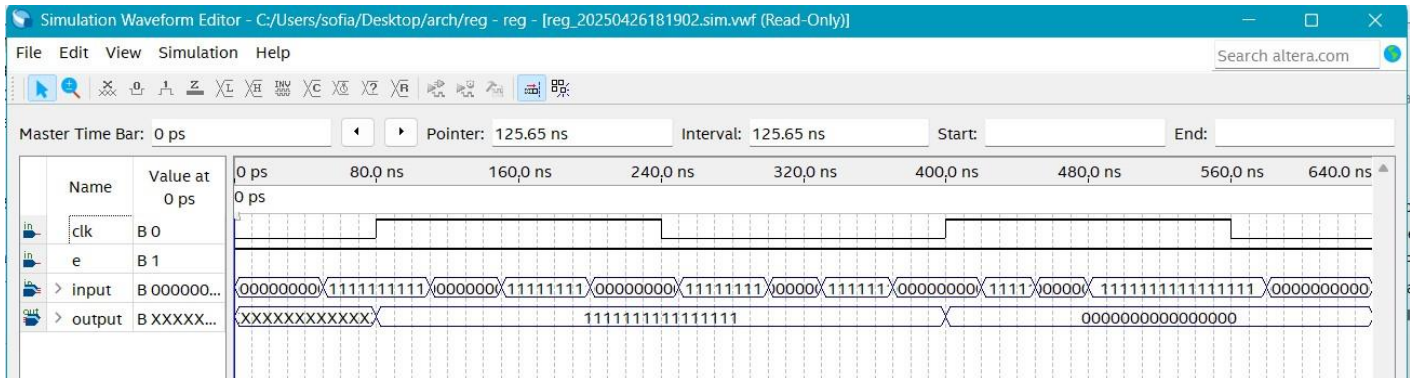


## 1-bit D-Flip-Flop

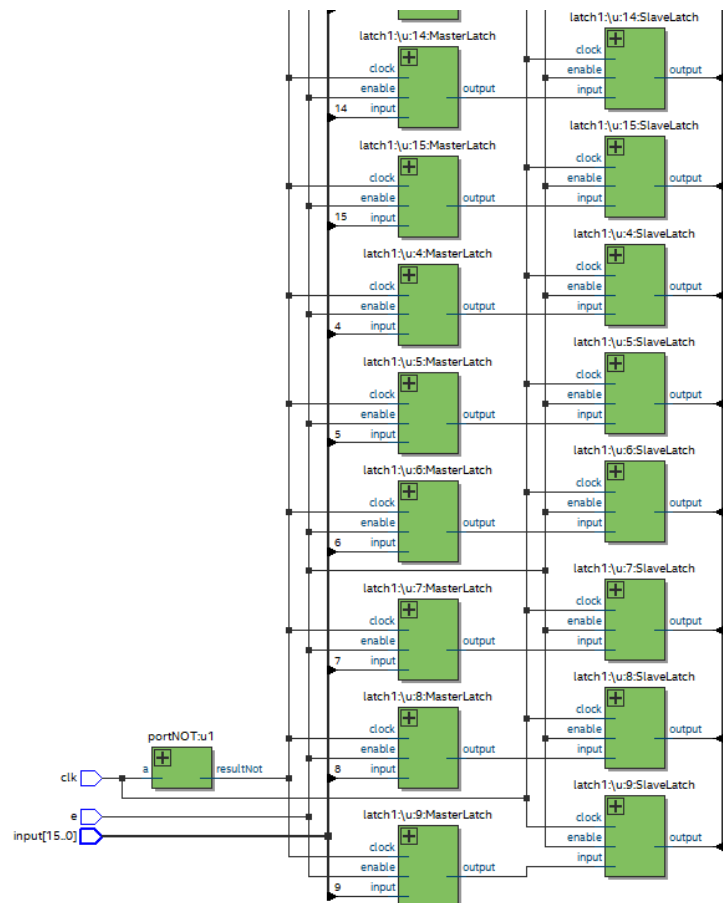




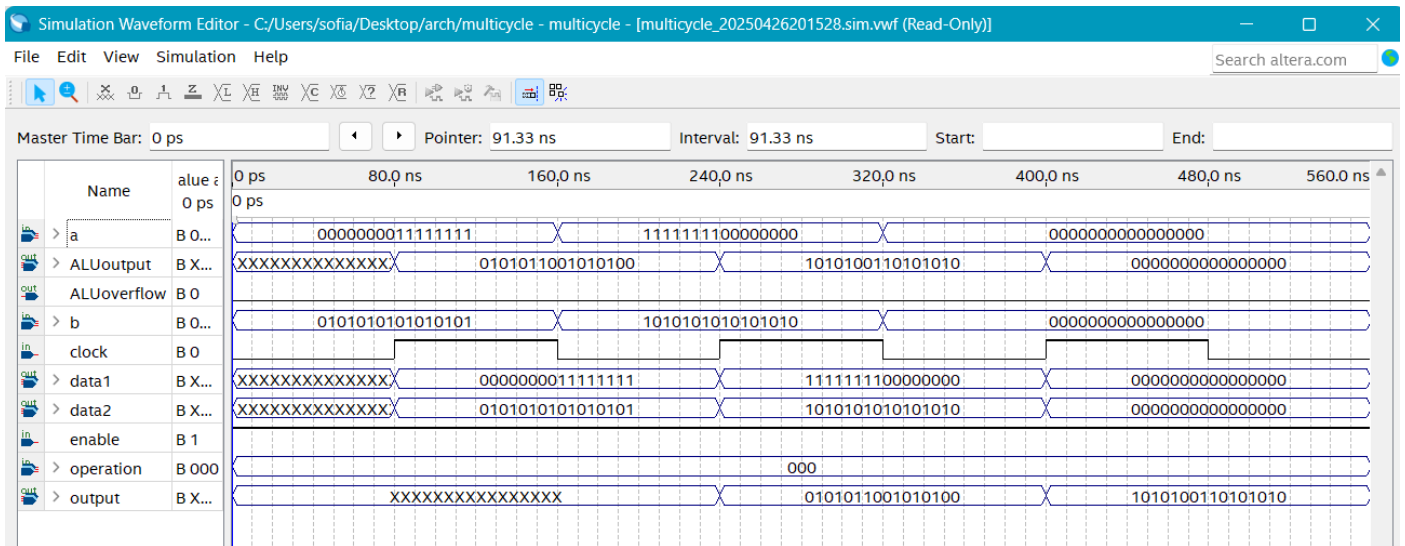
## 16-bit D-Flip-Flop



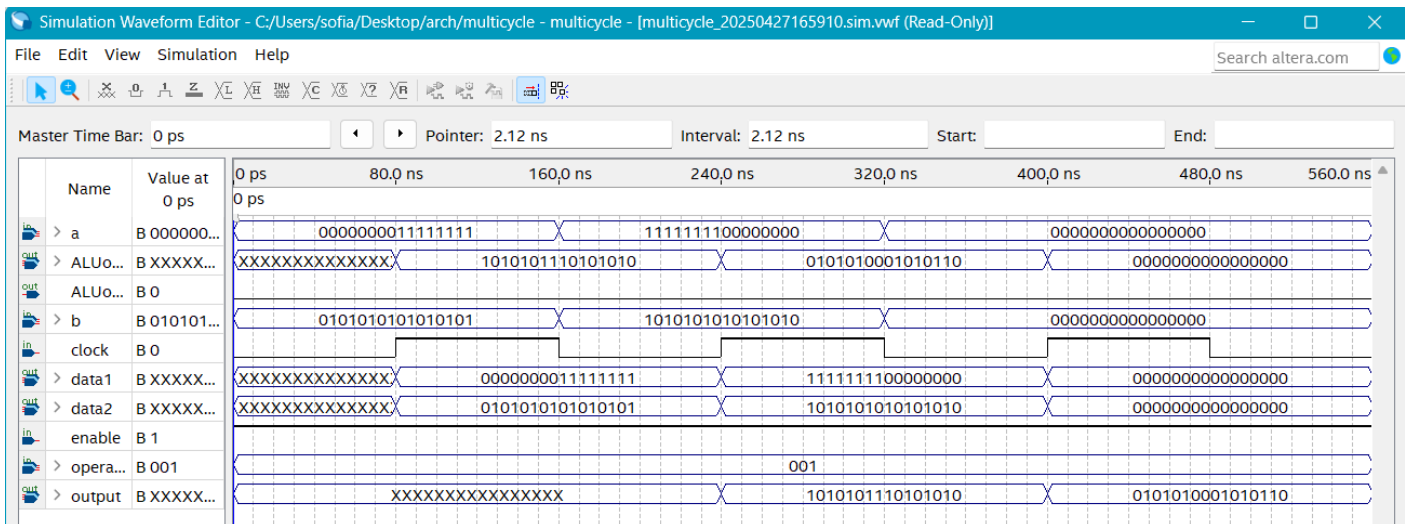
## 16-bit D-Flip-Flop RTL Schema



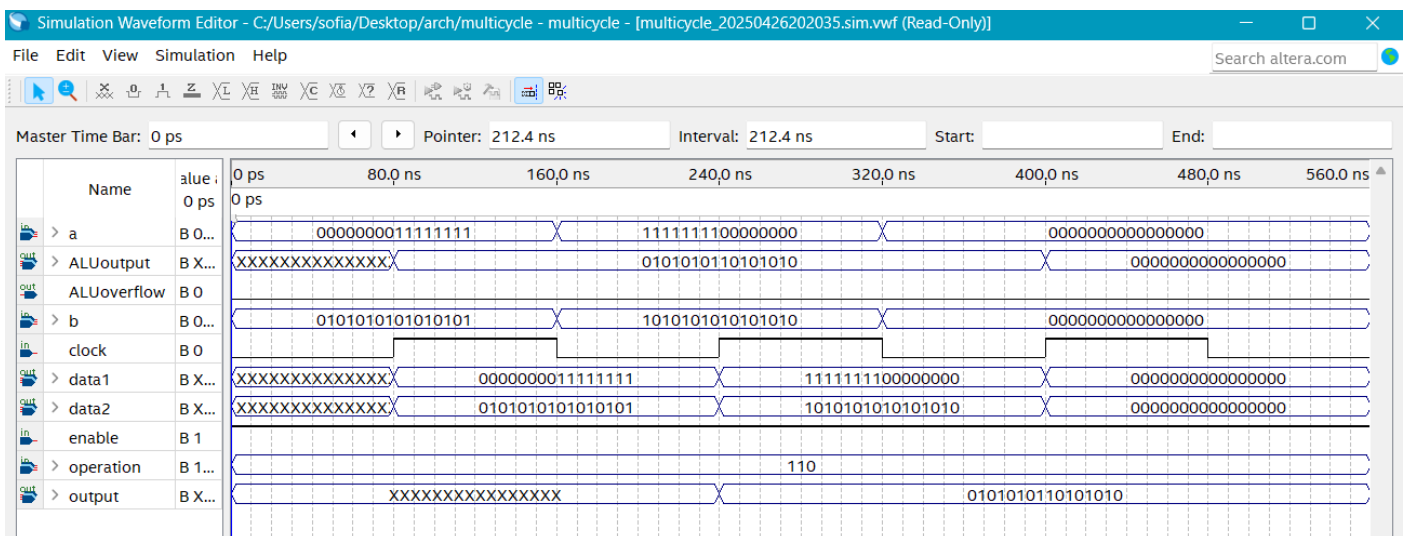
## Arithmetic Addition (ADD) - M



## Arithmetic Subtraction (SUB) - Multicycle

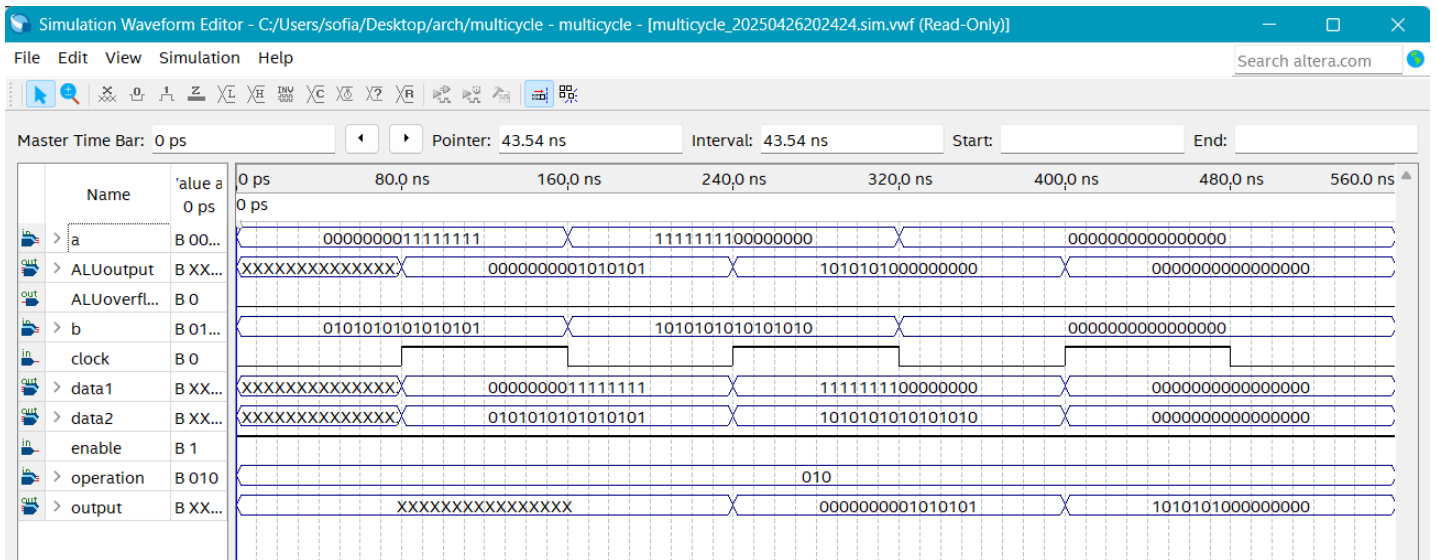


## Exclusive OR (XOR) - Multicycle

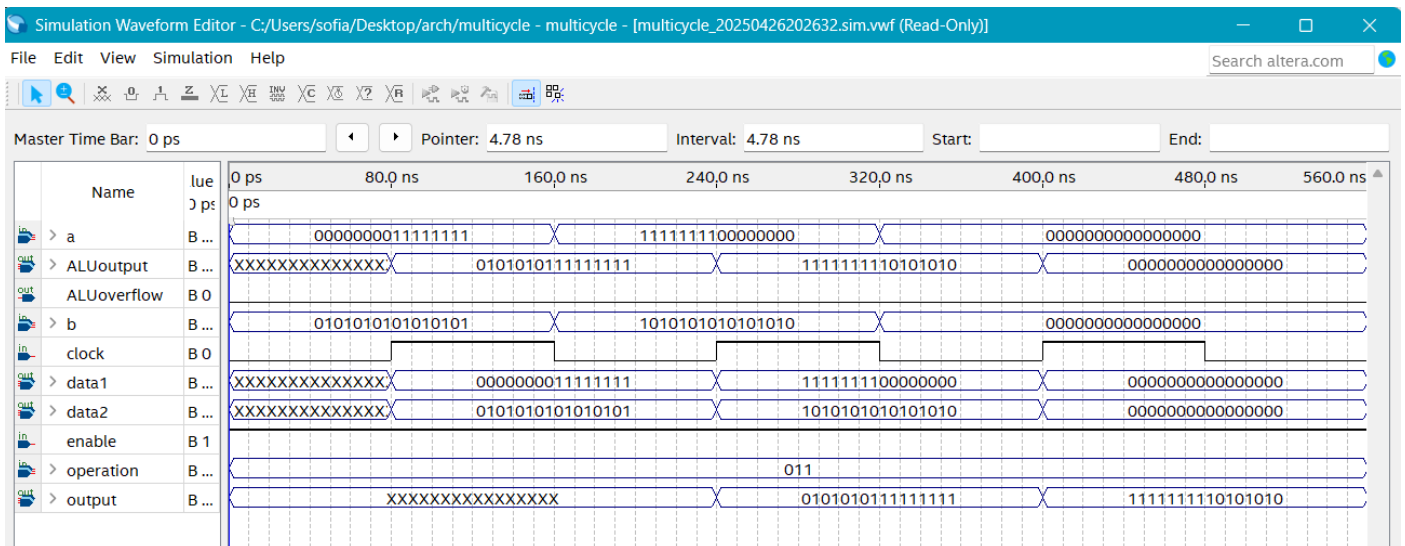


## Logical AND - Multicycle

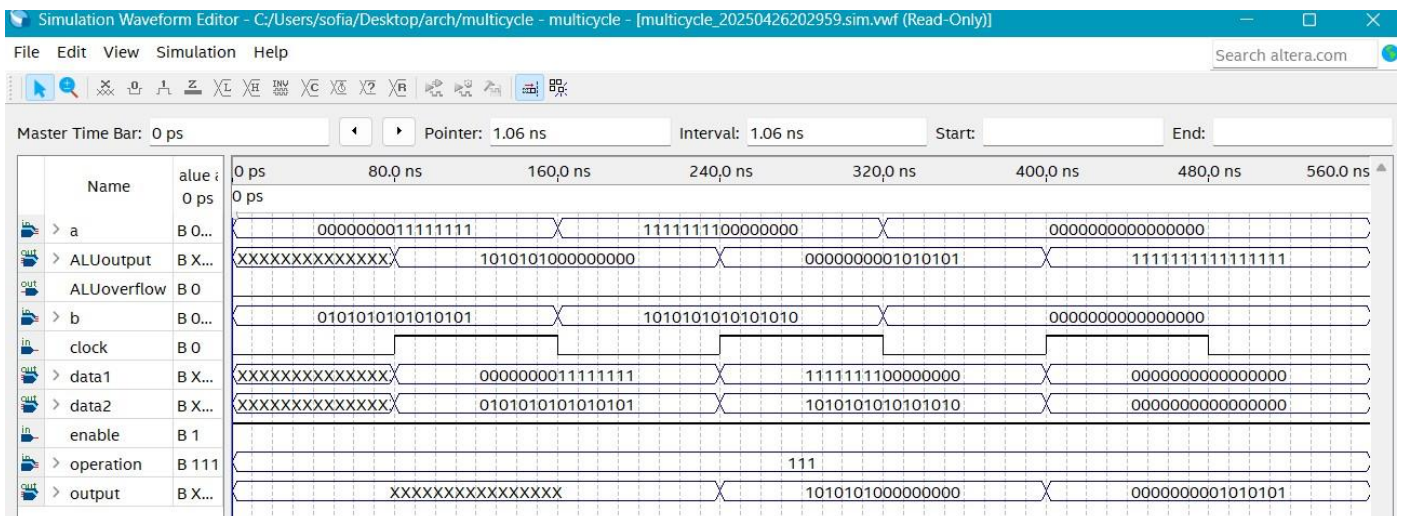




## Logical OR - Multicycle

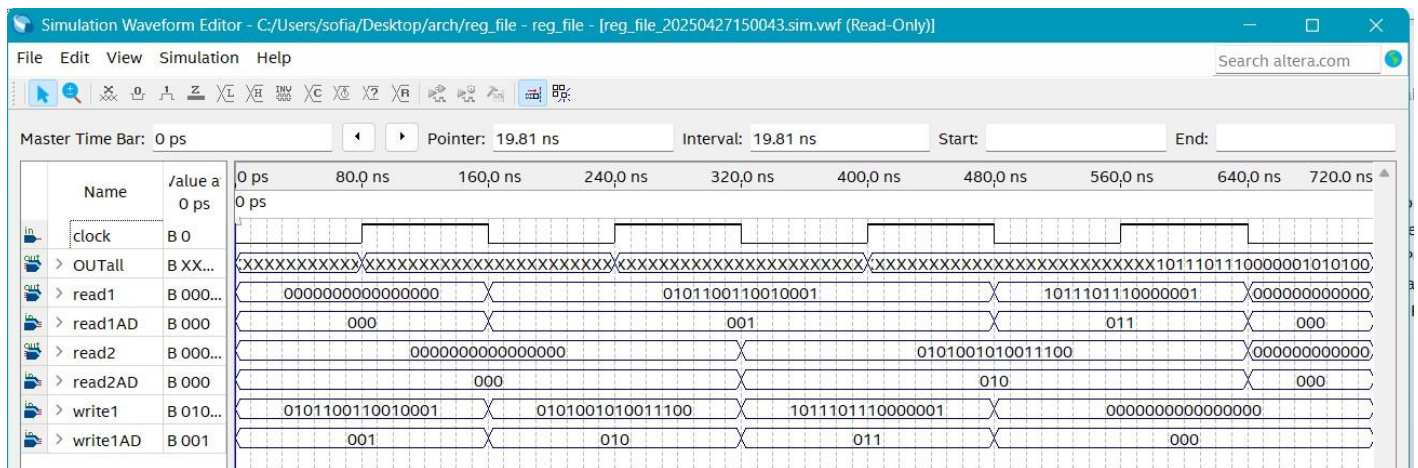


## Logical NOR - Multicycle

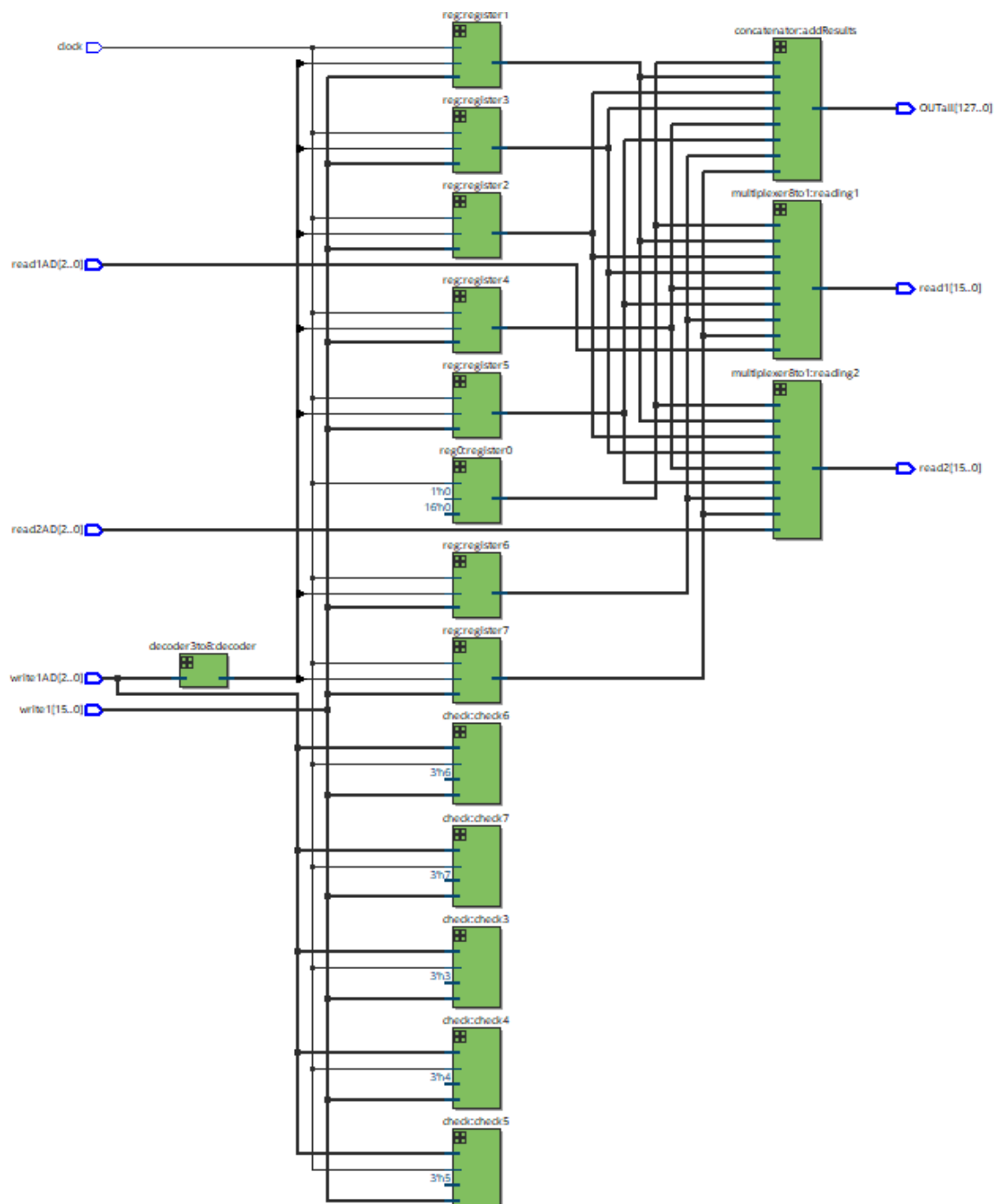


## Logical NOT - Multicycle



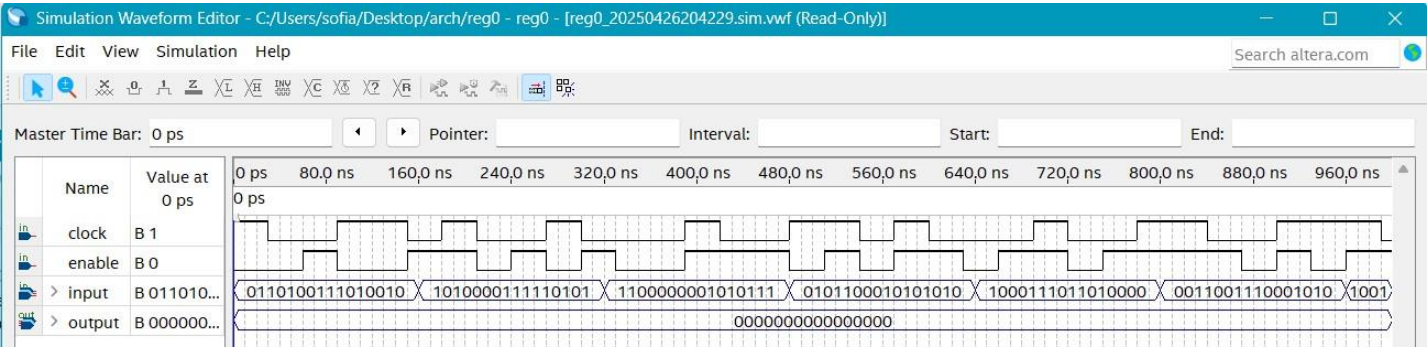


## Register File RTL Schema





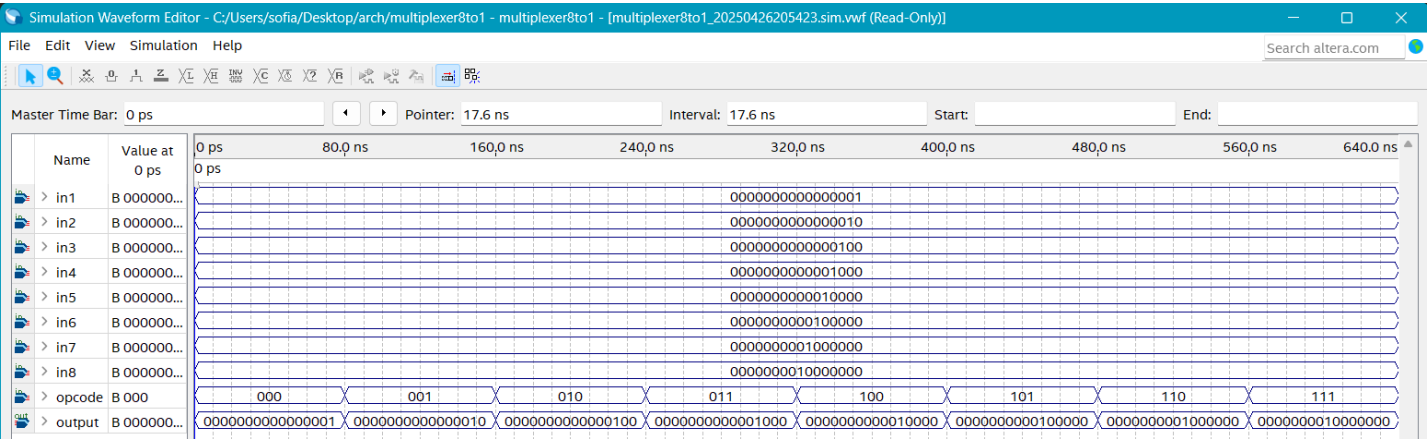
# Pseudo-Register



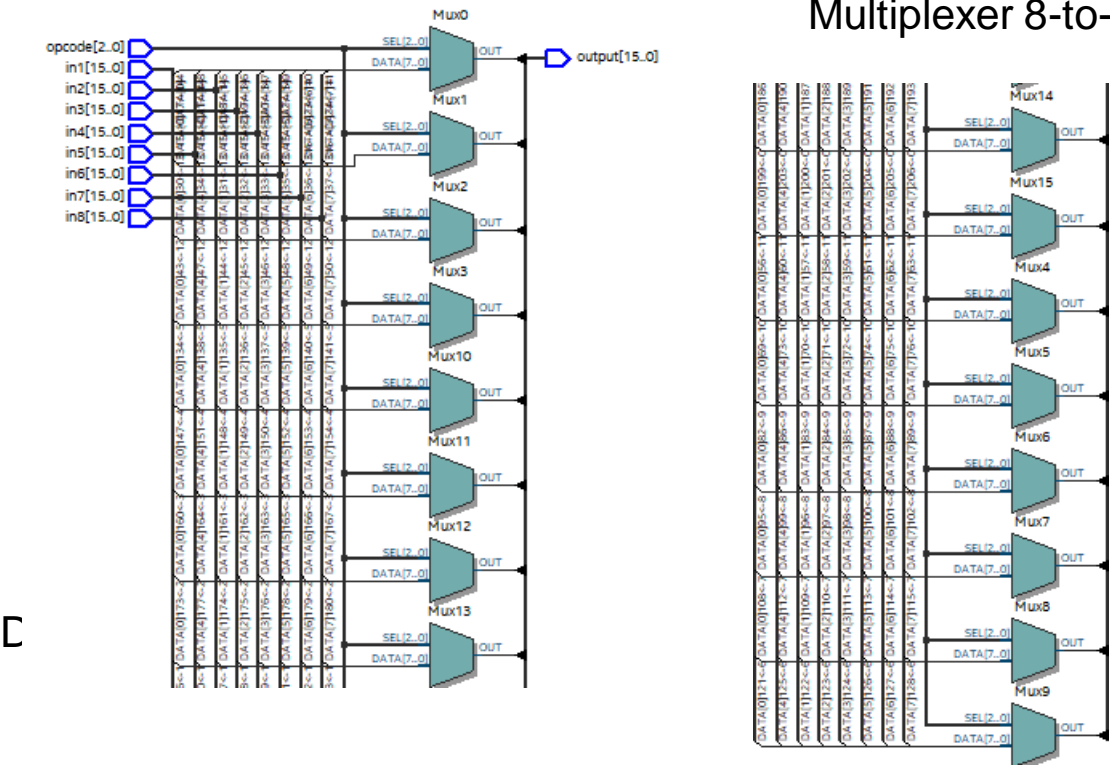
## Pseudo-register RTL Schema

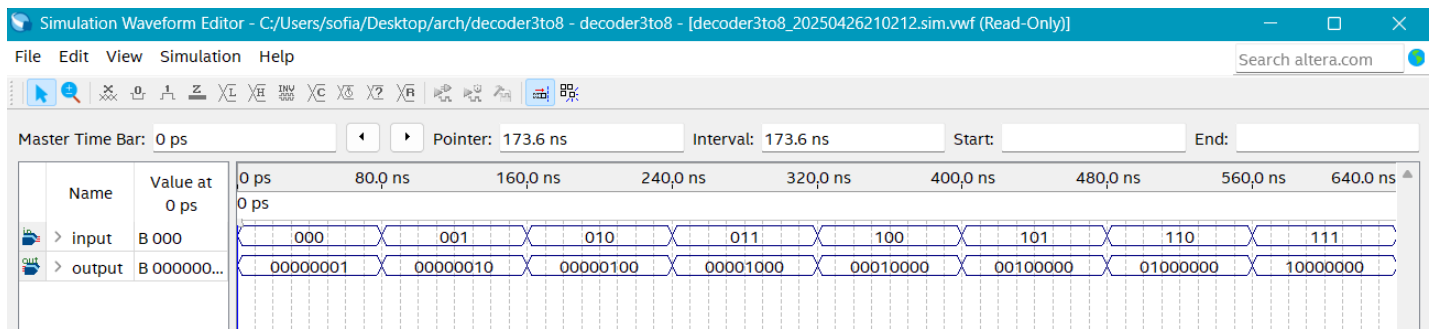


## Multiplexer 8-to-1

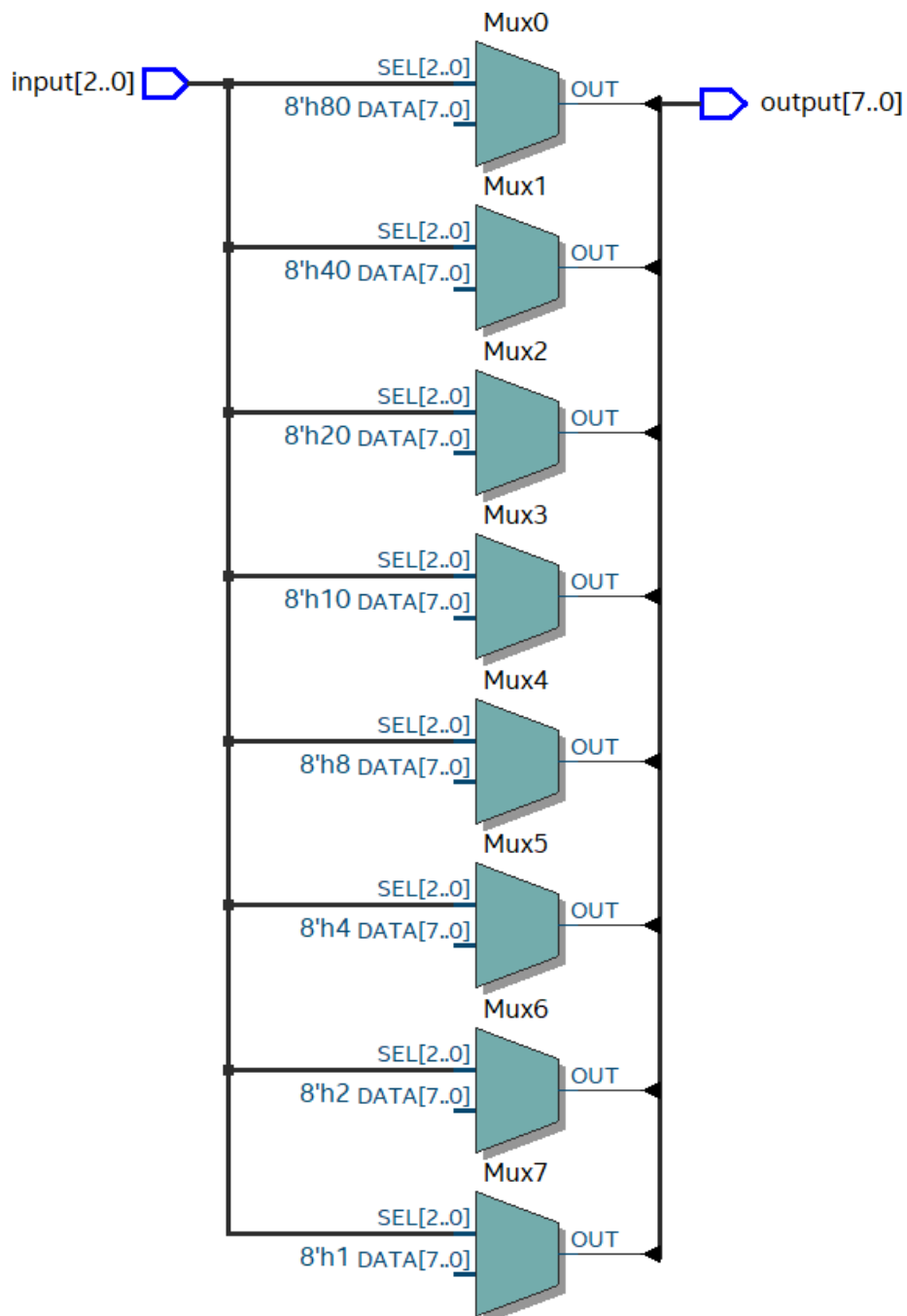


## Multiplexer 8-to-1 RTL Schema

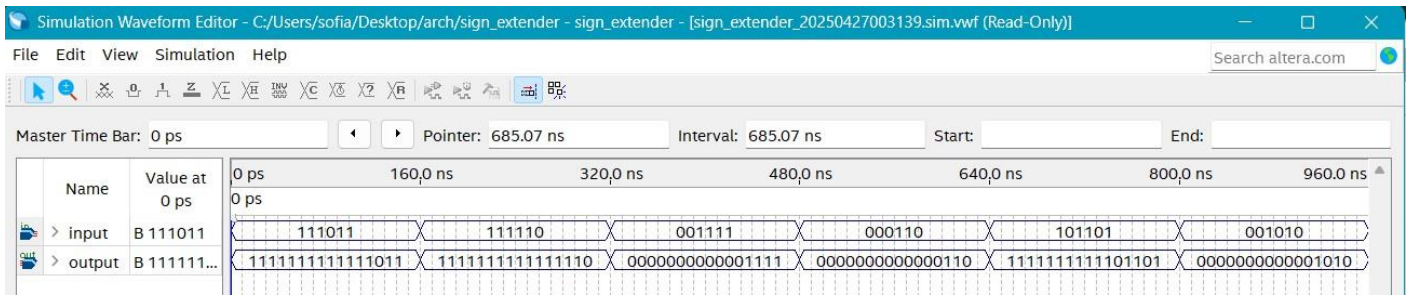




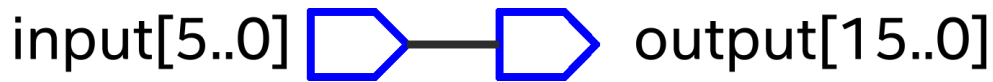
## Decoder 3-to-8 RTL Schema



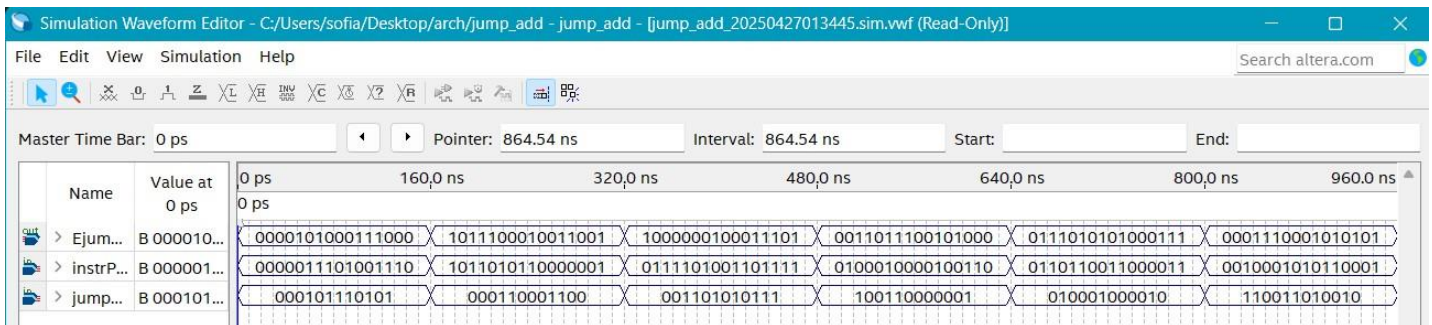
Immediate extension



## Immediate extension RTL Schema



## JumpAddress Calculation



## JumpAddress Calculation RTL Schema

