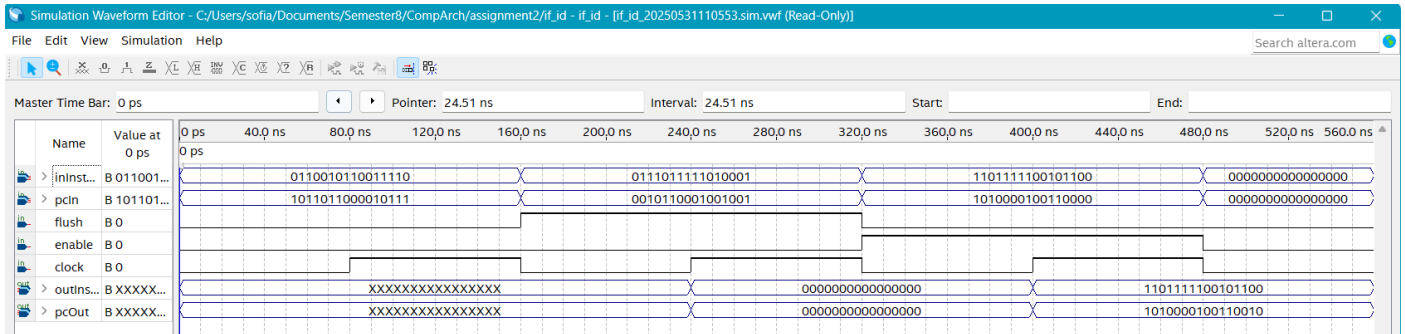


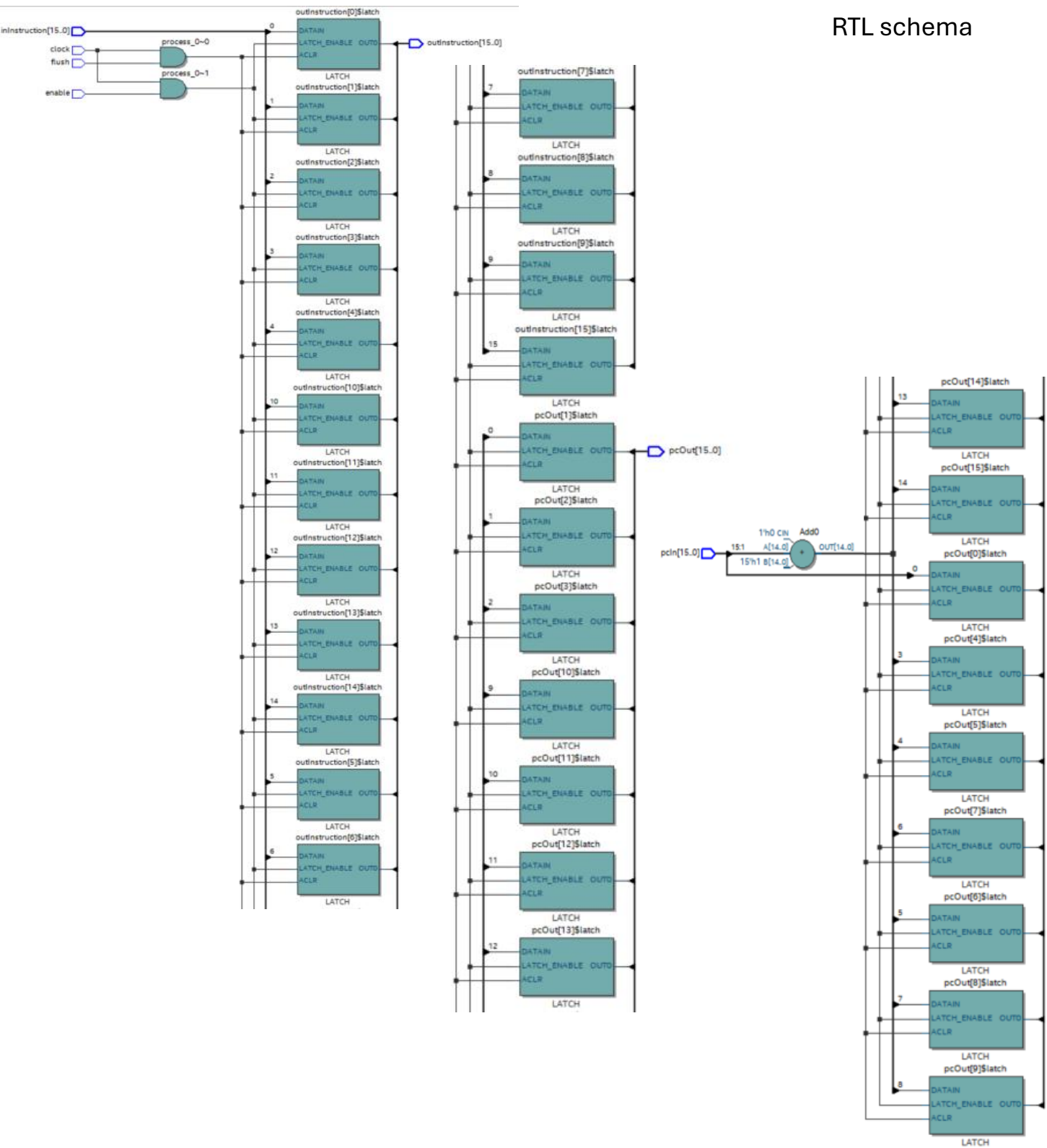
Computer Architecture: 2nd Lab Assignment

Author: Sofia-Zoi Sotiriou, p3210192

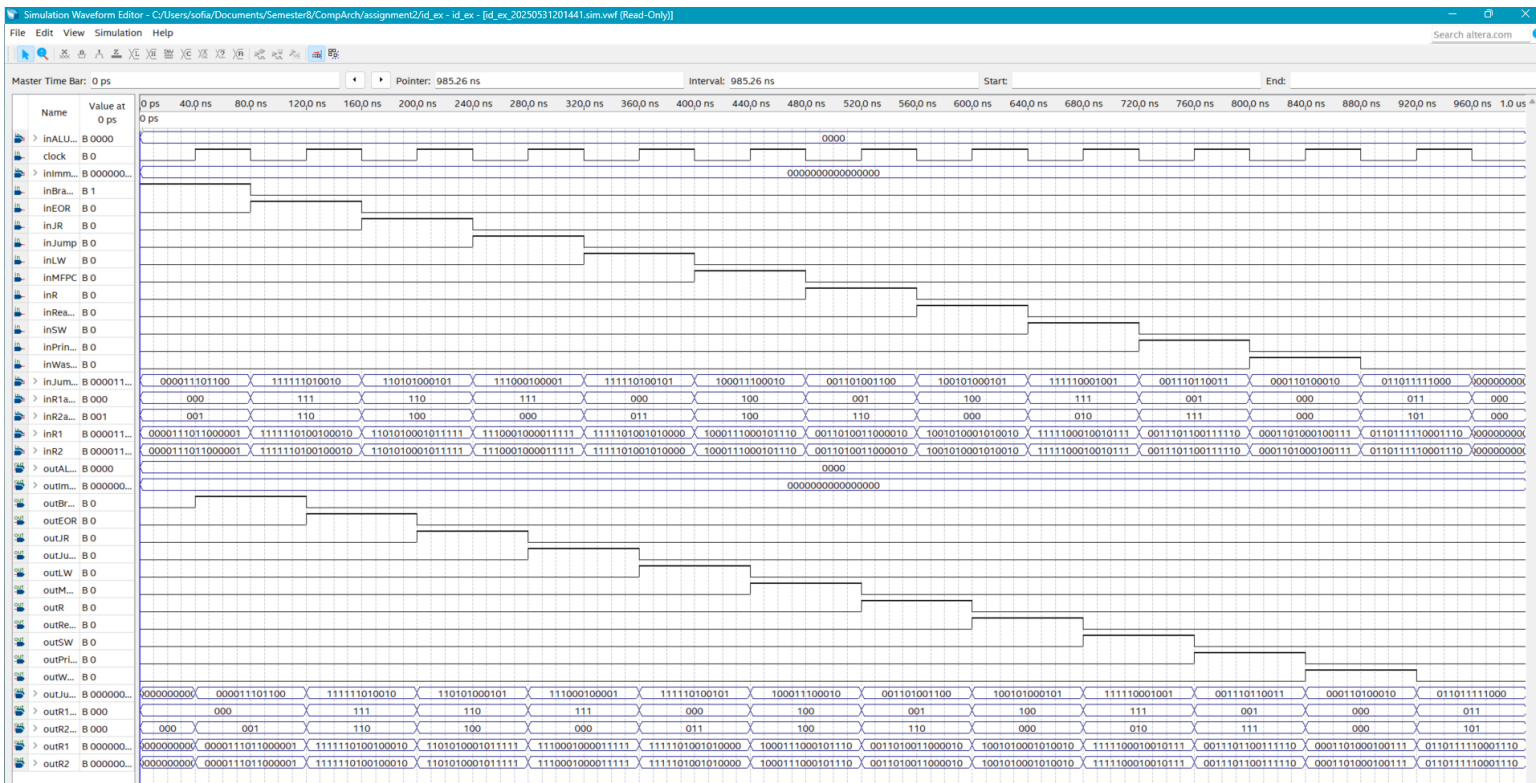
IF/ID register



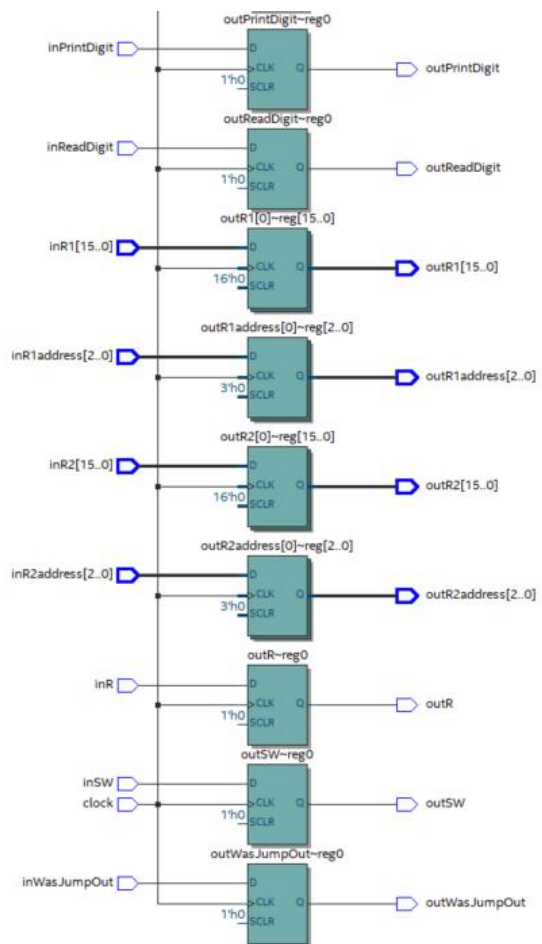
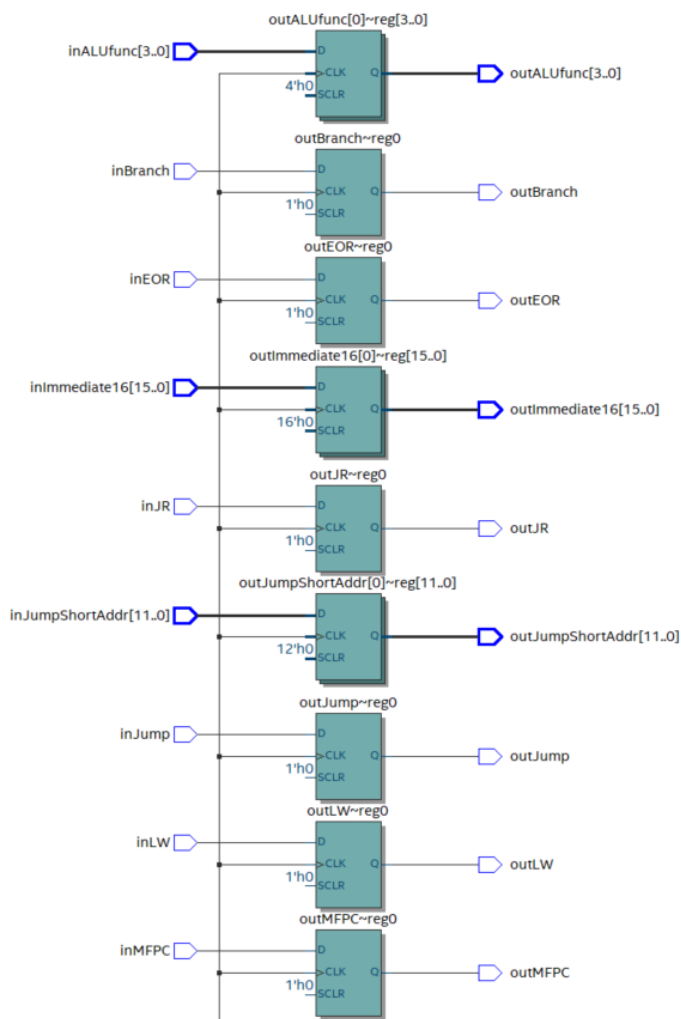
RTL schema



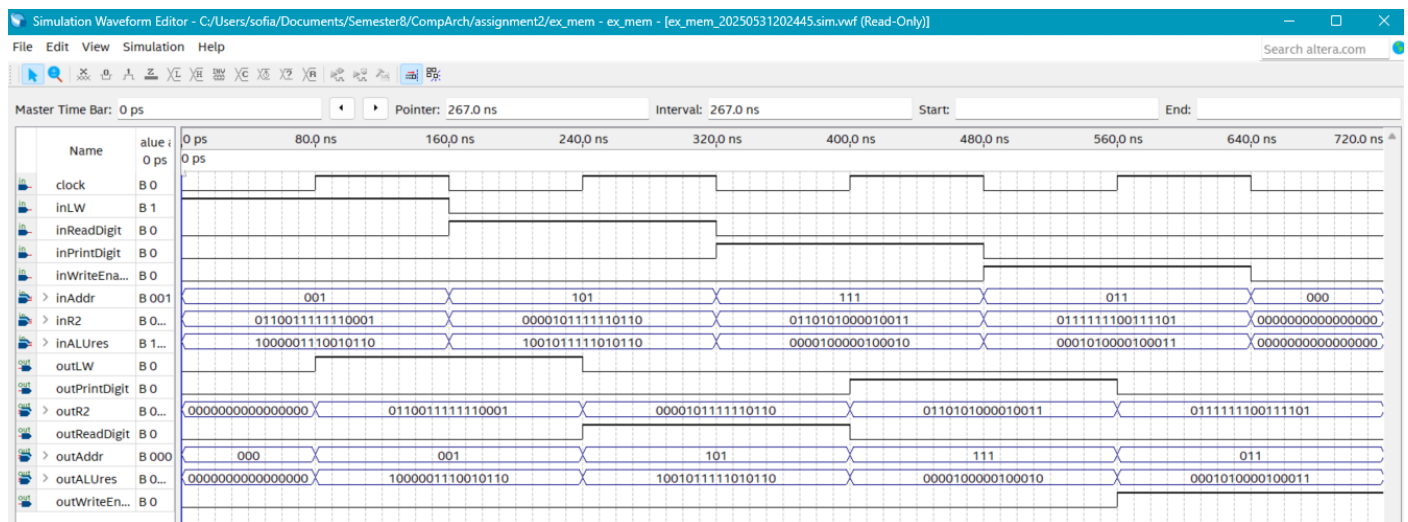
ID/EX register



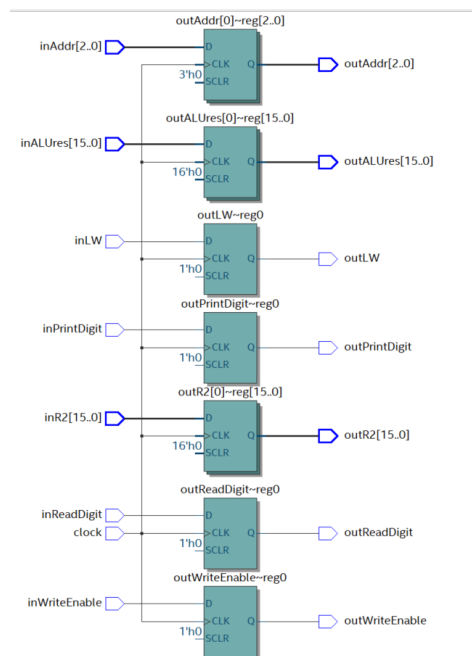
RTL schema



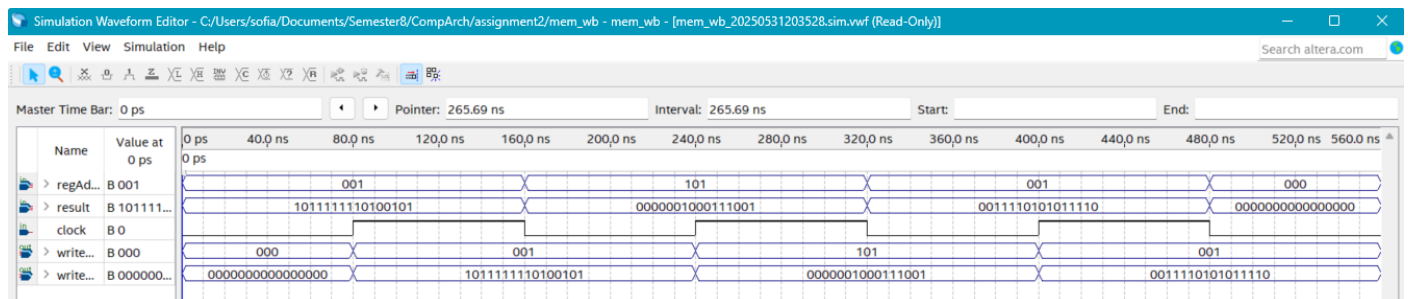
EX/MEM register



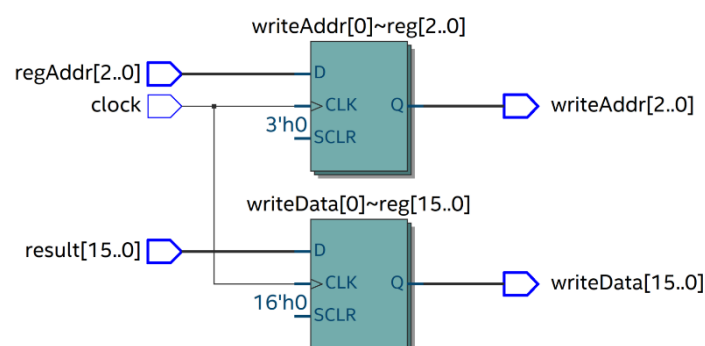
RTL schema



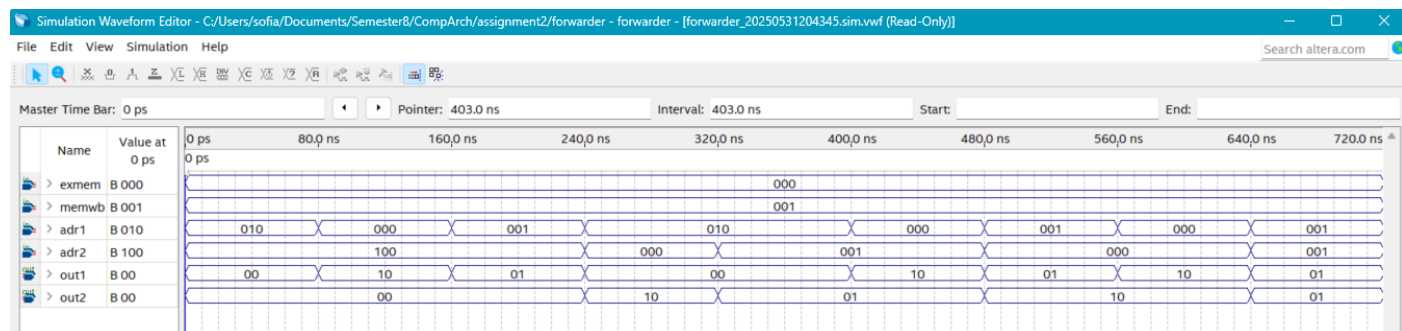
MEM/WB register



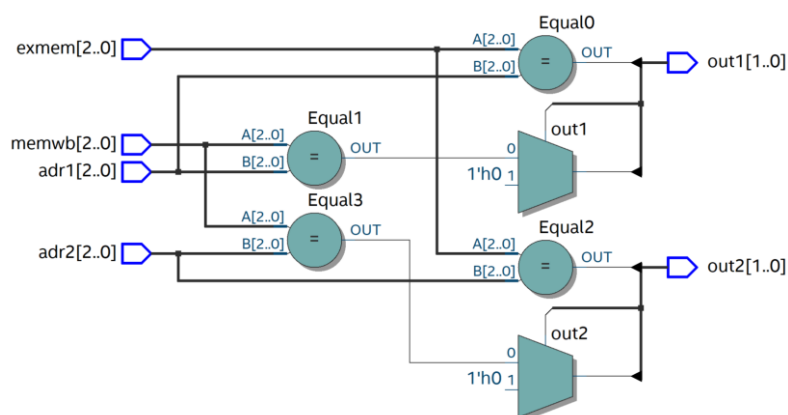
RTL schema



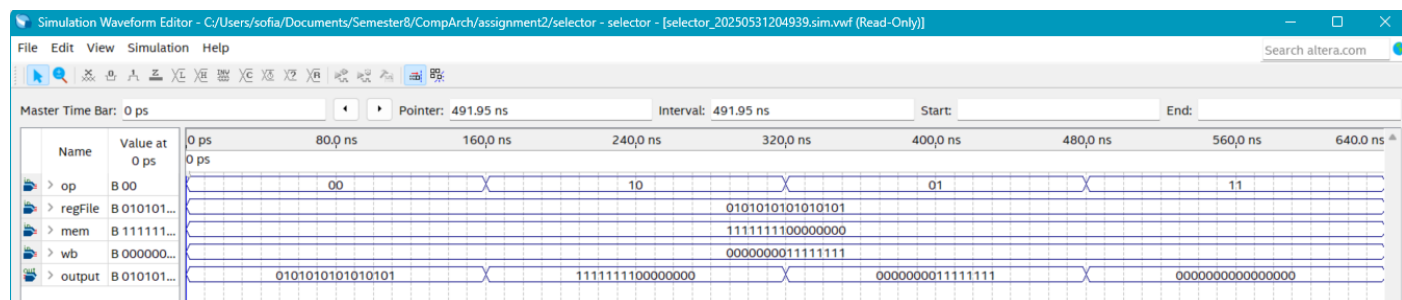
Forwarder



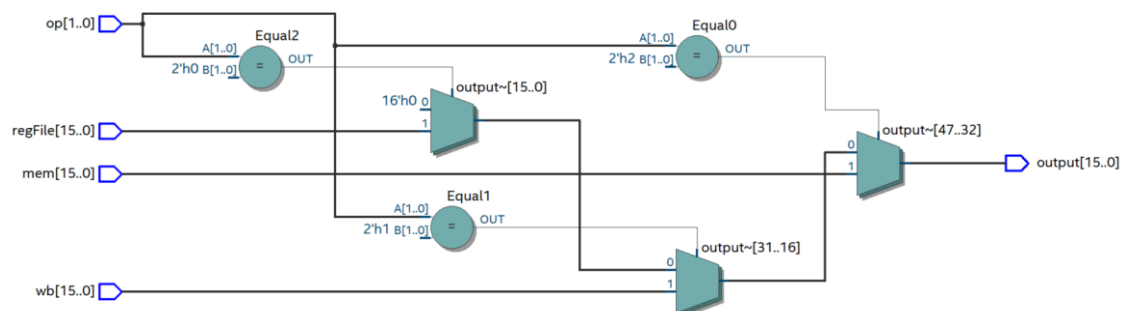
RTL schema



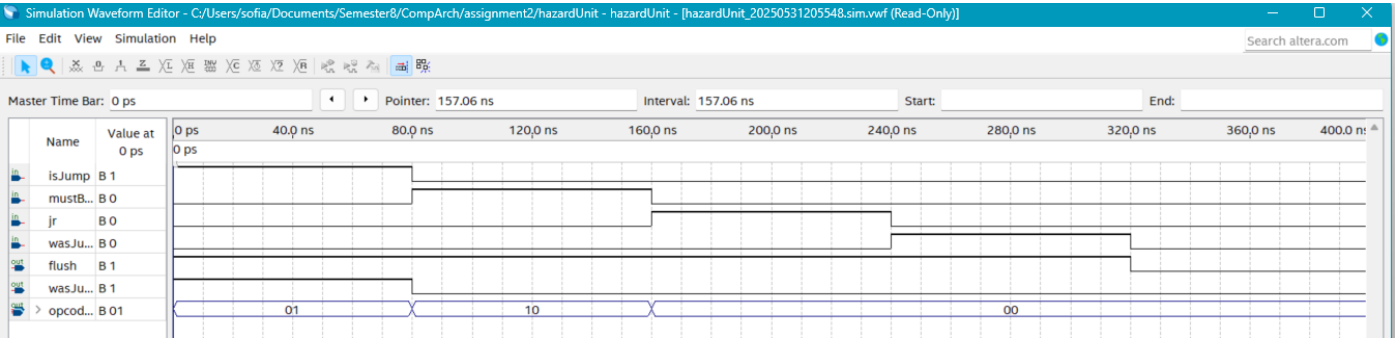
Selector (ALU-in multiplexer)



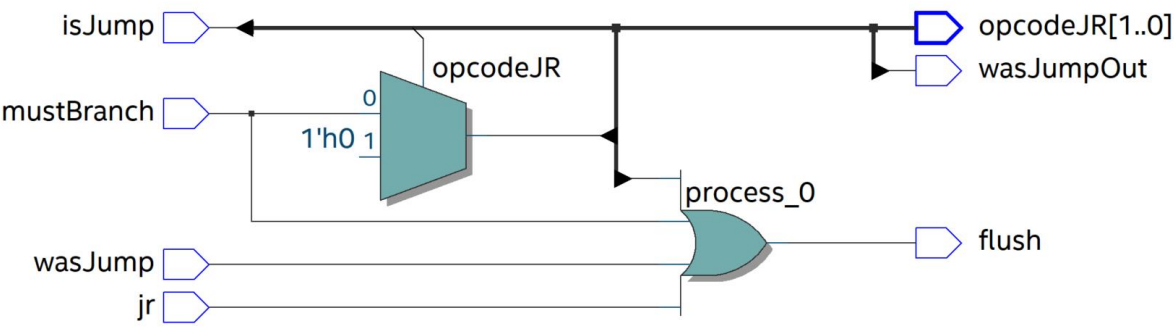
RTL schema



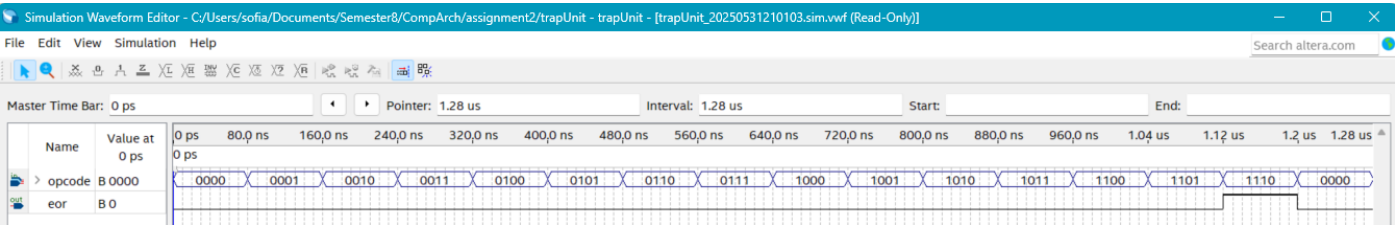
Hazard unit



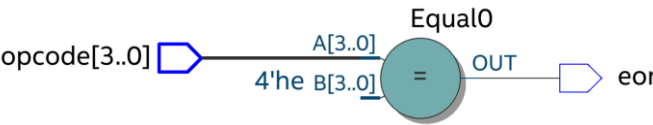
RTL schema



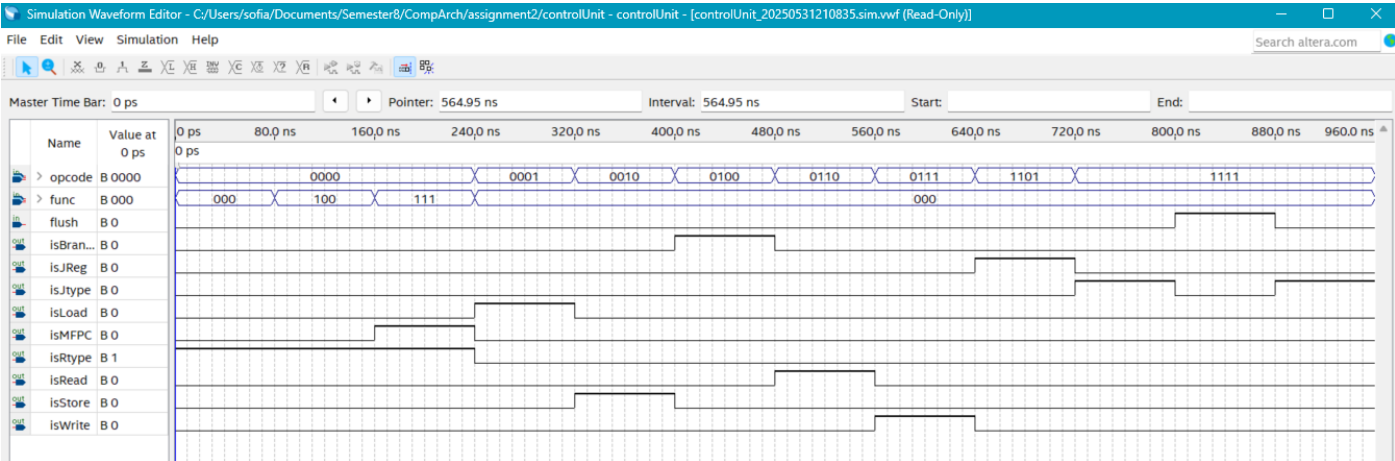
Trap unit



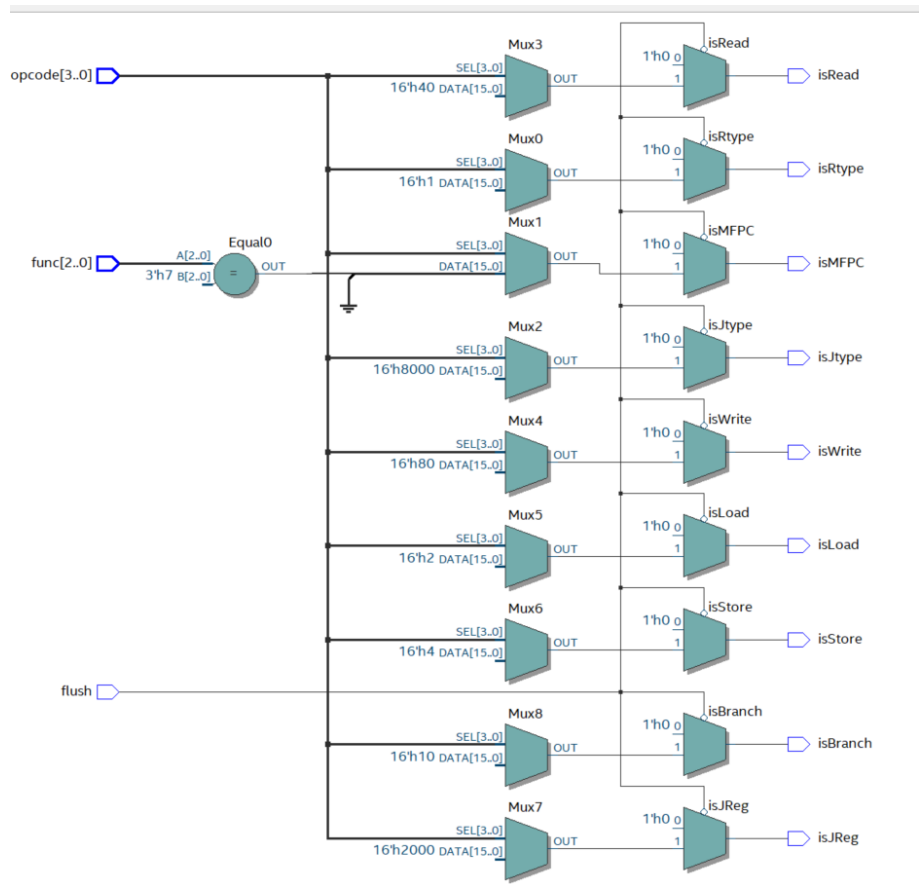
RTL schema



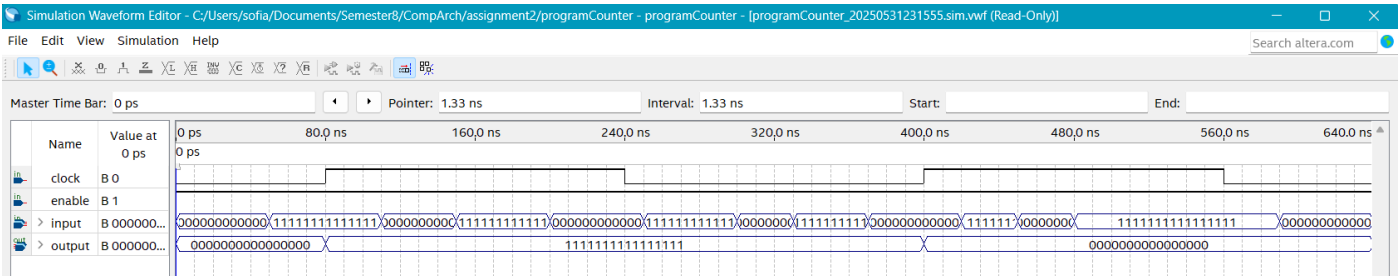
Control Unit



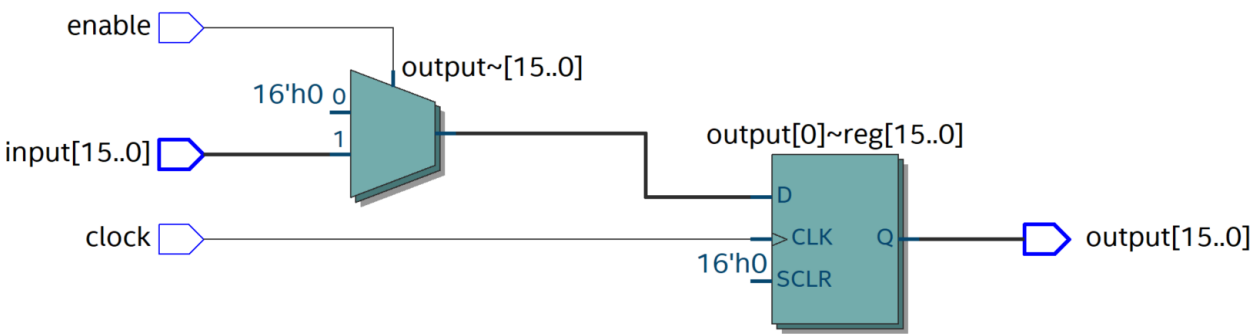
RTL schema



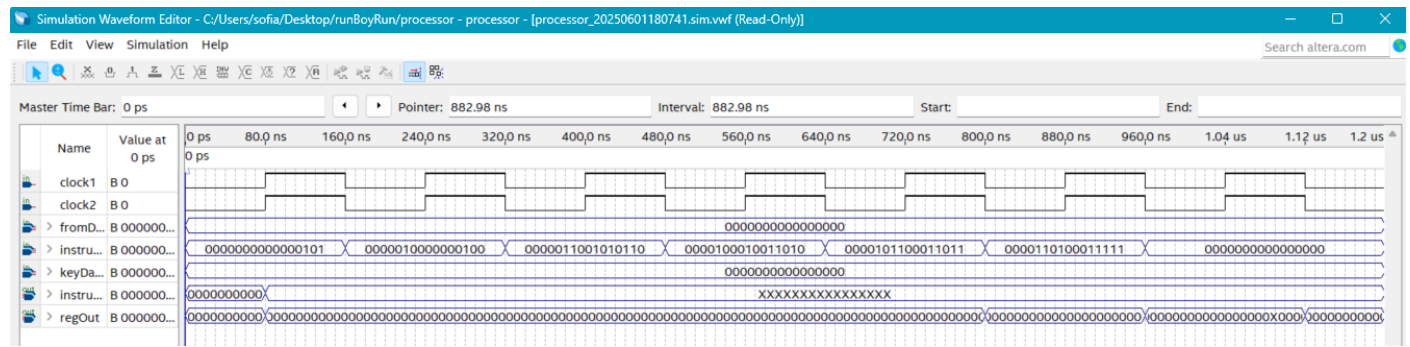
ProgramCounter



RTL Schema



Processor



RTL Schema

