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Problem Statement: A 4-bit code converter for even parity converts the 4-bit input to 5-bit output so that even parity is ensured

Theory:

Parity bit comes in hand to check whether a unit of binary data has any error during the transmission of binary data. The message containing the binary data with the parity bit gets transmitted from the transmitter node to the receiver node.

Even parity refers to a parity checking mode in asynchronous communication systems that indicates whether a unit of binary data is an even number or odd. The parity bit is set to 1 if the number of 1s in the binary number is an odd number. The parity bit is set to 0 if the number of 1s in the binary number is an even number.

There are two types of parity bits, even and odd.
If the original data is 1010, the parity bit will be 0 so that the number of 1's in the data remains even.
Parity bit sequence matters significantly since any wrong bit can lead to a misinterpreted output.

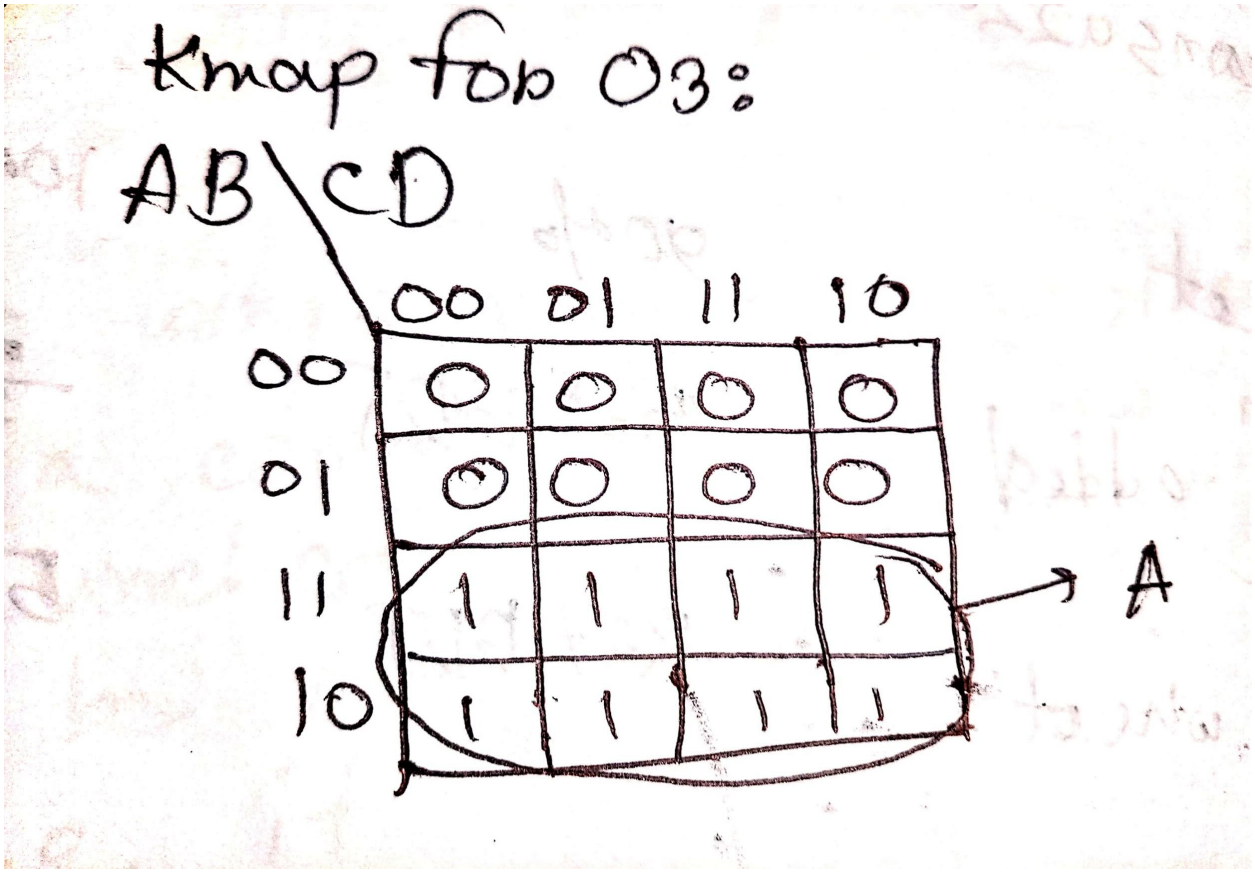
Truth Table:

Below the input combinations are given as A, B, C, D. A is the MSB and D is the LSB. and outputs as O3, O2, O1, O0. O3 is the MSB and O0 is the LSB. P indicates the parity bit.

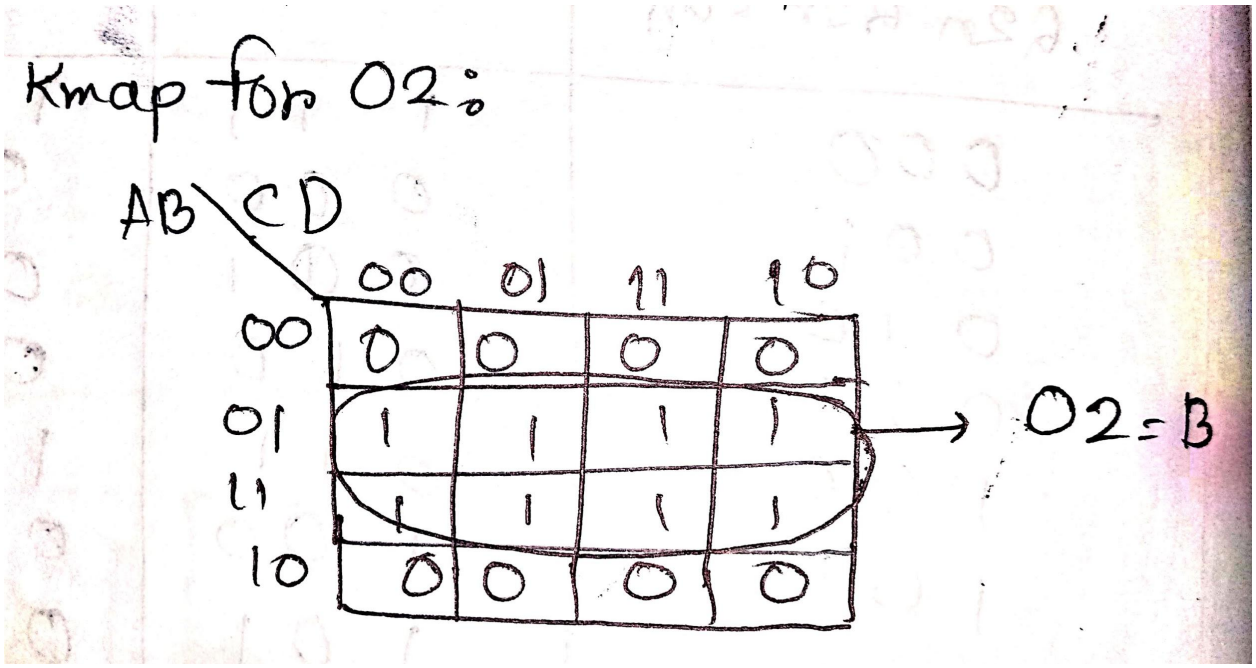
A	B	C	D	O3	O2	O1	O0	P
0	0	0	0	0	0	0	0	0
0	0	0	1	0	0	0	1	1
0	0	1	0	0	0	1	0	1
0	0	1	1	0	0	1	1	0

0	1	0	0	0	1	0	0	1
0	1	0	1	0	1	0	1	0
0	1	1	0	0	1	1	0	0
0	1	1	1	0	1	1	1	1
1	0	0	0	1	0	0	0	1
1	0	0	1	1	0	0	1	0
1	0	1	0	1	0	1	0	0
1	0	1	1	1	0	1	1	1
1	1	0	0	1	1	0	0	0
1	1	0	1	1	1	0	1	1
1	1	1	0	1	1	1	0	1
1	1	1	1	1	1	1	1	0

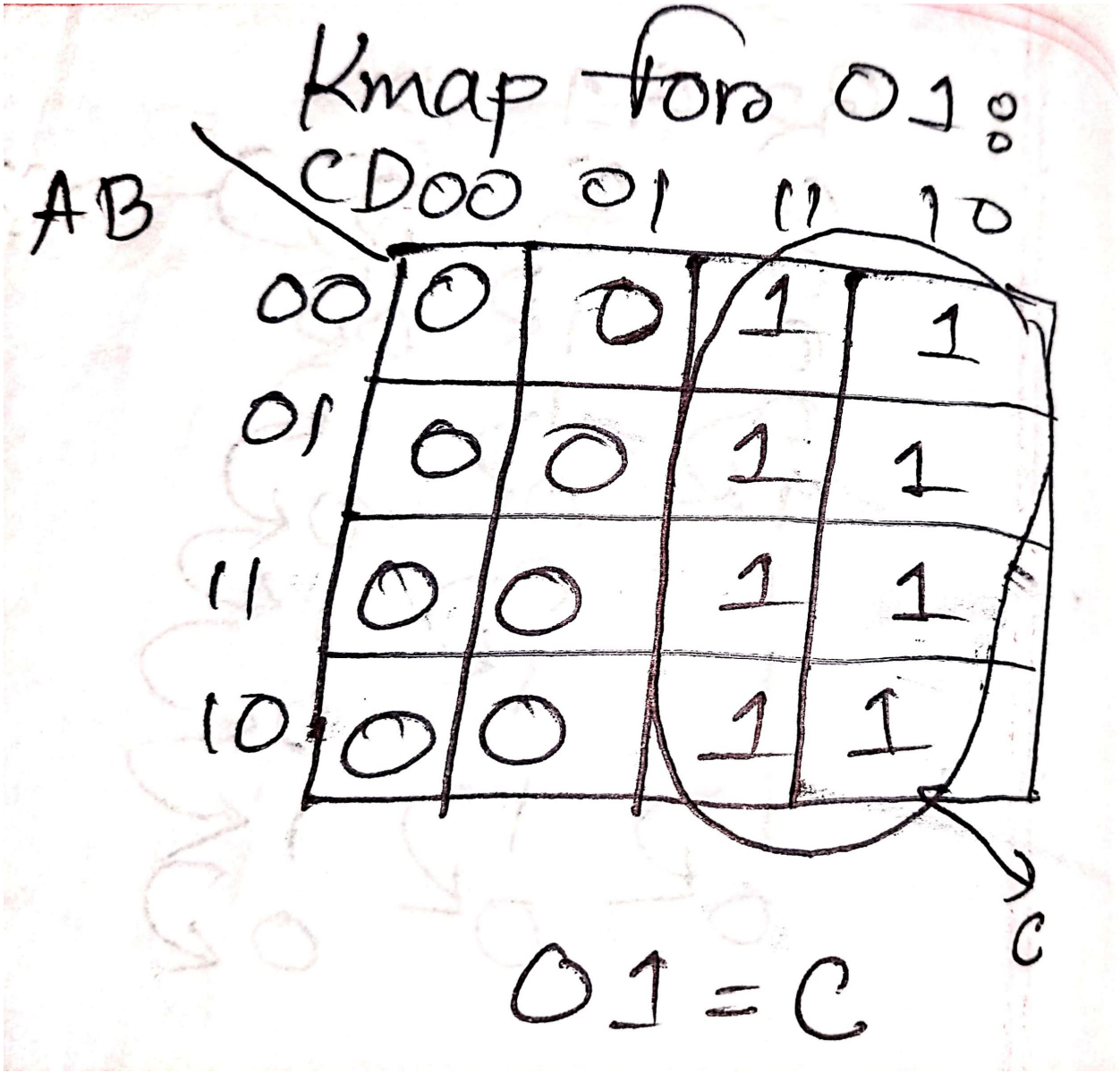
K map:



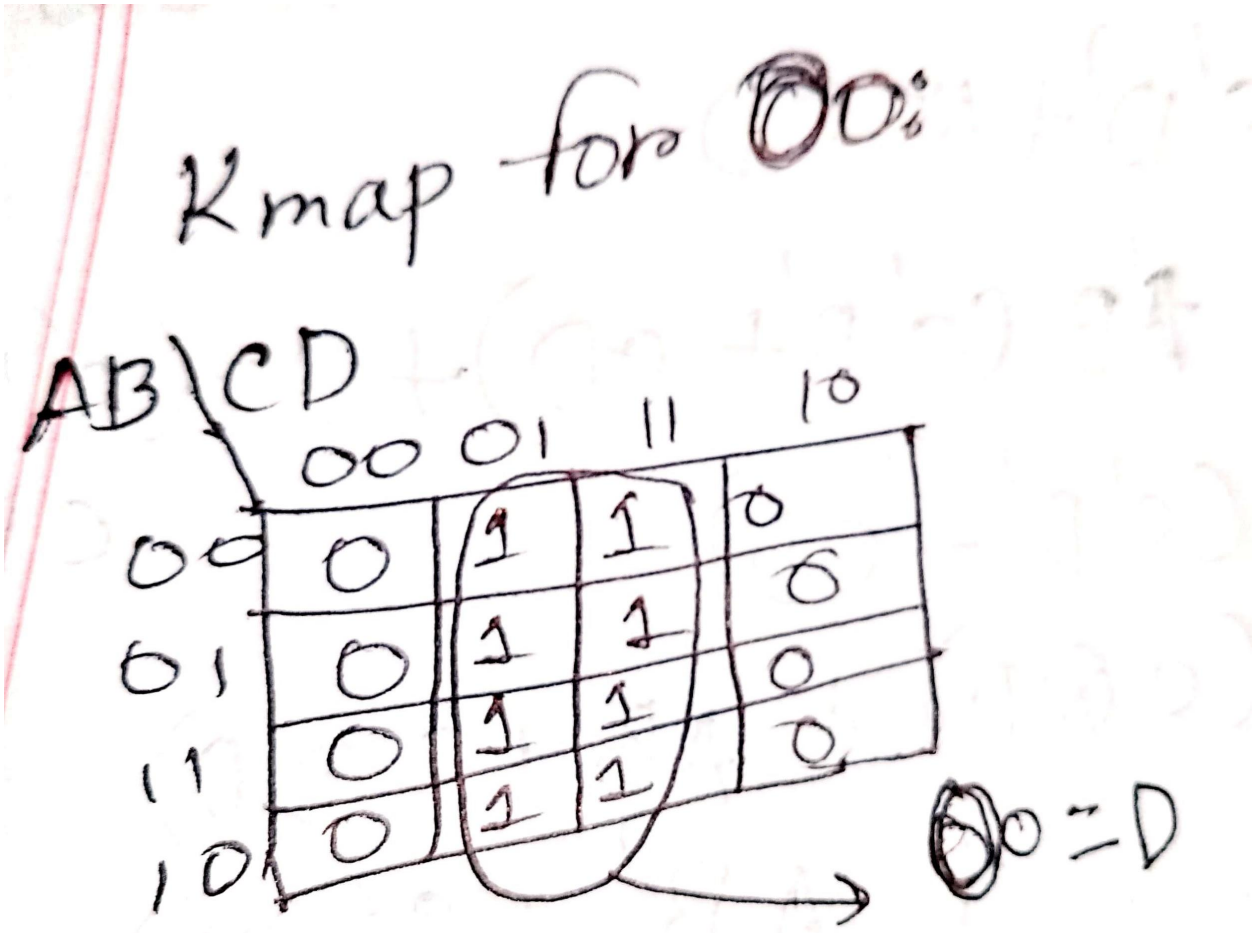
Expression: O3 = A



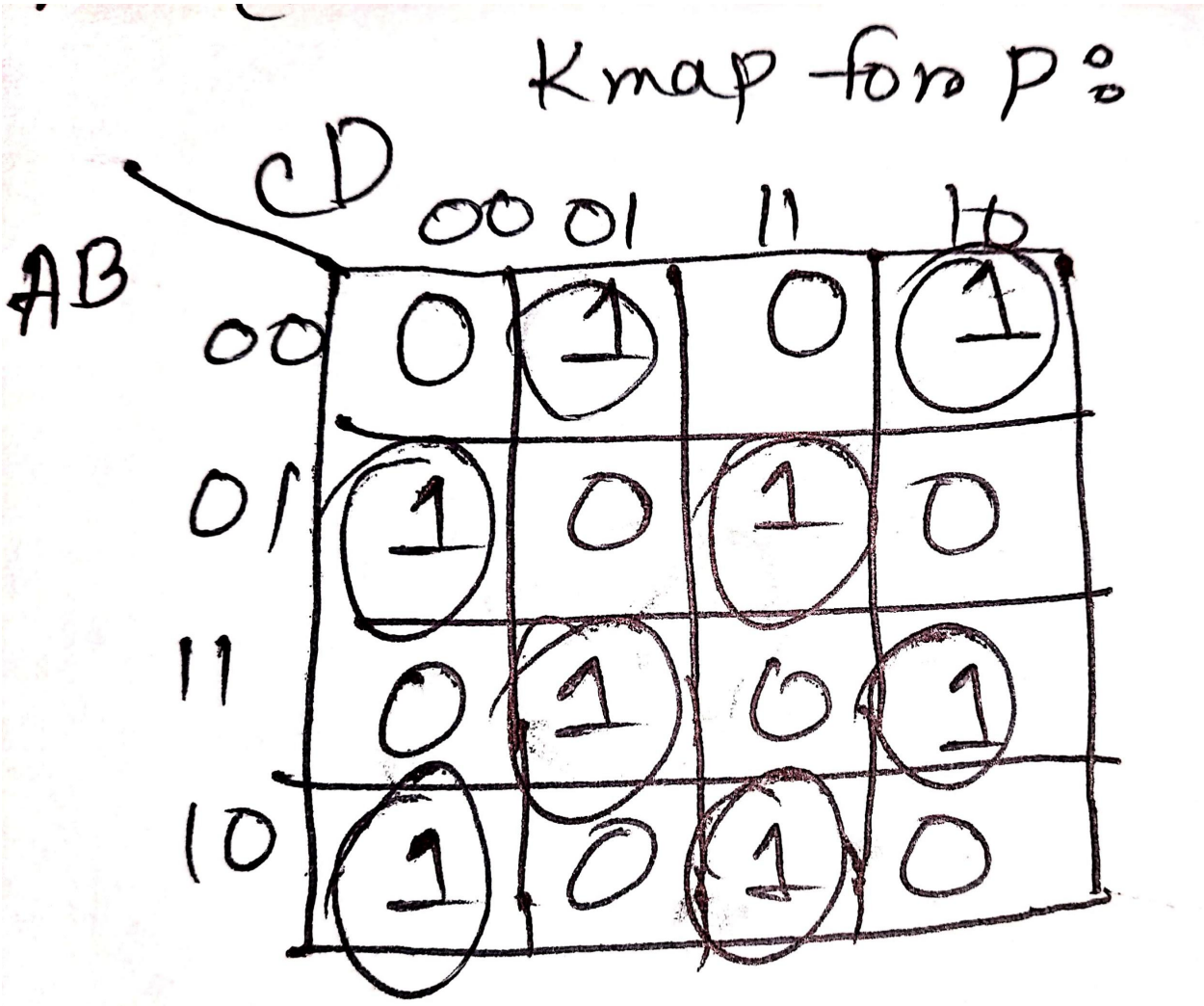
Expression: O2 = B



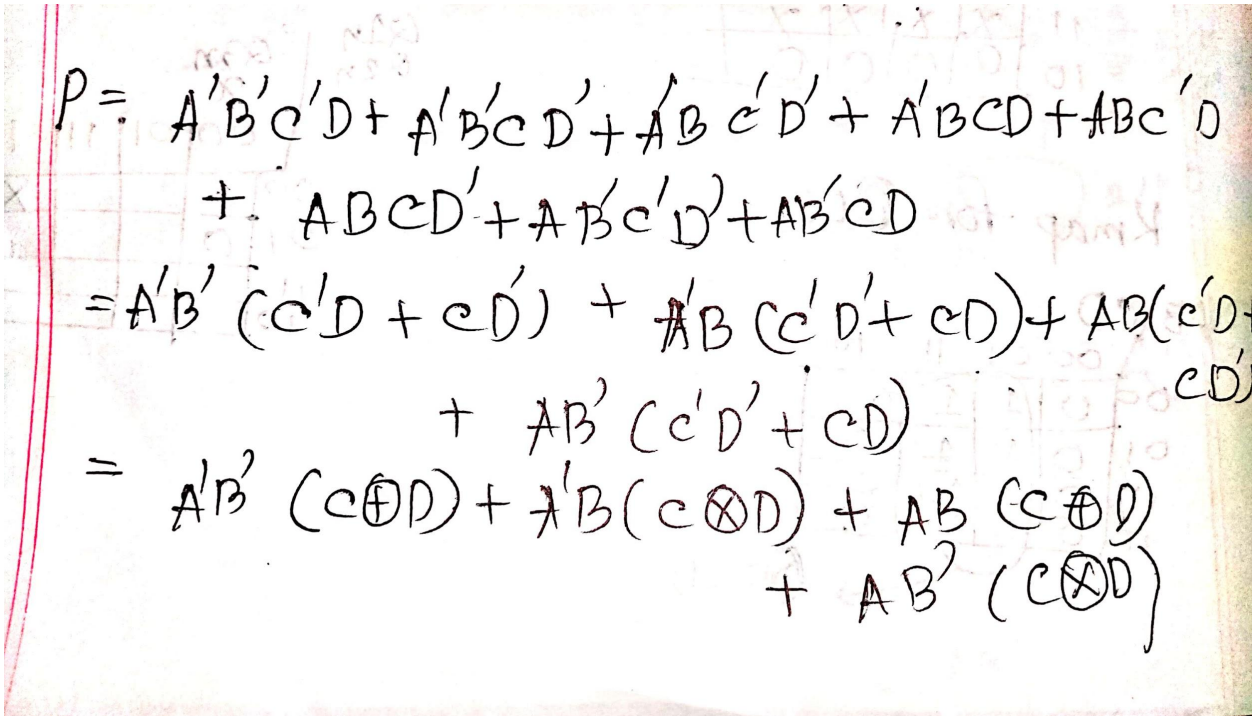
Expression: O1 = C

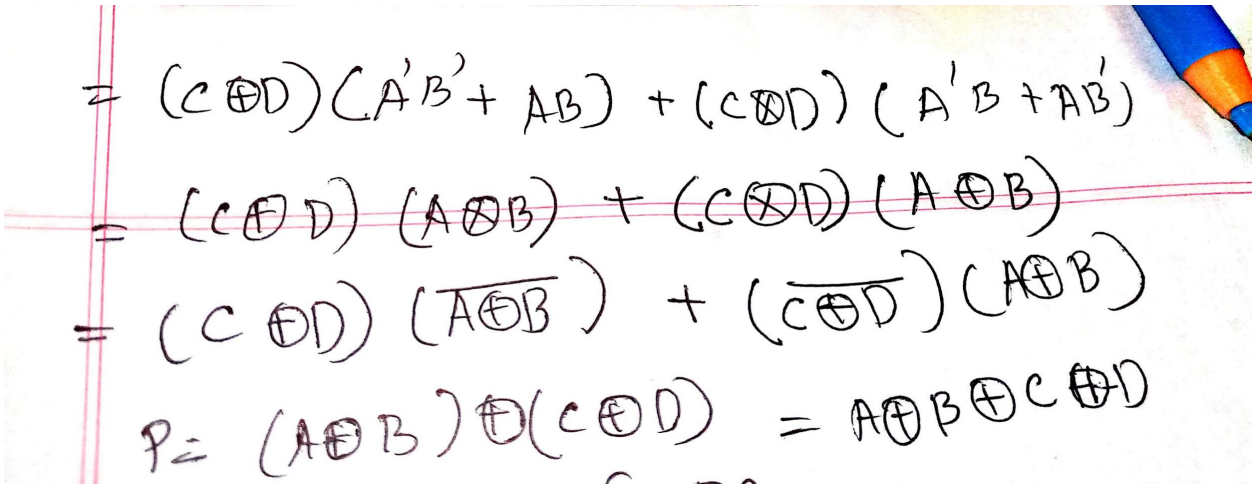


Expression: O0 = D

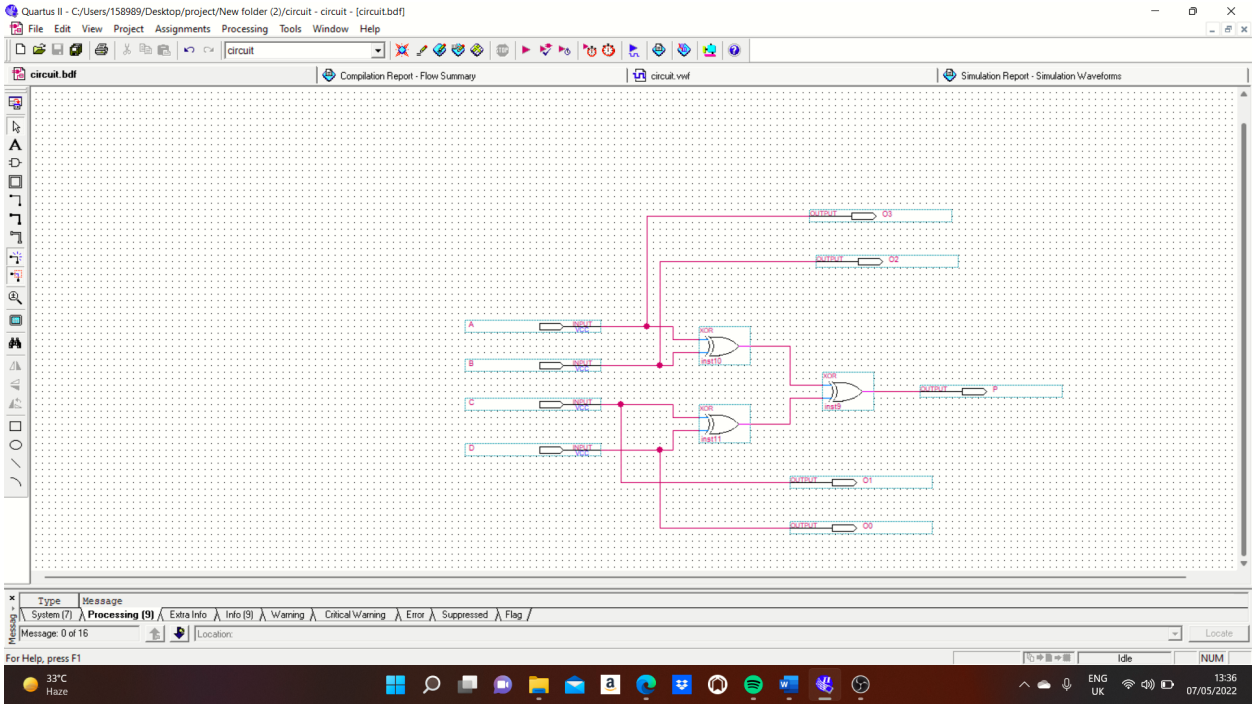


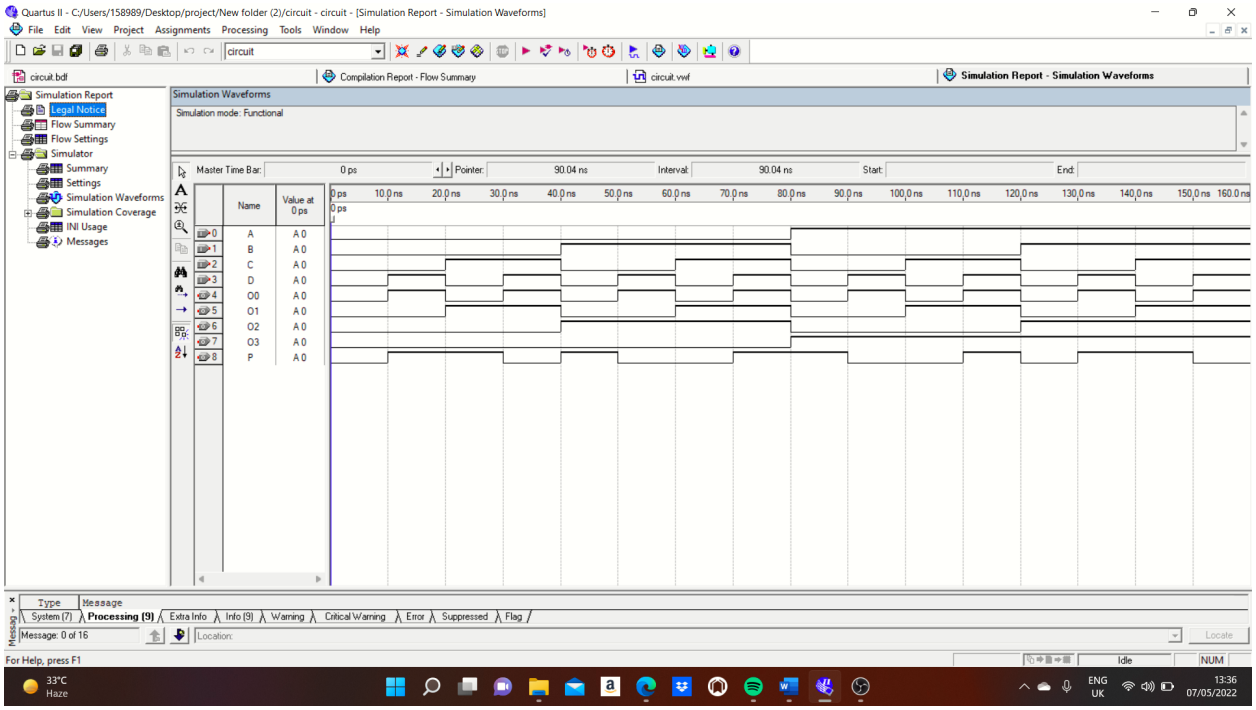
Expression:



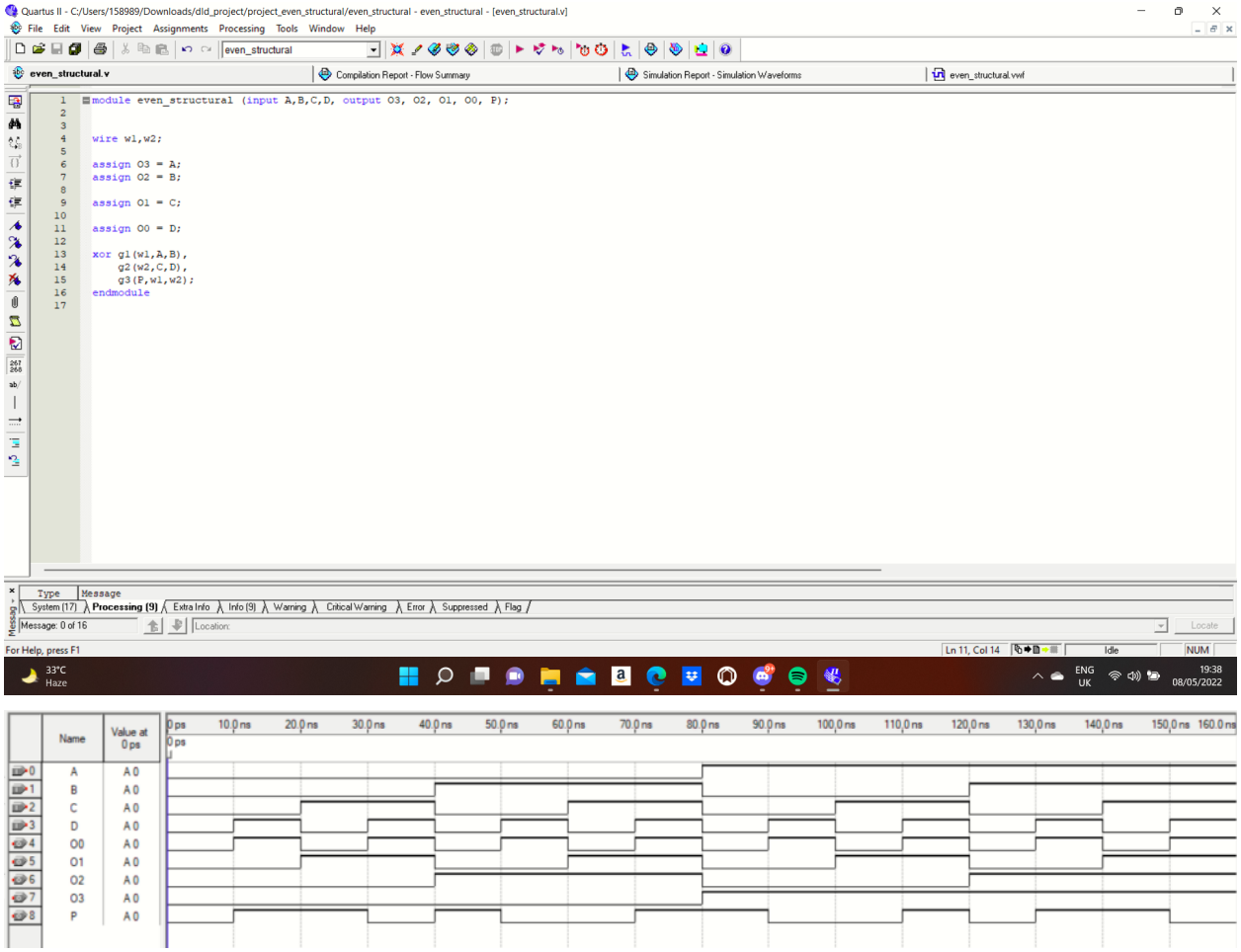


Circuit Simulation and Verilog codes:

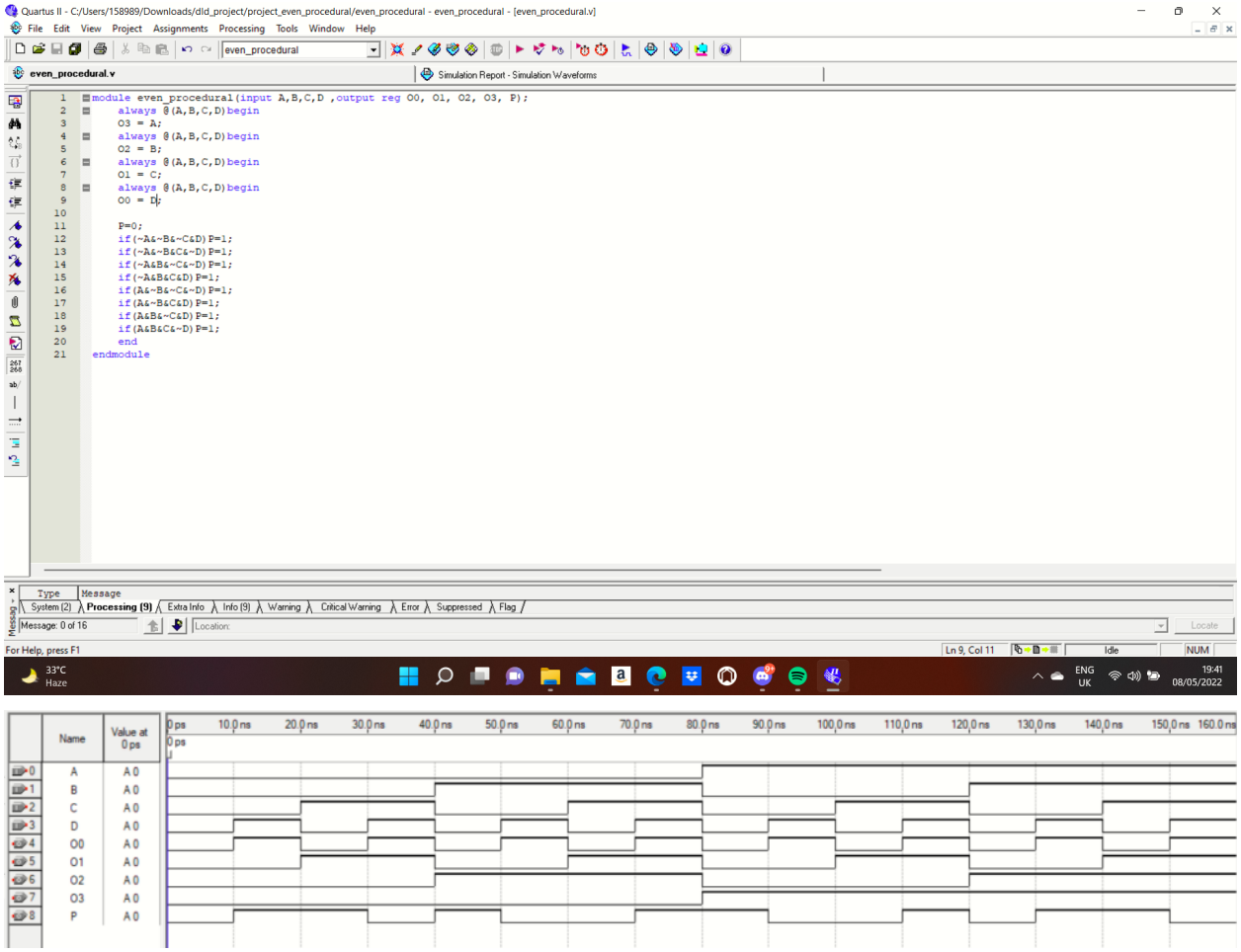




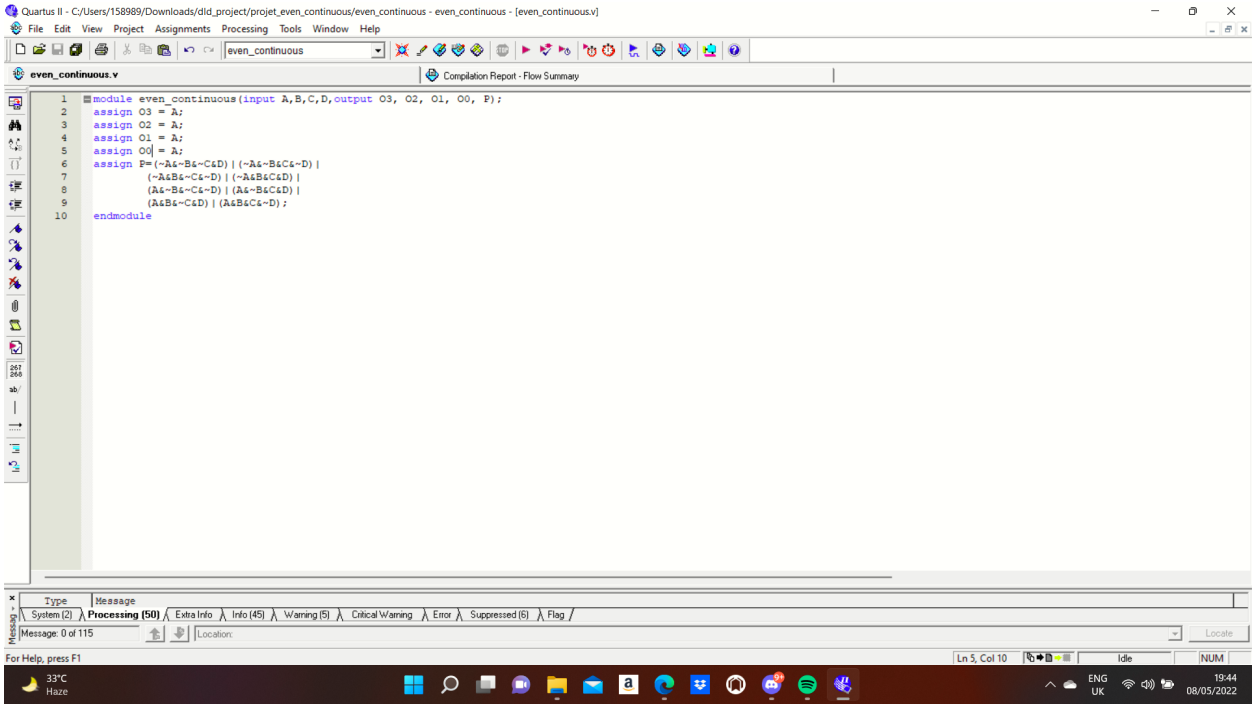
Structural Verilog Code with Simulation:

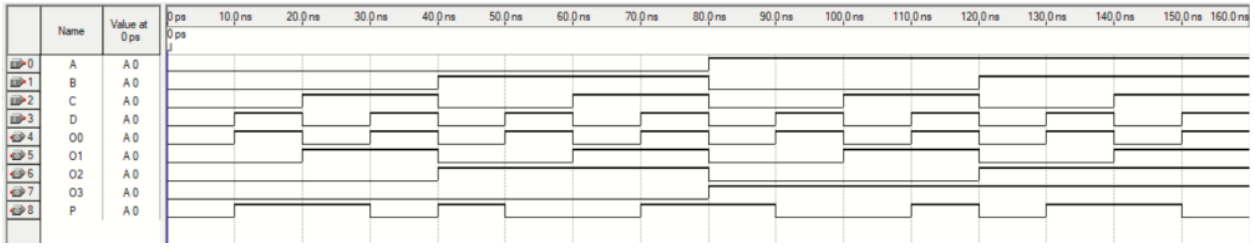


Behavioral Verilog using Procedural Model:



Behavioral Verilog using Continuous Assign Statement:





The experiment was conducted successfully.