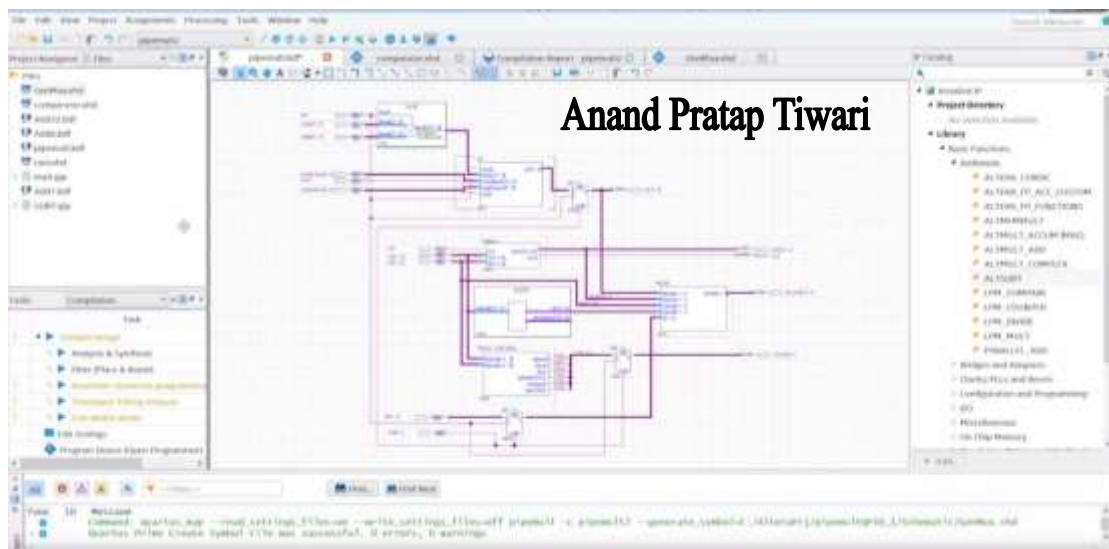
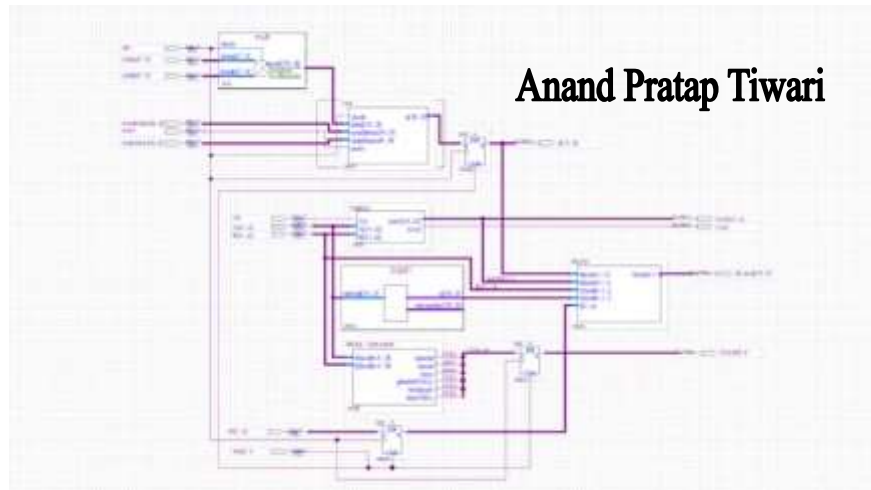
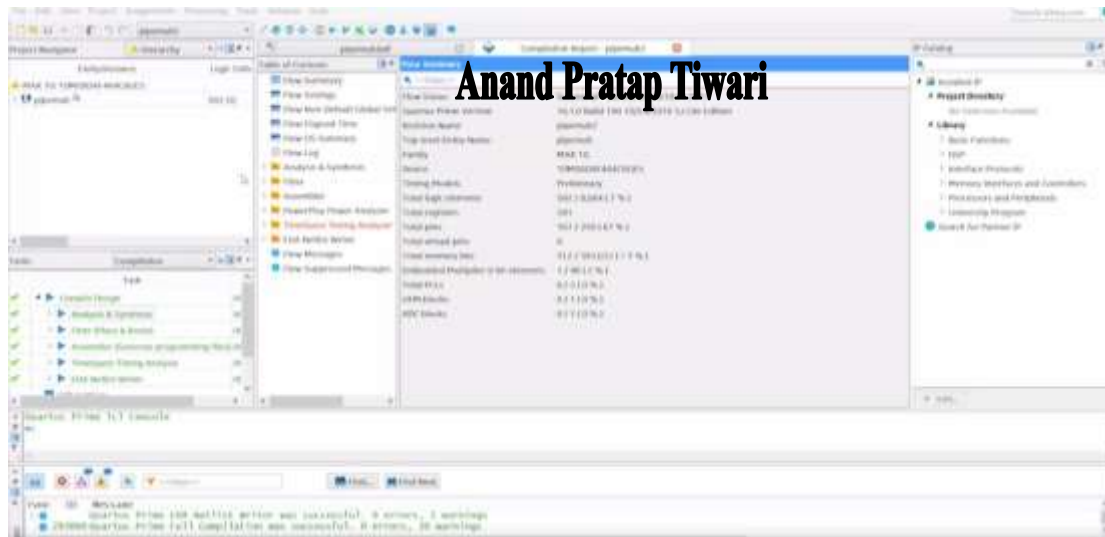


Screen Shot Submission Of Coursera
(Introduction To FPGA Design For Embedded System)-
Anand Pratap Tiwari

Video-3(FPGA Schematic Diagram)



Video-4(Compilation Report)



Video-4(F- Max % Utilization)



Video-6(The Assignment Editor Showing “Signal Wren”)

Status	From	To	Assignment Name	Value	Enabled	Entity	Comment
177		wraddress[1]	I/O Standard	3.3-...CMOS	Yes	pipemult	
178		wraddress[0]	I/O Standard	3.3-...CMOS	Yes	pipemult	
179		A	Location	IOBANK_8	Yes		
180		ALUout	Location	IOBANK_7	Yes		
181		B	Location	IOBANK_6	Yes		
182		CCout	Location	IOBANK_7	Yes		
183		dataa	Location	IOBANK_5	Yes		
184		datab	Location	IOBANK_5	Yes		
185		IR	Location	IOBANK_6	Yes		
186		q	Location	IOBANK_4	Yes		
187		Sum	Location	IOBANK_3	Yes		
188		rdaddress	Location	IOBANK_5	Yes		
189		wraddress	Location	IOBANK_5	Yes		
190		wren	Location	IOBANK_5	Yes		
191		Cin	Location	IOBANK_3	Yes		
192		Cout	Location	IOBANK_3	Yes		
193	<<new>>						

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Video-9(Compilation Report)

[illegible]

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