1. It is a monolithic code having single class with no inheritance.
2. In the codebase it is observed that there are unnecessary code blocks which are commented that can be removed.
3. In the (try catch) clauses, some catch clauses are empty.
4. The codebase is not observed to be modular.
5. In the VLSI Experiment 2, when the "Experiment" link is clicked on Virtual Experiment page, and circuit is created for NAND gate, the simulation should be successful. But "The circuit is not complete, Please Complete it and try again." message is displayed.
6. In the VLSI Experiment 2, when the "Quiz" link is clicked the Quiz page should be opened and Content should be present with no distortions and Junk characters, but the images are not displayed on Quiz page
7. In the VLSI Experiment 2, when the "Experiment" link is clicked on Virtual Experiment page, and circuit is created for NOR gate, the simulation should be successful. but "The circuit is not complete, Please Complete it and try again." message is displayed.