

# How to design a scalable embedded product

supporting different NXP i.MX applications processor families

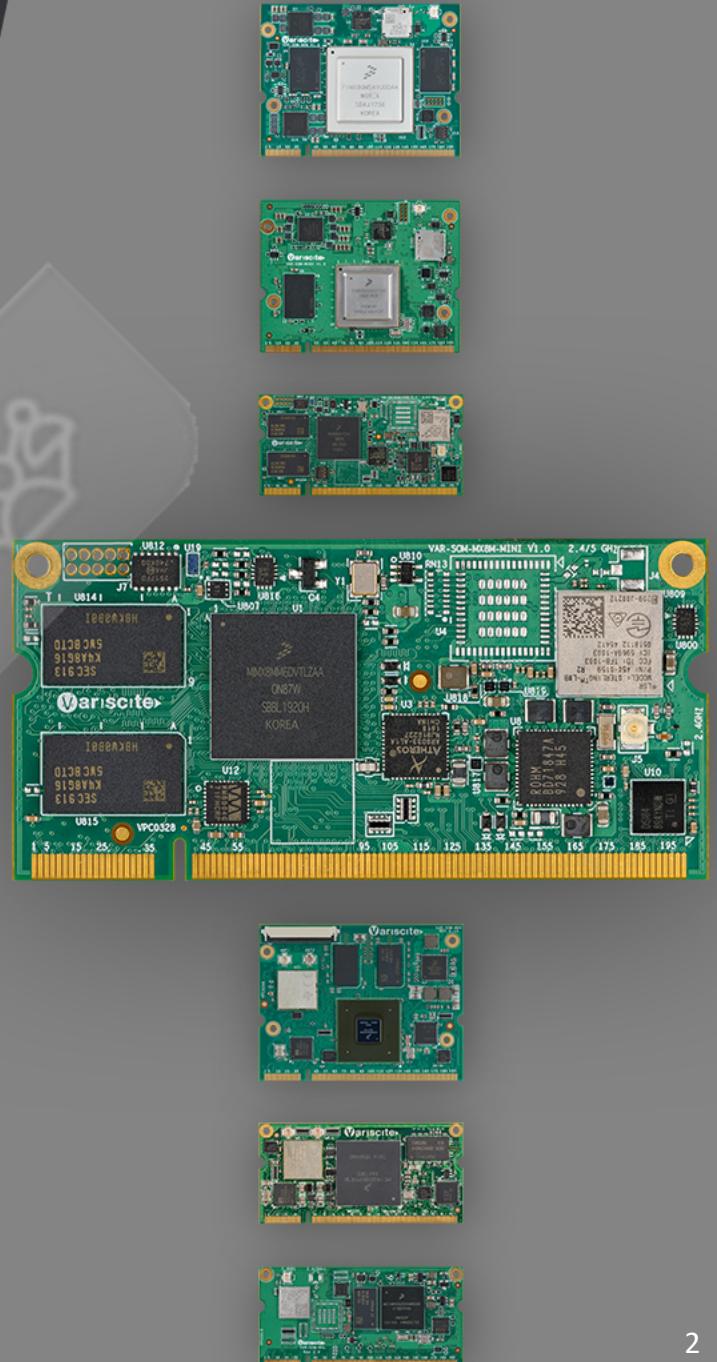
## Speakers

- Robert Thompson, Director Global i.MX Ecosystem, NXP Semiconductors
- Ofer Austerlitz, VP Business Development & Sales, Variscite
- Aviad Hadad, R&D Hardware expert, Variscite
- Pierluigi Passaro, R&D Software expert, Variscite



# Webinar Agenda

- The System-on-Module concept for a scalable design
- NXP's i.MX 8 product portfolio
- Variscite pin-to-pin System-on-Module families
- How to design a scalable embedded product supporting various i.MX processors:
  - Hardware aspects
  - Software aspects
  - Q&As



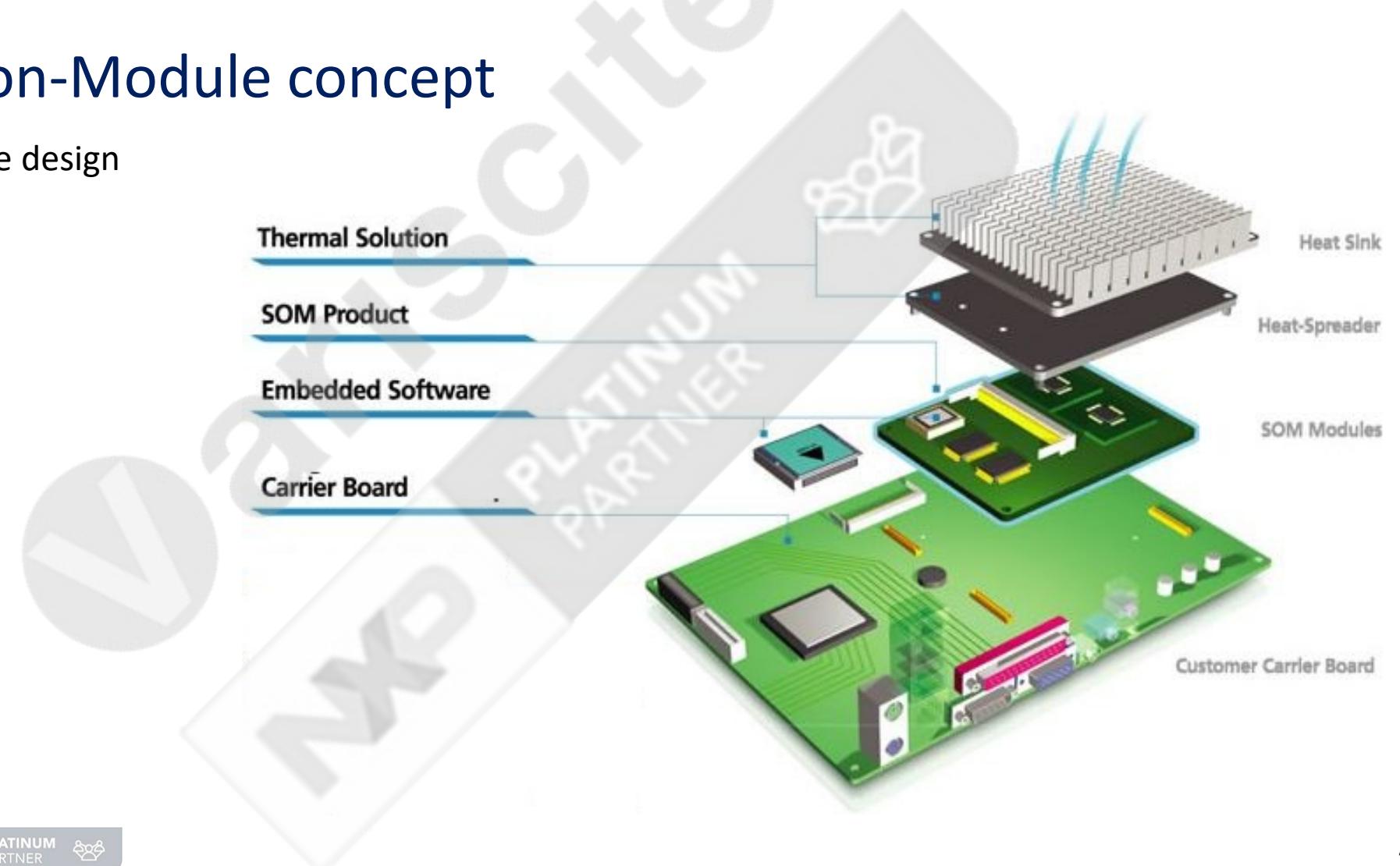
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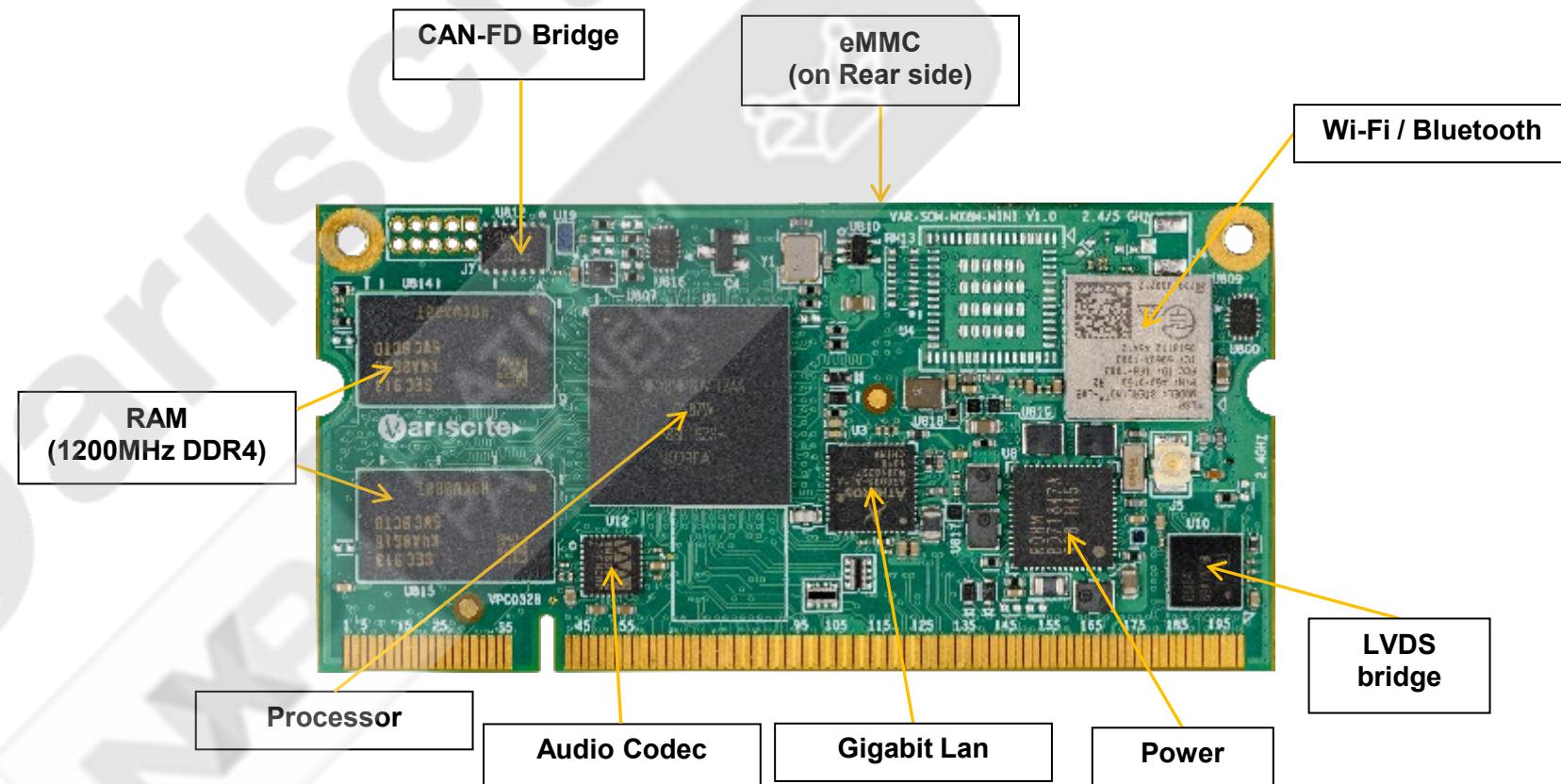
# The System-on-Module concept

The basis for a scalable design



# A typical System-on-Module

- The VAR-SOM-MX8M-MINI based on i.MX 8M Mini
- DART-MX8M-MINI Size:  
55.0 x 30.0 mm  
(~2.2 x 1.2 in)



## System-on-Module:

Off-The-Shelf stability,  
Custom design flexibility

- ✓ Fast time to market
- ✓ Reduce R&D cost
- ✓ Scalable AND Upgradeable
- ✓ 100% yield – All the time
- ✓ Production-ready software support
- ✓ Tested and used by hundreds of customers

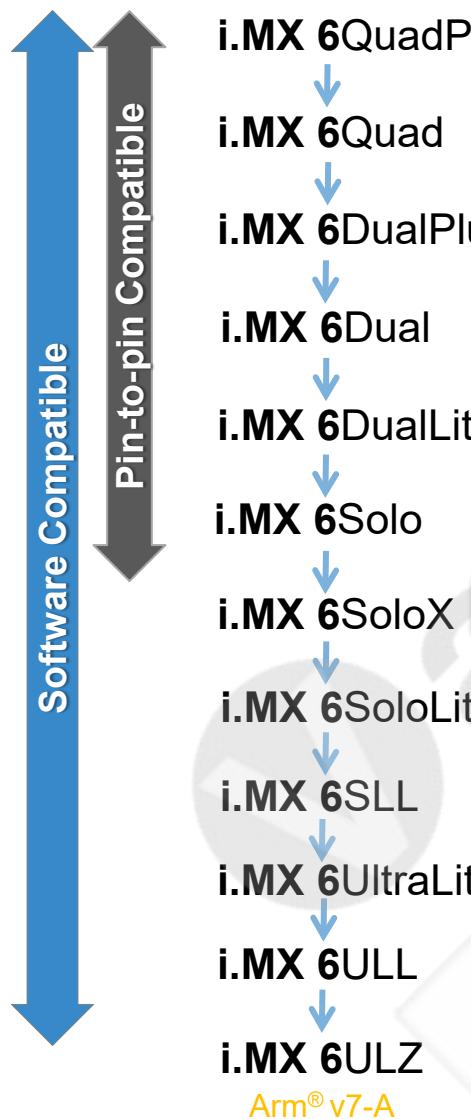
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# i.MX 8M Family of Applications Processors



i.MX 8 family  
Advanced Graphics, Vision & Performance

i.MX 8M family  
Advanced Computing, Audio/Video & Voice

i.MX 8X family  
Safety Certifiable & Efficient Performance

Arm® v8-A (32-bit/ 64-bit)

i.MX 7 family  
Flexible Efficient Connectivity

i.MX 7ULP family  
Ultra Low Power with Graphics

Arm® v7-A (32-bit)

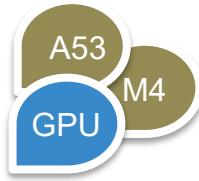


# i.MX 8 Series: Target Applications

Advanced graphics, video, image processing, vision, audio and voice

## i.MX 8M Family

Advanced Computing,  
Audio/Video & Voice



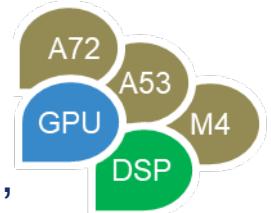
## i.MX 8X Family

Safety Certifiable &  
Efficient Performance



## i.MX 8 Family

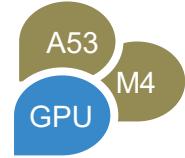
Advanced Graphics,  
Vision & Performance



# i.MX 8 Series: Scalable Solutions

Scalable series of three Arm V8 64-bit (/32-bit) based SoC Families

**i.MX 8M Family**  
Advanced Computing,  
Audio/Video & Voice



Pin Compatible



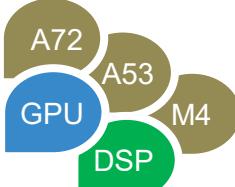
Pin Compatible

**i.MX 8X Family**  
Safety Certifiable &  
Efficient Performance



Pin Compatible

**i.MX 8 Family**  
Advanced Graphics,  
Vision & Performance



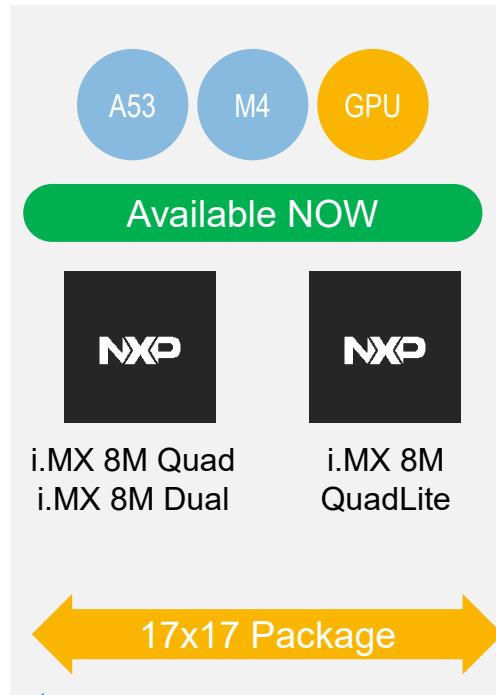
Pin Compatible

70% Hardware and Software Reuse

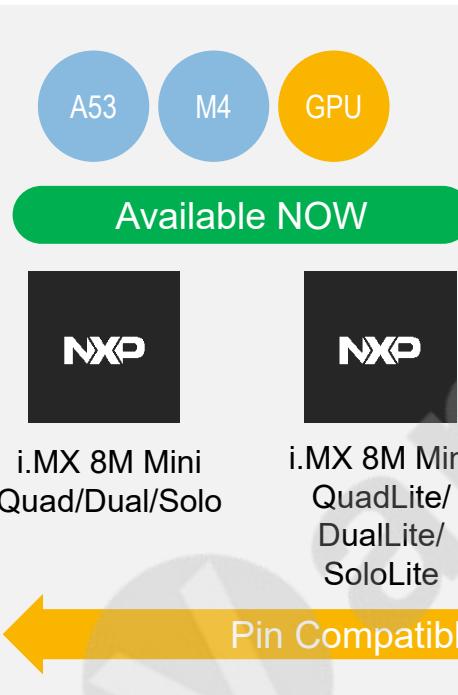
Software Compatible (including GPU Tools)

# i.MX 8M: Scalable broad market Solutions

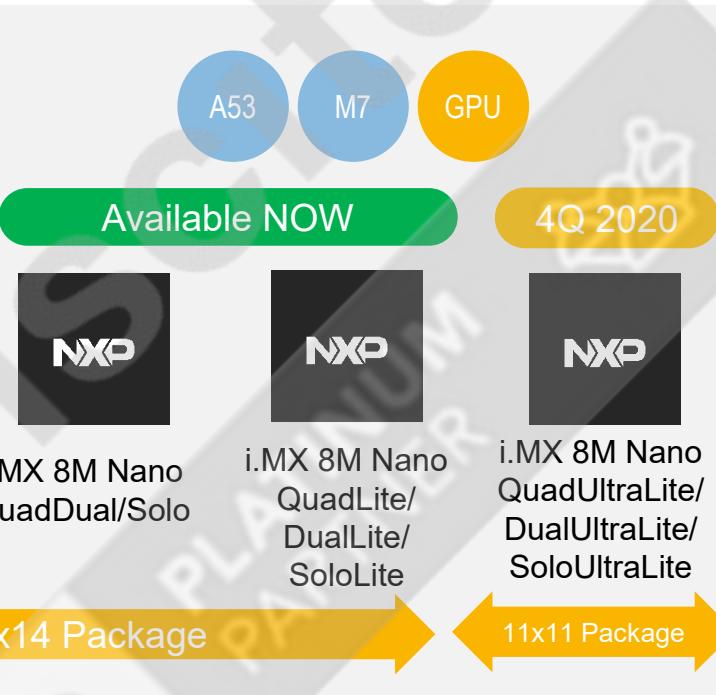
## i.MX 8M Quad Family



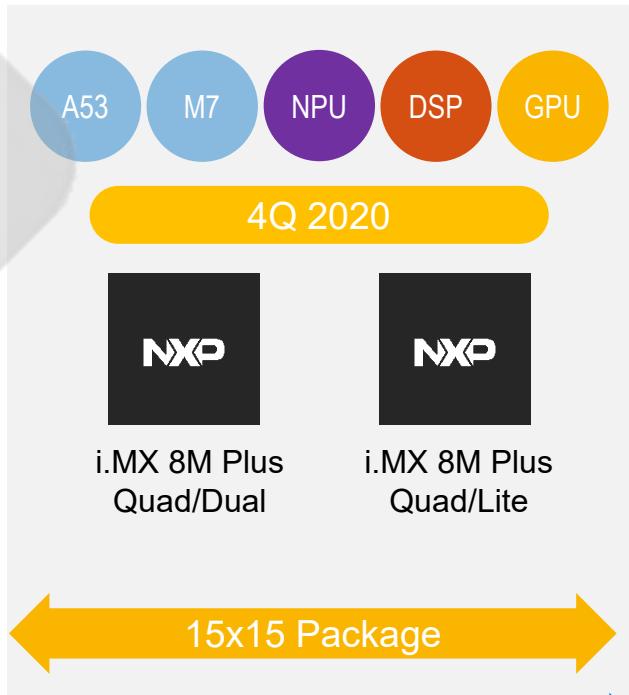
## i.MX 8M Mini Family



## i.MX 8M Nano Family



## i.MX 8M Plus Family



Software Compatible (including GPU Tools)

Scalable series of **FOUR** Arm V8 64-bit (/32-bit) based SoC Families



# i.MX 8M Target Applications

Consumer & Pro  
Audio Systems



Smart Home &  
Building Automation



Industrial HMI, Vision  
and Automation



Enterprise,  
Commercial &  
Healthcare



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Ofer Austerlitz, VP Business Development & Sales, Variscite

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# Variscite Pin2Pin product families

Two highly scalable product families based on NXP processors

## VAR-SOM Pin2Pin Family

VAR-SOM-MX8M-PLUS



Coming Soon

NXP i.MX 8M Plus  
4x 2GHz Cortex-A53

VAR-SOM-MX8



NXP i.MX 8 2x 1.8GHz Cortex-A72  
+ 4x 1.2GHz Cortex-A53

VAR-SOM-MX8X



NXP i.MX 8X  
4x 1.2GHz Cortex-A35

VAR-SOM-MX8M-MINI



NXP i.MX 8M Mini  
4x 1.8GHz Cortex-A53

VAR-SOM-MX8M-NANO



NXP i.MX 8M Nano  
4x 1.5GHz Cortex-A53

VAR-SOM-MX6



NXP i.MX 6  
4x 1.2GHz Cortex-A9

VAR-SOM-SOLO/DUAL



NXP i.MX 6  
2x 1GHz Cortex-A9

VAR-SOM-6UL



NXP i.MX 6 UL/ULL/ULZ  
900MHz Cortex-A7

Pin2Pin Compatible

## DART Pin2Pin Family

DART-MX8M-PLUS



Coming Soon

NXP i.MX 8M Plus  
4x 2GHz Cortex-A53

DART-MX8M



NXP i.MX 8M  
4x 1.5GHz Cortex-A53

DART-MX8M-MINI



NXP i.MX 8M Mini  
4x 1.8GHz Cortex-A53

Note:  
pin2pin compatibility depends on pinmux options



PLATINUM  
PARTNER



Pin2Pin Compatible

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# VAR-SOM Pin2Pin family

## Main compatible features of the VAR-SOM family:

### Display:

- LVDS
- Touch controller

### Networking:

- Ethernet
- Certified Dual band 802.11 ac/a/b/g/n Wi-Fi +BT v4.2 module

### Audio:

- Analog Headphone, Line In
- Digital microphone + Digital audio I/F

### Multimedia:

- MIPI CSI2 Camera

### Connectivity:

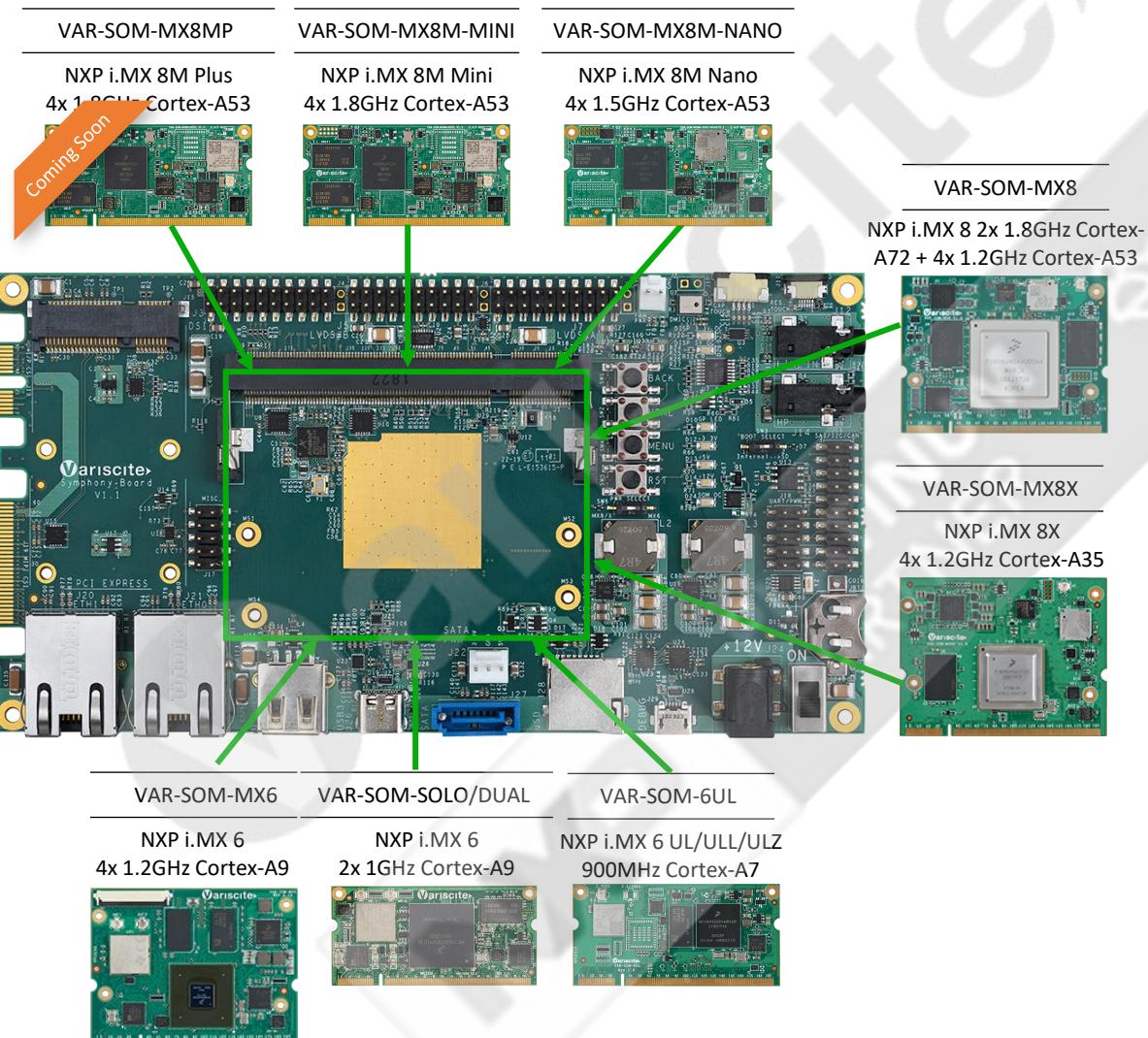
- USB 2.0/3.0
- PCIe Gen 2.0
- SD/MMC

### OS support:

- Linux – Yocto, Debian

### Unique features in specific modules

- 4K H.265/H.264 Decode
- 1080p H.265/H.264 encode/decode
- HDMI/eDP/DP
- USB 3.0
- Dual Gbit Ethernet
- Parallel CSI
- ADC
- SATA
- Parallel RGB
- E-ink display support

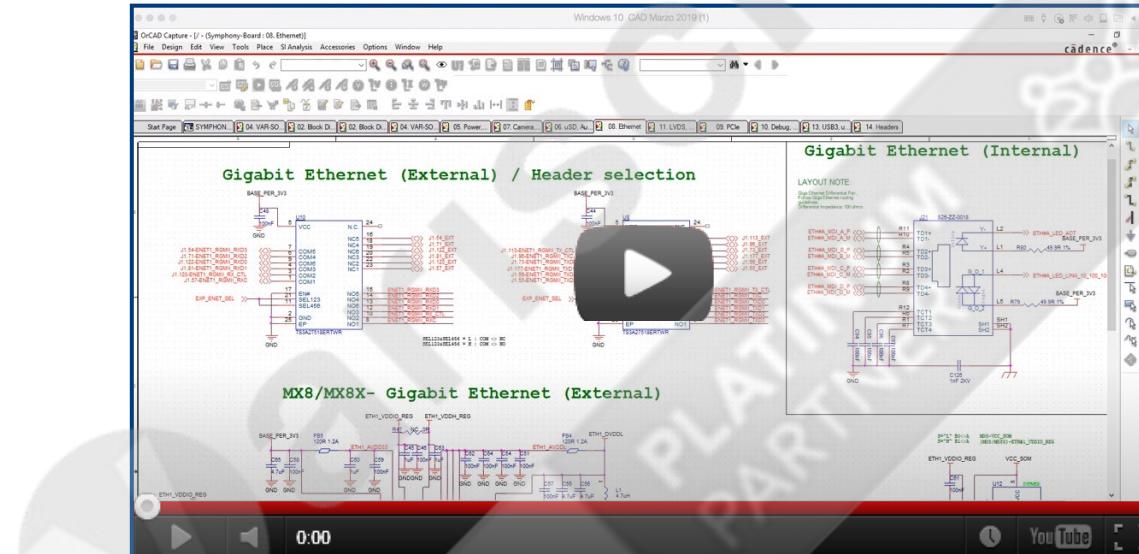


## Symphony-Board EVK main Features:

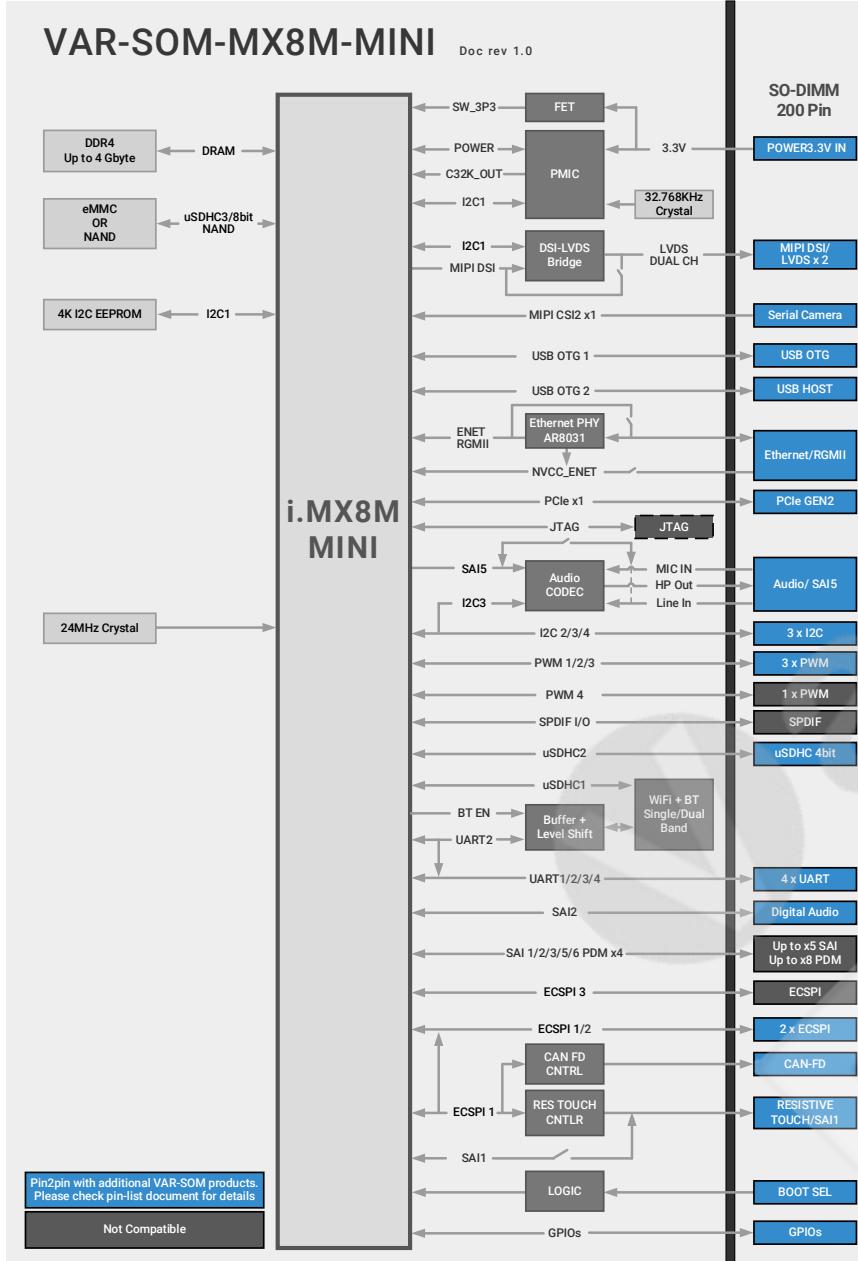
- Display connection - MIPI-DSI,LVDS, HDMI/DP(via Extension Card)
- Capacitive, Resistive touch connector
- Dual Gigabit Ethernet via RJ45 connector
- Mini PCIe Socket
- USB3.0 OTG Type C
- USB2.0 Host Type A
- Headphones, Line In jack, DMIC
- Micro SD card slot
- MIPI CSI camera , Parallel camera (via Extension Card)
- Micro SATA connector



# VAR-SOM Pin2Pin family – video intro



# Scalable Embedded design – SOM BD overview



Many interface options exist especially with the pin mux options. We selected the most commonly used interfaces in the embedded market and decided to make them pin2pin (blue) the others can be “partial” pin2pin or even unique for a specific processor/SoM.

Conclusion: one needs to pay attention when designing the custom carrier board and make sure that his own interfaces are falling into the pin2pin options

# Scalable Embedded design – Pinmuxing

## A glance at the VAR-SOM-MX8M-MINI datasheet

- SO-DIMM pinout table
- Pinmux table
- Interface Pinout table

### VAR-SOM-MX8M-MINI SYSTEM ON MODULE

#### 7.3.1. VAR-SOM-MX8M-MINI SO-DIMM Pin-out

**Table 3: SO-DIMM PIN-OUT**

PIN#	ASSY	BALL NAME	GPIO	NOTES	BALL
1	No EC	ENET_TX_CTL	GPIO1_IO22	Powered by VDD_ENET pin; On some SOM modules this pin is GND; If placed in such carrier with no "EC" configuration define PAD as input!	SOC.AF24
1	EC	NC		With "EC" configuration this pin is Not Connected.	NC_EC
2		GND		Digital Ground	GND
3	No EC	ENET_TD3	GPIO1_IO18	Powered by VDD_ENET pin	SOC.AF25
3	EC	ETH_TRX0_P		Signal source is Ethernet PHY.	AR8033.11
4	No EC	ENET_RDO	GPIO1_IO26	Powered by VDD_ENET pin	SOC.AE27
4	EC	ETH_TRX2_P		Signal source is Ethernet PHY.	AR8033.17
5	No EC	ENET_TD2	GPIO1_IO19	Powered by VDD_ENET pin	SOC.AG25
5	EC	ETH_TRX0_N		Signal source is Ethernet PHY.	AR8033.12
6	No EC	ENET_RD1	GPIO1_IO27	Powered by VDD_ENET pin	SOC.AD27
6	EC	ETH_TRX2_N		Signal source is Ethernet PHY.	AR8033.18
7		GND		Digital Ground	GND
8		GND		Digital Ground	GND
9	No EC	ENET_TD1	GPIO1_IO20	Powered by VDD_ENET pin	SOC.AF26
9	EC	ETH_TRX1_P		Signal source is Ethernet PHY.	AR8033.14
10	No EC	ENET_RD2	GPIO1_IO28	Powered by VDD_ENET pin	SOC.AD26
10	EC	ETH_TRX3_P		Signal source is Ethernet PHY.	AR8033.20
11	No EC	ENET_TDO	GPIO1_IO21	Powered by VDD_ENET pin	SOC.AG26
11	EC	ETH_TRX1_N		Signal source is Ethernet PHY.	AR8033.15
12	No EC	ENET_RD3	GPIO1_IO29	Powered by VDD_ENET pin	SOC.AC26
12	EC	ETH_TRX3_N		Signal source is Ethernet PHY.	AR8033.21
13		GND		Digital Ground	GND
14		GND		Digital Ground	GND
15	No EC	ENET_RX_CTL	GPIO1_IO24	Powered by VDD_ENET pin	SOC.AF27

### VAR-SOM-MX8M-MINI SYSTEM ON MODULE

#### 7.4. VAR-SOM-MX8M-MINI Pin-Mux

This section tables lists the SOM connectors with the available functions on each pin.

**Table 4: VAR-SOM-MX8M-MINI PINMUX**

PIN	ASSY	BALL	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6
1	No EC	SOC.AF24	ENET_TX_CTL					GPIO1_IO22	
3	No EC	SOC.AF25	ENET_TD3					GPIO1_IO18	
4	No EC	SOC.AE27	ENET_RDO					GPIO1_IO26	
5	No EC	SOC.AG25	ENET_TD2	IN=ENET_TX_CLK OUT=ENET_REF_CLK_ROOT					GPIO1_IO19
6	No EC	SOC.AD27	ENET_RD1					GPIO1_IO27	
9	No EC	SOC.AF26	ENET_TD1					GPIO1_IO20	
10	No EC	SOC.AD26	ENET_RD2					GPIO1_IO28	
11	No EC	SOC.AC26	ENET_TDO					GPIO1_IO21	
12	No EC	SOC.AC26	ENET_RD3					GPIO1_IO29	
15	No EC	SOC.AF27	ENET_RX_CTL					GPIO1_IO24	
16	No EC	SOC.AE26	ENET_RXC	ENET_RX_ER				GPIO1_IO25	
17		SOC.AF8	SPDIF_EXT_CLK	PWM1_OUT					GPIO5_IO05
18	No AC	SOC.AC13	SAI5_RXD3	SAI1_TXD5	SAI1_TXFS	SAI5_TXD0	PDM_BIT3	GPIO3_IO24	
20	No AC	SOC.AD15	SAI5_MCLK	SAI1_TXC					GPIO3_IO25
21		SOC.AC24	SAI2_RXD0	SAI5_TXD0				UART1 RTS_B	GPIO4_IO23
22		SOC.AB22	SAI2_RXC	SAI5_TXC				UART1_RXD	GPIO4_IO22
23		SOC.AC19	SAI2_RXFS	SAI5_TXFS	SAI5_TXD1	SAI2_RXD1	UART1_TxD	GPIO4_IO21	
24		SOC.AD23	SAI2_TXFS	SAI5_TxD1				SAI2_TxD1	UART1_CTS_B
									GPIO4_IO24

### VAR-SOM-MX8M-MINI SYSTEM ON MODULE

#### 8.11.1.1. UART1 Signals

**Table 32: UART1 Signals**

PIN#	ASSY	ALT_NAME	ALT#	NOTES	BALL
24		UART1_CTS_B	4		SOC.AD23
55		UART1_CTS_B	1	Appear on pins 55 & 175 for other SOM modules UART compatibility	SOC.E18
21		UART1_RTS_B	4		SOC.AC24
57		UART1_RTS_B	1	Appear on pins 57 & 124 for other SOM modules UART compatibility	SOC.D18
124		UART1_RTS_B	1	Appear on pins 57 & 124 for other SOM modules UART compatibility	SOC.D18
22		UART1_RXD	4		SOC.AB22
54		UART1_RXD	0		SOC.E14
23		UART1_TxD	4		SOC.AC19
56		UART1_TxD	0		SOC.F13

# Scalable Embedded design – Pinmuxing

Using the VAR-SOMs Compatibility spreadsheet:

- VAR-SOM-xx Pinmux tab available for each SoM in the VAR-SOM Pin2Pin family

PIN#	Name	SOM Usage	Applicable Configuration	Note	
44	NC/*/CAN_TX				Even
45	~ECSP1_MOSI//UART3_TXD////GPIO5_IO07	ECSP1	CN or TP	Shared	Odd
46	NC/*/CAN_RX				Even
47	GND				Odd
48	GPIO1_IO02/~WDOG_B////WDOG_ANY	WDOG_B		Always connected to PMIC_WDOG_B input	Even
49	SOM_3V3_PER				Odd
50	SAI3_RXC/GPT1_CLK//SAI5_RXC///~UART2_CTS_B////GPIO4_IO29	UART2	WBD or WB	Function can be released with BT disabled	Even
51	SAI3_RXD/GPT1_COMPARE1//SAI5_RXD0///~UART2_RTS_B////GPIO4_IO30	UART2	WBD or WB	Function can be released with BT disabled	Odd
52	SAI3_TXC/GPT1_COMPARE2//SAI5_RXD2///~UART2_TXD////GPIO5_IO00	UART2	WBD or WB	Function can be released with BT disabled	Even
53	SAI3_TXFS/GPT1_CAPTURE2//SAI5_RXD1///SAI3_TXD1///~UART2_RXD////GPIO4_IO31	UART2	WBD or WB	Function can be released with BT disabled	Odd
54	UART1_RXD/ECSP13_SCLK////GPIO5_IO22				Even
55	_UART3_RXD/UART1_CTS_B////GPIO5_IO26			Duplicate pin on 157	Odd
56	UART1_TXD/ECSP13_MOSI////GPIO5_IO23				Even
57	UART3_TXD/UART1_RTS_B////GPIO5_IO27			Duplicate pin on 124	Odd
58	GND				Even
59	GND				Odd
60	SD2_CLK////GPIO2_IO13				Even
61	SD2_DATA2////GPIO2_IO17				Odd
62	SD2_DATA0////GPIO2_IO15				Even
63	SD2_DATA1////GPIO2_IO16				Odd
64	SD2_CMD////GPIO2_IO14				Even
65	SD2_DATA3////GPIO2_IO18				Odd
66	GND				Even

# Scalable Embedded design – Pinmuxing

Using the VAR-SOMs Compatibility spreadsheet:

- “CompatibilityPinMap” tab - ALL VAR-SOM MOST COMMON FUNCTION table

**ALL VAR-SOM MOST COMMON FUNCTION; If none will display unique or GPIO by default;**

**Function to highlight**

**Enter PIN#**

**SPECIFIC SOM PIN FUNCTIONS :**

17	VAR-SOM-MX6	IPU1_DISPO_DATA09/IPU2_DISPO_DATA09//PWM2_OUT//WDOG2_B///GPIO4_IO30
	VAR-SOM-MX8	LVDS0_GPIO0_IO00/LVDS0_PWM0_OUT//LSIO_GPIO1_IO04
	VAR-SOM-MX8X	MIPI_DSI0_GPIO0_IO00/ADMA_I2C1_SCL//MIPI_DSI0_PWM0_OUT///LSIO_GPIO1_IO27
	VAR-SOM-MX8MM	SPDIF_EXT_CLK/PWM1_OUT///GPIO5_IO05
	VAR-SOM-MX8MN	SPDIF_EXT_CLK/PWM1_OUT///GPIO5_IO05
	VAR-SOM-MX8UL	ENET_REF_CLK2/PWM4_OUT//OTG2_ID//CSI_FIELD//USDHCI_VSELECT///GPIO1_IO5(ADC IN5)///ENET2_1588_EVENT0_OUT//CCM_PLL3_BYP//UARTS_RX
	VAR-SOM-SOLO	IPU1_DISPO_D09/LCD_D09//PWM2_OUT//WDOG2_B///GPIO4_IO30
	VAR-SOM-MX8MP	SPDIF1_EXT_CLK/PWM1_OUT//GPT1_COMPARE3///GPIO5_IO05

# Scalable Embedded design – Pinmuxing

Using the VAR-SOMs Compatibility spreadsheet:

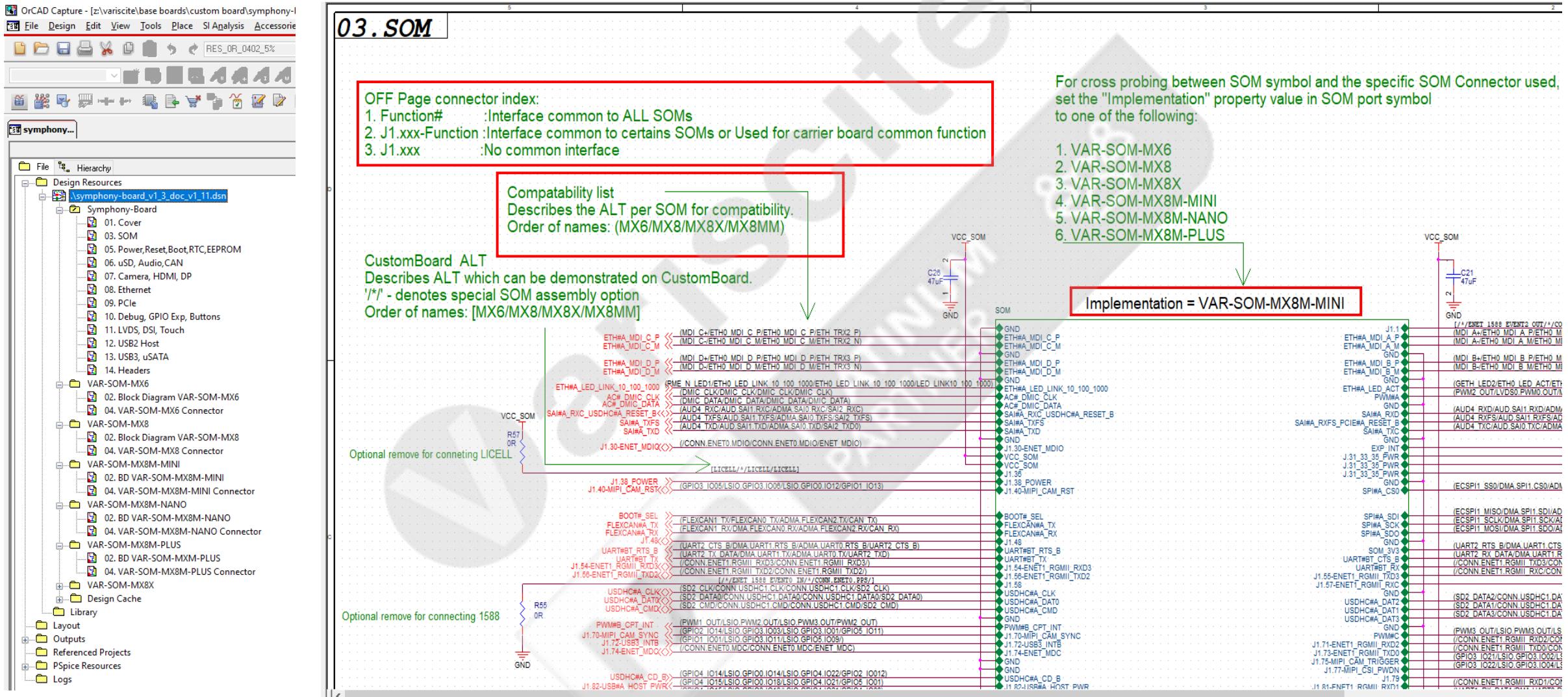
- “CompatibilityPinMap” tab - ALL VAR-SOM MOST COMMON FUNCTION table (Cont.)

PIN#	ALL VAR-SOM MOST COMMON FUNCTION; If none will display unique or GPIO by default;								UART	User PIN#	SPECIFIC SOM PIN FUNCTIONS :
	VAR-SOM-MX6	VAR-SOM-MX8	VAR-SOM-MX8X	VAR-SOM-MX8MM	VAR-SOM-MX8MN	VAR-SOM-6UL	VAR-SOM-SOLO	VAR-SOM-MX8MP			
1	GND	GND	GND	GND	GND	DGND	DGND	GND			
2	GND	GND	GND	GND	GND	DGND	DGND	GND			
39	ECSPI1_SSO	DMA_SPI1_CS0	ADMA_SPI2_CS0	ECSPI1_SSO	ECSPI1_SSO	ECSPI4_SSO	ECSPI1_SSO	ECSPI2_SSO			
40	GPIO3_IO05	LSIO_GPIO3_IO06	LSIO_GPIO0_IO12	GPIO1_IO13	GPIO1_IO13	NC	GPIO3_IO05	GPIO1_IO00			
41	ECSPI1_MISO	DMA_SPI1_SD1	ADMA_SPI2_SD1	ECSPI1_MISO	ECSPI1_MISO	ECSPI4_MISO	ECSPI1_MISO	ECSPI2_MISO			
42	SRC_BOOT_CFG07	BOOT_SEL	BOOT_SEL	BOOT_SEL	BOOT_SEL	BOOT_SELO	SRC_BOOT_CFG07	BOOT_SEL			
43	ECSP1_SCLK	DMA_SPI1_SCK	ADMA_SPI2_SCK	ECSP1_SCLK	ECSP1_SCLK	ECSP14_SCLK	ECSP1_SCLK	ECSP12_SCLK			
44	FLEXCAN1_TX	FLEXCAN0_TX	ADMA_FLEXCAN2_TX	CAN_TX	CAN_TX	CAN1_TX	FLEXCAN1_TX	FLEXCAN2_TX			
45	ECSP1_MOSI	DMA_SPI1_SDO	ADMA_SPI2_SDO	ECSP1_MOSI	ECSP1_MOSI	ECSP14_MOSI	ECSP1_MOSI	ECSP12_MOSI			
46	FLEXCAN1_RX	DMA_FLEXCAN0_RX	ADMA_FLEXCAN2_RX	CAN_RX	CAN_RX	CAN1_RX	FLEXCAN1_RX	FLEXCAN2_RX			
47	GND	GND	GND	GND	DGND	DGND	GND	GND			
48	GPIO4_IO10	LSIO_GPIO0_IO17	LSIO_GPIO3_IO02	GPIO1_IO02/WDOG_B	GPIO1_IO02/WDOG_B	GPIO1_IO25	GPIO4_IO10	SAI2_MCLK			
49	SOM_3V3_PER	SOM_3V3_PER	SOM_3V3_PER	SOM_3V3_PER	SOM_3V3_PER	SOM_3V3_PER	SOM_3V3_PER	SOM_3V3_PER			
50	UART2_CTS_B	DMA_UART1_RTS_B	ADMA_UART0_RTS_B	UART2_CTS_B	UART2_CTS_B	UART2_CTS_B	UART3_CTS_B				
51	UART2_RTS_B	DMA_UART1_CTS_B	ADMA_UART0_CTS_B	UART2_RTS_B	UART2_RTS_B	UART2_RTS_B	UART3_RTS_B				
52	UART2_TX_DATA	DMA_UART1_TX	ADMA_UART0_TX	UART2_TXD	UART2_TXD	UART2_TX	UART2_TX	UART3_TX			
53	UART2_RX_DATA	DMA_UART1_RX	ADMA_UART0_RX	UART2_RXD	UART2_RXD	UART2_RX	UART2_RX	UART3_RX			
54	UART3_RX_DATA	UART3_RX	LSIO_GPIO0_IO05	UART1_RXD	UART1_RXD	UART5_RX	UART3_RX	GPIO4_IO09			
55	UART3_CTS_B	UART3_RTS (actually CTS)	LSIO_GPIO0_IO03	UART1_CTS_B	UART1_CTS_B	UART5_CTS_B	UART3_CTS_B	GPIO4_IO15			
56	UART3_TX_DATA	UART3_TX	LSIO_GPIO0_IO01	UART1_TXD	UART1_TXD	UART5_TX	UART3_TX	GPIO4_IO14			
57	UART3_RTS_B	UART3_CTS (actually RTS)	LSIO_GPIO0_IO04	UART1_RTS_B	UART1_RTS_B	UART5_RTS_B	UART3_RTS_B	GPIO4_IO11			
58	GND	GND	GND	GND	GND	DGND	GPIO2_IO30	GND			
59	GND	GND	GND	GND	GND	DGND	DGND	GND			
60	SD2_CLK	CONN_USDHCI1_CLK	CONN_USDHCI1_CLK	SD2_CLK	SD2_CLK	SD1_CLK	SD2_CLK	USDHC2_CLK			
61	SD2_DATA2	CONN_USDHCI1_DATA2	CONN_USDHCI1_DATA2	SD2_DATA2	SD2_DATA2	SD1_DATA2	SD2_D2	USDHC2_DATA2			
62	SD2_DATA0	CONN_USDHCI1_DATA0	CONN_USDHCI1_DATA0	SD2_DATA0	SD2_DATA0	SD1_DATA0	SD2_D0	USDHC2_DATA0			
63	SD2_DATA1	CONN_USDHCI1_DATA1	CONN_USDHCI1_DATA1	SD2_DATA1	SD2_DATA1	SD1_DATA1	SD2_D1	USDHC2_DATA1			
64	SD2_CMD	CONN_USDHCI1_CMD	CONN_USDHCI1_CMD	SD2_CMD	SD2_CMD	SD1_CMD	SD2_CMD	USDHC2_CMD			
65	SD2_DATA3	CONN_USDHCI1_DATA3	CONN_USDHCI1_DATA3	SD2_DATA3	SD2_DATA3	SD1_DATA3	SD2_D3	USDHC2_DATA3			
66	GND	GND	GND	GND	GND	DGND	DGND	GND			
67	GND	GND	GND	GND	GND	DGND	DGND	GND			
68	PWM1_OUT	LSIO_PWM2_OUT	LSIO_PWM3_OUT	PWM2_OUT	PWM2_OUT	PWM2_OUT	PWM1_OUT	PWM3_OUT			

Revision	Mnemonics	Compatibility_PinMap	SymphonyConnectors	ConcertoConnectors	VAR-SOM-MX6	VAR-SOM-MX8	VAR-SOM-MX8X	VAR-SOM-MX8MM	VAR-SOM-MX8MN	VAR-SOM-MX8MP	VAR-SOM...
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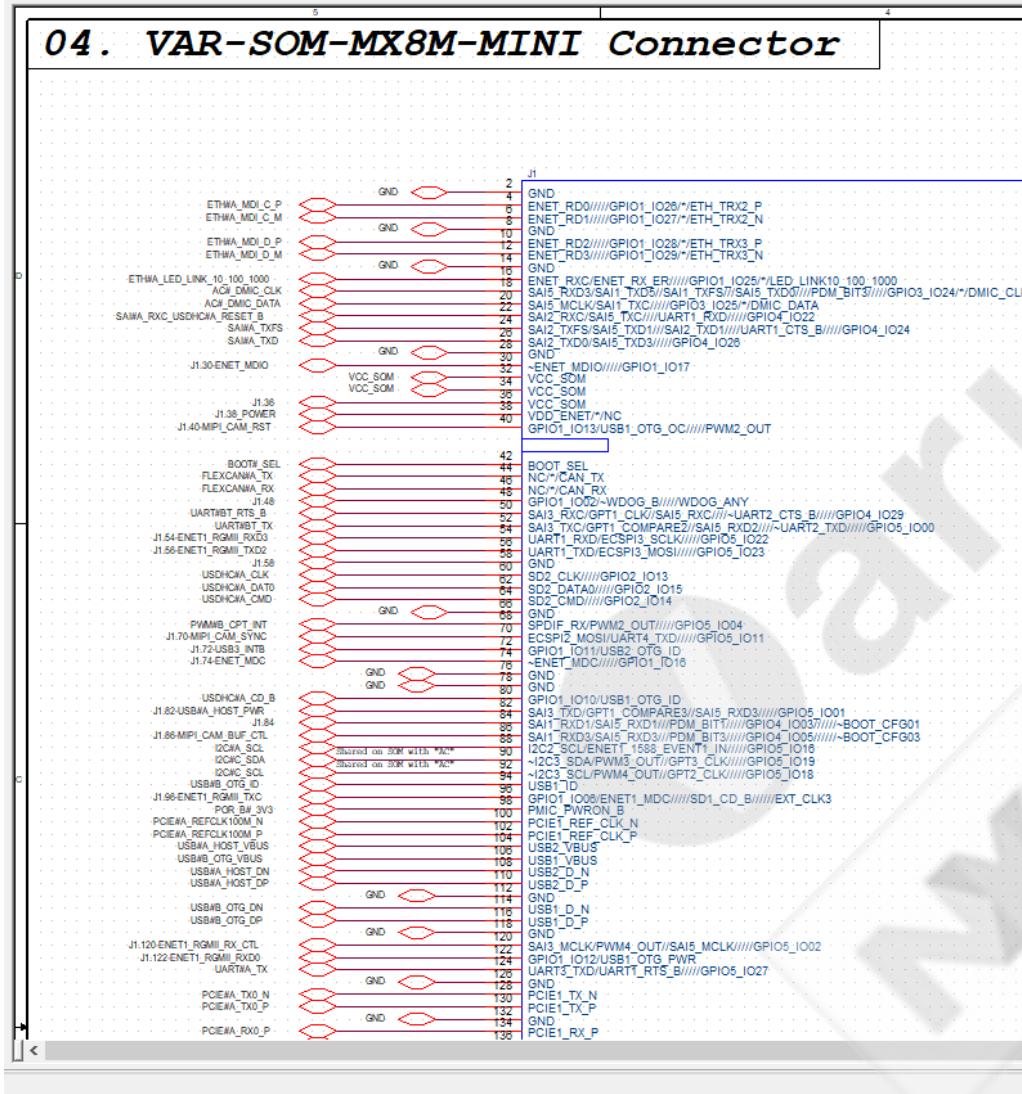
# Carrier board design– Symphony-Board introduction

# An Overview of the Symphony-Board schematics

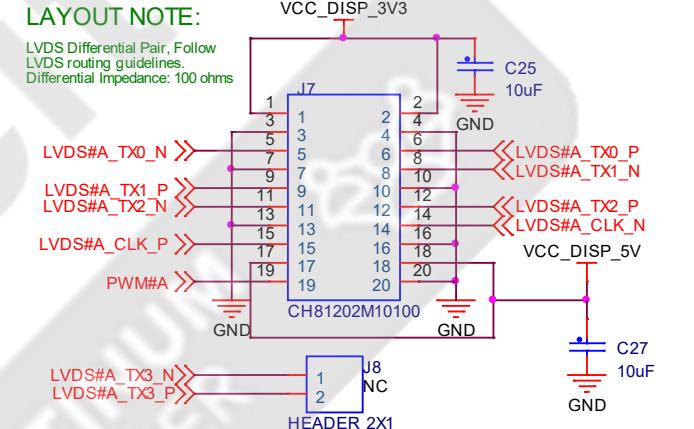


# Carrier board design– Symphony-Board introduction

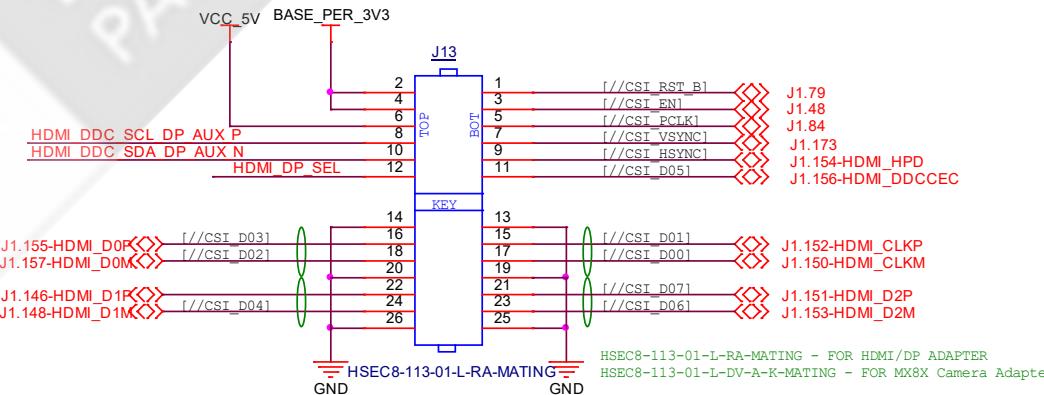
The Symphony-Board Schematics Hierarchy includes the dedicated Schematic page for all SOMs.  
Off-page connectors naming follow index denoted on SOM page



## LVDS DISPLAY A



## MX6/MX8-HDMI , MX8-DP , MX8X-CSI



# Carrier board design guidelines/recommendations – Schematics

- Start the design by adopting the EVK pinmux selection as a baseline for the common required interfaces and go along adding additional interfaces from the available pins as required.
- When using SOM pins for alternate functions not demonstrated in EVK, verify pins are not used internally by SOM for other functions.  
Refer to the SOM datasheet Pinout tables.
- Some incompatibility may exist between SOM pinouts. The EVK schematics has dealt with most common ones, follow it.

## 8.23.3.1. Power up sequence

Figure 6 illustrates the timing relationship between VCC\_SOM and SOM\_3V3\_PER to the internal (not exposed) POR\_B and boot configuration pins drive.

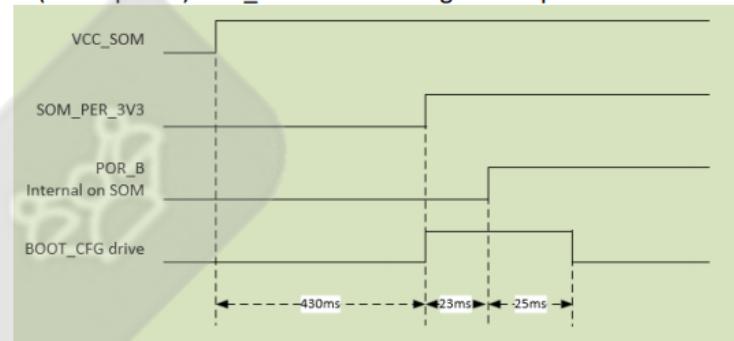


Figure 6 : VAR-SOM-MX8M-MINI power up timing

Figure 7 illustrates cold reset following PMIC\_PWRON\_B going low for >10ms debounce time.

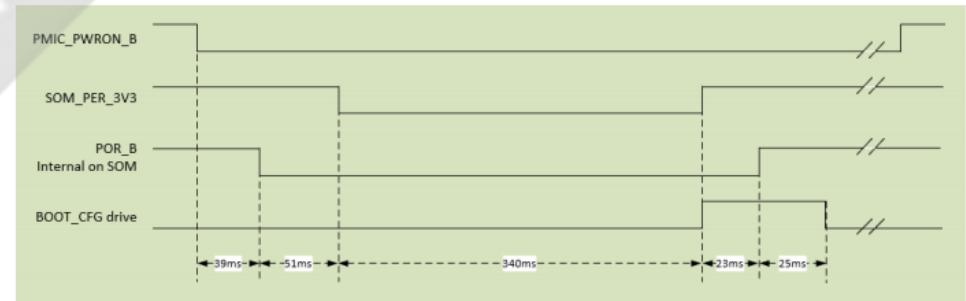


Figure 7 : VAR-SOM-MX8M-MINI Cold Reset Timing

VAR-SOM-MX8M-MINI\_V1.x Datasheet

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Rev. 1.04, 04/2020

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# Carrier board design guidelines/recommendations – Schematics

- Follow as much as possible EVK portions related to Power, reset and boot.
  - Boot pins - Verify pins are not driven externally to an undesirable state
  - Reset - Verify handling of POR signal in your carrier board
  - Power -
    - Ensure sufficient supply to module
    - Depending on Power supply proximity, add bulk capacitance for SOM power supply pins
    - Pay attention to design of Carrier board peripherals 3.3V supply and the carrier board power rails discharge
- USB – verify connections of VBUS, ID signals
- Add ESD and EMI protection devices on sensitive Interfaces

## 8.23.3.1. Power up sequence

Figure 6 illustrates the timing relationship between VCC\_SOM and SOM\_3V3\_PER to the internal (not exposed) POR\_B and boot configuration pins drive.

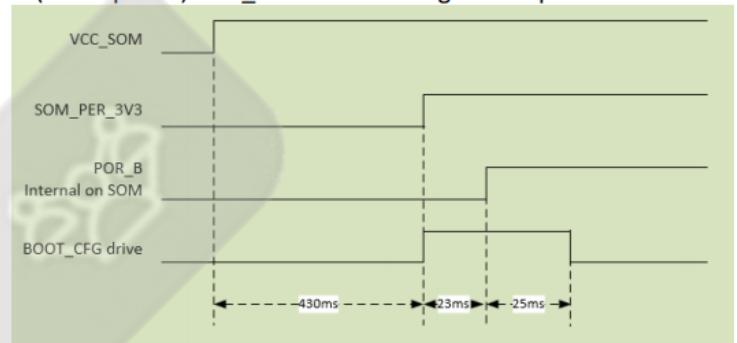


Figure 6 : VAR-SOM-MX8M-MINI power up timing

Figure 7 illustrates cold reset following PMIC\_PWRON\_B going low for >10ms debounce time.

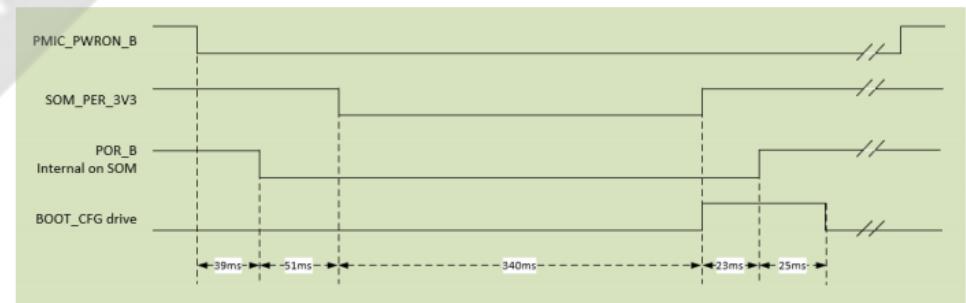


Figure 7 : VAR-SOM-MX8M-MINI Cold Reset Timing

VAR-SOM-MX8M-MINI\_V1.x Datasheet

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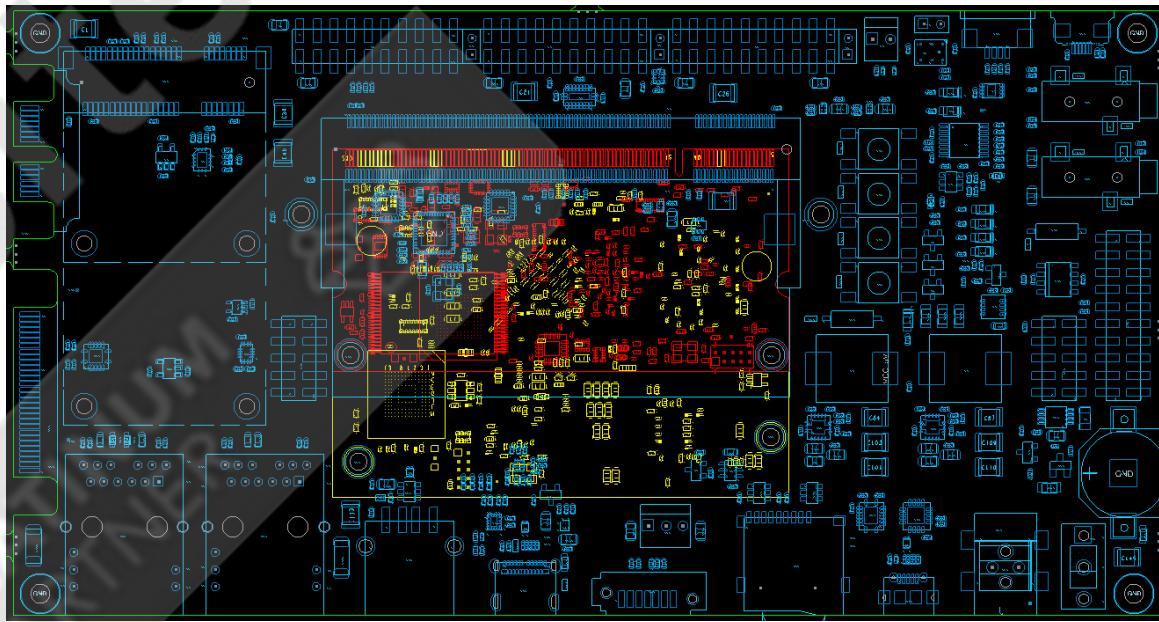
# Carrier board design - Layout

## Placement

- Verify SOM and holes' placement using reference design files
- When placing components under SOM check Height constraints
- Try to minimize distance of High speed interfaces connectors from SOM pins
- Place bulk capacitance of SOM power supply near SOM pins

## Stackup

- Suggest using a minimum of 6 layer stackup
- Work with your PCB manufacture to achieve a stackup which provides all impedances with practical trace width/spacing dimensions and reference planes for high speed signals



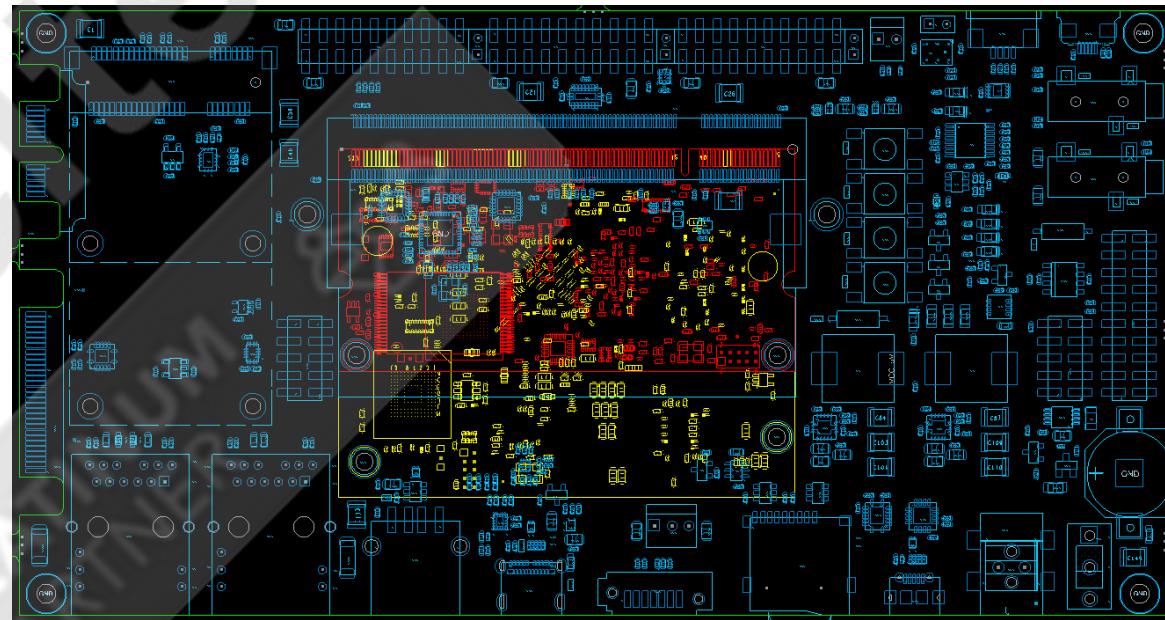
# Carrier board design - Layout

## Routing

- Give priority to High speed signals such as PCI, USB 3.0, LVDS and HDMI
- Make effort to route high speed buses as a group in same layer
- length match signals of same bus, match intra pair (Positive/Negative) signals of differential pairs
- Ensure a continuous reference plane for impedance controlled signals
- Minimize crosstalk between high speed interfaces
- Keep high speed/sensitive signals away from noisy lines

## Power

- Follow placement and routing guidelines of power supplies to reduce noise avoid EMC issues
- Use short thick connections
- Use multiple vias to connect between planes



# Carrier board design – useful links

Design source files are available on our FTP:

<ftp://customerv:Variscite1@ftp.variscite.com/VAR-SOM-MX8/Hardware/Symphony-Board/V1.3A>

Mechanical 2D/3D files of SOM/carrier boards can be found under documentation tab of SOM/carrier boards page in variscite website.

SOMs:

<https://www.variscite.com/products/system-on-module-som/>

Carrier boards:

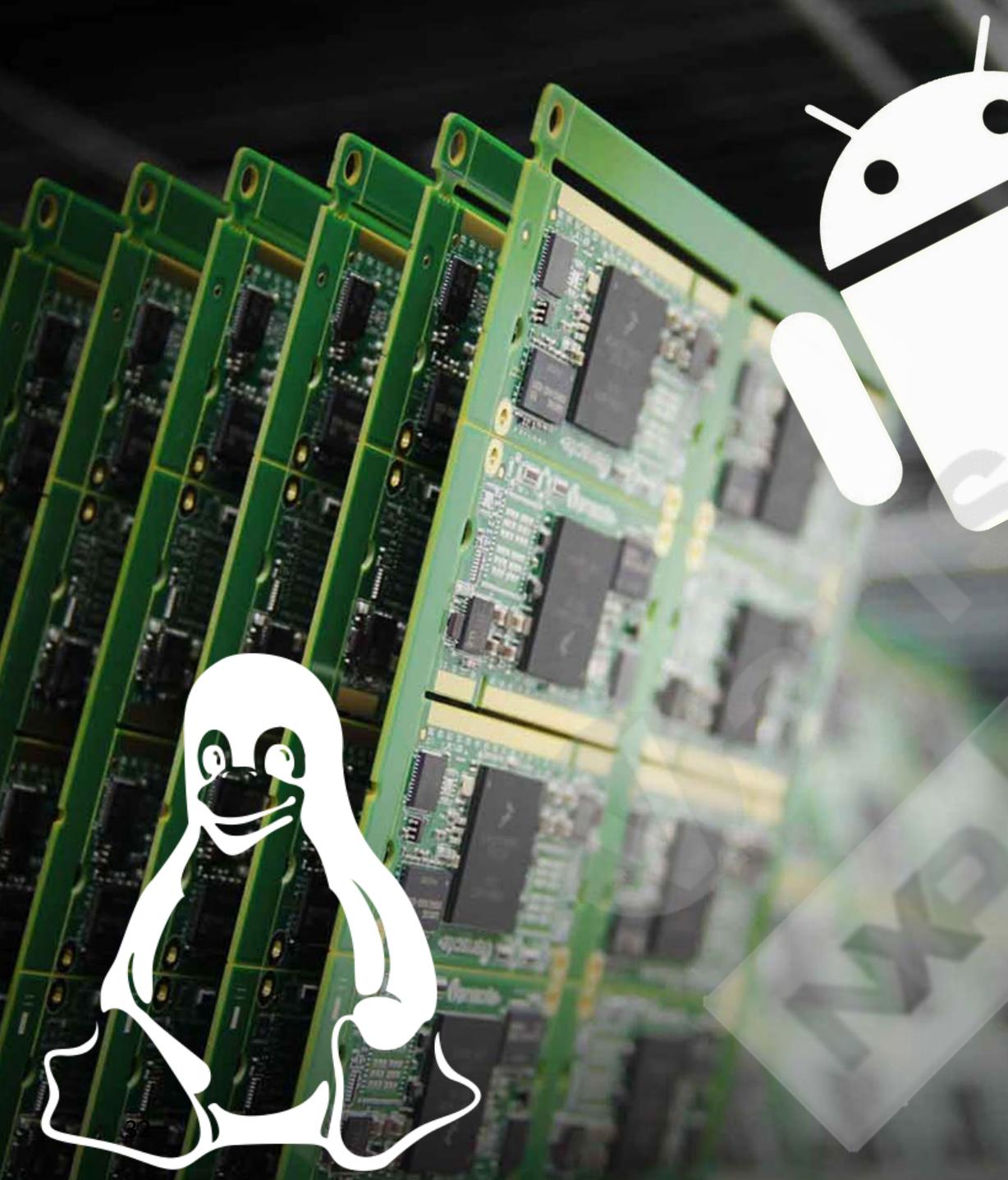
<https://www.variscite.com/products/single-board-computers/>

# Webinar Agenda

- The System-on-Module concept for a scalable design
- NXP's i.MX 8 product portfolio
- Variscite pin-to-pin System-on-Module families
- How to design a scalable embedded product supporting various i.MX processors:
  - Hardware aspects
  - Software aspects
  - Q&As

Pierluigi Passaro, R&D Software expert, Variscite





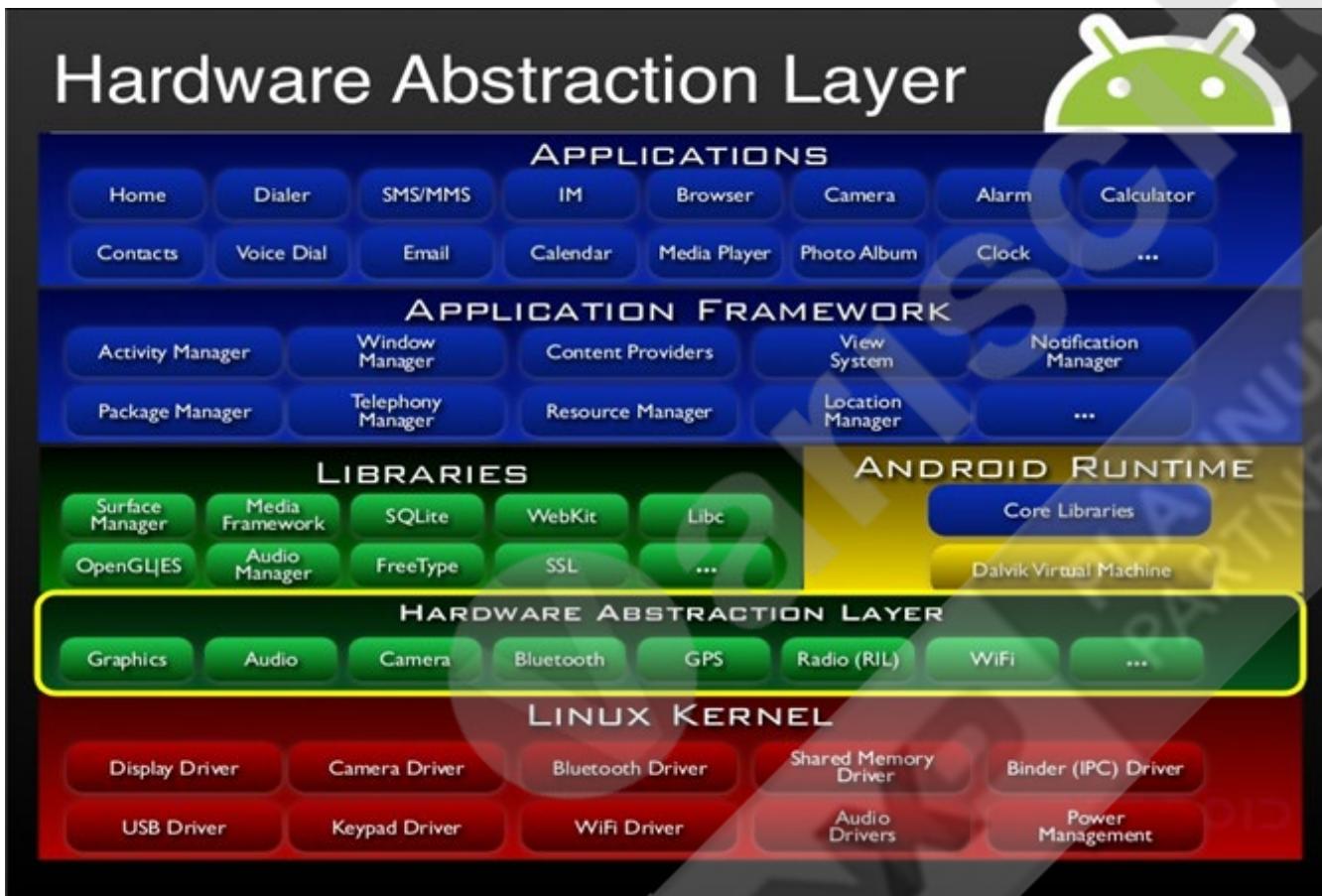
## SW scalability

- Scalability definitions
- Android approach
- Linux kernel HAL
- Wrapper libraries
- Application design

# System vs Software scalability

- System scalability
  - capability of a system to adapt and fit to specific problems
- Software scalability
  - capability of a software to correctly manage an increased workload (users)
- Variscite SoM scalability
  - capability to run the same application on the same board while using different SoMs

# Android approach: the HAL



- 1 SDK
- 1 apk
- several devices

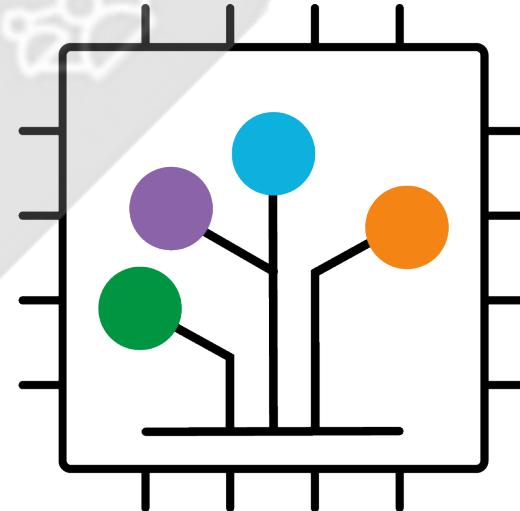
# Android SDK limitations

- No direct access to HW busses
  - GPIO
  - I2C
  - SPI
  - UART
  - USB
- Designed to limit user access to HW: Android SDK focus on devices functionalities
  - LEDs/keys (GPIO)
  - Audio (I2C)
  - Sensors (SPI)
  - Bluetooth (UART)
  - Cameras (USB)

# HAL requirements for Linux kernel

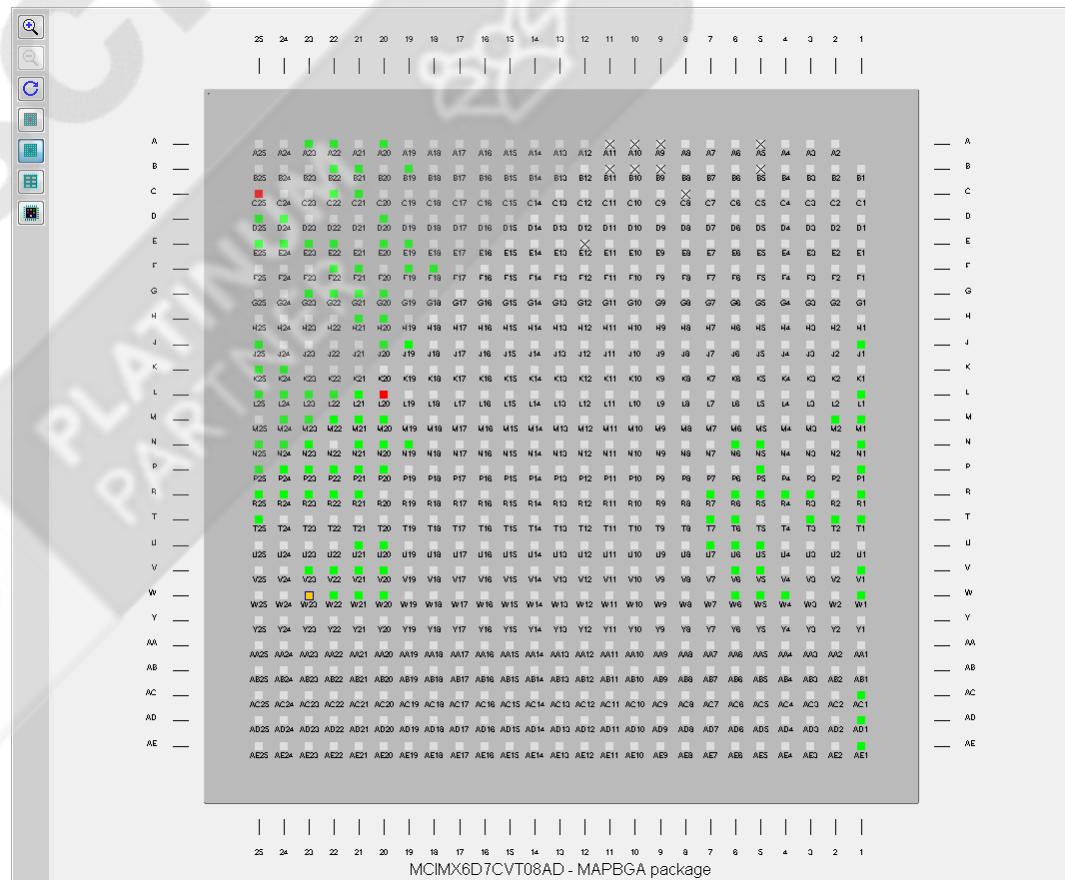
- Availability of drivers exposing standard interfaces
  - Audio
  - Power supply
  - Touchscreens
- Device trees exposing standard interfaces

```
backlight: backlight {  
    compatible = "pwm-backlight";  
    pwms = <&pwm1 0 1000000 0>;  
    brightness-levels = <0 1 2 3 4 5 6 7>;  
    default-brightness-level = <8>;  
    status = "ok";  
};
```



# Variscite Device tree design: resource availability

- Expose the same interfaces using the same SoM pins
- NXP pinmuxing
  - SymphonyBoard J18.3/5 provide UARTs
    - VAR-SOM-MX8M-MINI
    - VAR-SOM-MX8M-NANO
    - VAR-SOM-MX8X
    - VAR-SOM-MX8



# Customer Device tree design: avoid using low level GPIOs

- gpio-keys: allow exposing key events instead of GPIO indexes
- gpio-leds: allow exposing symbolic names to set GPIO status

```
gpio-keys {  
    compatible = "gpio-keys";  
    pinctrl-names = "default";  
    pinctrl-0 = <&pinctrl_gpio_keys>;  
  
    up {  
        label = "Up";  
        gpios = <&gpio4 18 GPIO_ACTIVE_LOW>;  
        linux,code = <KEY_UP>;  
    };  
};
```

```
gpio-leds {  
    compatible = "gpio-leds";  
    pinctrl-names = "default";  
    pinctrl-0 = <&pinctrl_leds>;  
  
    emmc {  
        label = "eMMC";  
        gpios = <&gpio4 17 GPIO_ACTIVE_HIGH>;  
        linux,default-trigger = "mmc0";  
    };  
};
```

# Customer Device tree design: avoid I2C / SPI raw access

- Use dedicated kernel drivers for devices connected to the busses -  
This will provide standard interfaces regardless of the used bus

```
&i2c2 {  
    clock-frequency = <100000>;  
    pinctrl-names = "default";  
    pinctrl-0 = <&pinctrl_i2c2>;  
    status = "okay";  
  
    /* DS1337 RTC module */  
    rtc@0x68 {  
        status = "okay";  
        compatible = "dallas,ds1337";  
        reg = <0x68>;  
        pinctrl-names = "default";  
        pinctrl-0 = <&pinctrl_rtc>;  
        interrupt-parent = <&gpio1>;  
        interrupts = <15 IRQ_TYPE_EDGE_FALLING>;  
    };  
};
```

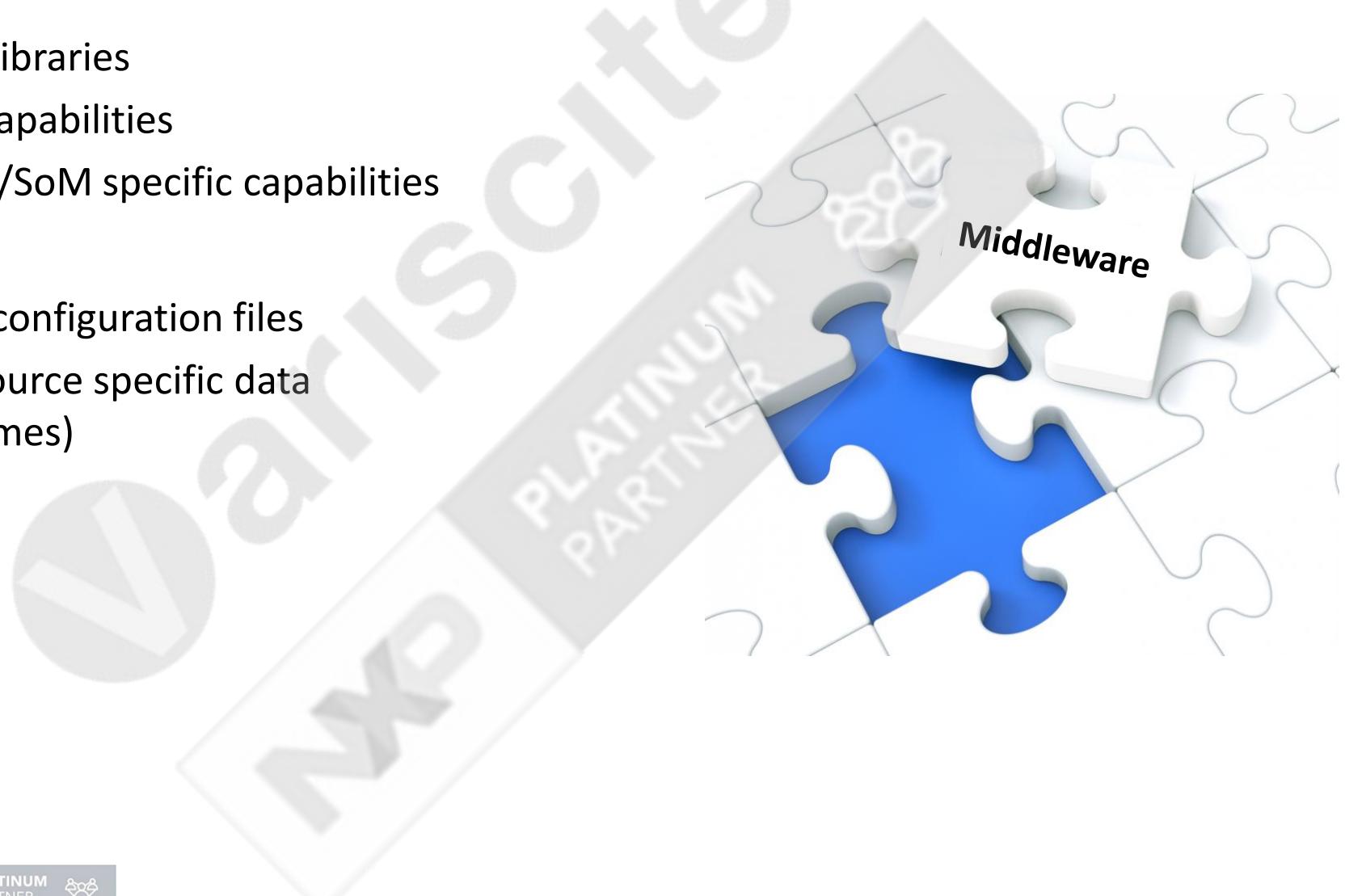
# Device tree limitations

- Missing resources (Second Ethernet port, GPU, VPU, ...)
- Different device naming (UARTs)
  - SymphonyBoard J18.3/5 provide UARTs
    - VAR-SOM-MX8M-MINI => ttymxc2
    - VAR-SOM-MX8M-NANO => ttymxc2
    - VAR-SOM-MX8X => ttylp1
    - VAR-SOM-MX8 => ttylp2



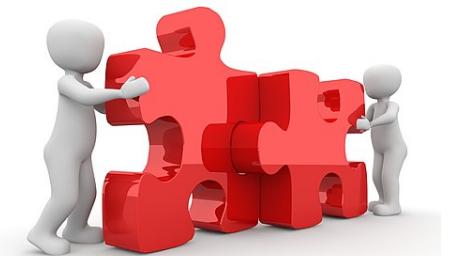
# middleware: user-space HAL

- Design dedicated libraries
  - probing HW capabilities
  - providing SoC/SoM specific capabilities
- Design dedicated configuration files
  - providing resource specific data  
(like UART names)



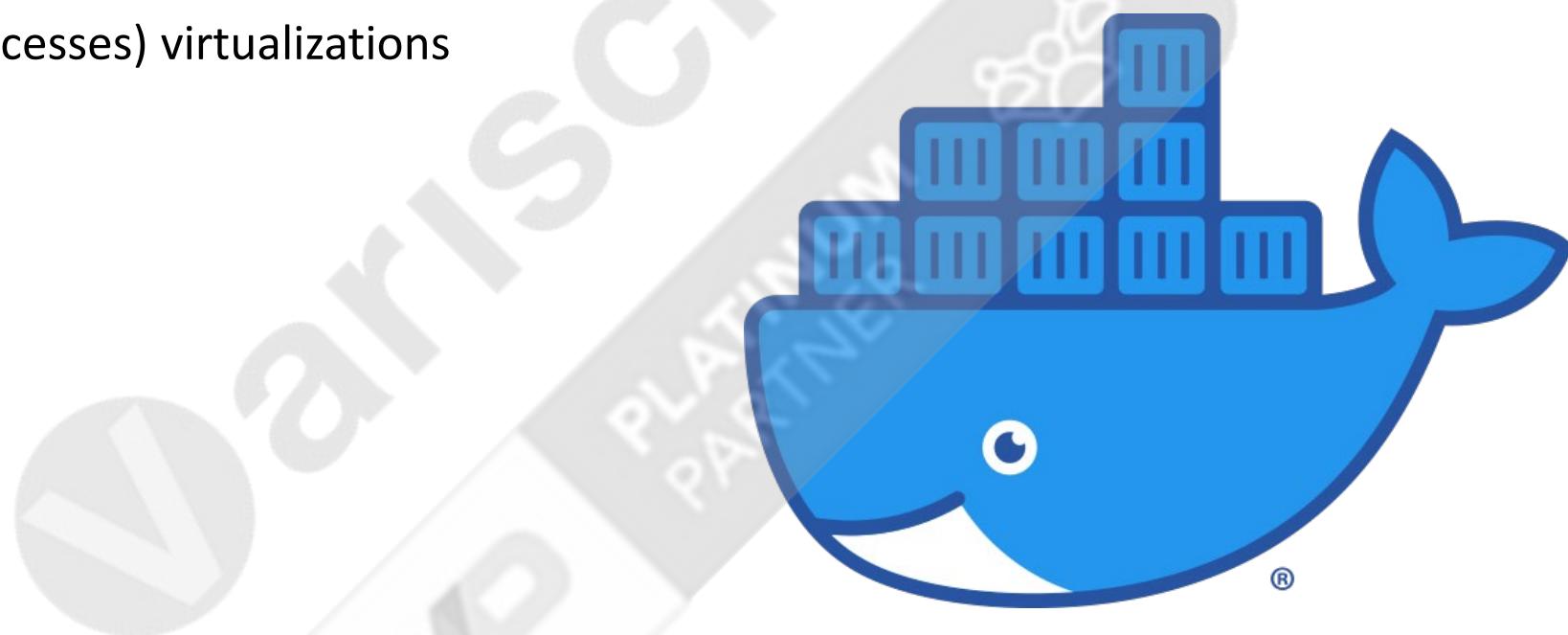
# Application design

- No HW dependencies
- Develop and test the application on a specific SoM (or even on a Linux PC)
- Not just HW scalability (one board / several SoMs)
- Not just SW scalability (one applications / several SoMs)
- Simultaneous HW/SW scalability (one board, one application / several SoMs)



# Beyond HW/SW scalability

- Docker containers
  - Devices virtualization
  - Resource (processes) virtualizations



# Contact Information

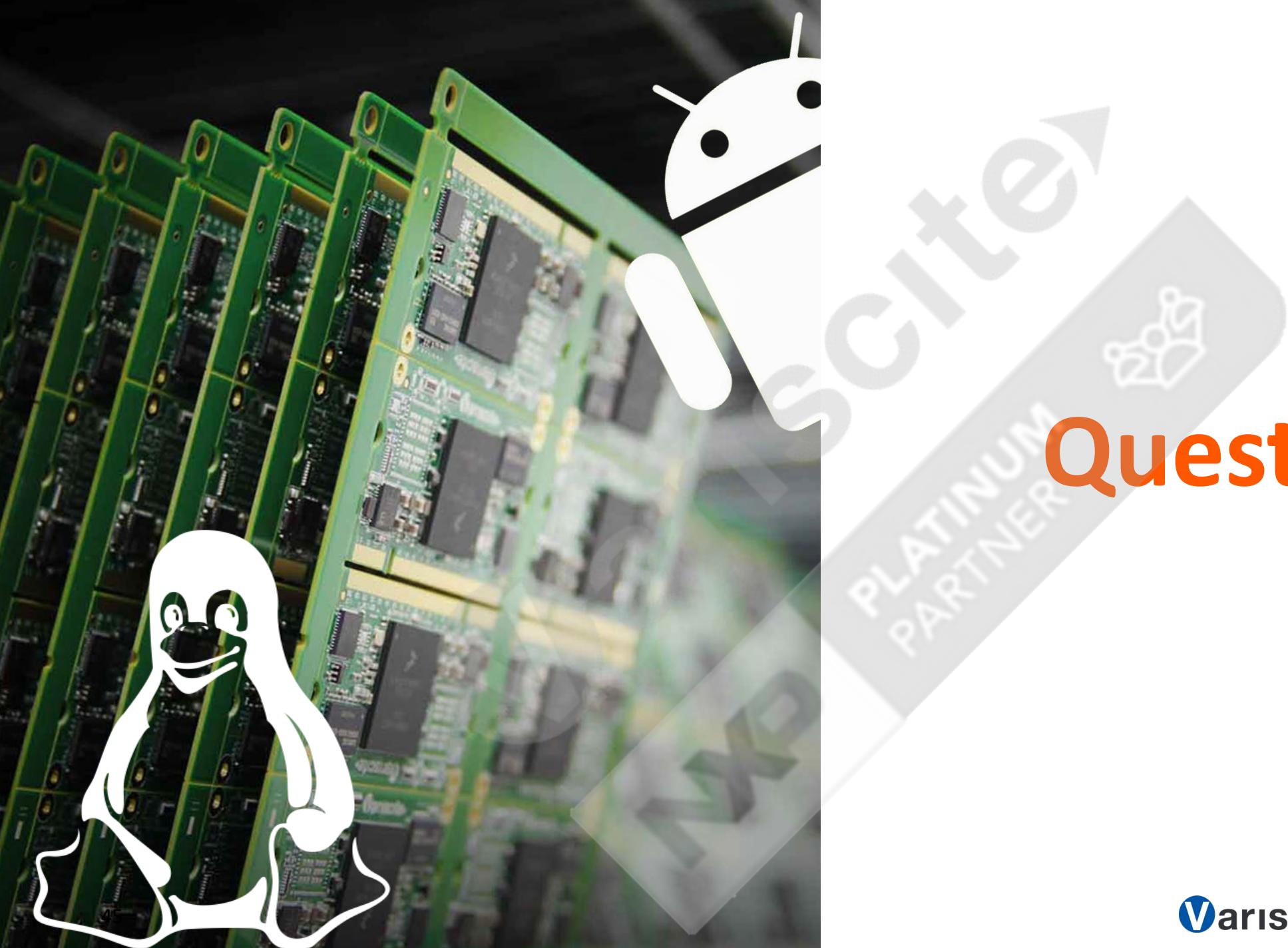
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Website | [www.variscite.com](http://www.variscite.com)

Variscite wiki | [www.variwiki.com](http://www.variwiki.com)

Customer Portal | [Variscite Portal](#)





# Questions?

# THANK YOU!



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