

Symphony-Board



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Disclaimer:

Schematics are for reference only.
Variscite LTD provides no warranty for the use of these schematics.
Schematics are subject to change without notice.

Revision History

Document	Carrier
1.0	1.0 Initial
1.1	1.1 Released
1.2	<ul style="list-style-type: none"> 1.1 Updated Block Diagrams Added SH1 wire short symbol Updated Compatibility value for SOM pins 68,69,176 Updated SOM pin 22 net name Fixed U22_B1, C113.1 net name Fixed R1-R2,R35-R38 net name
1.3	<ul style="list-style-type: none"> 1.2 Removed SH1 wire short, J1_68 routed to capacitive touch Changed R22 to C185 Changed R123,R127 to N.C. Added resistors R130-132 Removed ADC, INxx alternate function from VAR-SOM-MX8 Symbol Updated PCIe resistor assembly note
1.4	<ul style="list-style-type: none"> 1.2 Updated Parallel Camera/HDMI/DP Note Fixed ETH pin names VAR-SOM-MX8x Symbol
1.5	1.2A Disconnected R129
1.6	1.2A Added VAR-SOM-MX8M-MINI Block Diagram and Symbol PRE-RELEASE VERSION !!!! Subject to change without notice
1.7	1.2B Fixed VAR-SOM-MX8M-MINI Symbol Changed U29_U30_U31 to P/N: FPF2193 Changed R60 to 47K
1.8	<ul style="list-style-type: none"> 1.2C Update VAR-SOM-MX8M-MINI Symbol to V1.1 with side notes for v1.0B(Early access customers) Update VAR-SOM-MX8M-MINI Block Diagram POR circuit fed by VCC, SOM: see U7 R60 R61 R40 R60 D5 Removed
1.9	1.2D Raise VCC_3V3 to Nominal 3.39V for VAR-SOM-MX8M-MINI/NANO power up threshold voltage requirement of >3.35V
1.10	<ul style="list-style-type: none"> 1.2E Reference for new designs: (changes not implemented in V1.2 BRD) <ul style="list-style-type: none"> * Added x2 footprint for U10 for POR support * Base R60 - 30Ω needed slew rate limit * U7 (Base POR circuit) added CB_WDOG resistor assembly options * U29_U30_U31 - Added assembly note * VAR-SOM-MX8M-NANO pages added with symbol pinout * VAR-SOM-MX8 Connector update - added NC on // assembly options * Power switch in OFF position discharge of Custom rails added * Ethernet PHY clock filter U9 replaced with 49.9 Ohm /0603 resistor * Base RJ45 LEDs matched to SOM behaviour
1.11	1.3 * Added VAR-SOM-MX8M-PLUS Preliminary Symbol and Block Diagram Symbol is Pre-Release Version Subject to change without notice! * All C1210 capacitor footprint updated to C1210_v0 * MS1 to MS6 not assembled
1.12	1.3A <ul style="list-style-type: none"> * ETH1 PHY clock filter U9 replaced with 49.9 Ohm /0603 resistor * Added design note for ETH1 switches U8 and U10.
1.13	1.4 <ul style="list-style-type: none"> * MSS and MS6 location adopted to heatplate design - Layout * Update J1 Manufacturer PN, NAME and footprint to represent the assembled part * Replace PCB AC caps on R2 lines with 0 ohm resistors * Updated U10 analog switch for U10 to U11 swap pins 1 58 80, swap pins 41 43 and 84 147 * U1 Modify Camera connector orientation * Remove U8 U10 analog switches on ETH1 * U9 revert to EMI filter on RGMI, RX clock line * Added RNI RN1 RN3 R151 R136 isolating stubs on ETH1 RGMI signals * U26 footprint updated to U26_v0 * Y1 C66 C67 updated * Support for VAR-SOM-MX8M-GUI boot: - BOOT_MODE=1 - R117 assembled - BOOT_MODE=0 - Added PD R149 - USB# PWR to HOST_J23 always enabled * Remove R39 on pin J1..156 to support SOM-MX8MP 2nd MIPI-CSI Lane2 routing * J3 J30 pinout change
1.14	1.4A <ul style="list-style-type: none"> * Support for VAR-SOM-MX8MP USB OTG - Changed U5_P4 Pull for board identification, U21.9 connected to GPIO: - Changed R43,R130,R106 to N.C. - Changed R44,R132 to Assembled * Changed Q4 P/N from: TPS27082L (EOL) to ->TPS27081A * Updated VAR-SOM-MX8M-PLUS Block Diagram, Symbol pins 36,38 names * Added notes for SOM pins 29,79,84
1.15	1.4A <ul style="list-style-type: none"> * Changes in v1.14/1.4A for R43,R44 were not implemented (part of board identification) and only appear in revision history: board identification implemented via EEPROM U3. Board identification required for QS to identify method of OTG ID used: PTN5150 or GPIO
1.16	1.5 <ul style="list-style-type: none"> * Modified VCC_3V3 to 3.35V nominal for all SOMs. For VAR-SOM-MX8M-MINI/NANO, power up threshold voltage requirement of >3.35V is implemented using Q10.R152 * Added note for VAR-SOM-MX8M-MINI/NANO pin 91
1.17	1.5 <ul style="list-style-type: none"> * Updated note for I2C#B pull up resistors
1.18	1.5 <ul style="list-style-type: none"> * Updated note for PTN36043BX/Y chip
1.19	1.5A <ul style="list-style-type: none"> * Q10 changed to 2N7002P_215 Transistor Q10 changed to 2N7002P to stabilize the SOM voltage in the OFF state. Old transistor leakage current (IDG) changed the feedback current and increased the SOM voltage. 2N7002P does not have SG diode that allowed IDSS to flow into the Gate * SOM Pin 84 Note changed
1.20	1.6 <ul style="list-style-type: none"> Ethernet PHY replaced to ADIN1300 R22,R23,R35,R36 assembled with Ferrite Bead C185 assembled with 10K resistor, R30 not assembled U2 changed to CBTL02043B USB3 crossover switch changed to CBTL02043B
1.21	1.6A <ul style="list-style-type: none"> Due to EOL: U35 changed to NFL18ZT207H1A3D Due to allocation problems: U13 changed to SN65HVD232QDR

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Rev	01_Cover
Customer Document Number	Symphony-Board
Project	Symphony-Board
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Document Rev	1.6
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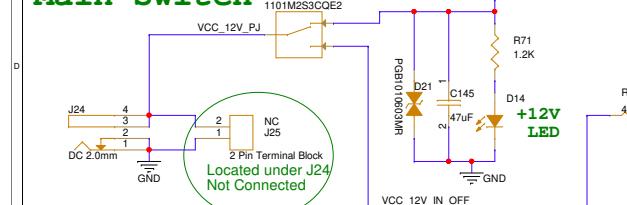
05. Power, Reset, Boot, RTC, EEPROM

POWER DISCHARGE

SOM BOOTSTRAP

12VDC INPUT

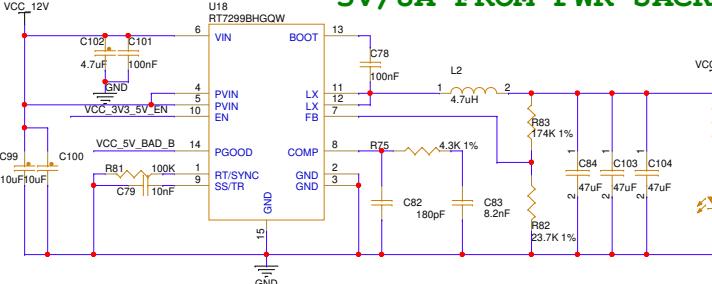
Main Switch



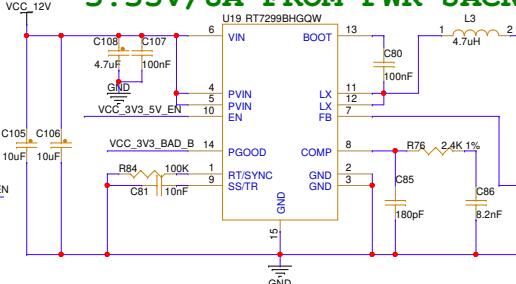
Boot Options:
OFF : INT
ON : SD
Internal boot is from eMMC
MX6 for eMMC boot see additional changes n

For supporting MX6 eMMC boot option:
Remove R9
Assemble R56,R11
Note: Normal configuration is with NAND

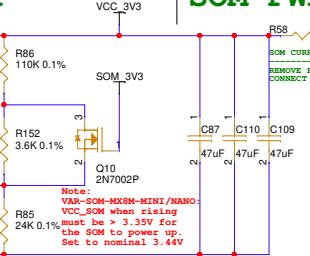
5V/8A FROM PWR JACK



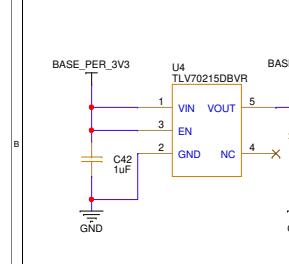
3.35V/8A FROM PWR JACK



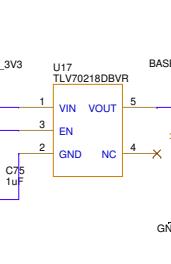
SOM PW



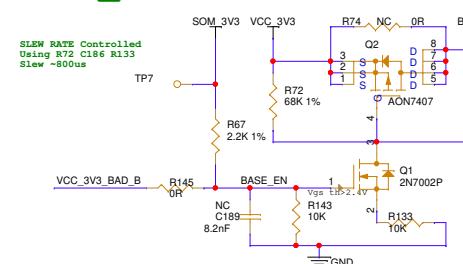
1.5V BASE



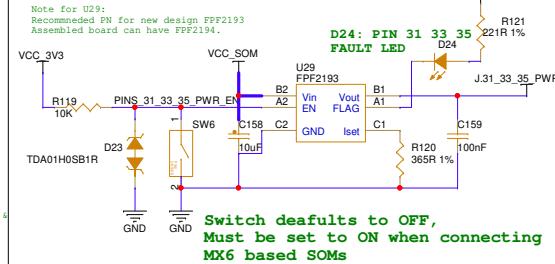
1.8V BASE



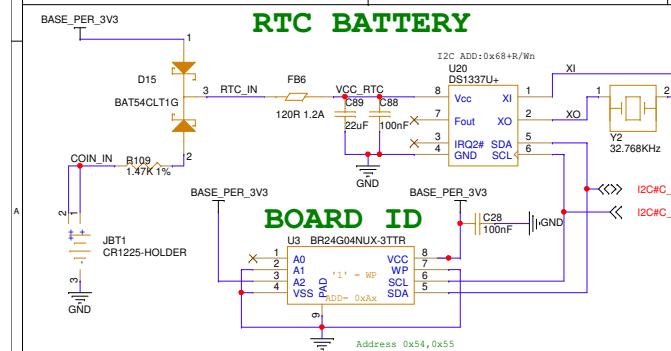
BASE_3V3



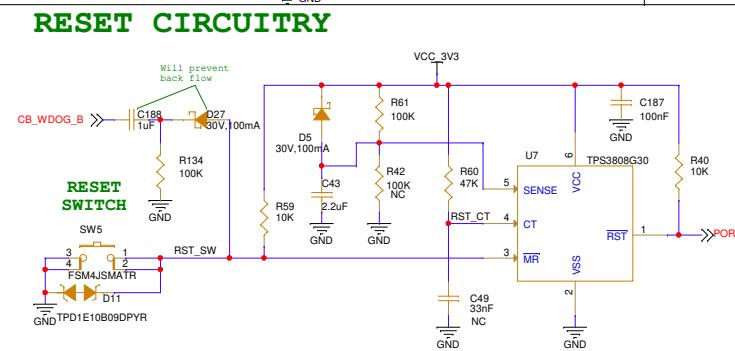
PINS 31 33 35 **POWER**



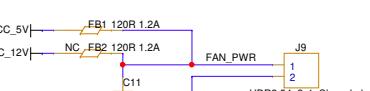
RTC BATTERY



RESET CIRCUITRY



FAN PWR



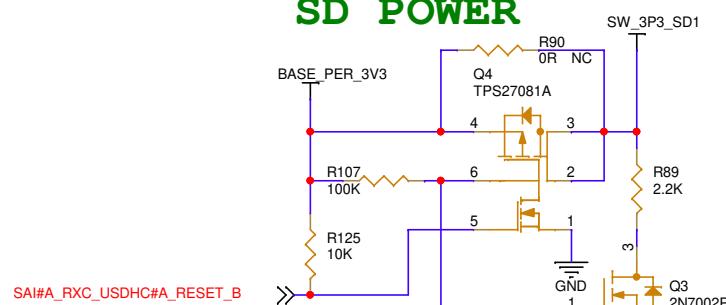
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Title

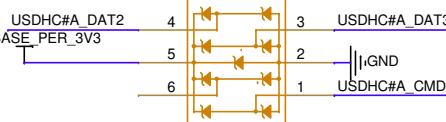
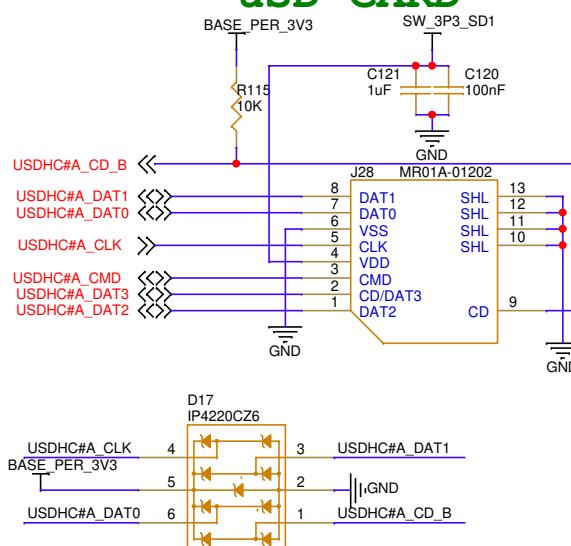
05. Power,Reset,Boot,RTC,EEPROM			
Size A3	Document Number	Project	Rev 1.6A_Rt.21
Designer:	Aviad H.	Approved By:	

06. uSD, Audio, CAN

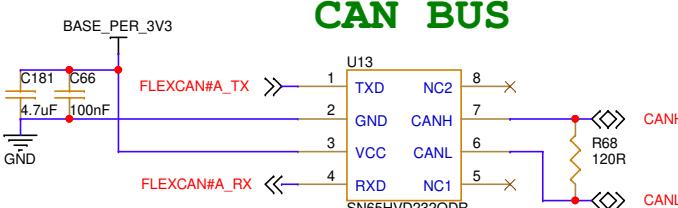
SD POWER



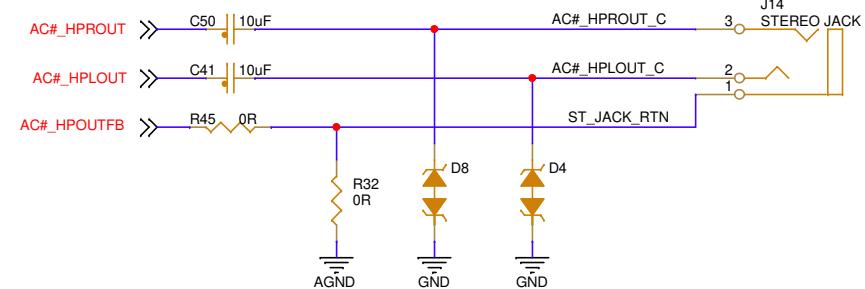
uSD CARD



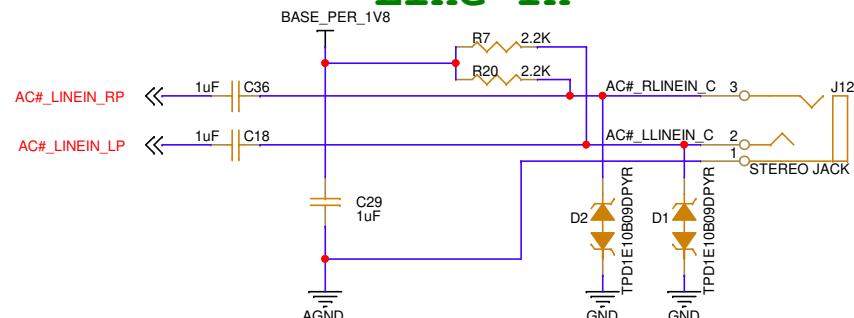
CAN BUS



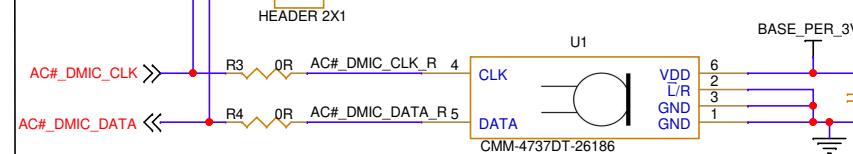
Headphones



Line In



DIGITAL MIC



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Title

06. uSD, Audio,CAN

Size

A4

Document Number

Symphony-Board

Project

Symphony-Board

Rev

1.6A

R1.2

Designer:

Aviad H.

Date:

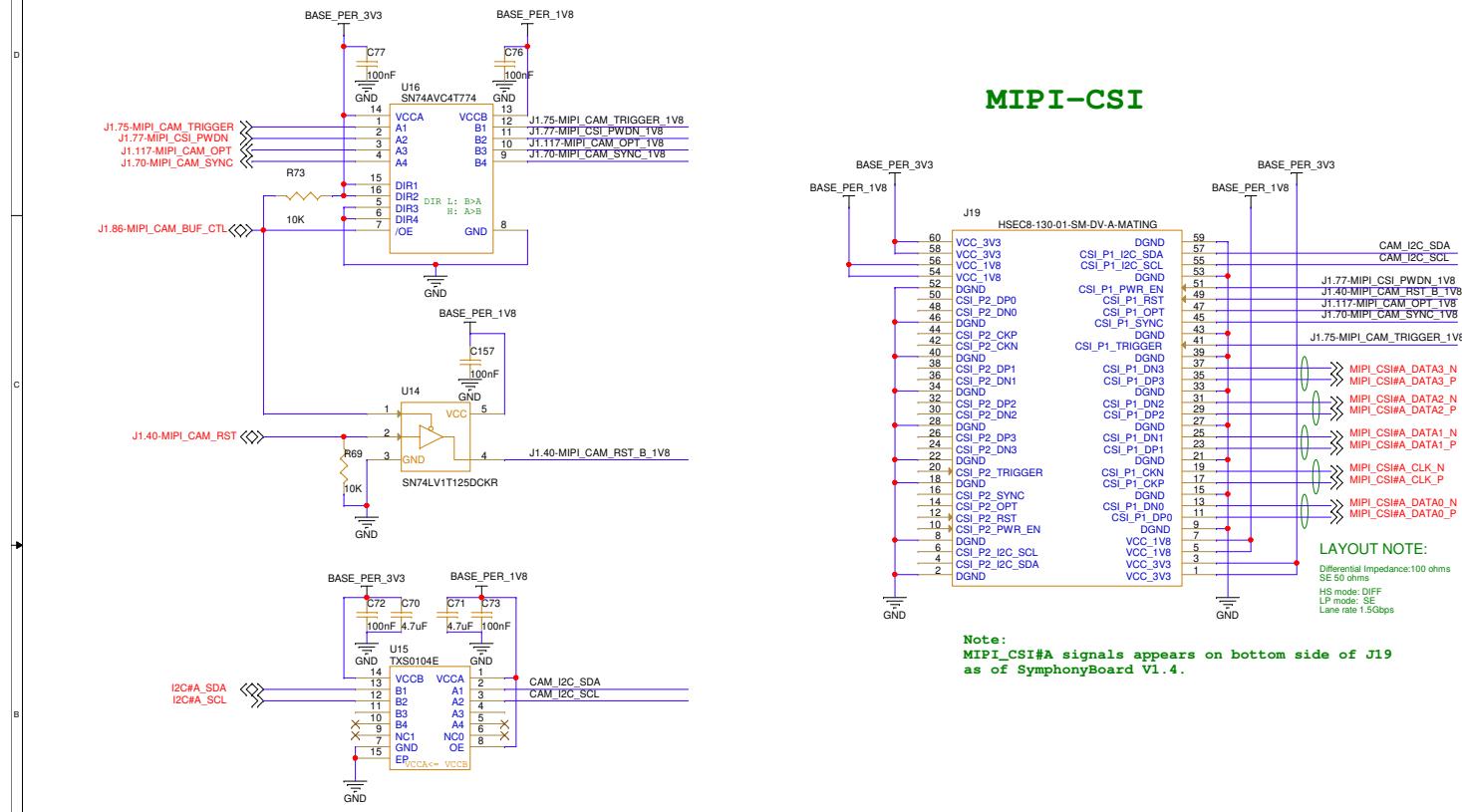
Monday, April 04, 2022

Approved By:

Sheet

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07. Camera, HDMI, DP



Note for U32 (anabg switch):
Switch is to enable support for the following adapters:
Parallel camera, HDMI, DisplayPort and second MIPI-CSI.

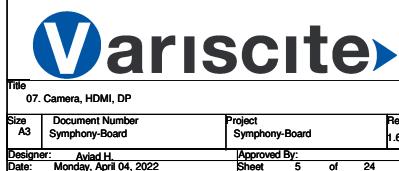
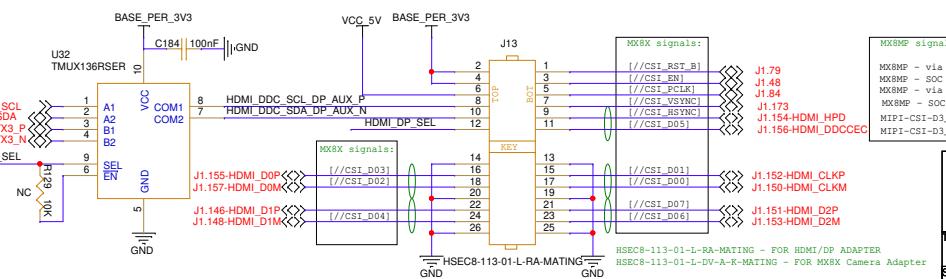
Switch select controlled on adaptor will select between:
1) I2C# which can export

VAR-SOM-MX8X-I2C3 Used by parallel camera
VAR-SOM-MX8: I2C# DDC Used by HDMI (GPIO1_22 in should be set High in SW)

2) LVDS#_TX3 which can export:
VAR-SOM-MX8(DP assembly option): HDMI AUX used by DP

Switch can be omitted when designing for only one of the above interfaces.

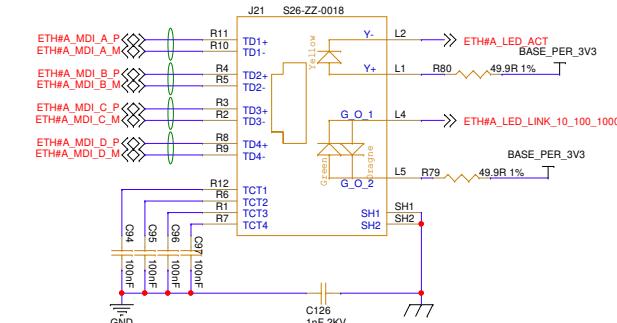
J13: MX6/MX8-HDMI, MX8-DP, MX8X-CSI, MX8MP-2nd MIPI-CSI



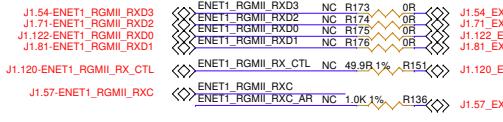
08. Ethernet

Gigabit Ethernet (Internal)

LAYOUT NOTE:
Giga Ethernet Differential Pair,
Follow Giga Ethernet routing
guidelines
Differential Impedance: 100 ohms



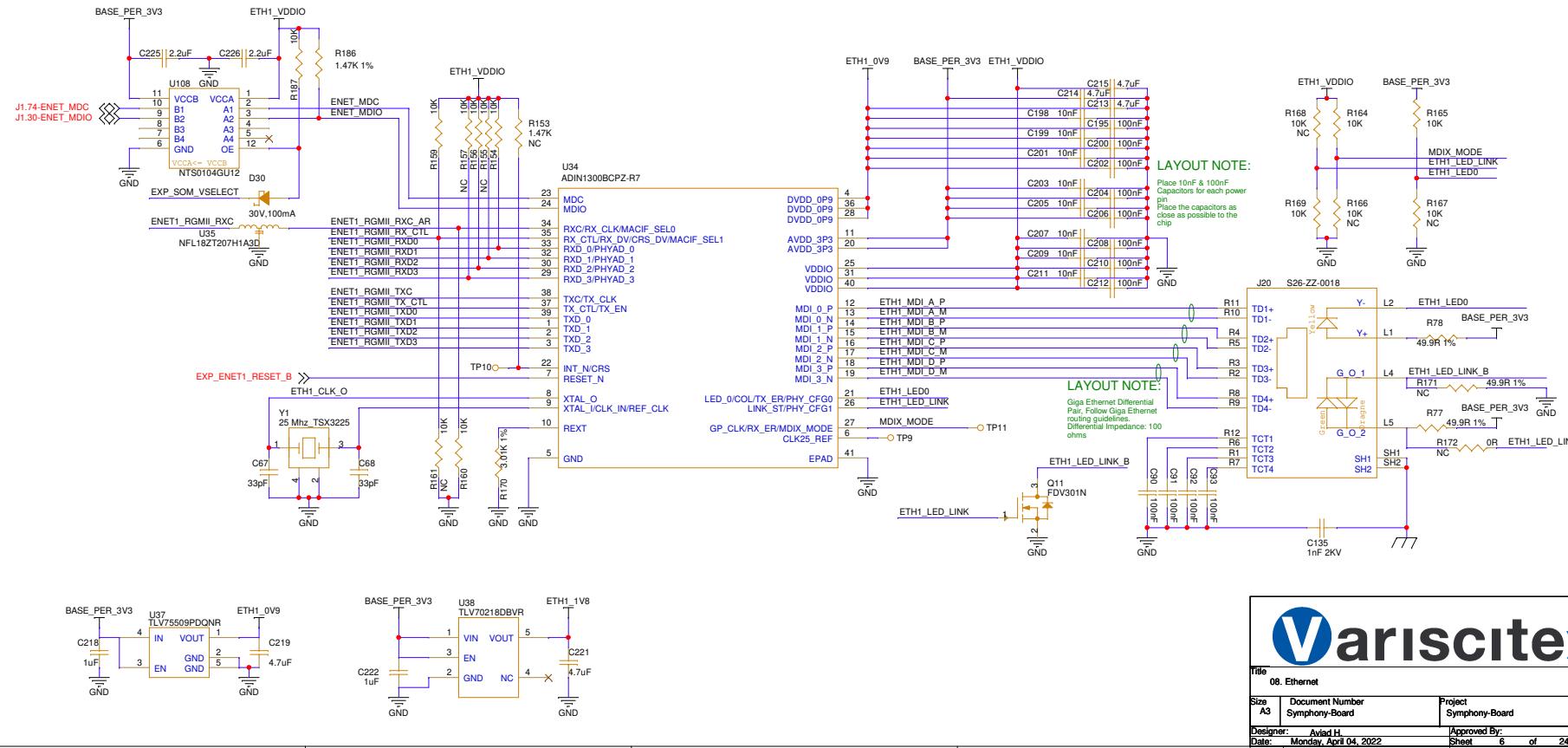
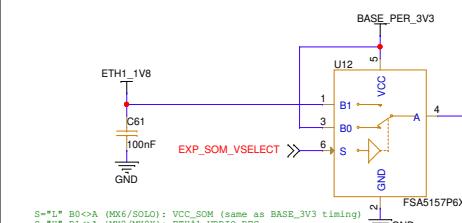
Header/Stub isolation resistors



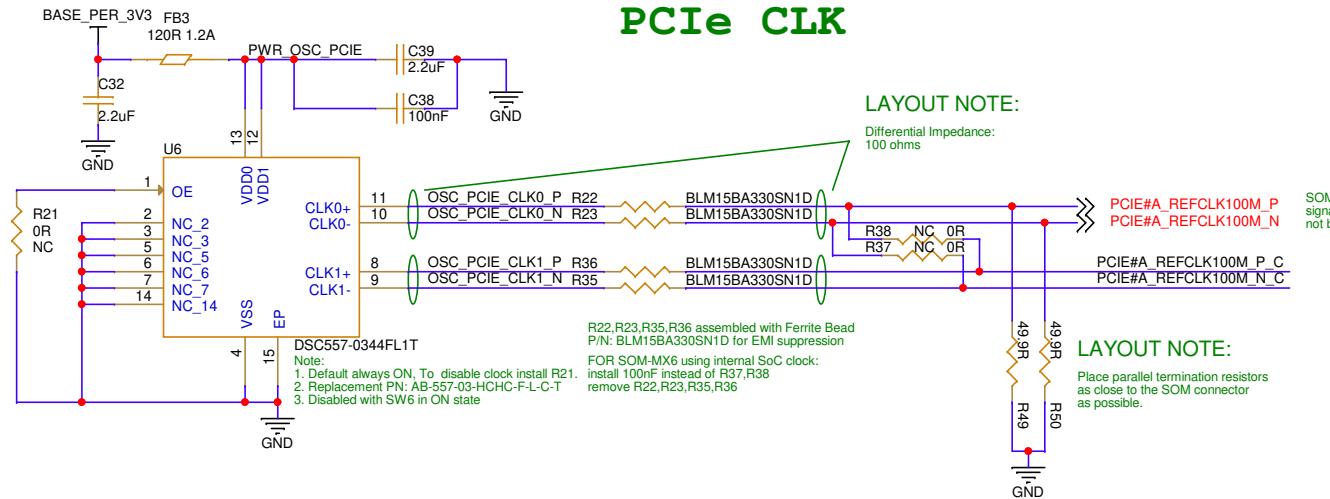
Note:
Customer requiring usage of J30 header (located on bottom side)
should assemble these resistors if not assembled by default

VDD_ENET for SOM-MX8/MX8X/MX8MP

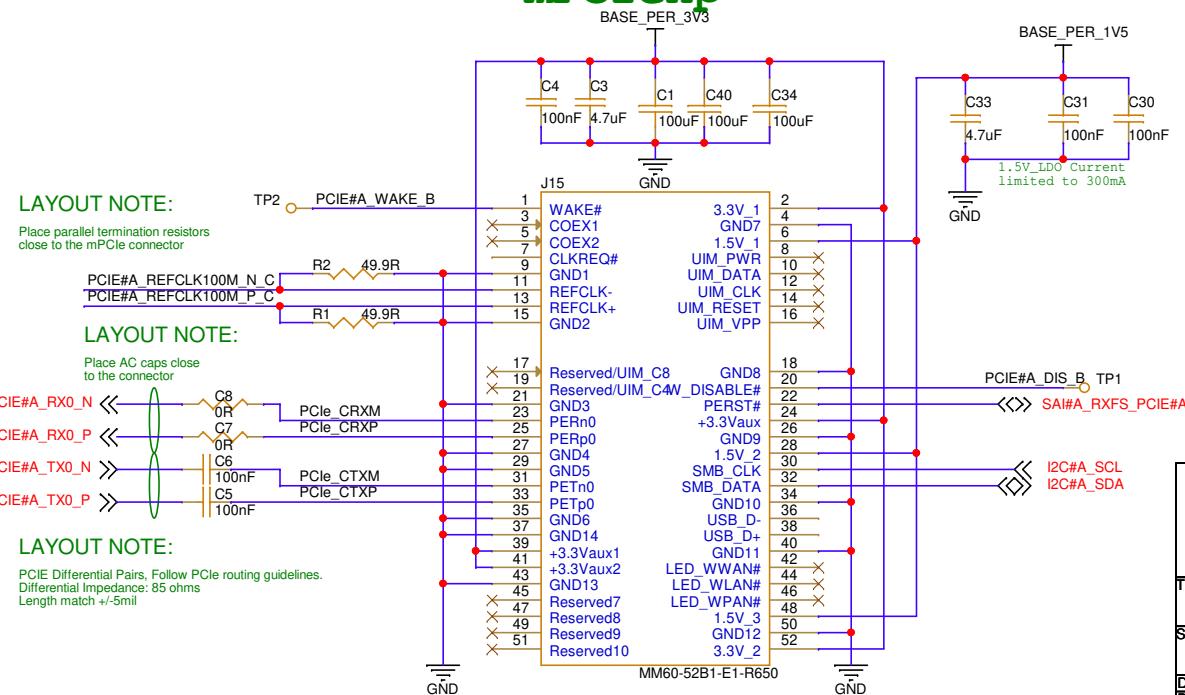
Power for ENET1_RGMII IOs on SOM power fed from pin J1.38
For specific SOM listed above, requiring second ETH port on ENET1 this power should
be set to 1.8V source from U11 PHY



09. PCIe



mPCIexp

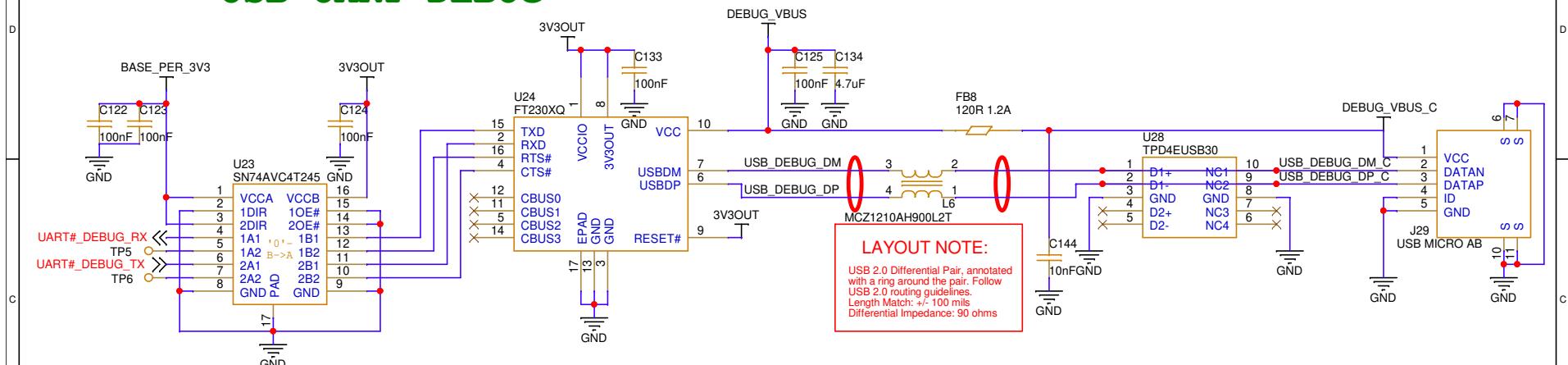


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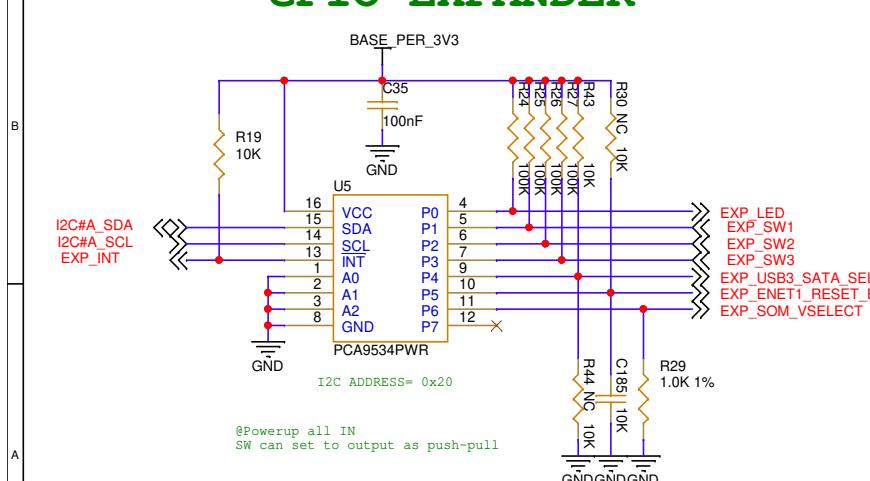
Title 09. PCIe			
Size A4	Document Number Symphony-Board	Project	Rev 1.6A_R1.21
Designer: Aviad H.		Approved By:	
Date: Monday, April 04, 2022	Sheet 7	of 24	

10. Debug, GPIO Exp, Buttons, LED

USB UART DEBUG

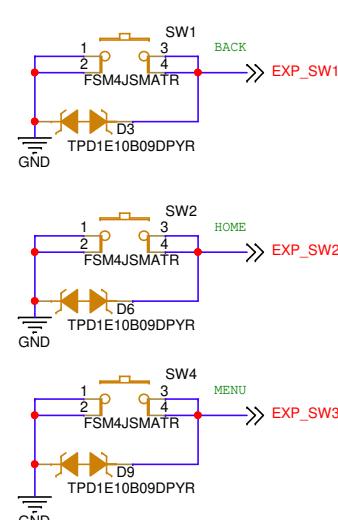


GPIO EXPANDER



In VAR-SOM-MX8 SOM pin 29 EXP_INT is referenced to 1.8V.
When using pin 29 as an input pin driven by higher input voltage,
use an external voltage divider or limit the current using a series resistor to a maximum of 1mA.

GP BUTTON



GP LED

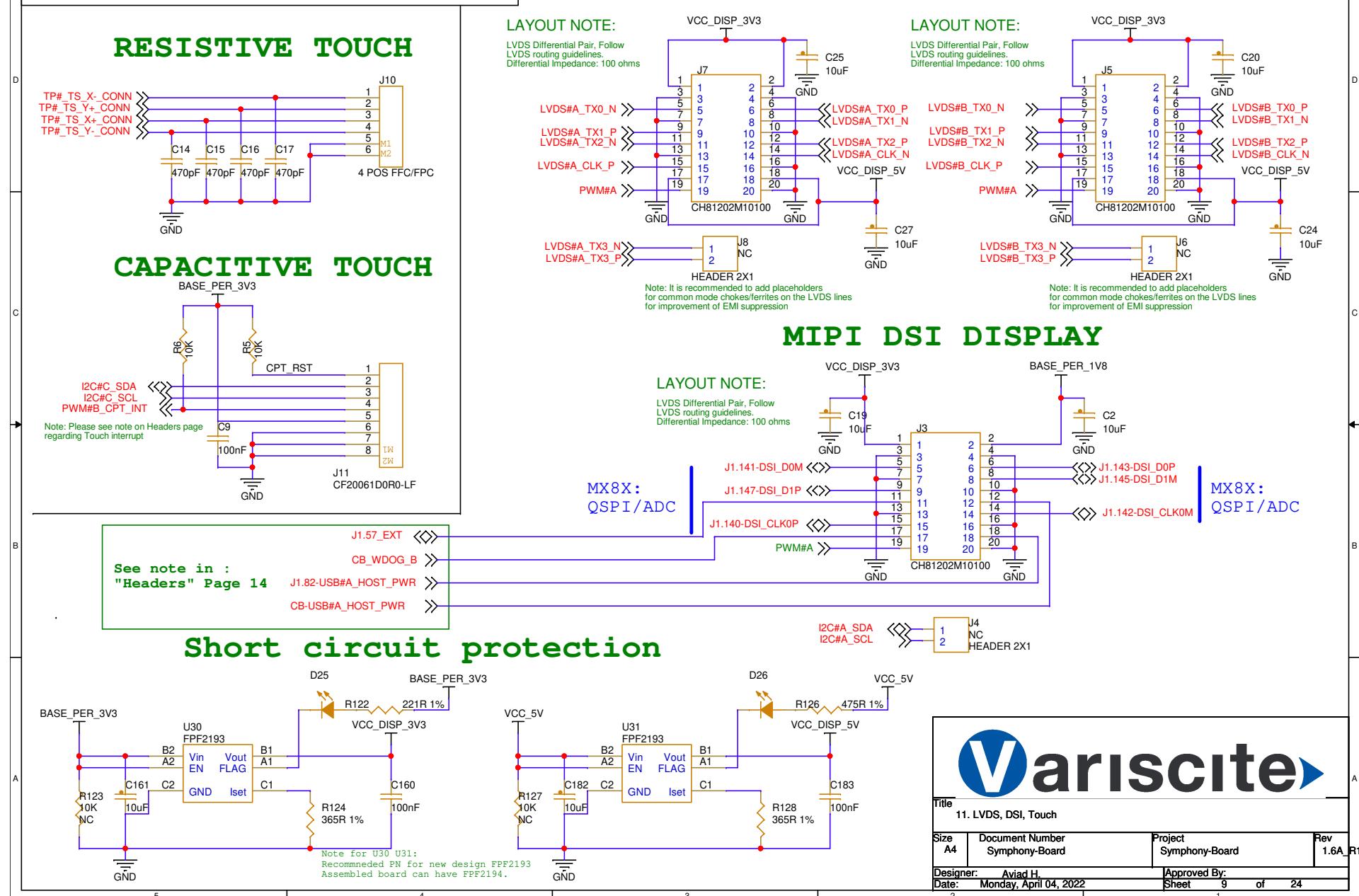


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Title: 10. Debug, GPIO Exp, Buttons, LED

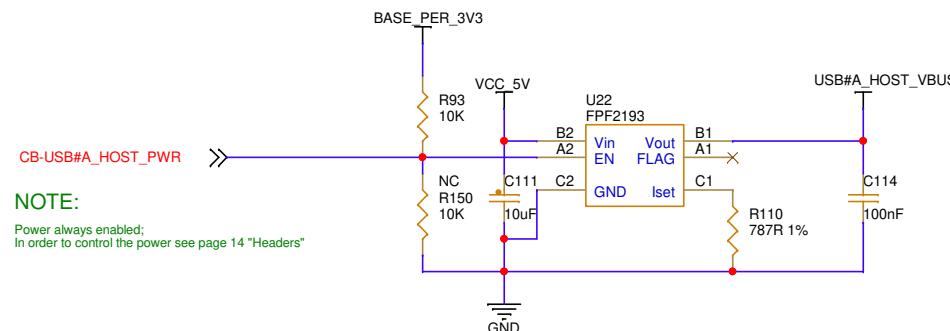
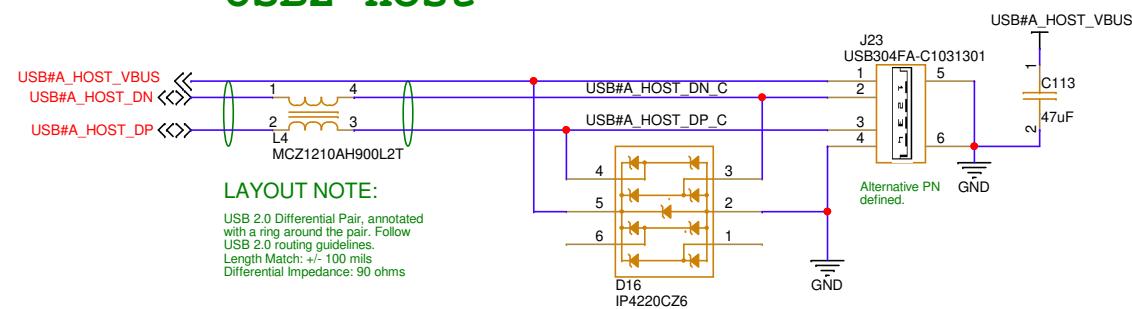
Size	Document Number	Project	Rev
A4	Symphony-Board		1.6A_R1.21
Designer:	Aviad H.	Approved By:	
Date:	Monday, April 04, 2022	Sheet	8 of 24

11. LVDS, DSI, Touch



12. USB2 Host

USB2 Host



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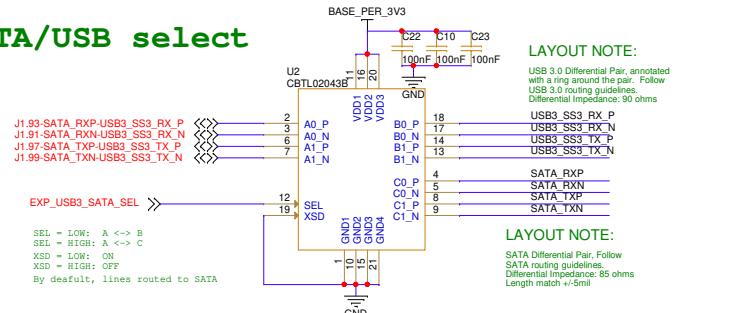
Title

12. USB2 Host

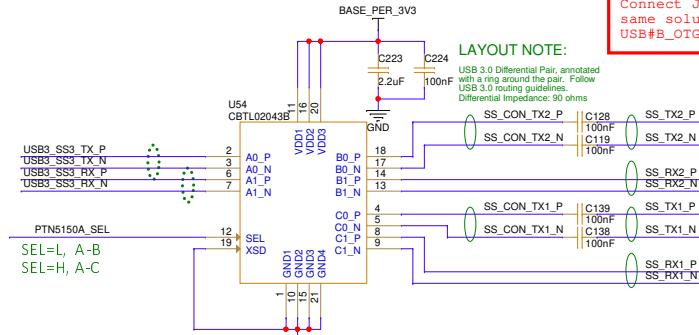
Size	Document Number	Project	Rev
A4	Symphony-Board	Symphony-Board	1.6A R1.2
Designer:	Aviad H.	Approved By:	
Date:	Monday, April 04, 2022	Sheet	10 of 24

13. USB3, uSATA

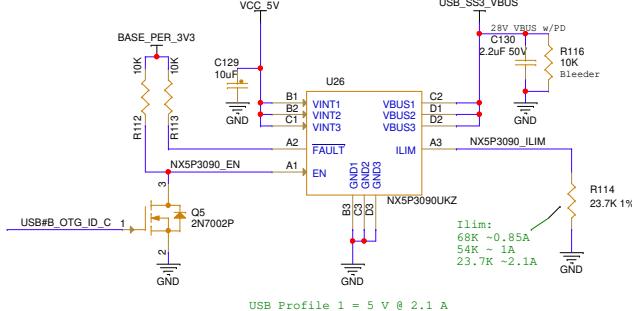
SATA/USB select



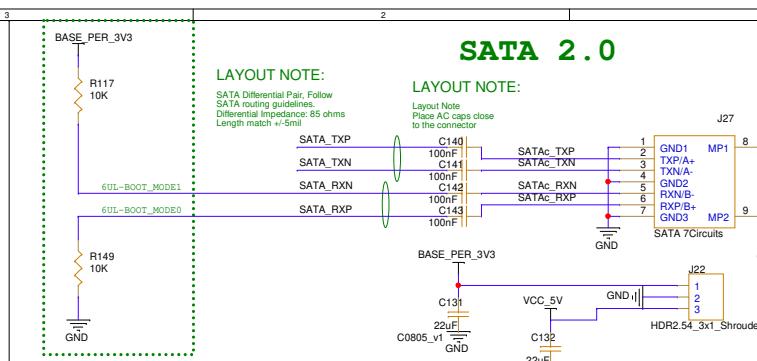
USB TYPE C Circuitry



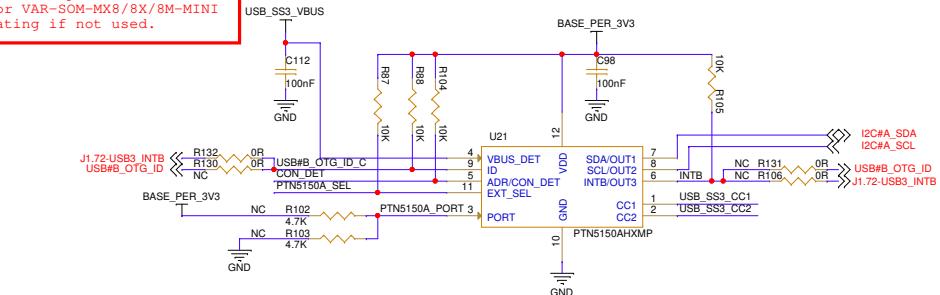
5V Source Load Switch



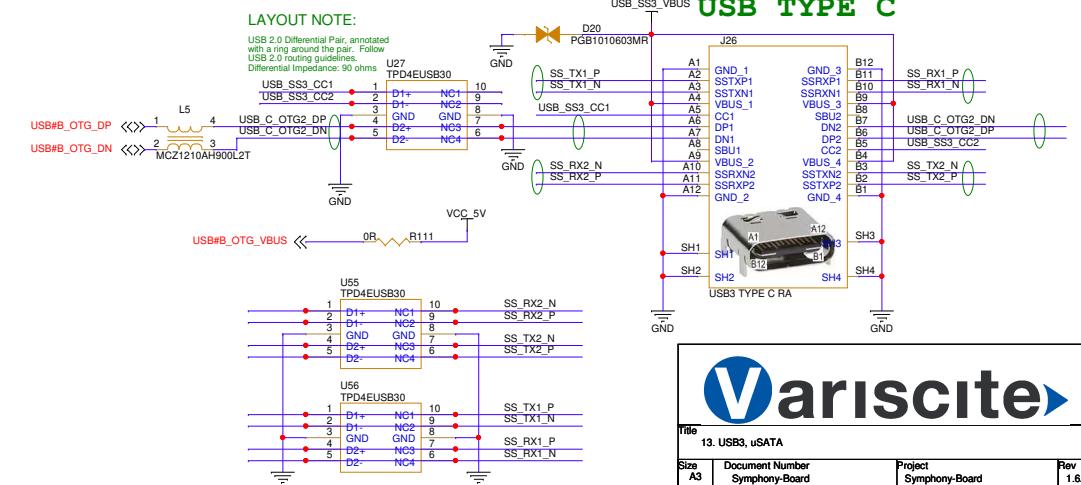
SATA 2.0



Config Channel Logic Detection & Indication of Plug Orientation

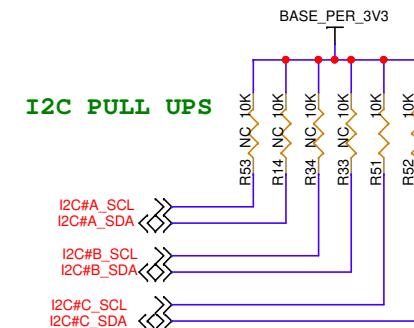
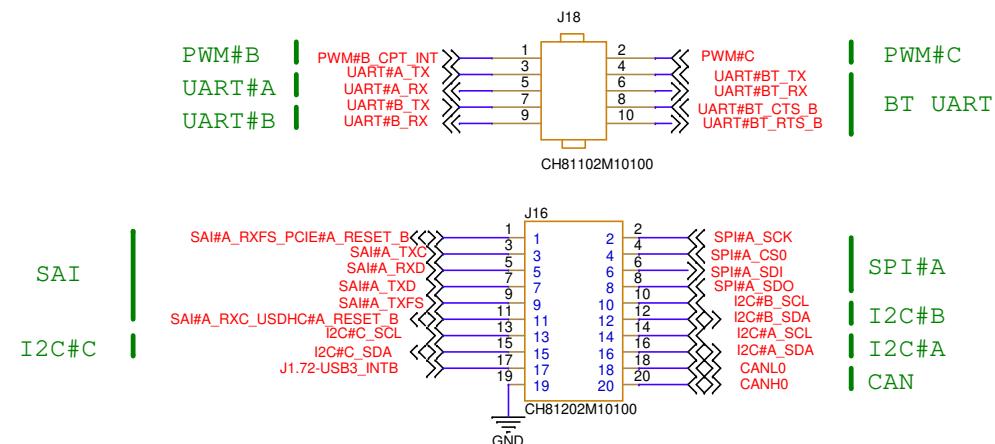


USB TYPE C



14. Headers

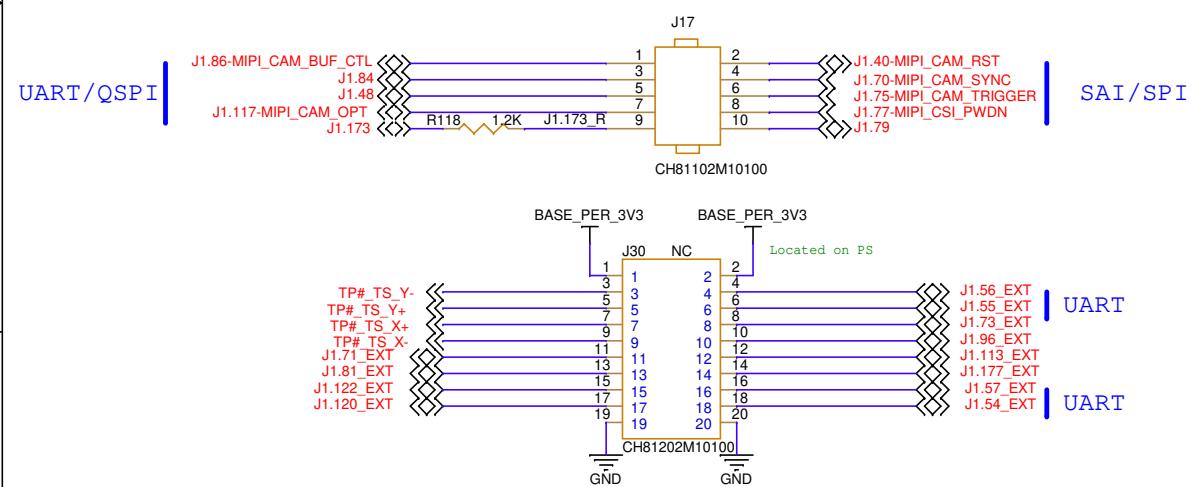
Headers arranged for compatible alternate function



I2C_A has internal pulls in Camera buffer

I2C_B has internal pulls in MX6/MX8/MX8X/MX8MP SOMs.
For MX8MM/MX8MN/6UL SOMs - external pull ups should be added.

Headers arranged for partial compatible alternate function



For complete header alternate function refer
to "VAR-SOMs_Compatibility_and_Pinout.xls" located at:
ftp://ftp.variscite.com/SOM_Compatibility

COLD RESET ON WDOG_B EVENT for MX6/SOLO and 6UL SOMs

Listed above SOMs require short on headers to
get "reboot" to function.
For all other watch dog looped on SOM

CB_WDOG_B	↳ Symphony Board reset circuitry watch dog input	See J3.17
J1.57_EXT	↳ SOM 6UL: PIN57_WDOG1_B	See J3.11
PWM#B_CPT_INT	↳ MX6/SOLO: PIN68_WDOG1_B	See J18.1

USB#A Host VBUS power control

In order to control the USB#A HOST VBUS power a short is required:
CB-USBA_HOST_PWR ↳ Symphony Board U22 See J3.12
J1.82-USBA_HOST_PWR ↳ control input See J3.18

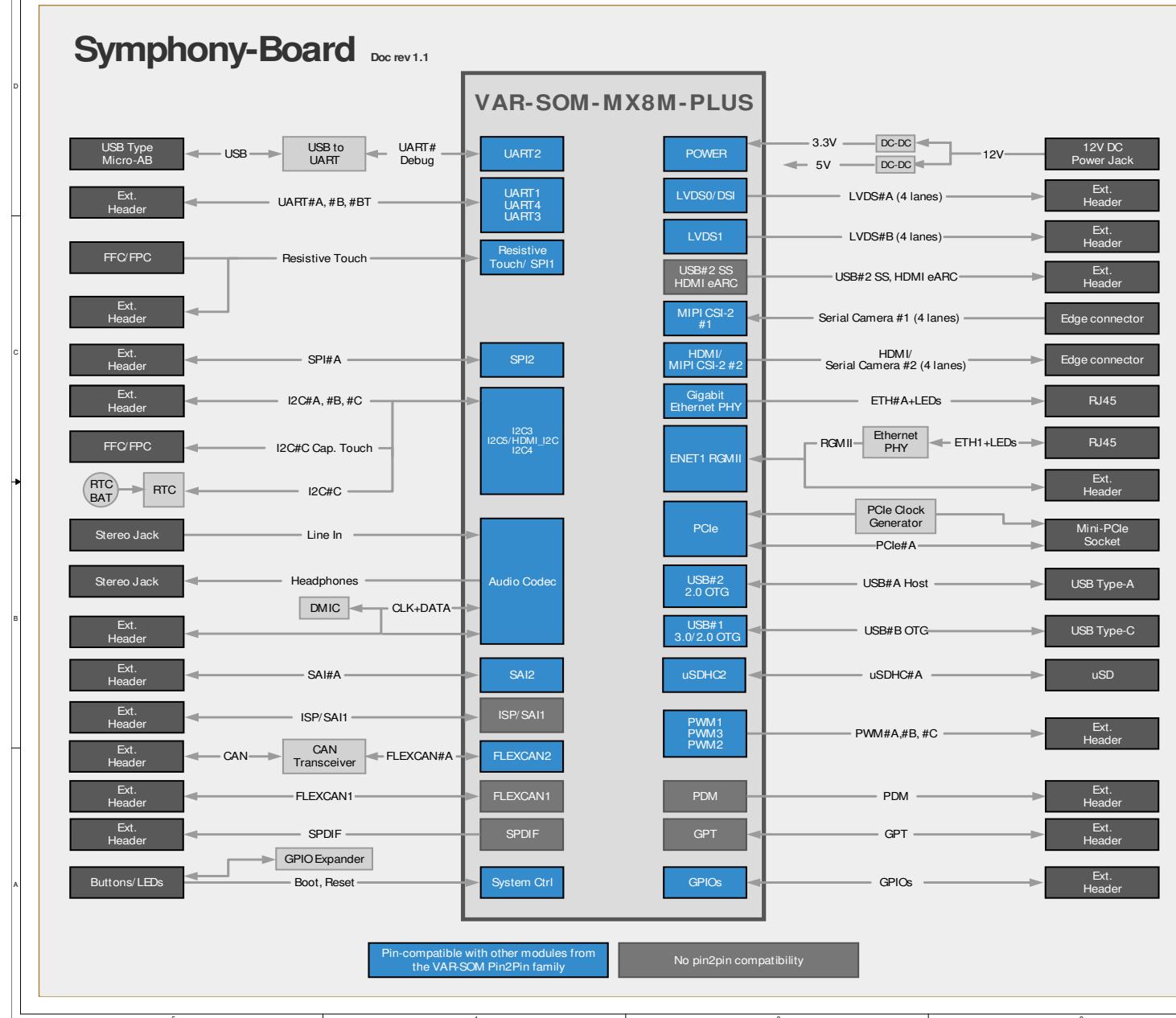


Title

14. Headers

Size	Document Number	Project	Rev
A4	Symphony-Board	Symphony-Board	R1.2
Designer:	Aviad H.	Approved By:	
Date:	Monday, April 04, 2022	Sheet	12 of 24

02. Block Diagram VAR-SOM-MX8M-PLUS



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Title 02. Block Diagram VAR-SOM-MX8MP

Size	Document Number	Project	Rev
A3	Symphony-Board	Symphony-Board	1.0A Rev 1.21
Designer:	Avid H.	Approved By:	
Date:	Monday, April 04, 2022	Sheet	21 of 24

04. VAR-SOM-MX8M-PLUS Connector



1150 高等数学

The Variscite logo consists of the word "Variscite" in a bold, lowercase, sans-serif font. The letter "V" is significantly larger than the other letters. A blue arrow points to the right from the end of the "e".