

Symphony-Board



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Disclaimer:

Schematics are for reference only.
Variscite LTD provides no warranty for the use of these schematics.
Schematics are subject to change without notice.

Revision History

Document	Carrier	Notes
1.0	1.0	Initial
1.1	1.1	Released
1.2	1.1	Updated Block Diagrams Added SH1 wire short symbol Updated Compatibility value for SOM pins 68,69,176 Updated SOM pin 22 net name Fixed U22_B1, C113.1 net name Fixed R1-R2,R35-R38 net name
1.3	1.2	Removed SH1 wire short, J1_68 routed to capacitive touch Changed R29 to C185 Changed R123,R127 to N.C. Added resistors R130-132 Removed ADC_Inxx alternate function from VAR-SOM-MX8 Symbol Updated PCIe resistor assembly note
1.4	1.2	Updated Parallel Camera/HDMI/DP Note Fixed ETH pin names VAR-SOM-MX8X Symbol
1.5	1.2A	Disconnected R129
1.6	1.2A	Adds VAR-SOM-MX8-MINI Block Diagram and Symbol PRE-RELEASE VERSION !!! Subject to change without notice
1.7	1.2B	Fixed VAR-SOM-MX8-MINI Symbol Changed U20_U30_U31 to P/N: FPF2193 Changed R69 to 47K
1.8	1.2C	Update VAR-SOM-MX8-MINI Symbol to V1.1 with side notes for v1.0B(Early access customers) Update VAR-SOM-MX8-MINI Block Diagram POR circuitry fed by VCC_SOM: see UT R68 R61 R40 R60 D5 Removed
1.9	1.2D	Raise VCC_3V3 to Nominal 3.39V for VAR-SOM-MX8-MINI/NANO power up threshold voltage requirement of >3.35V
1.10	1.2E	Reference for new designs: (changes not implemented in V1.2 BRD) * Added x2 studs for heat plate support * Base per .3v3 added slew rate limit * U7 [Base PO5 circuit] added CB_WDOG resistor assembly options * U10 [Base PO6 circuit] added CB_WDOG resistor assembly options * VAR-SOM-MX8-MINI pages added with symbol pinout * VAR-SOM-MX8 Connector update - added NC on // assembly options * Power switch in OFF position discharge of Custom rails added * Ethernet magnetics - supports Marlin, Phoenix & UDE; * Ethernet RGMII LEDs now in SOTN package * Added VAR-SOM-MX8-PLUS Preliminary Symbol and Block Diagram Symbol a Pre-Release Version! Subject to change without notice! * All C1210 capacitor footprint updated to C1210_v0 * M51 to M55 not assembled
1.12	1.3A	* ETH1 PHY clock filter U9 replaced with 49.9 Ohm/0603 resistor * Added design note for ETH1 switches U8 and U10.
1.13	1.4	* MSS and MS6 location adopted to headerless design - Layout * Updated J11 and J12 to MSS and footprint to represent the assembled part * Replace PCIe AC caps on RX lines with 0 ohm resistors * Updated VAR-SOM-MX8-PLUS Symbol pins 41 43 and 84 147 * J19 Modify Camera connector orientation * Remove U8 U10 isolating stubs on ETH1 * U9 isolating stubs on RGMII_Rx line * Added RN1 RN2 RN3 R151 R136 isolating stubs on ETH1 RGMII signals * U26 footprint updated to DS * Y1 C68 C67 updated * SOTN R10 R11 R12 R13 R14 R15 boot: - BOOT_MODE0 = R117 assembled - BOOT_MODE0 - Added PD R149 - USB#A PWR to HOST_J23 always enabled * Remove R39 on pin J1.156 to support SOM-MX8MP 2nd MIPI-CSI Lane2 routing J3 130 pinout change
1.14	1.4A	* Support for VAR-SOM-MX8MP USB OTG - Changed U5_P4 pull for board identification, U21.9 connected to GPIO: - Changed R43,R130,R106 to N.C. - Changed R44,R132 to Assembled * Changed Q4 PIN from TPS27082L (EOL) to -> TPS27081A * Updated VAR-SOM-MX8-PLUS Block Diagram, Symbol pins 36,38 names * Added notes for SOM pins 29,79,84
1.15	1.4A	Changes in v1.141.4A for R43,R44 were not implemented (part of board identification) and only appear in revision history; board identification implemented via EEPROM U3. Board identification required for OS to identify method of OTG ID used: PTN510 or GPIO
1.16	1.5	* Modified VCC_3V3 to 3.35V nominal for all SOMs. For VAR-SOM-MX8-MINI/NANO, power up threshold voltage requirement of >3.35V is implemented using Q10,R152 * Added note VAR-SOM-MX8-MINI/NANO pin 91
1.17	1.5	* Updated note for I2C#B pull up resistors
1.18	1.5	* Updated note for PTN36043BXY chip
1.19	1.5A	* Q10 changed to 2N7002P_215 Transistor Q10 changed to 2N7002P to stabilize the SOM voltage in the OFF state. Old transistor leakage current (IDG) changed the feedback current and increased the SOM voltage. 2N7002P does not have SG diode that allowed IDSS to flow into the Gate * SOM Pin 84 Note changed
1.20	1.6	Ethernet PHY replaced to ADIN1300 R22,R23,R35,R36 assembled with Ferrite Bead C185 assembled with 10K resistor, R30 not assembled U2 changed to CBTU02043B USB3 crossover switch changed to CBTU02043B
1.21	1.6A	Due to EOL: U35 changed to NFL18ZT207H1A3D Due to allocation problems: U13 changed to SN65HVD232QDR
1.22	1.6B	Due to allocation problems: U22,U29,U30,U31 changed to P/N: FPF2194
1.23	1.6C	Added VAR-SOM-MM62 Block Diagram and Symbol Added VAR-SOM-MM93 Block Diagram and Symbol Temporary removed compatibility notes Added hand wired EXP_MDI0_EN line.



Rev. A	Document Number	Project Name
01	Symphony-Board	Symphony-Board
Date	Mon, 20. January 2023	Page No.
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OFF PAGE CONNECTOR INDEX:

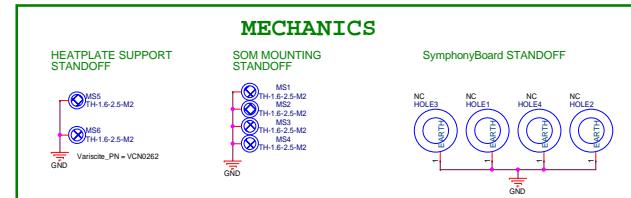
- Function# :Interface common to ALL SOMs
- J1.xxx-Function :Interface common to certains SOMs or Used for carrier board common function
- J1.xxx :No common interface

For cross probing between SOM symbol and the specific SOM Connector used, set the "Implementation" property value in SOM port symbol to one of the following:

1. VAR-SOM-MX6
2. VAR-SOM-MX8
3. VAR-SOM-MX8X
4. VAR-SOM-MX8M-MINI
5. VAR-SOM-MX8M-NANO
6. VAR-SOM-MX8M-PLUS
7. VAR-SOM-MX93
8. VAR-SOM-AM62

For complete alternate function per pin and specific SOM: please refer to "VAR-SOMs_Compatibility_and_Pinout.XLS" located at: ftp://ftp.variscite.com/SOM_Compatibility

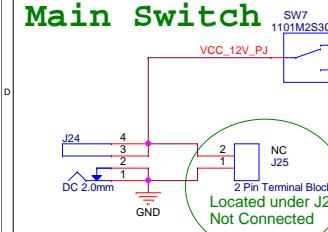
Compatibility list
Describes the ALT per SOM for compatibility.
Order of names: (MX6/MX8/MX8X/MX8MM/MX8MN/MX8MP)
Note: single name means identical name for all.



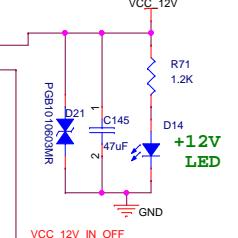
05. Power,Reset,Boot,RTC,EEPROM

12VDC INPUT

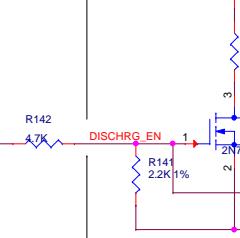
Main Switch



POWER DISCHARGE



SOM BOOTSTRP



POWER DISCHARGE

Internal boot is from eMMC
MX6 for eMMC boot see additional changes note

3.35V/8A FROM PWR JACK

For supporting MX6 eMMC boot option:
Remove R9
Assemble R56,R11
Note: Normal configuration is with NAND

3.35V/8A FROM PWR JACK

BASE_PER_3V3

R56 NC OR /*EMMC_BOOT// J1.40-MIPI_CAM_RST

R11 NC OR /*EMMC_BOOT// AC#_AGND

R9 0R AGND

R17 NC 0R //SCU_BOOT_MODEL J1.146-HDMI_D1P

GND

SOM PWR

SOM CURRENT MEASURING:
REMOVE R58 AND CONNECT SERIES AMPEREMETER

SOM PWR

VCC_SOM

R58 0.0R

5V/8A FROM PWR JACK

U18 RT2299BHGQW

VIN

BOOT

PVIN

EN

LX

FB

C101 4.7uF

C100 100nF

C99 10uF

C100 10uF

VCC_3V3_5V_EN

R81 100K

C97 100F

R81 100K

C97 100F

PGOOD

COMP

GND

RT/SYNC

SS/TR

GND

L2 4.7uH

C78 100nF

R75 4.3K 1%

R83 174K 1%

C82 180pF

C83 8.2nF

C84 47uF

C103 47uF

C104 47uF

D13 +5V LED

VCC_12V

VCC_5V

R70 475R 1%

R92 100K

C105 10uF

C106 10uF

C84 100K

C85 100F

R84 100K

C81 100F

PGOOD

COMP

GND

RT/SYNC

SS/TR

GND

L3 4.7uH

C80 100nF

R78 2.4K 1%

R152 3.6K 0.1%

C86 8.2nF

C85 180pF

R85 24K 0.1%

Q10 2N7002P

VCC_12V

VCC_3V3

R83 174K 1%

C82 180pF

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C84 47uF

C103 47uF

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C85 180pF

R85 24K 0.1%

Q10 2N7002P

VCC_12V

VCC_3V3

R92 100K

C105 10uF

C106 10uF

C84 100K

C85 180pF

R84 100K

C81 100F

PGOOD

COMP

GND

RT/SYNC

SS/TR

GND

L3 4.7uH

C80 100nF

R78 2.4K 1%

R152 3.6K 0.1%

C86 8.2nF

C85 180pF

R85 24K 0.1%

Q10 2N7002P

VCC_12V

VCC_3V3

R92 100K

C105 10uF

C106 10uF

C84 100K

C85 180pF

R84 100K

C81 100F

PGOOD

COMP

GND

RT/SYNC

SS/TR

GND

L3 4.7uH

C80 100nF

R78 2.4K 1%

R152 3.6K 0.1%

C86 8.2nF

C85 180pF

R85 24K 0.1%

Q10 2N7002P

VCC_12V

VCC_3V3

R92 100K

C105 10uF

C106 10uF

C84 100K

C85 180pF

R84 100K

C81 100F

PGOOD

COMP

GND

RT/SYNC

SS/TR

GND

L3 4.7uH

C80 100nF

R78 2.4K 1%

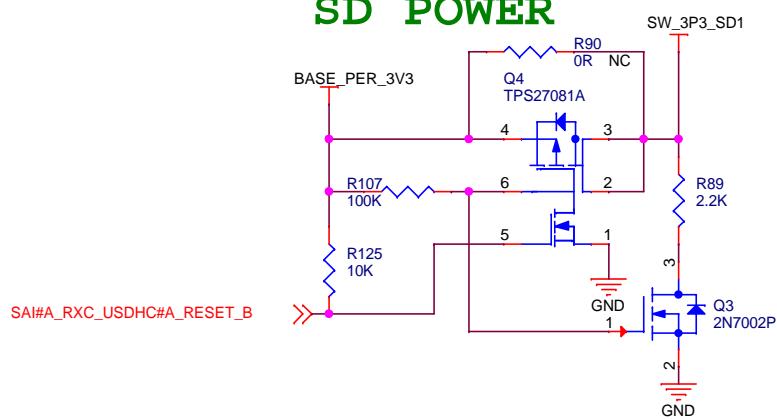
R152 3.6K 0.1%

C86 8.2nF

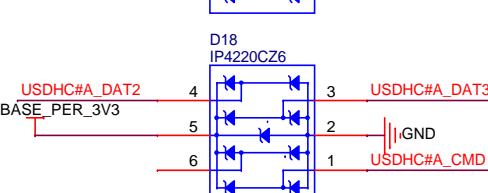
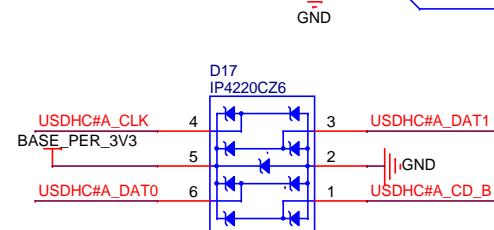
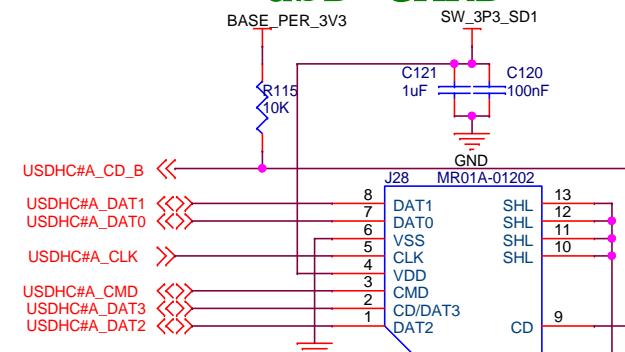
C85 180

06. uSD, Audio,CAN

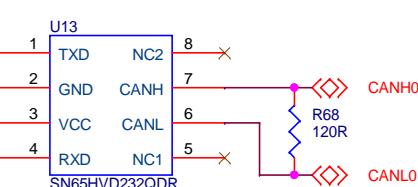
SD POWER



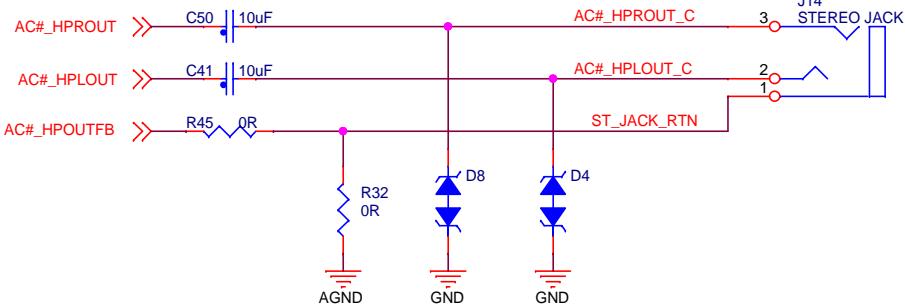
uSD CARD



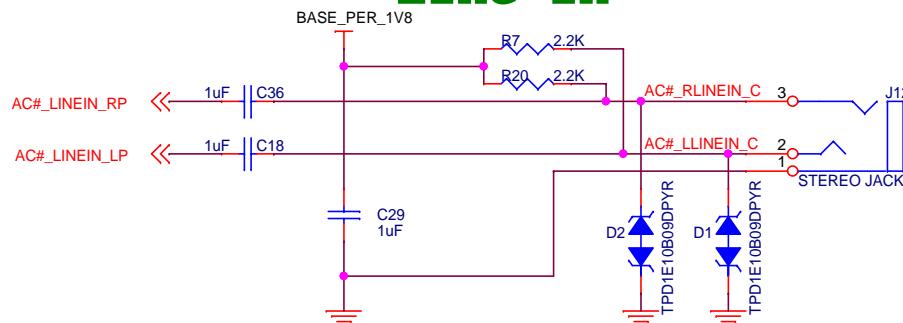
CAN BUS



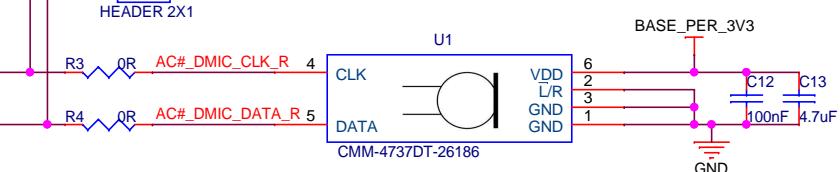
Headphones



Line In



DIGITAL MIC



Variscite

Title

06. uSD, Audio,CAN

Size

A4

Document Number

Symphony-Board

Project

Symphony-Board

Rev

R1.2

Designer:

Aviad H.

Approved By:

[Redacted]

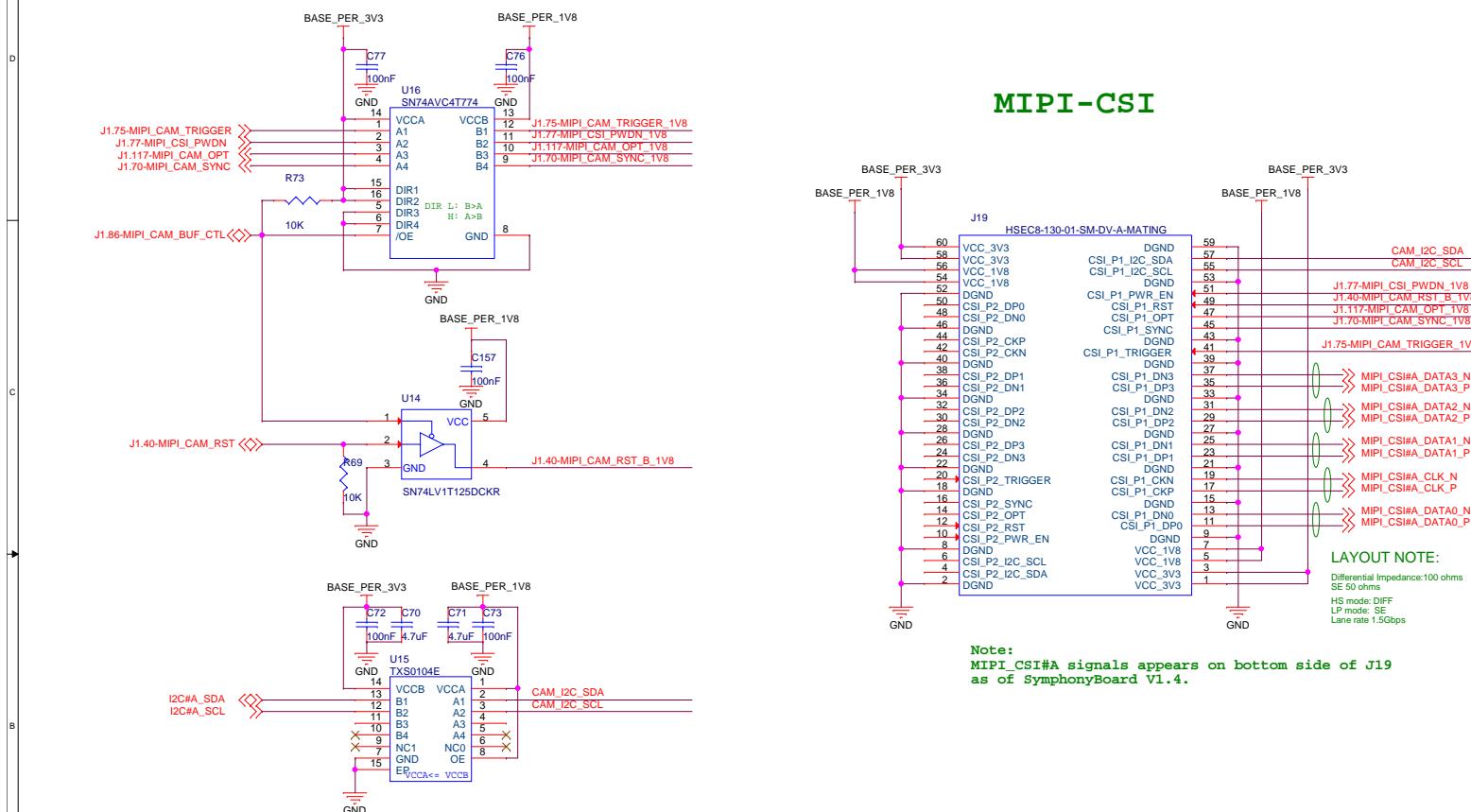
Date:

Monday, January 30, 2023

Sheet

4 of 24

07. Camera, HDMI, DP



Note for U32 (analog switch):
Switch is to enable support for the following adapters:
Parallel camera, HDMI, DisplayPort and second MIPI-CSI.

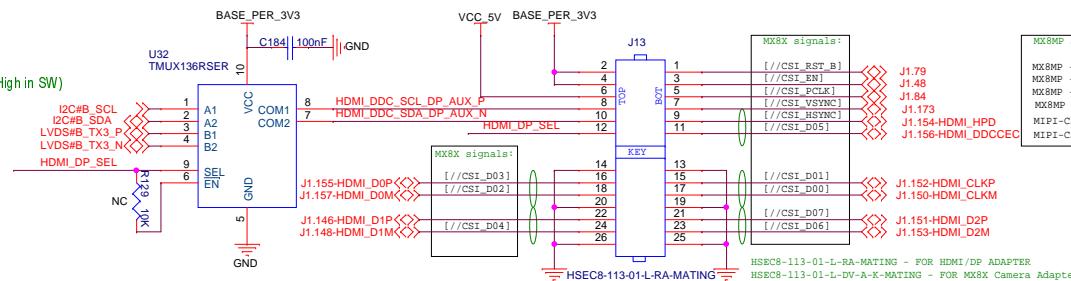
Switch select controlled on adaptor will select between:
1) I2C#B which can export

VAR-SOM-MX8X: I2C3 Used by parallel camera
VAR-SOM-MX8: HDMI DDC Used by HDMI (GPIO1_22 in should be set High in SW)

2) LVD#B, TX3 which can export:
VAR-SOM-MX8(DP assembly option): HDMI AUX used by DP

Switch can be omitted when designing for only one of the the above interfaces.

J13: MX6/MX8-HDMI, MX8-DP, MX8X-CSI, MX8MP-2nd MIPI-CSI

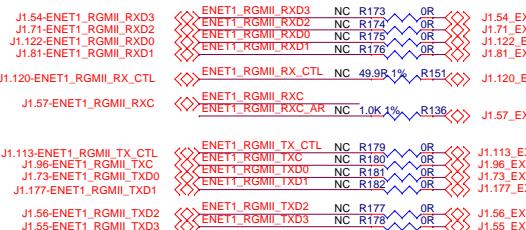


Title: 07. Camera, HDMI, DP

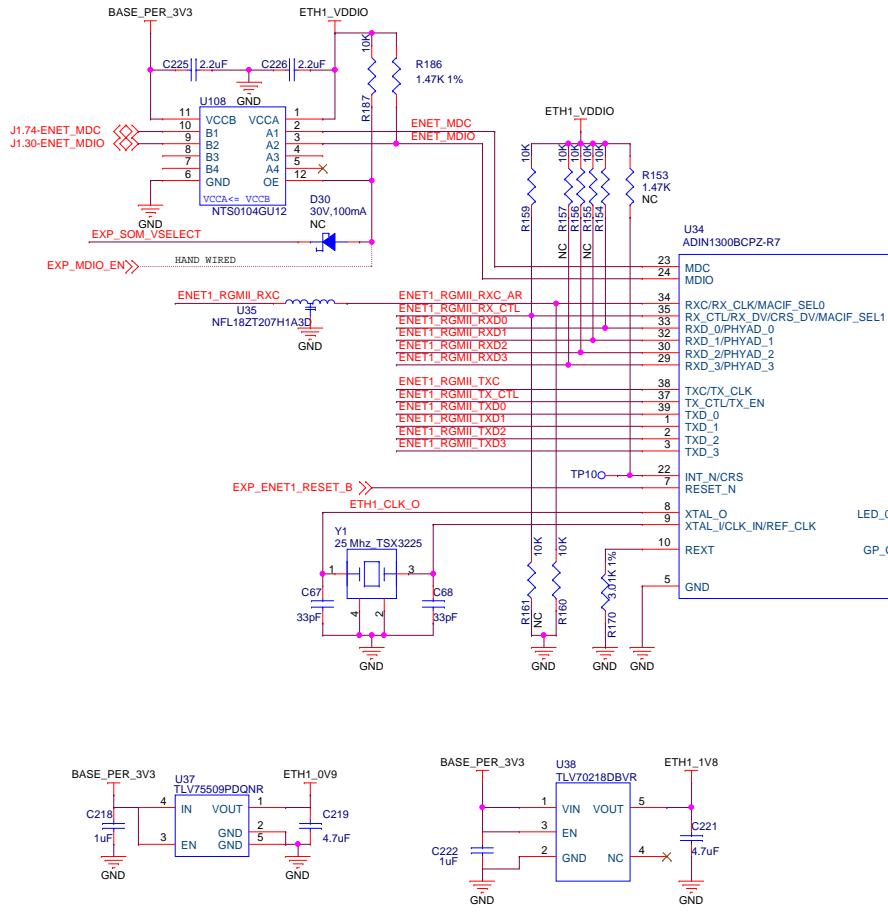
Size A3	Document Number Symphony-Board	Project Symphony-Board	Rev 1.6C_R1.23
Designer: Aviad H.	Approved By:		
Date: Monday, January 30, 2023	Sheet 5 of 24		1

08. Ethernet

Header/Stub isolation resistors

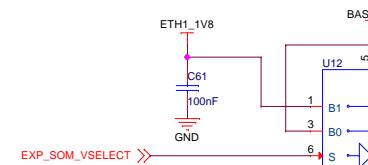


Note:
Customer requiring usage of J30 header (located on bottom side)
should assemble these resistors if not assembled by default



VDD_ENET for SOM-MX8/MX8X/MX8MP

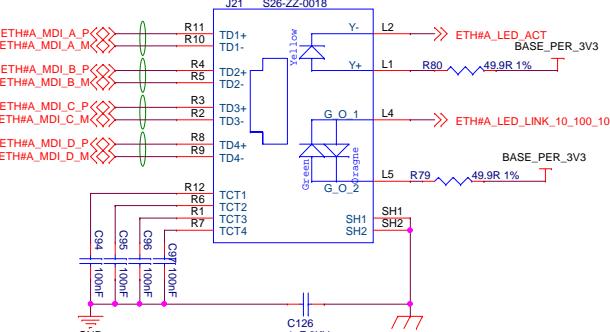
Power for ENET1_RGMII IOs on SOM power fed from pin J1.38
For specific SOM listed above, requiring second ETH port on ENET1 this power should be set to 1.8V source from U11 PHY



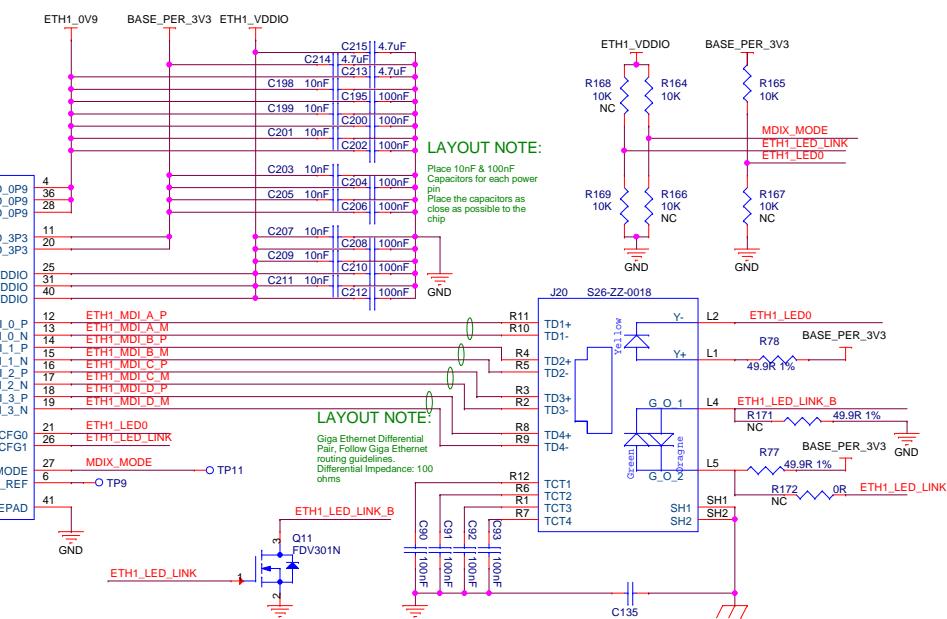
S="L" BO<>A (MX6/SOLO): VCC_SOM (same as BASE_3V3 timing) 2
S="L" BO<>A (MX6/MX6XL): ETH161 UDP/DIGI REC

Gigabit Ethernet (Internal)

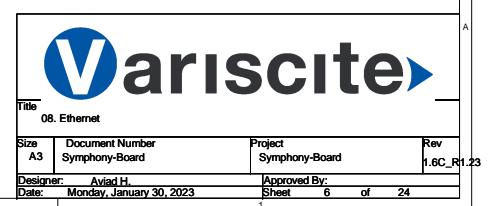
LAYOUT NOTE: Giga Ethernet Differential Pair, Follow Giga Ethernet routing guidelines.



C202 100nF LAYOUT NOT

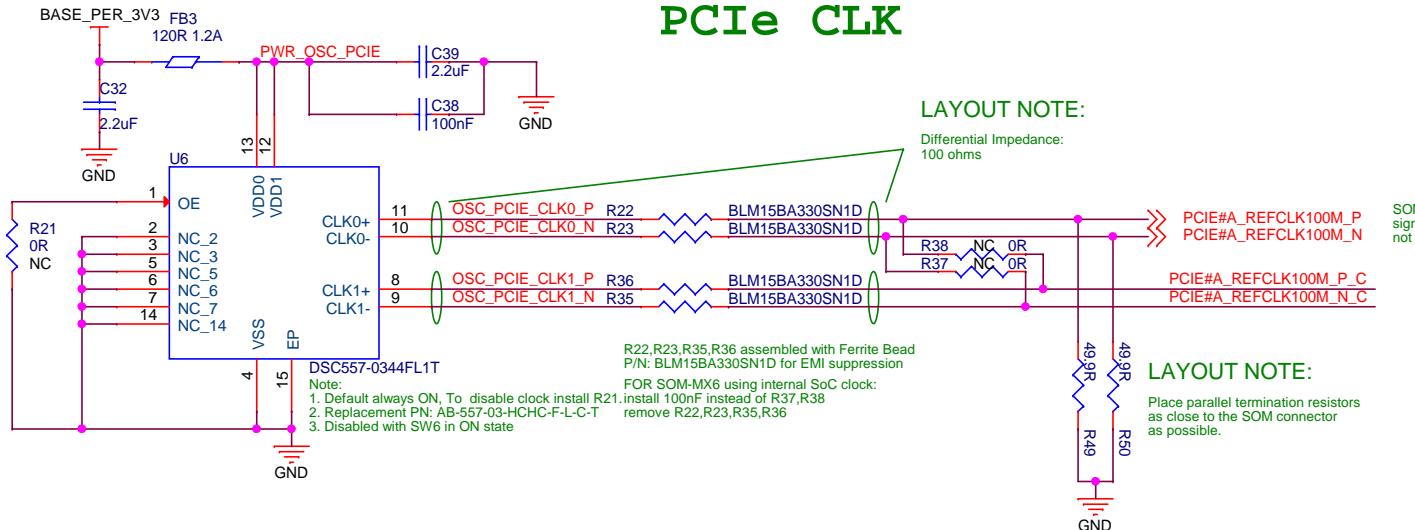


Ethernet Differential

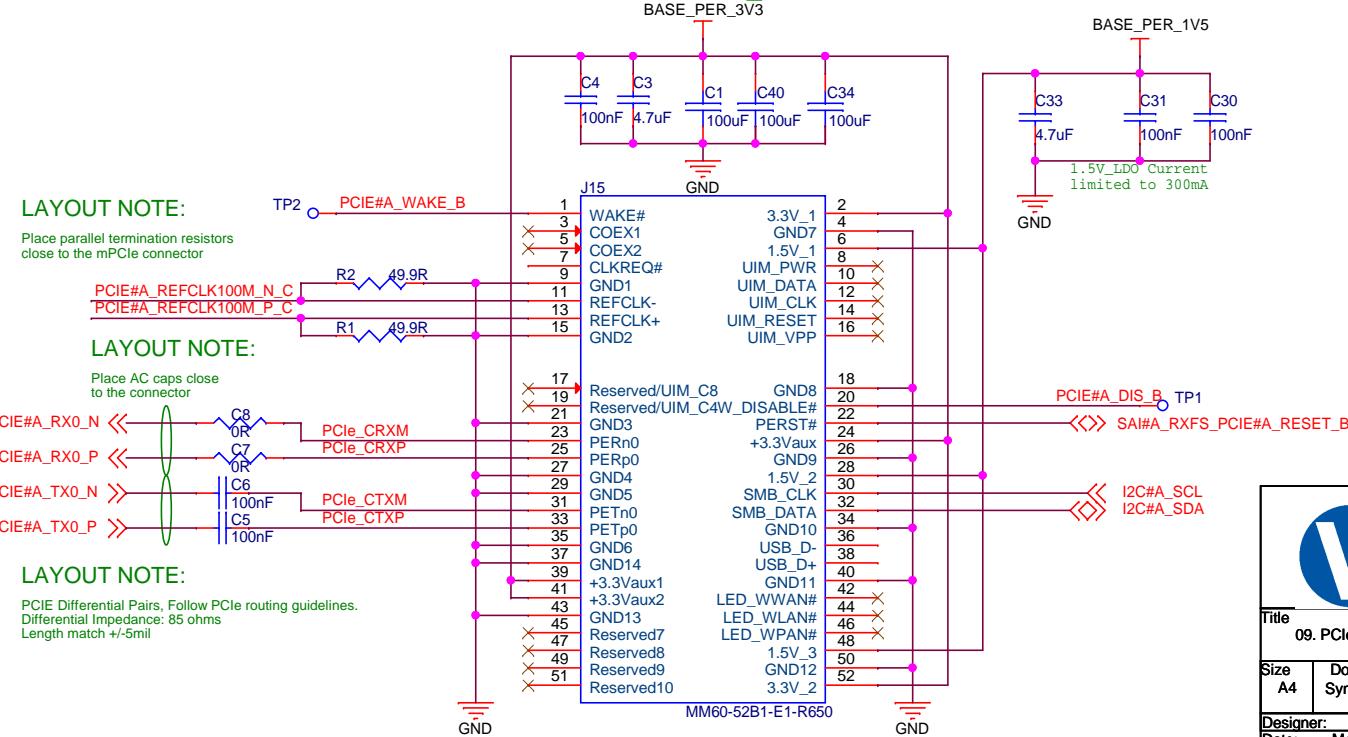


09. PCIe

PCIe CLK



mPCIexp

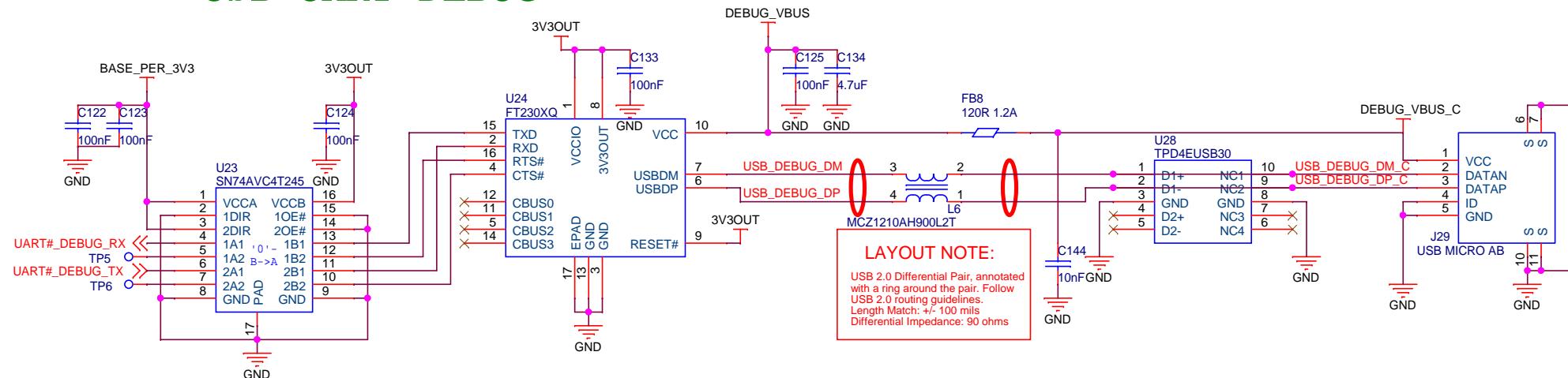


Variscite

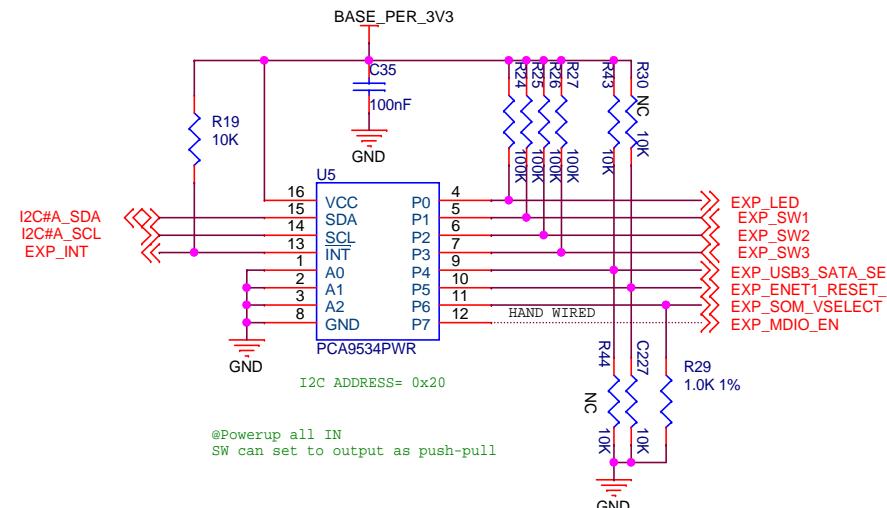
Title 09. PCIe			
Size A4	Document Number Symphony-Board	Project	Rev 1.6C_R1.23
Designer: Aviad H.	Approved By:		
Date: Monday, January 30, 2023	Sheet 7 of 24	1	

10. Debug, GPIO Exp, Buttons, LED

USB UART DEBUG

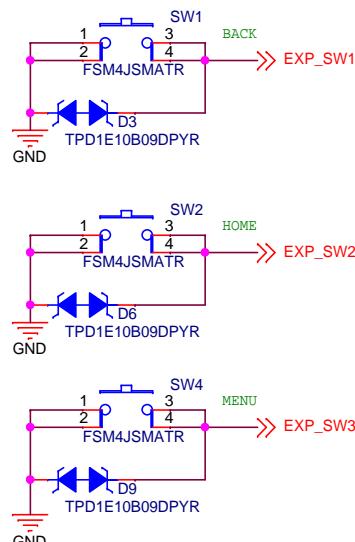


GPIO EXPANDER



In VAR-SOM-MX8 SOM pin 29 EXP_INT is referenced to 1.8V.
When using pin 29 as an input pin driven by higher input voltage,
use an external voltage divider or limit the current using a series resistor to a maximum of 1mA.

GP BUTTON



GP LED



Variscite

Title 10. Debug, GPIO Exp, Buttons, LED

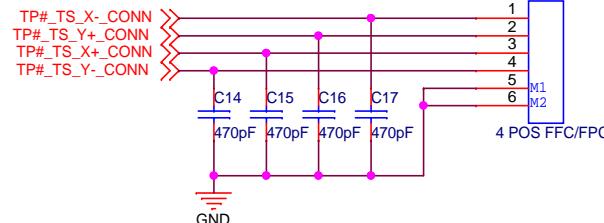
Size	Document Number	Project	Rev
A4	Symphony-Board		1.6C_R1.23
Designer:	Aviad H.	Approved By:	
Date:	Monday, January 30, 2023	Sheet	8 of 24

11. LVDS, DSI, Touch

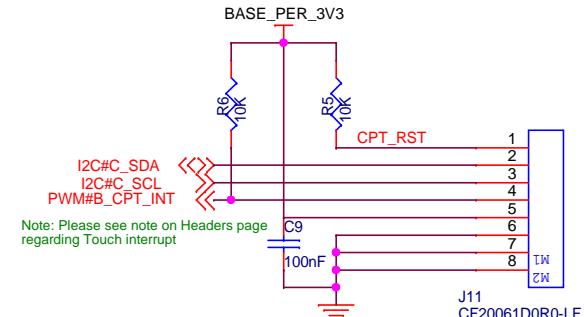
LVDS DISPLAY A

LVDS DISPLAY B

RESISTIVE TOUCH

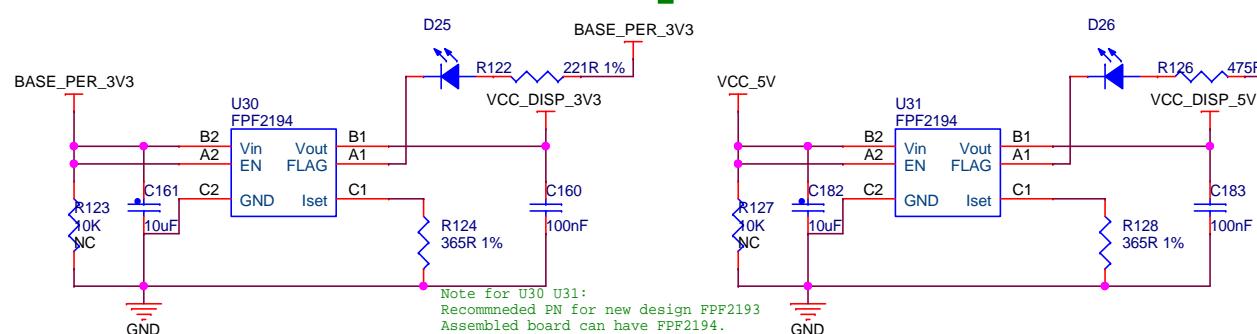


CAPACITIVE TOUCH



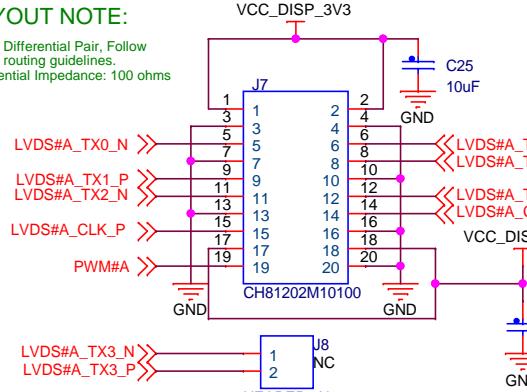
See note in:
"Headers" Page 14

Short circuit protection



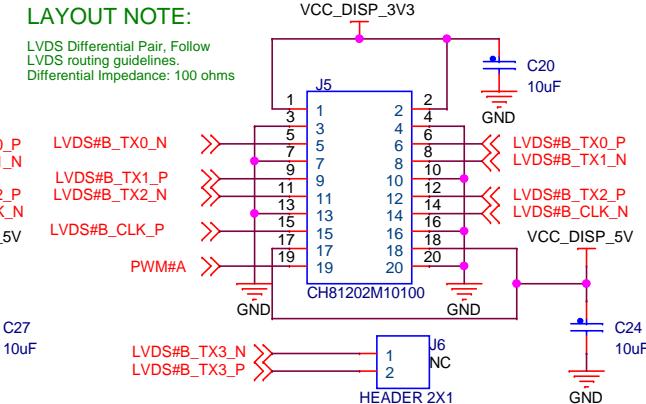
LAYOUT NOTE:

LVDS Differential Pair, Follow LVDS routing guidelines.
Differential Impedance: 100 ohms



LAYOUT NOTE:

LVDS Differential Pair, Follow LVDS routing guidelines.
Differential Impedance: 100 ohms

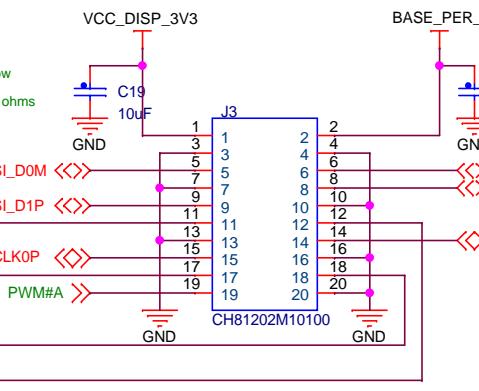


MIPI DSI DISPLAY

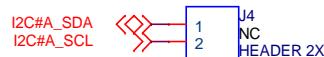
LAYOUT NOTE:

LVDS Differential Pair, Follow LVDS routing guidelines.
Differential Impedance: 100 ohms

MX8X:
QSPI/ADC



MX8X:
QSPI/ADC

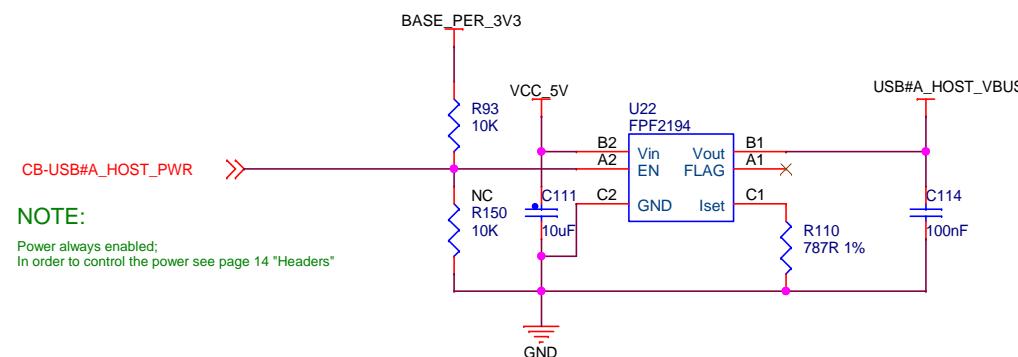
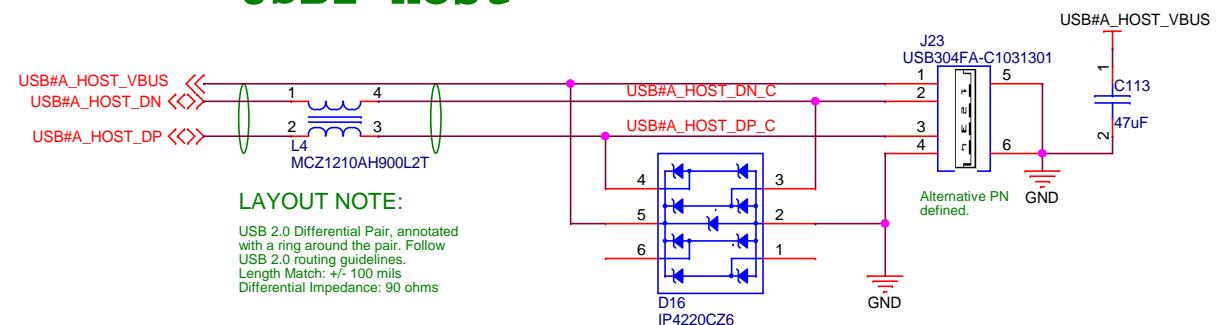


Title
11. LVDS, DSI, Touch

Size	Document Number	Project	Rev
	Symphony-Board	Symphony-Board	R1.6C R1.2
Design: Aviad H.		Approved By:	
Date: Monday, January 30, 2023		Sheet	9 of 24

12. USB2 Host

USB2 Host



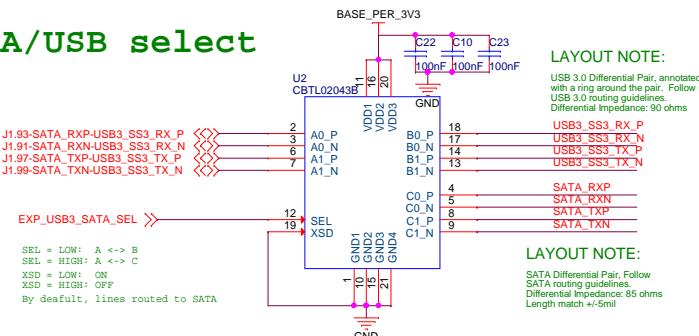
Variscite

Title
12. USB2 Host

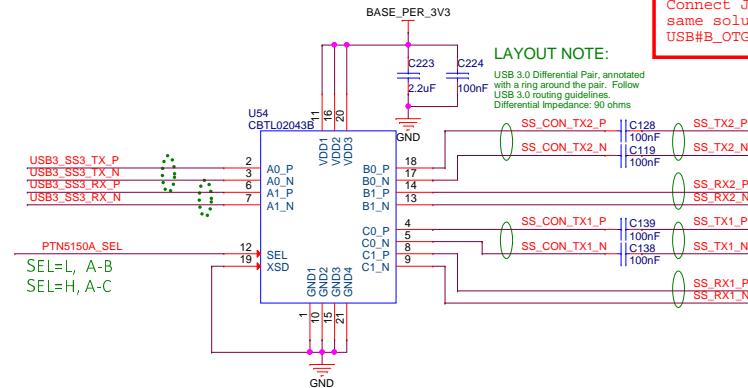
Size A4	Document Number Symphony-Board	Project Symphony-Board	Rev 1.6C R1.2
Designer: Aviad H.	Approved By:		
Date: Monday, January 30, 2023	Sheet 10 of 24		

13. USB3, uSATA

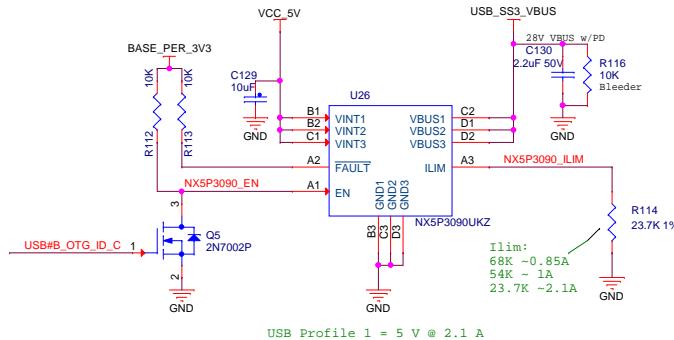
SATA/USB select



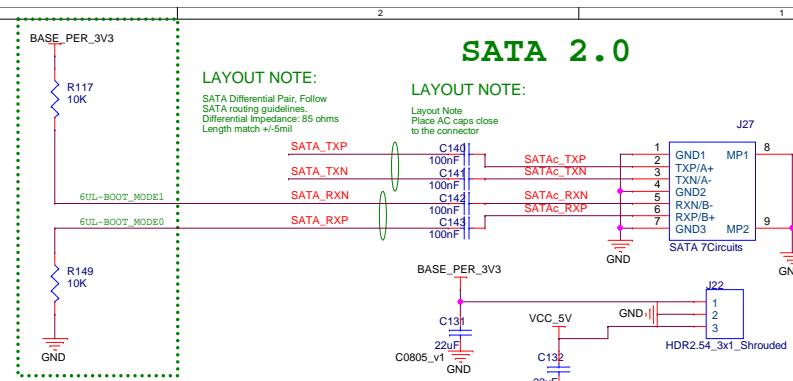
USB TYPE C Circuitry



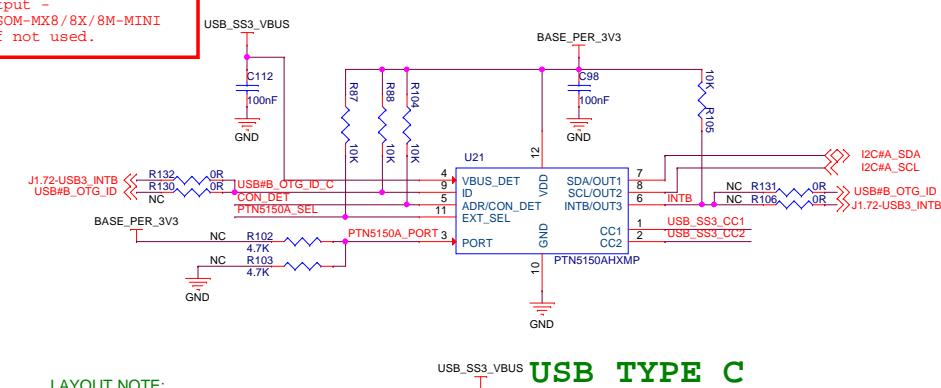
5V Source Load Switch



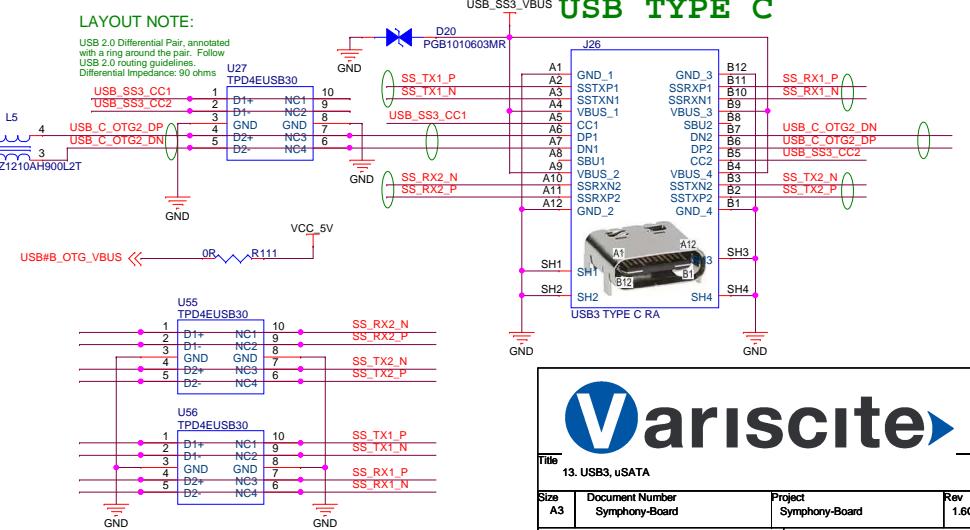
SATA 2.0



Config Channel Logic Detection & Indication of Plug Orientation



USB TYPE C



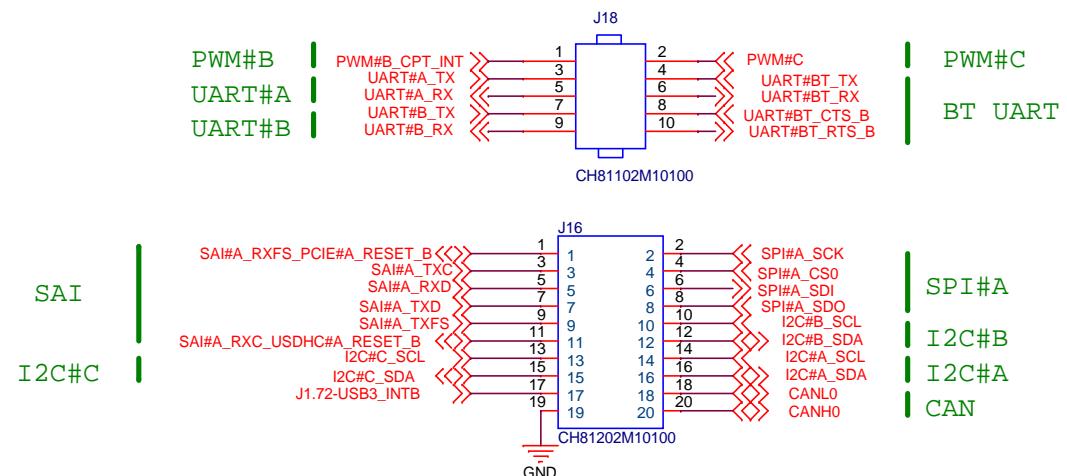
Variscite

Title: 13. USB3, uSATA

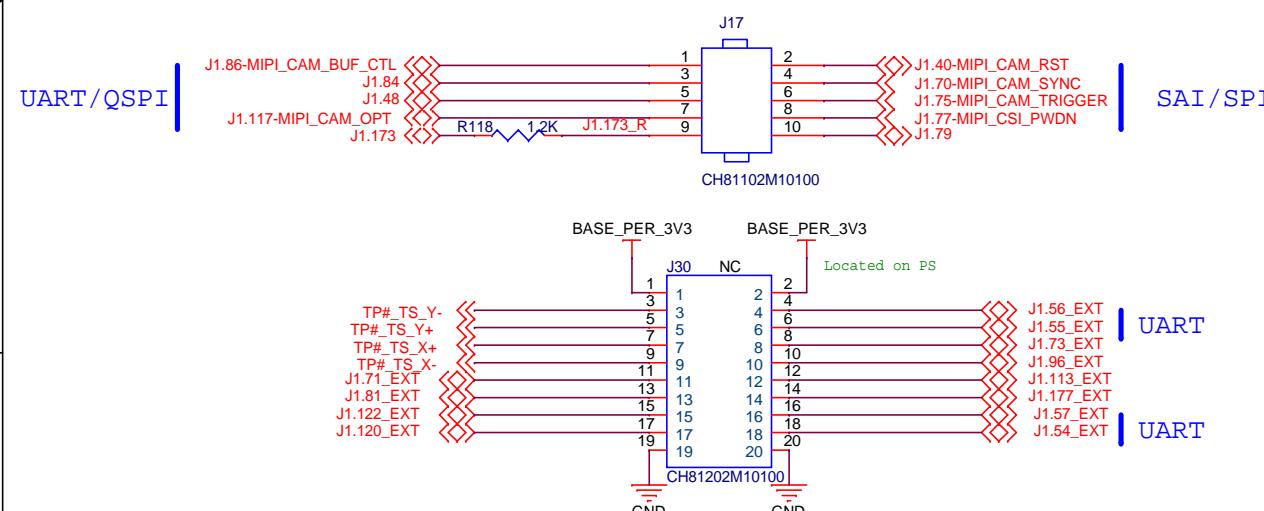
Size	Document Number	Project	Rev
A3	Symphony-Board	Symphony-Board	1.6C
Designer:	Aviad H.	Approved By:	
Date:	Monday, January 30, 2023	Sheet	11 of 24

14. Headers

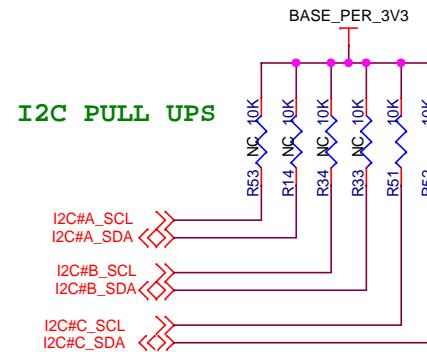
Headers arranged for compatible alternate function



Headers arranged for partial compatible alternate function



For complete header alternate function refer to "VAR-SOMs_Compatibility_and_Pinout.XLS" located at:
ftp://ftp.variscite.com/SOM_Compatibility



I2C_A has internal pulls in Camera buffer
I2C_B has internal pulls in MX6/MX8/MX8X/MX8MP SOMs.
For MX8MM/MX8MN/6UL SOMs - external pull ups should be added.

COLD RESET ON WDOG_B EVENT for MX6/SOLO and 6UL SOMs

Listed above SOMs require short on headers to get "reboot" to function.
For all other watch dog looped on SOM

CB_WDOG_B	➤ Symphony Board reset circuitry watch dog input	See J3.17
J1.57_EXT	➤ SOM_6UL: PIN57 WDOG1_B	See J3.11
PWM#B_CPT_INT	➤ MX6/SOLO: PIN68 WDOG1_B	See J18.1

USB#A Host VBUS power control

In order to control the USB#A HOST VBUS power a short is required:

CB-USB#A_HOST_PWR	➤ Symphony Board U22 control input	See J3.12
J1.82-USB#A_HOST_PWR	➤	See J3.18



Title

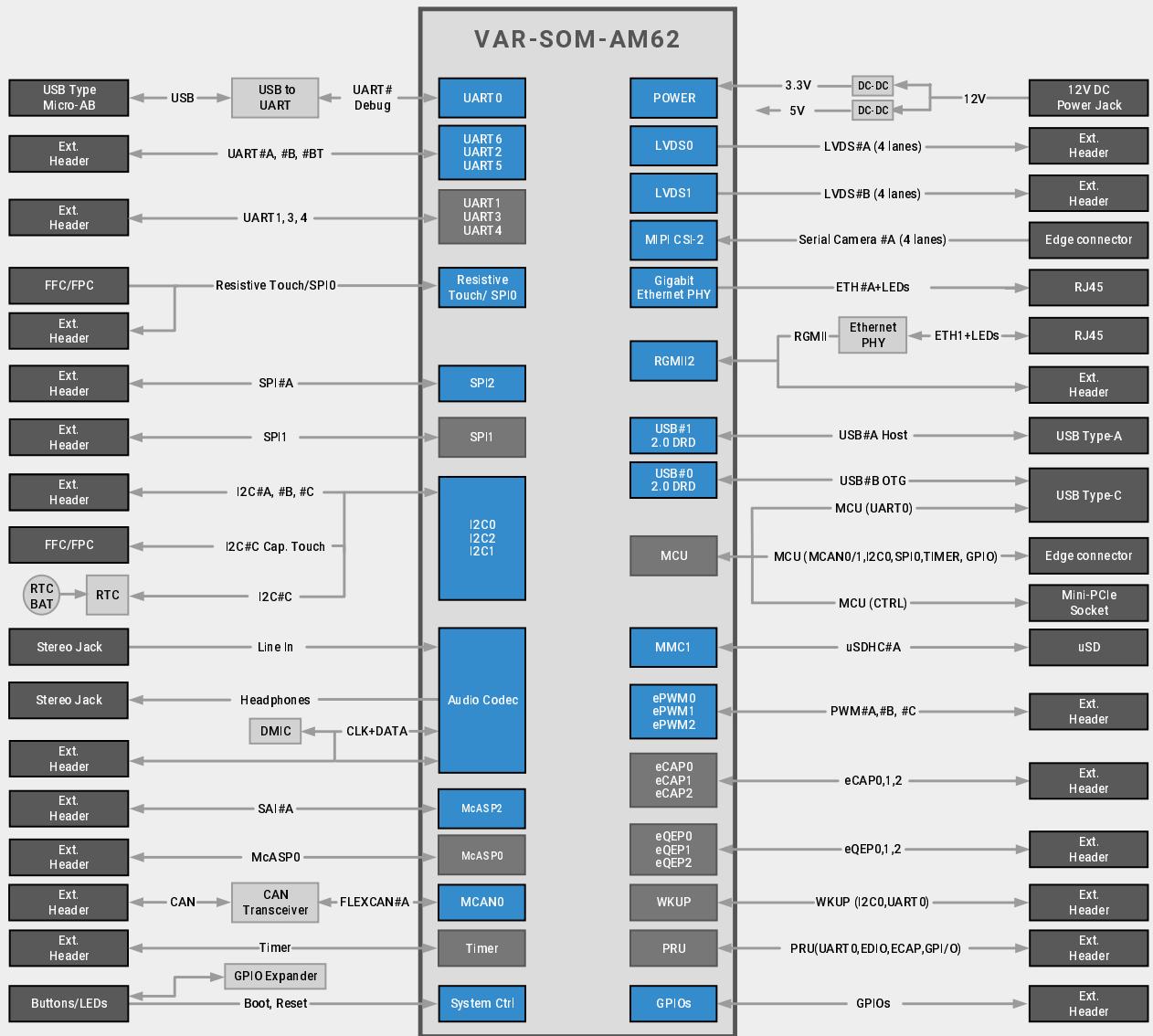
14. Headers

Size	Document Number	Project	Rev
A4	Symphony-Board	Symphony-Board	R1.6C_R1.2
Designer:	Aviad H.	Approved By:	
Date:	Monday, January 30, 2023	Sheet	12 of 24

02. Block Diagram VAR-SOM-AM62

Symphony-Board

Doc rev 1.0



Title 02. Block Diagram VAR-SOM-AM62

Size A3	Document Number Symphony-Board	Project Symphony-Board	Rev R1.23
Designer: Aviad H.	Approved By:		
Date: Monday, January 30, 2023	Sheet 21 of 24		

04. VAR-SOM-AM62 Connector

