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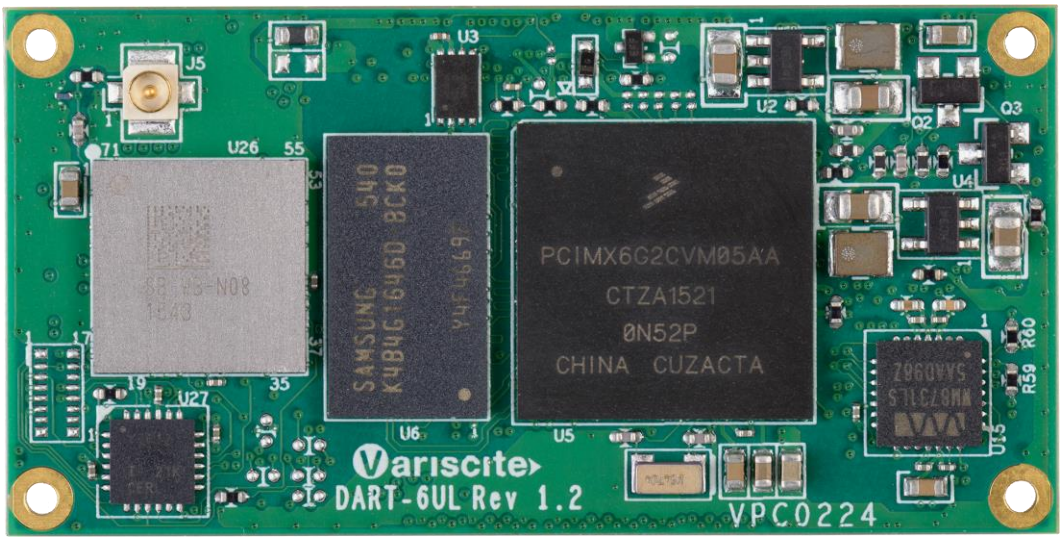
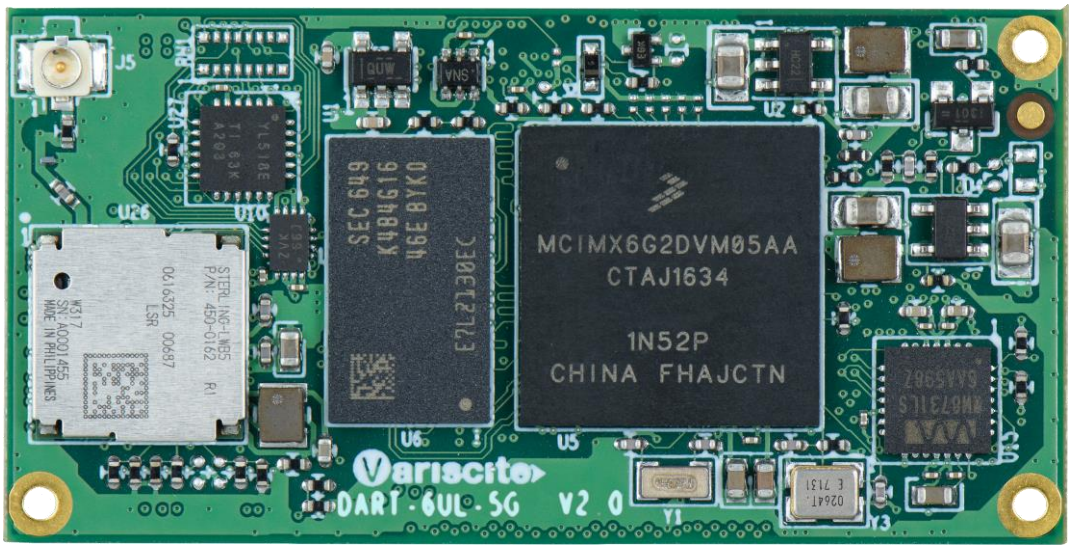
DART-6UL v1.X, DART-6UL-5G v2.X Datasheet

NXP/Freescale i.MX6UltraLite / 6ULL™ - based System-on-Module





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DART-6UL/DART-6UL-5G Datasheet

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2.17	14/07/2020	Updated section 6.2 Operating Conditions Updated Section 6.3 Power consumption
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2.19	03/01/2023	Updated section 2.5 - Key Features
2.20	26/02/2023	Updated section 7 Updated the eMMC sections 1.2, 2.2
2.21	05/03/2023	Correct Typo section 2.4 Heading
2.22	08/02/2024	Updated section 2.5

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1. Overview

1.1. General Information

The DART-6UL/DART-6UL-5G is a power-optimized cost-effective System-on-Module that perfectly fits various embedded and industrial products and segment. It is based on i.MX6 UltraLight/ 6ULL up to 900MHz ARM® Cortex™-A7 multipurpose processor from NXP/Freescale.

The DART-6UL/DART-6UL-5G provides an ideal building block for simple integration with a wide range of products in target markets requiring low power consumption, small size and a very cost effective solution.

Variscite also provides a complete hardware and software development kit (DVK) for the SoM in the form of a carrier board with two 90 pins Board to Board connectors for the DART-6UL/DART-6UL-5G and an optional TFT display and touch panel. The carrier board of the DART-6UL/DART-6UL-5G is ideal not only as reference for the customer to develop its own custom board but also as a cost effective solution for production.

Supporting products:

- VAR-6ULCustomBoard – carrier board, complements the DART-6UL/DART-6UL-5G
- VAR-DVK-6UL: full development kit, including:
  - ✓ VAR-6ULCustomBoard
  - ✓ DART-6UL/DART-6UL-5G
  - ✓ Display and touch
  - ✓ Accessories and cables

Contact Variscite support services for further information: mailto:support@variscite.com.

1.2. Feature Summary

- NXP/Freescalei.MX 6UltraLite / 6ULL
  - ✓ Power optimized up to 900MHz ARM Cortex-A7™
  - ✓ Up to 512MB DDR3L, 512MB NAND / 128GB eMMC
  - ✓ Integrated security features
  - ✓ 2D pixel acceleration engine (PxP)
- Display Support
  - ✓ 24bits Parallel LCD up to WXGA (1366 x 768)
  - ✓ Touch screen controller
  - ✓ EPDC for E-Ink EPD panels up to 2048x1536@106Hz (6ULL only)
- Networking
  - ✓ 2 x 10/100Mbps Ethernet
  - ✓ Certified Wi-Fi 802.11 b/g/n (DART-6UL)
  - ✓ Certified Wi-Fi 802.11 ac/a/b/g/n (DART-6UL-5G)
  - ✓ Bluetooth: 5.2 / BLE
- USB
  - ✓ USB 2.0 OTG
  - ✓ USB 2.0 Host
- Audio
  - ✓ Digital audio SAI/SPDIF
  - ✓ ESAI (6ULL only)
  - ✓ Analog microphone (stereo)
  - ✓ Headphone out, line-in
- Camera
  - ✓ Parallel input
- Other Interfaces:
  - ✓ Dual CAN, I2C, SPI, PWM, JTAG, UART, SD/MMC
- Power
  - ✓ Single 3.3V
  - ✓ Low Power consumption, optimized in both operational and suspend modes
- Dimensions (W x L x H): 25mm x 50mm x 4mm
- Industrial temperature support

1.3. Block Diagram

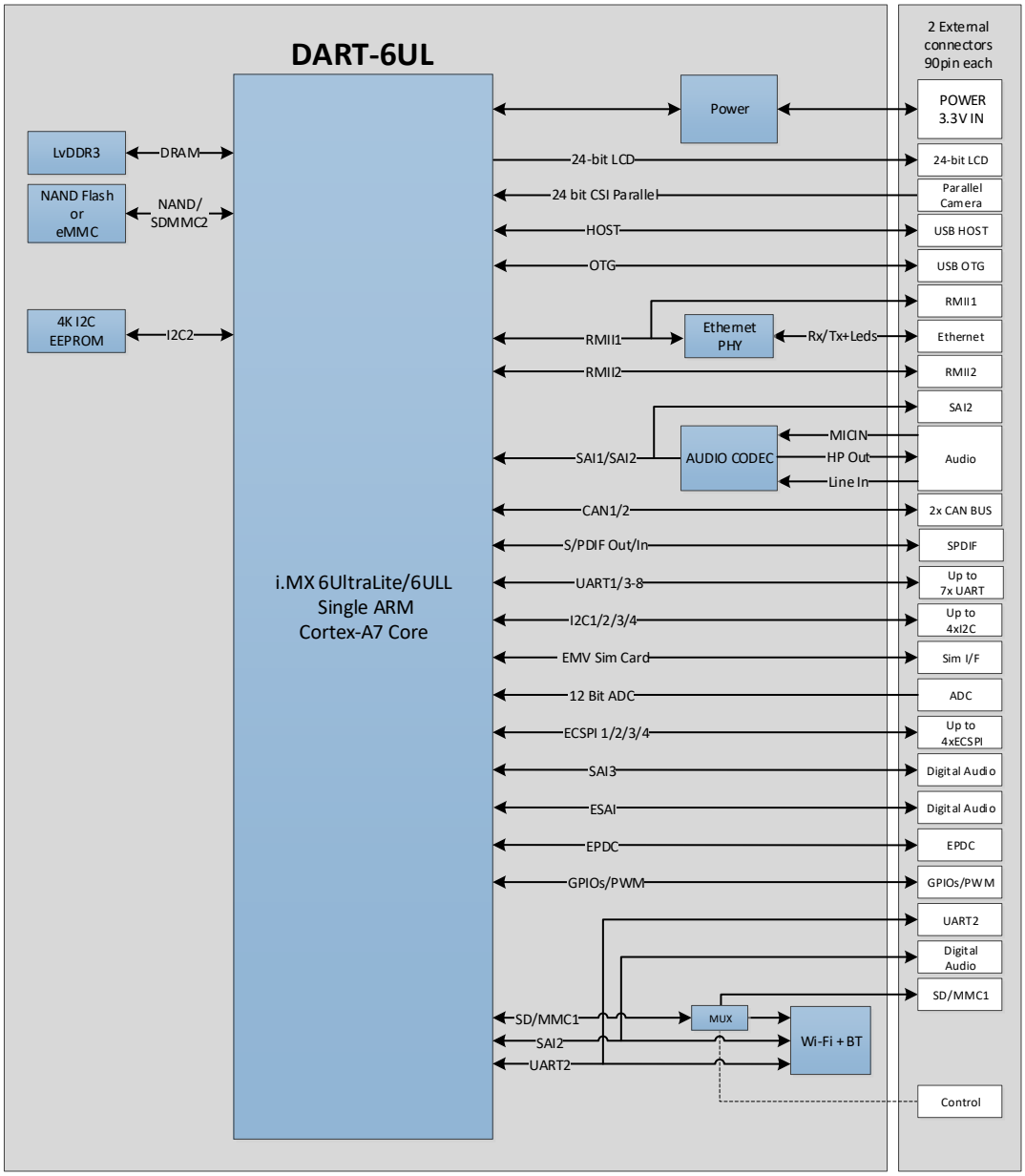

Figure 1-1 SOM Block Diagram

2. Main Hardware Components

This section summarizes the main hardware building blocks of the DART-6UL/DART-6UL-5G

2.1. NXP/Freescale i.MX 6UltraLite / 6ULL

2.1.1. Overview

The i.MX 6UltraLite / 6ULL is a high performance, ultra-efficient processor family with featuring NXP/Freescale's advanced implementation of the single ARM Cortex®-A7 core, which operates at speeds of up to 900MHz. i.MX 6UltraLite / 6ULL includes integrated power management module that reduces the complexity of external power supply and simplifies the power sequencing. Each processor in this family provides various memory interfaces, Quad SPI, and a wide range of other interfaces for connecting peripherals, such as WLAN, Bluetooth™, GPS, displays, and camera sensors. The i.MX 6UltraLite / 6ULL processors are specifically useful for applications such as:

- Electronics Point-of-Sale device
- Telematics
- IoT Gateway
- Access control panels
- Human Machine Interfaces (HMI)
- Smart appliances
- Industrial control and automation

2.1.2. CPU Platform

The i.MX 6UltraLite / 6ULL processors are based on ARM Cortex-A7 MPCore™ Platform, which has the following features:

- Supports single ARM Cortex-A7 MPCore (with TrustZone) with:
  - ✓ 32 KByte L1 Instruction Cache
  - ✓ 32 KByte L1 Data Cache
  - ✓ Private Timer and Watchdog
  - ✓ Cortex-A7 NEON MPE (Media Processing Engine) Co-processor
- General Interrupt Controller (GIC) with 128 interrupts support
- Global Timer
- Snoop Control Unit (SCU)
- 128 KB unified I/D L2 cache
- Single Master AXI bus interface output of L2 cache
- NEON MPE coprocessor
  - ✓ SIMD Media Processing Architecture
  - ✓ NEON register file with 32x64-bit general-purpose registers
  - ✓ NEON Integer execute pipeline (ALU, Shift, MAC)
  - ✓ NEON dual, single-precision floating point execute pipeline (FADD, FMUL)
  - ✓ NEON load/store and permute pipeline
  - ✓ 32 double-precision VFPv3 floating point registers

2.1.3. Memory Interfaces

The SoC-level memory system consists of the following additional components:

- Boot ROM, including HAB (96 KB)
- Internal multimedia/shared, fast access RAM (OCRAM, 128 KB)
- Secure/non-secure RAM (32 KB)

External memory interfaces: The i.MX 6UltraLite / 6ULL processors support latest, high volume, cost effective handheld DRAM, NOR, and NAND Flash memory standards.
SoM Supports:

- 16-bit LV-DDR3-800
- 8-bit NAND-Flash

2.1.4. DMA engine

The SDMA is multi-channel flexible DMA engine. It helps in maximizing system performance by off-loading the various cores in dynamic data routing. It has the following features:

- Powered by a 16-bit Instruction-Set micro-RISC engine
- Multi-channel DMA supporting up to 32 time-division multiplexed DMA channels
- 48 events with total flexibility to trigger any combination of channels
- Memory accesses including linear, FIFO, and 2D addressing
- Shared peripherals between ARM and SDMA Very fast Context-Switching with 2-level priority based preemptive multi-tasking
- DMA units with auto-flush and prefetch capability
- Flexible address management for DMA transfers (increment, decrement, and no address changes on source and destination address)
- DMA ports can handle unit-directional and bi-directional flows (copy mode)
- Up to 8-word buffer for configurable burst transfers for EMIv2.5
- Support of byte-swapping and CRC calculations
- Library of Scripts and API is available

2.1.5. Display Subsystem

The chip display and graphics subsystem consists of the dedicated modules found here.

- LCDIF (LCD interface): 24-bit parallel RGB LCD interface
  The LCDIF is a general purpose display controller that is used to drive a wide range of display devices. These displays can vary in size and capability. Many of these displays have had an asynchronous parallel MPU interface for command and data transfer to an integrated frame buffer. There are other popular displays that support moving pictures and require the RGB interface mode or the VSYNC mode for high-speed data transfers. In addition to these displays, it is also common to provide support for digital video encoders that accept ITU-R BT.656 format 4:2:2 YCbCr digital component video and convert it to analog TV signals. The LCDIF block supports these different interfaces by providing fully programmable functionality. The block has several major features:

- ✓ Bus master interface to source frame buffer data for display refresh and a DMA interface to manage input data transfers from the LCD requiring minimal CPU overhead.
- ✓ 8/16/18/24/32 bit LCD data bus support available depending on I/O mux options.
- ✓ Programmable timing and parameters for MPU, VSYNC and DOTCLK LCD interfaces to support a wide variety of displays.
- ✓ ITU-R BT.656 mode (called Digital Video Interface or DVI mode here) including progressive-to-interlace feature and RGB to YCbCr 4:2:2 color space conversion to support 525/60 and 625/50 operation

- PXP pixel pipeline: pixel/image processing engine for LCD display
  The pixel pipeline is used to perform image processing on image/video buffers before sending to an LCD display. The main features of PXP include:
  - ✓ Multiple input/output format support, including YUV/RGB/Grayscale
  - ✓ Supports both RGB/YUV scaling
  - ✓ Supports overlay with Alpha blending
- CSI (camera sensor interface): up to -bit parallel interface for image sensor
  The CSI enables the chip to connect directly to external CMOS image sensors. CMOS image sensors are separated into two classes, dumb and smart. Dumb sensors are those that support only traditional sensor timing (Vertical SYNC and Horizontal SYNC) and output only Bayer and statistics data, while smart sensors support CCIR656 video decoder formats and perform additional processing of the image (for example, image compression, image pre-filtering, and various data output formats). The capabilities of the CSI include:
  - ✓ Configurable interface logic to support most commonly available CMOS sensors.
  - ✓ Support for CCIR656 video interface as well as traditional sensor interface.
  - ✓ 8-bit/24-bit data port for YCC, YUV, or RGB data input.
  - ✓ 8-bit/10-bit/16-bit data port for Bayer data input.
  - ✓ Full control of 8-bit/pixel, 10-bit/pixel or 16-bit/pixel data format to 32-bit receive FIFO packing.
  - ✓ 128 × 32 FIFO to store received image pixel data. Receive FIFO overrun protection mechanism.
  - ✓ Embedded DMA controllers to transfer data from receive FIFO or statistic FIFO through AHB bus.
  - ✓ Support 2D DMA transfer from the receive FIFO to the frame buffers in the external memory.
  - ✓ Support double buffering two frames in the external memory.
  - ✓ Single interrupt source to interrupt controller from maskable interrupt sources: Start of Frame, End of Frame, Change of Field, FIFO full, FIFO overrun, DMA transfer done, CCIR error and AHB bus response error.
  - ✓ Configurable master clock frequency output to sensor.
  - ✓ Statistic data generation for Auto Exposure (AE) and Auto White Balance (AWB) control of the camera (only for Bayer data and 8-bit/pixel format).

2.1.6. Audio Back End

- Medium Quality Sound (MQS)
  MQS is used to generate medium quality audio via a standard GPIO in the pinmux. The user can connect stereo speakers or headphones to a power amplifier without an additional DAC chip.
  - ✓ 2-channel, MSB-valid 16 bit, MSB first
  - ✓ Frame sync aligned with the left channel data
  - ✓ 44.1 kHZ or 48 kHZ I2S signals from SAI1
  - ✓ SNR target as no more than 20 dB for the signals below 10 kHZ
  - ✓ Signals Over 10 kHZ have worse THD + N values
- Synchronous Audio Interface (SAI)
  - ✓ Transmitter with independent Bit Clock and Frame Sync supporting 1 data line
  - ✓ Receiver with independent Bit Clock and Frame Sync supporting 1 data line
  - ✓ Maximum Frame Size of 32 Words
  - ✓ Word size programmable from 8-bits to 32-bits
  - ✓ Word size configured separately for first word and remaining words in frame.
  - ✓ Asynchronous FIFO for each Transmit and Receive data line
  - ✓ Graceful restart after FIFO Error

- Sony/Philips Digital Interface (SPDIF)
  The Sony/Philips Digital Interface (SPDIF) module is a stereo that allows the processor transmit digital audio over it using the IEC60958 standard, consumer format. i.MX 6UltraLite / 6ULL provides one SPDIF transmitter with one output and one SPDIF receiver with four inputs.
  The SPDIF allows the handling of both SPDIF channel status (CS) and User (U) data. For the SPDIF transmitter, the audio data is provided by the processor via the SPDIFTxLeft and SPDIFTxRight registers, and the data is stored in two 16-word-deep FIFOs, one for the right channel, the other for the left channel. The FIFOs support programmable watermark levels so that FIFO Empty service request can be triggered when the combined number of empty data words locations in both FIFOs is 8, 16, 24 or 32 words. It is recommended to program the watermark level to trigger a FIFO Empty service request when 16 word locations are empty. For optimal performance when servicing the FIFO Empty service request, the FIFOs should be written alternately, starting with the left channel FIFO. The Channel Status bits are also provided via the corresponding registers. The SPDIF transmitter generates an SPDIF output bit stream in the bi-phase mark format (IEC 60958), which consists of audio data, channel status and user bits.
  The data handled by the SPDIF module is 24-bit wide. The 24-bit SPDIF data is aligned in the 24 least significant bits of the 32-bit shared peripheral bus data word. The 8 most significant bits of the 32-bit word are ignored by the SPDIF

Transmitter when data is being stored in the Transmit FIFOs from the peripheral bus. The 8 most significant bits of the 32-bit word are zeroed by the SPDIF Receiver module when the data is being read from the Receiver FIFOs to the peripheral bus. Note that 16-bit data is left-aligned in the 24-bit word format of the SPDIF. When 16-bit data is to be transmitted, the 32-bit word to be written to the SPDIF Transmit FIFOs should be created as follows: the 16-bit data should be located in the middle two bytes of the 32-bit data word and the 8 bits of the LSB must be set to zero, while the 8 bits of the MSB will be ignored.

The SPDIF Transmit clock is generated by the SPDIF internal clock generator module and the clock sources are from outside of the SPDIF block. The clock sources should provide a clock that is at least 64 x Fs, where Fs is the sampling frequency. The external clock source should provide at least 128 x Fs. Clocks of higher frequency may be provided as long as the multiplication factor is a power of 2 (for example, 128x, 256x or 512x). Also, clock frequency precision of 100ppm or better should be provided

2.1.7. 10/100 Ethernet Controller

The core implements a dual speed 10/100 Mbit/s Ethernet MAC compliant with the IEEE802.3-2002 standard. The MAC layer provides compatibility with half- or full duplex 10/100 Mbit/s Ethernet LANs.

The MAC operation is fully programmable and can be used in Network Interface Card (NIC), bridging, or switching applications. The core implements the remote network monitoring (RMON) counters according to IETF RFC 2819.

The core also implements a hardware acceleration block to optimize the performance of network controllers providing TCP/IP, UDP, and ICMP protocol services. The acceleration block performs critical functions in hardware, which are typically implemented with large software overhead.

The core implements programmable embedded FIFOs that can provide buffering on the receive path for lossless flow control.

Advanced power management features are available with magic packet detection and programmable power-down modes.

A unified DMA (uDMA), internal to the ENET module, optimizes data transfer between the ENET core and the SoC, and supports an enhanced buffer descriptor programming model to support IEEE 1588 functionality.

The programmable 10/100 Ethernet MAC with IEEE 1588 integrates a standard IEEE 802.3 Ethernet MAC with a time-stamping module. The IEEE 1588 standard provides accurate clock synchronization for distributed control nodes for industrial automation applications.

Ethernet MAC features

- Implements the full 802.3 specification with preamble/SFD generation, frame padding generation, CRC generation and checking
- Supports zero-length preamble
- Dynamically configurable to support 10/100 Mbit/s operation
- Supports 10/100 Mbit/s full-duplex and configurable half-duplex operation
- Compliant with the AMD magic packet detection with interrupt for node remote power management
- Seamless interface to commercial Ethernet PHY devices via one of the following:

  - ✓ 4-bit Media Independent Interface (MII) operating at 2.5/25 MHz.
  - ✓ 4-bit non-standard MII-Lite (MII without the CRS and COL signals) operating at 2.5/25 MHz.
  - ✓ 2-bit Reduced MII (RMII) operating at 50 MHz.
- Simple 64-Bit FIFO user-application interface
- CRC-32 checking at full speed with optional forwarding of the frame check sequence (FCS) field to the client
- CRC-32 generation and append on transmit or forwarding of user application provided FCS selectable on a per-frame basis
- In full-duplex mode:
  - ✓ Implements automated pause frame (802.3 x31A) generation and termination, providing flow control without user application intervention
  - ✓ Pause quanta used to form pause frames — dynamically programmable
  - ✓ Pause frame generation additionally controllable by user application offering flexible traffic flow control
  - ✓ Optional forwarding of received pause frames to the user application
  - ✓ Implements standard flow-control mechanism
- In half-duplex mode: provides full collision support, including jamming, backoff, and automatic retransmission
- Supports VLAN-tagged frames according to IEEE 802.1Q
- Programmable MAC address: Insertion on transmit; discards frames with mismatching destination address on receive (except broadcast and pause frames)
- Programmable promiscuous mode support to omit MAC destination address checking on receive
- Multicast and unicast address filtering on receive based on 64-entry hash table, reducing higher layer processing load
- Programmable frame maximum length providing support for any standard or proprietary frame length
- Statistics indicators for frame traffic and errors (alignment, CRC, length) and pause frames providing for IEEE 802.3 basic and mandatory management information database (MIB) package and remote network monitoring (RFC 2819)
- Simple handshake user application FIFO interface with fully programmable depth and threshold levels
- Provides separate status word for each received frame on the user interface providing information such as frame length, frame type, VLAN tag, and error information
- Multiple internal loopback options
- MDIO master interface for PHY device configuration and management supports two programmable MDIO base addresses, and standard (IEEE 802.3 Clause 22) and extended (Clause 45) MDIO frame formats
- Supports legacy FEC buffer descriptors
- Interrupt coalescing reduces the number of interrupts generated by the MAC, reducing CPU loading

2.2. Memory

2.2.1. RAM

The DART-6UL/DART-6UL-5G is available with up to 512MB of DDR3L memory.

2.2.2. Non-volatile Storage Memory

The DART-6UL/DART-6UL-5G is available with a variety of non-volatile storage memory options, used for Flash Disk purposes, O.S. run-time-image, Boot-loader and application/user data storage.
The DART-6UL/DART-6UL-5G can arrive with up to 512MB SLC NAND flash or up to 128GB MLC eMMC
(note: it is not possible to use both on-SOM NAND and eMMC at the same time).

2.3. 10/100 Ethernet PHY

The DART-6UL/DART-6UL-5G features Micrel™ KSZ8081RNL Ethernet PHY. KSZ8081 is a single supply 10Base-T/100BaseTX Ethernet physical-layer transceiver for transmission and reception of data over standard CAT-5 unshielded twisted pair (UTP) cable.
The KSZ8081 is a highly integrated PHY solution. It reduces the board cost and simplifies board layout by using on-chip termination resistors for the differential pairs and by integrating a low noise regulator to supply the 1.2V core and by offering 1.8/2.5/3.3V interface support.

2.4. WM8731L Audio

The WM8731L is low power stereo CODEC with an integrated headphone driver. The WM8731/L is designed specifically for portable MP3 audio and speech players and recorders. The WM8731 is also ideal for MD, CD-RW machines and DAT recorders. Stereo line and mono microphone level audio inputs are provided, along with a mute function, programmable line level volume control and a bias voltage output suitable for an electret type microphone. Stereo 24-bit multi-bit sigma delta ADCs and DACs are used with oversampling digital interpolation and decimation filters. Digital audio input word lengths from 16-32 bits and sampling rates from 8kHz to 96kHz are supported. Stereo audio outputs are buffered for driving headphones from a programmable volume control, line level outputs are also provided along with anti-thump mute and power up/down circuitry.
Features:

- Highly Efficient Headphone Driver
- Audio Performance
  - ✓ ADC SNR 90dB ('A' weighted)
  - ✓ DAC SNR 100dB ('A' weighted)
- ADC and DAC Sampling Frequency: 8kHz – 96kHz
- Selectable ADC High Pass Filter
- 2 or 3-Wire MPU Serial Control Interface
- Programmable Audio Data Interface Modes
  - ✓ I2S, Left, Right Justified or DSP
  - ✓ 16/20/24/32 bit Word Lengths

- ✓ Master or Slave Clocking Mode
- Microphone Input and Electret Bias with Side Tone Mixer Digital microphone

2.5. Wi-Fi + BT

2.5.1. DART-6UL-5G

The DART-6UL-5G contains LSR's pre-certified high performance Sterling-LWB5™ Dual band 2.4/5 GHz Wi-Fi® and Bluetooth® Smart Ready Multi-Standard Module based upon the Cypress (formerly Broadcom) CYW43353 chipset supporting 802.11 ac/a/b/g/n, BT 2.1+EDR, and BLE 5.2 wireless connectivity.

2.5.2. DART-6UL

The DART-6UL contains LSR's pre-certified high performance Sterling-LWB™ 2.4 GHz Wi-Fi® and Bluetooth® Smart Ready Multi-Standard Module based upon the Cypress (formerly Broadcom) CYW4343W chipset supporting IEEE 802.11 b/g/n, BT 2.1+EDR, and BLE 5.1 wireless connectivity.

Both the DART-6UL/DART-6UL-5G modules realize the necessary PHY/MAC layers to support WLAN applications in conjunction with a host processor over a SDIO interface. The modules also provide a Bluetooth/BLE platform through the HCI transport layer. Both WLAN and Bluetooth share the same antenna port.

DART-6UL/DART-6UL-5G Key Features:

- IEEE 802.11 ac/a/b/g/n (**DART-6UL-5G**)
- IEEE 802.11 b/g/n (**DART-6UL**)
- Bluetooth 2.1+EDR, and BLE 5.2
- U.FL connector for external antenna
- Latest Linux and Android drivers supported directly by LSR and Cypress
- Wi-Fi/BT module Broad certifications with multiple antennas: FCC (USA), IC (Canada), ETSI (Europe), Giteki (Japan), and RCM (AU/NZ)
- Industrial operating Temperature Range: -40 to +85

3. External Connectors

The DART-6UL/DART-6UL-5G exposes two 90-pin Board To Board connectors. The recommended mating connectors for baseboard interfacing are Hirose DF40C-90DS-0.4V(51)

Figure 3-1 SOM J1 Connector

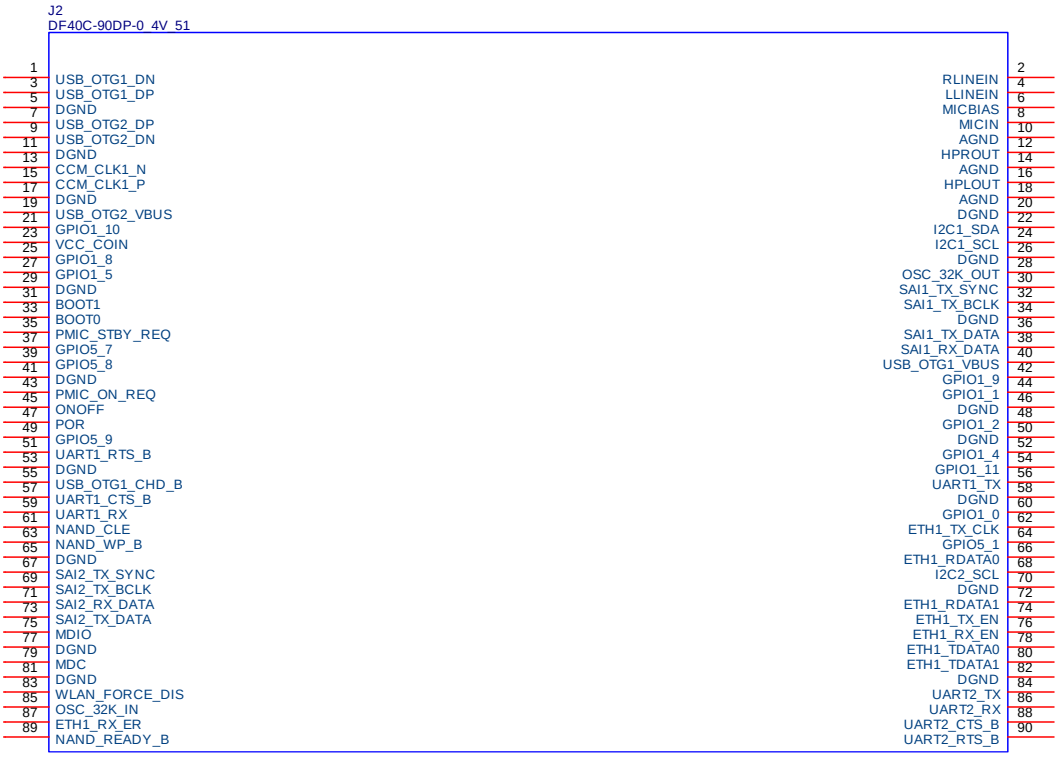

Figure 3-2 SOM J2 Connector

3.1. DART-6UL/DART-6UL-5G Connector Pin-out

Pin #	Name	Description	Notes	Ball
J1.1	ETH_RXDN	Ethernet 1 RX Data Differential Negative	NC if Ethernet PHY is not assembled	KSZ8051RNL.4
J1.2	LCD_DATA22	LCD Interface Data 22	See note [1] below	SOC.A14
J1.3	ETH_RXDP	Ethernet 1 RX Data Differential Positive	NC if Ethernet PHY is not assembled	KSZ8051RNL.5
J1.4	LCD_DATA20	LCD Interface Data 20	See note [1] below	SOC.C14
J1.5	LINKSPEED	Ethernet 1 Speed LED	NC if Ethernet PHY is not assembled	KSZ8051RNL.31
J1.6	LCD_DATA16	LCD Interface Data 16	See note [1] below	SOC.C13
J1.7	LINKLED	Ethernet 1 Link LED	NC if Ethernet PHY is not assembled	KSZ8051RNL.30
J1.8	LCD_DATA18	LCD Interface Data 18	See note [1] below	SOC.A13
J1.9	ETH_TXDN	Ethernet 1 TX Data Differential Negative	NC if Ethernet PHY is not assembled	KSZ8051RNL.6
J1.10	LCD_DATA17	LCD Interface Data 17	See note [1] below	SOC.B13
J1.11	ETH_TXDP	Ethernet 1 TX Data Differential Positive	NC if Ethernet PHY is not assembled	KSZ8051RNL.7
J1.12	DGND	Digital Ground		SOC.N7
J1.13	VCC_3V3_IN	3.3V Main power supply input		
J1.14	LCD_DATA13	LCD Interface Data 13	See note [1] below	SOC.B12
J1.15	VCC_3V3_IN	3.3V Main power supply input		
J1.16	LCD_DATA14	LCD Interface Data 14	See note [1] below	SOC.A12
J1.17	VCC_3V3_IN	3.3V Main power supply input		
J1.18	LCD_DATA12	LCD Interface Data 12	See note [1] below	SOC.C12
J1.19	VCC_3V3_IN	3.3V Main power supply input		
J1.20	LCD_DATA8	LCD Interface Data 8	See note [1] below	SOC.B11
J1.21	VCC_3V3_IN	3.3V Main power supply input		
J1.22	LCD_DATA9	LCD Interface Data 9	See note [1] below	SOC.A11
J1.23	VCC_3V3_IN	3.3V Main power supply input		
J1.24	DGND	Digital Ground		SOC.N7
J1.25	VCC_3V3_IN	3.3V Main power supply input		
J1.26	LCD_DATA4	LCD Interface Data 4	See note [1] below	SOC.C10
J1.27	VCC_3V3_IN	3.3V Main power supply input		
J1.28	LCD_DATA5	LCD Interface Data 5	See note [1] below	SOC.B10
J1.29	DGND	Digital Ground		SOC.N7
J1.30	LCD_DATA6	LCD Interface Data 6	See note [1] below	SOC.A10
J1.31	ETH2_RX_EN	Ethernet 2 RX Enable		SOC.B17
J1.32	LCD_DATA19	LCD Interface Data 19	See note [1] below	SOC.D14
J1.33	LCD_DATA23	LCD Interface Data 23	See note [1] below	SOC.B16
J1.34	LCD_DATA15	LCD Interface Data 15	See note [1] below	SOC.D13
J1.35	ETH2_TDATA1	Ethernet 2 TX 1 Data		SOC.A16
J1.36	DGND	Digital Ground		SOC.N7
J1.37	ETH2_RDATA0	Ethernet 2 RX 0 Data		SOC.C17
J1.38	LCD_DATA1	LCD Interface Data 1	See note [1] below	SOC.A9
J1.39	ETH2_RDATA1	Ethernet 2 RX 1 Data		SOC.C16
J1.40	LCD_DATA3	LCD Interface Data 3	See note [1] below	SOC.D10

Pin #	Name	Description	Notes	Ball
J1.41	DGND	Digital Ground		SOC.N7
J1.42	LCD_DATA7	LCD Interface Data 7	See note [1] below	SOC.D11
J1.43	ETH2_TDATA0	Ethernet 2 TX 0 Data		SOC.A15
J1.44	LCD_DATA0	LCD Interface Data 0	See note [1] below	SOC.B9
J1.45	ETH2_TX_EN	Ethernet 2 TX Enable		SOC.B15
J1.46	LCD_DATA10	LCD Interface Data 10	See note [1] below	SOC.E12
J1.47	LCD_DATA21	LCD Interface Data 21	See note [1] below	SOC.B14
J1.48	DGND	Digital Ground		SOC.N7
J1.49	LCD_CLK	LCD Interface Pixel Clock		SOC.A8
J1.50	LCD_ENABLE	LCD Interface Data Enable		SOC.B8
J1.51	GPIO5_5	General Purpose Input Output Register 5 Bit 5		SOC.N8
J1.52	LCD_VSYNC	LCD Interface Vertical Sync		SOC.C9
J1.53	DGND	Digital Ground		SOC.N7
J1.54	LCD_HSYNC	LCD Interface Horizontal Sync		SOC.D9
J1.55	ETH2_RX_ER	Ethernet 2 RX Error		SOC.D16
J1.56	LCD_RESET	LCD Interface Reset		SOC.E9
J1.57	ETH2_TX_CLK	Ethernet 2 TX Clock		SOC.D17
J1.58	NAND_CE1_B	NAND Chip Enable 1		SOC.B5
J1.59	UART3_TX	Uart 3 TX		SOC.H17
J1.60	DGND	Digital Ground		SOC.N7
J1.61	UART3_RX	Uart 3 RX		SOC.H16
J1.62	NAND_DQS	NAND Interface DQS	Function Must not be Altered if NAND is assembled	SOC.E6
J1.63	GPIO5_3	General Purpose Input Output Register 5 Bit 3		SOC.P10
J1.64	GPIO4_18	General Purpose Input Output Register 4 Bit 18		SOC.E5
J1.65	DGND	Digital Ground		SOC.N7
J1.66	SD1_DATA3	SD Card 1 Interface Data 1 Signal	Not connected when the Wi-Fi is enabled	SOC.A2 (via TXS02612)
J1.67	UART3_CTS_B	Uart 3 CTS		SOC.H15
J1.68	SD1_DATA0	SD Card 1 Interface Data 0 Signal	Not connected when the Wi-Fi is enabled	SOC.B3 (via TXS02612)
J1.69	UART3_RTS_B	Uart 3 RTS		SOC.G14
J1.70	DGND	Digital Ground		SOC.N7
J1.71	I2C2_SDA	I2C Bus 2 Data	Function Must not be altered	SOC.G13
J1.72	DGND	Digital Ground		SOC.N7
J1.73	LCD_DATA11	LCD Interface Data 11	See note [1] below	SOC.D12
J1.74	SD1_DATA1	SD Card 1 Interface Data 1 Signal	Not connected when the Wi-Fi is enabled	SOC.B2 (via TXS02612)
J1.75	LCD_DATA2	LCD Interface Data 2	See note [1] below	SOC.E10
J1.76	GPIO4_17	General Purpose Input Output Register 4 Bit 17		SOC.F5
J1.77	DGND	Digital Ground		SOC.N7
J1.78	SD1_DATA2	SD Card 1 Interface Data 1 Signal	Not connected when the Wi-Fi is enabled	SOC.B1 (via TXS02612)
J1.79	DGND	Digital Ground		SOC.N7
J1.80	GPIO4_21	General Purpose Input Output Register 4 Bit 21		SOC.E4

Pin #	Name	Description	Notes	Ball
J1.81	DGND	Digital Ground		SOC.N7
J1.82	SD1_CMD	SD Card 1 Interface Command Signal	Not connected when the Wi-Fi is enabled	SOC.C2 (via TXS02612)
J1.83	SD1_CLK	SD Card 1 Interface Clock Signal	Not connected when the Wi-Fi is enabled	SOC.C1 (via TXS02612)
J1.84	DGND	Digital Ground		SOC.N7
J1.85	DGND	Digital Ground		SOC.N7
J1.86	GPIO4_20	General Purpose Input Output Register 4 Bit 20		SOC.F3
J1.87	GPIO4_24	General Purpose Input Output Register 4 Bit 24		SOC.E1
J1.88	GPIO4_22	General Purpose Input Output Register 4 Bit 22		SOC.E3
J1.89	GPIO4_19	General Purpose Input Output Register 4 Bit 19		SOC.F2
J1.90	GPIO4_23	General Purpose Input Output Register 4 Bit 23		SOC.E2
J2.1	USB_OTG1_DN	USB Host 1 Data Negative		SOC.T15
J2.2	RLINEIN	Audio Interface Line In Right	NC if the Audio chip is not assembled	WM8731L.14
J2.3	USB_OTG1_DP	USB Host 1 Data Positive		SOC.U15
J2.4	LLINEIN	Audio Interface Line In Left	NC if the Audio chip is not assembled	WM8731L.13
J2.5	DGND	Digital Ground		SOC.N7
J2.6	MICBIAS	Audio Interface Microphone Bias	NC if the Audio chip is not assembled	WM8731L.21
J2.7	USB_OTG2_DP	USB Host 2 Data Positive		SOC.U13
J2.8	MICIN	Audio Interface Microphone In	NC if the Audio chip is not assembled	WM8731L.22
J2.9	USB_OTG2_DN	USB Host 2 Data Negative		SOC.T13
J2.10	AGND	Audio Interface Ground Reference		WM8731L.19
J2.11	DGND	Digital Ground		SOC.N7
J2.12	HPROUT	Audio Interface Headphones Right Output	NC if the Audio chip is not assembled	WM8731L.14
J2.13	CCM_CLK1_N	CCM clock Differential Negative		SOC.P16
J2.14	AGND	Audio Interface Ground Reference		WM8731L.15
J2.15	CCM_CLK1_P	CCM clock Differential Negative		SOC.P17
J2.16	HPLOUT	Audio Interface Headphones Left Output	NC if the Audio chip is not assembled	WM8731L.13
J2.17	DGND	Digital Ground		SOC.N7
J2.18	AGND	Audio Interface Ground Reference		WM8731L.19
J2.19	USB_OTG2_VBUS	USB Host 2 Vbus		SOC.U12
J2.20	DGND	Digital Ground		SOC.N7
J2.21	GPIO1_10	General Purpose Input Output Register 1 Bit 10		SOC.P15
J2.22	I2C1_SDA	I2C Bus 1 Data		SOC.G16
J2.23	VCC_COIN	RTC Clock power supply	Must be connected to coin or 3.3V even if the RTC is not used	SOC.P12
J2.24	I2C1_SCL	I2C Bus 1 Clock		SOC.G17
J2.25	GPIO1_8	General Purpose Input Output Register 1 Bit 8		SOC.N17
J2.26	DGND	Digital Ground		SOC.N7
J2.27	GPIO1_5	General Purpose Input Output Register 1 Bit 5		SOC.M17
J2.28	OSC_32K_OUT	32KHz reference clock	Reference Clock out for Wi-Fi module. It is also part of TSC controller. It may be connected to J2.85 if TSC controller is not in use	SOC.L17
J2.29	DGND	Digital Ground		SOC.N7

Pin #	Name	Description	Notes	Ball
J2.30	SAI1_TX_SYNC	SAI1 Frame Sync	Used on subset of SoMs that has both BT Audio and Audio Codec in use.	SOC.D4
J2.31	BOOT1	Boot mode bit 1 signal	See note [1] below	SOC.U10
J2.32	SAI1_TX_BCLK	SAI1 TX Byte Clock	Used on subset of SoMs that has both BT Audio and Audio Codec in use.	SOC.D3
J2.33	BOOT0	Boot mode bit 0 signal	See note [1] below	SOC.T10
J2.34	DGND	Digital Ground		SOC.N7
J2.35	PMIC_STBY_REQ	Standby request output from the CPU		SOC.U9
J2.36	SAI1_TX_DATA	SAI1 TX Data	Used on subset of SoMs that has both BT Audio and Audio Codec in use.	SOC.D1
J2.37	GPIO5_7	General Purpose Input Output Register 5 Bit 7		SOC.N10
J2.38	SAI1_RX_DATA	SAI1 RX Data	Used on subset of SoMs that has both BT Audio and Audio Codec in use.	SOC.D2
J2.39	GPIO5_8	General Purpose Input Output Register 5 Bit 8		SOC.N9
J2.40	USB_OTG1_VBUS	USB Host 1 Vbus		SOC.T12
J2.41	DGND	Digital Ground		SOC.N7
J2.42	GPIO1_9	General Purpose Input Output Register 1 Bit 9		SOC.M15
J2.43	PMIC_ON_REQ	Power On signal request output from the CPU		SOC.T9
J2.44	GPIO1_1	General Purpose Input Output Register 1 Bit 1		SOC.L15
J2.45	ONOFF	On Off signal of the CPU		SOC.R8
J2.46	DGND	Digital Ground		SOC.N7
J2.47	POR	System Reset		SOC.P8
J2.48	GPIO1_2	General Purpose Input Output Register 1 Bit 2		SOC.L14
J2.49	GPIO5_9	General Purpose Input Output Register 5 Bit 9		SOC.R6
J2.50	DGND	Digital Ground		SOC.N7
J2.51	UART1_RTS_B	Debug UART RTS		SOC.J14
J2.52	GPIO1_4	General Purpose Input Output Register 1 Bit 4		SOC.M16
J2.53	DGND	Digital Ground		SOC.N7
J2.54	SAI1_MCLK	SAI1 Master Clock	Must be NC if AUDIO chip is assembled on the SOM. Used as CLOCK for SAI1 interface	SOC.P14
J2.55	USB_OTG1_CHD_B	USB Host 1 Charger Detect		SOC.U16
J2.56	UART1_TX	Debug UART TX		SOC.K14
J2.57	UART1_CTS_B	Debug UART CTS		SOC.K15
J2.58	DGND	Digital Ground		
J2.59	UART1_RX	Debug UART RX		SOC.K16
J2.60	GPIO1_0	General Purpose Input Output Register 1 Bit 0		SOC.K13
J2.61	NAND_CLE	NAND Interface CLE	Function Must not be Altered if NAND is assembled	SOC.A4
J2.62	ETH1_TX_CLK	Ethernet 1 TX Clock		SOC.F14
J2.63	NAND_WP_B	NAND Interface WP	Function Must not be Altered if NAND is assembled	SOC.D5
J2.64	GPIO5_1	General Purpose Input Output Register 5 Bit 1		SOC.R9
J2.65	DGND	Digital Ground		SOC.N7

Pin #	Name	Description	Notes	Ball
J2.66	ETH1_RDATA0	Ethernet 1 RX 0 Data	Must be NC if Ethernet PHY is assembled	SOC.F16
J2.67	SAI2_TX_SYNC	Audio Codec or Bluetooth Frame Sync	Must be NC if Wi-Fi is assembled and SoM has BT Audio or when Audio codec in use	SOC.N15
J2.68	I2C2_SCL	I2C Bus 2 Clock	Function Must not be altered	SOC.F17
J2.69	SAI2_TX_BCLK	Audio Codec or Bluetooth TX Byte Clock	Must be NC if Wi-Fi is assembled and SoM has BT Audio or when Audio codec in use	SOC.N16
J2.70	DGND	Digital Ground		SOC.N7
J2.71	SAI2_RX_DATA	Audio Codec or Bluetooth RX Data	Must be NC if Wi-Fi is assembled and SoM has BT Audio or when Audio codec in use	SOC.M14
J2.72	ETH1_RDATA1	Ethernet 1 RX 1 Data	Must be NC if Ethernet PHY is assembled	SOC.E17
J2.73	SAI2_TX_DATA	Audio Codec or Bluetooth TX Data	Must be NC if Wi-Fi is assembled and SoM has BT Audio or when Audio codec in use	SOC.N14
J2.74	ETH1_TX_EN	Ethernet 1 TX Enable	Must be NC if Ethernet PHY is assembled	SOC.F15
J2.75	MDIO	Management Data input/output Interface Data	Function Must not be Altered if Ethernet PHY is assembled	SOC.K17
J2.76	ETH1_RX_EN	Ethernet 1 RX Enable	Must be NC if Ethernet PHY is assembled	SOC.E16
J2.77	DART-6UL: DGND	Digital Ground	In DART-6UL connect pin to DGND	SOC.N7
	DART-6UL-5G: SD_VSELECT	Optional manual setting of SD1 voltage level: When High-1.8V, When low - 3.3V.	For all DART-6UL-5G SOMs **not assembled** with iMX6UL 'G3' variant: Voltage is set automatically via SW-**Pin should be connected to DGND**. For DART-6UL-5G SOMs **assembled** with iMX6UL 'G3' variant and WiFi: When routing SD1 interface to WiFi - Connect this pin to 3.3V. When routing SD1 interface to J1- Connect this pin to DGND. (see also section 4.5)	
J2.78	ETH1_TDATA0	Ethernet 1 TX 0 Data	Must be NC if Ethernet PHY is assembled	SOC.E15
J2.79	MDC	Management Data input/output Interface Clock	Function Must not be Altered if Ethernet PHY is assembled	SOC.L16
J2.80	ETH1_TDATA1	Ethernet 1 TX 1 Data	Must be NC if Ethernet PHY is assembled	SOC.E14
J2.81	DGND	Digital Ground		SOC.N7
J2.82	DGND	Digital Ground		SOC.N7
J2.83	WLAN_FORCE_DIS	Wi-Fi Mux disable	Setting this pin to low will disconnect the SD1 from Wi-Fi and connect it J1.	
J2.84	UART2_TX	Bluetooth UART TX	DART-6UL: Must be NC if Wi-Fi is assembled and BT_DISABLE is not high DART-6UL-5G: Must be NC in SOM variants with Bluetooth assembled.	SOC.J17
J2.85	OSC_32K_IN	Wi-Fi 32Khz oscillator input	Can be connected to J2.28 if TSC controller is not in use.	

Pin #	Name	Description	Notes	Ball
J2.86	UART2_RX	Bluetooth UART RX	DART-6UL: Must be NC if Wi-Fi is assembled and BT_DISABLE is not high DART-6UL-5G: Must be NC in SOM variants with Bluetooth assembled.	SOC.J16
J2.87	ETH1_RX_ER	Ethernet 1 RX Error	Must be NC if Ethernet PHY is assembled	SOC.D15
J2.88	UART2_CTS_B	Bluetooth UART CTS	DART-6UL: Must be NC if Wi-Fi is assembled and BT_DISABLE is not high DART-6UL-5G: Must be NC in SOM variants with Bluetooth assembled.	SOC.J15
J2.89	NAND_READY_B	NAND Interface READY	Function Must not be Altered if NAND is assembled	SOC.A3
J2.90	UART2_RTS_B	Bluetooth UART RTS	DART-6UL: Must be NC if Wi-Fi is assembled and BT_DISABLE is not high DART-6UL-5G: Must be NC in SOM variants with Bluetooth assembled.	SOC.H14

Table 3-1 SOM connectors pin out

Note [1]:
Pin is being latched at boot to determine boot configuration.
External drivers to this pin should be disabled in time of boot otherwise they may change the boot option and the SOM will not boot. For more information please see section 5.

4. SOM's interfaces

4.1. LCD port

The SOM exposes one 24bit LCD interface with the following capabilities:

- Bus master interface to source frame buffer data for display refresh and a DMA interface to manage input data transfers from the LCD requiring minimal CPU overhead.
- 8/16/18/24 bit LCD data bus support available depending on I/O mux options.
- Programmable timing and parameters for MPU, VSYNC and DOTCLK LCD interfaces to support a wide variety of displays.
- ITU-R BT.656 mode (called Digital Video Interface or DVI mode here) including progressive-to-interlace feature and RGB to YCbCr 4:2:2 color space conversion to support 525/60 and 625/50 operation

Pin#	Name	Description	Ball
J1.49	LCD_CLK	LCD Interface Pixel Clock	SOC.A8
J1.44[1]	LCD_DATA[0]	LCD Interface Data 0	SOC.B9
J1.38[1]	LCD_DATA[1]	LCD Interface Data 1	SOC.A9
J1.46[1]	LCD_DATA[10]	LCD Interface Data 10	SOC.E12
J1.73[1]	LCD_DATA[11]	LCD Interface Data 11	SOC.D12
J1.18[1]	LCD_DATA[12]	LCD Interface Data 12	SOC.C12
J1.14[1]	LCD_DATA[13]	LCD Interface Data 13	SOC.B12
J1.16[1]	LCD_DATA[14]	LCD Interface Data 14	SOC.A12
J1.34[1]	LCD_DATA[15]	LCD Interface Data 15	SOC.D13
J1.06[1]	LCD_DATA[16]	LCD Interface Data 16	SOC.C13
J1.10[1]	LCD_DATA[17]	LCD Interface Data 17	SOC.B13
J1.08[1]	LCD_DATA[18]	LCD Interface Data 18	SOC.A13
J1.32[1]	LCD_DATA[19]	LCD Interface Data 19	SOC.D14
J1.75[1]	LCD_DATA[2]	LCD Interface Data 2	SOC.E10
J1.04[1]	LCD_DATA[20]	LCD Interface Data 20	SOC.C14
J1.47[1]	LCD_DATA[21]	LCD Interface Data 21	SOC.B14
J1.02[1]	LCD_DATA[22]	LCD Interface Data 22	SOC.A14
J1.33[1]	LCD_DATA[23]	LCD Interface Data 23	SOC.B16
J1.40[1]	LCD_DATA[3]	LCD Interface Data 3	SOC.D10
J1.26[1]	LCD_DATA[4]	LCD Interface Data 4	SOC.C10
J1.28[1]	LCD_DATA[5]	LCD Interface Data 5	SOC.B10
J1.30[1]	LCD_DATA[6]	LCD Interface Data 6	SOC.A10
J1.42[1]	LCD_DATA[7]	LCD Interface Data 7	SOC.D11
J1.20[1]	LCD_DATA[8]	LCD Interface Data 8	SOC.B11
J1.22[1]	LCD_DATA[9]	LCD Interface Data 9	SOC.A11
J1.50	LCD_ENABLE	LCD Interface Data Enable	SOC.B8
J1.54	LCD_HSYNC	LCD Interface Horizontal Sync	SOC.D9
J1.56	LCD_RESET	LCD Interface Reset	SOC.E9
J1.52	LCD_VSYNC	LCD Interface Vertical Sync	SOC.C9

Table 4-1 LCD Interface signals

Note: Pins marked with [1] are being latched at boot to determine boot configuration. External drivers to these pins should be disabled in time of boot otherwise they may change the boot option and the SOM will not boot. For more information please see section 5.

4.2. EPDC

The SOM exposes The EPDC is a feature-rich, low power and high performance direct drive active matrix EPD controller. It is specifically designed to drive E-INK EPD panels supporting a wide variety of TFT backplanes.

Key features of the EPDC are as follows:

- TFT resolutions up to 4096 x 4096 pixels with 20 Hz refresh (programmable up to 8191 x 8191)
- TFT resolutions up to 1650 x 2332 pixels at 106 Hz refresh
- Industry standard bus interfaces (AMBA AXI and APB)
- Up to 5-bit pixel representation for up to 32 greyscale levels

Note: The EPDC interface is available in iMX6ULL based SOMs only.

Pin#	Name	Description	Ball
J1.49	EPDC_SDCLK	Positive Source Driver-Shift Clock	SOC.A8
J1.14[1]	EPDC_BDR[0]	Panel-Border Control	SOC.B12
J1.08[1]	EPDC_BDR[1]	Panel-Border Control	SOC.A13
J1.06[1]	EPDC_GDCLK	Gate Driver-Clock	SOC.C13
J1.56	EPDC_GDOE	Gate Driver-Output Enable	SOC.E9
J1.34[1]	EPDC_GDRL	Gate Driver-Shift direction	SOC.D13
J1.10[1]	EPDC_GDSP	Gate Driver-Start Pulse	SOC.B13
J1.46[1]	EPDC_PWRCOM	Panel-Power control	SOC.E12
J1.18[1]	EPDC_PWRCTRL[0]	Panel-Power control	SOC.C12
J2.22	EPDC_PWRCTRL[1]	Panel-Power control	SOC.G16
J1.20[1]	EPDC_PWRIRQ	Panel-Power irq	SOC.B11
J1.73[1]	EPDC_PWRSTAT	Panel-Power status good	SOC.D12
J1.22[1]	EPDC_PWRWAKE	Panel-Power control wake signal	SOC.A11
J1.52	EPDC_SDCE[0]	Source Driver-Chip-enable/StartPulse	SOC.C9
J1.47[1]	EPDC_SDCE[1]	Source Driver-Chip-enable/StartPulse	SOC.B14
J1.02[1]	EPDC_SDCE[2]	Source Driver-Chip-enable/StartPulse	SOC.A14
J1.33[1]	EPDC_SDCE[3]	Source Driver-Chip-enable/StartPulse	SOC.B16
J2.66*	EPDC_SDCE[4]	Source Driver-Chip-enable/StartPulse	SOC.F16
J2.72*	EPDC_SDCE[5]	Source Driver-Chip-enable/StartPulse	SOC.E17
J2.76*	EPDC_SDCE[6]	Source Driver-Chip-enable/StartPulse	SOC.E16
J2.78*	EPDC_SDCE[7]	Source Driver-Chip-enable/StartPulse	SOC.E15
J2.80*	EPDC_SDCE[8]	Source Driver-Chip-enable/StartPulse	SOC.E14
J2.74*	EPDC_SDCE[9]	Source Driver-Chip-enable/StartPulse	SOC.F15
J1.44[1]	EPDC_SDDO[0]	Source Driver-Shift signal	SOC.B9
J1.38[1]	EPDC_SDDO[1]	Source Driver-Shift signal	SOC.A9
J1.31	EPDC_SDDO[10]	Source Driver-Shift signal	SOC.B17
J1.43	EPDC_SDDO[11]	Source Driver-Shift signal	SOC.A15
J1.35	EPDC_SDDO[12]	Source Driver-Shift signal	SOC.A16
J1.45	EPDC_SDDO[13]	Source Driver-Shift signal	SOC.B15
J1.57	EPDC_SDDO[14]	Source Driver-Shift signal	SOC.D17
J1.55	EPDC_SDDO[15]	Source Driver-Shift signal	SOC.D16
J1.75[1]	EPDC_SDDO[2]	Source Driver-Shift signal	SOC.E10
J1.40[1]	EPDC_SDDO[3]	Source Driver-Shift signal	SOC.D10
J1.26[1]	EPDC_SDDO[4]	Source Driver-Shift signal	SOC.C10
J1.28[1]	EPDC_SDDO[5]	Source Driver-Shift signal	SOC.B10
J1.30[1]	EPDC_SDDO[6]	Source Driver-Shift signal	SOC.A10
J1.42[1]	EPDC_SDDO[7]	Source Driver-Shift signal	SOC.D11

Pin#	Name	Description	Ball
J1.37	EPDC_SDDO[8]	Source Driver-Shift signal	SOC.C17
J1.39	EPDC_SDDO[9]	Source Driver-Shift signal	SOC.C16
J1.50	EPDC_SDLE	Source Driver-Latch Enable	SOC.B8
J1.54	EPDC_SDOE	Source Driver-Output Enable	SOC.D9
J2.62*	EPDC_SDOED	Source Driver-Output Enable (to VDD)	SOC.F14
J2.87*	EPDC_SDOEZ	Source Driver-Output Enable (to Zero)	SOC.D15
J1.16[1]	EPDC_SDSHR	Source Driver-Shift dir	SOC.A12
J1.32[1]	EPDC_VCOM[0]	Panel-VCOM	SOC.D14
J1.04[1]	EPDC_VCOM[1]	Panel-VCOM	SOC.C14

Table 4-2 EPDC Interface signals

Note: Pins marked with * are used on SOM internal connections and can be used on the specific subsets of SOM. In other case the signals must be left floating.

Note: Pins marked with [1] are being latched at boot to determine boot configuration. External drivers to these pins should be disabled in time of boot otherwise they may change the boot option and the SOM will not boot. For more information please see section 5.

4.3. Synchronous Audio Interface (SAI)

The SOM exposes 3 Synchronous Audio Interfaces, one of them used internally by audio codec or/and by Bluetooth Audio. SAI2 is used by Audio Codec SAI1 is not accessible and is used only on SoMs that have two audio interfaces both Bluetooth Audio and Analog Audio Codec.

- Transmitter with independent Bit Clock and Frame Sync supporting 1 data line
- Receiver with independent Bit Clock and Frame Sync supporting 1 data line
- Maximum Frame Size of 32 Words
- Word size programmable from 8-bits to 32-bits
- Word size configured separately for first word and remaining words in frame.
- Asynchronous FIFO for each Transmit and Receive data line
- Graceful restart after FIFO Error

The SOM exposes 1 Mono Analog Microphone, 1 Stereo Line In input and 1 Headset Interface. Audio is provided via WM8731L audio codec.

Pin#	Name	Description	Notes
J2.4	LLINEIN	Audio Interface Line In Left	NC if the Audio chip is not assembled
J2.16	HPLOUT	Audio Interface Headphones Left Output	NC if the Audio chip is not assembled
J2.2	RLINEIN	Audio Interface Line In Right	NC if the Audio chip is not assembled
J2.12	HPROUT	Audio Interface Headphones Right Output	NC if the Audio chip is not assembled
J2.14	AGND	Audio Interface Ground Reference	
J2.10	AGND	Audio Interface Ground Reference	
J2.18	AGND	Audio Interface Ground Reference	
J2.6	MICBIAS	Audio Interface Microphone Bias	NC if the Audio chip is not assembled
J2.8	MICIN	Audio Interface Microphone In	NC if the Audio chip is not assembled

Table 4-3 Audio Interface signals

Pin#	Name	Description	Ball
J1.44[1]	SAI1_MCLK	Serial Audio Interface 1 Master Clock	SOC.B9
J1.88	SAI1_MCLK	Serial Audio Interface 1 Master Clock	SOC.E3
J1.87	SAI1_RX_BCLK	Serial Audio Interface 1 Byte Clock	SOC.E1
J1.40[1]	SAI1_RX_DATA	Serial Audio Interface 1 RX Data	SOC.D10
J2.38*	SAI1_RX_DATA	Serial Audio Interface 1 RX Data	SOC.D2
J1.90	SAI1_RX_SYNC	Serial Audio Interface 1 RX Sync	SOC.E2
J1.75[1]	SAI1_TX_BCLK	Serial Audio Interface 1 Byte Clock	SOC.E10
J2.32*	SAI1_TX_BCLK	Serial Audio Interface 1 Byte Clock	SOC.D3
J1.26[1]	SAI1_TX_DATA	Serial Audio Interface 1 TX Data	SOC.C10
J2.36*	SAI1_TX_DATA	Serial Audio Interface 1 TX Data	SOC.D1
J1.38[1]	SAI1_TX_SYNC	Serial Audio Interface 1 TX Sync	SOC.A9
J2.30*	SAI1_TX_SYNC	Serial Audio Interface 1 TX Sync	SOC.D4
J1.83*	SAI2_MCLK	Serial Audio Interface 2 Master Clock	SOC.C1
J2.54*	SAI2_MCLK	Serial Audio Interface 2 Master Clock	SOC.P14
J1.78*	SAI2_RX_DATA	Serial Audio Interface 2 RX Data	SOC.B1

Pin#	Name	Description	Ball
J2.71*	SAI2_RX_DATA	Serial Audio Interface 2 RX Data	SOC.M14
J1.82*	SAI2_RX_SYNC	Serial Audio Interface 2 RX Sync	SOC.C2
J1.74*	SAI2_TX_BCLK	Serial Audio Interface 2 Byte Clock	SOC.B2
J2.69*	SAI2_TX_BCLK	Serial Audio Interface 2 Byte Clock	SOC.N16
J1.66*	SAI2_TX_DATA	Serial Audio Interface 2 TX Data	SOC.A2
J2.73*	SAI2_TX_DATA	Serial Audio Interface 2 TX Data	SOC.N14
J1.68*	SAI2_TX_SYNC	Serial Audio Interface 2 TX Sync	SOC.B3
J2.67*	SAI2_TX_SYNC	Serial Audio Interface 2 TX Sync	SOC.N15
J1.49	SAI3_MCLK	Serial Audio Interface 3 Master Clock	SOC.A8
J1.22[1]	SAI3_MCLK	Serial Audio Interface 3 Master Clock	SOC.A11
J1.73[1]	SAI3_RX_BCLK	Serial Audio Interface 3 Byte Clock	SOC.D12
J1.16[1]	SAI3_RX_DATA	Serial Audio Interface 3 RX Data	SOC.A12
J1.52	SAI3_RX_DATA	Serial Audio Interface 3 RX Data	SOC.C9
J1.46[1]	SAI3_RX_SYNC	Serial Audio Interface 3 RX Sync	SOC.E12
J1.14[1]	SAI3_TX_BCLK	Serial Audio Interface 3 Byte Clock	SOC.B12
J1.54	SAI3_TX_BCLK	Serial Audio Interface 3 Byte Clock	SOC.D9
J1.34[1]	SAI3_TX_DATA	Serial Audio Interface 3 TX Data	SOC.D13
J1.56	SAI3_TX_DATA	Serial Audio Interface 3 TX Data	SOC.E9
J1.18[1]	SAI3_TX_SYNC	Serial Audio Interface 3 TX Sync	SOC.C12
J1.50	SAI3_TX_SYNC	Serial Audio Interface 3 TX Sync	SOC.B8

Table 4-4 Digital Audio Interface signals.

Note: Pins marked with * are used on SOM internal connections and can be used on the specific subsets of SOM. In other case the signals must be left floating.

Note: SAI1 Pins used in SoMs that does not require CSI.

Note: Pins marked with [1] are being latched at boot to determine boot configuration. External drivers to these pins should be disabled in time of boot otherwise they may change the boot option and the SOM will not boot. For more information please see section 5.

4.4. Enhanced Synchronous Audio Interface (ESAI)

The SOM exposes 1 Enhanced Synchronous Audio Interface with the following features:

- Independent (asynchronous mode) or shared (synchronous mode) transmit and receive sections with separate or shared internal/external clocks and frame syncs, operating in Master or Slave mode.
- Up to six transmitters and four receivers with TX2_RX3, TX3_RX2, TX4_RX1, and TX5_RX0 pins shared by transmitters 2 to 5 and receivers 0 to 3. TX0 AND TX1 pins are used by transmitters 0 and 1 only.
- Programmable data interface modes such as I2S, LSB aligned, MSB aligned
- Programmable word length (8, 12, 16, 20 or 24bits)
- Flexible selection between system clock or external oscillator as input clock source, programmable internal clock divider and frame sync generation
- AC97 support
- Time Slot Mask Registers for reduced ARM platform overhead (for both Transmit and Receive)

Note: The ESAI interface is available in iMX6ULL based SOMs only.

Pin#	Name	Description	Ball
J1.80	ESAI_TX_HF_CLK	ESAI interface TX high frequency clock	SOC.E4
J1.88	ESAI_RX_HF_CLK	ESAI interface RX high frequency clock	SOC.E3
J1.90	ESAI_RX_FS	ESAI interface RX frame sync signal	SOC.E2
J1.87	ESAI_RX_CLK	ESAI interface RX serial bit clock	SOC.E1
J2.30*	ESAI_TX_FS	Frame sync for both the transmitters and receivers in the synchronous mode (SYN=1) and for the transmitters only in asynchronous mode	SOC.D4
J2.32*	ESAI_TX_CLK	ESAI interface TX serial bit clock	SOC.D3
J2.38*	ESAI_TX5_RX0	TX5 for transmitting data from the ESAI_TX5 serial transmit shift register when programmed as a transmitter pin, RX0 signal for receiving serial data to the ESAI_RX0 serial receive shift register when programmed as a receiver pin	SOC.D2
J2.36*	ESAI_TX0	Data Transmit from the ESAI_TX0 serial transmit shift register	SOC.D1
J1.86	ESAI_TX1	Data Transmit from the ESAI_TX1 serial transmit shift register	SOC.F3
J1.76	ESAI_TX3_RX2	TX3 for transmitting data from the ESAI_TX3 serial transmit shift register when programmed as a transmitter pin, RX2 signal for receiving serial data to the ESAI_RX2 serial receive shift register when programmed as a receiver pin	SOC.F5
J1.64	ESAI_TX2_RX3	TX2 for transmitting data from the ESAI_TX2 serial transmit shift register when programmed as a transmitter pin, RX3 signal for receiving serial data to the ESAI_RX3 serial receive shift register when programmed as a receiver pin	SOC.E5
J1.89	ESAI_TX4_RX1	TX4 for transmitting data from the ESAI_TX4 serial transmit shift register when programmed as a transmitter pin, RX1 signal for receiving serial data to the ESAI_RX1 serial receive shift register when programmed as a receiver pin	SOC.F2

Table 4-5 ESAI Interface signals.

Note: ESAI Pins used can be used in SoMs that does not require CSI.

Note: Pins marked with * are used on SOM internal connections and can be used on the specific subsets of SOM. In other case the signals must be left floating.

4.5. Wi-Fi and Bluetooth Interface

The DART-6UL/DART-6UL-5G contains a certified high performance Wi-Fi and Bluetooth module.
For DART-6UL: IEEE 802.11 b/g/n + Bluetooth 2.1+EDR, and BLE 5.2
For DART-6UL-5G: IEEE 802.11 ac/a/b/g/n + Bluetooth 2.1+EDR, and BLE 5.2
The modules have an antenna connection through a U.FL JACK connector.
Antenna cable connected to module must have 50-Ω impedance.
In order to give the most flexible solution the Bluetooth UART and Bluetooth Audio bus is buffered and it can be disconnected from the module and used by external circuity.

One of the following options can be implemented:

- The system will use all the wireless interfaces: Wi-Fi, Bluetooth, and Bluetooth Audio. In this case all the external pins of the interfaces should be left floating.
- The system will use only Wi-Fi; the Bluetooth interface will not be used. In this case
  DART-6UL:
  the Bluetooth should be disabled, the Bluetooth module pins will be entering Hi-Z and the SOC pins will be accessible.
  DART-6UL-5G:
  The module can be purchased with Wi-Fi assembled and Bluetooth buffer not assembled.
- The system will not use wireless connections. In this case the module can be purchased without Wi-Fi module assembled and all the interfaces are accessible.

Pin#	Name	Description	Ball
J2.67*	SAI2_TX_SYNC	Bluetooth Frame Sync	SOC.N15
J2.71*	SAI2_RX_DATA	Bluetooth RX Data	SOC.M14
J2.69*	SAI2_TX_BCLK	Bluetooth TX Byte Clock	SOC.N16
J2.73*	SAI2_TX_DATA	Bluetooth TX Data	SOC.N14
J2.88*	UART2_CTS_B	Bluetooth UART CTS	SOC.J15
J2.90*	UART2_RTS_B	Bluetooth UART RTS	SOC.H14
J2.86*	UART2_RX	Bluetooth UART RX	SOC.J16
J2.84*	UART2_TX	Bluetooth UART TX	SOC.J17

Table 4-6 Bluetooth Interface signals

Note: Pins marked with * are used on SOM internal connections and can be used on the specific subsets of SOM. In other case the signals must be left floating.

The Wi-Fi module connected to the i.MX6 Ultralight processor via SD1 SD Card interface. The second available interface is used by the SOM for the internal boot and storage. The SD card interface SD1 is mixed and routed to the external connector and the Wi-Fi module to allow SD Card recovery and to ease the development process. This means that booting from the SD card must be done with the kernel that does not have W-Fi module definitions inside i.e. Wi-Fi interface is not accessible when booting from SD card.
The SOM can be ordered without Wi-Fi module assembled and, in this case, the SD1 interface is directly routed to the J1 connector. In this case the routing does not pass the mixer chip and the pins can be used for other interfaces.

Pin#	Name	Description	Ball
J1.83*	SD1_CLK	SD Card 1 Interface Clock Signal	
J1.82*	SD1_CMD	SD Card 1 Interface Command Signal	SOC.C2
J1.68*	SD1_DATA0	SD Card 1 Interface Data 0 Signal	SOC.B3
J1.74*	SD1_DATA1	SD Card 1 Interface Data 1 Signal	SOC.B2
J1.78*	SD1_DATA2	SD Card 1 Interface Data 2 Signal	SOC.B1
J1.66*	SD1_DATA3	SD Card 1 Interface Data 3 Signal	SOC.A2
J2.83	WLAN_FORCE_DIS	Connecting this pin to DGND will route SD1 interface to J1	SOC.C4

Table 4-7 Wi-Fi SD Card Interface signals

Note: Pins marked with * are used on SOM internal connections and can be used on the specific subsets of SOM. In other case the signals must be left floating.

Pin#	Name	Description	Ball
J2.28	OSC_32K_OUT	Reference Clock out for Wi-Fi module. It is also part of TSC controller. It may be connected to J2.85 if TSC controller is not in use	SOC.L17
J2.85	OSC_32K_IN	32khz OSC required for WiFi. Can be connected to J2.28 if TSC controller is not in use.	

Table 4-8 Additional Wi-Fi Interface signals

Additional WiFi SD1 signal in DART-6UL-5G SOMs only:

Pin#	Name	Description	Notes
J2.77	SD_VSELECT	Optional manual setting of SD1 voltage level: When High-1.8V, When low - 3.3V.	For all DART-6UL-5G SOMs **not assembled** with iMX6UL 'G3' variant: Voltage is set automatically via SW-**Pin should be connected to DGND**. For DART-6UL-5G SOMs **assembled** with iMX6UL 'G3' variant and WiFi: When routing SD1 interface to WiFi - Connect this pin to 3.3V. When routing SD1 interface to J1- Connect this pin to DGND.

Table 4-9 Additional Wi-Fi SD Card Interface signals signal in DART-6UL-5G

In SOMs assembled with iMX6UL 'G3' variant GPIO5 domain pins used to automatically toggle SD1 routing selection are not available. In such SOMs, controlling SD1 interface routing should be done manually using pins J2.77 and J2.83.
The Following tables summarize the pin settings for these SOM variants:

DART-6UL:

Pin#	Name	SD1 interface routed to J1	SD1 interface routed to WiFi
J2.83	WLAN_FORCE_DIS	Connect to DGND	Floating
J2.77	SD_VSELECT	Connect to DGND	Connect to DGND

DART-6UL-5G:

Pin#	Name	SD1 interface routed to J1	SD1 interface routed to WiFi
J2.83	WLAN_FORCE_DIS	Connect to DGND	Floating
J2.77	SD_VSELECT	Connect to DGND	Connect to 3.3V

4.6. USB ports

The USB controller block provides high performance USB functionality that conforms to the Universal Serial Bus Specification, Rev. 2.0 (Compaq, Hewlett-Packard, Intel, Lucent, Microsoft, NEC, Philips; 2000), and the On-The-Go and Embedded Host Supplement to the USB Revision 2.0 Specification (Hewlett-Packard Company, Intel Corporation, LSI Corporation, Microsoft Corporation, Renesas Electronics Corporation, ST-Ericsson; 2012). The USB controller consists of two independent USB controller cores: two On-The-Go (OTG) controller cores. Each controller core supports UTMI interface. See Features for more details. All two controller cores are single-port cores. For the OTG cores, there is only one port. The port can be used as either a downstream or an upstream port.

Pin#	Name	Description	Ball
J2.55	USB_OTG1_CHD_B	USB Host 1 Charger Detect	SOC.U16
J2.1	USB_OTG1_DN	USB Host 1 Data Negative	SOC.T15
J2.3	USB_OTG1_DP	USB Host 1 Data Positive	SOC.U15
J2.40	USB_OTG1_VBUS	USB Host 1 Vbus	SOC.T12
J2.9	USB_OTG2_DN	USB Host 2 Data Negative	SOC.T13
J2.7	USB_OTG2_DP	USB Host 2 Data Positive	SOC.U13
J2.19	USB_OTG2_VBUS	USB Host 2 Vbus	SOC.U12

Table 4-10 USB port signals

4.7. UART Interfaces

The DART-6UL/DART-6UL-5G exposes up to 8 UART interfaces that are mixed with other peripherals. Part of them is used on the SOM and can be accessible only in subset versions of the DART-6UL/DART-6UL-5G.
Universal Asynchronous Receiver/Transmitter (UART) provides serial communication capability with external devices through a level converter and an RS-232 cable or through use of external circuitry that converts infrared signals to electrical signals (for reception) or transforms electrical signals to signals that drive an infrared LED (for transmission) to provide low speed IrDA compatibility. UART supports NRZ encoding format, RS485 compatible 9 bit data format and IrDA compatible infrared slow data rate (SIR) format.

Pin#	Name	Description	Ball
J2.57	UART1_CTS	UART 1 CTS line	SOC.K15
J2.75*	UART1_CTS	UART 1 CTS line	SOC.K17
J2.51	UART1_RTS	UART 1 RTS line	SOC.J14
J2.79*	UART1_RTS	UART 1 RTS line	SOC.L16
J2.28	UART1_RX	UART 1 RX line	SOC.L17
J2.59	UART1_RX	UART 1 RX line	SOC.K16
J2.48	UART1_TX	UART 1 TX line	SOC.L14
J2.56	UART1_TX	UART 1 TX line	SOC.K14
J1.59	UART2_CTS	UART 2 CTS line	SOC.H17
J2.88*	UART2_CTS	UART 2 CTS line	SOC.J15
J1.61	UART2_RTS	UART 2 RTS line	SOC.H16
J2.90*	UART2_RTS	UART 2 RTS line	SOC.H14
J2.86*	UART2_RX	UART 2 RX line	SOC.J16
J2.84*	UART2_TX	UART 2 TX line	SOC.J17
J1.58	UART3_CTS	UART 3 CTS line	SOC.B5
J1.67	UART3_CTS	UART 3 CTS line	SOC.H15
J1.69	UART3_RTS	UART 3 RTS line	SOC.G14
J2.61*	UART3_RTS	UART 3 RTS line	SOC.A4
J1.61	UART3_RX	UART 3 RX line	SOC.H16
J1.59	UART3_TX	UART 3 TX line	SOC.H17
J2.89*	UART3_TX	UART 3 TX line	SOC.A3
J1.54	UART4_CTS	UART 4 CTS line	SOC.D9
J2.72*	UART4_CTS	UART 4 CTS line	SOC.E17
J1.52	UART4_RTS	UART 4 RTS line	SOC.C9
J2.66*	UART4_RTS	UART 4 RTS line	SOC.F16
J1.50	UART4_RX	UART 4 RX line	SOC.B8
J2.22	UART4_RX	UART 4 RX line	SOC.G16
J1.49	UART4_TX	UART 4 TX line	SOC.A8
J2.24	UART4_TX	UART 4 TX line	SOC.G17
J1.87	UART5_CTS	UART 5 CTS line	SOC.E1
J2.42	UART5_CTS	UART 5 CTS line	SOC.M15
J2.78*	UART5_CTS	UART 5 CTS line	SOC.E15
J1.90	UART5_RTS	UART 5 RTS line	SOC.E2

Pin#	Name	Description	Ball
J2.25	UART5_RTS	UART 5 RTS line	SOC.N17
J2.76*	UART5_RTS	UART 5 RTS line	SOC.E16
J1.71*	UART5_RX	UART 5 RX line	SOC.G13
J1.88	UART5_RX	UART 5 RX line	SOC.E3
J2.27	UART5_RX	UART 5 RX line	SOC.M17
J1.80	UART5_TX	UART 5 TX line	SOC.E4
J2.52	UART5_TX	UART 5 TX line	SOC.M16
J2.68*	UART5_TX	UART 5 TX line	SOC.F17
J1.86	UART6_CTS	UART 6 CTS line	SOC.F3
J2.80*	UART6_CTS	UART 6 CTS line	SOC.E14
J1.89	UART6_RTS	UART 6 RTS line	SOC.F2
J2.74*	UART6_RTS	UART 6 RTS line	SOC.F15
J1.39	UART6_RX	UART 6 RX line	SOC.C16
J1.64	UART6_RX	UART 6 RX line	SOC.E5
J1.37	UART6_TX	UART 6 TX line	SOC.C17
J1.76	UART6_TX	UART 6 TX line	SOC.F5
J1.30[1]	UART7_CTS	UART 7 CTS line	SOC.A10
J2.62*	UART7_CTS	UART 7 CTS line	SOC.F14
J1.42[1]	UART7_RTS	UART 7 RTS line	SOC.D11
J2.87*	UART7_RTS	UART 7 RTS line	SOC.D15
J1.10[1]	UART7_RX	UART 7 RX line	SOC.B13
J1.43	UART7_RX	UART 7 RX line	SOC.A15
J1.06[1]	UART7_TX	UART 7 TX line	SOC.C13
J1.31	UART7_TX	UART 7 TX line	SOC.B17
J1.26[1]	UART8_CTS	UART 8 CTS line	SOC.C10
J1.57	UART8_CTS	UART 8 CTS line	SOC.D17
J1.28[1]	UART8_RTS	UART 8 RTS line	SOC.B10
J1.55	UART8_RTS	UART 8 RTS line	SOC.D16
J1.45	UART8_RX	UART 8 RX line	SOC.B15
J1.47[1]	UART8_RX	UART 8 RX line	SOC.B14
J1.04[1]	UART8_TX	UART 8 TX line	SOC.C14
J1.35	UART8_TX	UART 8 TX line	SOC.A16

Table 4-11 UART signals

Note: Pins marked with * are used on SOM internal connections and can be used on the specific subsets of SOM. In other case the signals must be left floating.

Note: Pins marked with [1] are being latched at boot to determine boot configuration. External drivers to these pins should be disabled in time of boot otherwise they may change the boot option and the SOM will not boot. For more information please see section 5.

4.8. I2C Interface

DART-6UL/DART-6UL-5G SOM exposes 4 I2C interfaces on the external connectors. I2C is a two-wire, bidirectional serial bus that provides a simple, efficient method of data exchange, minimizing the interconnection between devices. This bus is suitable for applications requiring occasional communications over a short distance between many devices. The flexible I2C standard allows additional devices to be connected to the bus for expansion and system development.

Pin#	Name	Description	Ball
J2.48	I2C1_SCL	I2C1 Clock	SOC.L14
J2.24	I2C1_SCL	I2C1 Clock	SOC.G17
J1.64	I2C1_SCL	I2C1 Clock	SOC.E5
J2.28	I2C1_SDA	I2C1 Data	SOC.L17
J2.22	I2C1_SDA	I2C1 Data	SOC.G16
J1.76	I2C1_SDA	I2C1 Data	SOC.F5
J2.68*	I2C2_SCL	I2C2 Clock	SOC.F17
J1.71*	I2C2_SDA	I2C2 Data	SOC.G13
J2.56	I2C3_SCL	I2C3 Clock	SOC.K14
J1.37	I2C3_SCL	I2C3 Clock	SOC.C17
J1.38[1]	I2C3_SCL	I2C3 Clock	SOC.A9
J2.59	I2C3_SDA	I2C3 Data	SOC.K16
J1.39	I2C3_SDA	I2C3 Data	SOC.C16
J1.44[1]	I2C3_SDA	I2C3 Data	SOC.B9
J2.84*	I2C4_SCL	I2C4 Clock	SOC.J17
J1.31	I2C4_SCL	I2C4 Clock	SOC.B17
J1.40[1]	I2C4_SCL	I2C4 Clock	SOC.D10
J2.86*	I2C4_SDA	I2C4 Data	SOC.J16
J1.75[1]	I2C4_SDA	I2C4 Data	SOC.E10
J1.43	I2C4_SDA	I2C4 Data	SOC.A15

Table 4-12 I2C interface signals

Note: Pins marked with * are used on SOM internal connections and can be used on the specific subsets of SOM. In other case the signals must be left floating.

Note: Pins marked with [1] are being latched at boot to determine boot configuration. External drivers to these pins should be disabled in time of boot otherwise they may change the boot option and the SOM will not boot. For more information please see section 5.

Note:
I2C2 Interface exported on pins J1.71, J2.68 is used by On SOM EEPROM (address 0x50 & 0x51) and Audio Codec (address 0x1A). Function of these pins must not be altered.

Pull up resistors on SOM are present on I2C2 pins J1.71, J2.68 only.
When using other I2C interfaces, please place pull up resistors on Carrier board.

4.9. Sony/Philips Digital Interface (SPDIF)

The SOM exposes 1 SPDIF interface.

Pin#	Name	Description	Ball
J1.42[1]	SPDIF_EXT_CLK	SPDIF Interface External Clock	SOC.D11
J1.62	SPDIF_EXT_CLK	SPDIF Interface External Clock	SOC.E6
J2.59	SPDIF_IN	SPDIF Interface Input	SOC.K16
J2.42	SPDIF_IN	SPDIF Interface Input	SOC.M15
J1.20[1]	SPDIF_IN	SPDIF Interface Input	SOC.B11
J1.83*	SPDIF_IN	SPDIF Interface Input	SOC.C1
J1.30[1]	SPDIF_LOCK	SPDIF Interface Lock	SOC.A10
J2.56	SPDIF_OUT	SPDIF Interface Output	SOC.K14
J2.25	SPDIF_OUT	SPDIF Interface Output	SOC.N17
J1.28[1]	SPDIF_OUT	SPDIF Interface Output	SOC.B10
J1.82*	SPDIF_OUT	SPDIF Interface Output	SOC.C2
J2.21	SPDIF_OUT	SPDIF Interface Output	SOC.P15
J1.26[1]	SPDIF_SR_CLK	SPDIF SR Clock Signal	SOC.C10

Table 4-13 SPDIF Interface signals

Note: Pins marked with * are used on SOM internal connections and can be used on the specific subsets of SOM. In other case the signals must be left floating.

Note: Pins marked with [1] are being latched at boot to determine boot configuration. External drivers to these pins should be disabled in time of boot otherwise they may change the boot option and the SOM will not boot. For more information please see section 5.

4.10. Flexible Controller Area Network (FLEXCAN)

DART-6UL/DART-6UL-5G Exposes 2 FLEXCAN interfaces.
The Flexible Controller Area Network (FLEXCAN) module is a communication controller implementing the CAN protocol according to the CAN 2.0B protocol specification. The CAN protocol was primarily designed to be used as a vehicle serial data bus meeting the specific requirements of this field: real-time processing, reliable operation in the EMI environment of a vehicle, cost-effectiveness and required bandwidth. The FLEXCAN module is a full implementation of the CAN protocol specification, which supports both standard and extended message frames. 64 Message Buffers are supported.

Pin#	Name	Description	Ball
J1.69	CAN1_RX	CAN1 RX Input	SOC.G14
J2.72*	CAN1_RX	CAN1 RX Input	SOC.E17
J1.22[1]	CAN1_RX	CAN1 RX Input	SOC.A11
J1.74*	CAN1_RX	CAN1 RX Input	SOC.B2
J1.20[1]	CAN1_TX	CAN1 TX Output	SOC.B11
J1.67	CAN1_TX	CAN1 TX Output	SOC.H15
J2.66*	CAN1_TX	CAN1 TX Output	SOC.F16
J1.68*	CAN1_TX	CAN1 TX Output	SOC.B3
J2.90*	CAN2_RX	CAN2 RX Input	SOC.H14

Pin#	Name	Description	Ball
J2.78*	CAN2_RX	CAN2 RX Input	SOC.E15
J1.66*	CAN2_RX	CAN2 RX Input	SOC.A2
J1.73[1]	CAN2_RX	CAN2 RX Input	SOC.D12
J2.88*	CAN2_TX	CAN2 TX Output	SOC.J15
J2.76*	CAN2_TX	CAN2 TX Output	SOC.E16
J1.46[1]	CAN2_TX	CAN2 TX Output	SOC.E12
J1.78*	CAN2_TX	CAN2 TX Output	SOC.B1

Table 4-14 FLEXCAN Interface signals

Note: Pins marked with * are used on SOM internal connections and can be used on the specific subsets of SOM. In other case the signals must be left floating.

Note: Pins marked with [1] are being latched at boot to determine boot configuration. External drivers to these pins should be disabled in time of boot otherwise they may change the boot option and the SOM will not boot. For more information please see section 5.

4.11. 10/100-Mbps Ethernet MAC (ENET)

The DART-6UL/DART-6UL-5G implements a dual speed 10/100 Mbit/s Ethernet MAC compliant with the IEEE802.3-2002 standard. SoM contains on board Ethernet 10/100 PHY based on KSZ8051RNL chip. This PHY is assembled on ETH1 interface.

Pin#	Name	Description	Ball
J2.60	ENET1_1588_EVENT0_IN	ENET 1 1588 EVENT 0 IN	SOC.K13
J2.44	ENET1_1588_EVENT0_OUT	ENET 1 1588 EVENT 0 OUT	SOC.L15
J1.67	ENET1_1588_EVENT1_IN	ENET 1 1588 EVENT 1 IN	SOC.H15
J1.69	ENET1_1588_EVENT1_OUT	ENET 1 1588 EVENT 1 OUT	SOC.G14
J1.44[1]	ENET1_1588_EVENT2_IN	ENET 1 1588 EVENT 2 IN	SOC.B9
J1.38[1]	ENET1_1588_EVENT2_OUT	ENET 1 1588 EVENT 2 OUT	SOC.A9
J1.75[1]	ENET1_1588_EVENT3_IN	ENET 1 1588 EVENT 2 IN	SOC.E10
J1.40[1]	ENET1_1588_EVENT3_OUT	ENET 1 1588 EVENT 2 OUT	SOC.D10
J2.90*	ENET1_COL	ENET 1 COL	SOC.H14
J2.88*	ENET1_CRS	ENET 1 CRS	SOC.J15
J2.79*	ENET1_MDC	ENET 1 MDC	SOC.L16
J1.39	ENET1_MDC	ENET 1 MDC	SOC.C16
J2.75*	ENET1_MDIO	ENET 1 MDIO	SOC.K17
J1.37	ENET1_MDIO	ENET 1 MDIO	SOC.C17
J2.66*	ENET1_RDATA[0]	ENET 1 RDATA 0	SOC.F16
J2.72*	ENET1_RDATA[1]	ENET 1 RDATA 1	SOC.E17
J2.56	ENET1_RDATA[2]	ENET 1 RDATA 2	SOC.K14
J2.59	ENET1_RDATA[3]	ENET 1 RDATA 3	SOC.K16
J2.57	ENET1_RX_CLK	ENET 1 RX CLK	SOC.K15
J2.76*	ENET1_RX_EN	ENET 1 RX EN	SOC.E16
J2.87*	ENET1_RX_ER	ENET 1 RX ER	SOC.D15

Pin#	Name	Description	Ball
J2.78*	ENET1_TDATA[0]	ENET 1 TDATA 0	SOC.E15
J2.80*	ENET1_TDATA[1]	ENET 1 TDATA 1	SOC.E14
J2.84*	ENET1_TDATA[2]	ENET 1 TDATA 2	SOC.J17
J2.86*	ENET1_TDATA[3]	ENET 1 TDATA 3	SOC.J16
J2.62*	ENET1_TX_CLK	ENET 1 TX CLK	SOC.F14
J2.74*	ENET1_TX_EN	ENET 1 TX EN	SOC.F15
J2.51	ENET1_TX_ER	ENET 1 TX ER	SOC.J14
J2.52	ENET2_1588_EVENT0_IN	ENET 2 1588 EVENT 0 IN	SOC.M16
J2.27	ENET2_1588_EVENT0_OUT	ENET 2 1588 EVENT 0 OUT	SOC.M17
J2.57	ENET2_1588_EVENT1_IN	ENET 2 1588 EVENT 1 IN	SOC.K15
J2.51	ENET2_1588_EVENT1_OUT	ENET 2 1588 EVENT 1 OUT	SOC.J14
J1.26[1]	ENET2_1588_EVENT2_IN	ENET 2 1588 EVENT 2 IN	SOC.C10
J1.28[1]	ENET2_1588_EVENT2_OUT	ENET 2 1588 EVENT 2 OUT	SOC.B10
J1.30[1]	ENET2_1588_EVENT3_IN	ENET 2 1588 EVENT 2 IN	SOC.A10
J1.42[1]	ENET2_1588_EVENT3_OUT	ENET 2 1588 EVENT 2 OUT	SOC.D11
J1.71*	ENET2_COL	ENET 2 COL	SOC.G13
J2.68*	ENET2_CRS	ENET 2 CRS	SOC.F17
J2.79*	ENET2_MDC	ENET 2 MDC	SOC.L16
J2.74*	ENET2_MDC	ENET 2 MDC	SOC.F15
J2.75*	ENET2_MDIO	ENET 2 MDIO	SOC.K17
J2.80*	ENET2_MDIO	ENET 2 MDIO	SOC.E14
J1.37	ENET2_RDATA[0]	ENET 2 RDATA 0	SOC.C17
J1.39	ENET2_RDATA[1]	ENET 2 RDATA 1	SOC.C16
J1.59	ENET2_RDATA[2]	ENET 2 RDATA 2	SOC.H17
J1.61	ENET2_RDATA[3]	ENET 2 RDATA 3	SOC.H16
J1.67	ENET2_RX_CLK	ENET 2 RX CLK	SOC.H15
J1.31	ENET2_RX_EN	ENET 2 RX EN	SOC.B17
J1.55	ENET2_RX_ER	ENET 2 RX ER	SOC.D16
J1.43	ENET2_TDATA[0]	ENET 2 TDATA 0	SOC.A15
J1.35	ENET2_TDATA[1]	ENET 2 TDATA 1	SOC.A16
J2.24	ENET2_TDATA[2]	ENET 2 TDATA 2	SOC.G17
J2.22	ENET2_TDATA[3]	ENET 2 TDATA 3	SOC.G16
J1.57	ENET2_TX_CLK	ENET 2 TX CLK	SOC.D17
J1.45	ENET2_TX_EN	ENET 2 TX EN	SOC.B15
J1.69	ENET2_TX_ER	ENET 2 TX ER	SOC.G14

Table 4-15 Ethernet Interface signals

Note: Pins marked with * are used on SOM internal connections and can be used on the specific subsets of SOM. In other case the signals must be left floating.

Note: Pins marked with [1] are being latched at boot to determine boot configuration. External drivers to these pins should be disabled in time of boot otherwise they may change the boot option and the SOM will not boot. For more information please see section 5.

4.12. Enhanced Configurable SPI (ECSPI)

The Enhanced Configurable Serial Peripheral Interface (ECSPI) is a full-duplex, Synchronous, four-wire serial communication block.
The ECSPI contains a 64 x 32 receive buffer (RXFIFO) and a 64 x 32 transmit buffer (TXFIFO). With data FIFOs, the ECSPI allows rapid data communication with fewer software interrupts.

Pin#	Name	Description	Ball
J1.33[1]	ECSPI1_MISO	ECSPI 1 Master In Slave Out	SOC.B16
J2.36*	ECSPI1_MISO	ECSPI 1 Master In Slave Out	SOC.D1
J1.02[1]	ECSPI1_MOSI	ECSPI 1 Master Out Slave In	SOC.A14
J2.38*	ECSPI1_MOSI	ECSPI 1 Master Out Slave In	SOC.D2
J1.18[1]	ECSPI1_RDY	ECSPI 1 Ready	SOC.C12
J1.04[1]	ECSPI1_SCLK	ECSPI 1 Clock	SOC.C14
J2.30*	ECSPI1_SCLK	ECSPI 1 Clock	SOC.D4
J1.47[1]	ECSPI1_SS0	ECSPI 1 Chip Select 0	SOC.B14
J2.32*	ECSPI1_SS0	ECSPI 1 Chip Select 0	SOC.D3
J1.28[1]	ECSPI1_SS1	ECSPI 1 Chip Select 1	SOC.B10
J1.30[1]	ECSPI1_SS2	ECSPI 1 Chip Select 2	SOC.A10
J1.42[1]	ECSPI1_SS3	ECSPI 1 Chip Select 3	SOC.D11
J2.79*	ECSPI1_TESTER_TRIGGER	ECSPI 1 Tester Trigger	SOC.L16
J1.71*	ECSPI2_MISO	ECSPI 2 Master In Slave Out	SOC.G13
J1.87	ECSPI2_MISO	ECSPI 2 Master In Slave Out	SOC.E1
J2.68*	ECSPI2_MOSI	ECSPI 2 Master Out Slave In	SOC.F17
J1.90	ECSPI2_MOSI	ECSPI 2 Master Out Slave In	SOC.E2
J1.50	ECSPI2_RDY	ECSPI 2 Ready	SOC.B8
J2.24	ECSPI2_SCLK	ECSPI 2 Clock	SOC.G17
J1.80	ECSPI2_SCLK	ECSPI 2 Clock	SOC.E4
J2.22	ECSPI2_SS0	ECSPI 2 Chip Select 0	SOC.G16
J1.88	ECSPI2_SS0	ECSPI 2 Chip Select 0	SOC.E3
J1.54	ECSPI2_SS1	ECSPI 2 Chip Select 1	SOC.D9
J1.52	ECSPI2_SS2	ECSPI 2 Chip Select 2	SOC.C9
J1.56	ECSPI2_SS3	ECSPI 2 Chip Select 3	SOC.E9
J2.25	ECSPI2_TESTER_TRIGGER	ECSPI 2 Tester Trigger	SOC.N17
J2.90*	ECSPI3_MISO	ECSPI 3 Master In Slave Out	SOC.H14
J2.61*	ECSPI3_MISO	ECSPI 3 Master In Slave Out	SOC.A4
J2.88*	ECSPI3_MOSI	ECSPI 3 Master Out Slave In	SOC.J15
J1.58	ECSPI3_MOSI	ECSPI 3 Master Out Slave In	SOC.B5
J2.63*	ECSPI3_RDY	ECSPI 3 Ready	SOC.D5
J2.86*	ECSPI3_SCLK	ECSPI 3 Clock	SOC.J16
J2.84*	ECSPI3_SS0	ECSPI 3 Chip Select 0	SOC.J17
J2.89*	ECSPI3_SS0	ECSPI 3 Chip Select 0	SOC.A3
J2.42	ECSPI3_TESTER_TRIGGER	ECSPI 3 Tester Trigger	SOC.M15

Pin#	Name	Description	Ball
J1.35	ECSPI4_SCLK	ECSPI 4 Clock	SOC.A16
J1.57	ECSPI4_MISO	ECSPI 4 Master In Slave Out	SOC.D17
J1.45	ECSPI4_MOSI	ECSPI 4 Master Out Slave In	SOC.B15
J1.55	ECSPI4_SS0	ECSPI 4 Chip Select 0	SOC.D16
J2.56	ECSPI4_TESTER_TRIGGER	ECSPI 4 Tester Trigger	SOC.K14

Table 4-16 ECSPI Interface signals

Note: Pins marked with * are used on SOM internal connections and can be used on the specific subsets of SOM. In other case the signals must be left floating.

Note: Pins marked with [1] are being latched at boot to determine boot configuration. External drivers to these pins should be disabled in time of boot otherwise they may change the boot option and the SOM will not boot. For more information please see section 5.

4.13. Pulse Width Modulation (PWM)

The Pulse Width Modulation (PWM) has a 16-bit counter, and is optimized to generate sound from stored sample audio images and it can also generate tones. It uses 16-bit resolution and a 4 x 16 data FIFO.

Pin#	Name	Description	Ball
J2.25	PWM1_OUT	PWM 1 Output	SOC.N17
J1.44[1]	PWM1_OUT	PWM 1 Output	SOC.B9
J2.66*	PWM1_OUT	PWM 1 Output	SOC.F16
J2.42	PWM2_OUT	PWM 2 Output	SOC.M15
J1.38[1]	PWM2_OUT	PWM 2 Output	SOC.A9
J2.72*	PWM2_OUT	PWM 2 Output	SOC.E17
J2.52	PWM3_OUT	PWM 3 Output	SOC.M16
J1.75[1]	PWM3_OUT	PWM 3 Output	SOC.E10
J2.63*	PWM4_OUT	PWM 4 Output	SOC.D5
J2.27	PWM4_OUT	PWM 4 Output	SOC.M17
J1.40[1]	PWM4_OUT	PWM 4 Output	SOC.D10
J2.80*	PWM5_OUT	PWM 5 Output	SOC.E14
J1.62	PWM5_OUT	PWM 5 Output	SOC.E6
J1.08[1]	PWM5_OUT	PWM 5 Output	SOC.A13
J2.74*	PWM6_OUT	PWM 6 Output	SOC.F15
J1.32[1]	PWM6_OUT	PWM 6 Output	SOC.D14
J2.69*	PWM6_OUT	PWM 6 Output	SOC.N16
J2.62*	PWM7_OUT	PWM 7 Output	SOC.F14
J1.89	PWM7_OUT	PWM 7 Output	SOC.F2
J2.71*	PWM7_OUT	PWM 7 Output	SOC.M14
J2.87*	PWM8_OUT	PWM 8 Output	SOC.D15
J1.86	PWM8_OUT	PWM 8 Output	SOC.F3
J2.73*	PWM8_OUT	PWM 8 Output	SOC.N14

Table 4-17 PWM Interface signals

Note: Pins marked with * are used on SOM internal connections and can be used on the specific subsets of SOM. In other case the signals must be left floating.

Note: Pins marked with [1] are being latched at boot to determine boot configuration. External drivers to these pins should be disabled in time of boot otherwise they may change the boot option and the SOM will not boot. For more information please see section 5.

4.14. CMOS Sensor Interface (CSI)

The CSI enables the chip to connect directly to external CMOS image sensors. CMOS image sensors are separated into two classes, dumb and smart. Dumb sensors are those that support only traditional sensor timing (Vertical SYNC and Horizontal SYNC) and output only Bayer and statistics data, while smart sensors support CCIR656 video decoder formats and perform additional processing of the image (for example, image compression, image pre-filtering, and various data output formats). The capabilities of the CSI include:

- Configurable interface logic to support most commonly available CMOS sensors.
- Support for CCIR656 video interface as well as traditional sensor interface.
- 8-bit / 24-bit data port for YCbCr, YUV, or RGB data input.
- 8-bit / 10-bit / 16-bit data port for Bayer data input.
- Full control of 8-bit/pixel, 10-bit/pixel or 16-bit / pixel data format to 32-bitreceive FIFO packing.
- 256 x 32 FIFO to store received image pixel data.
- Embedded DMA controllers to transfer data from receive FIFO or statistic FIFO through AHB bus.
- Support 2D DMA transfer from the receive FIFO to the frame buffers in the external memory.
- Support double buffering two frames in the external memory.
- Single interrupt source to interrupt controller from mask able interrupt sources: Start of Frame, End of Frame, Change of Field, FIFO full, FIFO overrun, DMA transfer done, CCIR error and AHB bus response error.
- Configurable master clock frequency output to sensor.

Pin#	Name	Description	Ball
J1.10[1]	CSI_DATA[0]	Sensor Data Bit 0	SOC.B13
J1.61	CSI_DATA[0]	Sensor Data Bit 0	SOC.H16
J1.06[1]	CSI_DATA[1]	Sensor Data Bit 1	SOC.C13
J1.59	CSI_DATA[1]	Sensor Data Bit 1	SOC.H17
J1.08[1]	CSI_DATA[10]	Sensor Data Bit 10	SOC.A13
J1.67	CSI_DATA[10]	Sensor Data Bit 10	SOC.H15
J1.32[1]	CSI_DATA[11]	Sensor Data Bit 11	SOC.D14
J1.69	CSI_DATA[11]	Sensor Data Bit 11	SOC.G14
J1.04[1]	CSI_DATA[12]	Sensor Data Bit 12	SOC.C14
J2.24	CSI_DATA[12]	Sensor Data Bit 12	SOC.G17
J1.47[1]	CSI_DATA[13]	Sensor Data Bit 13	SOC.B14
J2.22	CSI_DATA[13]	Sensor Data Bit 13	SOC.G16

Pin#	Name	Description	Ball
J1.02[1]	CSI_DATA[14]	Sensor Data Bit 14	SOC.A14
J2.68*	CSI_DATA[14]	Sensor Data Bit 14	SOC.F17
J1.33[1]	CSI_DATA[15]	Sensor Data Bit 15	SOC.B16
J1.71*	CSI_DATA[15]	Sensor Data Bit 15	SOC.G13
J1.20[1]	CSI_DATA[16]	Sensor Data Bit 16	SOC.B11
J2.66*	CSI_DATA[16]	Sensor Data Bit 16	SOC.F16
J1.22[1]	CSI_DATA[17]	Sensor Data Bit 17	SOC.A11
J2.72*	CSI_DATA[17]	Sensor Data Bit 17	SOC.E17
J1.46[1]	CSI_DATA[18]	Sensor Data Bit 18	SOC.E12
J2.76*	CSI_DATA[18]	Sensor Data Bit 18	SOC.E16
J1.73[1]	CSI_DATA[19]	Sensor Data Bit 19	SOC.D12
J2.78*	CSI_DATA[19]	Sensor Data Bit 19	SOC.E15
J1.80	CSI_DATA[2]	Sensor Data Bit 2	SOC.E4
J2.56	CSI_DATA[2]	Sensor Data Bit 2	SOC.K14
J1.18[1]	CSI_DATA[20]	Sensor Data Bit 20	SOC.C12
J2.80*	CSI_DATA[20]	Sensor Data Bit 20	SOC.E14
J1.14[1]	CSI_DATA[21]	Sensor Data Bit 21	SOC.B12
J2.74*	CSI_DATA[21]	Sensor Data Bit 21	SOC.F15
J1.16[1]	CSI_DATA[22]	Sensor Data Bit 22	SOC.A12
J2.62*	CSI_DATA[22]	Sensor Data Bit 22	SOC.F14
J1.34[1]	CSI_DATA[23]	Sensor Data Bit 23	SOC.D13
J2.87*	CSI_DATA[23]	Sensor Data Bit 23	SOC.D15
J1.88	CSI_DATA[3]	Sensor Data Bit 3	SOC.E3
J2.59	CSI_DATA[3]	Sensor Data Bit 3	SOC.K16
J1.90	CSI_DATA[4]	Sensor Data Bit 4	SOC.E2
J2.57	CSI_DATA[4]	Sensor Data Bit 4	SOC.K15
J1.87	CSI_DATA[5]	Sensor Data Bit 5	SOC.E1
J2.51	CSI_DATA[5]	Sensor Data Bit 5	SOC.J14
J2.30*	CSI_DATA[6]	Sensor Data Bit 6	SOC.D4
J2.84*	CSI_DATA[6]	Sensor Data Bit 6	SOC.J17
J2.32*	CSI_DATA[7]	Sensor Data Bit 7	SOC.D3
J2.86*	CSI_DATA[7]	Sensor Data Bit 7	SOC.J16
J2.38*	CSI_DATA[8]	Sensor Data Bit 8	SOC.D2
J2.88*	CSI_DATA[8]	Sensor Data Bit 8	SOC.J15
J2.36*	CSI_DATA[9]	Sensor Data Bit 9	SOC.D1
J2.90*	CSI_DATA[9]	Sensor Data Bit 9	SOC.H14
J1.62	CSI_FIELD	Sensor Field Signal	SOC.E6
J2.27	CSI_FIELD	Sensor Field Signal	SOC.M17
J1.86	CSI_HSYNC	Sensor Horizontal Synchronization Signal	SOC.F3
J2.42	CSI_HSYNC	Sensor Horizontal Synchronization Signal	SOC.M15
J1.76	CSI_MCLK	Sensor Master Clock Signal	SOC.F5
J2.75*	CSI_MCLK	Sensor Master Clock Signal	SOC.K17
J1.64	CSI_PIXCLK	Sensor Pixel Clock Signal	SOC.E5
J2.79*	CSI_PIXCLK	Sensor Pixel Clock Signal	SOC.L16

Pin#	Name	Description	Ball
J1.89	CSI_VSYNC	Sensor Vertical Synchronization Signal	SOC.F2
J2.25	CSI_VSYNC	Sensor Vertical Synchronization Signal	SOC.N17

Table 4-18 CMOS Sensor Interface (CSI) signals

Note: Please see iMX6UL chip Reference Manual for better understanding of the signals. 8bit sensors connect to DATA[2..9], 10bit sensors connect to DATA[0..9], 16 bit sensors connect to DATA[0..16]

Note: Pins marked with * are used on SOM internal connections and can be used on the specific subsets of SOM. In other case the signals must be left floating.

Note: Pins marked with [1] are being latched at boot to determine boot configuration. External drivers to these pins should be disabled in time of boot otherwise they may change the boot option and the SOM will not boot. For more information please see section 5.

4.15. Analog to Digital Converter (ADC)

The analog-to-digital converter (ADC) is a successive approximation ADC designed for operation within an integrated microcontroller system-on-chip.
The features of the ADC-Digital are as follows:

- Configuration registers
- 32-bit, word aligned, byte enabled registers. (Byte and Half word access is not supported)
- Linear successive approximation algorithm with up to 12-bit resolution with 10/11 bit accuracy.
- Up to 10 ENOB (dedicated Single Ended Channels)
- Up to 1MS/s sampling rate
- Up to 16 single-ended external analog inputs
- Single or continuous conversion (automatic return to idle after single conversion)
- Output Modes: (in right-justified unsigned format)
    - 12-bit
    - 10-bit
    - 8-bit
- Configurable sample time and conversion speed/power
- Conversion complete and hardware average complete flag and interrupt
- Configurable sample time and conversion speed/power
- Conversion complete and hardware average complete flag and interrupt
- Input clock selectable from up to four sources
- Asynchronous clock source for lower noise operation with option to output the clock
- Selectable asynchronous hardware conversion trigger with hardware channel select
- Selectable voltage reference, Internal, External, or Alternate
- Automatic compare with interrupt for less-than, greater-than or equal-to, within range, or out-of-range, programmable value
- Operation in low power modes for lower noise operation
- Hardware average function
- Self-calibration mode

Pin#	Name	Description	Ball
J2.60	ADC1_IN0	Analog to Digital Converter 1 channel 0	SOC.K13
J2.44	ADC1_IN1	Analog to Digital Converter 1 channel 1	SOC.L15
J2.48	ADC1_IN2	Analog to Digital Converter 1 channel 2	SOC.L14
J2.28	ADC1_IN3	Analog to Digital Converter 1 channel 3	SOC.L17
J2.52	ADC1_IN4	Analog to Digital Converter 1 channel 4	SOC.M16
J2.27	ADC1_IN5	Analog to Digital Converter 1 channel 5	SOC.M17
J2.75*	ADC1_IN6	Analog to Digital Converter 1 channel 6	SOC.K17
J2.79*	ADC1_IN7	Analog to Digital Converter 1 channel 7	SOC.L16
J2.25	ADC1_IN8	Analog to Digital Converter 1 channel 8	SOC.N17
J2.42	ADC1_IN9	Analog to Digital Converter 1 channel 9	SOC.M15
J2.60	ADC2_IN0	Analog to Digital Converter 2 channel 0	SOC.K13
J2.44	ADC2_IN1	Analog to Digital Converter 2 channel 1	SOC.L15
J2.48	ADC2_IN2	Analog to Digital Converter 2 channel 2	SOC.L14
J2.28	ADC2_IN3	Analog to Digital Converter 2 channel 3	SOC.L17
J2.52	ADC2_IN4	Analog to Digital Converter 2 channel 4	SOC.M16
J2.27	ADC2_IN5	Analog to Digital Converter 2 channel 5	SOC.M17
J2.75*	ADC2_IN6	Analog to Digital Converter 2 channel 6	SOC.K17
J2.79*	ADC2_IN7	Analog to Digital Converter 2 channel 7	SOC.L16
J2.25	ADC2_IN8	Analog to Digital Converter 2 channel 8	SOC.N17
J2.42	ADC2_IN9	Analog to Digital Converter 2 channel 9	SOC.M15

Table 4-19 Analog To Digital Converter signals

4.16. Touch Screen Controller (TSC)

TSC is responsible for providing control of ADC and touch screen analogue block to form a touch screen system, which achieves function of touch detection and touch location detection. The controller utilizes ADC hardware trigger function and control switches in touch screen analogue block. The controller only supports 4-wire of 5-wire screen touch modes.

Pin#	Name	Description	Ball
J2.60	WIPER	Wiper Touch Controller Input	SOC.K13
J2.44	YNLR	YNLR Touch Controller Input	SOC.L15
J2.48	YPLL	YPLL Touch Controller Input	SOC.L14
J2.28	XNUR	XNUR Touch Controller Input	SOC.L17
J2.52	XPUL	XPUL Touch Controller Input	SOC.M16

Table 4-20 Touch Screen Controller signals

4.17. General Purpose Input/Output (GPIO)

The GPIO general-purpose input/output peripheral provides dedicated general-purpose pins that can be configured as either inputs or outputs.
When configured as an output, it is possible to write to an internal register to control the state driven on the output pin. When configured as an input, it is possible to detect the state of the input by reading the state of an internal register. In addition, the GPIO peripheral can produce CORE interrupts.

Pin#	Name	Description	Ball
J2.60	GPIO1_IO[0]	General Purpose Input Output Pin Bank 1 bit 0	SOC.K13
J2.44	GPIO1_IO[1]	General Purpose Input Output Pin Bank 1 bit 1	SOC.L15
J2.21	GPIO1_IO[10]	General Purpose Input Output Pin Bank 1 bit 10	SOC.P15
J2.54*	GPIO1_IO[11]	General Purpose Input Output Pin Bank 1 bit 11	SOC.P14
J2.67*	GPIO1_IO[12]	General Purpose Input Output Pin Bank 1 bit 12	SOC.N15
J2.69*	GPIO1_IO[13]	General Purpose Input Output Pin Bank 1 bit 13	SOC.N16
J2.71*	GPIO1_IO[14]	General Purpose Input Output Pin Bank 1 bit 14	SOC.M14
J2.73*	GPIO1_IO[15]	General Purpose Input Output Pin Bank 1 bit 15	SOC.N14
J2.56	GPIO1_IO[16]	General Purpose Input Output Pin Bank 1 bit 16	SOC.K14
J2.59	GPIO1_IO[17]	General Purpose Input Output Pin Bank 1 bit 17	SOC.K16
J2.57	GPIO1_IO[18]	General Purpose Input Output Pin Bank 1 bit 18	SOC.K15
J2.51	GPIO1_IO[19]	General Purpose Input Output Pin Bank 1 bit 19	SOC.J14
J2.48	GPIO1_IO[2]	General Purpose Input Output Pin Bank 1 bit 2	SOC.L14
J2.84*	GPIO1_IO[20]	General Purpose Input Output Pin Bank 1 bit 20	SOC.J17
J2.86*	GPIO1_IO[21]	General Purpose Input Output Pin Bank 1 bit 21	SOC.J16
J2.88*	GPIO1_IO[22]	General Purpose Input Output Pin Bank 1 bit 22	SOC.J15
J2.90*	GPIO1_IO[23]	General Purpose Input Output Pin Bank 1 bit 23	SOC.H14
J1.59	GPIO1_IO[24]	General Purpose Input Output Pin Bank 1 bit 24	SOC.H17
J1.61	GPIO1_IO[25]	General Purpose Input Output Pin Bank 1 bit 25	SOC.H16
J1.67	GPIO1_IO[26]	General Purpose Input Output Pin Bank 1 bit 26	SOC.H15
J1.69	GPIO1_IO[27]	General Purpose Input Output Pin Bank 1 bit 27	SOC.G14
J2.24	GPIO1_IO[28]	General Purpose Input Output Pin Bank 1 bit 28	SOC.G17
J2.22	GPIO1_IO[29]	General Purpose Input Output Pin Bank 1 bit 29	SOC.G16
J2.28	GPIO1_IO[3]	General Purpose Input Output Pin Bank 1 bit 3	SOC.L17
J2.68*	GPIO1_IO[30]	General Purpose Input Output Pin Bank 1 bit 30	SOC.F17
J1.71*	GPIO1_IO[31]	General Purpose Input Output Pin Bank 1 bit 31	SOC.G13
J2.52	GPIO1_IO[4]	General Purpose Input Output Pin Bank 1 bit 4	SOC.M16
J2.27	GPIO1_IO[5]	General Purpose Input Output Pin Bank 1 bit 5	SOC.M17
J2.75*	GPIO1_IO[6]	General Purpose Input Output Pin Bank 1 bit 6	SOC.K17
J2.79*	GPIO1_IO[7]	General Purpose Input Output Pin Bank 1 bit 7	SOC.L16
J2.25	GPIO1_IO[8]	General Purpose Input Output Pin Bank 1 bit 8	SOC.N17
J2.42	GPIO1_IO[9]	General Purpose Input Output Pin Bank 1 bit 9	SOC.M15
J2.66*	GPIO2_IO[0]	General Purpose Input Output Pin Bank 2 bit 0	SOC.F16
J2.72*	GPIO2_IO[1]	General Purpose Input Output Pin Bank 2 bit 1	SOC.E17

Pin#	Name	Description	Ball
J1.31	GPIO2_IO[10]	General Purpose Input Output Pin Bank 2 bit 10	SOC.B17
J1.43	GPIO2_IO[11]	General Purpose Input Output Pin Bank 2 bit 11	SOC.A15
J1.35	GPIO2_IO[12]	General Purpose Input Output Pin Bank 2 bit 12	SOC.A16
J1.45	GPIO2_IO[13]	General Purpose Input Output Pin Bank 2 bit 13	SOC.B15
J1.57	GPIO2_IO[14]	General Purpose Input Output Pin Bank 2 bit 14	SOC.D17
J1.55	GPIO2_IO[15]	General Purpose Input Output Pin Bank 2 bit 15	SOC.D16
J1.82*	GPIO2_IO[16]	General Purpose Input Output Pin Bank 2 bit 16	SOC.C2
J1.83*	GPIO2_IO[17]	General Purpose Input Output Pin Bank 2 bit 17	SOC.C1
J1.68*	GPIO2_IO[18]	General Purpose Input Output Pin Bank 2 bit 18	SOC.B3
J1.74*	GPIO2_IO[19]	General Purpose Input Output Pin Bank 2 bit 19	SOC.B2
J2.76*	GPIO2_IO[2]	General Purpose Input Output Pin Bank 2 bit 2	SOC.E16
J1.78*	GPIO2_IO[20]	General Purpose Input Output Pin Bank 2 bit 20	SOC.B1
J1.66*	GPIO2_IO[21]	General Purpose Input Output Pin Bank 2 bit 21	SOC.A2
J2.78*	GPIO2_IO[3]	General Purpose Input Output Pin Bank 2 bit 3	SOC.E15
J2.80*	GPIO2_IO[4]	General Purpose Input Output Pin Bank 2 bit 4	SOC.E14
J2.74*	GPIO2_IO[5]	General Purpose Input Output Pin Bank 2 bit 5	SOC.F15
J2.62*	GPIO2_IO[6]	General Purpose Input Output Pin Bank 2 bit 6	SOC.F14
J2.87*	GPIO2_IO[7]	General Purpose Input Output Pin Bank 2 bit 7	SOC.D15
J1.37	GPIO2_IO[8]	General Purpose Input Output Pin Bank 2 bit 8	SOC.C17
J1.39	GPIO2_IO[9]	General Purpose Input Output Pin Bank 2 bit 9	SOC.C16
J1.49	GPIO3_IO[0]	General Purpose Input Output Pin Bank 3 bit 0	SOC.A8
J1.50	GPIO3_IO[1]	General Purpose Input Output Pin Bank 3 bit 1	SOC.B8
J1.28[1]	GPIO3_IO[10]	General Purpose Input Output Pin Bank 3 bit 10	SOC.B10
J1.30[1]	GPIO3_IO[11]	General Purpose Input Output Pin Bank 3 bit 11	SOC.A10
J1.42[1]	GPIO3_IO[12]	General Purpose Input Output Pin Bank 3 bit 12	SOC.D11
J1.20	GPIO3_IO[13]	General Purpose Input Output Pin Bank 3 bit 13	SOC.B11
J1.22[1]	GPIO3_IO[14]	General Purpose Input Output Pin Bank 3 bit 14	SOC.A11
J1.46[1]	GPIO3_IO[15]	General Purpose Input Output Pin Bank 3 bit 15	SOC.E12
J1.73[1]	GPIO3_IO[16]	General Purpose Input Output Pin Bank 3 bit 16	SOC.D12
J1.18[1]	GPIO3_IO[17]	General Purpose Input Output Pin Bank 3 bit 17	SOC.C12
J1.14[1]	GPIO3_IO[18]	General Purpose Input Output Pin Bank 3 bit 18	SOC.B12
J1.16[1]	GPIO3_IO[19]	General Purpose Input Output Pin Bank 3 bit 19	SOC.A12
J1.54	GPIO3_IO[2]	General Purpose Input Output Pin Bank 3 bit 2	SOC.D9
J1.34[1]	GPIO3_IO[20]	General Purpose Input Output Pin Bank 3 bit 20	SOC.D13
J1.06[1]	GPIO3_IO[21]	General Purpose Input Output Pin Bank 3 bit 21	SOC.C13
J1.10[1]	GPIO3_IO[22]	General Purpose Input Output Pin Bank 3 bit 22	SOC.B13
J1.08[1]	GPIO3_IO[23]	General Purpose Input Output Pin Bank 3 bit 23	SOC.A13
J1.32[1]	GPIO3_IO[24]	General Purpose Input Output Pin Bank 3 bit 24	SOC.D14
J1.04[1]	GPIO3_IO[25]	General Purpose Input Output Pin Bank 3 bit 25	SOC.C14
J1.47[1]	GPIO3_IO[26]	General Purpose Input Output Pin Bank 3 bit 26	SOC.B14
J1.02[1]	GPIO3_IO[27]	General Purpose Input Output Pin Bank 3 bit 27	SOC.A14
J1.33[1]	GPIO3_IO[28]	General Purpose Input Output Pin Bank 3 bit 28	SOC.B16

Pin#	Name	Description	Ball
J1.52	GPIO3_IO[3]	General Purpose Input Output Pin Bank 3 bit 3	SOC.C9
J1.56	GPIO3_IO[4]	General Purpose Input Output Pin Bank 3 bit 4	SOC.E9
J1.44[1]	GPIO3_IO[5]	General Purpose Input Output Pin Bank 3 bit 5	SOC.B9
J1.38[1]	GPIO3_IO[6]	General Purpose Input Output Pin Bank 3 bit 6	SOC.A9
J1.75[1]	GPIO3_IO[7]	General Purpose Input Output Pin Bank 3 bit 7	SOC.E10
J1.40[1]	GPIO3_IO[8]	General Purpose Input Output Pin Bank 3 bit 8	SOC.D10
J1.26[1]	GPIO3_IO[9]	General Purpose Input Output Pin Bank 3 bit 9	SOC.C10
J2.63*	GPIO4_IO[11]	General Purpose Input Output Pin Bank 4 bit 11	SOC.D5
J2.89*	GPIO4_IO[12]	General Purpose Input Output Pin Bank 4 bit 12	SOC.A3
J1.58	GPIO4_IO[14]	General Purpose Input Output Pin Bank 4 bit 14	SOC.B5
J2.61*	GPIO4_IO[15]	General Purpose Input Output Pin Bank 4 bit 15	SOC.A4
J1.62	GPIO4_IO[16]	General Purpose Input Output Pin Bank 4 bit 16	SOC.E6
J1.76	GPIO4_IO[17]	General Purpose Input Output Pin Bank 4 bit 17	SOC.F5
J1.64	GPIO4_IO[18]	General Purpose Input Output Pin Bank 4 bit 18	SOC.E5
J1.89	GPIO4_IO[19]	General Purpose Input Output Pin Bank 4 bit 19	SOC.F2
J1.86	GPIO4_IO[20]	General Purpose Input Output Pin Bank 4 bit 20	SOC.F3
J1.80	GPIO4_IO[21]	General Purpose Input Output Pin Bank 4 bit 21	SOC.E4
J1.88	GPIO4_IO[22]	General Purpose Input Output Pin Bank 4 bit 22	SOC.E3
J1.90	GPIO4_IO[23]	General Purpose Input Output Pin Bank 4 bit 23	SOC.E2
J1.87	GPIO4_IO[24]	General Purpose Input Output Pin Bank 4 bit 24	SOC.E1
J2.30*	GPIO4_IO[25]	General Purpose Input Output Pin Bank 4 bit 25	SOC.D4
J2.32*	GPIO4_IO[26]	General Purpose Input Output Pin Bank 4 bit 26	SOC.D3
J2.38*	GPIO4_IO[27]	General Purpose Input Output Pin Bank 4 bit 27	SOC.D2
J2.36*	GPIO4_IO[28]	General Purpose Input Output Pin Bank 4 bit 28	SOC.D1
J2.64	GPIO5_IO[1]	General Purpose Input Output Pin Bank 5 bit 1	SOC.R9
J2.33[1]	GPIO5_IO[10]	General Purpose Input Output Pin Bank 5 bit 10	SOC.T10
J2.31[1]	GPIO5_IO[11]	General Purpose Input Output Pin Bank 5 bit 11	SOC.U10
J1.63	GPIO5_IO[3]	General Purpose Input Output Pin Bank 5 bit 3	SOC.P10
J1.51*	GPIO5_IO[5]	General Purpose Input Output Pin Bank 5 bit 5	SOC.N8
J2.37	GPIO5_IO[7]	General Purpose Input Output Pin Bank 5 bit 7	SOC.N10
J2.39	GPIO5_IO[8]	General Purpose Input Output Pin Bank 5 bit 8	SOC.N9
J2.49	GPIO5_IO[9]	General Purpose Input Output Pin Bank 5 bit 9	SOC.R6

Table 4-21 General Purpose Input/Output signals

Note: Pins marked with * are used on SOM internal connections and can be used on the specific subsets of SOM. In other case the signals must be left floating.

Note: Pins marked with [1] are being latched at boot to determine boot configuration. External drivers to these pins should be disabled in time of boot otherwise they may change the boot option and the SOM will not boot. For more information please see section 5.

4.18. Power

The DART-6UL/DART-6UL-5G gets its power from external 3.3VDC 2A power supply.

Pin#	Name	Description
J1.13	VCC_3V3_IN	3.3V Main power supply input
J1.15	VCC_3V3_IN	3.3V Main power supply input
J1.17	VCC_3V3_IN	3.3V Main power supply input
J1.19	VCC_3V3_IN	3.3V Main power supply input
J1.21	VCC_3V3_IN	3.3V Main power supply input
J1.23	VCC_3V3_IN	3.3V Main power supply input
J1.25	VCC_3V3_IN	3.3V Main power supply input
J1.27	VCC_3V3_IN	3.3V Main power supply input
J2.10	AGND	Audio Interface Ground Reference
J2.18	AGND	Audio Interface Ground Reference
J2.14	AGND	Audio Interface Ground Reference
J1.12	DGND	Digital Ground
J1.24	DGND	Digital Ground
J1.29	DGND	Digital Ground
J1.36	DGND	Digital Ground
J1.41	DGND	Digital Ground
J1.48	DGND	Digital Ground
J1.53	DGND	Digital Ground
J1.60	DGND	Digital Ground
J1.65	DGND	Digital Ground
J1.72	DGND	Digital Ground
J1.77	DGND	Digital Ground
J1.79	DGND	Digital Ground
J1.81	DGND	Digital Ground
J1.84	DGND	Digital Ground
J1.85	DGND	Digital Ground
J2.5	DGND	Digital Ground
J2.11	DGND	Digital Ground
J2.17	DGND	Digital Ground
J2.20	DGND	Digital Ground
J2.26	DGND	Digital Ground
J2.29	DGND	Digital Ground
J2.34	DGND	Digital Ground
J2.41	DGND	Digital Ground
J2.46	DGND	Digital Ground
J2.50	DGND	Digital Ground
J2.53	DGND	Digital Ground
J2.58	DGND	Digital Ground

J2.65	DGND	Digital Ground
J2.70	DGND	Digital Ground
J2.77	DART-6UL: DGND	Digital Ground
	DART-6UL-5G: SD_VSELECT	For all DART-6UL-5G SOMs **not assembled** with iMX6UL 'G3' variant: Voltage is set automatically via SW- **Pin should be connected to DGND**. For DART-6UL-5G SOMs **assembled** with iMX6UL 'G3' variant and WiFi: When routing SD1 interface to WiFi -Connect this pin to 3.3V. When routing SD1 interface to J1- Connect this pin to DGND.
J2.81	DGND	Digital Ground
J2.82	DGND	Digital Ground
J1.70	DGND	Digital Ground

Table 4-22 Power pins

5. BOOT configuration

DART-6UL/DART-6UL-5G can be programmed to boot from the following sources:

- On board NAND Flash memory (if available)
- On board eMMC Flash memory (if available)
- External SD Card (using Wi-Fi SDHC Interface)

The selection of the boot mode is done via strap options resistors on LCD_DATA lines. In addition, Boot mode pins should be set to Internal Boot, BOOT_MODE[1:0]= 10. Attention should be paid using these boot strap pins as inputs to the SOM. External drivers should be disabled in time of Reset otherwise they may change the boot option and the SOM will not boot.

Pin#	Name	Description	NAND	eMMC	SD Card
J1.44	LCD_DATA[0]	Boot Configuration Byte 1 Bit 0	0	0	0
J1.38	LCD_DATA[1]	Boot Configuration Byte 1 Bit 1	0	0	0
J1.75	LCD_DATA[2]	Boot Configuration Byte 1 Bit 2	0	0	0
J1.40	LCD_DATA[3]	Boot Configuration Byte 1 Bit 3	0	0	0
J1.26	LCD_DATA[4]	Boot Configuration Byte 1 Bit 4	0	0	0
J1.28	LCD_DATA[5]	Boot Configuration Byte 1 Bit 5	1	1	1
J1.30	LCD_DATA[6]	Boot Configuration Byte 1 Bit 6	0	1	1
J1.42	LCD_DATA[7]	Boot Configuration Byte 1 Bit 7	1	0	0
J1.20	LCD_DATA[8]	Boot Configuration Byte 2 Bit 0	0	0	0
J1.22	LCD_DATA[9]	Boot Configuration Byte 2 Bit 1	1	1	1
J1.46	LCD_DATA[10]	Boot Configuration Byte 2 Bit 2	0	0	0
J1.73	LCD_DATA[11]	Boot Configuration Byte 2 Bit 3	X	1	0
J1.18	LCD_DATA[12]	Boot Configuration Byte 2 Bit 4	0	0	0
J1.14	LCD_DATA[13]	Boot Configuration Byte 2 Bit 5	1	1	1
J1.16	LCD_DATA[14]	Boot Configuration Byte 2 Bit 6	0	0	0
J1.34	LCD_DATA[15]	Boot Configuration Byte 2 Bit 7	0	0	0
J1.06	LCD_DATA[16]	Boot Configuration Byte 4 Bit 0	0	0	0
J1.10	LCD_DATA[17]	Boot Configuration Byte 4 Bit 1	0	0	0
J1.08	LCD_DATA[18]	Boot Configuration Byte 4 Bit 2	0	0	0
J1.32	LCD_DATA[19]	Boot Configuration Byte 4 Bit 3	0	0	0
J1.04	LCD_DATA[20]	Boot Configuration Byte 4 Bit 4	0	0	0
J1.47	LCD_DATA[21]	Boot Configuration Byte 4 Bit 5	0	0	0
J1.02	LCD_DATA[22]	Boot Configuration Byte 4 Bit 6	0	0	0
J1.33	LCD_DATA[23]	Boot Configuration Byte 4 Bit 7	0	0	0
J2.33	BOOT0	Boot mode bit 0 signal	0	0	0
J2.31	BOOT1	Boot mode bit 1 signal	1	1	1

Table 5-1 Boot Configuration signals.

Note: 0 – Represents pull down or floating. 1 – Represents pull up of 10KΩ or stronger. X – Represents don't care.

For more information, please refer to i.MX6UL Reference Manual section 8.

6. Electrical specifications

6.1. Absolute maximum ratings

Parameter		Min	Max	Unit
VCC_3V3_IN	Main supply input voltage	-0.5	3.6	V
VCC_COIN	RTC supply input voltage	-0.5	3.6	V
USB_VBUS	USB_OTG1_VBUS, USB_OTG2_VBUS		5.5	V

Table 6-1 Absolute maximum ratings

6.2. Operating conditions

Parameter		Min	Typ	Max	Unit
VCC_3V3_IN	Main supply input voltage	3.2	3.3	3.6	V
VCC_COIN	RTC supply input voltage	3.0	3.3	3.6	V
USB_VBUS	USB_OTG1_VBUS, USB_OTG2_VBUS	4.4	5.0	5.5	V

Table 6-2 Operating conditions

6.3. Power Consumption

Mode	Voltage	Current	Power	Notes
Run	3.3V	350mA	1.15W	Linux up, Wi-Fi connected and Iperf is running 802.11 n 2.4GHz
Run	3.3V	130mA	429mW	Linux up
Standby	3.3V	4.5mA	14.85mW	Memory retention mode
Off (RTC)	3.0V	120uA	360uW	Off mode, only RTC is powered

Table 6-3 DART-6UL Power consumption

Note: Although the Max continuous supply current to the LWB Wi-Fi module is < 300 mA, when providing power to the Wi-Fi module, a power source capable of supplying 600 mA peak current for a duration of ~20 msec is required by the Wi-Fi module

Mode	Voltage	Current	Power	Notes
Run	3.3V	422mA	1.39W	Linux up, Wi-Fi connected and Iperf is running 802.11 ac 5GHz
Run	3.3V	400mA	1.32W	Linux up, Wi-Fi connected and Iperf is running 802.11 n 2.4GHz
Run	3.3V	148mA	488.4mW	Linux up
Standby	3.3V	4mA	13.2mW	Memory retention mode
Off (RTC)	3.0V	120uA	360uW	Off mode, only RTC is powered

Table 6-4 DART-6UL-5G Power consumption

Note: Although the Max continuous supply current to the LWB5 Wi-Fi module is < 320 mA, when providing power to the Wi-Fi module, a power source capable of supplying 750 mA peak current for a duration of ~20 msec is required by the Wi-Fi module

7. Environmental Specifications

	Min	Max
Commercial Operating Temperature Range	0 ^{0}C	+70 ^{0}C
Industrial Operating Temperature Range	-40^{0}C	+85 ^{0}C
Storage temperature	-40°C	85°C
Relative humidity (operation)	10%	90%
Relative humidity (storage)	05%	95%
Referring Telcordia Technologies Special Report SR-332, Issue 4 Reliability Prediction Method Model: 25Deg Celsius, Class B-1, GM	10296 Khrs >	

Note: Industrial Temperature is only based on the operating temperature grade of the SoM components. Customer should consider specific thermal design for the final product based upon the specific environmental and operational conditions.

8. Mechanical

8.1. The SOM board mounting to the Carrier board

The SOM has 4 mounting holes for mounting it to the carrier board.
The holes are plated inside and connected to GND.

Note:
The size and footprint of SOM 90-pin connectors Hirose P/N: DF40C-90DP-0.4V(51) is different from mating Carrier board 90-pin connectors Hirose P/N: DF40C-90DS-0.4V(51). To ensure correct positioning of your carrier board connectors and holes please refer to VAR-6ULCustomBoard DXF available here (under documentation tab):
http://www.variscite.com/products/single-board-computers/var-6ulcustomboard

8.2. SOM board mounting.

The SOM dimensions in mm are:

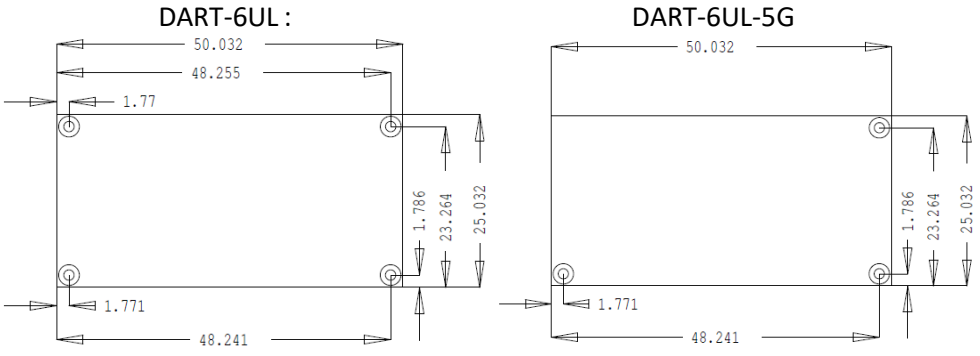

Figure 8-1 SOM Mechanical view

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