VARISCITE LTD.

DART–4460

Texas Instruments OMAP4^{TM}-based
System-on-Module
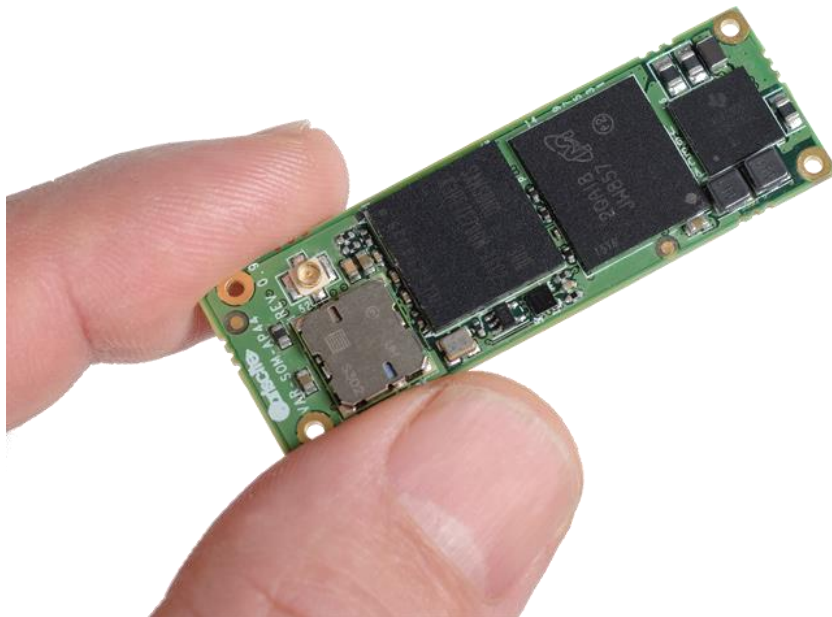
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DART-4460 Datasheet

Document Revision History

Revision		Date	Notes
PCB	**Data Sheet**		
1.0	**1.0**	09/05/2013	Preliminary
1.0	**1.01**	13/07/2013	Section 4.19 fixed. Input voltage DC-IN is 3.3-4.2v
1.0	**1.02**	16/07/2013	Connectors' names changed to J1, J2, and J3. J3 Connector pin-out change updated
1.0	**1.03**	16/07/2013	Sysboot pin clarifications.
1.0, 1.01	**1.04**	27/09/2013	Section 4.19. JTAG signals added
1.0, 1.01	**1.05**	25/10/2013	• Section 4.10 - Only MCBSP1 is supported • Section 4.12.4 – I2C on-SOM devices list
1.0, 1.01	**1.06**	09/11/2013	• PWM2 signal added • J1.57 pin description fixed • J1.43 pin description fixed • J1.8 pin description fixed
1.0, 1.01	**1.07**	10/01/2014	• Section descriptions 4.3.3 fixed • Section descriptions 4.3.4 fixed

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1 Overview

1.1 General Information

The DART-4460 is a high performance System-on-Module. It provides an ideal building block that easily integrates with a wide range of target markets requiring rich multimedia functionality, powerful graphics and video capabilities, as well as high-processing power. Compact, cost effective and with low power consumption, the DART-4460 secures an Intel Atom performance level.

Supporting products:

- DART-4460-ADAPTER – adapter to standard OM44 module
- VAR-OM44CustomBoard – evaluation board
  - ✓ Carrier - Board, compatible with DART-4460
  - ✓ Schematics
- O.S support
  - ✓ Android
  - ✓ Linux

Contact Variscite support services for further information: mailto:support@variscite.com.

1.2 Feature Summary

- Texas Instruments OMAP4460 CPU:
    - Up to 1.5 GHz Dual Core ARM Cortex™-A9 Processor with 1MB L2 cache. Each core has:
        - NEON™ Advanced SIMD and Vector Floating Point Unit (VFPv3) coprocessors
        - 32 KB Instruction an 32 KB Data L1 cache
    - High Definition image and video hardware accelerator (IVA-HD 1.0)
    - PowerVR™ SGX540 2D/3D graphics accelerator
    - DSP sub-system based on TMS320DMC64x+™ very long instruction word (VLIW) DSP core with 32 KB L1 cache and 128 KB L2 cache running at
- 512-1024 MB LPDDR2 SDRAM
- EMMC up to 8GBytes for storage and boot
- WLAN 802.11 b/g/n
- Triple Display:
    - 24-bit Parallel RGB
    - HDMI
    - Serial Display Interface (DSI)
- RAW image-sensor module interface
    - 16-bit Camera Parallel Interface (CPI)
    - 2 x Camera Serial Interface (CSI2)
- USB:
    - USB 2.0 high-speed host interface
    - USB 2.0 OTG interface
- Audio:
    - Head phone-out
    - Line-in
    - Digital microphone interface
    - Multichannel buffered serial port
- SDIO/MMC interface
- Local BUS (GPMC) Interface
- Bluetooth
- Keypad interface
- UART ports
- SPI
- I2C interfaces
- 1 – wire/ HDQ
- Power:
    - Single 3.3VDC - input power supply
    - RTC back-up battery input

1.3 Block Diagram
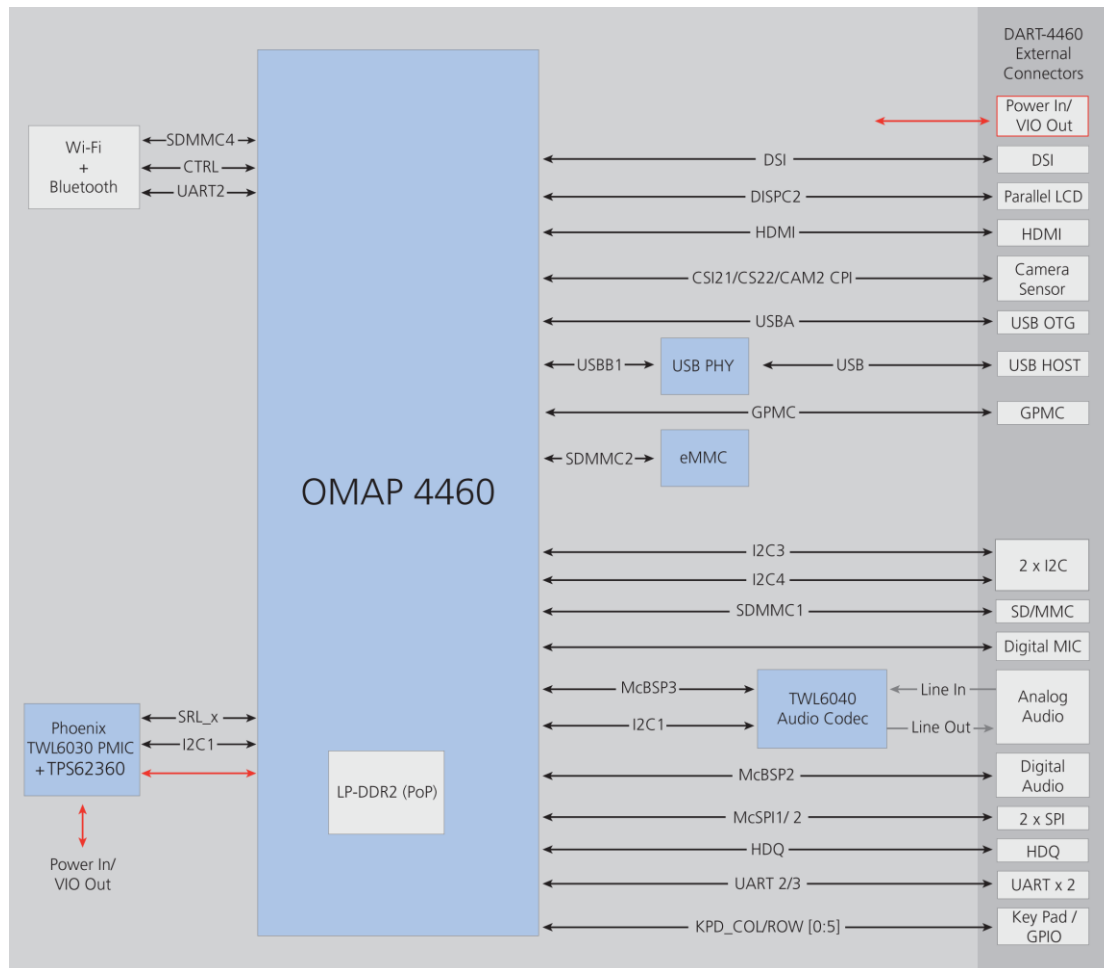
2 Main Hardware Components

This section summarizes the main hardware building blocks of the DART-4460

2.1 Texas Instruments OMAP4460

2.1.1 Overview

The OMAP4460 high-performance applications processor is based on the enhanced OMAP™ 4 architecture and uses 45 nm process technology.

The architecture is designed to provide best-in-class video, image and graphics processing which can support the following:

- Streaming video up to full HD
- 2D/3D mobile gaming
- Video conferencing
- High-resolution still image
- Video capture

The following subsystems are part of the OMPA4460 device:

- Up to 1.5 GHz , ARM® Cortex™-A9 microprocessor unit (MPU) subsystem based on the microprocessor, including two ARM® Cortex-A9 cores
- Digital Signal Processor (DSP) subsystem
- Image and Video Accelerator High-Definition (IVA-HD) subsystem
- Cortex™-M3 MPU subsystem, including two ARM Cortex-M3 microprocessors
- Display subsystem
- Audio Back-End (ABE) subsystem
- Imaging Sub-System (ISS), consisting of Image Signal Processor (ISP) and Still Image CO-Processor (SIMCOP) block
- 2D/3D graphic accelerator (SGX) subsystem
- Emulation (EMU) subsystem

2.1.2   OMAP4460 Block Diagram

OMAP4460 Block Diagram
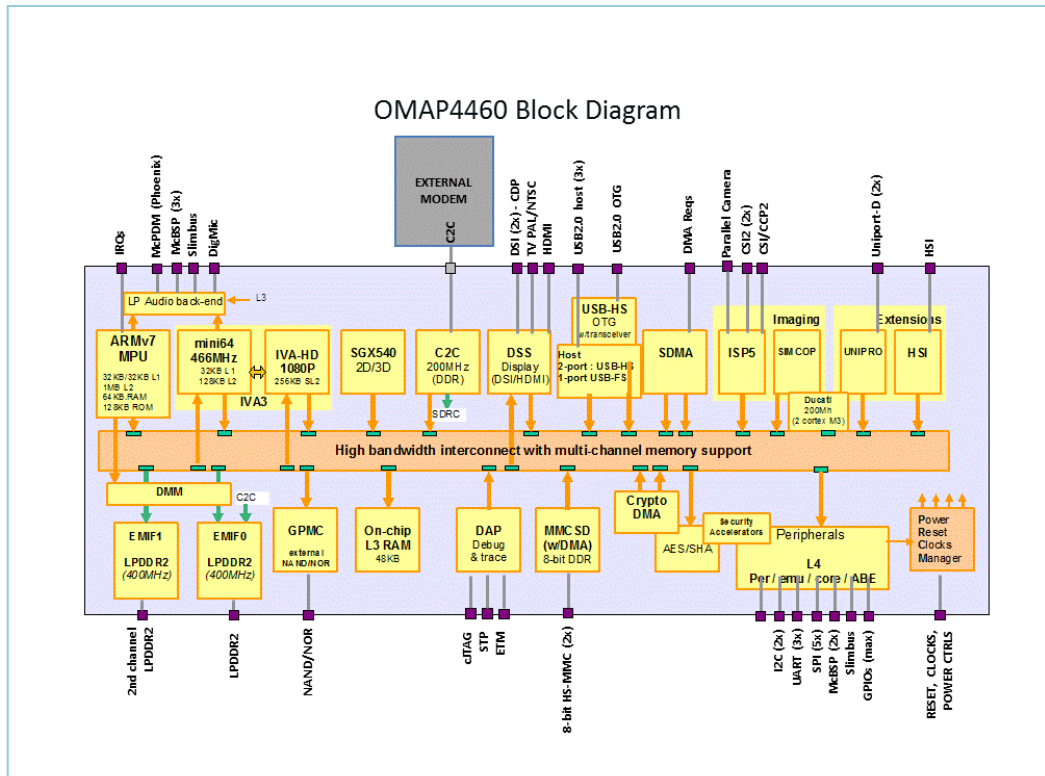
2.1.3   MPU Subsystem

The MPU subsystem integrates the following modules:

The Cortex-A9 MPU subsystem, integrating the following sub-modules:

- ARM Cortex-A9 MPCore
  - Two ARM Cortex-A9 central processing units (CPUs)
  - ARM Version 7 ISA™: Standard ARM instruction set plus Thumb®-2, Jazelle® RCT and Jazelle DBX Java™ accelerators
  - Neon™ SIMD coprocessor and VFPv3 per CPU
  - Interrupt controller (Cortex-A9 MPU INTC) with up to 128 interrupt requests
  - One general-purpose timer and one watchdog timer per CPU
  - Debug and trace features
  - 32 KB instruction and 32 KB data level 1 (L1) caches per CPU
- Shared 1 MB level 2 (L2) cache
- 48 KB bootable ROM
- Local power, reset, and clock management (PRCM) module
- Emulation features
- Digital phase-locked loop (DPLL)

2.1.4   External Memory Interfaces

The OMAP™ 4 includes two external memory interfaces:

- General Purpose Memory Controller (GPMC): The GPMC is an unified memory controller dedicated to interfacing external memory devices:
  - Asynchronous SRAM-like memories and application-specific integrated circuit (ASIC) devices
  - Asynchronous, synchronous, and page mode (only available in non-muxed mode) burst NOR flash devices
  - NAND Flash
  - Pseudo-SRAM devices
- EMIF Module: The EMIF module provides connectivity between the device and the LPDDR2-type memories and manages data bus read/write accesses between external memories, the microprocessor unit (MPU) and the direct memory access (DMA) controller.

2.1.5   DMA Controllers

The device embeds one generic DMA controller, the system DMA (sDMA) controller, used for memory-to-memory, memory-to-peripheral, and peripheral-to-memory transfers:

- One read port, one write port
- 32 logical DMA channels supporting among other features:
  - 8-bit, 16-bit, or 32-bit data element transfer size
  - Software-triggered or hardware-synchronized transfers
  - Flexible source and destination address generation
  - Burst read and write
  - Chained multiple-channel transfers
  - Endianism conversion
  - Draining

- Up to 127 DMA requests
- 256 x 64-bit FIFO dynamically allocable between active channels

2.1.6   Display Subsystem

The Display Sub-System (DSS) provides the logic to display a video frame from the memory frame buffer on a Liquid Crystal Display (LCD) panel or a TV set.

LCD Interface:

The primary LCD output:
- DSI1 (MIPI® DSI) - SXGA (1400x1050) VESA timing @ 60 FPS

The secondary LCD output:
- Parallel RGB output (MIPI DPI 1.0) - SXGA (1400x1050) VESA timing @ 85 fps1080i/720p

HDMI interface:

High-Definition Multimedia Interface (using TV set out) - HD-1080p, HD-1080i, HD-720p, SD-480p, SD-576p, SD-576i, and SD-480i using HDMI

2.1.7   IVA-HD Subsystem

The IVA-HD subsystem is a set of video encoder/decoder hardware accelerators. It supports up to 1080p × 30 fps, slow-motion camcorder, triple play (HD and SD capture and JPEG capture), real-time transcoding of up to 720p, and video conferencing up to 720p.

The IVA-HD supports the following formats:

- MPEG-1/-2/-4 such as MPEG-2 MP, ML, and MPEG-4 as SP/ASP
- DivX 5.02 and above
- Sorenson Spark (decode)
- H.263 P0 (encode/decode) and P3 (decode)
- H.264 Annex G (scalable baseline profile up to 720p)
- H.264 BL/MP/HP
- H.264 Annex H (partial)
- Stereoscopic video
- JPEG (encode/decode)
- VC-1 SP/MP/AP
- AVS-1.0
- RealVideo® 8/9/10 (decode only)
- On2® VP6.2/VP7 (decode only)

2.1.8   2D and 3D Graphics Accelerator (SGX)

The 2D/3D graphics accelerator (SGX) subsystem accelerates 2-Dimensional (2D) and 3-Dimensional (3D) graphics applications. The SGX subsystem is based on the PowerVR® SGX core from Imagination Technologies. SGX is a new generation of programmable PowerVR graphics IP cores. The PowerVR SGX540 v1.2.0 architecture is scalable and can target all market segments from mainstream mobile devices to high-end desktop graphics. PowerVR® SGX main features:

- 3D graphics, vector graphics, and video supported on common hardware
- Tile-based architecture
- Universal Scalable Shader Engine (USSE™): a multi-threaded engine that incorporates pixel and vertex shader functionality and reduces die area
- Advanced shader feature set in excess of Microsoft VS3.0, PS3.0, and OpenGL™2.0
- Industry standard application programming interface (API) support: OpenGL ES 1.1 and 2.0, OpenVG v1.1
- Fine-grained task switching, load balancing, and power management
- Advanced geometry, direct memory access (DMA)-driven operation for minimum CPU interaction
- Programmable high-quality image anti-aliasing

- Fully virtualized memory addressing for Operating System (OS) functioning in a unified memory architecture

2.1.9 Imaging Sub-System

The Imaging Sub-System (ISS) deals with the processing of the pixel data coming from an external image sensor, data from memory (image format encoding and decoding can be done to and from memory), or data from SL2 in IVA-HD for hardware encoding. With subparts, such as interfaces and interconnects, Image Signal Processor (ISP), and Still Image COProcessor (SIMCOP), the ISS is a key component for the following multimedia applications: Camera viewfinder, video record, and still image capture.

The ISS is mainly composed of CCP2 and CSI2-A, CSI2-B camera interfaces, a parallel interface (CPI), an ISP and a block-based imaging accelerator (SIMCOP). The ISS is designed to reach high throughput and low latency with large image sensors. In high-performance mode, the ISS supports a pixel throughput of 200 MPix/s.

The ISS targets the following major use cases:
- Viewfinder with digital zoom, video stabilization, and rotations
- Up to 1080 p video record at 30 fps with digital zoom, video stabilization, and rotation
  Up to 16 MPix still image capture with digital zoom and rotation
  High performance mode: Up to 200 MPix/s throughput
- High quality and low light modes: Up to 50 MPix/s throughputs
- Still image capture during video record

2.1.10 Audio Back End

The Audio Back End (ABE) module is a subsystem that manages various audio and voice uplink and downlink streams between the initiator (the Cortex™-A9 microprocessor unit [MPU], Digital Signal Processor [DSP], or Direct Memory Access [DMA] controller) and the peripheral physical interfaces (Multichannel Buffered Serial Port [McBSP], SLIMbus®, Digital MICrocontroller [DMIC], Multichannel Pulse Density Modulation [McPDM], and Multichannel Audio Serial Port [McASP]). In addition it contains Audio Engine (AE) that performs some real-time signal processing like sample rate conversion, filtering, equalizing, and side-tone.

2.2 Memory

2.2.1 RAM

The DART-4460 is available with 512 or 1024 MB of LPDDR2 memory, using Package-on-Package (PoP) technology.

2.2.2 Non-volatile Storage Memory

The on board EMMC up to 8GBytes is used for boot and as a mass storage device.

2.3 TWL6041 Audio

The TWL6041 device is an audio coder/decoder (codec) with a high level of integration providing analog audio codec functions for portable applications. It contains multiple audio analog inputs

and outputs, as well as microphone biases and accessory detection. The device is connected to the OMAP4™ host processor through a proprietary PDM interface for audio data communication enabling partitioning with optimized power consumption and performance. Multichannel audio data is multiplexed to a single wire for downlink (PDML) and uplink (PDMUL).

DART-4460 utilizes TWL6041's line-in and the headphone driver analog interfaces.

2.4 TWL6032 PMIC

The TWL6032 is a dedicated integrated power-management IC for the OMAP4™ platform and supports the OMAP4460 power-management architecture to ensure maximum performance and operation time for user satisfaction (audio/video support) while offering versatile power-management techniques for maximum design flexibility, depending on application requirements.

The device provides seven configurable step-down converters with up to 1.6 A capability for memory, processor core, I/O, auxiliary, pre-regulation for LDOs, etc. The device also contains 11 LDO regulators that can be supplied from a battery or a pre-regulated supply. Power-up/power-down controller is configurable and can support any power-up/power-down sequences (EPROM based). The Real-Time Clock (RTC) provides a 32-kHz output buffer, second/minute/hour/day/month/year information and alarm wake up.

3 External Connectors

The DART-4460 exposes tree low profile connectors. Two are 70 pin and one is 40 pin. The recommended mating connectors for baseboard are DF40C-70DS-0.4V(51), DF40C-40DS-0.4V(51) or equivalent.

The following list describes this chapter's column header tables:

Pin#:
Pin Number on the external connector

Pin Name:
Default DART-4460 Pin Name

Type:
Pin Type & Direction:
- I – In
- O – Out
- DS – Differential Signal
- A – Analog
- Power – Power Pin

Pin Group:
Pin Functionality group

OMAP4 Ball:
OMAP4460 ball number

Mode (Tables 3.2 & 3.4):
OMAP4^{TM} – Pin Mux mode option

J1			
Pin #	Pin Name	Pin Group	Ball
1	I2C4_SDA	I2C4 Interface / Pin Mux Table 3.2	AH22
2	I2C4_SCL	I2C4 Interface / Pin Mux Table 3.2	AG21
3	VIO	Main Power	
4	USBHOST_DN	USB HOST1	
5	RESET_IN	Reset In - Active Low	
6	USBHOST_DP	USB HOST1	
7	VBACKUP	Real time clock power in	
8	SYS_BOOT1/GPIO_184	Sys boot select / Pin Mux Table 3.2	F26
9	GND	Digital GND	
10	VBAT	Main Power	
11	I2C3_SDA/GPIO_131	I2C3 Interface[1]	Y27
12	VBAT	Main Power	
13	I2C3_SCL/GPIO_130	I2C3 Interface[1]	W27
14	VBAT	Main Power	
15	ABE_McBSP2_FSX/McSPI2_CS0//GPIO_113	MCBSP2 Interface / Pin Mux Table 3.2	AC28
16	VBAT	Main Power	
17	ABE_McBSP2_DX/McSPI2_SIMO/GPIO_112	MCBSP2 Interface / Pin Mux Table 3.2	AD25
18	GND	Digital GND	
19	ABE_McBSP2_DR/McSPI2_SOMI/GPIO_111	MCBSP2 Interface / Pin Mux Table 3.2	AD26
20	USB_HOST_VBUS	USB HOST1	
21	ABE_McBSP2_CLKX/McSPI2_CLK/GPIO_110	MCBSP2 Interface / Pin Mux Table 3.2	AD27
22	USB_OTG_VBUS	USB OTG Bus Power	
23	GPMC_nCS5/DSI1_TE1/GPIO_102/SYS_NDMAREQ2	GPMC Interface /Pin Mux Table 3.4	B24
24	USB_OTG_DP	USB On The Go / Pin Mux Table 3.2	B5
25	GND	Digital GND	
26	USB_OTG_DM	USB On The Go / Pin Mux Table 3.2	B4
27	UART3_CTS_RCTX	UART3 Port / Pin Mux Table 3.2	F27
28	USB_OTG_ID	USB On The Go Device Type	
29	UART3_RTS_IRSD	UART3 Port / Pin Mux Table 3.2	F28
30	GND	Digital GND	
31	UART3_RX_IRRX	UART3 Port / Pin Mux Table 3.2	G27
32	UART2_RX/SDMMC3_DAT0/GPIO_125	UART2 Port/ / Pin Mux Table 3.2 [1]	AA25
33	UART3_TX_IRTX	UART3 Port / Pin Mux Table 3.2	G28
34	UART2_TX/SDMMC3_DAT1/GPIO_126	UART2 Port/ / Pin Mux Table 3.2 [1]	AA26
35	McSPI1_CS0/GPIO_137	SPI1 Interface / Pin Mux Table 3.2	AE23
36	UART2_RTS/SDMMC3_CMD/GPIO_124	UART2 Port/ / Pin Mux Table 3.2 [1]	AB27
37	McSPI1_CLK/GPIO_134	SPI1 Interface / Pin Mux Table 3.2	AF22
38	UART2_CTS/SDMMC3_CLK/GPIO_123	UART2 Port/ / Pin Mux Table 3.2 [1]	AB26

39	McSPI1_SIMO/GPIO_136	SPI1 Interface / Pin Mux Table 3.2	AG22
40	KPD_ROW2/CAM2_D11/GPIO_3	Keypad Interface / Pin Mux Table 3.2	K27
41	McSPI1_SOMI/GPIO_135	SPI1 Interface / Pin Mux Table 3.2	AE22
42	KPD_ROW3/CAM2_D4/GPIO_175	Keypad Interface / Pin Mux Table 3.2	J26
43	VPMIC_VAUX1_2V8	2.8v output for external use	
44	MMC1_CD	MMC1 Card detect	
45	HDQ_SIO/GPIO_127	One Wire Interface / Pin Mux Table 3.2	AA27
46	DMIC_DIN3/GPIO_122/DMTIMER9_PWM_EVT	PWM / Pin Mux Table 3.2	AH24
47	GND	Digital GND	
48	GND	Digital GND	
49	GPMC_nCS4/GPIO_101/SYS_NDMAREQ1	GPMC Interface /Pin Mux Table 3.4	A24
50	DMIC_CLK1/GPIO_119	Digital Microphone Clock / Pin Mux Table 3.2	AE24
51	FREF_CLK1_OUT/GPIO_181	Reference Clock Out / Pin Mux Table 3.2	AA28
52	DMIC_DIN2/GPIO_121/DMTIMER11_PWM_EVT	Digital Microphone Data /Pin Mux Table 3.2	AG24
53	CSI21_DX3/GPI_73	Camera Interface / Pin Mux Table 3.2	V26
54	CSI21_DX0/GPI_67	Camera Interface / Pin Mux Table 3.2	R26
55	CSI21_DY3/GPI_74	Camera Interface / Pin Mux Table 3.2	V25
56	CSI21_DY0/GPI_68	Camera Interface / Pin Mux Table 3.2	R25
57	TWL6030 PWM2		
58	GND	Digital GND	
59	CSI21_DX4/GPI_75	Camera Interface / Pin Mux Table 3.2	W26
60	CSI21_DX2/GPI_71	Camera Interface / Pin Mux Table 3.2	U26
61	CSI21_DY4/GPI_76	Camera Interface / Pin Mux Table 3.2	W25
62	CSI21_DY2/GPI_72	Camera Interface / Pin Mux Table 3.2	U25
63	CSI22_DX1/GPI_79	Camera Interface / Pin Mux Table 3.2	N26
64	CSI21_DX1/GPI_69	Camera Interface / Pin Mux Table 3.2	T26
65	CSI22_DY1/GPI_80	Camera Interface / Pin Mux Table 3.2	N25
66	CSI21_DY1/GPI_70	Camera Interface / Pin Mux Table 3.2	T25
67	CSI22_DX0/GPI_77	Camera Interface / Pin Mux Table 3.2	M26
68	CSI22_DX2/CAM2_FID	Camera Interface / Pin Mux Table 3.2	N27
69	CSI22_DY0/GPI_78	Camera Interface / Pin Mux Table 3.2	M25
70	CSI22_DY2/CAM2_WEN	Camera Interface / Pin Mux Table 3.2	M27

Table 3-1 J1 Connector Pin Out

Notes:

[1] The UART2 is used for on board Bluetooth connectivity. Pin mode can't be changed if Wi-Fi/Bluetooth is enabled.

J2			
Pin #	Pin Name	Pin Group	Ball
1	DSI1_DX0	MIPI DSI Interface	P3
2	DSI1_DY1	MIPI DSI Interface	N4
3	DSI1_DY0	MIPI DSI Interface	P4
4	DSI1_DX1	MIPI DSI Interface	N3
5	DSI1_DX2	MIPI DSI Interface	M3
6	DSI1_DY3	MIPI DSI Interface	L4
7	DSI1_DY2	MIPI DSI Interface	M4
8	DSI1_DX3	MIPI DSI Interface	L3
9	DISPC2_DATA3/DSI1_TE0/GPIO_27	DPI / Pin Mux Table 3.2	AB2
10	DSI1_DY4	MIPI DSI Interface	K4
11	DISPC2_DATA5/SDIxx/GPIO_25	DPI / Pin Mux Table 3.2	AA3
12	DSI1_DX4	MIPI DSI Interface	K3
13	DISPC2_DATA7/SDIxx/GPIO_23	DPI / Pin Mux Table 3.2	AA1
14	DISPC2_DATA2/DSI1_TE1/GPIO_28	DPI / Pin Mux Table 3.2	AB3
15	GND	Digital GND	
16	DISPC2_DATA4/SDIxx/GPIO_26	DPI / Pin Mux Table 3.2	AA4
17	DISPC2_DATA11/SDIxx/GPIO_168	DPI / Pin Mux Table 3.2	AE9
18	DISPC2_DATA6/SDIxx/GPIO_24	DPI / Pin Mux Table 3.2	AA2
19	DISPC2_DATA13/SDIxx/GPIO_166	DPI / Pin Mux Table 3.2	AF10
20	GND	Digital GND	
21	DISPC2_DATA15/GPIO_164	DPI / Pin Mux Table 3.2	AH11
22	DISPC2_DATA10/SDIxx/GPIO_14	DPI / Pin Mux Table 3.2	V1
23	DISPC2_DATA17/GPIO_17	DPI / Pin Mux Table 3.2	W2
24	DISPC2_DATA12/SDIxx/GPIO_167	DPI / Pin Mux Table 3.2	AG10
25	DISPC2_DATA19/GPIO_162	DPI / Pin Mux Table 3.2	AF11
26	DISPC2_DATA14/GPIO_165	DPI / Pin Mux Table 3.2	AE10
27	DISPC2_DATA21/GPIO_160	DPI / Pin Mux Table 3.2	AG13
28	DISPC2_DATA9/GPIO_15	DPI / Pin Mux Table 3.2	V2
29	DISPC2_DATA23/GPIO_158	DPI / Pin Mux Table 3.2	AF12
30	DISPC2_DATA18/SDIxx/GPIO_163	DPI / Pin Mux Table 3.2	AG11
31	DISPC2_DATA16/GPIO_16	DPI / Pin Mux Table 3.2	W1
32	DISPC2_DATA20/SDIxx/GPIO_161	DPI / Pin Mux Table 3.2	AE11
33	DISPC2_VSYNC/GPIO_20	DPI / Pin Mux Table 3.2	Y2
34	DISPC2_DATA22//GPIO_159	DPI / Pin Mux Table 3.2	AE12
35	GND	Digital GND	
36	DISPC2_HSYNC/GPIO_18	DPI / Pin Mux Table 3.2	W3
37	SDMMC1_CMD	SDMMC1 Interface/Pin Mux Table 3.2	E3

38	DISPC2_PCLK/GPIO_19	DPI / Pin Mux Table 3.2	W4
39	SDMMC1_CLK	SDMMC1 Interface/Pin Mux Table 3.2	D2
40	DISPC2_DATA8/GPIO_22	DPI / Pin Mux Table 3.2	Y4
41	I2C2_SCL/UART1_RX/GPIO_128	UART1 Port / Pin Mux Table 3.2	C26
42	DISPC2_DE/GPIO_21	DPI / Pin Mux Table 3.2	Y3
43	McSPI1_CS3/UART1_RTS/GPIO_140	UART1 Port / Pin Mux Table 3.2	AH23
44	DISPC2_DATA0/DSI2_TE1	DPI / Pin Mux Table 3.2	AC4
45	McSPI1_CS2/UART1_CTS/GPIO_139	UART1 Port / Pin Mux Table 3.2	AG23
46	DISPC2_DATA1/DSI2_TE0	DPI / Pin Mux Table 3.2	AB4
47	I2C2_SDA/UART1_TX/GPIO_129	UART1 Port / Pin Mux Table 3.2	D26
48	SDMMC1_DAT0	SDMMC1 Interface/Pin Mux Table 3.2	E4
49	AUD_IN_L	Audio Line In Left	
50	SDMMC1_DAT1	SDMMC1 Interface/Pin Mux Table 3.2	E2
51	AUD_IN_R	Audio Line In Right	
52	SDMMC1_DAT2	SDMMC1 Interface/Pin Mux Table 3.2	E1
53	AUD_OUT_R	Headphone Out Right	
54	SDMMC1_DAT3	SDMMC1 Interface/Pin Mux Table 3.2	F4
55	AUD_OUT_L	Headphone Out Left	
56	HDMI_DATA1X	HDMI Interface	C9
57	AUD_GND	Audio GND	
58	HDMI_DATA1Y	HDMI Interface	D9
59	HDMI_DATA0Y	HDMI Interface	D10
60	HDMI_HPD/GPIO_63	HDMI Hot plug detect / Pin Mux Table 3.2	B9
61	HDMI_DATA0X	HDMI Interface	C10
62	HDMI_CLOCKY	HDMI Interface	D11
63	GND	Digital GND	
64	HDMI_CLOCKX	HDMI Interface	C11
65	HDMI_DDC_SDA/GPIO_66	HDMI Display Data Control / Pin Mux Table 3.2	B8
66	HDMI_CEC/GPIO_64	Consumer Electronic Control / Pin Mux Table 3.2	B10
67	HDMI_DATA2X	HDMI Interface	C8
68	HDMI_DDC_SCL/GPIO_65	HDMI Display Data Control / Pin Mux Table 3.2	A8
69	HDMI_DATA2Y	HDMI Interface	D8
70	GND	Digital GND	

Table 3-2 J2 Connector Pin Out

J3			
Pin #	Pin Name	Pin Group	Ball
1	KPD_COL2/KPD_COL5/CAM2_D10/GPIO_1	KPAD Interface /Pin Mux Table 3.4	H27
2	KPD_COL3/KPD_COL0/CAM2_D0/GPIO_171	KPAD Interface /Pin Mux Table 3.4	G26
3	KPD_COL1/KPD_COL4/CAM2_D8/GPIO_0	KPAD Interface /Pin Mux Table 3.4	J27
4	KPD_COL4/KPD_COL1/CAM2_D1/GPIO_172	KPAD Interface /Pin Mux Table 3.4	G25
5	KPD_COL0/KPD_COL3/CAM2_D3	KPAD Interface /Pin Mux Table 3.4	H25
6	KPD_COL5/KPD_COL2/CAM2_D2/GPIO_173	KPAD Interface /Pin Mux Table 3.4	H26
7	CAM_SHUTTER/GPIO_81	Camera Interface / Pin Mux Table 3.2	T27
8	KPD_ROW1/KPD_ROW4/GPIO_2	KPAD Interface /Pin Mux Table 3.4	L27
9	CAM_STROBE/GPIO_82	Camera Interface / Pin Mux Table 3.2	U27
10	GND	Digital GND	
11	CAM_GLOBALRESET/GPIO_83	Camera Interface / Pin Mux Table 3.2	V27
12	GPMC_AD14	GPMC Interface /Pin Mux Table 3.4	C19
13	GND	Digital GND	
14	GPMC_AD13	GPMC Interface /Pin Mux Table 3.4	D18
15	GPMC_A22/GPIO_46	GPMC Interface /Pin Mux Table 3.4	A21
16	GPMC_AD12	GPMC Interface /Pin Mux Table 3.4	C18
17	GPMC_AD0/SDMMC2_DAT0	GPMC Interface /Pin Mux Table 3.4	C12
18	GPMC_AD11	GPMC Interface /Pin Mux Table 3.4	D17
19	GPMC_AD15/GPIO39	GPMC Interface /Pin Mux Table 3.4	D19
20	GPMC_AD10	GPMC Interface /Pin Mux Table 3.4	C17
21	GPMC_nWP/DSI1_TE0/GPIO_54	GPMC Interface /Pin Mux Table 3.4	C25
22	GPMC_AD9	GPMC Interface /Pin Mux Table 3.4	D16
23	GPMC_CLK/GPIO_55/SYS_nDMAREQ2	GPMC Interface /Pin Mux Table 3.4	B22
24	GPMC_AD8	GPMC Interface /Pin Mux Table 3.4	C16
25	GPMC_nADV_ALE/DSI1_TE1/GPIO_56/SYS_NDMAREQ3	GPMC Interface /Pin Mux Table 3.4	D25
26	GPMC_AD7	GPMC Interface /Pin Mux Table 3.4	B16
27	GPMC_nOE/SDMMC2_CLK	GPMC Interface /Pin Mux Table 3.4	B11
28	GPMC_AD6	GPMC Interface /Pin Mux Table 3.4	A16
29	GPMC_nWE/SDMMC2_CMD	GPMC Interface /Pin Mux Table 3.4	B12
30	GPMC_AD5	GPMC Interface /Pin Mux Table 3.4	D15
31	GPMC_NBE0_CLE/GPIO_59	GPMC Interface /Pin Mux Table 3.4	C23
32	GPMC_AD4	GPMC Interface /Pin Mux Table 3.4	C15
33	GPMC_nCS0/GPIO_50	GPMC Interface /Pin Mux Table 3.4	B25
34	GPMC_AD3_SDMMC2_D3	GPMC Interface /Pin Mux Table 3.4	D13
35	GPMC_A20/GPIO_44	GPMC Interface /Pin Mux Table 3.4	B19
36	GPMC_AD2_SDMMC2_D2	GPMC Interface /Pin Mux Table 3.4	C13
37	GPMC_A21/GPIO_45	GPMC Interface /Pin Mux Table 3.4	B20
38	GPMC_AD1_SDMMC2_D1	GPMC Interface /Pin Mux Table 3.4	D12
39	GND	Digital GND	
40	GND	Digital GND	

Table 3-3 J3 Connector Pin Out

3.1 Pin Mux

The table below summarizes the additional available on the various connectors

Pin #	Mode 0	Mode 1	Mode 2	Mode 3	Mode 4	Mode 5
J1.1	i2c4_sda			gpio_133		
J1.2	i2c4_scl			gpio_132		
J1.8	sys_boot0			gpio_184		
J1.11	i2c3_sda			gpio_131		
J1.13	i2c3_scl			gpio_130		
J1.15	abe_mcbsp2_fsx	mcspi2_cs0	abe_mcasp_afsx	gpio_113	usbb2_mm_txen	
J1.17	abe_mcbsp2_dx	mcspi2_simo	abe_mcasp_amute	gpio_112	usbb2_mm_rxrcv	
J1.19	abe_mcbsp2_dr	mcspi2_somi	abe_mcasp_axr	gpio_111	usbb2_mm_rxdp	
J1.21	abe_mcbsp2_clkx	mcspi2_clk	abe_mcasp_ahclkx	gpio_110	usbb2_mm_rxdm	
J1.23	c2c_data13	dsi1_te1	c2c_clkin1	gpio_102	sys_ndmareq2	
J1.24	usba0_otg_dp	uart3_rx_irrx	uart2_rx	gpio_179		
J1.26	usba0_otg_dm	uart3_tx_irtx	uart2_tx	gpio_180		
J1.27	uart3_cts_rctx	uart1_tx		gpio_141		
J1.29	uart3_rts_sd			gpio_142		
J1.31	uart3_rx_irrx	dmtimer8_pwm_evt		gpio_143		
J1.32	uart2_rx	sdmmc3_dat0		gpio_125		
J1.33	uart3_tx_irtx	dmtimer9_pwm_evt	cam2_strobe	gpio_144		
J1.34	uart2_tx	sdmmc3_dat1		gpio_126		
J1.35	mcspi1_cs0			gpio_137		
J1.36	uart2_rts	sdmmc3_cmd		gpio_124		
J1.37	mcspi1_clk			gpio_134		
J1.38	uart2_cts	sdmmc3_clk		gpio_123		
J1.39	mcspi1_simo			gpio_136		
J1.40	unipro_ry2	kpd_row5	cam2_d11	gpi_3		
J1.41	mcspi1_somi			gpio_135		
J1.42	unipro_rx0	kpd_row0	cam2_d4	gpi_175		
J1.43	VPMIC_VAUX1_2V8					
J1.45	hdq_sio	i2c3_sccb	i2c2_sccb	gpio_127		
J1.46	abe_dmic_din3	slimbus2_data	abe_dmic_clk2	gpio_122		
J1.49	c2c_data12	dsi1_te0	c2c_clkin0	gpio_101	sys_ndmareq1	
J1.50	abe_dmic_clk1			gpio_119	usbb2_mm_txse0	
J1.51	fref_clk1_out			gpio_181		
J1.52	abe_dmic_din2	slimbus2_clock		gpio_121		
J1.53	csi21_dx3	cam2_d7		gpi_73		
J1.54	csi21_dx0			gpi_67		
J1.55	csi21_dy3	cam2_d6		gpi_74		
J1.56	csi21_dy0			gpi_68		
J1.59	csi21_dx4	cam2_d5		gpi_75		
J1.60	csi21_dx2			gpi_71		
J1.61	csi21_dy4			gpi_76		
J1.62	csi21_dy2			gpi_72		
J1.63	csi22_dx1		cam2_d14	gpi_79		
J1.64	csi21_dx1			gpi_69		
J1.65	csi22_dy1		cam2_d15	gpi_80		
J1.66	csi21_dy1			gpi_70		
J1.67	csi22_dx0		cam2_d12	gpi_77		
J1.68	csi22_dx2		cam2_fld			
J1.69	csi22_dy0		cam2_d13	gpi_78		
J1.70	csi22_dy2		cam2_wen			
J2.9	dpm_emu16	dmtimer8_pwm_evt	dsi1_te0	gpio_27	rfbi_data3	dispc2_data3
J2.11	dpm_emu14	sys_drm_msecure	uart1_rx	gpio_25	rfbi_data5	dispc2_data5

Pin #	Mode 0	Mode 1	Mode 2	Mode 3	Mode 4	Mode 5
J2.13	dpm_emu12	usba0_ulpiphy_dat6		gpio_23	rfbi_data7	dispc2_data7
J2.14	dpm_emu17	dmtimer9_pwm_evt	dsi1_te1	gpio_28	rfbi_data2	dispc2_data2
J2.16	dpm_emu15	sys_secure_indicator		gpio_26	rfbi_data4	dispc2_data4
J2.17	usbb2_ulpitll_dat7	usbb2_ulpiphy_dat7	sdmmc3_clk	gpio_168	mcspi3_clk	dispc2_data11
J2.18	dpm_emu13	usba0_ulpiphy_dat7		gpio_24	rfbi_data6	dispc2_data6
J2.19	usbb2_ulpitll_dat5	usbb2_ulpiphy_dat5	sdmmc3_dat3	gpio_166	mcspi3_cs0	dispc2_data13
J2.21	usbb2_ulpitll_dat3	usbb2_ulpiphy_dat3	sdmmc3_dat1	gpio_164	hsi2_caready	dispc2_data15
J2.22	dpm_emu3	usba0_ulpiphy_stp		gpio_14		dispc2_data10
J2.23	dpm_emu6	usba0_ulpiphy_dat0	uart3_tx_irtx	gpio_17	rfbi_hsync0	dispc2_data17
J2.24	usbb2_ulpitll_dat6	usbb2_ulpiphy_dat6	sdmmc3_cmd	gpio_167	mcspi3_simo	dispc2_data12
J2.25	usbb2_ulpitll_dat1	usbb2_ulpiphy_dat1	sdmmc4_dat3	gpio_162	hsi2_acdata	dispc2_data19
J2.26	usbb2_ulpitll_dat4	usbb2_ulpiphy_dat4	sdmmc3_dat0	gpio_165	mcspi3_somi	dispc2_data14
J2.27	usbb2_ulpitll_nxt	usbb2_ulpiphy_nxt	sdmmc4_dat1	gpio_160	hsi2_acready	dispc2_data21
J2.28	dpm_emu4	usba0_ulpiphy_dir		gpio_15		dispc2_data9
J2.29	usbb2_ulpitll_stp	usbb2_ulpiphy_stp	sdmmc4_clk	gpio_158	hsi2_cadata	dispc2_data23
J2.30	usbb2_ulpitll_dat2	usbb2_ulpiphy_dat2	sdmmc3_dat2	gpio_163	hsi2_acflag	dispc2_data18
J2.31	dpm_emu5	usba0_ulpiphy_nxt		gpio_16	rfbi_te_vsync0	dispc2_data16
J2.32	usbb2_ulpitll_dat0	usbb2_ulpiphy_dat0	sdmmc4_dat2	gpio_161	hsi2_acwake	dispc2_data20
J2.33	dpm_emu9	usba0_ulpiphy_dat3	uart3_cts_rctx	gpio_20	rfbi_we	dispc2_vsync
J2.34	usbb2_ulpitll_dir	usbb2_ulpiphy_dir	sdmmc4_dat0	gpio_159	hsi2_caflag	dispc2_data22
J2.36	dpm_emu7	usba0_ulpiphy_dat1	uart3_rx_irrx	gpio_18	rfbi_cs0	dispc2_hsync
J2.37	sdmmc1_cmd		uart1_rx	gpio_101		
J2.38	dpm_emu8	usba0_ulpiphy_dat2	uart3_rts_sd	gpio_19	rfbi_re	dispc2_pclk
J2.39	sdmmc1_clk		dpm_emu19	gpio_100		
J2.40	dpm_emu11	usba0_ulpiphy_dat5		gpio_22	rfbi_data8	dispc2_data8
J2.41	i2c2_scl	uart1_rx		gpio_128		
J2.42	dpm_emu10	usba0_ulpiphy_dat4		gpio_21	rfbi_a0	dispc2_de
J2.43	mcspi1_cs3	uart1_rts	slimbus2_data	gpio_140		
J2.44	dpm_emu19	dmtimer11_pwm_evt	dsi2_te1	gpio_191	rfbi_data0	dispc2_data0
J2.45	mcspi1_cs2	uart1_cts	slimbus2_clock	gpio_139		
J2.46	dpm_emu18	dmtimer10_pwm_evt	dsi2_te0	gpio_190	rfbi_data1	dispc2_data1
J2.47	i2c2_sda	uart1_tx		gpio_129		
J2.48	sdmmc1_dat0		dpm_emu18	gpio_102		
J2.50	sdmmc1_dat1		dpm_emu17	gpio_103		
J2.52	sdmmc1_dat2		dpm_emu16	gpio_104	jtag_tms_tmsc	
J2.54	sdmmc1_dat3		dpm_emu15	gpio_105	jtag_tck	
J2.60	hdmi_hpd			gpio_63		
J2.65	hdmi_ddc_sda			gpio_66		
J2.66	hdmi_cec			gpio_64		
J2.68	hdmi_ddc_scl			gpio_65		
J3.1	unipro_ty2	kpd_col5	cam2_d10	gpio_1		
J3.2	unipro_tx0	kpd_col0	cam2_d0	gpio_171		
J3.3	unipro_tx2	kpd_col4	cam2_d8	gpio_0		
J3.4	unipro_ty0	kpd_col1	cam2_d1	gpio_172		
J3.5	unipro_ty1	kpd_col3	cam2_d3	gpio_174		
J3.6	unipro_tx1	kpd_col2	cam2_d2	gpio_173		
J3.7	cam_shutter		cam2_hs	gpio_81		
J3.8	unipro_rx2	kpd_row4	cam2_d9	gpi_2		
J3.9	cam_strobe		cam2_vs	gpio_82		
J3.11	cam_globalreset		cam2_pclk	gpio_83		
J3.12	gpmc_ad14	kpd_col2	c2c_data9	gpio_38		
J3.14	gpmc_ad13	kpd_col1	c2c_data10	gpio_37		
J3.15	gpmc_a22	kpd_col6	c2c_datain6	gpio_46	venc_656_data6	

Pin #	Mode 0	Mode 1	Mode 2	Mode 3	Mode 4	Mode 5
J3.16	gpmc_ad12	kpd_col0	c2c_data11	gpio_36		
J3.17	gpmc_ad0	sdmmc2_dat0				
J3.18	gpmc_ad11	kpd_row3	c2c_data12	gpio_35		
J3.19	gpmc_ad15	kpd_col3	c2c_data8	gpio_39		
J3.20	gpmc_ad10	kpd_row2	c2c_data13	gpio_34		
J3.21	gpmc_nwp	dsi1_te0		gpio_54	sys_ndmareq1	
J3.22	gpmc_ad9	kpd_row1	c2c_data14	gpio_33		
J3.23	gpmc_clk			gpio_55	sys_ndmareq2	
J3.24	gpmc_ad8	kpd_row0	c2c_data15	gpio_32		
J3.25	gpmc_nadv_ale	dsi1_te1		gpio_56	sys_ndmareq3	
J3.26	gpmc_ad7	sdmmc2_dat7	sdmmc2_clk_fdbk			
J3.27	gpmc_noe	sdmmc2_clk				
J3.28	gpmc_ad6	sdmmc2_dat6	sdmmc2_dir_cmd			
J3.29	gpmc_nwe	sdmmc2_cmd				
J3.30	gpmc_ad5	sdmmc2_dat5	sdmmc2_dir_dat1			
J3.31	gpmc_nbe0_cle	dsi2_te0		gpio_59		
J3.32	gpmc_ad4	sdmmc2_dat4	sdmmc2_dir_dat0			
J3.33	gpmc_ncs0			gpio_50	sys_ndmareq0	
J3.34	gpmc_ad3	sdmmc2_dat3				
J3.35	gpmc_a20	kpd_col4	c2c_datain4	gpio_44	venc_656_data4	
J3.36	gpmc_ad2	sdmmc2_dat2				
J3.37	gpmc_a21	kpd_col5	c2c_datain5	gpio_45	venc_656_data5	
J3.38	gpmc_ad1	sdmmc2_dat1				

Table 3-4 Connectors Pin Mux

4   Interface Details

4.1 Overview

This chapter describes in detail the DART-4460 interfaces, referring to the default SoM pin names. However, many additional interfaces are available when different pin modes are selected by the user. For example, the McSPI2 bus is available to the user when the McBSP2 pin mode is set to '1'. Tables 3 - 2 (Connectors Pin Mux) detail the additional possible options for each pin on the DART-4460 connectors.

The following list describes this chapter's column header tables:

Signal:
DART-4460 original pin name

Pin#:
Pin Number on the external connector

Type:
Pin Type & Direction:
- I – In
- O – Out
- DS – Differential Signal
- A – Analog
- Power – Power Pin

Description:
Short Pin functionality description

4.2 Display Interfaces

4.2.1 Overview

The DART-4460 provides the logic to display a video frame from the memory frame buffer on an LCD panel or a TV set
The primary LCD output:
- DSI1 (MIPI® DSI) – SXGA(1400x1050) VESA timing @ 60 FPS

The secondary LCD:
- Parallel RGB output (MIPI DPI 1.0) - SXGA (1400x1050) VESA timing @ 85 fps1080i/720p

HDMI interface:
High-Definition Multimedia Interface (using TV set out) - HD-1080p, HD-1080i, HD-720p, SD-480p, SD-576p, SD-576i, and SD-480i using HDMI

4.2.2   DPI (Display Parallel Interface)

4.2.2.1   DPI Features

Panel supported with MIPI DPI protocol:
- 4/8-bit monochrome passive matrix panel interface support (15 gray scale levels supported using dithering block)
- 8-bit color passive matrix panel interface support (3375 colors supported for a color panel using dithering block)
- 12/16/18/24-bit active matrix panel interface support

4.2.2.2   DPI Signals

Signal	Pin #	Type	Description
DISPC2_PCLK	J2.38	O	DPI Pixel Clock
DISPC2_HSYNC	J2.36	O	DPI Horizontal Sync
DISPC2_VSYNC	J2.33	O	DPI Vertical Sync
DISPC2_DE	J2.42	O	DPI Data Enable
DISPC2_DATA0	J2.44	O	DPI Data Line 0
DISPC2_DATA1	J2.46	O	DPI Data Line 1
DISPC2_DATA2	J2.14	O	DPI Data Line 2
DISPC2_DATA3	J2.09	O	DPI Data Line 3
DISPC2_DATA4	J2.16	O	DPI Data Line 4
DISPC2_DATA5	J2.11	O	DPI Data Line 5
DISPC2_DATA6	J2.18	O	DPI Data Line 6
DISPC2_DATA7	J2.13	O	DPI Data Line 7
DISPC2_DATA8	J2.40	O	DPI Data Line 8
DISPC2_DATA9	J2.28	O	DPI Data Line 9
DISPC2_DATA10	J2.22	O	DPI Data Line 10
DISPC2_DATA11	J2.17	O	DPI Data Line 11
DISPC2_DATA12	J2.24	O	DPI Data Line 12
DISPC2_DATA13	J2.19	O	DPI Data Line 13
DISPC2_DATA14	J2.26	O	DPI Data Line 14
DISPC2_DATA15	J2.21	O	DPI Data Line 15
DISPC2_DATA16	J2.31	O	DPI Data Line 16
DISPC2_DATA17	J2.23	O	DPI Data Line 17
DISPC2_DATA18	J2.30	O	DPI Data Line 18
DISPC2_DATA19	J2.25	O	DPI Data Line 19
DISPC2_DATA20	J2.32	O	DPI Data Line 20
DISPC2_DATA21	J2.27	O	DPI Data Line 21
DISPC2_DATA22	J2.34	O	DPI Data Line 22
DISPC2_DATA23	J2.29	O	DPI Data Line 23

Table 4-1 DPI Signals

4.2.3 DSI1Display Serial Interfaces

Signal	Pin #	Type	Description
DSI1_DX0	J2.1	DS	Serial data/clock lane
DSI1_DY0	J2.3	DS	Serial data/clock lane
DSI1_DX1	J2.4	DS	Serial data/clock lane
DSI1_DY1	J2.2	DS	Serial data/clock lane
DSI1_DX2	J2.5	DS	Serial data/clock lane
DSI1_DY2	J2.7	DS	Serial data/clock lane
DSI1_DX3	J2.8	DS	Serial data/clock lane
DSI1_DY3	J2.6	DS	Serial data/clock lane
DSI1_DX4	J2.12	DS	Serial data lane only
DSI1_DY4	J2.10	DS	Serial data lane only
DSI1_TE0	J2.9	I	DSI1 tearing effect (TE) input 0
DSI1_TE1	J2.11	I	DSI1 tearing effect (TE) input 1

Table 4-2 DPI Signals

4.2.4 HDMI

4.2.4.1 HDMI Features

Driven by the native OMPA4460 HDMI interface, the list below summarizes HDMI interface features:

- HDMI 1.3, HDCP 1.2, and DVI 1.0 compliant, including support for the 3D stereoscopic frame-packing formats of the HDMI v1.4 standard (720p, 50 Hz; 720p, 60 Hz; and 1080p, 24 Hz)
- EIA/CEA-861-D video format support (refer to Table 10 - 628 for more details)
- VESA DMT video format support (refer to Table 10 - 629 for more details)
- Support for deep-color mode:
  - 10-bit/component color depth up to 1080p @60 Hz
  - 12-bit/component color depth up to 720p/1080i @60 Hz
- Supports up to 148.5 MHz pixel clock (1920 x 1080p @60 Hz)
- Video formats: 24-bit RGB
- Uncompressed multi-channel (up to 8-channels) audio (L-PCM) support
- Master I2C interface for Display Data Channel (DDC) connection
- Consumer Electronic Control (CEC) interface
- Integrated High-bandwidth Digital Content Protection (HDCP) encryption engine for transmitting protected audio and video content (authentication performed by software)
- Integrated Transition Minimized Differential Signaling (TMDS) and TMDS Error Reduction Coding (TERC4) encoders for data island support
- Integrated TMDS PHY (3 TMDS differential data lanes + TMDS differential clock lane) – Up to 1,85625 Gbps per lane at (1080p @60 Hz at 10-bit/component, lower resolutions at 12-bit/component)

– 928,125Mbps per lane at (720p/1080i @60 Hz 10-bit/component, lower resolutions at 12-bit/component)

4.2.4.2 HDMI Signals

Signal	Pin #	Type	Description
HDMI_CLOCKX	J2.64	ODS	HDMI Clock Differential
HDMI_CLOCKY	J2.62	ODS	HDMI Clock Differential
HDMI_DATA0X	J2.61	ODS	HDMI Data 0 Differential
HDMI_DATA0Y	J2.59	ODS	HDMI Data 0 Differential
HDMI_DATA1X	J2.56	ODS	HDMI Data 1 Differential
HDMI_DATA1Y	J2.58	ODS	HDMI Data 1 Differential
HDMI_DATA2X	J2.67	ODS	HDMI Data 2 Differential
HDMI_DATA2Y	J2.69	ODS	HDMI Data 2 Differential
HDMI_DDC_SCL	J2.68	IO	Display Data Channel Clock
HDMI_DDC_SDA	J2.65	IO	Display Data Channel Data
HDMI_HPD	J2.60	I	Hot Plug Detect
HDMI_CEC	J2.66	IO	Consumer Electronic Control

Table 4-2 HDMI Signals

4.3 Camera Interfaces

The DART-4460 features three camera interfaces:

- 16-bit CPI (Camera Parallel Interface)
- 2 X CSI2 (Camera Serial Interface)

Note: The serial camera interface signals are muxed with camera parallel interface signals.

4.3.1 Camera Interface Features

CPI (Camera Parallel Interface):

- 16-bit wide
- Up to 148.5 MPix/s
- BT656 and SYNC mode (HS, VS, FIELD, WEN)

CSI (Camera Serial Interface):

CSI2 camera interfaces

- Transfer pixels and data received by the CSI2 digital physical layer receiver to the system memory or to the ISP
- Use unidirectional data link
- CSI2-A supports four configurable data links in addition to the clock signaling
- CSI2-B supports two configurable data links in addition to the clock signaling

- Maximum data rate of 1 Gbps per data lane
- Data merger for 2, 3, or 4-data lane configuration
- Maximum data rate of 1 Gbps per data lane, possible configurations are:
  - One data lane: 1000 Mbps (824 Mbps if lane 4 is used)
  - Two data lanes: 2 × 1000 Mbps (2 × 824 Mbps if lane 4 is used
  - Three data lanes: 3 × 1000 Mbps (3 × 824 Mbps if lane 4 is used)
  - Four data lanes: 4 × 824 Mbps
- Error detection and correction by the protocol engine
- Direct Memory Access (DMA) engine integrated with dedicated First In First Out (FIFO)
- 1-Dimensional (1D) and 2-Dimensional (2D) addressing mode
- Burst support
- Streaming burst support (64 or 32-bit)
- Eight contexts to support eight dedicated configurations of virtual channel ID and data types
- Ping-pong mechanism for double-buffering
- All primary and secondary MIPI-defined formats are supported
- Conversion of the RGB formats
- On-the-fly differential pulse code modulation (DPCM) decompression
- On-the-fly image cropping and A-law/DPCM compression

CCP2 camera interface (secondary)

- Four logical channels
- Transfer pixels and data received by the complex I/O PHY (CCP2 D-PHY RX to the system memory or the ISP)
- Use unidirectional data link
- Maximum data rate of 650 Mbps
- DMA engine integrated with dedicated FIFO
- 1D and 2D addressing mode
- False synchronization code protection
- Ping-pong mechanism for double-buffering
- RGB, RAW, YUV, and JPEG formats supported
- On-the-fly DPCM decompression
- On-the-fly image cropping and A-Law/DPCM compression

4.3.2 CPI Signals

Signal	Pin #	Type	Description
CAM2 _PCLK	J3.11	I	Parallel Interface Pixel Clock
CAM2 _HS	J3.7	IO	Line Trigger Input/output Signal
CAM2 _VS	J3.9	IO	Frame Trigger Input/output Signal
CAM2 _FLD	J1.68	IO	Field Identification Input/output Signal
CAM2 _WEN	J1.70	I	External Write-enable Signal

CAM _STROBE	J1.33	O	Flash Strobe Control Signal
CAM2_D0	J3.2	I	ISP Data (LSB)
CAM2 _D1	J3.4	I	ISP Data
CAM2 _D2	J3.6	I	ISP Data
CAM2 _D3	J3.5	I	ISP Data
CAM2 _D4	J1.42	I	ISP Data
CAM2 _D5	J1.59	I	ISP Data
CAM2 _D6	J1.55	I	ISP Data
CAM2 _D7	J1.53	I	ISP Data
CAM2 _D8	J3.3	I	ISP Data
CAM2 _D9	J3.8	I	ISP Data
CAM2 _D10	J3.1	I	ISP Data
CAM2 _D11	J1.40	I	ISP Data
CAM2 _D12	J1.67	I	ISP Data
CAM2 _D13	J1.69	I	ISP Data
CAM2 _D14	J1.63	I	ISP Data
CAM2 _D15	J1.65	I	ISP Data (MSB)

Table 4-3 CPI Signals

4.3.3   CSI21 Signals

Signal	Pin #	Type	Description
CSI21_DX0	J1.54	IDS	CSI2 (CSI21) Camera Lane 0 differential x
CSI21_DY0	J1.56	IDS	CSI2 (CSI21) Camera Lane 0 Differential Y
CSI21_DX1	J1.64	IDS	CSI2 (CSI21) Camera Lane 1 Differential X
CSI21_DY1	J1.66	IDS	CSI2 (CSI21) Camera Lane 1 Differential Y
CSI21_DX2	J1.60	IDS	CSI2 (CSI21) Camera Lane 2 Differential X
CSI21_DY2	J1.62	IDS	CSI2 (CSI21) Camera Lane 2 Differential Y
CSI21_DX3	J1.53	IDS	CSI2 (CSI21) Camera Lane 3 Differential X
CSI21_DY3	J1.55	IDS	CSI2 (CSI21) Camera Lane 3Differential Y
CSI21_DX4	J1.59	IDS	CSI2 (CSI21) Camera Lane 4 Differential X
CSI21_DY4	J1.61	IDS	CSI2 (CSI21) Camera Lane 4 Differential Y

Table 4-4 CSI21 Signals

4.3.4   CSI22 Signals

Signal	Pin #	Type	Description
CSI22_DX0	J1.67	IDS	CSI2 (CSI22) Camera Lane 0 Differential X
CSI22_DY0	J1.69	IDS	CSI2 (CSI22) Camera Lane 0 Differential Y
CSI22_DX1	J1.63	IDS	CSI2 (CSI22) Camera Lane 1 Differential X
CSI22_DY1	J1.65	IDS	CSI2 (CSI22) Camera Lane 1 Differential Y
CSI22_DX2	J1.68	IDS	CSI2 (CSI22) Camera Lane 2 Differential X
CSI22_DY2	J1.70	IDS	CSI2 (CSI22) Camera Lane 2 Differential Y

Table 4-5 CSI22 Signals

4.4 Wi-Fi & Bluetooth

Wi-Fi & Bluetooth connectivity is supported by on board Murata LBEH59XUHC, a IEEE802.11 b/g/n + Bluetooth 4.0 module based on TI's WL1271L chipset.

J4 is a U.FL connector for an external antenna connection, serves both Wi-Fi & Bluetooth modules.

4.5 USB HOST 2.0

4.5.1   USB Host Signals

Signal	Pin #	Type	Description
USBHOST_DP	J1.6	IODS	USB Host Data Positive
USBHOST_DN	J1.4	IODS	USB Host Data Negative
USBHOST_VBUS	J1.20	I	USB Host VBUS indicator (5V)

Table 4-6 USB HOST Signals

4.6 USB 2.0 On-The-Go

4.6.1   USB 2.0 On-The-Go Features

The OMAP4460 High-Speed USB controller is a high-speed, USB OTG dual-role-device (DRD) link controller supporting the following modes:

- USB 2.0 peripheral (function controller) in high/full speed (480/12 Mbps, respectively)
- USB 2.0 host in high/full/low speed (480/12/1.5 Mbps, respectively), with one downstream port but multipoint capability when a hub is connected to it (split transaction support etc.)
- USB 2.0 OTG DRD in high/full speed, with HNP (OTG1.3) and SRP support

4.6.2   OTG Signals

Signal	Pin #	Type	Description
USB_OTG_DN	J1.26	IODS	USB OTG Data Negative
USB_OTG_DP	J1.24	IODS	USB OTG Data Positive
USB_OTG_VBUS	J1.22	I	USB 2.0 OTG VBUS indicator (5V)
USB_OTG_ID	J1.28	I	USB OTG Host/Client ID Low : Host Mode Float: Client Mode

Table 4-7 USB OTG Signals

Note: In host mode, an external regulator is required to supply the USB bus voltage to the connected device(s).

4.7 MMC/SD/SDIO

Two MMC interfaces are supported.

1. MMC/SD/SDIO1 3.0v compatible
   MMC1 can be used for external SD-Card boot
2. MMC/SD/SDIO2 1.8v compatible. MMC/SD/SDIO2 is only available if on-board eMMC is not used.

4.7.1 MMC/SD/SDIO Features

Compliance with standards:

- Full compliance with MMC/eMMC command/response sets as defined in the JC64 MC/eMMC Standard Specification v4.41, including high-capacity (size 2 GB) cards HC MMC
- Full compliance with SD command/response sets as defined in the SD Specifications Part 1 Physical Layer Simplified Specification v3.01, including high-capacity SDHC cards up to 32 GB
- Full compliance with SDIO command/response sets and interrupt/read-wait suspend-resume operations, as defined in the SDIO Card Specification Part E1, v2.00
- Full compliance with sets as defined in the SD Card Specification Part A2, SD Host Controller Standard Specification v2.00
- Full compliance with MMC bus testing procedure as defined in the Multimedia Card System Specification v4.41
- Full compliance with CE-ATA command/response sets as defined in the CE-ATA Standard Specification
- Full compliance with ATA for MMCA specification
- Support command completion signal (CCS) and command completion signal disable (CCSD) management as specified in the CE-ATA Standard Specification

Main features of the MMC/SD/SDIO host controller:

- Flexible architecture allowing support for a new command structure
- Support:
  - 1 or 4-bit transfer mode specifications for SD and SDIO cards
  - 1, 4, or 8-bit transfer mode specifications for MMC cards
- Built-in buffer for read or write (up to 2048 bytes in single-buffering, 1024 bytes in double-buffering)
- 32-bit wide access bus to maximize bus throughput
- Single interrupt line for interrupt source events
- Two slave DMA channels (one for TX, one for RX)
- Designed for low power
- Programmable clock generation
- Support SDIO read wait and suspend/resume functions
- Support stop at block gap

- Support boot mode operations as specified in the JEDEC JC 64 MMC/eMMC Standard Specification v4.41
- Support Dual Data Rate transfers (DDR mode) as specified in JEDEC JC64 MMC/eMMC Standard Specification v4.41
- Support SDA 2.0 Part A2 programming model optional features (depending on module integration):
    - Master interface (Level 3 [L3] interconnect)
    - One master DMA (32-bit ADMA2), replacing the two slave DMA channels
- Retention mode is supported
- Supported clock frequencies:

    MMC mode:
    - Up to 48 MHz in DDR and SDR modes

    SD mode:
    - Up to 48 MHz in DDR mode
    - Up to 96 MHz in SDR mode

    SDIO mode:
    - Up to 48 MHz in SDR mode

4.7.2   SDMMC1 Signals

Signal	Pin #	Type	Description
MMC1_DAT0	J2.48	IO	MMC2 Data
MMC1_DAT1	J2.50	IO	MMC2 Data
MMC1_DAT2	J2.52	IO	MMC2 Data
MMC1_DAT3	J2.54	IO	MMC2 Data
MMC1_CLKO	J2.39	O	MMC Clock
MMC1_CMD	J2.37	O	MMC Command

Table 4-8 SDMMC1 Signals

4.8 Audio

The DART-4460 features four audio interfaces

- Stereo line in
- Stereo Headphones driver
- Digital microphone
- S/PDIF out

4.8.1 Audio Features

4.8.1.1 Analog

Analog audio signals are featured by an on-board TWL6041 audio codec device. Please refer to the TWL6041 data sheet for detailed electrical characteristics of relevant interfaces.

http://www.ti.com/lit/ds/symlink/TWL6041.pdf

4.8.1.2 Digital Microphone

- Microphone is directly connected to the TX filter decimator to extract the audio samples with a maximum of 96 db SNR at a frequency sampling set to 96 kHz.
- Supports idle request/acknowledge protocol
- Rising or falling edge configuration for the clock signal sampling
- DMIC-clock-programmable
- Interconnect slave interface (internal interconnect) supports 32-bit data bus width.
- One DMA request capability on a programmable FIFO threshold
- One RX FIFO (16-bit x 24-bit word depth)
- Complies with PRCM interrupts to the Cortex-A9 MPU and DSP subsystems
- Interconnect sample format: 32-bits (only 24 are significant)
- Supports idle request/acknowledge PRCM protocol

4.8.1.3 S/PDIF

- Support of the idle request/acknowledge protocol
- Buffer for transmit operations
- One transmit Direct Memory Access (DMA) request linked with a 32-bit register and one transmit interrupt request
- One transmit channel
- One serializer

4.8.1.4 Audio Signals

Signal	Pin #	Type	Description
AUD_GND	J2.57	P	Audio GND

Signal	Pin #	Type	Description
AUD_IN_L	J2.49	AI	Audio Line In Left
AUD_IN_R	J2.51	AI	Audio Line In Right
AUD_OUT_L	J2.55	AO	Headphone Out Left
AUD_OUT_R	J2.53	AO	Headphone Out Right

Table 4-9 Audio Signals

4.9 UART Interfaces

By default three UART interfaces are supported, refer to Table 3.2 for further configuration options for the UART interface.

4.9.1 UART Features

Main features of DART-4460 UARTS:

- 16C750 compatibility
- 64-byte FIFO buffer for receiver and 64-byte FIFO for transmitter
- Programmable baud rate generator up to 3.6 Mbits
- Programmable interrupt trigger levels for FIFOs
- Break character detection and generation
- Configurable data format:
    - Data bits: 5, 6, 7, or 8-bits
    - Parity bit: Even, odd, none
    - Stop-bit: 1, 1.5, 2-bit(s)
- Flow control: Hardware (RTS/CTS) or software (XON/XOFF)

Receive and transmit FIFO fill and drain operations can be done using programmed IO or DMA transfers. To minimize CPU overhead for UART communications, device driver software can setup interrupts and DMA for data transfers to/from memory.

4.9.2 UART1 Signals

Signal	Pin #	Type	Description
UART1_TX	J2.47	O	UART Transmit
UART1_RX	J2.41	I	UART Receive
UART1_RTS	J2.43	O	UART HW Flow Control RTS
UART1_CTS	J2.45	I	UART HW Flow Control CTS

Table 4-10 UART1 Signals

4.9.3 UART2 Signals

Signal	Pin #	Type	Description
UART2_TX	J1.34	O	UART Transmit
UART2_RX	J1.32	I	UART Receive
UART2_RTS	J1.36	O	UART HW Flow Control RTS
UART2_CTS	J1.38	I	UART HW Flow Control CTS

Table 4-11 UART2 Signals

Note: UART2 Signals are shared with an on board Bluetooth connectivity device.

4.9.4 UART3 Signals

Signal	Pin #	Type	Description
UART3_TX	J1.33	O	UART Transmit
UART3_RX	J1.31	I	UART Receive

UART3_RTS	J1.29	O	UART HW Flow Control RTS
UART3_CTS	J1.27	I	UART HW Flow Control CTS

Table 4-12 UART3 Signals

Note: UART3 is used as default boot debug port.

4.10 Multi-channel Buffered Serial Ports

The Multi-channel Buffered Serial Ports (McBSP) provide a full-duplex direct serial interface between the device and other devices in a system such as audio and voice codecs. DART-4460 supports McBSP in a 4-pin configuration (CLKR and FSR are connected internally to CLKX and FSX respectively). McBSP2 interface is supported, refer to MCBSP2 signals' table for further information.

4.10.1 McBSP Features

The main features of the McBSP modules are:
- L4 interconnect slave interface supports:
  - 32-bit data bus width
  - 32-bit access supported
  - 16/8-bit access not supported
  - 10-bit address bus width
  - Burst mode not supported
  - Write non-posted transaction mode supported
- 128 × 32-bit words (512 bytes) for each buffer for transmit/receive operations
- Transmit and receive Direct Memory Access (DMA) requests triggered with programmable FIFO thresholds
- Serial interface description
  - 6-pin configuration (McBSP 4 only)
  - 4-pin configuration (McBSP1, 2, 3)
  - Full-duplex communication
  - Multichannel selection modes
- Support to enable or block transfers in each channel
- 128 channels for transmission and reception
  - Direct interface to industry-standard codecs, Analog Interface Chips (AICs), and other serially
- Connected A/D and D/A devices:
  - Inter-IC sound (I2S™) compliant devices
  - Pulse Code Modulation (PCM) devices
  - Time Division Multiplexed (TDM) bus devices
  - A wide selection of data sizes: 8, 12, 16, 20, 24, and 32 bits
  - Bit reordering (send/receive Least Significant Bit [LSB])
- Clock and frame-synchronization generation support:
  - Independent clocking/framing for reception and transmission up to 48 MHz
  - Support for external generation of clock signals and frame-synchronization (frame-sync) signals
  - A programmable Sample Rate Generator (SRG) for internal generation and control of clock signals and frame-sync signals
  - Programmable polarity for frame-sync pulses and clock signals

4.10.2 McBSP2 Signals

Signal	Pin #	Type	Description
McBSP2_CLKX	J1.21	IO	McBSP Transmit Clock
McBSP2_FSX	J1.15	IO	McBSP Transmit Frame Synchronization
McBSP2_DR	J1.19	I	McBSP Receive Serial Data
McBSP2_DX	J1.17	(I)O	McBSP Transmit Serial Data

Table 4-13 McBSP2 Signals

4.11 SPI

The DART-4460 SPI is based on OMAP4 McSPI x. By default one McSPI (McSPI1) interface is supported. Refer to Table 3.2 for further McSPI interfaces configuration options.

4.11.1 SPI Features

The SPI interface includes the following main features:
- Serial clock with programmable frequency, polarity, and phase for each channel
- Wide selection of SPI word lengths, ranging from 4 to 32-bits
- Up to four master channels, or a single channel in slave mode
- Master multichannel mode:
  - Full duplex/half duplex
  - Transmit-only/receive-only/transmit-and-receive modes
  - Flexible I/O port controls per channel
  - Two DMA requests (read/write) per channel
- Single interrupt line for multiple interrupt source events
- Power management through wake-up capabilities
- Enable the addition of a programmable start-bit for SPI transfer per channel (start-bit mode)
- Supports start-bit write command
- Supports start-bit pause and break sequence
- 64-byte built-in FIFO available for a single channel
- Force CS mode for continuous transfers

4.11.2 McSPI1 Signals

Signal	Pin #	Type	Description
McSPI1_CLK	J1.37	IO	MsSPI1 Clock
McSPI1_SIMO	J1.39	IO	MsSPI1 SIMO Signal
McSPI1_SOMI	J1.41	IO	MsSPI1 MISO Signal
McSPI1_CS0	J1.35	IO	MsSPI1 Chip Select 0 Signal

Table 4-14 SPI Signals

4.12 I²C

By default, two I²C (I2C3, I2C4) interfaces are supported, driven by the OMAP4460 controller. Refer to Table 3.2 for further configuration options for I²C interfaces.

4.12.1 I²C Features

OMAP4 I²C controller main features are:

- Compliant with Philips I²C specification version 3.0
- Supports standard mode (up to 100 Kbps), fast mode (up to 400 Kbps), and fast mode+ (up to 1 Mbps)
- Supports HS mode for transfer up to 3.4 Mbps
- Support for 3-wire/2-wire SCCB master mode for I2C2 and I2C3 modules, 2-wire SCCB master mode for I2C1 and I2C4 modules, up to 100 Kbps
- 7-bit and 10-bit device addressing modes
- General call
- Start/restart/stop
- Multi-master transmitter/slave receiver mode
- Multi-master receiver/slave transmitter mode
- Combined master transmit/receive and receive/transmit mode
- Built-in configurable FIFO (8, 16, 32, 64-bytes) for buffered read or write
- Module enable/disable capability
- Programmable multi-slave channel (responds to four separate addresses)
- Programmable clock generation
- 8-bit-wide data access
- Open-core protocol (OCP) interface with LH application (OCP-IP 2.0 compliant)
- Designed for low power consumption
- Implement auto idle mechanism
- Implement idle Request/idle acknowledge handshake mechanism
- Support for asynchronous wake-up mechanism
- Two Direct Memory Access (DMA) channels
- Wide interrupt capability
- Supports OmniVision SCCB protocol
- Compliant with Highlander 0.8

The master transmitter HS I2C controller I2C5 has the following features:

- Support of HS and fast modes
- 7-bit addressing mode only
- Master transmitter mode only
- Start/restart/stop

4.12.2 I2C3 Signals

Signal	Pin #	Type	Description
I2C3_SCL	J1.13	IO	I2C3 I^{2}C Clock , Open Drain
I2C3_SDA	J1.11	IO	I2C3 I^{2}C Data, Open Drain

Table 4-15 I2C3 Signals

4.12.3 I2C4 Signals

Signal	Pin #	Type	Description
I2C4_SCL	J1.2	IO	I2C4 I^{2}C Clock, Open Drain
I2C4_SDA	J1.1	IO	I2C4 I^{2}C Data, Open Drain

Table 4-16 I2C4 Signals

4.12.4 On-SOM I2C devices

I2C4 – 0x48: Temperature sensor
I2C4 – 0x50: EEPROM – Unique SOM ID.

4.13 HDQ/1-Wire

The HDQ/1-Wire module implements the hardware protocol of the master functions of the Benchmark HDQ and Dallas Semiconductor 1-Wire® protocols. These protocols use a single wire for communication between the master (HDQ/1-Wire controller) and the slave (HDQ/1-Wire external compliant device).
A typical application of the HDQ/1-Wire is the communication with battery monitor (gas gauge) integrated circuits.

4.13.1 1-Wire / HDQ Feature

The HDQ/1-Wire provides a communication rate of 5 Kbps over an address space of 128 bytes.

4.13.2 1-Wire / HDQ Signal

Signal	Pin #	Type	Description
HDQ	J1.45	IO	HDQ / 1-Wire IO Signal

Table 4-17 HDQ Signal

4.14 PWM

By default, one PWM interface is supported, driven by the OMAP4460 controller, refer to Table 3.2 for further configuration options for PWM (under "DMTIMERX_PWM_EVT" functions).

4.14.1 PWM0 Signal

Signal	Pin #	Type	Description

Signal	Pin #	Type	Description
PWM0	J1.46	O	PWM Signal (mux mode 5)

Table 4-18 PWM0 Signal

4.14.2 TWL6030 PMIC PWM2 Signal

5 Signal	Pin #	Type	Description
TWL6030 PMIC PWM2	J1.57	O	PWM Signal

Table 4-19 PWM0 Signal

5.1 Local Bus

The General Purpose Memory Controller (GPMC) is used to interface external memory devices:
- SRAMs
- Asynchronous, synchronous, and page mode (only available in non-muxed mode) burst NOR flash devices
- NAND flashes
- Pseudo-SRAM devices

Most of OMAP4 local bus (GPMC) signals are available through DART-4460 40 pin FPC connector described above in the "SoM Connectors" section 3, Table 3.3.

5.2 Keypad

DART-4460 keypad interface is based on the OMAP4 keypad controller, not every OMAP4 keypad IO is supported by DART-4460. See the table below for more details.

5.2.1 Keypad Controller Features

The keyboard controller includes the following main features:

- Support of multi-configuration keyboards up to 3 rows × 6 columns
- Each key coded on 1-bit in two 32-bit registers
- Long-key value or repeat timing reconfigurable on-the-fly
- Event detection on key press and key release
- Multi-key-press detection and decoding
- Long-key detection on prolonged key press
- Integrated timer with four programmable comparison values
- Programmable time-out on permanent key press or after keyboard release
- Programmable interrupt generation on key events
- Software reset capability

The keyboard controller detects and decodes multi-key combinations using the following rules:

- Any 2-key combination is valid and can be decoded

- Combinations using more than two keys are valid only if the rows and columns used do not cross over another key that is to be detected. This is caused by equipotent propagation on a row/column (multi-key limitations).

5.2.2 Keypad Controller Signals

Signal	Pin #	Type	Description
KPD_ROW0	J3.33	I	Keypad Row
KPD_ROW1	J3.8	I	Keypad Row
KPD_ROW2	J1.40	I	Keypad Row
KPD_ROW3	J1.42	I	Keypad Row
KPD_COL0	J3.5	O	Keypad Column
KPD_COL1	J3.3	O	Keypad Column
KPD_COL2	J3.1	O	Keypad Column
KPD_COL3	J3.2	O	Keypad Column
KPD_COL4	J3.4	O	Keypad Column
KPD_COL5	J3.6	O	Keypad Column

Table 4-20 Keypad Signals

5.3 General Purpose IOs

Most of the SoM's IO pins can be used as GPIOs.
See Chapter 3, Table 3.2 and 3.4 for a complete SoM connectors signal list and GPIO multiplexing.

5.4 General System Control

5.4.1 Boot Options

The boot option signal (syb_boot1) configures the boot sequence of the DART-4460:
Logic '0' (Not Connected) : Boot device is an on-SOM eMMC via MMC/SD/SDIO2 interface.
Logic '1': boot device is an on-carrier board (using MMC/SD/SDIO1 interface), if failed, UART is used as a boot device.

5.4.2 Reset

'0' logic will reset major DART-4460 components:

- OMAP44660
- TWL6032 - PMIC
- TWL6041 – Audio Codec

5.4.3 Reference Clock Out

An OMAP4 output clock is controlled by the SCRM module. Please contact Variscite for further information regarding the configuration option for this clock.

5.4.4 General System Control Signals

Signal	Pin #	Type	Description
SYS_BOOT0	J1.8	I	System Boot Option Select (internally pulled down) [Low – Internal Device Boot] [High – MMC1 SD card]
RESET_IN	J1.5	I	Hardware Reset
FREF_CLK1_OUT	J1.51	O	General Purpose Clock Out

Table 4-21 General System Signals

5.5 JTAG

Jtag signals are available as tests points on DART-4460, and are marked with Silk
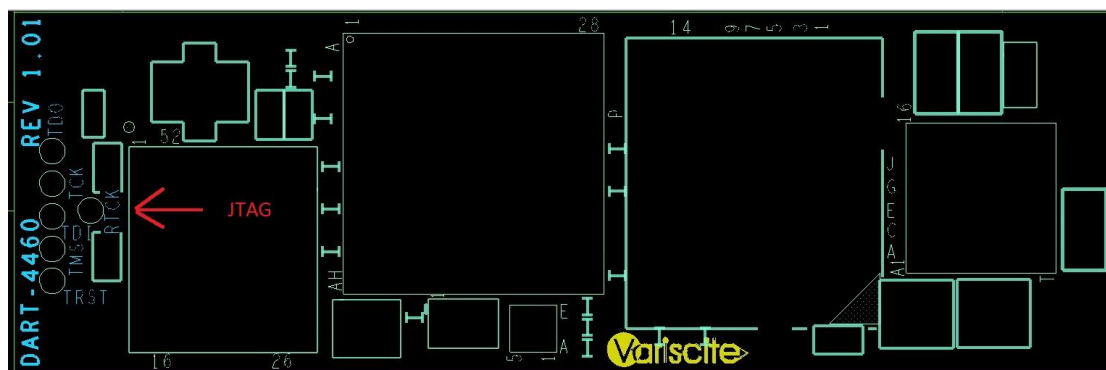
5.6 Power

Power Supply pins:

Signal	Pin #	Type	Description
VBAT_SOM	J1.10 J1.12 J1.14 J1.16	Power In	DART-4460 Single DC-IN Supply Voltage.
VIO	J1.3	Power Out	1.8V Output, up to 200 mA
RTC_BACKUP	J1.7	Power In	RTC Backup Battery Power Supply, Max : 8uA@ RTC_BACKUP = 3.2V ,VBAT =0,
VPMIC_VAUX1_2V8	J1.43	Power Out	2.8V Output, up to 100 mA

Table 4-22 Power Supply Pins

GND:

Signal	Pin #	Type	Description
GND	J1.9 J1.18 J1.25 J1.30 J1.47 J1.48 J1.58 J2.15 J2.20 J2.35 J2.63 J2.70		Digital Ground

Signal	Pin #	Type	Description
	J3.10 J3.13 J3.39 J3.40		
AGND	J2.57	Power	Analog GND

Table 4-23 Ground Pins

6 Absolute Maximum Characteristics

Power Supply	Min	Max	Unit
Main Power Supply, DC-IN	-0.3	4.5	V

Table 6-1 Absolute Maximum Characteristics

7 Operational Characteristics

7.1 Power supplies

	Min	Typical	Max	Unit
Main Power Supply, DC-IN	3.3	3.7	4.2	V
RTC Backup Battery Voltage	2.5	3.8	5.5	V

Table 7-1 Power Supplies Operational Characteristics

7.2 Power Consumption

The below tables summarizes the DART-4460 power consumption at various operational modes.

Power Consumption at various CPU utilization modes (@25°C)

Cores utilization [1]	CPU Cores Frequency [GHz]	Power [W]
Suspend	-	17mW(5ma)
Core 1 - <15% **Core 2 - <15%**	0.35	150mw
	0.92	0.8W
	1.2	0.9W
Core 1 - 100% **Core 2 - < 15%**	0.35	1.26
	0.92	2.05
	1.2	2.38
	1.5	2.66

Table 7-2-1 Power Consumption at various CPU utilization modes, 25°C

[1] 100%: CPU at full usage, running Dhrystone benchmark

8 DC Electrical Characteristics

Parameter	Min	Typical	Max	Unit
DIGITAL 1.8V IO [GPMC, DISPC,DSI,CSI, MMCx,HDQ, McBSP, HDMI_x, PDM,DMIC,SPI,UART,JTAG ,Keypad, GPIO_13, Reset]				
V_{IH}	1.17		2.1	V
V_{IL}	-0.3		0.63	V
V_{OH}	1.35			V
V_{OL}			0.45	V
I2C				
V_{IH}	1.26		2.3	V
V_{IL}	-0.5		0.54	V
V_{OH}	1.35			V
V_{OL}			0.45	V
USBHOSTx_PWORCTRL (Open Drain)				
V_{IH}	2		4.5	V
V_{IL}			0.8	V
OTG_VBUS				
Detect	2.93		3.15	V

Table 8-1 DC Electrical Characteristics

9 Environmental Specifications

|	Min	Max
Commercial Operating Temperature Range	0 ^{0}C	+70 ^{0}C
Extended Operating Temperature Range	-25 ^{0}C	+70 ^{0}C
Industrial Operating Temperature Range	-35 ^{0}C	+85 ^{0}C
Referring MIL-HDBK-217F-2 Parts Count Reliability Prediction Method Model: 50Deg Celsius, Class B-1, GM 50Deg Celsius, Class B-1, GB	121 Khrs > 1400 Khrs >	
Shock Resistance	50G/20 ms	
Vibration	20G/0 - 600 Hz	

Notes:

1. Extended and Industrial Temperature range is only based on the operating temperature grade of the SoM components. Customer should consider specific thermal design for the final product based upon the specific environmental and operational conditions.

2. WiFi/BT module is limited to -20 ^{0}C to 70 ^{0}C

3. The minimal temperature of -35 ^{0}C in Industrial grade is due to the board-to-board connector operating temperature definition; all other components support -40 ^{0}C

10 Mechanical Drawings

Board is 52x17mm

Top View [mm]
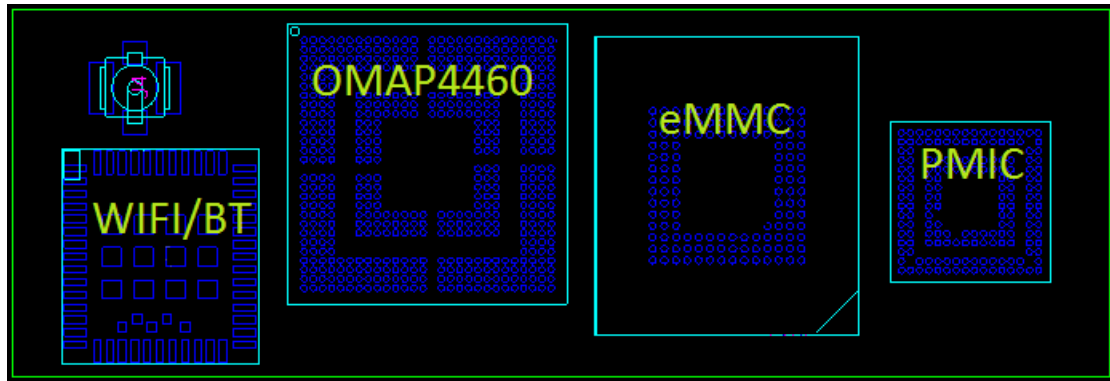
CAD file are available for download at http://www.variscite.com/

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