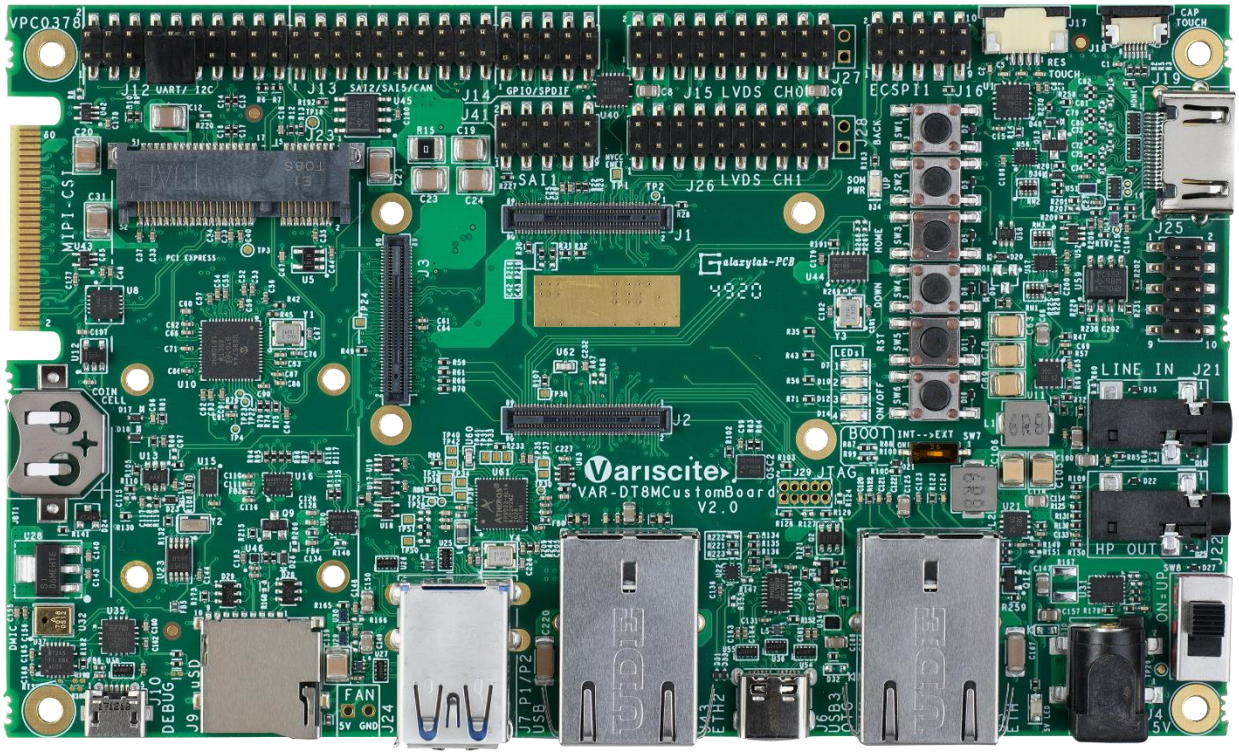
VARISCITE LTD

VAR-DT8MCustomBoard V3.x Datasheet

Carrier-board for the DART-MX8M, DART-MX8M-MINI and DART-MX8M-PLUS



VARISCITE LTD.

VAR-DT8MCustomBoard Datasheet

Variscite Ltd.
4, Hamelacha Street
Lod
P.O.B 1121
Airport City, 70100
ISRAEL

Tel: +972 (9) 9562910
Fax: +972 (9) 9589477

1 Revision History

Revision	Date	Notes
1.00	Feb 01, 2021	Initial – Preliminary
1.01	Jun 24, 2021	Updated Table 2-12 Assy column
1.02	Nov 04, 2021	Corrected Table 5-12 pins 24,26
1.03	Apr 11, 2022	Added VAR-DT8CustomBoard v3.0 changes: Modified mechanical drawing section 4.6 Updated Ethernet section 5.3.5 Updated RTC IC P/N sections 4.2, 5.4.3.4 Updated SW8 section 5.4.2.2
1.04	Mar 14, 2023	Corrected BD section 4.5 – PCIe modified to Gen 3.0

2 Table of Contents

3 List of Tables

4 Overview

This chapter provides an overview of the VAR-DT8MCustomBoard.

4.1 General Information

VAR-DT8MCustomBoard is a complete development board, utilizing all of the DART-MX8M, DART-MX8M-MINI and DART-MX8M-PLUS System-on-Modules features. It is assembled with large variety of user and debug interfaces enabling it to serve as both a complete development kit or a stand-alone end-product.

4.1.1 Supported Variscite products

- DART-MX8M
- DART-MX8M-MINI
- DART-MX8M-PLUS
- 7” Capacitive touch LCD

4.1.2 Supporting O.S

- Linux
- Android

4.1.3 Additional information

Board schematics as well as mechanical CAD database is available for download at www.variscite.com,

SW support information can be found: http://variwiki.com/

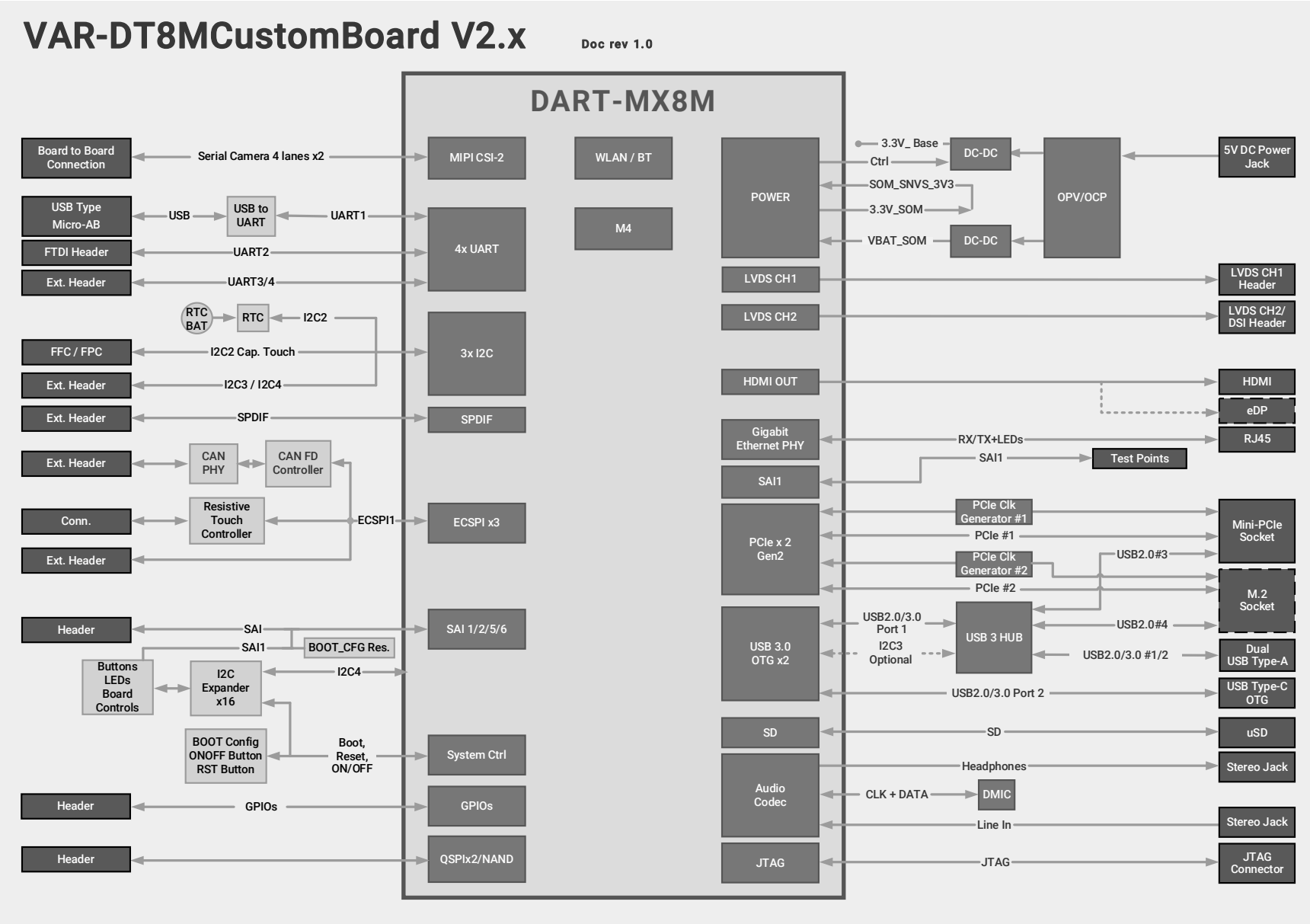
For more information contact Variscite support at mailto:support@variscite.com.

4.2 VAR-DT8MCustomBoard features summary

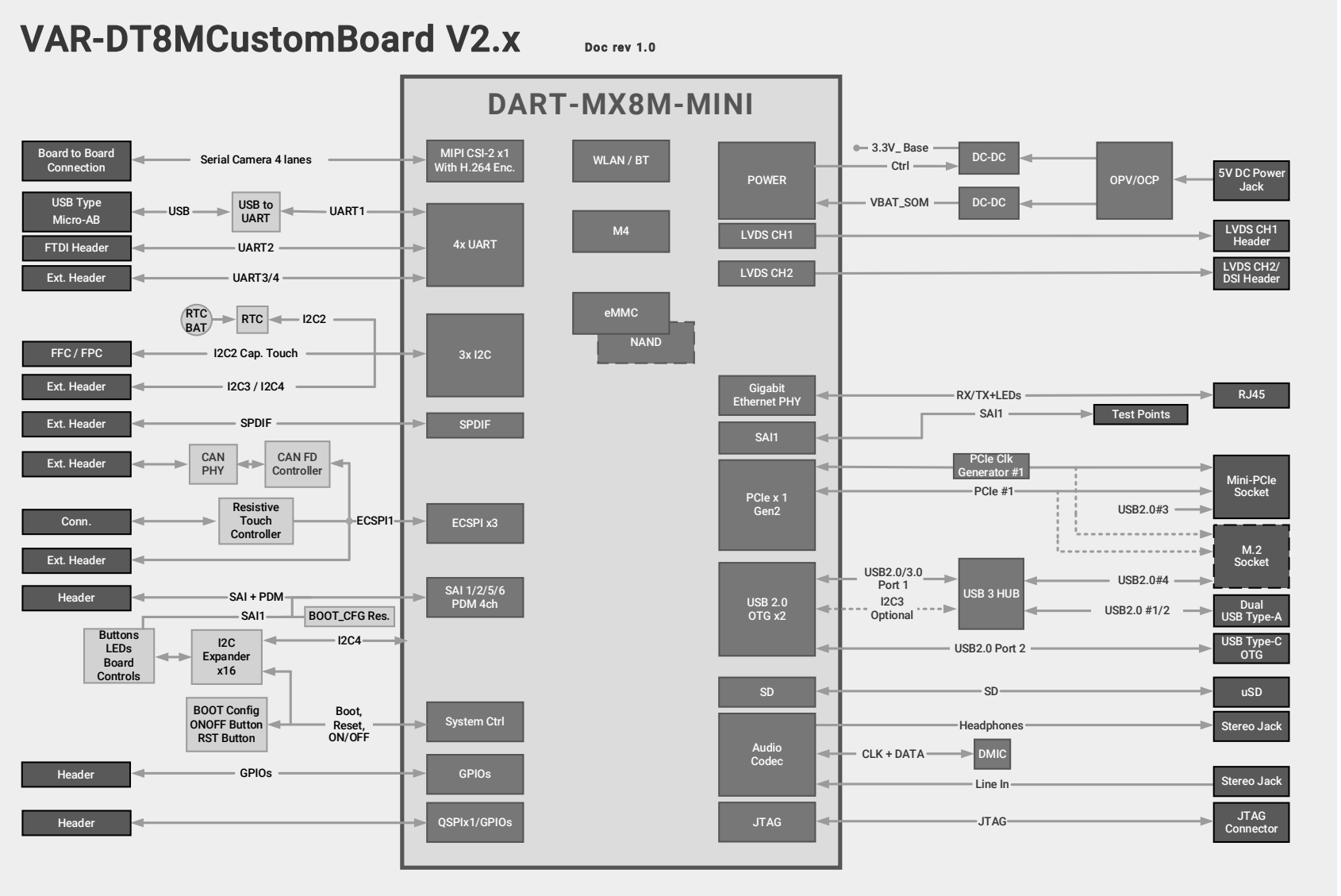
- 3 x 90 pin high density connectors, compatible with the DART-MX8M
- Display
  - 18 bit LVDS Interface supporting Variscite's 7" TFT capacitive touch LCD
  - HDMI 2.0a
  - eDP Port 1.4 (not assembled)
  - DSI
- Touch panel interface
  - Capacitive - I2C based
  - Resistive – SPI based
- Ethernet
  - 2 x 10/100/1000BaseT – RJ45
- PCIe
  - Mini PCIe
  - M.2 (Not assembled)
- USB
  - USB3.0 OTG Type C
  - USB3.0 Host Type A x 2
- AUDIO
  - 3.5mm Headphones jack
  - 3.5mm Line in jack
  - Digital Microphone
- µSD-Card slot
- Camera
  - Serial interface – Dual MIPI CSI x4 lanes each.
- Debug
  - USB debug (UART1) - Type Micro AB
  - JTAG – Header
- RTC
  - DS1337U+ Chip
- Additional
  - SAI (Serial Audio Interface) – Headers, Test Points
  - UART, QSPI, ECSPI, I2C, GPIO's – Headers
  - CAN Bus - SPI based controller with 5Mb/s or 12Mb/s CAN PHY – Header
    DT8M-PLUS only – 2nd 5Mb/s or 12Mb/s CAN PHY - Header
  - General purpose LEDs, Buttons

- Power
    - 5V DC Input. - 2.0mm DC jack / 2 pin Terminal Block
    - 5V DC Out – 2 pin Header
    - RTC Backup battery - CR1225 Battery Holder

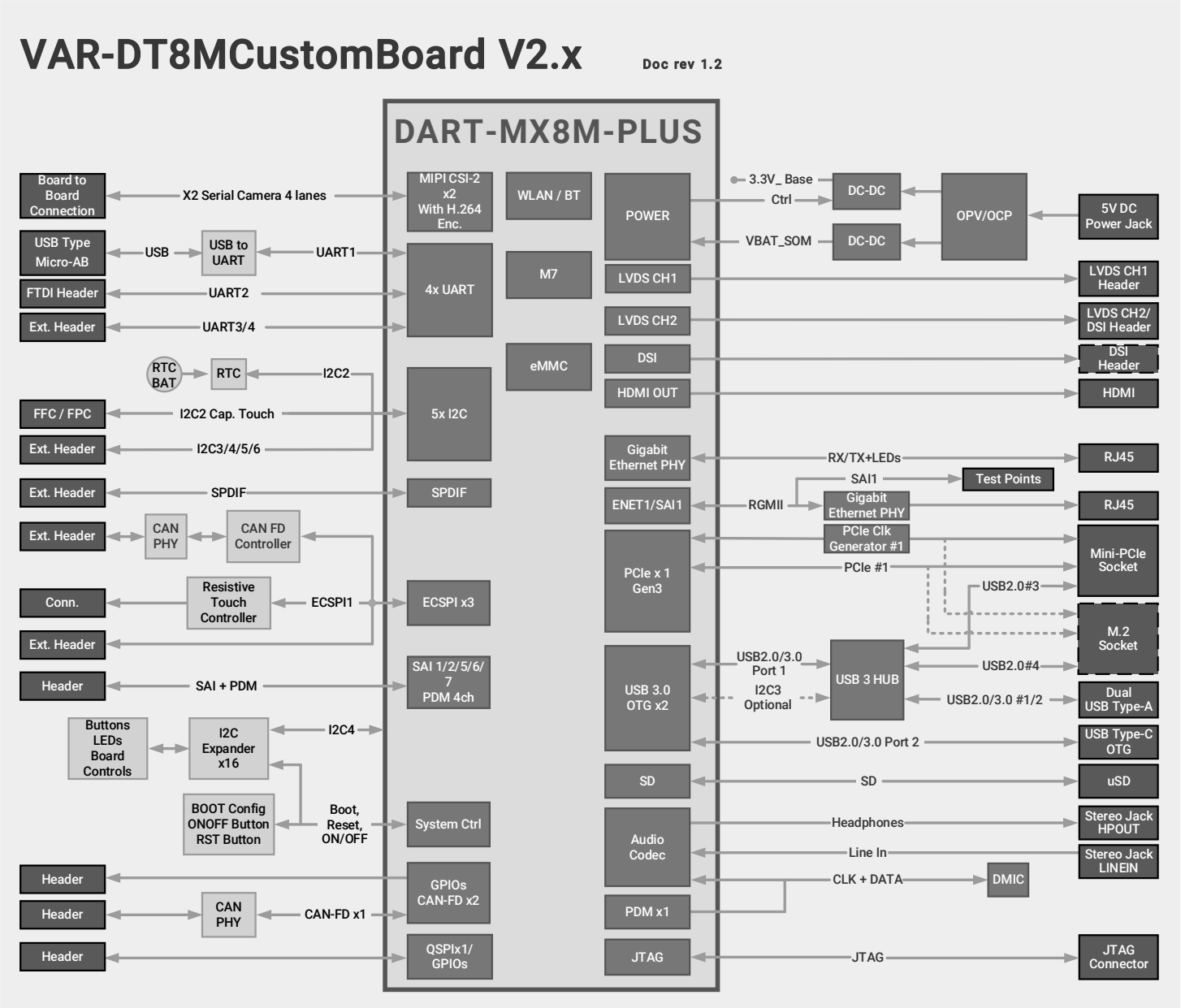
4.3 Block Diagram with DART-MX8M



4.4 Block Diagram with DART-MX8M-MINI

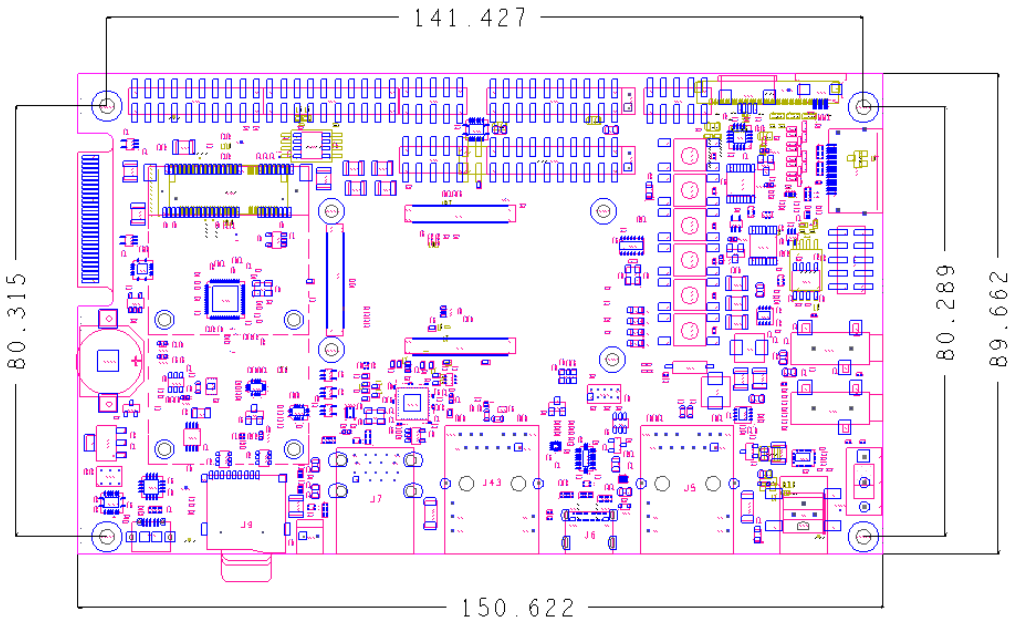


4.5 Block Diagram with DART-MX8M-PLUS



4.6 Board Layout

The VAR-DT8MCustomBoard's physical dimensions are 151 x 90 mm.



Detailed CAD files are available for download at www.variscite.com.

4.7 VAR-DT8MCustomBoard connectors

The below table lists all available connectors on VAR-DT8MCustomBoard,
Refer to chapter 2 for a more detailed description and Pin-out of each connector.

Table 4-1 VAR-DT8MCustomBoard connectors

Reference	Function	Type
J1	DART J1	Board to board, 90 pos., 0.4mm
J2	DART J2	Board to board, 90 pos., 0.4mm
J3	DART J3	Board to board, 90 pos., 0.4mm
J4	Power In	DC In Jack 2.0 mm
J5	10/100/1000Mbps ETH1 Port	RJ-45
J6	USB 3.0/2.0 OTG	USB Type C
J7	USB 3.0 Host x2	USB 3.0 Type A Stacked
J9	SD-MMC	uSD Connector
J10	USB Debug	USB Type micro AB
J11	MIPI-CSI (4 lanes x 2 Cameras)	Edge Connector mates to HSEC8-130-01-SM-DV-A
J12	UART, I2C	Header SMT, 10x2, 2.54mm
J13	SAI2, SAI5	Header SMT, 10x2, 2.54mm
J14	GPIO, SPDIF	Header SMT, 5x2, 2.54mm
J15	LVDS#1 (Clock & Data pairs 0-2)	Header SMT, 10x2, 2.54mm
J16	ECSPI, BT/WIFI Host wake	Header SMT, 5x2, 2.54mm
J17	Resistive Touch I/F	FFC/FPC 4-pin
J18	Capacitive Touch Panel I/F	FFC/FPC 6-pin
J19	HDMI	HDMI Type A Rcpt. SMT, R/A
J20	eDP	Wire to board 1x40 0.5mm SMT, RA
J21	Line In	Audio Jack 3.5 mm
J22	Headphones	Audio Jack 3.5 mm
J23	Mini PCIe Conn #1	Mini PCIe Conn, 2x26 0.8mm
J24	FAN 5V	Header TH, 2x1, 2.54mm
J25	SAI1	Header SMT, 5x2, 2.54mm
J26	LVDS#2 (Clock & Data pairs 0-2)	Header SMT, 5x2, 2.54mm
J27	LVDS#1 (Data pair 3)	Header TH, 2x1, 2.54mm
J28	LVDS#2 (Data pair 3)	Header TH, 2x1, 2.54mm
J29	JTAG	Header TH, 5x2, 1.27mm
J32	Mini PCIe Conn #2	Mini PCIe Conn, 2x26 0.8mm
J40	Power In	2 Pin Terminal Block
J41	QSPIA	Header SMT, 5x2, 2.54mm
J42	DSI/QSPIB	Header SMT, 10x2, 2.54mm
J43	10/100/1000Mbps ETH2 Port	RJ-45
JBT1	RTC Battery Holder	CR1225 Battery Holder

5 Detailed Description

5.1 Overview

This chapter details the VAR-DT8MCustomBoard features and external interfaces, some of which are driven directly by the DART-MX8M, DART-MX8M-MINI or DART-MX8M-PLUS.

Please refer to the applicable DART data sheet for more information.

Table 5-1 describes this chapter table headers and acronyms used.

Table 5-1: Acronyms used on tables column header

Heading	Options	Meaning
Pin#	x	**Pin number on a connector**
Assy		**SOM Applicability**
	Empty	Applicable for all
	DT8M	Applicable for DART-MX8M only
	DT8MM	Applicable for DART-MX8M-MINI only
	DT8MP	Applicable for DART-MX8M-PLUS only
	DT8M/P	Applicable for DART-MX8M and DART-MX8M-PLUS
Type		**Pin type & direction**
	I	INPUT
	O	OUTPUT
	DS	Differential Signal
	A	Analog
	P	Power
Signal		**VAR-DT8MCustomBoard schematic signal name**
Description		**Short Pin functionality description**

5.2 VAR-DT8MCustomBoard Interfaces

5.2.1 DART-MX8M & DART-MX8M-MINI & DART-MX8M-PLUS

VAR-DT8MCustomBoard features x3 90 pin mating connectors to connect with the DART-MX8M or DART-MX8M-MINI or DART-MX8M-PLUS System-on-module.

Please refer to the applicable SOM module data sheet for a complete signal description and pin-out on J1, J2 and J3 connectors.

5.3 Standard External Interfaces

5.3.1 USB HOST & OTG

The DART-MX8M and DART-MX8M-PLUS features two USB3.0/2.0 ports while the DART-MX8M-MINI has only USB2.0 ports.

Custom board implements the following:

- First port connected to a USB3.0/2.0 Type C OTG connector
- Second port connected to a USB3 four port hub which connects as follows:
    - Two hub ports connect to a USB3.0/2.0 Type A stacked Host Connector
    - Two hub ports connect to the USB2.0 interface of two mPCIe connectors.

5.3.1.1 USB3.0/2.0 Type-C OTG Connector Pin-out (J6)

Table 5-2 USB Type-C OTG Connector Pin-out (J6)

Pin #	Assy	CustomBoard Signal	Type	Description
A1		GND	P	Ground return
A2	DT8M/P	SS_TX1_P	DSO	SuperSpeed diff. pair #1, TX, positive
A3	DT8M/P	SS_TX1_N	DSO	SuperSpeed diff. pair #1, TX, negative
A4		USB_SS3_VBUS	P	Bus power
A5		USB_SS3_CC1	IO	Configuration channel
A6		USB_C_OTG_DP	DSIO	Non-SuperSpeed diff. pair, pos. 1, positive
A7		USB_C_OTG_DN	DSIO	Non-SuperSpeed diff. pair, pos. 1, negative
A8		SBU1	IO	Sideband use (SBU)
A9		USB_SS3_VBUS	P	Bus power
A10	DT8M/P	SS_RX2_N	DSI	SuperSpeed diff. pair #4, RX, negative
A11	DT8M/P	SS_RX2_P	DSI	SuperSpeed diff. pair #4, RX, positive
A12		GND	P	Digital Ground
B1		GND	P	Digital Ground
B2	DT8M/P	SS_TX2_P	DSO	SuperSpeed diff. pair #3, TX, positive
B3	DT8M/P	SS_TX2_N	DSO	SuperSpeed diff. pair #3, TX, negative
B4		USB_SS3_VBUS	P	Bus power
B5		USB_SS3_CC2	IO	Configuration channel
B6		USB_C_OTG_DP	DSIO	Non-SuperSpeed diff. pair, pos. 2, positive
B7		USB_C_OTG_DN	DSIO	Non-SuperSpeed diff. pair, pos. 2, negative
B8		SBU2	IO	Sideband use (SBU)
B9		USB_SS3_VBUS	P	Bus power
B10	DT8M/P	SS_RX1_N	DSI	SuperSpeed diff. pair #2, RX, negative
B11	DT8M/P	SS_RX1_P	DSI	SuperSpeed diff. pair #2, RX, positive

Pin #	Assy	CustomBoard Signal	Type	Description
B12		GND	P	Digital Ground
SH1		GND	P	SHIELD pin reference
SH2		GND	P	SHIELD pin reference
SH3		GND	P	SHIELD pin reference
SH4		GND	P	SHIELD pin reference

5.3.1.2 USB3.0/2.0 HOST Connector Pin-out (J7)

Table 5-3 USB3.0/2.0 Host Connector Pin-out (J7)

Pin #	Assy	CustomBoard Signal	Type	Description
1		USB3_PRT2_PWR	P	Port2 Bus power
2		USB2_P2_C_DN	DSIO	Port2 SuperSpeed diff. pair, negative
3		USB2_P2_C_DP	DSIO	Port2 Non-SuperSpeed diff. pair, positive
4		GND	P	Digital Ground
5	DT8M/P	USB2_P2_RXN	DSI	Port2 SuperSpeed diff. pair RX, negative
6	DT8M/P	USB2_P2_RXP	DSI	Port2 SuperSpeed diff. pair RX, positive
7		GND	P	Digital Ground
8	DT8M/P	USB2_P2_C_TXN	DSO	Port2 SuperSpeed diff. pair TX, negative
9	DT8M/P	USB2_P2_C_TXP	DSO	Port2 SuperSpeed diff. pair TX, positive
10		USB3_PRT1_PWR	P	Bus power
11		USB2_P1_C_DN	DSIO	Port1 Non-SuperSpeed diff. pair, negative
12		USB2_P1_C_DP	DSIO	Port1 Non-SuperSpeed diff. pair, positive
13		GND	P	Digital Ground
14	DT8M/P	USB2_P1_RXN	DSI	Port1 SuperSpeed diff. pair RX, negative
15	DT8M/P	USB2_P1_RXP	DSI	Port1 SuperSpeed diff. pair RX, positive
16		GND	P	Digital Ground
17	DT8M/P	USB2_P1_C_TXN	DSO	Port1 SuperSpeed diff. pair TX, negative
18	DT8M/P	USB2_P1_C_TXP	DSO	Port1 SuperSpeed diff. pair TX, positive
SH1		GND	P	SHIELD pin reference
SH2		GND	P	SHIELD pin reference
SH3		GND	P	SHIELD pin reference
SH4		GND	P	SHIELD pin reference

5.3.2 uSD Card

uSD Card interface is driven by SD/MMC2 interface of the DART-MX8M/MINI/PLUS.

5.3.2.1 uSD card slot Connector Pin-out (J9)

Table 5-4 uSD Card Slot Connector Pin-out (J9)

Pin #	Assy	CustomBoard Signal	Type	Description
1		CONN_SD2_DATA2	IO	MMC Parallel Data2
2		CONN_SD2_DATA3	IO	MMC Parallel Data3
3		CONN_SD2_CMD	IO	MMC Command
4		SW_3P3_SD2	P	3.3V supply from SOM; Supply is switchable
5		CONN_SD2_CLK_R	I	MMC Clock
6		GND	P	Digital Ground
7		CONN_SD2_DATA0	IO	MMC Parallel Data0
8		CONN_SD2_DATA1	IO	MMC Parallel Data1
9		CONN_SD2_CD_B	O	MMC Card Detect
10		GND	P	SHIELD pin reference
11		GND	P	SHIELD pin reference
12		GND	P	SHIELD pin reference
13		GND	P	SHIELD pin reference

5.3.3 Mini PCIe

The VAR-DT8MCustomBoard exports the DART-MX8M/MINI/PLUS PCIe port1 (common to all DART) interface through a standard Mini PCI Express connector supporting connection of min PCI Express expansion cards.

5.3.3.1 Mini PCIe Connector Pin-out (J23)

Table 5-5 mini PCI Express Connector Pin-out (J23)

Pin #	Assy	CustomBoard Signal	Type	Description
1				
2		BASE_PER_3V3	P	Base board 3.3V
3				
4		GND	P	Digital Ground
5				
6		BASE_PER_1V5	P	Base board 1.5V Limited to 300mA
7				
8				
9		GND	P	Digital Ground

Pin #	Assy	CustomBoard Signal	Type	Description
10				
11		PCIE1_REFCLK100M_N	DSI	PCIe Clock Diff. Negative; 100MHz HCSL
12				
13		PCIE1_REFCLK100M_P	DSI	PCIe Clock Diff. Positive; 100MHz HCSL
14				
15		GND	P	Digital Ground
16				
17				
18		GND	P	Digital Ground
19				
20				
21		GND	P	Digital Ground
22		EXP_MPCIE1_RST_B	O	PCIe Port #1 Reset signal; GPIO Expander #2 Port 3
23		PCIE1_CRXM	DSI	PCIe Receive lane Diff. Negative; SOC port #1
24		BASE_PER_3V3	P	Base board 3.3V
25		PCIE1_CRXP	DSI	PCIe Receive lane Diff. Positive; SOC port #1
26		GND	P	Digital Ground
27		GND	P	Digital Ground
28		BASE_PER_1V5	P	Base board 1.5V Limited to 300mA
29		GND	P	Digital Ground
30		I2C4_SCL	O	I2C #4 Clock
31		PCIE1_CTXM	DSO	PCIe Transmit lane Diff. Negative; SOC port #1
32		I2C4_SDA	IO	I2C #4 Data
33		PCIE1_CTXP	DSO	PCIe Transmit lane Diff. Positive; SOC port #1
34		GND	P	Digital Ground
35		GND	P	Digital Ground
36		USB_MPCIE1_DM	DSIO	USB2.0 Diff. Negative; USB Hub port #3
37		GND	P	Digital Ground
38		USB_MPCIE1_DP	DSIO	USB2.0 Diff. Positive; USB Hub port #3
39		BASE_PER_3V3	P	Base board 3.3V
40		GND	P	Digital Ground
41		BASE_PER_3V3	P	Base board 3.3V
42				
43		GND	P	Digital Ground
44				
45				

Pin #	Assy	CustomBoard Signal	Type	Description
46				
47				
48		BASE_PER_1V5	P	Base board 1.5V Limited to 300mA
49				
50		GND	P	Digital Ground
51				
52		BASE_PER_3V3	P	Base board 3.3V

5.3.4 M.2

The VAR-DT8MCustomBoard has an option to export the DART-MX8M PCIe port2 (available only on DART-MX8M) through an M.2 connector supporting connection of expansion cards compatible with the M.2 form factor.

For DART-MX8M-MINI/PLUS, PCIe port1, if needed, can be routed to M.2 connector instead of mini PCIe connector (J23) by resistor assembly option (see VAR-DT8-CustomBoard schematic assembly notes).

5.3.4.1 M.2 Connector Pin-out (J32)

Table 5-6 M.2 Connector Pin-out (J32)

Pin #	Assy	CustomBoard Signal	Type	Description
1		GND	P	Digital Ground
2		BASE_PER_3V3	P	Base board 3.3V
3		USB_MPCIE2_DP	DSIO	USB2.0 Diff. Positive; USB Hub port #4
4		BASE_PER_3V3	P	Base board 3.3V
5		USB_MPCIE2_DM	DSIO	USB2.0 Diff. Negative; USB Hub port #4
6				
7		GND	P	Digital Ground
8				
9				
10				
11				
12				
13				
14				
15				
16				
17				
18		GND	P	Digital Ground
19				
20				

Pin #	Assy	CustomBoard Signal	Type	Description
21				
22				
23				
32				
33		GND	P	Digital Ground
34				
35		PCIE2_CTXP	DSO	PCIe Transmit lane Diff. Positive; DART-MX8M - port #2 DART-MX8M-MINI/PLUS - port #1 (exported via assembly option see VAR-DT8CustomBoard schematics)
36				
37		PCIE2_CTXN	DSO	PCIe Transmit lane Diff. Negative; DART-MX8M - port #2 DART-MX8M-MINI/PLUS - port #1 (exported via assembly option see VAR-DT8CustomBoard schematics)
38		BASE_PER_1V8	P	Optional 1.8V VDDIO (exported via assembly option see VAR-DT8CustomBoard schematics)
39		GND	P	Digital Ground
40		BASE_PER_1V8	P	Optional 1.8V VDDIO (exported via assembly option see VAR-DT8CustomBoard schematics)
41		PCIE2_CRXP	DSI	PCIe Receive lane Diff. Positive; DART-MX8M - port #2 DART-MX8M-MINI/PLUS - port #1
42				
43		PCIE2_CRXM	DSI	PCIe Receive lane Diff. Negative; DART-MX8M - port #2 DART-MX8M-MINI/PLUS - port #1
44				
45		GND	P	Digital Ground
46				
47		PCIE2_REFCLK100M_P	DSI	PCIe Clock Diff. Positive; 100MHz HCSL
48				
49		PCIE2_REFCLK100M_N	DSI	PCIe Clock Diff. Negative; 100MHz HCSL
50				
51		GND	P	Digital Ground
52		EXP_MPCIE2_RST_B	O	PCIe Port #2 Reset signal; GPIO Expander #2 Port 2
53		M.2_CLK_REQ_B	I	M.2 Clock request by UART4_TXD(GPIO5_IO29)

Pin #	Assy	CustomBoard Signal	Type	Description
				requires GPIO Expander #2 port1 EXP_CSI_BUF_EN_B signal to be set HIGH (exported via assembly option see VAR-DT8CustomBoard schematics)
54				
55		M.2_WAKE_B	I	M.2 Host Wake signal Exported to Test point
56		M.2_WIFI_DIS_B	O	M.2 WIFI Disable signal Exported to Test point
57		GND	P	Digital Ground
58		I2C4_SDA_1V8	IO	I2C #4 Data
59				
60		I2C4_SCL_1V8	O	I2C #4 Clock
61				
62				
63		GND	P	Digital Ground
64				
65				
66				
67				
68				
69		GND	P	Digital Ground
70				
71				
72		BASE_PER_3V3	P	Base board 3.3V
73				
74		BASE_PER_3V3	P	Base board 3.3V
75		GND	P	Digital Ground

Note

1. *J32 located on the print side and is not assembled*
2. *Certain signals are routed via serial resistors/capacitors assembly option to J32. Refer to* VAR-DT8-CustomBoard *schematics assembly notes.*
3. *When using J32 to route DART-MX8M PCIe port #2 to J32, R215 should be removed to enable PCIe reference clock. Enabling the interface in the DTS file, with no reference clock running will prevent full boot*

5.3.5 Ethernet

The VAR-DT8MCustomBoard connects the DART-MX8M/DART-MX8M-MINI/DART-MX8M-PLUS Gigabit Ethernet interface, sourced by its' internal PHY, to a standard RJ45 Ethernet jack connector with integrated magnetics.

The VAR-DT8MCustomBoard includes also an external Ethernet PHY and 2nd RJ45 Ethernet jack connector with integrated magnetics circuitry for implementing the 2nd Gigabit Ethernet interface available from SAI1 pin only in the DART-MX8M-PLUS. The lines are also routed to Test points for optional use in case of DART-MX8M/DART-MX8M-MINI (see Digital Audio section).

Please refer to the applicable SOM module datasheet for more information.

5.3.5.1 10/100/1000BaseT RJ45 Connector Pin-out (J5) – Internal PHY

Table 5-7 10/100/100BaseT Internal PHY RJ45 Connector Pin-out (J5)

Pin #	Assy	CustomBoard Signal	Type	Description
L1		LED_ACT	O	Activity LED Anode;
L2		GND	P	Digital Ground
L4		LED_LINK10_100	IO	Link 10/100 LED Anode;
				Link 1000 LED Cathode;
L5		LED_LINK1000	IO	Link 1000 LED Anode;
				Link 10/100 LED Cathode;
R1		TCT3	O	Primary transformer common pin
R2		ETH_TRX2_N	DSIO	Bi-directional diff. pair C negative
R3		ETH_TRX2_P	DSIO	Bi-directional diff. pair C positive
R4		ETH_TRX1_P	DSIO	Bi-directional diff. pair B positive
R5		ETH_TRX1_N	DSIO	Bi-directional diff. pair B negative
R6		TCT2	O	Primary transformer common pin
R7		TCT4	O	Primary transformer common pin
R8		ETH_TRX3_P	DSIO	Bi-directional diff. pair D positive
R9		ETH_TRX3_N	DSIO	Bi-directional diff. pair D negative
R10		ETH_TRX0_N	DSIO	Bi-directional diff. pair A negative
R11		ETH_TRX0_P	DSIO	Bi-directional diff. pair A positive
R12		TCT1	O	Primary transformer common pin
SH1		GND_EARTH	P	EARTH
SH2		GND_EARTH	P	EARTH

Note

For detailed LED behavior see LED status table in SOM data sheet.

5.3.5.2 10/100/1000BaseT RJ45 Connector Pin-out (J43) – External PHY

Table 5-8 10/100/100BaseT External PHY RJ45 Connector Pin-out (J43)

Pin #	Assy	CustomBoard Signal	Type	Description
L1		ETH1_LED0	O	Activity LED Anode;
L2		GND	P	Digital Ground
L4		GND	P	Digital Ground
L5		LED_LINK	IO	Link 1000 LED Anode;
R1		TCT3	O	Primary transformer common pin
R2		ETH1_MDI_C_N	DSIO	Bi-directional diff. pair C negative
R3		ETH1_MDI_C_P	DSIO	Bi-directional diff. pair C positive
R4		ETH1_MDI_B_P	DSIO	Bi-directional diff. pair B positive
R5		ETH1_MDI_B_N	DSIO	Bi-directional diff. pair B negative
R6		TCT2	O	Primary transformer common pin
R7		TCT4	O	Primary transformer common pin
R8		ETH1_MDI_D_P	DSIO	Bi-directional diff. pair D positive
R9		ETH1_MDI_D_N	DSIO	Bi-directional diff. pair D negative
R10		ETH1_MDI_A_N	DSIO	Bi-directional diff. pair A negative
R11		ETH1_MDI_A_P	DSIO	Bi-directional diff. pair A positive
R12		TCT1	O	Primary transformer common pin
SH1		GND_EARTH	P	EARTH
SH2		GND_EARTH	P	EARTH

Table 5-9 Ethernet PHY LED Behavior

STATUS / LED	10M Link	10M Active	100M Link	100M Active	1000M Link	1000M Active
LED_LINK	ON	ON	ON	ON	ON	ON
ETH1_LED0	ON	BLINK	ON	BLINK	ON	BLINK

5.3.6 AUDIO

The VAR-DT8MCustomBoard features two 3.5mm jacks for analog audio interfaces.

- Headphone
- Line in

The analog audio I/F signals are driven by the DART-MX8M/DART-MX8M-MINI/DART-MX8M-PLUS CODEC. Please refer to the applicable SOM module data sheet for complete audio codec information.

Also, a digital microphone is implemented on the VAR-DT8MCustomBoard, see schematics for U32.

5.3.6.1 Line In Jack Connector Pin-out (J21)

Table 5-10 Line in Jack Connector Pin-out (J21)

Pin #	Assy	CustomBoard Signal	Type	Description
1		AGND	AP	Analog ground return for audio.
2		LLINEIN_C	AI	Line-in Left input
3		RLINEIN_C	AI	Line-in Right input

5.3.6.2 Headphone jack Connector Pin-out (J22)

Table 5-11 Headphone out Jack Connector Pin-out (J22)

Pin #	Assy	CustomBoard Signal	Type	Description
1		AGND	AP	Analog ground return for audio.
2		HPLOUT_C	AO	Headphone out Left
3		HPROUT_C	AO	Headphone out Right

5.3.7 Serial Camera

The VAR-DT8MCustomBoard supports two MIPI CSI camera sensor inputs using an extension camera board connected to an edge connector in the VAR-DT8CustomBoard.

The Camera Board Mating connector: SAMTEC 60POS 0.8mm pitch, **HSEC8-130-01-SM-DV-A**

5.3.7.1 Serial Camera Connector Pin-out (J11)

Table 5-12 Serial Camera Connector Pin-out (J11)

Pin #	Assy	CustomBoard Signal	Type	Description
1		BASE_PER_3V3	P	Base board 3.3V
2		GND	P	Digital Ground
3		BASE_PER_3V3	P	Base board 3.3V
4		I2C4_SDA_1V8	IO	I2C #4 Data
5		BASE_PER_1V8	P	Base board 1.8V
6		I2C4_SCL_1V8	IO	I2C #4 Clock
7		BASE_PER_1V8	P	Base board 1.8V
8		GND	P	Digital Ground
9		GND	P	Digital Ground
10		EXP_CSI_P2_PWREN_1V8	O	Power down control; Active Low; GPIO Expander #1 port 2
11		CSI_P1_DP0	DSI	CSI Port1 Lane0; Positive
12		EXP_CSI_P2_RST_B_1V8	O	Reset control; Active Low; GPIO Expander #1 port 0
13		CSI_P1_DN0	DSI	CSI Port1 Lane0; Negative
14		CSI_P2_OPT_1V8	O	Optional discrete
15		GND	P	Digital Ground
16		CSI_P2_SYNC_1V8	O	Sync signal
17		CSI_P1_CKP	DSI	CSI Port1 Clock; Positive
18		GND	P	Digital Ground
19		CSI_P1_CKN	DSI	CSI Port1 Clock; Negative
20		CSI_P2_TRIG_1V8	I	Trigger
21		GND	P	Digital Ground
22		GND	P	Digital Ground
23		CSI_P1_DP1	DSI	CSI Port1 Lane1; Positive
24	DT8M/P	CSI_P2_DN3	DSI	CSI Port2 Lane3; Negative
25		CSI_P1_DN1	DSI	CSI Port1 Lane1; Negative
26	DT8M/P	CSI_P2_DP3	DSI	CSI Port2 Lane3; Positive
27		GND	P	Digital Ground
28		GND	P	Digital Ground
29		CSI_P1_DP2	DSI	CSI Port1 Lane2; Positive

Pin #	Assy	CustomBoard Signal	Type	Description
30	DT8M/P	CSI_P2_DN2	DSI	CSI Port2 Lane2; Negative
31		CSI_P1_DN2	DSI	CSI Port1 Lane2; Negative
32	DT8M/P	CSI_P2_DP2	DSI	CSI Port2 Lane2; Positive
33		GND	P	Digital Ground
34		GND	P	Digital Ground
35		CSI_P1_DP3	DSI	CSI Port1 Lane3; Positive
36	DT8M/P	CSI_P2_DN1	DSI	CSI Port2 Lane1; Negative
37		CSI_P1_DN3	DSI	CSI Port1 Lane3; Negative
38	DT8M/P	CSI_P2_DP1	DSI	CSI Port2 Lane1; Positive
39		GND	P	Digital Ground
40		GND	P	Digital Ground
41		CSI_P1_TRIG_1V8	I	Trigger
42	DT8M/P	CSI_P2_CKN	DSI	CSI Port2 Clock; Negative
43		GND	P	Digital Ground
44	DT8M/P	CSI_P2_CKP	DSI	CSI Port2 Clock; Positive
45		CSI_P1_SYNC_1V8	O	Sync signal
46		GND	P	Digital Ground
47		CSI_P1_OPT_1V8	O	Optional discrete
48	DT8M/P	CSI_P2_DN0	DSI	CSI Port2 Lane0; Negative
49		EXP_CSI_P1_RST_B_1V8	O	Reset control; Active Low; GPIO Expander #1 port 1
50	DT8M/P	CSI_P2_DP0	DSI	CSI Port2 Lane0; Positive
51		EXP_CSI_P1_PWREN_1V8	O	Power down control; Active Low; GPIO Expander #1 port 3
52		GND	P	Digital Ground
53		GND	P	Digital Ground
54		BASE_PER_1V8	P	Base board 1.8V
55		I2C2_SCL_1V8	IO	I2C #2 Clock
56		BASE_PER_1V8	P	Base board 1.8V
57		I2C2_SDA_1V8	IO	I2C #2 Data
58		BASE_PER_3V3	P	Base board 3.3V
59		GND	P	Digital Ground
60		BASE_PER_3V3	P	Base board 3.3V

Note

Camera control (reset, power down) and I2C interfaces runs at 1.8V levels.

5.3.8 LVDS & DSI Display

The VAR-DT8MCustomBoard exposes Dual-Link LVDS interface, MIPI-DSI to FlatLink™ bridge assembled on the DART-MX8M and DART-MX8M-MINI. Refer to the DART-MX8M/ DART-MX8M-MINI data sheet for detailed description of the FlatLink™ interface.
For DART-MX8M-PLUS, LVDS interface is exposed over the same pins is native from the SOC;

The interface is exposed using two Variscite standard 20 pin Headers. Fourth data bit of each interface is extended using additional 2 pin connectors J27, J28.

J15 is used for connecting Variscite's standard 7" LVDS LCD screen.

The VAR-DT8MCustomBoard also exposes native MIPI-DSI 4 lanes**.**
For all SOMs, in case of ***without "LD"*** option – DSI is exported **instead** of LVDS pins to J26, J28.
For DART-MX8M-PLUS ***with*** **"LD"** option, DSI is exported to pins which are not compatible on the DART-MX8M/DART-MX8M-MINI and routed to J42.

5.3.8.1 LVDS#1 Connector Pin-out (J15)

Table 5-13 LVDS Channel 1 Connector Pin-out (J15)

Pin #	Assy	CustomBoard Signal	Type	Description
1		BASE_PER_3V3	P	Base power 3.3V
2		BASE_PER_3V3	P	Base power 3.3V
3		GND	P	Digital Ground
4		GND	P	Digital Ground
5		LVDS1_TX0_N	DSO	LVDS Data0 Diff. Negative
6		LVDS1_TX0_P	DSO	LVDS Data0 Diff. Positive
7		GND	P	Digital Ground
8		LVDS1_TX1_N	DSO	LVDS Data1 Diff. Negative
9		LVDS1_TX1_P	DSO	LVDS Data1 Diff. Positive
10		GND	P	Digital Ground
11		LVDS1_TX2_N	DSO	LVDS Data2 Diff. Negative
12		LVDS1_TX2_P	DSO	LVDS Data2 Diff. Positive
13		GND	P	Digital Ground
14		LVDS1_CLK_N	DSO	LVDS Clock Diff. Negative
15		LVDS1_CLK_P	DSO	LVDS Clock Diff. Positive
16		GND	P	Digital Ground
17		VCC_5V	P	Backlight LED 5V power
18		VCC_5V	P	Backlight LED 5V power
19		GPIO1_IO01(PWM1_OUT)	IO	Backlight Brightness Control; GPIO1_IO01
20		GND	P	Digital Ground

5.3.8.2 LVDS#1 Data3 Extension Connector Pin-out (J27)

Table 5-14 LVDS Channel 1 Data3 Connector Pin-out (J27)

Pin #	Assy	CustomBoard Signal	Type	Description
1		LVDS1_TX3_P	DSO	LVDS Data3 Diff. Positive
2		LVDS1_TX3_N	DSO	LVDS Data3 Diff. Negative

5.3.8.3 LVDS#2 Connector Pin-out (J26)

Table 5-15 LVDS Channel 2 Connector Pin-out (J26)

Pin #	Assy	CustomBoard Signal	Type	Description
1		BASE_PER_3V3	P	Base power 3.3V
2		BASE_PER_3V3	P	Base power 3.3V
3		GND	P	Digital Ground
4		GND	P	Digital Ground
5		LVDS2_DSI_TX0_N	DSO	LVDS Data0 Diff. Negative
6		LVDS2_DSI_TX0_P	DSO	LVDS Data0 Diff. Positive
7		GND	P	Digital Ground
8		LVDS2_DSI_TX1_N	DSO	LVDS Data1 Diff. Negative
9		LVDS2_DSI_TX1_P	DSO	LVDS Data1 Diff. Positive
10		GND	P	Digital Ground
11		LVDS2_TX2_DSI_CLK_N	DSO	LVDS Data2 Diff. Negative
12		LVDS2_TX2_DSI_CLK_P	DSO	LVDS Data2 Diff. Positive
13		GND	P	Digital Ground
14		LVDS2_CLK_DSI_TX2_N	DSO	LVDS Clock Diff. Negative
15		LVDS2_CLK_DSI_TX2_P	DSO	LVDS Clock Diff. Positive
16		GND	P	Digital Ground
17		VCC_5V	P	Backlight LED 5V power
18		VCC_5V	P	Backlight LED 5V power
19		GPIO1_IO01(PWM1_OUT)	IO	Backlight Brightness Control; GPIO1_IO01
20		GND	P	Digital Ground

Note

1. *Connector carries the native MIPI-DSI lanes of the DART-MX8M/DART-MX8M-MINI/DART-MX8M-PLUS SOC when hardware configuration is without "LD"*
2. *LVDS Data2 becomes MIPI-DSI CLK*
3. *LVDS CLK becomes MIPI-DSI Lane2*

5.3.8.4 LVDS#2 Data3 Extension Connector Pin-out (J28)

Table 5-16 LVDS Channel 2 Data3 Connector Pin-out (J28)

Pin #	Assy	CustomBoard Signal	Type	Description
1		LVDS2_DSI_TX3_P	DSO	LVDS Data3 Diff. Positive
2		LVDS2_DSI_TX3_N	DSO	LVDS Data3 Diff. Negative

Note
See J26 table note for DSI function

5.3.8.5 DSI/QSPIB Connector Pin-out (J42)

J42 exports MIPI-DSI lanes of the DART-MX8M-PLUS when hardware configuration is ***with*** "LD"
For DART-MX8M/DART-MX8M-MINI, J42 exports the QSPIB or other alternate functions available.

Table 5-17 DSI/QSPIB Connector Pin-out (J42)

Pin #	Assy	CustomBoard Signal	Type	Description
1		I2C4_SDA	IO	I2C #4 Data
2		I2C4_SCL	O	I2C #4 Clock
3		BASE_PER_3V3	P	Base power 3.3V
4		BASE_PER_3V3	P	Base power 3.3V
5		GND	P	Digital Ground
6		GND	P	Digital Ground
7	DT8M	NAND_DATA04	IO	QSPI B Data 0
7	DT8MM	NAND_DATA04	NC	Not Connected
7	DT8MP	NAND_DATA04	DSO	DT8MP-DSI1_D0_N; DSI Data0 Diff. Negative
8	DT8M	NAND_RE_B	IO	QSPI B Strobe
8	DT8MM	NAND_RE_B	IO	GPIO1_IO07
8	DT8MP	NAND_RE_B	DSO	DT8MP-DSI1_D0_P; DSI Data0 Diff. Positive
9		GND	P	Digital Ground
10	DT8M	NAND_DATA05	IO	QSPI B Data 1
10	DT8MM	NAND_DATA05	NC	Not Connected
10	DT8MP	NAND_DATA05	DSO	DT8MP-DSI1_D1_N; DSI Data1 Diff. Negative
11	DT8M	NAND_CLE	IO	QSPI B Serial Clock
11	DT8MM	NAND_CLE	O	CLKOUT1; 1.8V Level only.
11	DT8MP	NAND_CLE	DSO	DT8MP-DSI1_D1_P; DSI Data1 Diff. Positive
12		GND	P	Digital Ground
13	DT8M	NAND_WP_B	IO	GPIO3_IO18
13	DT8MM	NAND_WP_B	NC	Not Connected
13	DT8MP	NAND_WP_B	DSO	DT8MP-DSI1_D2_N; DSI Data2 Diff. Negative
14	DT8M	NAND_WE_B	IO	GPIO3_IO17
14	DT8MM	NAND_WE_B	NC	Not Connected
14	DT8MP	NAND_WE_B	DSO	DSI Data2 Diff. Positive; DSI Data2 Diff. Positive
15		GND	P	Digital Ground

Pin #	Assy	CustomBoard Signal	Type	Description
16	DT8M	NAND_DATA07	IO	QSPI B Data 3
16	DT8MM	NAND_DATA07	I	CLKIN1; 1.8V Level only.
16	DT8MP	NAND_DATA07	DSO	DT8MP-DSI1_CLK_N; DSI Clock diff. Negative
17	DT8M	NAND_DATA06	IO	QSPI B Data 2
17	DT8MM	NAND_DATA06	I	CLKIN2; 1.8V Level only.
17	DT8MP	NAND_DATA06	DSO	DT8MP-DSI1_CLK_P; DSI Clock Diff. Positive
18		GND	P	Digital Ground
19		VCC_5V	P	Backlight LED 5V power
20		VCC_5V	P	Backlight LED 5V power
21		GPIO1_IO01(PWM1_OUT)	IO	Backlight Brightness Control; GPIO1_IO01
22		GND	P	Digital Ground
23	DT8MP	DT8MP-DSI1_D3_N	DSO	DT8MP-DSI1_D3_N; DSI Data3 Diff. Negative
24	DT8MP	DT8MP-DSI1_D3_P	DSO	DT8MP-DSI1_D3_P; DSI Data3 Diff. Positive

Note

See J42 is located on print side and not assembled

5.3.9 HDMI & eDP Display

The VAR-DT8MCustomBoard exposes the HDMI or DP/eDP alternate function of the DART-MX8M/DART-MX8M-PLUS.

Selection between HDMI and DP/eDP interface is done according to assembly option.
Default assembly option routes the lines to a HDMI connector.

HDMI path coupling and level termination
For DART-MX8M, NXP design requires AC coupling and level termination on HDMI path;
For DART-MX8MP, NXP reference requires DC coupling with no level termination;

Default assembly option is DC coupling and no termination.
This design has been tested ok on the DART-MX8M HDMI and DP paths with resolutions up to 4K;
Though tested with DART-MX8M with limited number of monitors to be functioning properly,
Variscite recommends to use the dedicated lane coupling and termination per each SOC requirements.
See VAR-DT8CustomBoard schematics reference for DART-MX8M HDMI path.

Note - different DTS files are required for HDMI and for DP/eDP.

Refer to the DART-MX8M data sheet for detailed description of these interfaces and HDMI level termination.

Note
HDMI/DP interface does not exist in DART-MX8M-MINI
DP/eDP interface does not exist in DART-MX8M-PLUS

5.3.9.1 HDMI Connector Pin-out (J19)

Table 5-18 HDMI Connector Pin-out (J19)

Pin #	Assy	CustomBoard Signal	Type	Description
1	DT8M/P	HDMI_CN_D2_P	DSO	HDMI TMDS Diff. Data 2; Positive
2		GND	P	Digital Ground
3	DT8M/P	HDMI_CN_D2_N	DSO	HDMI TMDS Diff. Data 2; Negative
4	DT8M/P	HDMI_CN_D1_P	DSO	HDMI TMDS Diff. Data 1; Positive
5		GND	P	Digital Ground
6	DT8M/P	HDMI_CN_D1_N	DSO	HDMI TMDS Diff. Data 1; Negative
7	DT8M/P	HDMI_CN_D0_P	DSO	HDMI TMDS Diff. Data 0; Positive
8		GND	P	Digital Ground
9	DT8M/P	HDMI_CN_D0_N	DSO	HDMI TMDS Diff. Data 0; Negative
10	DT8M/P	HDMI_CN_CLK_P	DSO	HDMI TMDS Diff. Clock; Positive
11		GND	P	Digital Ground
12	DT8M/P	HDMI_CN_CLK_N	DSO	HDMI TMDS Diff. Clock; Negative
13	DT8M/P	HDMI_CN_CEC	IO	Consumer Electronics Control; 1 Wire Serial; Bidirectional

Pin #	Assy	CustomBoard Signal	Type	Description
14	DT8M/P	HDMI_CN_UTILITY/HEAC+	DSIO	HDMI Utility; Alternatively, can be HDMI Ethernet and Audio Return Channel Diff. Positive
15	DT8M/P	HDMI_CN_SCL	O	I2C Serial Clock for DDC (Data Display Channel)
16	DT8M/P	HDMI_CN_SDA	IO	I2C Serial Data for DDC (Data Display Channel)
17		GND	P	Digital Ground
18		VCC_5V_HDMI	P	HDMI 5V Power out
19	DT8M/P	HDMI_CN_HPD/HEAC-	DSIO	HDMI Hot Plug Detect; Alternatively, can be HDMI Ethernet and Audio Return Channel Diff. Negative
MTG1		GND	P	SHIELD pin reference
MTG2		GND	P	SHIELD pin reference
MTG3		GND	P	SHIELD pin reference
MTG4		GND	P	SHIELD pin reference

5.3.9.2 Embedded Display Port Connector Pin-out (J20)

Table 5-19 Embedded DisplayPort Connector Pin-out (J20)

Pin #	Assy	CustomBoard Signal	Type	Description
1				
2		GND	P	Digital Ground
3	DT8M	EDP3_N	DSO	eDP Diff. Data 3; Negative (exported via assembly option see VAR-DT8CustomBoard schematics)
4	DT8M	EDP3_P	DSO	eDP Diff. Data 3; Positive (exported via assembly option see VAR-DT8CustomBoard schematics)
5		GND	P	Digital Ground
6	DT8M	EDP2_N	DSO	eDP Diff. Data 2; Negative (exported via assembly option see VAR-DT8CustomBoard schematics)
7	DT8M	EDP2_P	DSO	eDP Diff. Data 2; Positive (exported via assembly option see VAR-DT8CustomBoard schematics)
8		GND	P	Digital Ground
9	DT8M	EDP1_N	DSO	eDP Diff. Data 1; Negative (exported via assembly option see VAR-DT8CustomBoard schematics)
10	DT8M	EDP1_P	DSO	eDP Diff. Data 1; Positive (exported via assembly option see VAR-DT8CustomBoard schematics)

Pin #	Assy	CustomBoard Signal	Type	Description
11		GND	P	Digital Ground
12	DT8M	EDP0_N	DSO	eDP Diff. Data 0; Negative (exported via assembly option see VAR-DT8CustomBoard schematics)
13	DT8M	EDP0_P	DSO	eDP Diff. Data 0; Positive (exported via assembly option see VAR-DT8CustomBoard schematics)
14		GND	P	Digital Ground
15	DT8M	EDP_AUX_P	DSO	eDP Diff. Auxiliary; Positive (exported via assembly option see VAR-DT8CustomBoard schematics)
16	DT8M	EDP_AUX_N	DSO	eDP Diff. Auxiliary; Negative (exported via assembly option see VAR-DT8CustomBoard schematics)
17		GND	P	Digital Ground
18		VCC_3V3_EDP	P	eDP power 3.3V (exported via assembly option see VAR-DT8CustomBoard schematics)
19		VCC_3V3_EDP	P	eDP power 3.3V (exported via assembly option see VAR-DT8CustomBoard schematics)
20		VCC_3V3_EDP	P	eDP power 3.3V (exported via assembly option see VAR-DT8CustomBoard schematics)
21		VCC_3V3_EDP	P	eDP power 3.3V (exported via assembly option see VAR-DT8CustomBoard schematics)
22				
23		GND	P	Digital Ground
24		GND	P	Digital Ground
25		GND	P	Digital Ground
26		GND	P	Digital Ground
27	DT8M	EDP_HPD	O	HDMI Hot Plug Detect (exported via assembly option see VAR-DT8CustomBoard schematics)
28		GND	P	Backlight Digital Ground
29		GND	P	Backlight Digital Ground
30		GND	P	Backlight Digital Ground
31		GND	P	Backlight Digital Ground
32		EPD_BL_EN	O	eDP backlight Enable (exported via assembly option see VAR-DT8CustomBoard schematics)
33		EPD_BL_PWM	O	eDP backlight PWM (exported via assembly option see

Pin #	Assy	CustomBoard Signal	Type	Description
				VAR-DT8CustomBoard schematics)
34				
35				
36		EDP_BL_PWR	P	eDP Backlight power (exported via assembly option see VAR-DT8CustomBoard schematics)
37		EDP_BL_PWR	P	eDP Backlight power (exported via assembly option see VAR-DT8CustomBoard schematics)
38		EDP_BL_PWR	P	eDP Backlight power (exported via assembly option see VAR-DT8CustomBoard schematics)
39		EDP_BL_PWR	P	eDP Backlight power (exported via assembly option see VAR-DT8CustomBoard schematics)
40				
41		GND	P	Digital Ground
42		GND	P	Digital Ground
43		GND	P	Digital Ground
44		GND	P	Digital Ground

Note

J20 is located of print side and not assembled

5.3.10 Capacitive Touch

VAR-DT8MCustomBoard provides a capacitive Touch interface exposed to an FFC/FPC connector for connecting to Variscite's standard 7" Capacitive touch LCD screen.

5.3.10.1 Capacitive Touch Panel Connector Pin-out (J18)

Table 5-20 Capacitive Touch Panel Connector Pin-out (J18)

Pin #	Assy	CustomBoard Signal	Type	Description
1		EXP_CAPTOUCH_RST_B	O	Capacitive Touch Reset; Active Low; GPIO Expander #2 port 4
2		I2C2_SDA	IO	I2C #2 Data
3		I2C2_SCL	O	I2C #2 Clock
4		GPIO1_IO14	IO	Capacitive Touch Interrupt; Active Low; GPIO1_IO14
5		BASE_PER_3V3	P	Base board 3.3V
6		GND	P	Digital Ground
7		GND	P	Digital Ground
8		GND	P	Digital Ground

5.3.11 Resistive Touch

VAR-DT8MCustomBoard provides a resistive interface exposed to a FFC/FPC connector for connecting to a resistive touch LCD screen.

5.3.11.1 Resistive Touch Connector Pin-out (J17)

Table 5-21 Resistive Touch Connector Pin-out (J17)

Pin #	Assy	CustomBoard Signal	Type	Description
1		TS_X-	AI	X negative side plate connection
2		TS_Y+	AI	Y positive side plate connection
3		TS_X+	AI	X positive side plate connection
4		TS_Y-	AI	Y negative side plate connection
5		GND	P	Digital Ground
6		GND	P	Digital Ground

NOTE

DART-MX8M-PLUS uses GPIO1_IO07 for resistive touch controller interrupt, while DART-MX8M and DART-MX8M-MINI uses GPIO1_IO03

5.3.12 USB - Debug

The VAR-DT8MCustomBoard exposes the debug UART1 interface. The signals are driven by an on-board UART-to-USB Bridge and exposed to a Micro USB connector.

5.3.12.1 USB Debug Connector Pin-out (J10)

Table 5-22 USB Debug Connector Pin-out (J10)

Pin #	Assy	CustomBoard Signal	Type	Description
1		DEBUG_VBUS_C	P	5V power input
2		USB_DEBUG_DM	DSIO	USB Data Negative
3		USB_DEBUG_DP	DSIO	USB Data Positive
4		GND	I	USB Micro ID signal (Slave function)
5		GND	P	Digital Ground
6		GND	P	SHIELD pin reference
7		GND	P	SHIELD pin reference
10		GND	P	SHIELD pin reference
11		GND	P	SHIELD pin reference

5.3.13 I2C & UART & ENET MDIO

The VAR-DT8MCustomBoard exposes I2C, UART and ENET MDIO interfaces. Signals are exported to a standard 20 pin Header.

UART4 is used on SOMs with "WBD" configuration. See DART-MX8M/DART-MX8M-MINI data sheet for details on using any alternate function of these pads externally with “WBD” configuration; For the DART-MX8M-PLUS it is applicable for “WBD” or “WB” configuration.

UART2 on the header implements FTDI adapter connector layout for simple conversion to USB by external module.

5.3.13.1 I2C and UART Connector Pin- out (J12)

Table 5-23 I2C, UART and ENET MDIO Connector Pin-out (J12)

Pin #	Assy	CustomBoard Signal	Type	Description
1		BT_UART4_TX	IO	UART4 Transmit Note: Used by SOM in "WBD" configuration
2		FTDI_RTSN	O	FTDI Header Ready To Send; Active Low
3		BT_UART4_CTS_B	IO	UART4 Clear To Send Note: Used by SOM in "WBD" configuration
4		FTDI_RXI	IO	UART2 Transmit
5		BT_UART4_RX	IO	UART4 Receive Note: Used by SOM in "WBD" configuration
6		FTDI_TXO	IO	UART2 Receive
7		BT_UART4_RTS_B	IO	UART4 Ready To Send Note: Used by SOM in "WBD" configuration
8				
9		BASE_PER_3V3	P	Base board 3.3V;
10		FTDI_CTSN	IO	FTDI Header Clear To Send; Active Low
11		UART3_RXD	IO	UART3 Receive
12		GND	P	Digital Ground
13		UART3_TXD	IO	UART3 Transmit
14		ENET_MDIO	IO	ENET Management Data; Note: Shared with SOM in "EC" Configuration Run at 2.5V levels in this configuration
15		GND	P	Digital Ground
16		ENET_MDC	O	ENET Management Clock; Note: Shared with SOM in "EC" Configuration Run at 2.5V levels in this configuration
17		I2C4_SCL	IO	I2C #4 Clock
18		I2C3_SCL	IO	I2C #3 Clock Note: Shared by SOM all configurations; 10K Pullup included on SOM
19		I2C4_SDA	IO	I2C #4 Data
20		I2C3_SDA	IO	I2C #3 Data Note: Shared by SOM all configurations; 10K pullup included on SOM

5.3.14 GPIO & Digital Audio (SPDIF)

The VAR-DT8MCustomBoard exports alternate GPIO's and SPDIF through a standard 10 pin Header.

5.3.14.1 GPIO & SPDIF Pin-out (J14)

Table 5-24 GPIOs and SPDIF Connector Pin-out (J14)

Pin #	Assy	CustomBoard Signal	Type	Description
1		BASE_PER_3V3	P	Base power 3.3V
2		GPIO1_IO11	IO	GPIO1_IO11 Note: Used by SOM in "LD" configuration
3		SPDIF_RX	IO	SPDIF Receive Data (exported via assembly option see VAR-DT8CustomBoard schematics)
4		GPIO1_IO12	IO	GPIO1_IO12
5		SPDIF_EXT_CLK	IO	SPDIF External Clock Note: Used by SOM in "WBD" configuration
6		GPIO1_IO08	IO	GPIO1_IO08 Note: Used by SOM in "WBD" configuration
7		SPDIF_TX	IO	SPDIF Transmit Data (exported via assembly option see VAR-DT8CustomBoard schematics)
8		GPIO1_IO15	IO	GPIO1_IO15 Note: Connected on custom board to RTC_IRQn Via a series resistor.
9		GND	P	Digital Ground
10		GPIO1_IO06	IO	GPIO1_IO06

5.3.15 Digital Audio (SAI1 & SAI2 & SAI5)

VAR-DT8MCustomBoard exports SAI2 and SAI5 signals through standard 10 pin Headers.
SAI1 signals are exported via a 10 Pin Header and via test points connected in parallel to the signals of the Ethernet PHY on carrier board.
For interfacing SAI1 pins from Test pins, GPIO Expander #2 port 0 EXP_ENET1_IO_LEVEL line should be set low (refer to VAR-DT8CustomBoard schematics for more information).

See DART-MX8M/DART-MX8M-MINI/DART-MX8M-PLUS data sheet for other configurations of SAI.

NOTE

1. SAI1 TXD[7..0] and RXD[7..0] pins are used by DART-MX8M and DART-MX8M-MINI for boot config. Care should be given not to drive them before rise of POR_B signal + 1ms;
   See "Boot Configuration" in data sheet.
2. **DART-MX8M-PLUS boot configuration** set by 4 BOOT_MODE[0..3] pins; Critical one is BOOT_MODE[0] connected internally to SAI1_TXD2 – previous module BOOT_CONFIG10
3. DART-MX8M-MINI has PDM interface available on SAI1 & SAI5

5.3.15.1 SAI2 & SAI5 & CAN-FD Header Pin-out (J13)

Table 5-25 SAI2 & SAI5 Header Pin-out (J13)

Pin #	Assy	CustomBoard Signal	Type	Description
1		CAN_H	IO	CAN Bus High side;
2		CAN_L	IO	CAN Bus Low side
3		BASE_PER_1V8	P	Base board 1.8V
4		GND	P	Digital Ground
5		SAI2_RXC	IO	SAI2 Receive Bit Clock (exported via assembly option see VAR-DT8CustomBoard schematics)
6		PMIC_STBY_REQ	O	SOM PMIC standby request; If used, isolate with high impedance input
7		SAI2_RXFS	IO	SAI2 Receive Frame Sync
8		SAI5_RXC	IO	SAI2 Receive Bit Clock
9		SAI2_RXD0	IO	SAI2 Receive Data 0
10		SAI5_RXFS	IO	SAI5 Receive Frame Sync
11		SAI2_TXC	IO	SAI2 Transmit Bit Clock (exported via assembly option see VAR-DT8CustomBoard schematics)
12		SAI5_RXD0	IO	SAI5 Receive Data 0
13		SAI2_TXFS	IO	SAI2 Transmit Frame Sync
14		SAI5_RXD1	IO	SAI5 Receive Data 1
15		SAI2_TXD0	IO	SAI2 Transmit Data 0
16		SAI5_RXD2	IO	SAI5 Receive Data 2
17		SAI2_MCLK	IO	SAI2 Master Clock
18		SAI5_RXD3	IO	SAI2 Receive Data 0
19		SOM_VDD_PHY_1V8	P	DT8M - SOM INT HDMI PHY 1.8V Power; I < 10mA DT8MP - NVCC_SAI1_SAI5 output from the SOM programmable PMIC LDO.
20		SAI5_MCLK	IO	SAI5 Master Clock

5.3.15.2 SAI1 Header Pin-out (J25)

Table 5-26 SAI1 Header Pin-out (J25)

Pin #	Assy	CustomBoard Signal	Type	Description
1		HDMI_DDC_SCL	O	I2C Serial Clock for DDC (Data Display Channel) (SoC side)
2		SAI1_RXFS	IO	SAI1 Receive Frame Sync
3		HDMI_DDC_SDA	IO	I2C Serial Data for DDC (Data Display Channel) (SoC side)
4		SAI1_RXC	IO	SAI1 Receive Bit Clock
5		HDMI_CEC	IO	Consumer Electronics Control; 1 Wire Serial; Bidirectional (SoC side)
6		SAI1_RXD0(GPIO4_IO02)	IO	SAI1 Receive Data 0 Note: Used by SOM for boot config @ power up
7		HDMI_HPD	O	HDMI Hot Plug Detect (SoC side)
8		SAI1_MCLK(GPIO4_IO20)	IO	SAI1 Master Clock
9	DT8M	SOM_WIFI32K	IO	GPIO1_IO00 Note: Used by SOM as 32.768Khz reference clock with "WBD" Configuration
9	DT8MM	GPIO1_IO00	IO	GPIO1_IO00
10		GND	P	Digital Ground

Note

SAI1 alternate function for DART-MX8M-MINI is PDM.

5.3.15.3 SAI1 Test Points

Table 5-27 SAI1 Test Points

Pin #	Assy	CustomBoard Signal	Type	Description
TP31		ENET1_RGMII_RD0	IO	SAI1_RXD4(GPIO4_IO06)
TP32		ENET1_RGMII_TD0	IO	SAI1_TXD0(GPIO4_IO12)
TP33		ENET1_RGMII_RD1	IO	SAI1_RXD5(GPIO4_IO07)
TP34		ENET1_RGMII_TD1	IO	SAI1_TXD1(GPIO4_IO13)
TP35		ENET1_RGMII_RD3	IO	SAI1_RXD7(GPIO4_IO09)
TP36		ENET1_RGMII_TXC	IO	SAI1_TXD5(GPIO4_IO17)
TP37		ENET1_RGMII_RD2	IO	SAI1_RXD5(GPIO4_IO07)
TP38		ENET1_RGMII_TD2	IO	SAI1_TXD2(GPIO4_IO14)
TP39		ENET1_RGMII_TD3	IO	SAI1_TXD3(GPIO4_IO15)
TP40		ENET1_RGMII_RXC	IO	SAI1_TXC(GPIO4_IO11)
TP41		ENET1_RGMII_RX_CTL	IO	SAI1_TXFS(GPIO4_IO10)
TP42		ENET1_RGMII_TX_CTL	IO	SAI1_TXD4(GPIO4_IO16)
TP50		DT8MP-ENET1_MDC	IO	SAI1_RXD2(GPIO4_IO04)
TP51		DT8MP-ENET1_MDIO	IO	SAI1_RXD3(GPIO4_IO05)

5.3.16 ECSPI & BT/WIFI Host Wake

VAR-DT8MCustomBoard exports the following signals through a standard 10 pin Header:

1. ECSPI1 interface
2. BT and WIFI Host wake signals available from the DART-MX8M/DART-MX8M-MINI/DART-MX8M-PLUS WIFI module (in case of "WBD" configuration only)
3. GPIO line to be connected to the host wake signal, running in the same levels.

5.3.16.1 ECSPI1 & BT/WIFI Host Wake Header Pin-out (J16)

Table 5-28 ECSPI1 & BT/WIFI Host Wake Header Pin-out (J16)

Pin #	Assy	CustomBoard Signal	Type	Description
1	WB/WBD	BT_HOST_WAKE	O	SOM WIFI module Bluetooth host wake
2		ECSPI1_SCLK	IO	SPI Serial Clock
3	DT8M	SD2_WP(GPIO2_IO20)	IO	GPIO2_IO20; 1.8V/3.3V levels depends on SD2 interface
3	DT8MM	SD1_DATA7(GPIO2_IO09)	IO	GPIO2_IO09; 1.8V level supported only!
3	DT8MP	SD1_RESET_B(GPIO2_IO10)	IO	GPIO2_IO10; WBD - 1.8V level WB - 3.3V level
4		ECSPI1_SS0	IO	SPI Slave Select; Active Low
5	WB/WBD	WIFI_HOST_WAKE	O	SOM WIFI module WIFI host wake
6		ECSPI1_MOSI	IO	SPI Master Out Slave In
7	DT8MP	CAN-MX8MP_H	DSIO	DART-MX8MP CAN-FD Bus High side
8		ECSPI1_MISO	IO	SPI Master In Slave Out
9	DT8MP	CAN-MX8MP_H	DSIO	DART-MX8MP CAN-FD Bus Low side
10		GND	P	Digital Ground

Note

1. *ECSPI1 interface used for the resistive touch controller assembled on the custom board. In order to use the interface via this header ECSPI1_MISO need to be disconnected from the resistive controller OR use a different GPIO as slave select.*
2. *BT HOST wake and/or WIFI HOST wake signals can be connected to J16.3 to use this function; Logic is required to use both.*

5.3.17 QSPIA & QSPIB

The VAR-DT8MCustomBoard exports QSPI and NAND signals through J41, J42 Headers. Both interfaces share the same pins on the SOM.

For NAND and other functions of these pins refer to the SOMs data sheet.

5.3.17.1 QSPIA Header Pin-out (J41)

Table 5-29 QSPIA Header Pin-out (J41)

Note

DART-MX8M-MINI exposes QSPIA signals only in case eMMC is assembled on SOM; In this case signals are 1.8V levels only.

Pin #	Assy	CustomBoard Signal	Type	Description
1	DT8M	NAND_DQS	IO	QSPI A Strobe
1	DT8MM	NAND_DQS	IO	QSPI A Strobe; 1.8V Level only.
1	DT8MP	NAND_DQS	IO	QSPI A Strobe; 1.8V Level only.
2	DT8M	NAND_READY_B	IO	GPIO3_IO16
2	DT8MM	NAND_READY_B	NC	Not Connected
2	DT8MP	NAND_READY_B	NC	Not Connected
3	DT8M	NAND_DATA03	IO	QSPI A Data 3
3	DT8MM	NAND_DATA03	IO	QSPI A Data 3; 1.8V Level only.
3	DT8MP	NAND_DATA03	IO	QSPI A Data 3; 1.8V Level only.
4	DT8M	NAND_CE2_B	IO	QSPI B Slave Select 0; Active Low
4	DT8MM	NAND_CE2_B	O	CLKOUT2; 1.8V Level only.
4	DT8MP	NAND_CE2_B	IO	GPIO1_IO09
5	DT8M	NAND_DATA02	IO	QSPI A Data 2
5	DT8MM	NAND_DATA02	IO	QSPI A Data 2; 1.8V Level only.
5	DT8MP	NAND_DATA02	IO	QSPI A Data 2; 1.8V Level only.
6	DT8M	EN_SOM_VBAT_3V3	I	EN_SOM_VBAT_3V3
6	DT8MM	EN_SOM_VBAT_3V3	NC	Not Connected
6	DT8MP	EN_SOM_VBAT_3V3	I	BOOT_MODE3
7	DT8M	NAND_DATA01	IO	QSPI A Data 1
7	DT8MM	NAND_DATA01	IO	QSPI A Data 1; 1.8V Level only.
7	DT8MP	NAND_DATA01	IO	QSPI A Data 1; 1.8V Level only.
8	DT8M	NAND_ALE	IO	QSPI A Serial Clock
8	DT8MM	NAND_ALE	IO	QSPI A Serial Clock; 1.8V Level only.
8	DT8MP	NAND_ALE	IO	QSPI A Serial Clock; 1.8V Level only.
9	DT8M	NAND_DATA00	IO	QSPI A Data 0

Pin #	Assy	CustomBoard Signal	Type	Description
9	DT8MM	NAND_DATA00	IO	QSPI A Data 0; 1.8V Level only.
9	DT8MP	NAND_DATA00	IO	QSPI A Data 0; 1.8V Level only.
10	DT8M	NAND_CE0_B	IO	QSPI A Slave Select 0; Active Low
10	DT8MM	NAND_CE0_B	IO	QSPI A Slave Select 0; Active Low; 1.8V Level only.
10	DT8MP	NAND_CE0_B	IO	QSPI A Slave Select 0; Active Low; 1.8V Level only.

5.3.17.2 DSI/QSPIB Header Pin-out (J42)

Please refer to DSI/QSPIB Connector Pin-out section.

5.3.18 JTAG

The VAR-DT8MCustomBoard exports the DART-MX8M JTAG signals through a standard 1.27" 10 pin Header.

5.3.18.1 JTAG Header Pin-out (J29)

Table 5-30 JTAG Header Pin-out (J29)

Pin #	Assy	CustomBoard Signal	Type	Description
1		JTAG_VREF	O	JTAG IO reference voltage. Connects to SOM_NVCC_3V3;
2		JTAG_TMS	I	JTAG Mode Select signal
3		GND	P	Digital Ground
4		JTAG_TCK	I	JTAG Clock signal; Requires 10K pull down.
5		GND	P	Digital Ground
6		JTAG_TDO	O	JTAG Data Out signal
7		NC		Not connected
8		JTAG_TDI	I	JTAG Data In signal
9		JTAG_NTRST_C	I	JTAG Reset signal
9	DT8MP	JTAG_MODE	I	Required to enter Boundary Scan (exported via assembly option see VAR-DT8CustomBoard schematics)
10		POR_B_D	IO	Programmer Reset; Open Drain; Used to put the SOC in reset state.

NOTE

J29 is not assembled.

5.4 User Interfaces

5.4.1 LED Indications

5.4.1.1 Power-On LEDs (D35, D34)

Two LED indicators used:

- **D35** indicates that the VAR-DT8MCustomBoard VCC_5V DC IN power after the over voltage and current limiter IC is ON.
- **D34** indicated the SOM power is ON

5.4.1.2 GP LEDs (D7, D10, D12, D14)

LEDs **D7**, **D10**, **D12** are General Purpose functionality LED controlled by GPIO Expander #2 ports 5-7.
LED **D14** is a General Purpose functionality LED controlled by a GPIO.

NOTE

GP-LED D14 is controlled by GPIO which is part of the boot configuration pins in DART-MX8M/DART-MX8M-MINI.
Care should be given not to drive it before rise of POR_B signal + 1ms.

5.4.2 Control Buttons

5.4.2.1 Boot Select (SW7)

The Boot select switch SW7 sets the DART-MX8M/DART-MX8M-MINI/DART-MX8M-PLUS boot source & sequence. Refer to the relevant module data sheet for detailed Boot description.

Table 5-31 Boot Select modes (SW7)

Assy	Position	Logic Level	Boot Source
	ON	High	External (SD)
DT8M/P	OFF	Low	Internal (eMMC)
DT8MM	OFF	Low	Internal (eMMC/NAND)

NOTE

DART-MX8M-MINI NAND configuration currently not available.

5.4.2.2 Power Switch (SW8)

The Power Switch SW8 Connect/Isolate the DC Power to VAR-VAR-DT8MCustomBoard regulators. (Default custom board assembly is: U31 is not assembled, R167 assembled)

The custom board schematics demonstrates an option for using U31 as an eFuse with multiple power protection modes. When used, Power Switch SW8 Connect/Isolate the DC Power input at U31 TPS25942ARVCT output to the VAR-DT8MCustomBoard regulators.

U31 is powered once a power source is available on J4 or J40, regardless of SW8 state!

5.4.2.3 User Buttons (SW1, SW2, SW3, SW4)

SW1, SW2, SW3 and SW4 are User Buttons connected to GPIO Expander #1 ports 4-7 for general purpose usage. In Linux release they can be configured as Left, Enter, and Right Buttons in the DTS file.

5.4.2.4 Reset Button (SW6)

A press on SW6 will perform a system hardware-reset resulting in a complete power cycle of the DART-MX8M/DART-MX8M-MINI and DART-MX8M-PLUS-v1.1 and onwards.

5.4.2.5 ON/OFF Button (SW6)

The ON/OFF is Button supports the following:

1. **In OFF mode:** A short button press causes the internal power management state machine to change state to ON.
2. **In ON mode:** A short button press generates an interrupt (intended to initiate a software-controllable power-down).
   An approximate 5 second or more button press causes a forced OFF.
3. **In Suspend mode:** A short button press will the system to exit suspend mode.

5.4.3 Power

The VAR-DT8MCustomBoard is powered by a +5V power supply, connected either through a 2.0 mm power plug or alternatively through a 2 pin Terminal block.

A 5V fan power output is available via shrouded 2 pin header. Mating Housing Molex 22-01-3027; Connector Terminal Female Molex 08-50-0114;

5.4.3.1 DC-in Jack Pin-out (J4)

Table 5-32 DC-in Jack Pin-out (J4)

Pin #	CustomBoard Signal	Type	Description
1	GND	P	Power supply return
2	GND	P	Power supply return
3	VCC_PJ	P	Power supply 5V
4	VCC_PJ	P	Power supply 5V

5.4.3.2 DC-in Terminal Block Pin-out (J40)

Table 5-33 DC-in 2 pins Terminal Block Pin-out (J40)

Pin #	CustomBoard Signal	Type	Description
1	GND	P	Power supply return
2	VCC_PJ	P	Power supply 5V

5.4.3.3 DC-out FAN 5V Pin-out (J24)

Table 5-34 DC-out 5V FAN Header Pin-out (J24)

Pin #	CustomBoard Signal	Type	Description
1	FAN_PWR	P	Power supply 5V out ***Note: Power via Ferrite Bead***
2	GND	P	Ground Return

Note

J24 is not assembled.

5.4.3.4 RTC Backup Battery (JBT1)

The VAR-DT8MCustomBoard features JBT1, a CR1225 battery holder for powering the on board DS1337U+ RTC Module.

6 Electrical Environmental Specifications

6.1 Absolute maximum electrical specifications

Table 6-1 DC Power Input absolute maximum electrical specifications

	Min	Max
Main Power Supply, DC-IN	-0.3V	6V

6.2 Operational electrical specifications

Table 6-2 DC Power Input Operational electrical specifications

	Min	Max
Main Power Supply, DC-IN	3.5V	5.6V

Note

Values dictated by protection IC U31(TPS25942A) configuration.

7 Environmental specifications

Table 7-1 Environmental specifications

	Min	Max
Commercial operating temperature range	0^0C	+70^0C
MTBF	>10kHRS	
Relative humidity, Operational	10%	90%
Relative humidity, Storage	5%	95%

8 Legal notice

Variscite LTD ("Variscite") products and services are sold subject to Variscite's terms and conditions of sale, delivery and payment supplied at the time of order acknowledgement.

Variscite warrants performance of its products to the specifications in effect at the date of shipment. Variscite reserves the right to make changes to its products and specifications or to discontinue any product or service without notice. Customers should therefore obtain the latest version of relevant information from Variscite to verify that the information is current.

Testing and other quality control techniques are utilized to the extent Variscite deems necessary to support its warranty.

Specific testing of all parameters of each device is not necessarily performed unless required by law or regulation.

In order to minimize risks associated with customer applications, the customer must use adequate design and operating safeguards to minimize inherent or procedural hazards. Variscite is not liable for applications assistance or customer product design. The customer is solely responsible for its selection and use of Variscite products. Variscite is not liable for such selection or use nor for use of any circuitry other than circuitry entirely embodied in a Variscite product.

Variscite products are not intended for use in life support systems, appliances, nuclear systems or systems where malfunction can reasonably be expected to result in personal injury, death or severe property or environmental damage. Any use of products by the customer for such purposes is at the customer's own risk.

Variscite does not grant any license (express or implied) under any patent right, copyright, mask work right or other intellectual property right of Variscite covering or relating to any combination, machine, or process in which its products or services might be or are used. Any provision or publication of any third party's products or services does not constitute Variscite's approval, license, warranty or endorsement thereof. Any third-party trademarks contained in this document belong to the respective third-party owner.

Reproduction of information from Variscite datasheets is permissible only if reproduction is without alteration and is accompanied by all associated copyright, proprietary and other notices (including this notice) and conditions. Variscite is not liable for any un-authorized alteration of such information or for any reliance placed thereon.

Any representations made, warranties given, and/or liabilities accepted by any person which differ from those contained in this datasheet or in Variscite's standard terms and conditions of sale, delivery and payment are made, given and/or accepted at that person's own risk. Variscite is not liable for any such representations, warranties or liabilities or for any reliance placed thereon by any person.

9 Contact information

Headquarters

Variscite LTD
4, Hamelacha St.
Lod.
P.O.B 1121
Airport City, 70100
ISRAEL
Phone +972 (9) 9562910 • Fax +972 (9) 9589477

Tel: +972 (9) 9562910
Fax: +972 (9) 9589477

Sales: sales@variscite.com
Technical support: support@variscite.com

Website: www.variscite.com