VAR-DT8MCustomBoard

Variscite

CONTENT

Disclaimer:

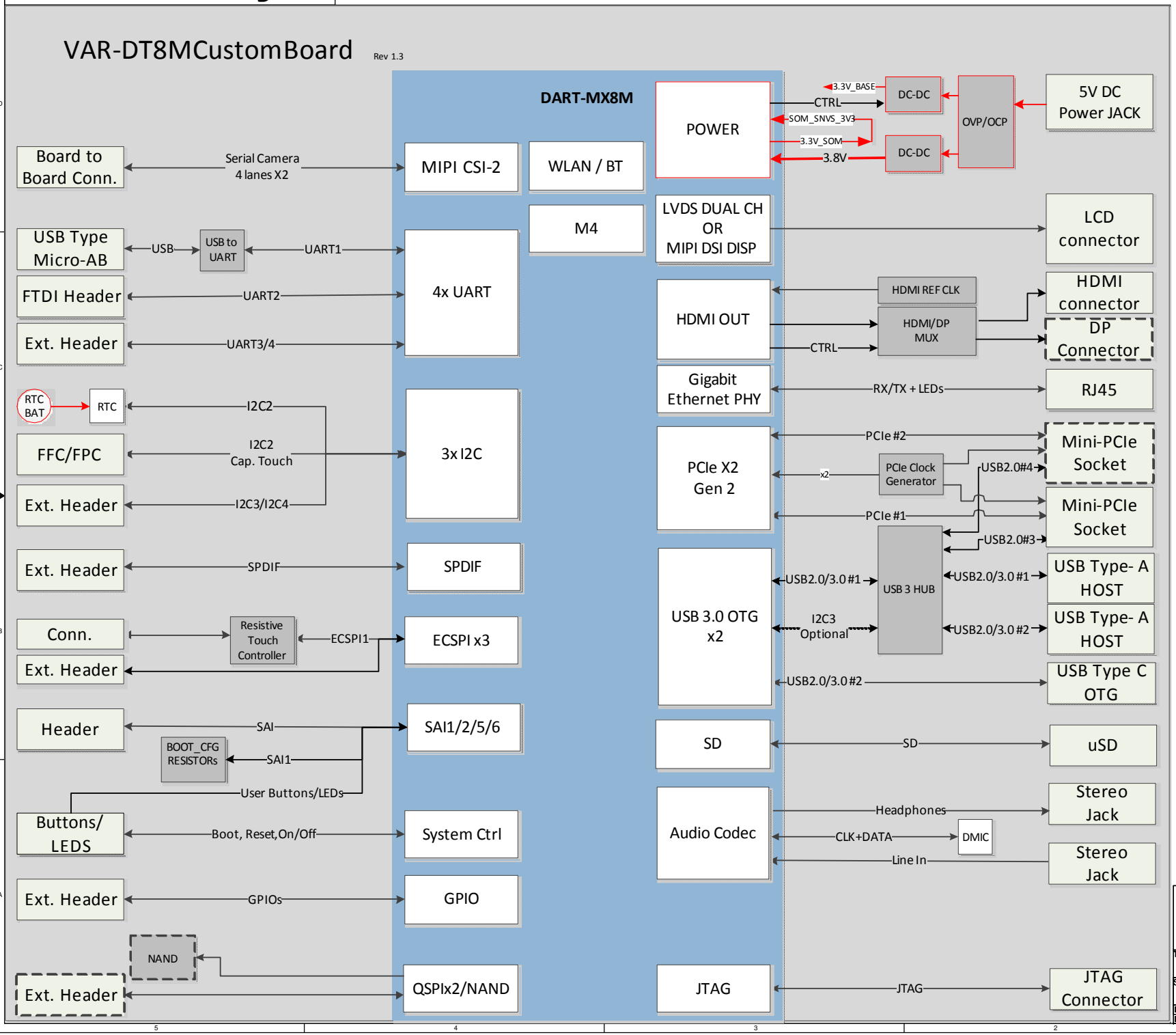
Revision History

Document	Carrier	
1.0	1.0	INITIAL
1.1	1.1	1st Release

Variscite

Title: 01. Cover			
Size: A3	Document Number: VAR-DT8MCustomBoard	Project: VAR-DT8MCustomBoard	Rev: 1.1_R2
Designer: Oded A.		Approved By:	
Date: Tuesday, March 13, 2018		Sheet 1 of 12	

02. Block Diagram



I2C BUS ADDRESS:

I2C1: Internal to SOM

I2C2: PU - 10K on U44
10K on custom
0x54 BOARD ID EEPROM Page0
0x55 BOARD ID EEPROM Page1
0x68 RTC
0x38 CAPACITIVE TOUCH CTRLR
0x3D USB-C CC Logic PTN5150AHXMP
0x3C CSI P1 Camera (1V8) OV5640

I2C3: PU - 5K on SOM
0x60 SOM - Int. power ctrl.
0x2D USB3 HUB
0xXX Header

I2C4: PU - 10K on U44
10K on custom
0x3C CSI P1 Camera (1V8) OV5640
0xXX Header
0xXX mPCIe

Important Notes:

1. Length match for HS signals according to SOM DS
2. USB routed as 90 ohm Diff pairs
3. PCIe/SATA routed as 85 ohm Diff pairs
4. LVDS routed as 100 ohm Diff pairs
5. Other fast changing signals routed as 50 ohm

Variscite

Title: 02. Block Diagram			
Size: A3	Document Number: VAR-DT8MCustomBoard	Project: VAR-DT8MCustomBoard	Rev: 1.1_R2
Designer: Oded A.		Approved By:	
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03 - DART-MX8M Connectors

POR_B : Add Series resistor on (direct CPU pin ~500 Ohm)

DART-MX8M_J1 CB — TOP

J1 — DF40C-90DS-0_4V_51

ETH/MDIO
I2C4
CLK 1/2
QSPI B/NAND
PCIe
CSI1

DART-MX8M_J2 CB — BOTTOM

J2 — DF40C-90DS-0_4V_51

JTAG
BOOT MODE
HDMI
SAI1 BOOT CFG
ECSPI1
UART

DART-MX8M_J3 CB — LEFT

J3 — DF40C-90DS-0_4V_51

LVDS/DSI
USB2
USB1
VBAT LICELL

ETH/MDIO
CTRL: ON/OFF, POR, PMIC_ON, PMIC_STBY
QSPI A/NAND
PCIe
SD2 WiFi Shared
CODEC/SAI3
UART4 Shared w/BT
WDOG + I2C2
SAI5 RX
SAI2 RX/TX
SAI1 BOOT CFG
UART
LVDS/DSI
SPDIF
GPIO1
CSI2

Note: Pinname with /*/ prefix denotes a HW assy option.

Title	03. DART-MX8M Connectors		
Size A2	Document Number	Project	Rev A.1_R2
Designer:	Oded A.	Approved By:	
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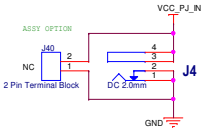
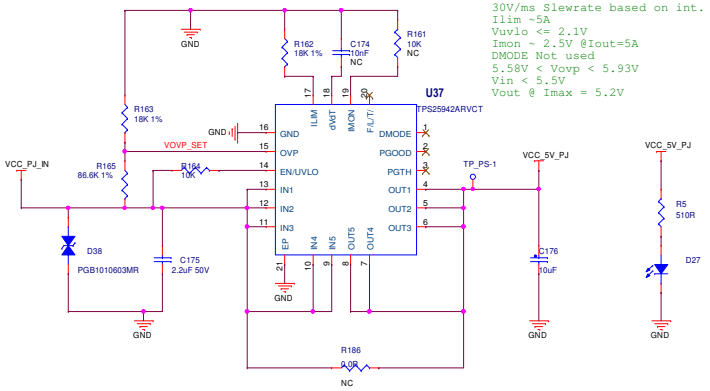
04. Power, RTC,Board ID

5VDC/4A POWER JACK

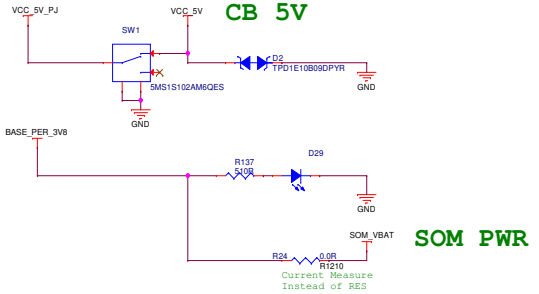


PWR JACK 5V IN OVP/OCP

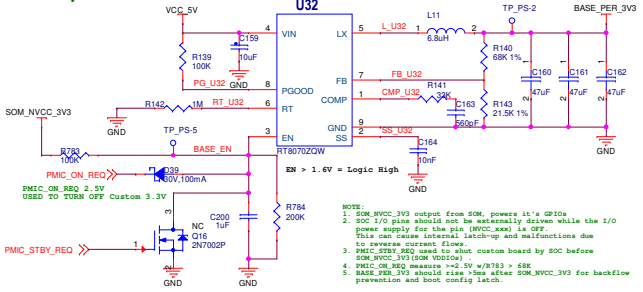
30V/ms Slewrate based on int. circuitry
Ilim ~5A
Vuvlo <= 2.1V
Imon ~ 2.5V @Iout=5A
DMODE Not used
5.58V < Vovp < 5.93V
Vin < 5.5V
Vout @ Imax = 5.2V



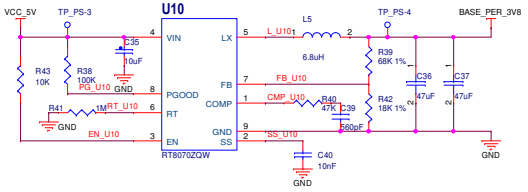
POWER SW/(ON/OFF)



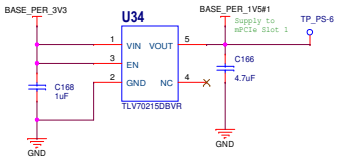
3.3V/3A BASE



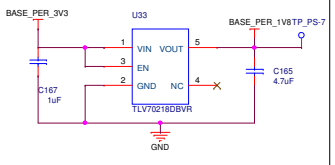
3.8V/3A FROM PWR JACK



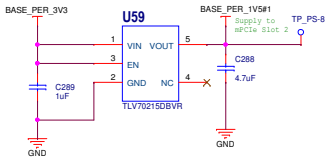
1.5V/0.3A #1 BASE



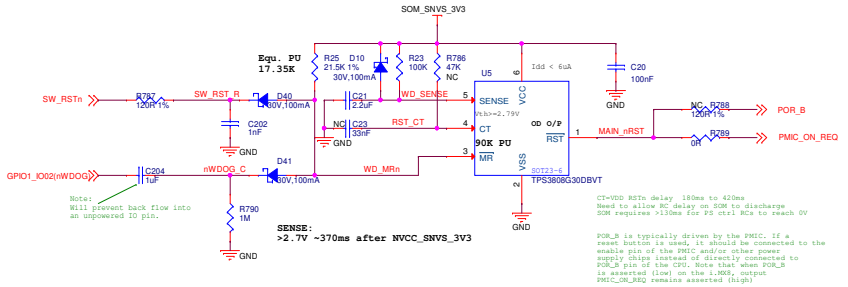
1.8V/0.3A BASE



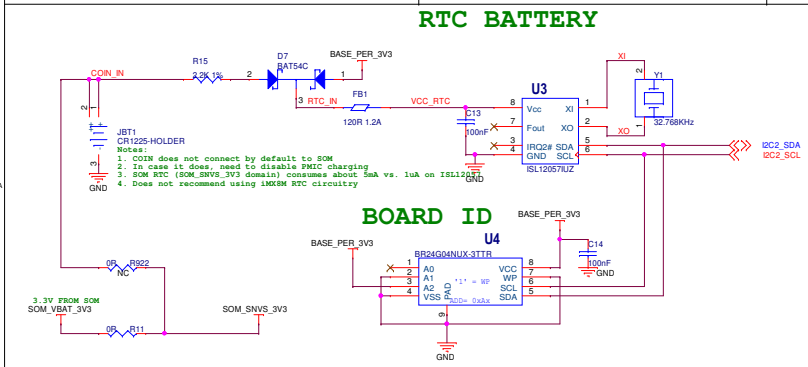
1.5V/0.3A #2 BASE



RESET & WATCHDOG

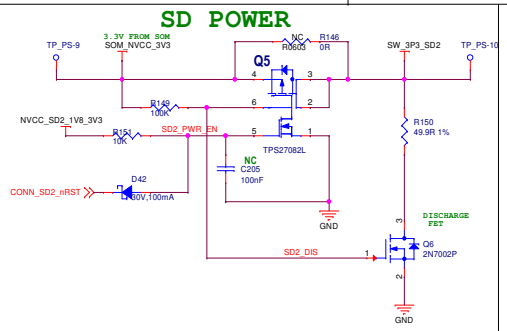


RTC BATTERY

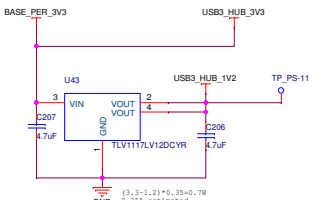


BOARD ID

SD POWER

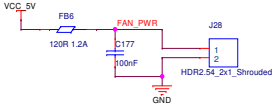


USB3 HUB POWER



Note: Need to ensure 1.2V rise before OR with 3.3V

FAN : 5V/0.2A



Variscite

Title: 04. Power, RTC,Board ID			
Size: A2	Document Number	Project	Rev: 1.1_R2
Designer: Oded A.		Approved By:	
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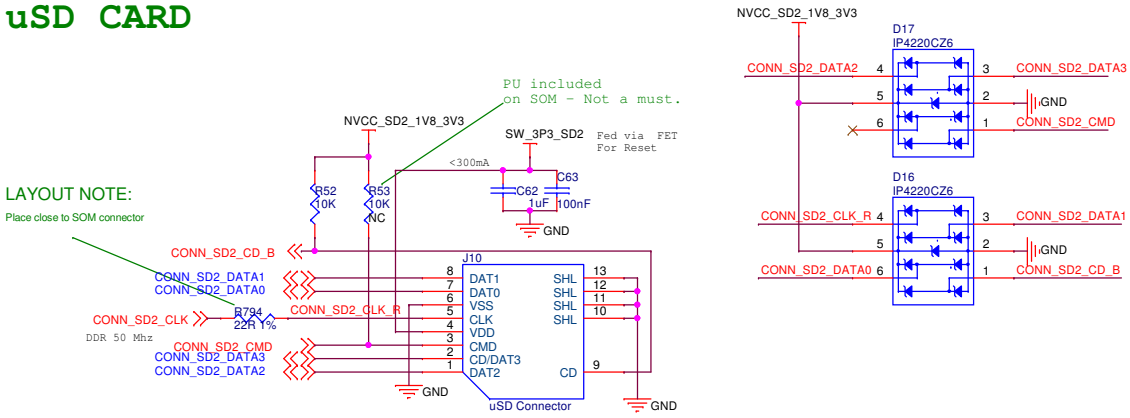
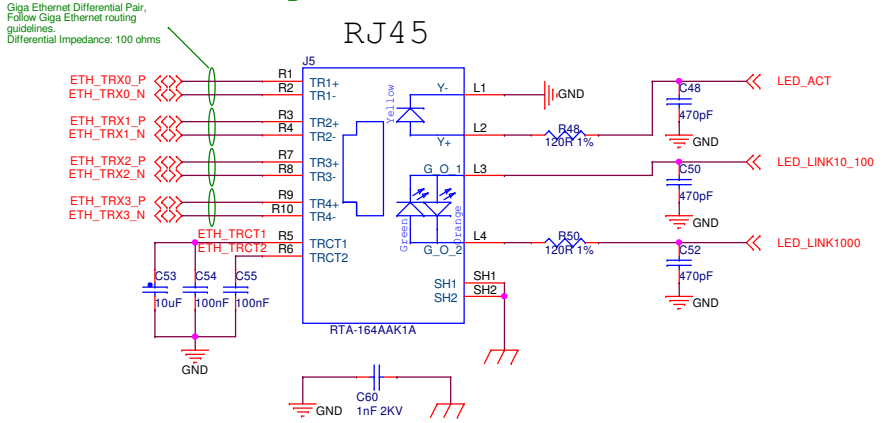
05. ETH, uSD, AUDIO, MIPI-CSI

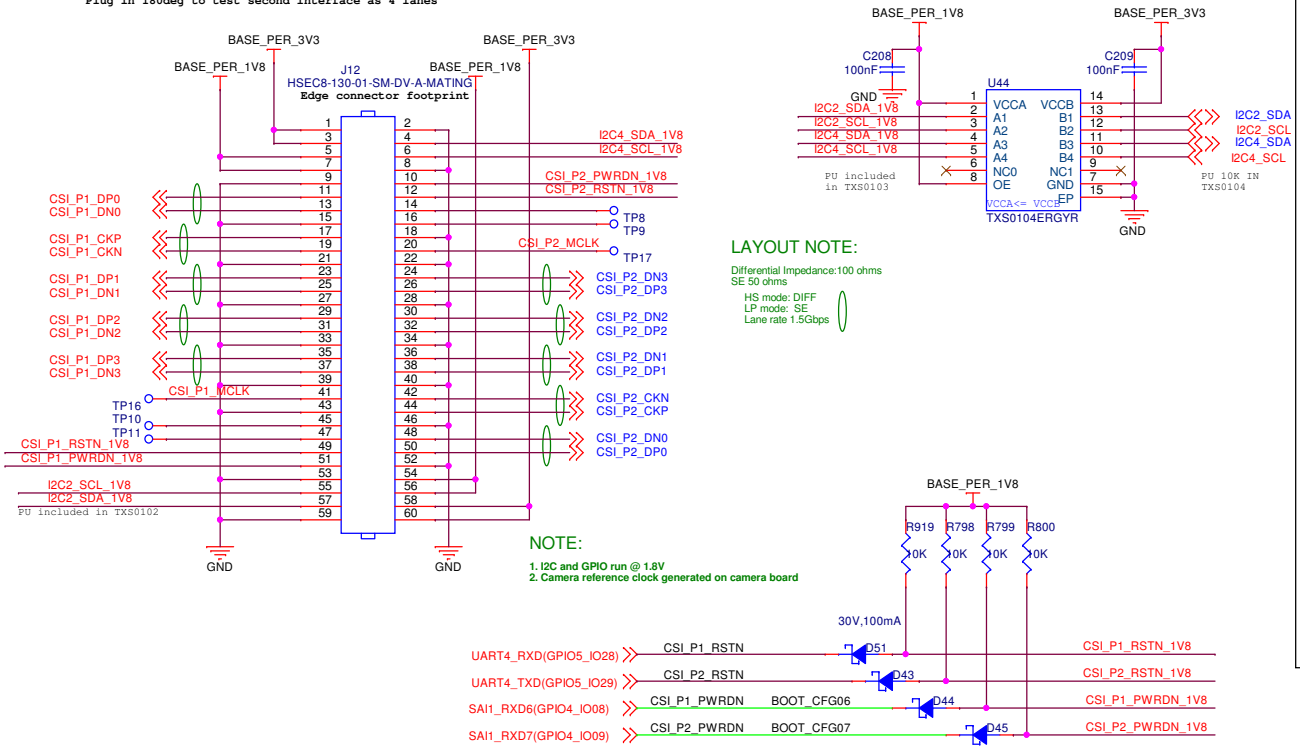
uSD CARD



Gigabit Ethernet2

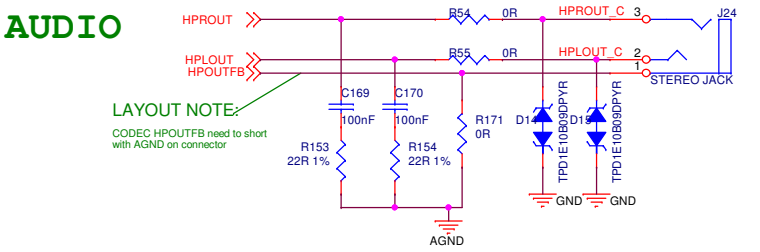


MIPI-CSI0 + MIPI-CSI1

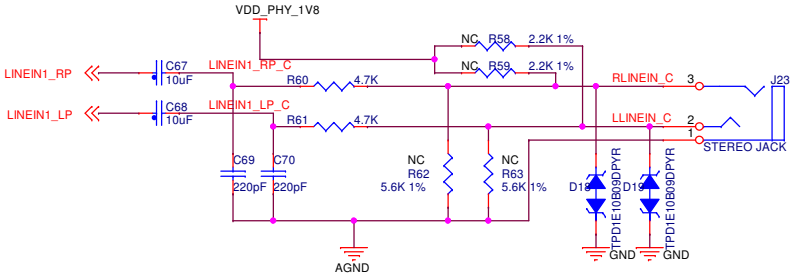


AUDIO

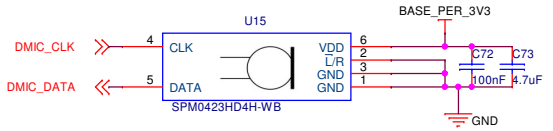
Headphones



Line In



DIGITAL MIC



Variscite

Title: 05. ETH, uSD, AUDIO, MIPI-CSI			
Size: A3	Document Number: VAR-DT8MCustomBoard	Project: VAR-DT8MCustomBoard	Rev: 1.1_R2
Designer: Oded A.		Approved By:	
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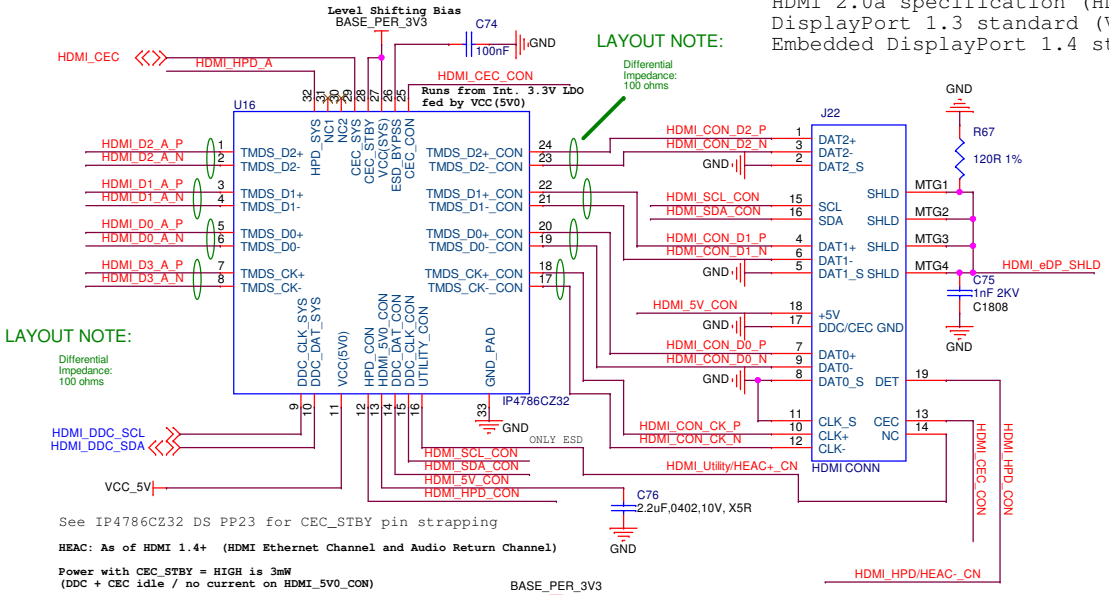
06. HDMI, eDP

HDMI PORT

HDMI 2.0a specification (HDMI.org)
DisplayPort 1.3 standard (VESA.org)
Embedded DisplayPort 1.4 standard



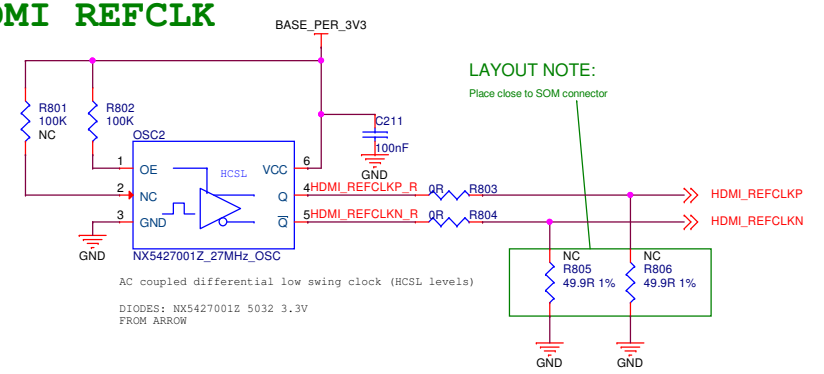
See IP4786CZ32 DS PP23 for CEC_STBY pin strapping

HEAC: As of HDMI 1.4+ (HDMI Ethernet Channel and Audio Return Channel)

Power with CEC_STBY = HIGH is 3mW
(DDC + CEC idle / no current on HDMI_5V0_CON)

Power with CEC_STBY = LOW is 1mW

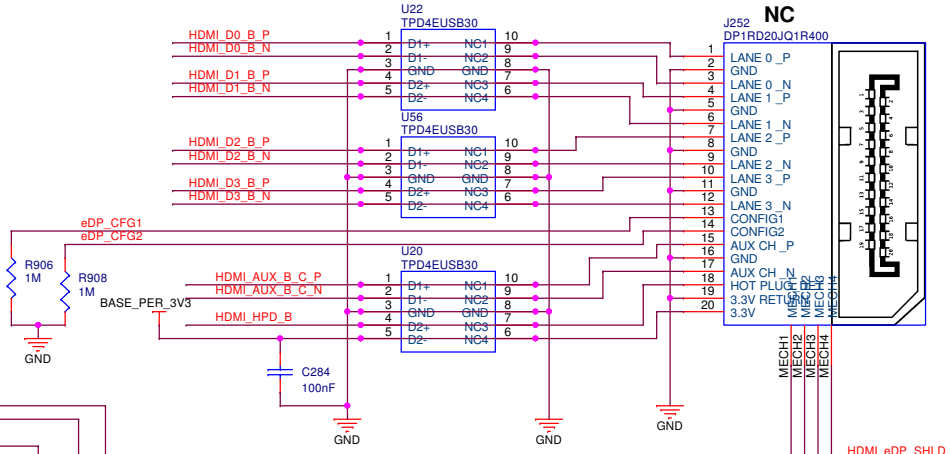
HDMI REFCLK



AC coupled differential low swing clock (HCSL levels)

DIODES: NX5427001Z 5032 3.3V
FROM ARROW

DP PORT



HDMI/eDP/DP SWITCH

HDMI PORT
+ Level Termination

Note : HDMI pull down must not be applied until VDD_PHY_1V8 is up.
Implemtation uses fact that BASE_PER_3V3 rises after all SOM power rails are up.
At boot time GPIO drives U57 switch to B state.

DP port

DISCLAIMER:
eDP/DP interface not validated!
Awaits NXP formal release.

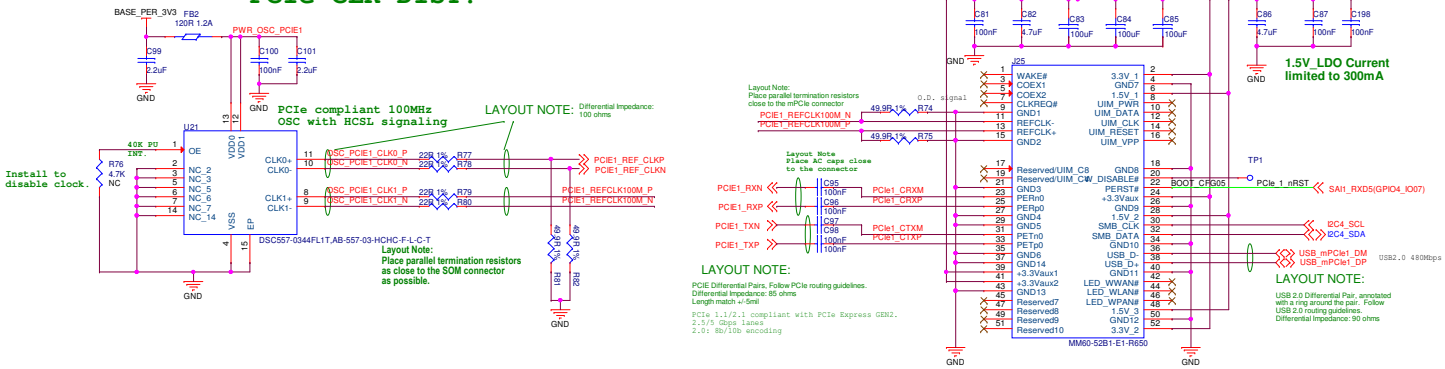
Variscite

Title: 06. HDMI , eDP			
Size: A3	Document Number: VAR-DT8MCustomBoard	Project: VAR-DT8MCustomBoard	Rev: 1.1_R2
Designer: Oded A.		Approved By: <Approved By>	
Date: Tuesday, March 13, 2018		Sheet 6 of 12	

mPCIexp CS

PCIe CLK DIST.

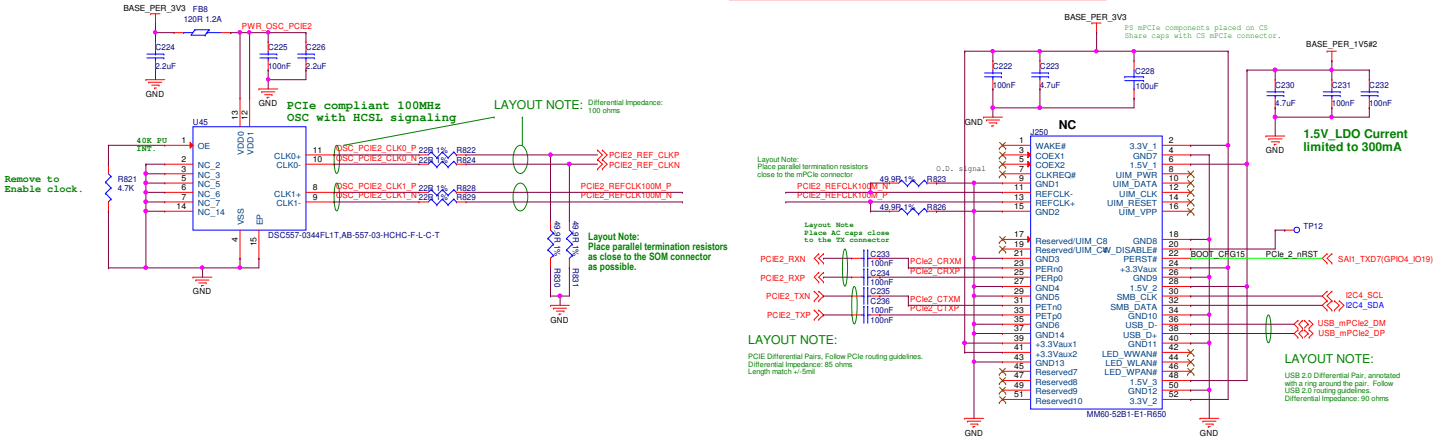
Customboard 5V power supply is limited to 3A, shared with Board's USB devices. Do not connect devices which exceed current limitation.



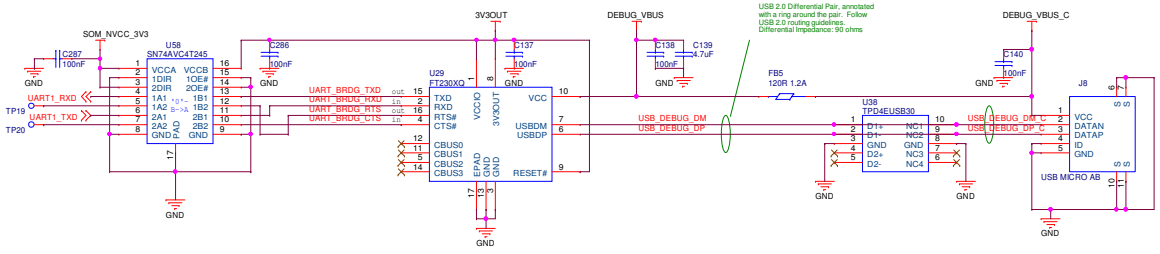
mPCIexp ON PS

PCIe CLK DIST.

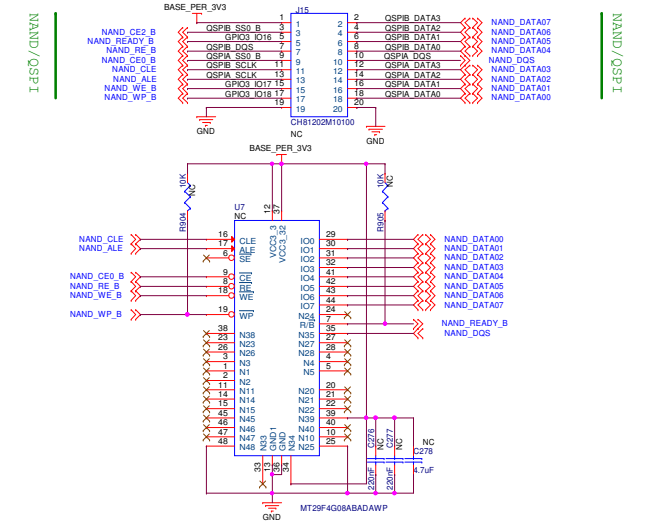
Customboard 5V power supply is limited to 3A, shared with Board's USB devices. Do not connect devices which exceed current limitation.



USB UART DEBUG



NAND+HEADER ON PS



Title: 07. PCIe, NAND, USB DEBUG			
Size: A2	Document Number: VAR-DT8MCustomBoard	Project:	Rev: 1.1_R2
Designer: Oded A.		Approved By:	<Approved By>
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08. USB TYPE C, USB 3 HUB

USB#1

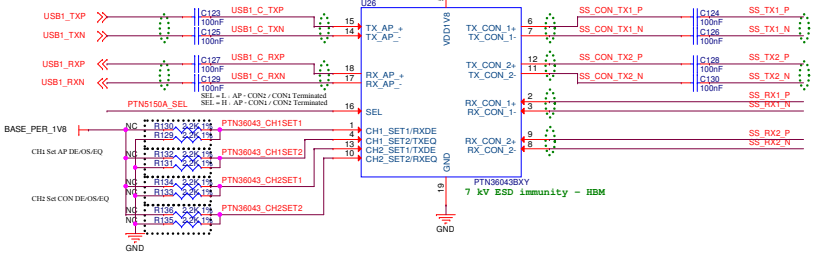
USB TYPE C OTG

LAYOUT NOTE:
USB 3.0 Differential Pair, annotated with a dashed ring around the pair.
Follow USB 3.0 routing guidelines.
Differential Impedance: 90 ohms

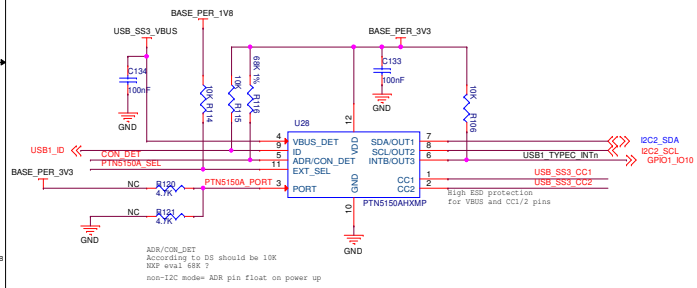
Active Demux

USB3 SIGNALS

Place AC-coupling CAPs closer to transmit side.

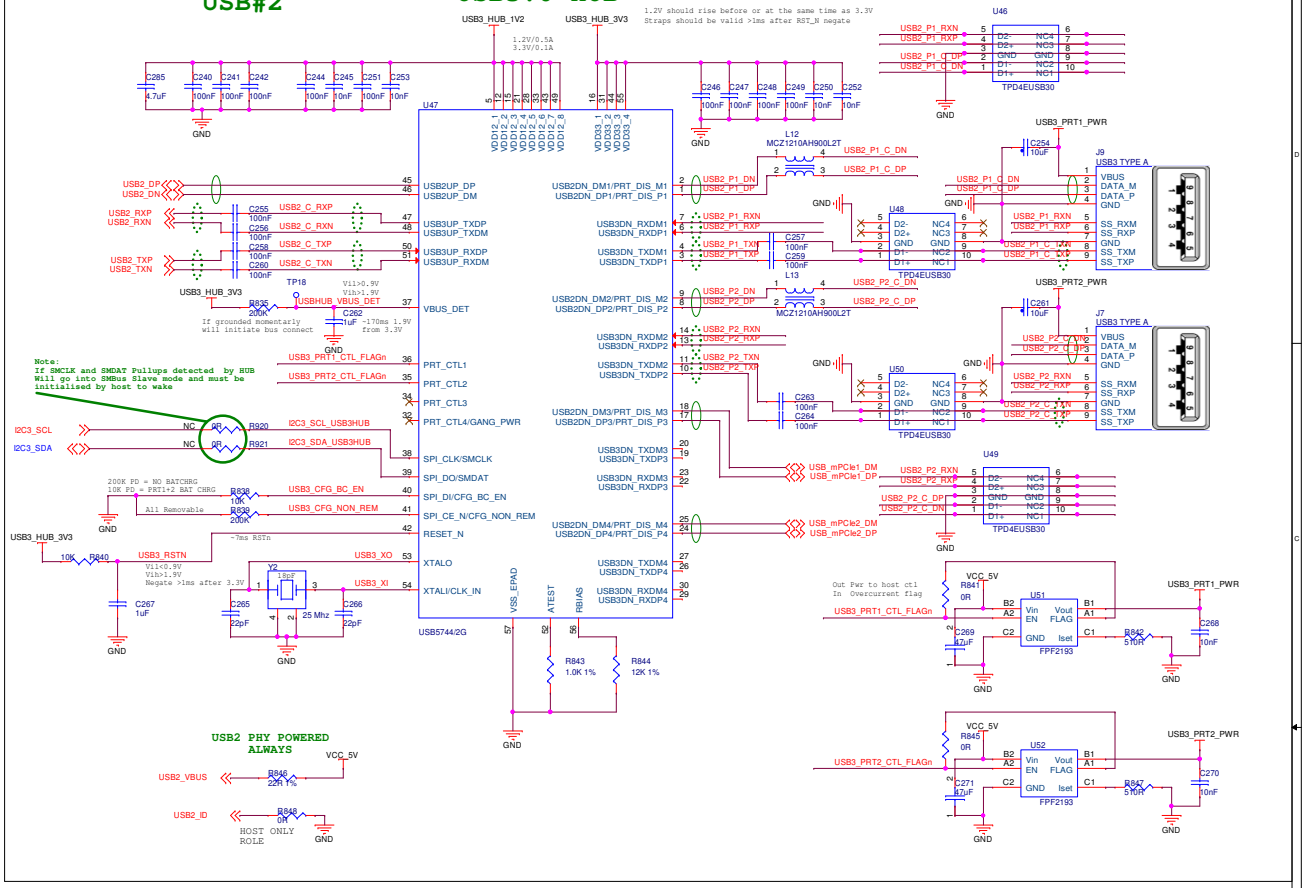


Config Channel Logic Detection & Indication of Plug Orientation

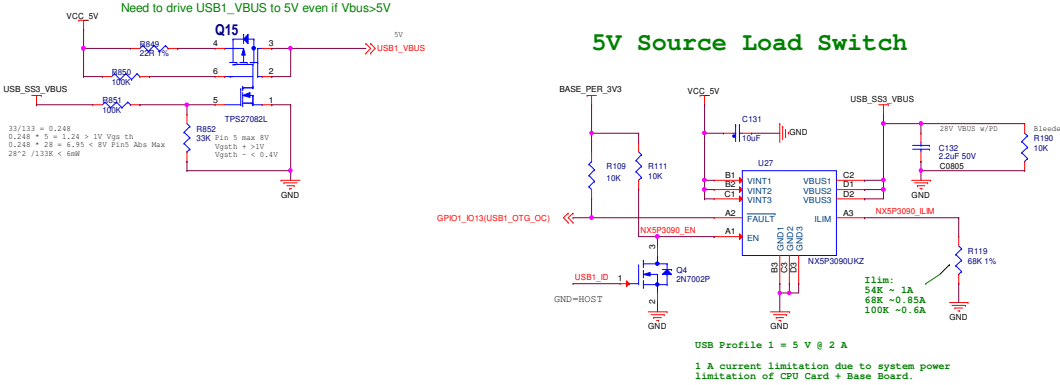


USB#2

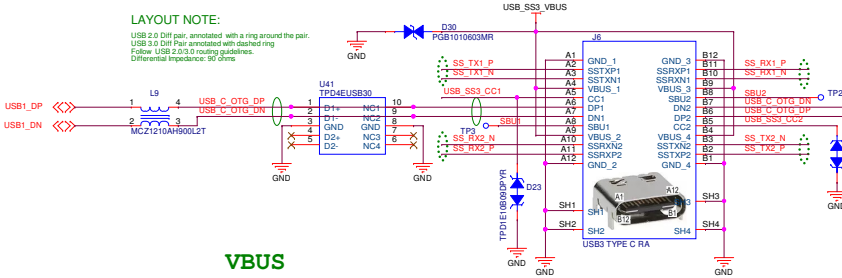
USB3.0 HUB



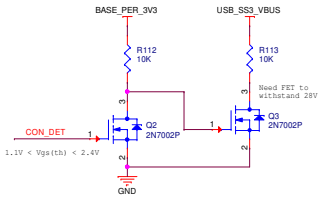
5V Source Load Switch



USB TYPE C OTG



VBUS DISCHARGE

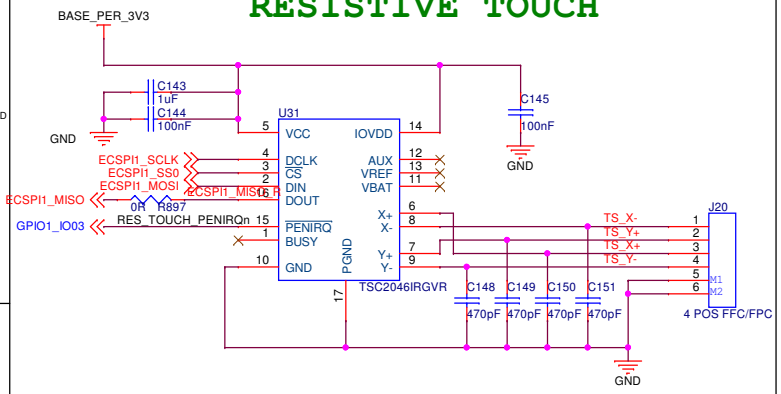


Variscite

Title: 08. USB TYPE C, USB3 HUB			
Size: A2	Document Number: VAR-DT8MCustomBoard	Project: VAR-DT8MCustomBoard	Rev: 1.1_R2
Designer: Oded A.		Approved By:	
Date: Tuesday, March 13, 2018		Sheet 8 of 12	

09. LVDS, TOUCH, JTAG, GP SW & LEDs

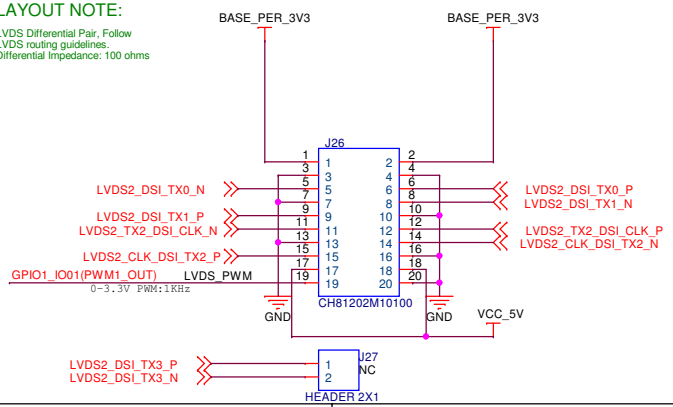
RESISTIVE TOUCH



LVDS CH1 DISPLAY

LAYOUT NOTE:

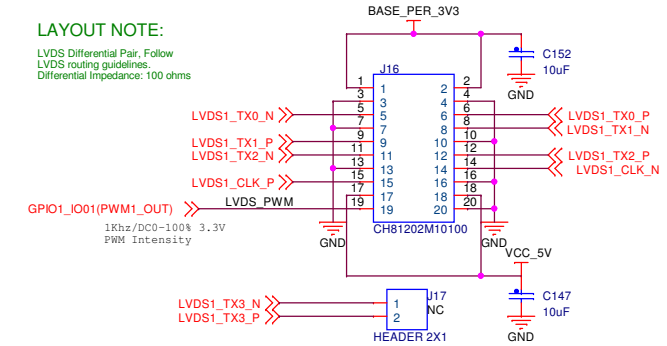
LVDS Differential Pair, Follow LVDS routing guidelines. Differential Impedance: 100 ohms



LVDS DISPLAY CH0

LAYOUT NOTE:

LVDS Differential Pair, Follow LVDS routing guidelines. Differential Impedance: 100 ohms

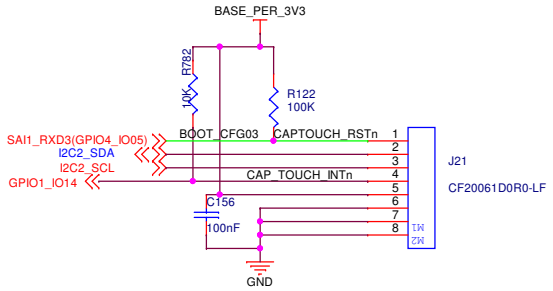


Remarks

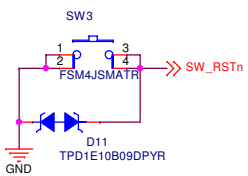
LVDS display running w/3 lanes referred as miniLVDS

LCD: GKTW70SDAE4SE
5V/0.45A
3.3V/0.17A

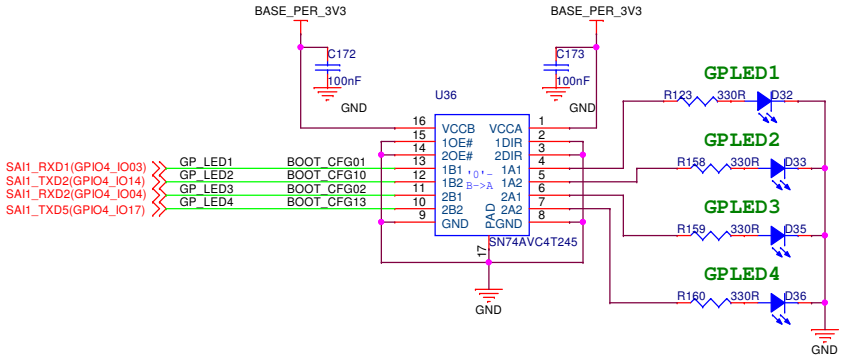
CAPACITIVE TOUCH



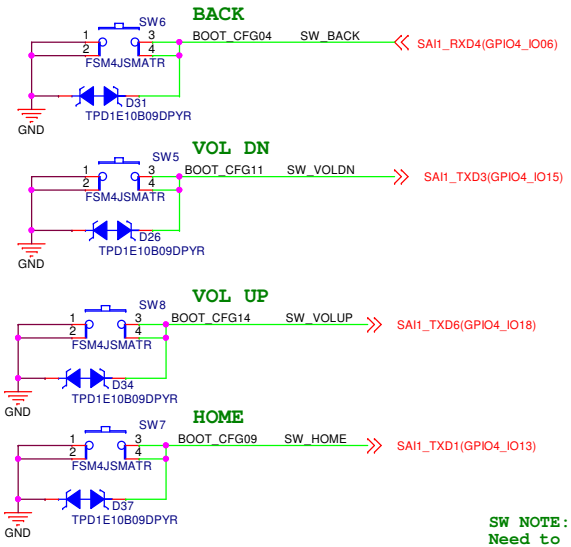
RST



GP LEDS

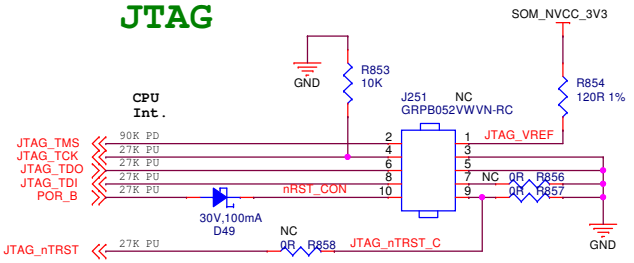


GP BUTTONS



SW NOTE:
Need to set Int. PU in SOC on all SWitches

JTAG



The new 10 pin smaller connector is now becoming an industry standard.

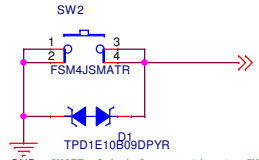
The ARM DStream comes with a 10-pin connector. If you need a ribbon, they can be purhased at Digikey:
Samtec Inc MPN: FFSD-05-D-04.00-01-N

If you need to expand to a 20-pin connector for a different JTAG device, the expander board can also be purchased at Digikey:
Olimex LTD MPN: ARM-JTAG-20-10

https://www.digikey.com/products/en/development-boards-kits-programmers/accessories/783?k=JTAG%20adapter

ON/OFF

PU Included on SOM



ONOFF: A brief connection to GND in OFF mode causes the internal power management state machine to change state to ON. In ON mode, a brief connection to GND generates an interrupt (intended to initiate a software-controllable power-down). An approximate 5 second or more connection to GND causes a forced OFF.

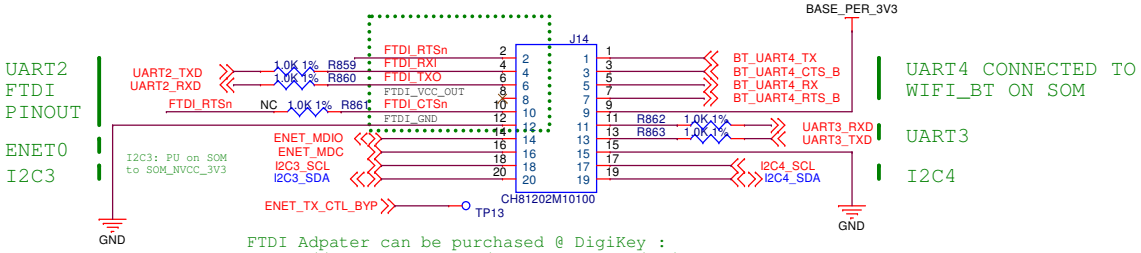
Not used leave NC

Variscite

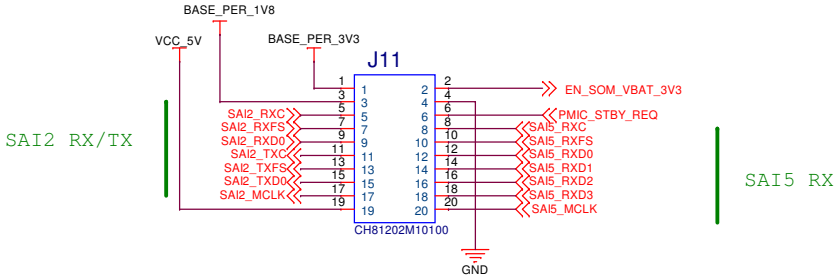
Title	09. LVDS, TOUCH, JTAG, GP SW & LEDs		
Size A3	Document Number VAR-DT8MCustomBoard	Project VAR-DT8MCustomBoard	Rev 1.1_R2
Designer: Oded A.		Approved By:	
Date: Tuesday, March 13, 2018		Sheet 9 of 12	

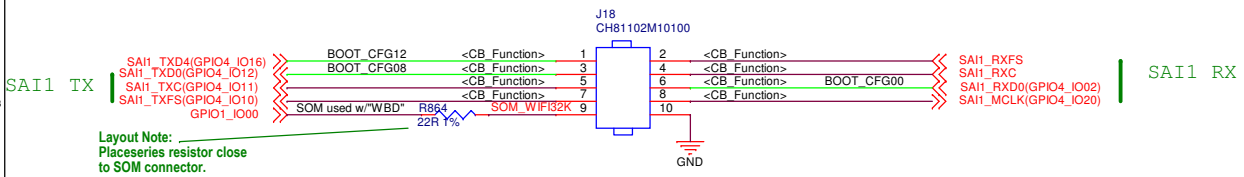
10. HEADERS, Pull Ups

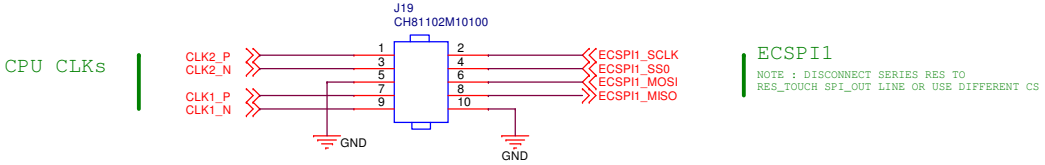
3.3V HEADERS

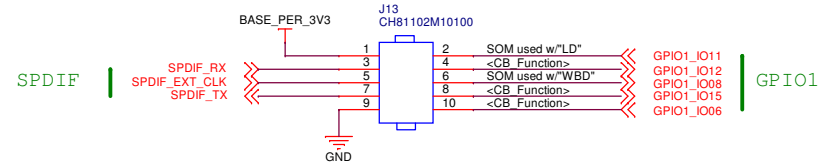


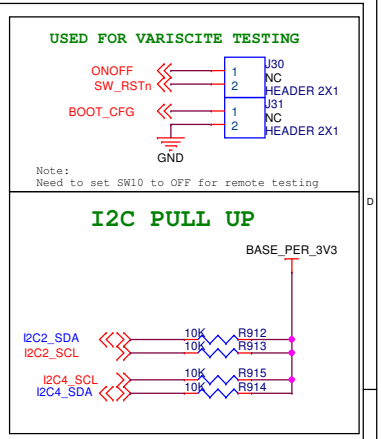
FTDI Adpater can be purchased @ DigiKey :
https://www.digikey.com/product-detail/en/ftdi-future-technology-devices-international-ltd/TTL-232R-3V3/768-1015-ND/1836393
See pinout: http://www.ftdichip.com/Support/Documents/DataSheets/Cables/DS_TTL-232R_CABLES.pdf



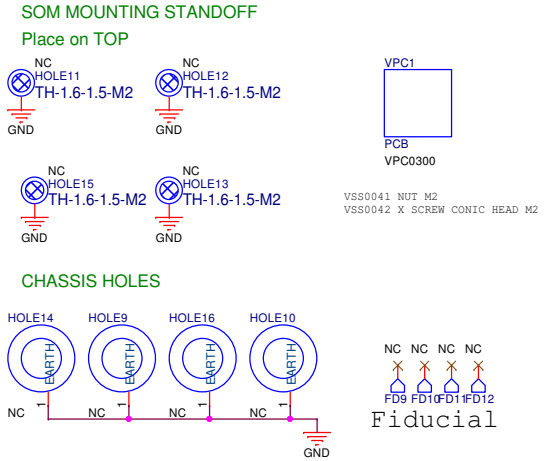








MECHANICS



Variscite

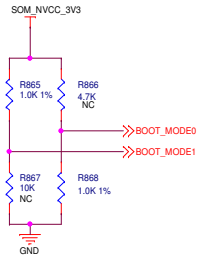
Title: 10. HEADERS, Mechanics, Pull Ups			
Size: A3	Document Number: VAR-DT8MCustomBoard	Project: VAR-DT8MCustomBoard	Rev: 1.1_R2
Designer: Oded A.		Approved By:	
Date: Tuesday, March 13, 2018		Sheet 10 of 12	

11. BOOT CONFIG & MODE

	Address	7	6	5	4	3	2	1	0
	0x470[15:8]	BOOT_CFG[15]	BOOT_CFG[14]	BOOT_CFG[13]	BOOT_CFG[12]	BOOT_CFG[11]	BOOT_CFG[10]	BOOT_CFG[9]	BOOT_CFG[8]
	0x470[15:8]	Infinit-Loop (Debug USE only) 0 - Disable 1 - Enable	0 01 - SD/eSD			Port Select: 0 0 - eSDHC1 - INT eMMC 0 1 - eSDHC2 - EXT		Power Cycle Enable '0' - No power cycle '1' - Enabled via	SD Loopback Clock Source Sel (for SDR50 and SDR104 only) '0' - through SD pad '1' - direct
	0x470[15:8]		0 10 - MMC/eMMC						
	0x470[15:8]		011 - NAND			Pages In Block: 00 - 128 01 - 64 10 - 32 11 - 256		Nand_Row_address_bytes: 00 - 3 01 - 2 10 - 4 11 - 5	
	0x470[15:8]		100 - QSPI			QSPI Instance 0 - QuadSPI0 1 - Reserved	SDR SMP: "000" - Default "001-111"		
	0x470[15:8]		110 - SPI NOR			Port Select: 000 - eCSPI1 001 - eCSPI2			SPI Addressing: 0 - 3-bytes (24-bit) 1 - 2-bytes (16-bit)
	0x470[15:8]	Others - Reserved for future use							

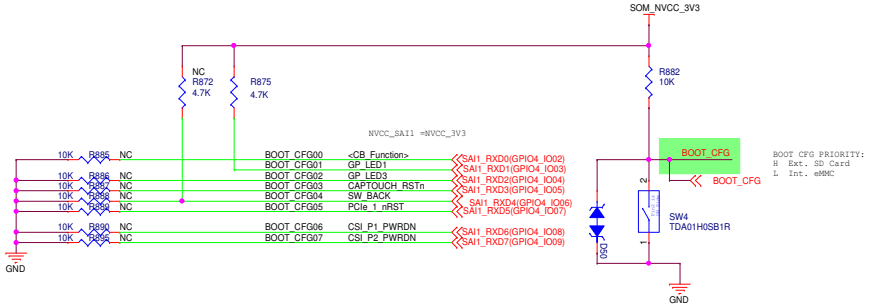
		BOOT_CFG[7]	BOOT_CFG[6]	BOOT_CFG[5]	BOOT_CFG[4]	BOOT_CFG[3]	BOOT_CFG[2]	BOOT_CFG[1]	BOOT_CFG[0]
SD/eSD	0x470[7:0]	Fast Boot: 0 - Regular 1 - Fast Boot	Reserved	Reserved	Bus Width: 0 - 1-bit 1 - 4-bit	Speed 000 - Normal/SDR12 001 - High/SDR25 010 - SDR50 011 - SDR104 101 - Reserved for DDR50 Others - Reserved			Reserved
MMC/eMMC	0x470[7:0]		Bus Width: 000 - 1-bit 001 - 4-bit 010 - 8-bit 101 - 4-bit DDR (MMC 4.4) 110 - 8-bit DDR (MMC 4.4) Else - reserved.			Speed 00 - Normal 01 - High 10 - Reserved for HS200 11 - Reserved		USDHC1 IO VOLTAGE SELECTION 0 - 3.3V 1 - 1.8V	USDHC2 IO VOLTAGE SELECTION 0 - 3.3V 1 - 1.8V
NAND	0x470[7:0]	BT_TOGGLEMODE	BOOT_SEARCH_COUNT: 00 - 2 01 - 2 10 - 4 11 - 8		Toggle Mode 33MHz Preamble Delay, Read Latency: '000' - 16 GPMICLK cycles. '001' - 1 GPMICLK cycles. '010' - 2 GPMICLK cycles. '011' - 3 GPMICLK cycles. '100' - 4 GPMICLK cycles. '101' - 5 GPMICLK cycles. '110' - 6 GPMICLK cycles. '111' - 7 GPMICLK cycles. '1111'- 15 GPMICLK cycles.			Reserved
QSPI	0x470[7:0]	HSPHS: Half Speed Phase Selection 0 : select sampling at non-inverted clock 1: select sampling at inverted clock	HSDLY: Half Speed Delay selection 0 : one clock delay 1: two clock delay	FSPHS: Full Speed Phase Selection 0 : select sampling at non-inverted clock 1: select sampling at inverted clock	FSDLY: Full Speed Delay selection 0 : one clock delay 1: two clock delay	Reserved	Reserved	Reserved	Reserved
SPINOR	0x470[7:0]	CS select (SPI only): 00 - CS#0 (default) 01 - CS#1 10 - CS#2 11 - CS#3		Reserved	Reserved	Reserved	Reserved	Reserved	Reserved

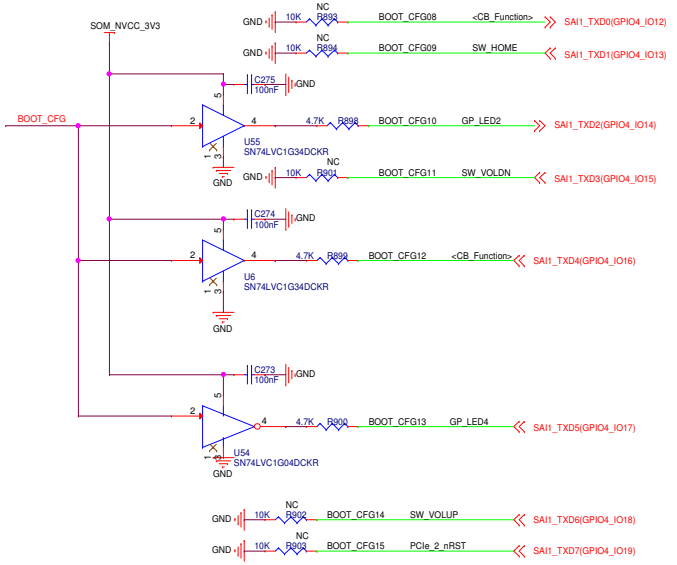
BMODE[1:0]	BOOT TYPE
00	Boot From Fuses
01	Serial Downloader
10	Internal Boot (Development)
11	Reserved



Notes:

a. Sampled on rising edge of POR_B
b. 95K ohm Int. SOC PD during POR_B and after on BOOT CFG[15:0] and BOOTMODE[1:0]
c. BMODE[1:0] ="10" is Int. Boot
d. Active boot cfg for one dip sw sel SD/eMMC
e. Yellow marks default setting
f. Orange marks must setting





Title	11. BOOT CONFIG & MODE		
Size C	Document Number VAR-DT8MCustomBoard		Rev 1.1_R2
Date: Tuesday, March 13, 2018	Sheet 11 of 12		

12. PINMUX J1 & J2 & J3

J1

	ALT0	ALT1	ALT2	ALT3	ALT5	ALT6	ALT IC	CB_FUNCTION
NAND_DATA00	NAND_DATA00	QSPIA_DATA0			GPIO3_IO06			
NAND_DATA01	NAND_DATA01	QSPIA_DATA1			GPIO3_IO07			
NAND_DATA02	NAND_DATA02	QSPIA_DATA2			GPIO3_IO08			
NAND_DATA03	NAND_DATA03	QSPIA_DATA3			GPIO3_IO09			
NAND_DATA04	NAND_DATA04	QSPIB_DATA0			GPIO3_IO10			
NAND_DATA05	NAND_DATA05	QSPIB_DATA1			GPIO3_IO11			
NAND_DATA06	NAND_DATA06	QSPIB_DATA2			GPIO3_IO12			
NAND_DATA07	NAND_DATA07	QSPIB_DATA3			GPIO3_IO13			
NAND_CE0_B	NAND_CE0_B	QSPIA_SS0_B			GPIO3_IO01			
NAND_CE2_B	NAND_CE2_B	QSPIB_SS0_B			GPIO3_IO03			
NAND_DQS	NAND_DQS	QSPIA_DQS			GPIO3_IO14			
NAND_ALE	NAND_ALE	QSPIA_SCLK			GPIO3_IO00			
NAND_WP_B	NAND_WP_B				GPIO3_IO18			
NAND_WE_B	NAND_WE_B				GPIO3_IO17			
NAND_RE_B	NAND_RE_B	QSPIB_DQS			GPIO3_IO15			
NAND_CLE	NAND_CLE	QSPIB_SCLK			GPIO3_IO05			
NAND_READY_B	NAND_READY_B				GPIO3_IO16			
CONN_SD2_CLK	SD2_CLK				GPIO2_IO13			
CONN_SD2_DATA0	SD2_DATA0				GPIO2_IO15			
CONN_SD2_DATA1	SD2_DATA1				GPIO2_IO16			
CONN_SD2_DATA2	SD2_DATA2				GPIO2_IO17			
CONN_SD2_DATA3	SD2_DATA3				GPIO2_IO18			
CONN_SD2_CMD	SD2_CMD				GPIO2_IO14			
CONN_SD2_CD_B	SD2_CD_B				GPIO2_IO12			
CONN_SD2_nRST	SD2_RESET_B				GPIO2_IO19			
ETH_TRX0_N	ENET_TD2				GPIO1_IO19		ETH_TRX0_N	
ETH_TRX0_P	ENET_TD3				GPIO1_IO18		ETH_TRX0_P	
ETH_TRX1_N	ENET_TD0				GPIO1_IO21		ETH_TRX1_N	
ETH_TRX1_P	ENET_TD1				GPIO1_IO20		ETH_TRX1_P	
ETH_TRX2_N	ENET_RD1				GPIO1_IO27		ETH_TRX2_N	
ETH_TRX2_P	ENET_RD0				GPIO1_IO26		ETH_TRX2_P	
ETH_TRX3_N	ENET_RD3				GPIO1_IO29		ETH_TRX3_N	
ETH_TRX3_P	ENET_RD2				GPIO1_IO28		ETH_TRX3_P	
ENET_TX_CTL_BYP	ENET_TX_CTL				GPIO1_IO22		NOT_CONNECTED	
LED_LINK10_100	ENET_TXC				GPIO1_IO23		LED_LINK10_100	
LED_LINK1000	ENET_RXC				GPIO1_IO25		LED_LINK1000	
LED_ACT	ENET_RX_CTL				GPIO1_IO24		LED_ACT	
ENET_MDIO	ENET_MDIO				GPIO1_IO17			SOM used w/"EC"
ENET_MDC	ENET_MDC				GPIO1_IO16			SOM used w/"EC"
GPIO1_IO00	GPIO1_IO00				REF_CLK_32K			SOM used w/"WBD"
I2C4_SCL	I2C4_SCL	PWM2_OUT	PCIE1_CLKREQ_B		GPIO5_IO20			
I2C4_SDA	I2C4_SDA	PWM1_OUT	PCIE2_CLKREQ_B		GPIO5_IO21			

J2

HPLOUT	SAI3_TXD	GPT1_COMPARE3	SAI5_RXD3		GPIO5_IO01		HPLOUT	
HPROUT	SAI3_TXC	GPT1_COMPARE2	SAI5_RXD2		GPIO5_IO00		HPROUT	
HPOUTFB	SAI3_RXFS	GPT1_CAPTURE1	SAI5_RXFS		GPIO4_IO28		HPOUTFB	
LINEIN1_LP	SAI3_RXC	GPT1_CAPTURE2	SAI5_RXC		GPIO4_IO29		LINEIN1_LP	
LINEIN1_RP	SAI3_TXFS	GPT1_CLK	SAI5_RXD1		GPIO4_IO31		LINEIN1_RP	
DMIC_CLK	SAI3_RXD	GPT1_COMPARE1	SAI5_RXD0		GPIO4_IO30		DMIC_CLK	
DMIC_DATA	SAI3_MCLK	PWM4_OUT	SAI5_MCLK		GPIO5_IO02		DMIC_DATA	
	ECSPI2_MOSI	UART4_TXD			GPIO5_IO11			SOM used w/"WBD"
BT_UART4_TX	ECSPI2_MISO	UART4_CTS_B			GPIO5_IO12			SOM used w/"WBD"
BT_UART4_CTS_B	ECSPI2_SCLK	UART4_RXD			GPIO5_IO10			SOM used w/"WBD"
BT_UART4_RX	ECSPI2_SS0	UART4_RTS_B			GPIO5_IO13			SOM used w/"WBD"
BT_UART4_RTS_B	GPIO1_IO02	WDOG_B						
GPIO1_IO02(nWDOG)								
I2C2_SDA	I2C2_SDA	ENET_1588_EVENT1_OUT			GPIO5_IO17			
I2C2_SCL	I2C2_SCL	ENET_1588_EVENT1_IN			GPIO5_IO16			
ECSPI1_SCLK	ECSPI1_SCLK	UART3_RX			GPIO5_IO06			
ECSPI1_SS0	ECSPI1_SS0	UART3_RTS_B			GPIO5_IO09			
ECSPI1_MISO	ECSPI1_MISO	UART3_CTS_B			GPIO5_IO08			
ECSPI1_MOSI	ECSPI1_MOSI	UART3_TX			GPIO5_IO07			
UART1_RXD	UART1_RXD	ECSPI3_SCLK			GPIO5_IO22			
UART1_TXD	UART1_TXD	ECSPI3_MOSI			GPIO5_IO23			
UART2_RXD	UART2_RXD	ECSPI3_MISO			GPIO5_IO24			
UART2_TXD	UART2_TXD	ECSPI3_SS0			GPIO5_IO25			
UART3_RXD	UART3_RXD	UART1_CTS_B			GPIO5_IO26			
UART3_TXD	UART3_TXD	UART1_RTS_B			GPIO5_IO27			
SAI2_MCLK	SAI2_MCLK	SAI5_MCLK			GPIO4_IO27			
SAI2_RXFS	SAI2_RXFS	SAI5_TXFS			GPIO4_IO21			
SAI2_RXC	SAI2_RXC	SAI5_TXC			GPIO4_IO22			
SAI2_TXFS	SAI2_TXFS	SAI5_TXD1			GPIO4_IO24			
SAI2_TXC	SAI2_TXC	SAI5_TXD2			GPIO4_IO25			
SAI2_RXD0	SAI2_RXD0	SAI5_TXD0			GPIO4_IO23			
SAI2_TXD0	SAI2_TXD0	SAI5_TXD3			GPIO4_IO26			
SAI5_MCLK	SAI5_MCLK	SAI1_TXC	SAI4_MCLK		GPIO3_IO25			
SAI5_RXFS	SAI5_RXFS	SAI1_TXD0			GPIO3_IO19			
SAI5_RXC	SAI5_RXC	SAI1_TXD1			GPIO3_IO20			
SAI5_RXD0	SAI5_RXD0	SAI1_TXD2			GPIO3_IO21			
SAI5_RXD1	SAI5_RXD1	SAI1_TXD3	SAI1_TXFS	SAI5_TXFS	GPIO3_IO22			
SAI5_RXD2	SAI5_RXD2	SAI1_TXD4	SAI1_TXFS	SAI5_TXC	GPIO3_IO23			
SAI5_RXD3	SAI5_RXD3	SAI1_TXD5	SAI1_TXFS	SAI5_TXD0	GPIO3_IO24			
SAI1_MCLK(GPIO4_IO20)	SAI1_MCLK	SAI5_MCLK	SAI1_TXC		GPIO4_IO20			
SAI1_RXFS	SAI1_RXFS	SAI5_RXFS			GPIO4_IO00			
SAI1_RXC	SAI1_RXC	SAI5_RXC			GPIO4_IO01			
SAI1_TXFS(GPIO4_IO10)	SAI1_TXFS	SAI5_TXFS			GPIO4_IO10			
SAI1_TXC(GPIO4_IO11)	SAI1_TXC	SAI5_TXC			GPIO4_IO11			
SAI1_RXD0(GPIO4_IO02)	SAI1_RXD0	SAI5_RXD0			GPIO4_IO02	BOOT_CFG00		
SAI1_RXD1(GPIO4_IO03)	SAI1_RXD1	SAI5_RXD1			GPIO4_IO03	BOOT_CFG01		GP_LED1
SAI1_RXD2(GPIO4_IO04)	SAI1_RXD2	SAI5_RXD2			GPIO4_IO04	BOOT_CFG02		GP_LED3
SAI1_RXD3(GPIO4_IO05)	SAI1_RXD3	SAI5_RXD3			GPIO4_IO05	BOOT_CFG03		CAPTOUCH_RSTn
SAI1_RXD4(GPIO4_IO06)	SAI1_RXD4	SAI6_TXC	SAI6_RXC		GPIO4_IO06	BOOT_CFG04		SW_BACK
SAI1_RXD5(GPIO4_IO07)	SAI1_RXD5	SAI6_TXD0	SAI6_RXD0	SAI1_RXFS	GPIO4_IO07	BOOT_CFG05		PCIe_1_nRST
SAI1_RXD6(GPIO4_IO08)	SAI1_RXD6	SAI6_TXFS	SAI6_RXFS		GPIO4_IO08	BOOT_CFG06		CSI_P1_PWRDN
SAI1_RXD7(GPIO4_IO09)	SAI1_RXD7	SAI6_MCLK	SAI1_TXFS	SAI1_TXD4	GPIO4_IO09	BOOT_CFG07		CSI_P2_PWRDN
SAI1_TXD0(GPIO4_IO12)	SAI1_TXD0	SAI5_TXD0			GPIO4_IO12	BOOT_CFG08		
SAI1_TXD1(GPIO4_IO13)	SAI1_TXD1	SAI5_TXD1			GPIO4_IO13	BOOT_CFG09		SW_HOME
SAI1_TXD2(GPIO4_IO14)	SAI1_TXD2	SAI5_TXD2			GPIO4_IO14	BOOT_CFG10		GP_LED2
SAI1_TXD3(GPIO4_IO15)	SAI1_TXD3	SAI5_TXD3			GPIO4_IO15	BOOT_CFG11		SW_VOLDN
SAI1_TXD4(GPIO4_IO16)	SAI1_TXD4	SAI6_RXC	SAI6_TXC		GPIO4_IO16	BOOT_CFG12		
SAI1_TXD5(GPIO4_IO17)	SAI1_TXD5	SAI6_RXD0	SAI6_TXD0		GPIO4_IO17	BOOT_CFG13		GP_LED4
SAI1_TXD6(GPIO4_IO18)	SAI1_TXD6	SAI6_RXFS	SAI6_TXFS		GPIO4_IO18	BOOT_CFG14		SW_VOLUP
SAI1_TXD7(GPIO4_IO19)	SAI1_TXD7	SAI6_MCLK			GPIO4_IO19	BOOT_CFG15		PCIe_2_nRST

J3

UART4_TXD(GPIO5_IO29)	UART4_TXD	UART2_RTS_B	PCIE2_CLKREQ_B		GPIO5_IO29			CSI_P2_RSTN
UART4_RXD(GPIO5_IO28)	UART4_RXD	UART2_CTS_B	PCIE1_CLKREQ_B		GPIO5_IO28			CSI_P1_RSTN
SPDIF_RX	SPDIF_RX	PWM2_OUT			GPIO5_IO04			
SPDIF_TX	SPDIF_TX	PWM3_OUT			GPIO5_IO03			
SPDIF_EXT_CLK	SPDIF_EXT_CLK	PWM1_OUT			GPIO5_IO05			SOM used w/"WBD"
I2C3_SDA	I2C3_SDA	PWM3_OUT	GPT3_CLK		GPIO5_IO19			
I2C3_SCL	I2C3_SCL	PWM4_OUT	GPT2_CLK		GPIO5_IO18			
GPIO1_IO01(PWM1_OUT)	GPIO1_IO01	PWM1_OUT			REF_CLK_24M	EXT_CLK2		LVDS_PWM
GPIO1_IO03	GPIO1_IO03	USDHC1_VSELECT				XTAL_OK		RES_TOUCH_PENIRQn
GPIO1_IO05	GPIO1_IO05	M4_NMI			PMIC_READY			HDMI_SW_GPU_SEL
GPIO1_IO06	GPIO1_IO06				SD1_CD_B	EXT_CLK3		<CB_Function>
GPIO1_IO08	GPIO1_IO08	ENET_1588_EVENT0_IN			SD2_RESET_B			SOM used w/"WBD"
GPIO1_IO10	GPIO1_IO10	USB1_OTG_ID						USB1_TYPEC_INTn
GPIO1_IO11	GPIO1_IO11	USB2_OTG_ID			PMIC_READY			SOM used w/"LP"
GPIO1_IO12	GPIO1_IO12	USB1_OTG_PWR						
GPIO1_IO13(USB1_OTG_OC)	GPIO1_IO13	USB1_OTG_OC			PWM2_OUT			
GPIO1_IO14	GPIO1_IO14	USB2_OTG_PWR			PWM3_OUT			CAP_TOUCH_INTn
GPIO1_IO15	GPIO1_IO15	USB2_OTG_OC			PWM4_OUT	CLKO2		
	DSI_TX2_P						LVDS2_CLK_P	
LVDS2_CLK_DSI_TX2_P	DSI_TX2_N						LVDS2_CLK_N	
LVDS2_CLK_DSI_TX2_N	DSI_TX0_P						LVDS2_TX0_P	
LVDS2_DSI_TX0_P	DSI_TX0_N						LVDS2_TX0_N	
LVDS2_DSI_TX0_N	DSI_TX1_P						LVDS2_TX1_P	
LVDS2_DSI_TX1_P	DSI_TX1_N						LVDS2_TX1_N	
LVDS2_DSI_TX1_N	DSI_CLK_P						LVDS2_TX2_P	
LVDS2_TX2_DSI_CLK_P	DSI_CLK_N						LVDS2_TX2_N	
LVDS2_TX2_DSI_CLK_N	DSI_TX3_P						LVDS2_TX3_P	
LVDS2_DSI_TX3_P	DSI_TX3_N						LVDS2_TX3_N	
LVDS2_DSI_TX3_N								
LVDS1_CLK_P	NOT_CONNECTED						LVDS1_CLK_P	
LVDS1_CLK_N	NOT_CONNECTED						LVDS1_CLK_N	
LVDS1_TX0_P	NOT_CONNECTED						LVDS1_TX0_P	
LVDS1_TX0_N	NOT_CONNECTED						LVDS1_TX0_N	
LVDS1_TX1_P	NOT_CONNECTED						LVDS1_TX1_P	
LVDS1_TX1_N	NOT_CONNECTED						LVDS1_TX1_N	
LVDS1_TX2_P	NOT_CONNECTED						LVDS1_TX2_P	
LVDS1_TX2_N	NOT_CONNECTED						LVDS1_TX2_N	
LVDS1_TX3_P	NOT_CONNECTED						LVDS1_TX3_P	
LVDS1_TX3_N	NOT_CONNECTED						LVDS1_TX3_N	

NOTE:

1. ORANGE FUNCTION DENOTES FUNCTION USED ON SOME SOM WITH OPTIONAL OREDERABLE CONFIGURATIONS. PLEASE REFER TO SOM DATASHEET FOR FURTHER DETAILS.
2. ALT0 TO ALT6 DENOTE ALTERNATE FUNCTIONS OF SOC PINS WHEN USED.
3. ALT IC DENOTE AN ALTERNATE FUNCTION WHEN RELEVANT SOM ORDERABLE CONFIGURATION CHOOSEN. FUNCTION GENERATED BY ALTERNATIVE IC WHEN USED. WHEN DESIGN WITH ALT IC - ALT0 TO ALT6 CANNOT BE USED!
4. GREEN NETS DENOTE PINS USED FOR BOOT CONFIGURATION USING POWER UP. CARE SHOULD BE GIVEN NOT DRIVING THESE LINES AFTER RISE OF POR_B+1ms.

Variscite

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