VARISCITE LTD.

DART-MX8M V1.x

Datasheet

NXP i.MX 8M™ - based System-on-Module

VARISCITE LTD.

DART-MX8M Datasheet

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1. Document Revision History

Revision	Date	Notes
1.0	Feb 5, 2018	Initial
1.01	Feb 17, 2018	Pre-launch editing changes

2. Overview

2.1. General Information

The DART-MX 8M offers high-performance processing for a low-power System-on-Module. It perfectly fits various embedded products, the growing market of connected and portable devices and segment for connected streaming audio/video devices, scanning/imaging devices and various devices requiring high-performance, low-power processors.
The product is based on the NXP i.MX 8M Dual/Quad Lite/Quad family of multi-purpose processors, featuring an ARM® Cortex™-A53 up to 1.5GHz with an additional 266MHz ARM Cortex-M4 core.
This heterogeneous multicore processing architecture enables the device to run an open operating system like Linux on the Cortex-A53 core and an RTOS like FreeRTOS™ on the Cortex-M4 core for time and security critical tasks.

The DART-MX8M provides an ideal building block for simple integration with a wide range of products in target markets requiring high-performance processing with low power consumption, compact size and a very cost-effective solution.

Supporting products:

- VAR-DT8MCustomBoard – evaluation board
  - ✓ Carrier Board, compatible with DART-MX8M
  - ✓ Schematics
- VAR-DVK-MX8M full development kit, including:
  - ✓ VAR-DT8MCustomBoard
  - ✓ DART-MX8M
  - ✓ Display and touch
  - ✓ Accessories and cables
- O.S support
  - ✓ Linux BSP
  - ✓ Android

Contact Variscite support services for further information: mailto:support@variscite.com.

2.2. Feature Summary

- NXP i.MX 8M series SOC
  - i.MX 8M Dual/Quad Lite/Quad ARM® Cortex™-A53 Core 1.5GHz
  - 266MHz ARM® Cortex™-M4
  - Up to 4GB LPDDR4 RAM
  - 8-bit up to 64GB eMMC boot and storage
- Display Support
  - Dual channel LVDS display interface
  - HDMI/eDP/DP
  - MIPI DSI
- Networking
  - 10/100/1000 Mbit/s Ethernet Interface
  - Certified Wi-Fi 802.11 ac/a/b/g/n
  - Bluetooth: 4.2/BLE
- Camera
  - 2 x CSI – CMOS Serial camera Interface 4 lanes each
- Audio
  - Analog Stereo line in
  - Analog headphones out
  - Digital microphone
  - 6x Digital audio (SAI, SPDIF)
- USB
  - 2 x USB 3.0/2.0 OTG
- Other Interfaces
  - SDIO/MMC
  - 2 x PCIe v2.0
  - Serial interfaces (ECSPI, QSPI, I2C, UART, JTAG)
  - GPIOs
  - NAND Flash – Off SOM
- Single power supply: 3.4V – 4.5V
- Dimensions (W x L x H): 30 x 55 x 4.5 [mm]
- Industrial temperature range -40 to 85 °C

2.3. Block Diagram

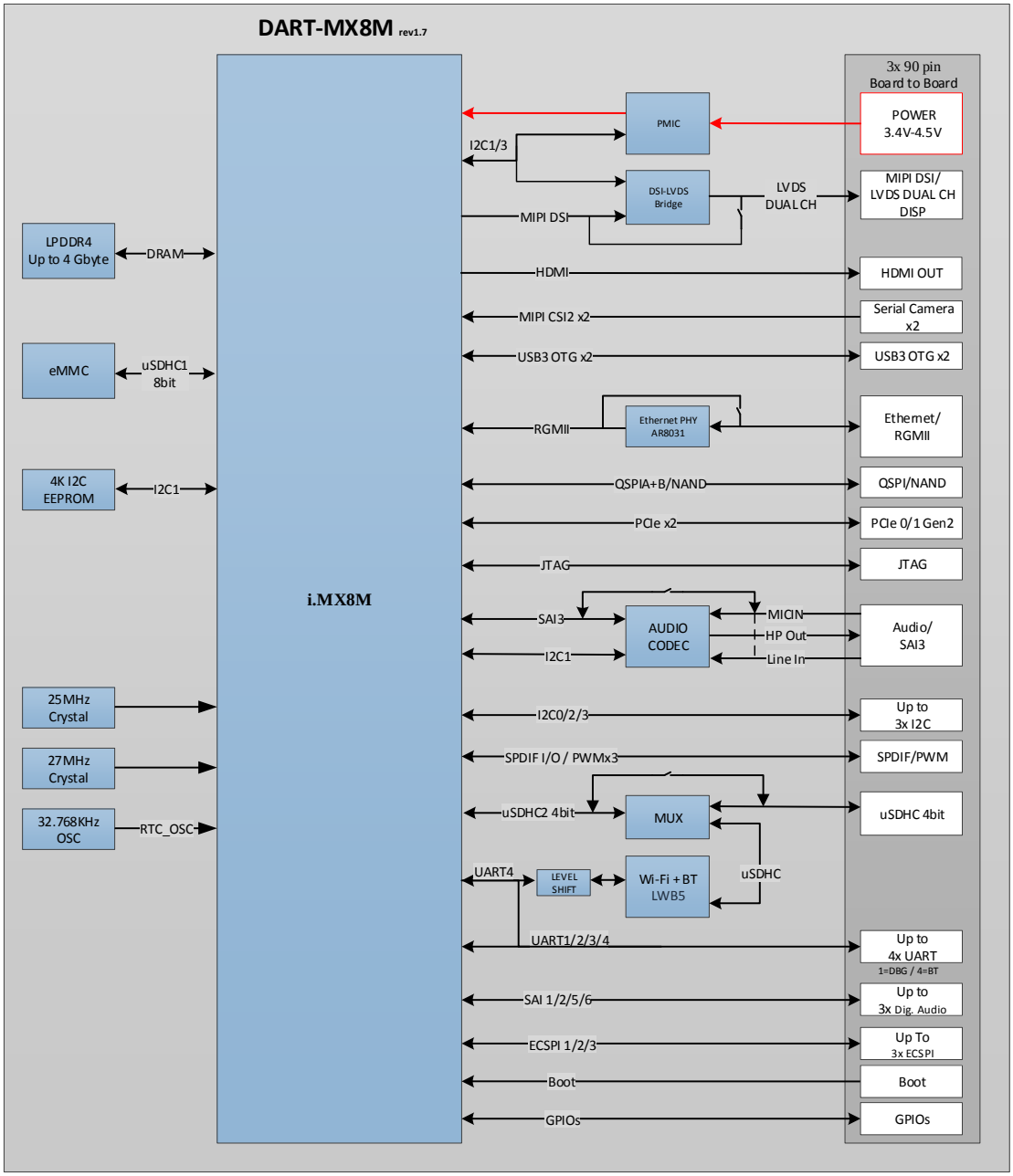

Figure 1 : DART-MX8M Block Diagram

3. Main Hardware Components

This section summarizes the main hardware building blocks of the DART-MX8M.

3.1. NXP i.MX 8M

3.1.1. Overview

The i.MX 8M Dual/8M QuadLite/8M Quad Applications Processors are the first products of the growing i.MX 8M family targeting the consumer market. They achieve both high performance and low power consumption and rely on a powerful, fully-coherent core complex based on a quad Cortex-A53 cluster, with graphics processing GPU supporting the latest graphic APIs.
The i.MX 8M family provides additional computing resources and peripherals:

- Advanced security modules for secure boot, cipher acceleration and DRM support
- General purpose Cortex-M4 processor for low power processing
- A wide range of audio interfaces including I2S, AC97, TDM and S/PDIF
- Large set of peripherals that are commonly used in consumer/industrial markets including USB 3.0, PCIe and Ethernet

3.1.2. i.MX8M Block Diagram

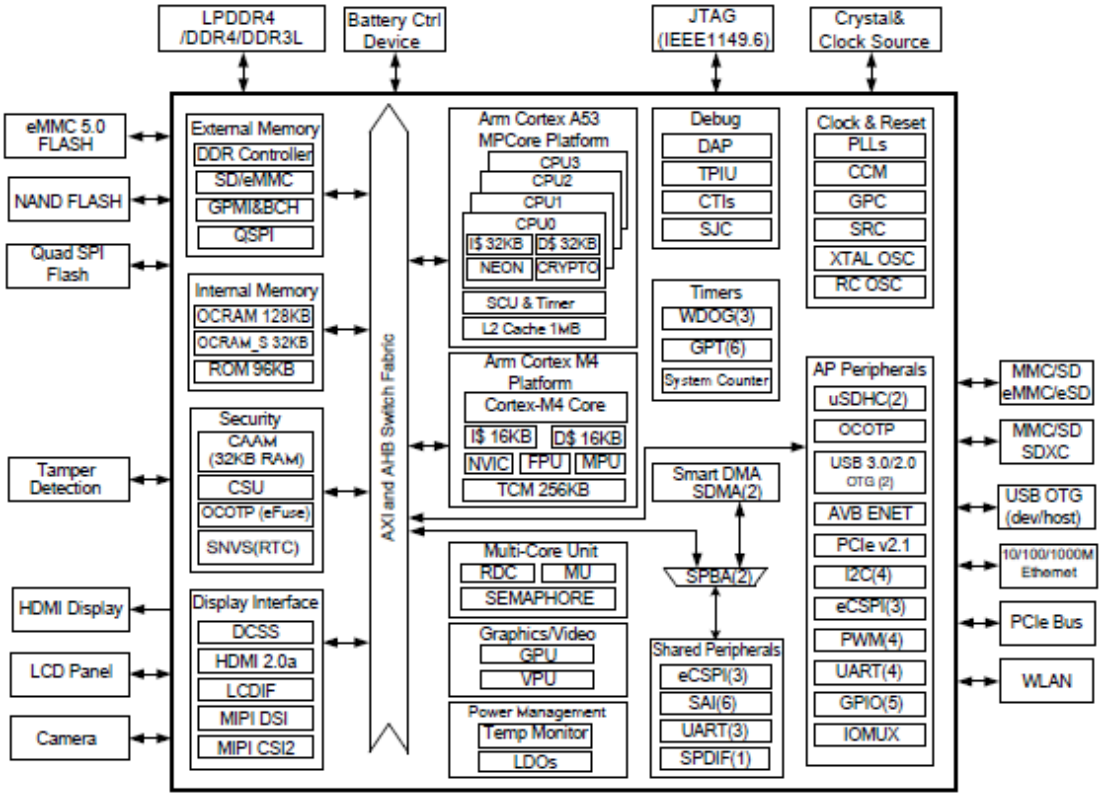

Figure 2 : iMX 8M Block Diagram

3.1.3. ARM Cortex-A53 MPCore™ Platform

The i.MX 8M family Applications Processors are based on the ARM Cortex-A53 MPCore™ platform, which has the following features:

- Quad symmetric Cortex-A53 processors, including:
  - 32KB L1 Instruction Cache
  - 32KB L1 Data Cache
  - Media Processing Engine (MPE) with NEON technology supporting the Advanced Single Instruction Multiple Data (SIMD) architecture
  - Floating Point Unit (FPU) with support of the VFPv4-D16 architecture
- Support of 64-bit ARMv8-A architecture
- 1 MB unified L2 cache
- Target frequency of 1.5GHz

3.1.4. Arm Cortex-M4 Platform

Cortex-M4 core platform includes the following:

- Low power microcontroller available for customer application:
  - Low power standby mode
  - IoT features including Weave
  - Manage IR or wireless remote

- ARM Cortex M4 CPU processor, including:
  - 16 KB L1 Instruction Cache
  - 16 KB L1 Data Cache
  - 256 KB TCM
  - Target frequency of 266MHz

3.1.5. System Bus and Interconnect

System bus and interconnect include the following:

- Network interconnect (NIC-301) AXI arbiter
- Quality of service controller (QoSC) to configure priorities and limits of AXI transactions
- Performance monitor (PERFMON) to monitor AXI bus activity
- Debug monitor (DBGMON) to record AXI transactions preceding a system reset

3.1.6. Clocking and Resets

Clocking and resets include:

- Clock control module (CCM) provides centralized clock generation and control
  - Simplified clock tree structure
  - Unified clock programming model for each clock root
  - Multicore awareness for resource domains
- System reset controller (SRC) provides reset generation and distribution

3.1.7. Interrupts and DMA

Interrupts and DMA include:

- 128 shared peripheral interrupts routed to Cortex-A53 Global Interrupt Controller (GIC) and Cortex-M4 nested vector interrupt controller (NVIC) for flexible interrupt handling
- Two Smart direct memory access (SDMA) engines. Although these two engines are identical to each other, they are integrated into the processor to serve different peripherals. Each SDMA controller supports 48 DMA requests.

3.1.8. On-Chip Memory

The on-chip memory system consists of the following:

- Boot ROM (96KB)
- On-chip RAM (128KB + 32KB)

3.1.9. External Memory Interface

The external memory interfaces supported on this chip include:

- 16/32-bit DRAM Interface: LPDDR4-3200, DDR4-2400, DDR3L-1600
- 8-bit NAND FLASH, including support for Raw MLC/SLC devices, BCH ECC up to 62-bit, and ONFi3.2 compliance (clock rates up to 100 MHz and data rates up to 200 MB/sec)
- eMMC 5.0 FLASH (2 interfaces)
- SPI NOR FLASH (3 interfaces)
- Quad SPI FLASH with support for XIP (for M4 in low-power mode) and parallel read mode of two identical FLASH devices

3.1.10. Timers

The timers on this chip include:

- One local generic timer integrated into each Cortex-A53 CPU
- Global system counter with timer bus interface to Cortex-A53 MPCore generic timers
- One local system timer (SysTick) integrated into the Cortex-M4 CPU
- Six general-purpose timer (GPT) modules
- Three watchdog timer (WDOG) modules
- Four pulse width modulation (PWM) modules

3.1.11. Graphics Processing Unit (GPU)

The chip incorporates the following Graphics Processing Unit (GPU) features:

- 4-shader
- Supports OpenGL ES 3.1, 3.0, 2.0, 1.0, OpenCL
- Target frequency of 800 MHz
- Frame Buffer Compression – Lossless compression of buffers
- TrustZone support using a local MMU to manage secure regions

3.1.12. Video Processing Unit (VPU)

The chip incorporates the following Video Processing Unit (VPU) features:

- 4Kp60 HEVC/H.265 Main, Main10 (Hantro G2) with best effort for 4Kp75
- 4Kp75 is needed to support PiP (Picture in Picture) for live TV and dual layer Dolby Vision decoding one 4Kp60 stream and one 1080p60 stream
- 4Kp60 VP9 Profile 0, 2 (10 bit) (Hantro G2)
- 4Kp30 AVC/H.264 Baseline, Main, High decoder (Hantro G1)
- 1080p60 MPEG-2, MPEG-4p2, VC-1, VP8, RV9, AVS, MJPEG, H.263 decoder (Hantro G1)
- Frame Buffer Compression – Lossless compression of buffers
- TrustZone support

3.1.13. Display Interfaces

The chip has the following display support:

- LCD Interface with MIPI-DSI Output:
    - MIPI-DSI 4 channels supporting one display with resolution up to 1920x1080p60
    - LCDIF display controller
    - Output can be LCDIF output or Display Controller output (turns off HDMI)

- Two MIPI-CSI2 Display Interfaces:
    - Each MIPI-CSI2 is 4 channels supporting one camera input. Supports 5M pixel at 15 fps, 1080p30, 720p60, VGA at 60 fps
    - Maximum bit rate of 1.5 Gbps

3.1.14. Audio

Audio include the following:

- S/PDIF Input and Output, including a new Raw Capture input mode
- Five SAI (synchronous audio interface) modules supporting I2S, AC97, TDM, and codec/DSP interfaces, including one SAI with 8x TX and 8 RX lanes, one SAI with 4x TX and 4x RX lanes, and three SAI with 1x TX and 1x RX lanes. Supports over 20x channels of audio
- One internal SAI port with 4x I2S lanes to drive HDMI audio output
- One internal S/PDIF interface to capture HDMI ARC at up to 192kHz F/s

3.1.15. General Connectivity Interfaces

The chip contains a rich set of general connectivity interfaces, including:

- Two PCI Express (PCIe):
    - Single lane supporting PCIe Gen 2
    - Dual mode operation to function as root complex or endpoint
    - Integrated PHY interface
    - Supports L1substate

- Two USB 3.0/2.0 OTG controller with integrated PHY interface
- Spread spectrum clock support
- Two Ultra Secure Digital Host Controller (uSDHC) interfaces
- MMC 5.0 compliance with HS400 DDR signaling to support up to 400 MB/sec
- SD/SDIO 3.01 compliance with 200 MHZ SDR signaling to support up to 100MB/sec
- Support for SDXC (extended capacity)
- One Gigabit Ethernet controller with support for EEE, Ethernet AVB and IEEE1588
- Four universal asynchronous receiver/transmitter (UART) modules
- Four I2C modules
- Three SPI modules

3.1.16. Security

Security functions are enabled and accelerated by the following hardware:

- RDC – Resource Domain Controller:
  - Supports 4 domains and up to 8 regions
- ARM TrustZone including the TZ architecture:
  - ARM Cortex-A53 MPCore TrustZone support
- On-chip RAM (OCRAM) secure region protection using OCRAM controller
- High Assurance Boot (HAB)
- Cryptographic Acceleration and Assurance Module (CAAM)
  - Support Widevine and PlayReady content protection
  - Public Key Cryptography (PKHA) with RSA and Elliptic Curve (ECC) algorithms
  - Real-time integrity checker (RTIC)
  - DRM support for RSA, AES, 3DES, DES
  - Side channel attack resistance
  - True random number generation (RNG)
  - Manufacturing protection support
- Secure Non-Volatile Storage(SNVS), including
  - Secure Real Time Clock (RTC)
- Secure JTAG Controller (SJC)

3.1.17. Multicore Support

Multicore support contains:

- Resource domain controller (RDC) to support isolation and safe sharing of system resources
- Messaging unit (MU)
- Hardware Semaphore (SEMA42)
- Shared bus topology

3.1.18. GPIO and Pin Multiplexing

- General-purpose input/output (GPIO) modules with interrupt capability
- Input/output multiplexing controller (IOMUXC) to provide centralized pad control

3.1.19. Power Management

The power management unit consists of:

- Temperature sensor with programmable trip points
- Flexible power domain partitioning with internal power switches to support efficient power management

3.1.20. System Debug

The system debug features are:

- ARM CoreSight debug and trace architecture
- Trace Port Interface Unit (TPIU) to support off-chip real-time trace
- Embedded Trace FIFO (ETF) with 4 KB internal storage to provide trace buffering
- Unified trace capability for Quad Cortex-A53 and Cortex-M4 CPUs
- Cross-Triggering Interface (CTI)
- Support for 5-pin (JTAG) debug interfaces

3.2. Memory

3.2.1. RAM

The DART-MX8M is available with up to 4 GB of LPDDR4 memory capable of running up to 3200MTS.

3.2.2. Non-volatile Storage Memory

The DART-MX8M is available with a non-volatile storage memory with optional densities. It is used for Flash Disk purposes, O.S. run-time-image, Boot-loader and application/user data storage.
The DART-MX8M can arrive with up to 64GB MLC eMMC

3.3. Audio (WM8904)

The WM8904 is a high performance ultra-low power stereo CODEC optimized for portable audio applications.
The device features stereo ground-referenced headphone amplifiers using the Wolfson 'Class-W' amplifier techniques. It incorporates an innovative dual-mode charge pump architecture - to optimize efficiency and power consumption during playback.
The ground-referenced headphone output eliminates AC coupling capacitors, and both outputs include common mode feedback paths to reject ground noise. Control sequences for audio path setup can be pre-loaded and executed by an integrated control write sequencer to reduce software driver development and minimize pops and clicks via SilentSwitch™ technology. The input impedance is constant with PGA gain setting. A stereo digital microphone interface is provided, with a choice of two inputs. A dynamic range controller provides compression and level control to support a wide range of portable recording applications. Anti-clip and quick release features offer good performance in the presence of loud impulsive noises. ReTuneTM Mobile 5-band parametric equalizer with fully programmable coefficients is integrated for optimization of speaker characteristics. Programmable dynamic range control is also available for maximizing loudness, protecting speakers from clipping and preventing premature shutdown due to battery droop. Common audio sampling frequencies are supported from a wide range of external clocks, either directly or generated via the FLL.

Features:

- 3.0mW quiescent power consumption for DAC to headphone playback
- DAC SNR 96dB typical, THD -86dB typical
- ADC SNR 91dB typical, THD -80dB typical
- 2.4mW quiescent power consumption for analogue bypass playback
- Control write sequencer for pop minimized start-up and shutdown
- Single register writes for default start-up sequence
- Integrated FLL provides all necessary clocks - Self-clocking modes allow processor to sleep - All standard sample rates from 8kHz to 96kHz
- Stereo digital microphone input
- 3 single ended inputs per stereo channel
- 1 fully differential mic / line input per stereo channel
- Digital Dynamic Range Controller (compressor / limiter)

- Digital sidetone mixing
- Ground-referenced headphone driver

3.4. Wi-Fi + BT (LWB5™)

The DART-MX8M contains LSR's pre-certified high-performance Sterling-LWB5™ Dual band 2.4/5 GHz Wi-Fi® and Bluetooth® Smart Ready Multi-Standard Module based upon the Cypress (formerly Broadcom) CYW43353 chipset supporting 802.11 ac/a/b/g/n, BT 2.1+EDR, and BLE 4.2 wireless connectivity.

The DART-MX8M module realizes the necessary PHY/MAC layers to support WLAN applications in conjunction with a host processor over a SDIO interface.
The modules also provide a Bluetooth/BLE platform through the HCI transport layer. Both WLAN and Bluetooth share the same antenna port.

Key Features:

- IEEE 802.11 ac/a/b/g/n
- Bluetooth 2.1+EDR, and BLE 4.2
- U.F.L connector for external antenna
- Latest Linux and Android drivers supported directly by LSR and Cypress
- SIG certified Bluetooth driver
- Wi-Fi/BT module Broad certifications with multiple antennas: FCC (USA), IC (Canada), ETSI (Europe), Giteki (Japan), and RCM (AU/NZ)
- Industrial operating Temperature Range: -40 to +85

3.5. PMIC

The DART-MX8M features Freescale/NXP's PF4210 as a Power Management Integrated circuit (PMIC) designed specifically for use with NXP's i.MX8M series of application processors. The PF4210 regulates all power rails required on SOM from a single power supply with 3.4V – 4.5V range.
The PMIC is fully programmable via the I2C interface and associated register map. Additional communication is provided by direct logic interfacing including interrupt, watchdog and reset.

3.6. 10/100/1000 Mbps Ethernet Transceiver (AR8033)

The DART-MX8M features Qualcomm Atheros AR8033 Integrated Ethernet Transceiver.
The AR8033 Ethernet transceiver requires only a single 3.3 V power supply. Embedded regulators are used to generate other required voltages. The AR8033 Ethernet transceiver integrates the termination circuitry at the line side.
The AR8033 Ethernet transceiver supports IEEE 802.3az standard. The key features include:

- 10BASE-Te/100BASE-TX/1000BASE-T IEEE 802.3 compliant
- 1000BASE-T PCS and auto-negotiation with next page support
- Green ETHOS power saving modes with internal automatic DSP power saving scheme
- IEEE 802.3az EEE
- Wake-on-LAN (WoL) to detect magic packet and notify the sleeping system to wake up

- Fully integrated digital adaptive equalizers, echo cancellers, and Near End Crosstalk (NEXT) cancellers
- Synchronous Ethernet with frequency selectable recovered clock output
- Robust Cable Discharge Event (CDE) protection of ±6 kV
- Robust operation over up to 140 meters of CAT5 cable
- Automatic Channel Swap (ACS)
- Automatic MDI/MDIX crossover
- Automatic polarity correction ν IEEE 802.3u compliant auto-negotiation
- Jumbo frame supports up to 10 KB (full-duplex)
- Industry temperature (I-temp) option

3.7. MIPI-DSI to Dual Channel LVDS Bridge (SN65DSI84)

The DART-MX8M features TI SN65DIS84 MIPI-DSI Bridge to FLATLINK LVDS display.

The SN65DSI84 DSI to FlatLink™ bridge features a single-channel MIPI® D-PHY receiver front-end configuration with 4 lanes per channel operating at 1 Gbps per lane. The bridge decodes MIPI® DSI 18bpp RGB666 and 24 bpp RGB888 packets and converts the formatted video data stream to a FlatLink™ compatible LVDS output operating at pixel clocks operating from 25 MHz to 154 MHz, offering a Dual-Link LVDS, Single-Link LVDS interface with four data lanes per link.
The SN65DSI84 is well suited for WUXGA 1920 x1200 at 60 frames per second, with up to 24 bits-per- pixel. Partial line buffering is implemented to accommodate the data stream mismatch between the DSI and LVDS interfaces.
Designed with industry compliant interface technology, the SN65DSI84 is compatible with a wide range of micro-processors, and is designed with a range of power management features including low running swing LVDS outputs, and the MIPI® defined ultra-low power state (ULPS) support.
The temperature ranges from -40ºC to 85ºC.

4. DART-MX8M Hardware Configuration

DART-MX8M hardware interfaces, explained on sections 3.3, 3.4, 3.6 and 3.7, configured using the orderable part number of the module.

Table 1 details the part of the hardware configuration orderable options.

Table 1: Partial Hardware Configuration Options

Option	Description
EC	Ethernet PHY assembled on SOM
AC	Audio Codec assembled on SOM
WBD	Dual band Wi-Fi and BT/BLE combo assembled on SOM
LD	LVDS Display bridge assembled on SOM

Note

Other orderable options are available and are not part of this datasheet.
Please refer to Variscite official website for full list of configuration options.

5. External Connectors

5.1. Board to Board Connector

- The DART-MX8M exposes three 90-pin board-to-board connectors.
- The recommended mating connector is: **Hirose Electric Co Ltd PN: DF40C-90DS-0.4V(51)**

5.2. Wi-Fi & BT Connector

- Modules with Wi-Fi ***"WBD" Configuration*** **-** a combined Wi-Fi + BT antenna connector is assembled
- Connector type: **U.FL JACK connector**
- Cable and antenna shall have a 50 Ohm characteristic impedance

5.3. DART-MX8M Connector Pin-out & Pin-Mux

Table *2,*

Table *3* and

Table 4 lists the SOM connectors with the available functions on each pin.
Table below lists two types of function- sets:

- Alternative functions of the SOC pins, configured using the BSP – under columns ALT0 to ALT6
- Additional chip function used on SOM; Relates to the DART-MX8M orderable configuration – under column ALT_IC.

Column		Meaning
Pin#		Pin number on a connector
	Jx.YY	Jx : Can be J1 J2 or J3
		YY : Can be 1 to 90
BALL		Source device and it's pin number
	XX.YY	XX : Source Chip can be: SOC.yy – pins connected to the iMX 8M SOC AR8033.yy – pins connected the Ethernet Controller (***"EC" Configuration***) WM8904.yy - pins connected the Audio Codec (***"AC" Configuration***) SN65DSI84.yy - pins connected the LVDS Display bridge (***"LD" Configuration***) YY : Pin/Ball number of source chip.

Table 2: DART-MX8M_J1 PINMUX

PIN#	Alt0/ SOM PIN	Alt1	Alt2	Alt3	Alt5	Alt6	Alt_IC	ALT0-6 BALL	Alt_IC Ball
J1.1	GPIO1_IO00				REF_CLK_32K			SOC.T6	
J1.2	ENET_TD1				GPIO1_IO20		ETH_TRX1_P	SOC.R21	AR8033.14
J1.3	ENET_TX_CTL				GPIO1_IO22				SOC.P19
J1.4	ENET_TD0				GPIO1_IO21		ETH_TRX1_N	SOC.R20	AR8033.15
J1.5	ENET_TXC				GPIO1_IO23		LED_LINK10_100	SOC.T19	AR8033.26
J1.6	ENET_TD2				GPIO1_IO19		ETH_TRX0_N	SOC.R19	AR8033.12
J1.7	ENET_RXC				GPIO1_IO25		LED_LINK1000	SOC.T20	AR8033.24
J1.8	ENET_TD3				GPIO1_IO18		ETH_TRX0_P	SOC.P20	AR8033.11
J1.9	ENET_RX_CTL				GPIO1_IO24		LED_ACT	SOC.T21	AR8033.23
J1.10	ENET_RD0				GPIO1_IO26		ETH_TRX2_P	SOC.U19	AR8033.17
J1.11	ENET_MDIO				GPIO1_IO17			SOC.N19	
J1.12	ENET_RD1				GPIO1_IO27		ETH_TRX2_N	SOC.U21	AR8033.18
J1.13	ENET_MDC				GPIO1_IO16			SOC.N20	
J1.14	ENET_RD2				GPIO1_IO28		ETH_TRX3_P	SOC.U20	AR8033.20
J1.16	ENET_RD3				GPIO1_IO29		ETH_TRX3_N	SOC.V19	AR8033.21
J1.17	I2C4_SCL	PWM2_OUT	PCIE1_CLKREQ_B		GPIO5_IO20			SOC.F8	
J1.19	I2C4_SDA	PWM1_OUT	PCIE2_CLKREQ_B		GPIO5_IO21			SOC.F9	
J1.20	ONOFF							SOC.W21	
J1.22	PMIC_ON_REQ							SOC.V20	
J1.23	CLK2_N							SOC.U22	
J1.24	POR_B							SOC.W20	
J1.25	CLK2_P							SOC.T22	
J1.26	PMIC_STBY_REQ							SOC.V21	
J1.28	SD2_RESET_B				GPIO2_IO19			SOC.R22	
J1.29	CLK1_N							SOC.T23	
J1.31	CLK1_P							SOC.R23	
J1.32	NAND_DATA01	QSPIA_DATA1			GPIO3_IO07			SOC.J20	
J1.34	NAND_CE0_B	QSPIA_SS0_B			GPIO3_IO01			SOC.H19	
J1.35	NAND_DATA07	QSPIB_DATA3			GPIO3_IO13			SOC.M19	

PIN#	Alt0/ SOM PIN	Alt1	Alt2	Alt3	Alt5	Alt6	Alt_IC	ALT0-6 BALL	Alt_IC Ball
J1.36	NAND_READY_B				GPIO3_IO16			SOC.K20	
J1.37	NAND_DATA06	QSPIB_DATA2			GPIO3_IO12			SOC.L19	
J1.38	NAND_DQS	QSPIA_DQS			GPIO3_IO14			SOC.M20	
J1.39	NAND_DATA04	QSPIB_DATA0			GPIO3_IO10			SOC.L20	
J1.40	NAND_ALE	QSPIA_SCLK			GPIO3_IO00			SOC.G19	
J1.41	NAND_RE_B	QSPIB_DQS			GPIO3_IO15			SOC.K19	
J1.42	NAND_WP_B				GPIO3_IO18			SOC.K21	
J1.43	NAND_DATA05	QSPIB_DATA1			GPIO3_IO11			SOC.J22	
J1.44	NAND_WE_B				GPIO3_IO17			SOC.K22	
J1.45	NAND_CLE	QSPIB_SCLK			GPIO3_IO05			SOC.H21	
J1.46	NAND_DATA03	QSPIA_DATA3			GPIO3_IO09			SOC.J21	
J1.47	NAND_CE2_B	QSPIB_SS0_B			GPIO3_IO03			SOC.F21	
J1.48	NAND_DATA00	QSPIA_DATA0			GPIO3_IO06			SOC.G20	
J1.50	NAND_DATA02	QSPIA_DATA2			GPIO3_IO08			SOC.H22	
J1.51	PCIE1_REF_CLKN							SOC.K24	
J1.53	PCIE1_REF_CLKP							SOC.K25	
J1.54	PCIE2_REF_CLKN							SOC.F24	
J1.56	PCIE2_REF_CLKP							SOC.F25	
J1.57	PCIE1_TXN							SOC.J24	
J1.59	PCIE1_TXP							SOC.J25	
J1.60	PCIE1_RXN							SOC.H24	
J1.62	PCIE1_RXP							SOC.H25	
J1.63	PCIE2_RXN							SOC.D24	
J1.65	PCIE2_RXP							SOC.D25	
J1.66	PCIE2_TXN							SOC.E24	
J1.68	PCIE2_TXP							SOC.E25	
J1.69	CSI_P1_DP3							SOC.D21	
J1.71	CSI_P1_DN3							SOC.C21	
J1.72	CONN_WI-FI_DISN[2]								
J1.73	CSI_P1_DP1							SOC.D22	
J1.74	SD2_CD_B				GPIO2_IO012			SOC.L21	

PIN#	Alt0/ SOM PIN	Alt1	Alt2	Alt3	Alt5	Alt6	Alt_IC	ALT0-6 BALL	Alt_IC Ball
J1.75	CSI_P1_DN1							SOC.C22	
J1.77	CSI_P1_DN2							SOC.B24	
J1.78	SD2_DATA2				GPIO2_IO17			SOC.P22	
J1.79	CSI_P1_DP2							SOC.C23	
J1.80	SD2_DATA1				GPIO2_IO16			SOC.N21	
J1.81	CSI_P1_DP0							SOC.B23	
J1.82	SD2_CLK				GPIO2_IO13			SOC.L22	
J1.83	CSI_P1_DN0							SOC.A23	
J1.84	SD2_DATA3				GPIO2_IO18			SOC.P21	
J1.86	SD2_DATA0				GPIO2_IO15			SOC.N22	
J1.87	CSI_P1_CKP							SOC.B22	
J1.88	SD2_CMD				GPIO2_IO14			SOC.M22	
J1.89	CSI_P1_CKN							SOC.A22	
J1.15	NVCC_SNVS_3V3							POWER OUT	
J1.27	NVCC_3V3							POWER OUT	
J1.90	NVCC_SD2_1V8_3V3							POWER OUT	
J1. 18,21,30 ,33,49,52 ,55,58,61 ,64,67,70 ,76,85	GND							GND	

Table 3: DART-MX8M_J2 PINMUX

PIN#	Alt0/ SOM PIN	Alt1	Alt2	Alt3	Alt5	Alt6	Alt_IC	ALT0-6 BALL	Alt_IC Ball
J2.1	JTAG_TCK							SOC.T5	
J2.2	SAI3_TXD	GPT1_COMPARE3	SAI5_RXD3		GPIO5_IO01		HPLOUT	SOC.C3	WM8904.13
J2.3	JTAG_TMS							SOC.V5	
J2.4	SAI3_TXC	GPT1_COMPARE2	SAI5_RXD2		GPIO5_IO00		HPROUT	SOC.C4	WM8904.15
J2.5	JTAG_TRST_B							SOC.U6	
J2.6	SAI3_RXFS	GPT1_CAPTURE1	SAI5_RXFS		GPIO4_IO28		HPOUTFB	SOC.G4	WM8904.14
J2.7	JTAG_TDI							SOC.W5	
J2.8	SAI3_RXC	GPT1_CAPTURE2	SAI5_RXC		GPIO4_IO29		LINEIN1_LP	SOC.F4	WM8904.26
J2.9	JTAG_TDO							SOC.U5	
J2.10	SAI3_TXFS	GPT1_CLK	SAI5_RXD1		GPIO4_IO31		LINEIN1_RP	SOC.G3	WM8904.24
J2.11	BOOT_MODE1							SOC.V6	
J2.13	BOOT_MODE0							SOC.W6	
J2.14	SAI3_RXD	GPT1_COMPARE1	SAI5_RXD0		GPIO4_IO30		DMIC_CLK	SOC.F3	WM8904.1
J2.15	HDMI_DDC_SCL							SOC.R3	
J2.16	SAI3_MCLK	PWM4_OUT	SAI5_MCLK		GPIO5_IO02		DMIC_DATA	SOC.D3	WM8904.27
J2.17	HDMI_DDC_SDA							SOC.P3	
J2.19	HDMI_CEC							SOC.W3	
J2.20	ECSPI2_MOSI	UART4_TXD			GPIO5_IO11			SOC.E5	
J2.21	HDMI_HPD							SOC.W2	
J2.22	ECSPI2_MISO	UART4_CTS_B			GPIO5_IO12			SOC.B5	
J2.24	ECSPI2_SCLK	UART4_RXD			GPIO5_IO10			SOC.C5	
J2.25	HDMI_AUX_P							SOC.V1	
J2.26	ECSPI2_SS0	UART4_RTS_B			GPIO5_IO13			SOC.A5	

PIN#	Alt0/ SOM PIN	Alt1	Alt2	Alt3	Alt5	Alt6	Alt_IC	ALT0-6 BALL	Alt_IC Ball
J2.27	HDMI_AUX_N							SOC.V2	
J2.28	GPIO1_IO02	WDOG_B						SOC.R4	
J2.29	HDMI_TX_M_LN_1							SOC.U1	
J2.30	I2C2_SDA	ENET_1588_EVENT1_OUT			GPIO5_IO17			SOC.F7	
J2.31	HDMI_TX_P_LN_1							SOC.U2	
J2.32	I2C2_SCL	ENET_1588_EVENT1_IN			GPIO5_IO16			SOC.G7	
J2.33	HDMI_TX_P_LN_0							SOC.T1	
J2.34	SAI5_RXFS	SAI1_TXD0			GPIO3_IO19			SOC.N4	
J2.35	HDMI_TX_M_LN_0							SOC.T2	
J2.36	SAI5_RXD0	SAI1_TXD2			GPIO3_IO21			SOC.M5	
J2.37	HDMI_REFCLK_N							SOC.R1	
J2.38	SAI5_RXD2	SAI1_TXD4	SAI1_TXFS	SAI5_TXC	GPIO3_IO23			SOC.M4	
J2.39	HDMI_REFCLK_P							SOC.R2	
J2.40	SAI5_RXC	SAI1_TXD1			GPIO3_IO20			SOC.L5	
J2.42	SAI5_RXD1	SAI1_TXD3	SAI1_TXFS	SAI5_TXFS	GPIO3_IO22			SOC.L4	
J2.43	HDMI_TX_P_LN_2							SOC.N2	
J2.44	SAI5_RXD3	SAI1_TXD5	SAI1_TXFS	SAI5_TXD0	GPIO3_IO24			SOC.K5	
J2.45	HDMI_TX_M_LN_2							SOC.N1	
J2.46	SAI5_MCLK	SAI1_TXC	SAI4_MCLK		GPIO3_IO25			SOC.K4	
J2.48	SAI2_RXFS	SAI5_TXFS			GPIO4_IO21			SOC.J4	
J2.49	HDMI_TX_P_LN_3							SOC.M1	
J2.50	SAI2_RXC	SAI5_TXC			GPIO4_IO22			SOC.H3	
J2.51	HDMI_TX_M_LN_3							SOC.M2	
J2.52	SAI2_TXFS	SAI5_TXD1			GPIO4_IO24			SOC.H4	
J2.54	SAI2_MCLK	SAI5_MCLK			GPIO4_IO27			SOC.H5	

PIN#	Alt0/ SOM PIN	Alt1	Alt2	Alt3	Alt5	Alt6	Alt_IC	ALT0-6 BALL	Alt_IC Ball
J2.55	SAI1_RXFS	SAI5_RXFS			GPIO4_IO00			SOC.L1	
J2.56	SAI2_TXC	SAI5_TXD2			GPIO4_IO25			SOC.J5	
J2.57	SAI1_RXC	SAI5_RXC			GPIO4_IO01			SOC.K1	
J2.58	SAI2_RXD0	SAI5_TXD0			GPIO4_IO23			SOC.H6	
J2.59	SAI1_RXD1	SAI5_RXD1			GPIO4_IO03	BOOT_CFG01		SOC.L2	
J2.60	SAI2_TXD0	SAI5_TXD3			GPIO4_IO26			SOC.G5	
J2.61	SAI1_RXD0	SAI5_RXD0			GPIO4_IO02	BOOT_CFG00		SOC.K2	
J2.62	SAI1_RXD3	SAI5_RXD3			GPIO4_IO05	BOOT_CFG03		SOC.J2	
J2.63	SAI1_RXD2	SAI5_RXD2			GPIO4_IO04	BOOT_CFG02		SOC.H2	
J2.64	SAI1_TXFS	SAI5_TXFS			GPIO4_IO10			SOC.H1	
J2.65	SAI1_RXD4	SAI6_TXC	SAI6_RXC		GPIO4_IO06	BOOT_CFG04		SOC.J1	
J2.66	SAI1_RXD6	SAI6_TX_SYNC	SAI6_RXFS		GPIO4_IO08	BOOT_CFG06		SOC.G2	
J2.67	SAI1_TXD1	SAI5_TXD1			GPIO4_IO13	BOOT_CFG09		SOC.E2	
J2.68	SAI1_RXD7	SAI6_MCLK	SAI1_TXFS	SAI1_TXD4	GPIO4_IO09	BOOT_CFG07		SOC.G1	
J2.69	SAI1_RXD5	SAI6_TXD0	SAI6_RXD0	SAI1_RXFS	GPIO4_IO07	BOOT_CFG05		SOC.F1	
J2.70	SAI1_TXD0	SAI5_TXD0			GPIO4_IO12	BOOT_CFG08		SOC.F2	
J2.71	SAI1_TXD5	SAI6_RXD0	SAI6_TXD0		GPIO4_IO17	BOOT_CFG13		SOC.C2	
J2.72	SAI1_TXC	SAI5_TXC			GPIO4_IO11			SOC.E1	
J2.73	SAI1_TXD3	SAI5_TXD3			GPIO4_IO15	BOOT_CFG11		SOC.D1	
J2.74	SAI1_TXD4	SAI6_RXC	SAI6_TXC		GPIO4_IO16	BOOT_CFG12		SOC.D2	
J2.76	SAI1_TXD7	SAI6_MCLK			GPIO4_IO19	BOOT_CFG15		SOC.C1	
J2.77	ECSPI1_SCLK	UART3_RX			GPIO5_IO06			SOC.D5	
J2.78	SAI1_TXD2	SAI5_TXD2			GPIO4_IO14	BOOT_CFG10		SOC.B2	
J2.79	ECSPI1_SS0	UART3_RTS_B			GPIO5_IO09			SOC.D4	
J2.80	SAI1_TXD6	SAI6_RXFS	SAI6_TXFS		GPIO4_IO18	BOOT_CFG14		SOC.B3	

PIN#	Alt0/ SOM PIN	Alt1	Alt2	Alt3	Alt5	Alt6	Alt_IC	ALT0-6 BALL	Alt_IC Ball
J2.81	ECSPI1_MISO	UART3_CTS_B			GPIO5_IO08			SOC.B4	
J2.82	SAI1_MCLK	SAI5_MCLK	SAI1_TXC		GPIO4_IO20			SOC.A3	
J2.83	ECSPI1_MOSI	UART3_TX			GPIO5_IO07			SOC.A4	
J2.85	UART2_RXD	ECSPI3_MISO			GPIO5_IO24			SOC.B6	
J2.86	UART2_TXD	ECSPI3_SS0			GPIO5_IO25			SOC.D6	
J2.87	UART3_RXD	UART1_CTS_B			GPIO5_IO26			SOC.A6	
J2.88	UART1_RXD	ECSPI3_SCLK			GPIO5_IO22			SOC.C7	
J2.89	UART3_TXD	UART1_RTS_B			GPIO5_IO27			SOC.B7	
J2.90	UART1_TXD	ECSPI3_MOSI			GPIO5_IO23			SOC.A7	
J2.12	AGND							AUDIO AGND	
J2.41	VDD_PHY_1V8							POWER OUT	
J2. 18,23,47, 53,75,84	GND							GND	

Table 4: DART-MX8M_J3 PINMUX

PIN#	Alt0/ SOM PIN	Alt1	Alt2	Alt3	Alt5	Alt6	Alt_IC	ALT0-6 BALL	Alt_IC Ball
J3.1	UART4_TXD	UART2_RTS_B	PCIE2_CLKREQ_B		GPIO5_IO29			SOC.D7	
J3.2							LVDS1_TX0_P		SN65DSI84.C8
J3.3	UART4_RXD	UART2_CTS_B	PCIE1_CLKREQ_B		GPIO5_IO28			SOC.C6	
J3.4							LVDS1_TX0_N		SN65DSI84.C9
J3.5							LVDS1_TX2_P		SN65DSI84.E8
J3.6							LVDS1_TX1_P		SN65DSI84.D8
J3.7							LVDS1_TX2_N		SN65DSI84.E9
J3.8							LVDS1_TX1_N		SN65DSI84.D9
J3.11							LVDS1_CLK_P		SN65DSI84.F8
J3.12	DSI_TX0_P						LVDS2_TX0_P	SOC.B17	SN65DSI84.B3
J3.13							LVDS1_CLK_N		SN65DSI84.F9
J3.14	DSI_TX0_N						LVDS2_TX0_N	SOC.A17	SN65DSI84.A3
J3.16	DSI_TX1_P						LVDS2_TX1_P	SOC.B16	SN65DSI84.B4
J3.17							LVDS1_TX3_P		SN65DSI84.G8
J3.18	DSI_TX1_N						LVDS2_TX1_N	SOC.A16	SN65DSI84.A4
J3.19							LVDS1_TX3_N		SN65DSI84.G9
J3.20	DSI_TX3_P						LVDS2_TX3_P	SOC.B15	SN65DSI84.B7
J3.22	DSI_TX3_N						LVDS2_TX3_N	SOC.A15	SN65DSI84.A7
J3.23	DSI_TX2_P						LVDS2_CLK_P	SOC.B18	SN65DSI84.B6
J3.25	DSI_TX2_N						LVDS2_CLK_N	SOC.A18	SN65DSI84.A6
J3.26	USB2_VBUS							SOC.D9	
J3.28	SPDIF_RX	PWM2_OUT			GPIO5_IO04			SOC.G6	
J3.29	DSI_CLK_N						LVDS2_TX2_N	SOC.C16	SN65DSI84.A5

PIN#	Alt0/ SOM PIN	Alt1	Alt2	Alt3	Alt5	Alt6	Alt_IC	ALT0-6 BALL	Alt_IC Ball
J3.30	GPIO1_IO11	USB2_OTG_ID			PMIC_READY			SOC.L6	
J3.31	DSI_CLK_P						LVDS2_TX2_P	SOC.D16	SN65DSI84.B5
J3.32	SPDIF_EXT_CLK	PWM1_OUT			GPIO5_IO05			SOC.E6	
J3.35	USB2_RXN								
J3.36	SPDIF_TX	PWM3_OUT			GPIO5_IO03			SOC.F6	
J3.37	USB2_RXP								
J3.38	GPIO1_IO15	USB2_OTG_OC			PWM4_OUT			SOC.J6	
J3.40	GPIO1_IO13	USB1_OTG_OC			PWM2_OUT			SOC.K6	
J3.41	USB2_TXN								
J3.42	I2C3_SDA	PWM3_OUT	GPT3_CLK		GPIO5_IO19			SOC.E9	
J3.43	USB2_TXP								
J3.44	USB2_ID							SOC.C9	
J3.46	I2C3_SCL	PWM4_OUT	GPT2_CLK		GPIO5_IO18			SOC.G8	
J3.47	USB2_DP							SOC.A10	
J3.48	GPIO1_IO14	USB2_OTG_PWR			PWM3_OUT			SOC.K7	
J3.49	USB2_DN							SOC.B10	
J3.50	GPIO1_IO12	USB1_OTG_PWR						SOC.L7	
J3.52	GPIO1_IO10	USB1_OTG_ID						SOC.M7	
J3.53	USB1_RXN								
J3.54	GPIO1_IO03	USDHC1_VSELECT				XTAL_OK		SOC.P4	
J3.55	USB1_RXP								
J3.56	USB1_ID							SOC.C14	
J3.58	GPIO1_IO06	ENET1_MDC			SD1_CD_B			SOC.N5	
J3.59	USB1_TXN								
J3.60	GPIO1_IO08	ENET1_1588_EVENT0_IN			SD2_RESET_B			SOC.N7	

PIN#	Alt0/ SOM PIN	Alt1	Alt2	Alt3	Alt5	Alt6	Alt_IC	ALT0-6 BALL	Alt_IC Ball
J3.61	USB1_TXP								
J3.62	GPIO1_IO05	M4_NMI			PMIC_READY			SOC.P7	
J3.64	GPIO1_IO01	PWM1_OUT			REF_CLK_24M			SOC.T7	
J3.65	USB1_DP							SOC.A14	
J3.66	USB1_VBUS							SOC.D14	
J3.67	USB1_DN							SOC.B14	
J3.70	CSI_P2_CKN							SOC.A19	
J3.72	CSI_P2_CKP							SOC.B19	
J3.76	CSI_P2_DN3							SOC.C19	
J3.78	CSI_P2_DP3							SOC.D19	
J3.80	CSI_P2_DN1							SOC.A20	
J3.82	CSI_P2_DP1							SOC.B20	
J3.84	CSI_P2_DN0							SOC.C20	
J3.86	CSI_P2_DP0							SOC.D20	
J3.88	CSI_P2_DN2							SOC.A21	
J3.90	CSI_P2_DP2							SOC.B21	
J3.69	LICELL							POWER IN	
J3. 9,15,21, 21,24,27, 33,34,39, 45,51,57, 63,68,74	**GND**							**GND**	
J3. 71,73,75, 77,79,81,	**VBAT**							**POWER IN**	

PIN#	Alt0/ SOM PIN	Alt1	Alt2	Alt3	Alt5	Alt6	Alt_IC	ALT0-6 BALL	Alt_IC Ball
83,85,87, 89									

6. SOM's interfaces

Acronym used in the tables listed under this section:

Table 5: Acronyms used on SOM's Interfaces Tables

Column		Meaning
Pin#		Pin number on a connector
	Jx.YY	Jx : Can be J1 J2 or J3
		YY : Can be 1 to 90
	*****	Denotes pins with alternative function selected using the PINMUX
	~	Denotes pins which exposes different functions depending on assembly options
	^	Denotes pins which are latched on boot to set the boot configuration
Type		Pin type & direction
	I	INPUT
	O	OUTPUT
	DS	Differential Signal
	A	Analog
	P	Power
BALL		Source device and it's pin number
	XX.YY	XX : Source Chip can be: SOC.yy – pins connected to the iMX 8M SOC AR8033.yy – pins connected the Ethernet Controller (***"EC" Configuration***) WM8904.yy - pins connected the Audio Codec (***"AC" Configuration***) SN65DSI84.yy - pins connected the LVDS Display bridge (***"LD" Configuration***) YY : Pin/Ball number of source chip.

NOTE

Any combination of the pin type and direction are valid, e.g. "DSI" = Differential Signal Input; "DSAIO" = Differential Signal Analog Input Output signal; "PO" = Power Output.

Trace Impedance

SOM traces are designed with the below table impedance list per signal group.
Table is a reference when you are updating or creating constraints in the PCB design tool to set up the impedances/trace widths.

Table 6: SOM Signal Group Traces Impedance

Signal Group	Impedance
All single ended signals	50 Ω Single ended
PCIe TX/RX data pairs	85 Ω Differential
USB Differential signals	90 Ω Differential
Differential signals including: Ethernet, PCIe clocks, HDMI, MIPI (CSI and DSI), LVDS lines	100 Ω Differential

6.1. Display Interfaces

The DART-MX8M consists of the following display interfaces options:

- HDMI/DP/eDP
  - HDMI1.4, HDMI 2.0a support for resolution up to 4096x2160p60
  - HDCP 2.2 and HDCP 1.4
  - Pixel clock up to 596 MHz
  - Display Port 1.3
  - eDP 1.4
  - One standard support at a time by means of software configuration.
  - All standards share the same pins.
- MIPI DSI – **No *"LD" Configuration***
  - MIPI-DSI standard v1.1 support resolution up to 1920x1080p60.
  - Up to 4 data lanes support D-PHY
  - 80Mbps - 1.5Gbps data rate in high speed operation
  - 10Mbps data rate in low power operation
  - Implements all three DSI Layers (Pixel to Byte packing, Low Level Protocol, Lane Management)
  - Supports High Speed and Low Power operation
  - Host Version
- LVDS - ***"LD" Configuration***
  - Implemented using SN65DSI84 (see section 3.7)
  - Single channel DSI to two Single-Link LVDS
  - Resolution up to 1920x1200 60 fps at 24 bpp/18 bpp, but limited by the DSI interface to 1920x1080.
  - DSI Channel has 4 DSI data lanes + 1 CLK lane.
  - Each LVDS link has 4 data lanes + 1 CLK lane.

NOTE

MIPI-DSI interface available on DART-MX8M connectors without ***"LD" Configuration***.

6.1.1. HDMI Signals

Table 7: HDMI Signals

PIN#	PIN Function	Type	Description	BALL
J2.15	HDMI_DDC_SCL	O	Display Data Channel (DDC) - Clock	SOC.R3
J2.17	HDMI_DDC_SDA	IO	Display Data Channel (DDC) - Data I2C based communication HDMI source device to read the data from the HDMI sink device to learn what audio/video formats it can take.	SOC.P3
J2.19	HDMI_CEC	IO	Consumer Electronics Control (CEC) Bidirectional serial bus to perform remote control functions	SOC.W3
J2.21	HDMI_HPD	AO	Hot Plug Detect (HPD)	SOC.W2
J2.25	HDMI_AUX_P	DSIO	Carries the HEAC POS - HDMI Ethernet Audio Channel	SOC.V1
J2.27	HDMI_AUX_N	DSIO	Carries the HEAC NEG - HDMI Ethernet Audio Channel	SOC.V2

PIN#	PIN Function	Type	Description	BALL
J2.29	HDMI_TX_M_LN_1	DSO	HDMI_DATA1 NEG	SOC.U1
J2.31	HDMI_TX_P_LN_1	DSO	HDMI_DATA1 POS	SOC.U2
J2.33	HDMI_TX_P_LN_0	DSO	HDMI_DATA0 POS	SOC.T1
J2.35	HDMI_TX_M_LN_0	DSO	HDMI_DATA0 NEG	SOC.T2
J2.37	HDMI_REFCLK_N	DSI	Core reference clock NEG (HCSL 27MHz)	SOC.R1
J2.39	HDMI_REFCLK_P	DSI	Core reference clock POS (HCSL 27MHz)	SOC.R2
J2.43	HDMI_TX_P_LN_2	DSO	HDMI_DATA2 POS	SOC.N2
J2.45	HDMI_TX_M_LN_2	DSO	HDMI_DATA2 NEG	SOC.N1
J2.49	HDMI_TX_P_LN_3	DSO	HDMI_CLK POS	SOC.M1
J2.51	HDMI_TX_M_LN_3	DSO	HDMI_CLK NEG	SOC.M2
J2.41	VDD_PHY_1V8	PO	HDMI Core power on SOM output Can be used to control the HDMI/DP/eDP termination	

6.1.1.1. HDMI Termination

HDMI CLK and Data lines (TMDS type) should be terminated using 604-Ohm resistors. Termination should be applied after HDMI analog core is powered. DART-MX8M power VDD_PHY_1V8 can be used for the termination control. See Figure 3 for illustration of the termination scheme.

Note: When the interface being used as DP or eDP termination should be disabled.

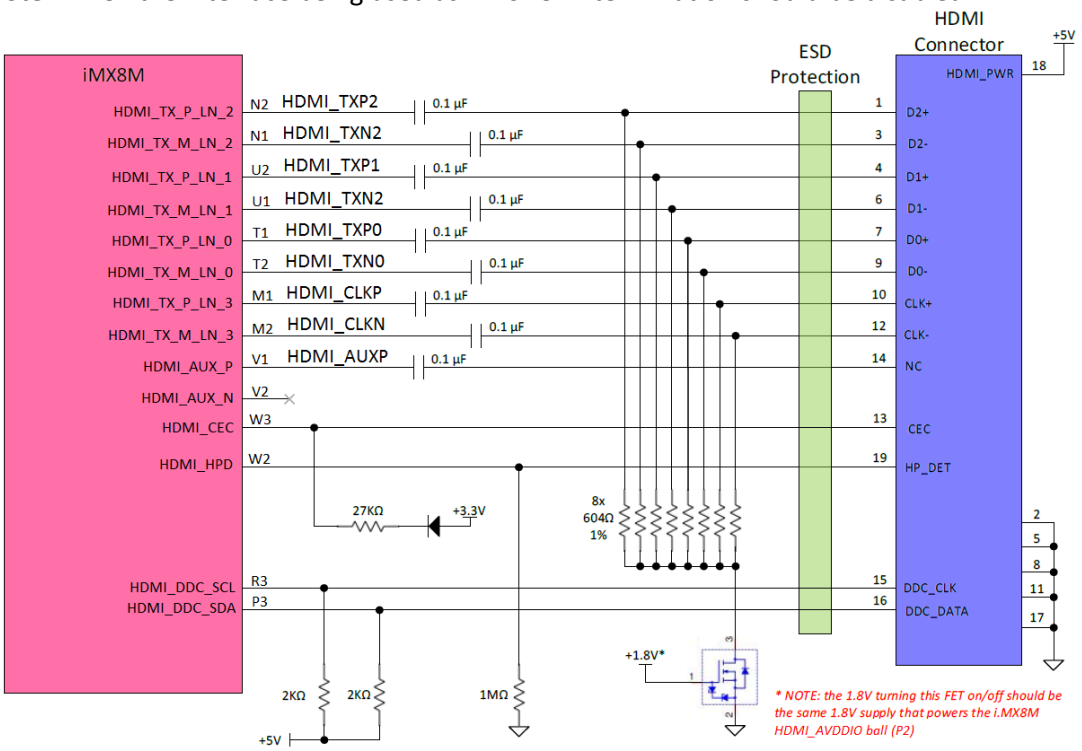

Figure 3 : HDMI output connectivity

When planning the HDMI interface, place the 604 Ω pull-down resistors directly on the signal trace, as shown in Figure 4.

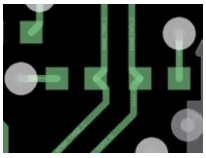

Figure 4: HDMI interface pull-down resistor placement

6.1.1.2. HDMI Reference Clock

When configured as HDMI output, the two pins named HDMI_REFCLK_P and HDMI_REFCLK_N are input pins to provide 27 MHz reference clock to the HDMI PHY to improve jitter performance. An external oscillator supporting HCSL compatible output generates the reference clock. Table 8 lists the specifications of the reference clock requirements.

Table 8 : HDMI external reference clock specification

Normative electrical parameter	Specification			Unit	Conditions
	Min.	Typ.	Max.		
External clock frequency	-	27	1	MHz	-
Input duty	45	-	55	%	-
Differential peak-to-peak amplitude at pin	0.5	-	2.2	V	-
Rise/Fall time (10–90 %)	-	-	200	ps	-
Input random jitter	-	-	-140	dBC/Hz	Noise floor density from 10 KHz to 10 MHz.
	-	-	2.963	ps	For a 27 MHz reference, integrated
					jitter from 10 KHz to 10 MHz.
Input determines tic jitter	-	-	9	ps	Over a band of 10 KHz to 10 MHz

6.1.2. Display Port/Embedded Display Port Signals

The Display port and Embedded Display port signals share the same pins as the HDMI interface with appropriate software changes to output the different display standard.

DisplayPort 1.3 standard (VESA.org)

- DP supports 1.6 GHz (RBR), 2.7 GHz (HBR), and 5.4 GHz (HBR2) rates. Those rates are managed in API (Host).
- RBR supports 1080p60 (RGB 8b), HBR supports 4kp30 (RGB 8b) and HBR2 supports 4kp60 (RGB 8b).

Embedded DisplayPort 1.4 standard (VESA.org)

- eDP link rates: R216 (2.16 Gbps), R243 (2.43 Gbps), R324 (3.24 Gbps), and R432 (4.32 Gbps)
- Fast Link Training is also supported

Table 9: Display Port/ Embedded DP Signals

PIN#	PIN Function	Type	Description	BALL
J2.21	HDMI_HPD	AO	Hot Plug Detect (HPD)	SOC.W2
J2.25	HDMI_AUX_P	DSIO	Auxilliary channel P	SOC.V1
J2.27	HDMI_AUX_N	DSIO	Auxilliary channel N	SOC.V2
J2.29	HDMI_TX_M_LN_1	DSO	DP/eDP LANE1 NEG	SOC.U1
J2.31	HDMI_TX_P_LN_1	DSO	DP/eDP LANE1 POS	SOC.U2
J2.33	HDMI_TX_P_LN_0	DSO	DP/eDP LANE0 POS	SOC.T1
J2.35	HDMI_TX_M_LN_0	DSO	DP/eDP LANE0 NEG	SOC.T2
J2.37	HDMI_REFCLK_N	DSI	Core reference clock NEG (HCSL 27MHz)	SOC.R1
J2.39	HDMI_REFCLK_P	DSI	Core reference clock POS (HCSL 27MHz)	SOC.R2
J2.43	HDMI_TX_P_LN_2	DSO	DP/eDP LANE2 POS	SOC.N2
J2.45	HDMI_TX_M_LN_2	DSO	DP/eDP LANE2 NEG	SOC.N1
J2.49	HDMI_TX_P_LN_3	DSO	DP/eDP LANE3 POS	SOC.M1
J2.51	HDMI_TX_M_LN_3	DSO	DP/eDP LANE3 NEG	SOC.M2

6.1.3. MIPI-DSI Signals

The MIPI-DSI signals share the same pins as the LVDS channel 2 function depending on the orderable configuration option.

Table 10: MIPI-DSI Signals

PIN#	PIN Function	Type	Description	BALL
J3.12~	DSI_TX0_P	DSIO	MIPI D-PHY LANE0 POS	SOC.B17
J3.14~	DSI_TX0_N	DSIO	MIPI D-PHY LANE0 NEG	SOC.A17
J3.16~	DSI_TX1_P	DSO	MIPI D-PHY LANE1 POS	SOC.B16
J3.18~	DSI_TX1_N	DSO	MIPI D-PHY LANE1 NEG	SOC.A16
J3.20~	DSI_TX3_P	DSO	MIPI D-PHY LANE3 POS	SOC.B15
J3.22~	DSI_TX3_N	DSO	MIPI D-PHY LANE3 NEG	SOC.A15
J3.23~	DSI_TX2_P	DSO	MIPI D-PHY LANE2 POS	SOC.B18
J3.25~	DSI_TX2_N	DSO	MIPI D-PHY LANE2 NEG	SOC.A18
J3.29~	DSI_CLK_N	DSO	MIPI D-PHY CLOCK NEG	SOC.C16
J3.31~	DSI_CLK_P	DSO	MIPI D-PHY CLOCK POS	SOC.D16

NOTE

"~" Denote pin function available without ***"LD" Configuration***.

6.1.4. LVDS Display Signals

The LVDS display support includes two channels generated by the driving IC, see section 3.7.

Sections 6.1.4.1 and 6.1.4.2 lists the interface pins and signal description.

6.1.4.1. LVDS Display Signals Channel 1

Table 11: LVDS Display Channel 1 Signals

PIN#	PIN Function	Type	Description	BALL
J3.2~	LVDS1_TX0_P	DSO	FlatLink Channel 1 LVDS Data0 POS	SN65DSI84.C8
J3.4~	LVDS1_TX0_N	DSO	FlatLink Channel 1 LVDS Data0 NEG	SN65DSI84.C9
J3.6~	LVDS1_TX1_P	DSO	FlatLink Channel 1 LVDS Data1 POS	SN65DSI84.D8
J3.8~	LVDS1_TX1_N	DSO	FlatLink Channel 1 LVDS Data1 NEG	SN65DSI84.D9
J3.5~	LVDS1_TX2_P	DSO	FlatLink Channel 1 LVDS Data2 POS	SN65DSI84.E8
J3.7~	LVDS1_TX2_N	DSO	FlatLink Channel 1 LVDS Data2 NEG	SN65DSI84.E9
J3.11~	LVDS1_CLK_P	DSO	FlatLink Channel 1 LVDS Clock POS	SN65DSI84.F8
J3.13~	LVDS1_CLK_N	DSO	FlatLink Channel 1 LVDS Clock NEG	SN65DSI84.F9
J3.17~	LVDS1_TX3_P	DSO	FlatLink Channel 1 LVDS Data3 POS	SN65DSI84.G8
J3.19~	LVDS1_TX3_N	DSO	FlatLink Channel 1 LVDS Data3 NEG	SN65DSI84.G9

NOTE

- ***"~"*** Denote pin function available with ***"LD" Configuration***.
- When the ***"LD" configuration*** NOT chosen, the LVDS Channel 1 pins are floating on the DART-MX8M connector.

6.1.4.2. LVDS Display Signals Channel 2

Table 12: LVDS Display Channel 2 Signals

PIN#	PIN Function	Type	Description	BALL
J3.12~	LVDS2_TX0_P	DSO	FlatLink Channel 2 LVDS Data0 POS	SN65DSI84.B3
J3.14~	LVDS2_TX0_N	DSO	FlatLink Channel 2 LVDS Data0 NEG	SN65DSI84.A3
J3.16~	LVDS2_TX1_P	DSO	FlatLink Channel 2 LVDS Data1 POS	SN65DSI84.B4
J3.18~	LVDS2_TX1_N	DSO	FlatLink Channel 2 LVDS Data1 NEG	SN65DSI84.A4
J3.31~	LVDS2_TX2_P	DSO	FlatLink Channel 2 LVDS Data2 POS	SN65DSI84.B5
J3.29~	LVDS2_TX2_N	DSO	FlatLink Channel 2 LVDS Data2 NEG	SN65DSI84.A5
J3.20~	LVDS2_TX3_P	DSO	FlatLink Channel 2 LVDS Data3 POS	SN65DSI84.B7
J3.22~	LVDS2_TX3_N	DSO	FlatLink Channel 2 LVDS Data3 NEG	SN65DSI84.A7
J3.23~	LVDS2_CLK_P	DSO	FlatLink Channel 2 LVDS Clock POS	SN65DSI84.B6
J3.25~	LVDS2_CLK_N	DSO	FlatLink Channel 2 LVDS Clock NEG	SN65DSI84.A6

NOTE

- ***"~"*** Denote pin function available with ***"LD" Configuration***.

6.2. Camera Interface

6.2.1. MIPI Camera Serial Interface

The CSI-2 Host Controller is a digital core that implements all protocol functions defined in the MIPI CSI-2 specification, providing an interface between the system and the MIPI D-PHY, allowing communication with an MIPI CSI-2 compliant camera sensor.

The MIPI-CSI2 Controller has the following key features:

- Implements all three CSI-2 MIPI layers (Pixel to byte packing, low level protocol, Lane management)
- Compliant to MIPI D-PHY standard specification V1.1 and Samsung D-PHY
- Supports unidirectional Master operation
- Transmitter and receiver versions
- Scalable data lane support, 1 to 4 Data Lanes
- Supports high speed mode (80Mbps - 1.5Gbps) per lane, providing 4K@30fps capability for the 4 lanes
- Supports 10Mbps data rate in low power mode
- Support 5M pixel at 15 fps, 1080p30, 720p60, VGA at 60 fp
- Includes high speed deserializers
- Loopback testability support
- Support for all CSI-2 data types:
  - Legacy YUV420 8 bit
  - YUV422 8 bit, YUV422 10 bit
  - RGB444, RGB555, RGB565, RGB666, RGB888,
  - RAW6, RAW7, RAW8, RAW10, RAW12, RAW14
  - User Defined Data Types
- Virtual Channel support
- Support for DPHY Ultra Low Power State (ULPS)
- Error collection support (Rx Only)
- Flexible pixel-based user interface
- Supports user generated packets
- Supports single, double, or quad pixel interface
- Supports PHY Protocol Interface (PPI) compatible MIPI D-PHYs
- Delivered fully integrated and verified with target MIPI D-PHY
- RX Video Interface
- APB Control and Status Register (CSR) interface with IRQ support
- Easy configuration and control via core ports
- Optimized for use in FPGAs and ASICs

6.2.2. MIPI-CSI2 Signals

The DART-MX8M exposes both CSI-2 port of the iMX 8M SOC.
The following table list the interface pinout for MIPI-CSI2 port 1 and port 2.

4.2.2.1. MIPI-CSI2 Port 1 Signals

Table 13: MIPI-CSI2 P1 Signals

PIN#	PIN Function	Type	Description	BALL
J1.81	CSI_P1_DP0	DSI	MIPI-CSI Port 1 Data 0 POS	SOC.B23
J1.83	CSI_P1_DN0	DSI	MIPI-CSI Port 1 Data 0 NEG	SOC.A23
J1.73	CSI_P1_DP1	DSI	MIPI-CSI Port 1 Data 1 POS	SOC.D22
J1.75	CSI_P1_DN1	DSI	MIPI-CSI Port 1 Data 1 NEG	SOC.C22
J1.79	CSI_P1_DP2	DSI	MIPI-CSI Port 1 Data 2 POS	SOC.C23
J1.77	CSI_P1_DN2	DSI	MIPI-CSI Port 1 Data 2 NEG	SOC.B24
J1.69	CSI_P1_DP3	DSI	MIPI-CSI Port 1 Data 3 POS	SOC.D21
J1.71	CSI_P1_DN3	DSI	MIPI-CSI Port 1 Data 3 NEG	SOC.C21
J1.87	CSI_P1_CKP	DSI	MIPI-CSI Port 1 Clock POS	SOC.B22
J1.89	CSI_P1_CKN	DSI	MIPI-CSI Port 1 Clock NEG	SOC.A22

4.2.2.2. MIPI-CSI2 Port 2 Signals

Table 14: MIPI-CSI2 P2 Signals

PIN#	PIN Function	Type	Description	BALL
J3.70	CSI_P2_CKN	DSI	MIPI-CSI Port 2 Data 0 POS	SOC.A19
J3.72	CSI_P2_CKP	DSI	MIPI-CSI Port 2 Data 0 NEG	SOC.B19
J3.76	CSI_P2_DN3	DSI	MIPI-CSI Port 2 Data 1 POS	SOC.C19
J3.78	CSI_P2_DP3	DSI	MIPI-CSI Port 2 Data 1 NEG	SOC.D19
J3.80	CSI_P2_DN1	DSI	MIPI-CSI Port 2 Data 2 POS	SOC.A20
J3.82	CSI_P2_DP1	DSI	MIPI-CSI Port 2 Data 2 NEG	SOC.B20
J3.84	CSI_P2_DN0	DSI	MIPI-CSI Port 2 Data 3 POS	SOC.C20
J3.86	CSI_P2_DP0	DSI	MIPI-CSI Port 2 Data 3 NEG	SOC.D20
J3.88	CSI_P2_DN2	DSI	MIPI-CSI Port 2 Clock POS	SOC.A21
J3.90	CSI_P2_DP2	DSI	MIPI-CSI Port 2 Clock NEG	SOC.B21

6.3. Ethernet Interface

The DART-MX8M exposes two **optional** interfaces on the same pins depending on the configuration:

- MDI lines driven by the AR8033 Gigabit PHY – ***"EC" Configuration***
- RGMII signal driven by the SOC – **No *"EC" Configuration***

The SOC core implements a triple-speed 10/100/1000-Mbit/s Ethernet MACs compliant with the IEEE802.3-2002 standard.

The i.MX8M processor also consists of HW support for **IEEE1588** standard.

6.3.1. Ethernet PHY

The On SOM Atheros AR8033 Gigabit PHY in conjunction with external magnetics on carrier board complete the interface to the media.

6.3.1.1. Gigabit Ethernet Signals

Table 15: Ethernet PHY Signals

PIN#	PIN Function	Type	Description	BALL
J1.8~	ETH_TRX0_P	DSAIO	Ethernet Lane 0 POS	AR8033.11
J1.6~	ETH_TRX0_N	DSAIO	Ethernet Lane 0 NEG	AR8033.12
J1.2~	ETH_TRX1_P	DSAIO	Ethernet Lane 1 POS	AR8033.14
J1.4~	ETH_TRX1_N	DSAIO	Ethernet Lane 1 NEG	AR8033.15
J1.10~	ETH_TRX2_P	DSAIO	Ethernet Lane 2 POS	AR8033.17
J1.12~	ETH_TRX2_N	DSAIO	Ethernet Lane 2 NEG	AR8033.18
J1.14~	ETH_TRX3_P	DSAIO	Ethernet Lane 3 POS	AR8033.20
J1.16~	ETH_TRX3_N	DSAIO	Ethernet Lane 3 NEG	AR8033.21
J1.5~	LED_LINK10_100	O	Activity LED for 10Mbps/100Mbps	AR8033.26
J1.7~	LED_LINK1000	O	Activity LED, Active High Part of AR8033 Boot Strap - 10K PD on SOM	AR8033.24
J1.9~	LED_ACT	O	Activity LED, Active High Part of AR8033 Boot Strap - 10K PD on SOM	AR8033.23

NOTE

"~" Denotes pins available on DART-MX8M connector with ***"EC" configuration***.

Table 16: Ethernet PHY LED Behavior

Symbol	10M link	10M active	100M link	100M active	1000M link	1000M active
LED_10_100	OFF	OFF	ON	ON	OFF	OFF
LED_1000	OFF	OFF	OFF	OFF	ON	ON
LED_ACT	ON	BLINK	ON	BLINK	ON	BLINK
ON = active; OFF = inactive						

6.3.2. 10/100/1000Mbps Ethernet MAC(ENET) Signals

Table 17: RGMII Signals

PIN#	PIN Function	Type	Description	BALL
J1.4*~	ENET_TD0	O	ENET RGMII Transmit Data 0	SOC.R20
J1.2*~	ENET_TD1	O	ENET RGMII Transmit Data 1	SOC.R21
J1.6*~	ENET_TD2	O	ENET RGMII Transmit Data 2	SOC.R19
J1.8*~	ENET_TD3	O	ENET RGMII Transmit Data 3	SOC.P20
J1.5*~	ENET_TXC	O	ENET RGMII Transmit Clock: 125MHz @ 1000Mbps / 25MHz @ 100Mbps / 2.5MHz @ 10Mbps Samples TD[3:0] and TX_CTL	SOC.T19
J1.3*~	ENET_TX_CTL	O	ENET RGMII Transmit data Control	SOC.P19
J1.10*~	ENET_RD0	I	ENET RGMII Receive Data 0	SOC.U19
J1.12*~	ENET_RD1	I	ENET RGMII Receive Data 1	SOC.U21
J1.14*~	ENET_RD2	I	ENET RGMII Receive Data 2	SOC.U20
J1.16*~	ENET_RD3	I	ENET RGMII Receive Data 3	SOC.V19
J1.7*~	ENET_RXC	I	ENET RGMII Receive Clock: 125MHz @ 1000Mbps / 25MHz @ 100Mbps / 2.5MHz @ 10Mbps Samples RD[3:0] and RX_CTL	SOC.T20
J1.9*~	ENET_RX_CTL	I	ENET RGMII Receive data Control	SOC.T21

NOTE

"~" Denotes interface available on DART-MX8M connector without ***"EC" configuration***.
"*" Denotes pins with alternative functions selected using the PINMUX

6.3.3. MDIO & 1588 Signals

Table 18: MDIO & 1588 Signals

PIN#	PIN Function	Type	Description	BALL
J1.11*	ENET_MDIO	IO	**Note: Used internally in SOM with *"EC" Configuration*** Management Interface data bidirectional Require without ***"EC" Configuration*** external 1.5K PU to NVCC_3V3	SOC.N19
J1.13*	ENET_MDC	O	**Note: Used internally in SOM with *"EC" Configuration*** Management Interface clock used to strobe MDIO line	SOC.N20
J3.60*	ENET_1588_ EVENT0_IN	I	SOC MAC Core 1588 Event input - option 0	SOC.N7
J2.30*	ENET_1588_ EVENT1_OUT	O	SOC MAC Core 1588 Event output - option 1 Should be used in conjunction with EVENT1_OUT	SOC.F7
J2.32*	ENET_1588_ EVENT1_IN	I	SOC MAC Core 1588 Event input - option 1 Should be used in conjunction with EVENT1_IN	SOC.G7

NOTE

"*" Denotes pins with alternative functions selected using the PINMUX

6.4. Wi-Fi & BT & MMC/SD/SDIO

The DART-MX8M contains a certified high-performance Wi-Fi and Bluetooth(BT) module:

- IEEE 802.11 ac/a/b/g/n
- Bluetooth 2.1+EDR
- BLE 4.2 capabilities
- Modules have an antenna connection through a U.FL JACK connector
- Antenna cable connected to module must have 50-Ω impedance

Figure 5 illustrates the DART-MX8M internal Wi-Fi and BT connectivity.

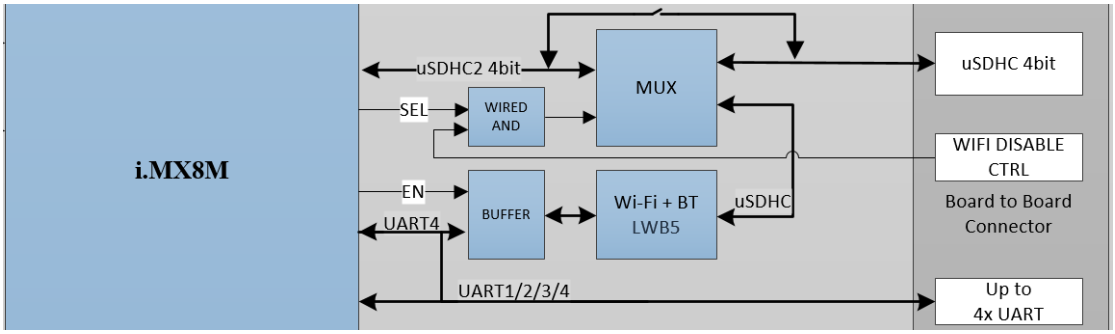

Figure 5: DART-MX8M Wi-Fi & BT Internal Connection

To allow the most flexible solution the following elements are added to the DART-MX8M:

- Tristate buffer on the BT link based on UART interface.
  Will allow isolation from the LWB5 module and the use by external circuity via the DART-MX8M connector.
- Multiplexer is used on the uSDHC2 (SOC SD2 interface) 4-bit bus controlled using an internal GPIO with conjunction to an external user control.

NOTE

- BT UART tristate buffer controlled using SD2_WP pin alternate function GPIO2_IO20.
  A logic "Low" enables the buffer.
- Multiplexer controlled using NAND_CE1_B alternate function GPIO3_IO02.
  A "High" connects the SD2 interface to the Wi-Fi SDIO lines.
  A "Low" connect the SD2 interface to the connector CONN_SD2 line.
  CONN_WI-FI_DISn line on pin J1.72 will override GPIO3_IO02 and force the SD2 interface. This is helpful in cases SD card boot is required, by pulling the line "Low" on boot.

6.4.1. Interface implementation options

6.4.1.1. Module configuration **with "WBD"** option

- System use: **Wi-Fi and Bluetooth**.
  - All external pins of the interfaces should float.
- System use: **Wi-Fi and no BT**.

- In this case, disable the BT buffer and BT function.
- BT UART interface pins can be used externally with any of the alternative functions.

- System use: **BT and no Wi-Fi**.
  - In this case, SET the SDIO multiplexer to the connector state and disable the Wi-Fi interface.
  - SD2 lines can be connected externally.

6.4.1.2. Module configuration **without "WBD"** option

- System use: **No Wi-Fi and no BT**.
  - SDIO signals bypassed and BT buffer not assembled.
  - All the interfaces are accessible externally with alternative functions.

A second available interface, SD2 used by the SOM for the internal eMMC boot and storage.

6.4.1.3. SD Card recovery & development

To allow SD Card recovery and to ease the development process, booting from the SD card must be done with the kernel that does not have W-Fi module definitions inside i.e. Wi-Fi interface is not accessible when booting from SD card.

6.4.2. Bluetooth Interface signals

Table 19: BT UART interface signals

PIN#	PIN Function	Type	Description	BALL
J2.20*	UART4_TXD	O	**Note: Used internally in SOM with *"WBD" Configuration,* But internal use can be released by GPIO control** SOC UART4 Transmit Data	SOC.E5
J2.22*	UART4_CTS_B	O	**Note: Used internally in SOM with *"WBD" Configuration*, BUT internal use can be released by GPIO control** SOC UART4 Clear To Send	SOC.B5
J2.24*	UART4_RXD	I	**Note: Used internally in SOM with *"WBD" Configuration*, BUT internal use can be released by GPIO control** SOC UART4 Receive Data	SOC.C5
J2.26*	UART4_RTS_B	I	**Note: Used internally in SOM with *"WBD" Configuration*, BUT internal use can be released by GPIO control** SOC UART4 Ready to Send	SOC.A5

NOTE

"*" Denotes pins with alternative functions selected using the PINMUX

6.4.3. SD2 Interface signals

The exposed uSDHC controller (SD2) can only support up to a 4-bit interface designed to support:

- SD/SDIO standard, up to version 3.0.
- MMC standard, up to version 5.0.
- 1.8 V and 3.3 V operation, but do not support 1.2 V operation
- 1-bit/4-bit SD and SDIO modes, 1-bit/4-bit MMC mode
- Up to SDR104 rate

The uSDHC controller (SD1) can support up to an 8-bit interface is used internally for the eMMC interface on the SOM.

Table 20: SD2 interface signals

PIN#	PIN Function	Type	Description	BALL
J1.1*	REF_CLK_32K	O	**Note: Used internally in SOM with *"WBD" Configuration*** Can be shared for external devices requiring this clock, with high impedance inputs.	SOC.T6
J1.28*	SD2_RESET_B	O	When using SOC SD2 external interface for SD card, should be used to control the SD card power in order to perform RESET function.	SOC.R22
J1.72	CONN_WIFI_DISN	I	When asserted "LOW", will force the internal SOC SD2 routing of data[3:0], clock and command lines to J1	
J1.74*	SD2_CD_B	I	**Note: Requires a PU to NVCC_SD2_1V8_3V3** SD2 card detect. PU should be used on this line when connected to an SD card socket CD switch.	SOC.L21
J1.82*	SD2_CLK	O	SD2 interface clock signal	SOC.L22
J1.88*	SD2_CMD	IO	**Note: Requires a PU to NVCC_SD2_1V8_3V3** SD2 interface command signal	SOC.M22
J1.86*	SD2_DATA0	IO	SD2 interface data 0 signal	SOC.N22
J1.80*	SD2_DATA1	IO	SD2 interface data 0 signal	SOC.N21
J1.78*	SD2_DATA2	IO	SD2 interface data 0 signal	SOC.P22
J1.84*	SD2_DATA3	IO	SD2 interface data 0 signal	SOC.P21
J1.90	NVCC_SD2_1V8_3V3	PO	Internal SOM power driving SD2 interface SOC IOs'. Use for PU resistor on SD2_CD_B and SD2_CMD lines.	POWER OUT

NOTE

"*" Denotes pins with alternative functions selected using the PINMUX

6.5. USB Ports

Two USB controllers and PHYs that support USB 3.0 and USB 2.0 interfaces are exposed on the DART-MX8M connectors.

Each USB 3.0 module includes the following features:

- Complies with USB specification rev 3.0 (xHCI compatible)
- Can operate in both 3.0 and 2.0 mode
- Supports operation as a standalone USB host controller
- USB dual-role operation and can be configured as host or device
- Super-speed (5 Gbit/s), high-speed (480 Mbit/s), full-speed (12 Mbit/s), and low speed (1.5 Mbit/s) operations.
- Supports operation as a standalone single port USB
- Supports four programmable, bidirectional USB endpoints
- OTG (on-the-go) 2.0 compliant, which includes both device and host capability.
- Super-speed operation is not supported when OTG is enabled

6.5.1. USB3 Modes of Operation

The USB 3.0 module operates in following modes.

- Host Mode: SS/HS/FS/LS
- Device Mode: SS/HS/FS
- OTG: HS/FS/LS

6.5.2. USB interface signals

Table 21: USB3.0/2.0 Port 1 & 2 Interface signals

PIN#	PIN Function	Type	Description	BALL
J3.66	USB1_VBUS	PI	USB PHY VBUS - 5V tolerant	SOC.D14
J3.53	USB1_RXN	DSI	USB PHY 3.0 SS Receive Data NEG	SOC.B12
J3.55	USB1_RXP	DSI	USB PHY 3.0 SS Receive Data POS	SOC.A12
J3.59	USB1_TXN	DSO	USB PHY 3.0 SS Transmit Data NEG	SOC.B13
J3.61	USB1_TXP	DSO	USB PHY 3.0 SS Transmit Data POS	SOC.A13
J3.56	USB1_ID	I	USB PHY ID Detect	SOC.C14
J3.65	USB1_DP	DSIO	USB PHY 2.0 Data POS	SOC.A14
J3.67	USB1_DN	DSIO	USB PHY 2.0 Data NEG	SOC.B14
J3.26	USB2_VBUS	PI	USB PHY VBUS - 5V tolerant	SOC.D9
J3.35	USB2_RXN	DSI	USB PHY 3.0 SS Receive Data NEG	SOC.B8
J3.37	USB2_RXP	DSI	USB PHY 3.0 SS Receive Data POS	SOC.A8
J3.41	USB2_TXN	DSO	USB PHY 3.0 SS Transmit Data NEG	SOC.B9
J3.43	USB2_TXP	DSO	USB PHY 3.0 SS Transmit Data POS	SOC.A9
J3.44	USB2_ID	I	USB PHY ID Detect	SOC.C9
J3.47	USB2_DP	DSIO	USB PHY 2.0 Data POS	SOC.A10
J3.49	USB2_DN	DSIO	USB PHY 2.0 Data NEG	SOC.B10

6.5.3. USB OTG interface signals

Table xx list the available DART-MX8M exposed pins, which can be optionally used to implement a complete OTG functions.

Table 22: USB Port 1 & 2 OTG Interface signals

PIN#	PIN Function	Type	Description	BALL
J3.48*	USB2_OTG_PWR	O	USB Port 2 OTG PWR signal, active high control signal used to enable power to the downstream port.	SOC.K7
J3.38*	USB2_OTG_OC	I	USB Port 2 OTG OC signal indicates that an overcurrent condition from an external current monitor on the downstream port occurred.	SOC.J6
J3.30*	USB2_OTG_ID	I	**Note: Used internally in SOM with *"LD" Configuration*** USB Port 2 OTG ID signal. "Low" means the SOC is Host role "High" means the SOC is Peripheral role.	SOC.L6
J3.50*	USB1_OTG_PWR	O	USB Port 1 OTG PWR signal	SOC.L7
J3.40*	USB1_OTG_OC	I	USB Port 1 OTG OC signal	SOC.K6
J3.52*	USB1_OTG_ID	I	USB Port 1 OTG ID signal.	SOC.M7

NOTE

"*" Denotes pins with alternative functions selected using the PINMUX

6.6. PCIe

DART-MX8M PCI exposes two PCI Express GEN 2 single lane interfaces. Each PCI Express port requires an external 100MHz PCIe compliant reference clock.

PCI port features:

- Dual mode (DM) controller provides a solution to implement a PCI Express port for a PCI Express root complex or endpoint application.
- Port solution includes the controller, an analog PHY macro, and application logic to source and sink data.
- PCI Express base specification 2.1 with maximum 5.0Gbps lane rate.
- Native PCIe PM Mechanisms

The PCIe controller implements the following standards:

- PCI Express Base Specification, Revision 4.0, Version 0.7
- PIPE Specification for PCI Express, Version 4.3, Intel Corporation
- PCI Local Bus Specification, Revision 3.0
- PCI Bus Power Management Specification, Revision 1.2
- PCI Express Card Electromechanical Specification, Revision 1.1

Note: Access to the above specification requires membership in PCI-SIG.

6.6.1. PCIE Signals

Table 23: PCIE Port 1 & 2 Signals

PIN#	PIN Function	Type	Description	BALL
J1.51	PCIE1_REF_CLKN	DSI	PCIE compliant 100MHz reference clock POS Terminate with 49.9 Ohm close to the connector	SOC.K24
J1.53	PCIE1_REF_CLKP	DSI	PCIE compliant 100MHz reference clock NEG Terminate with 49.9 Ohm close to the connector	SOC.K25
J1.57	PCIE1_TXN	DSO	PCIE GEN2.1 Transmit Data POS	SOC.J24
J1.59	PCIE1_TXP	DSO	PCIE GEN2.1 Transmit Data NEG	SOC.J25
J1.60	PCIE1_RXN	DSI	PCIE GEN2.1 Receive Data POS	SOC.H24
J1.62	PCIE1_RXP	DSI	PCIE GEN2.1 Receive Data NEG	SOC.H25
J1.54	PCIE2_REF_CLKN	DSI	PCIE compliant 100MHz reference clock POS Terminate with 49.9 Ohm close to the connector	SOC.F24
J1.56	PCIE2_REF_CLKP	DSI	PCIE compliant 100MHz reference clock NEG Terminate with 49.9 Ohm close to the connector	SOC.F25
J1.66	PCIE2_TXN	DSO	PCIE GEN2.1 Transmit Data POS	SOC.E24
J1.68	PCIE2_TXP	DSO	PCIE GEN2.1 Transmit Data NEG	SOC.E25
J1.63	PCIE2_RXN	DSI	PCIE GEN2.1 Receive Data POS	SOC.D24
J1.65	PCIE2_RXP	DSI	PCIE GEN2.1 Receive Data NEG	SOC.D25

6.6.2. PCIE Side band signals

Table 24: PCIE Side band signals

PIN#	PIN Function	Type	Description	BALL
J1.17*	PCIE1_CLKREQ_B	I	PCIE Port 1 Clock Request Signal	SOC.F8
J1.19*	PCIE2_CLKREQ_B	I	PCIE Port 2 Clock Request Signal	SOC.F9
J1.3*	PCIE1_CLKREQ_B	I	PCIE Port 1 Clock Request Signal	SOC.C6
J1.1*	PCIE2_CLKREQ_B	I	PCIE Port 2 Clock Request Signal	SOC.D7

NOTE

"*" Denotes pins with alternative functions selected using the PINMUX

6.7. Audio

The DART-MX8M features two types of audio interfaces:

- WM8904 Audio codec Analog outputs & input interfaces:
  - Stereo line input
  - Stereo HP output
  - Digital microphone input
- **S**ynchronous **A**udio **I**nterface (SAI)
- **S**ony **P**hilips **D**igital **I**nter**F**ace (SPDIF)

6.7.1. Analog Audio

Analog audio signals are part of the SOM WM8904 audio codec, available with ***"AC" Configuration*** only.

The Codec features stereo ground-referenced headphone amplifiers using the Wolfson 'Class-W' amplifier techniques -incorporating an innovative dual-mode charge pump architecture - to optimize efficiency and power consumption during playback. The ground-referenced headphone and line outputs eliminate AC coupling capacitors, and both outputs include common mode feedback paths to reject ground noise.

Figure 6 illustrates the connectivity for no large AC coupling capacitors

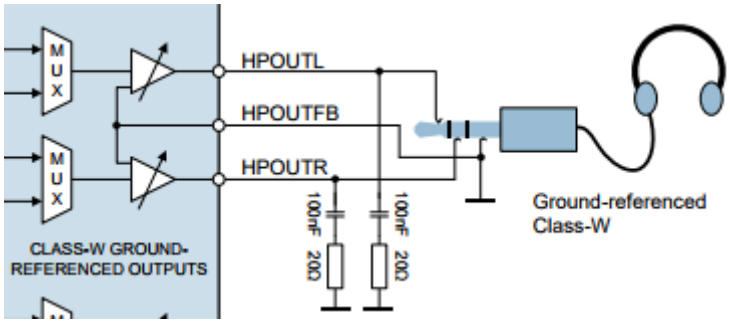

Figure 6: WM8904 Headphone connectivity

Refer to the data sheet for detailed electrical characteristics of the relevant interfaces
https://www.cirrus.com/products/wm8904/

Table 25: Analog Audio Signals

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PIN#	PIN Function	Type	Description	BALL
J3.2~	HPLOUT	AO	Left headphone output (line or headphone output)	WM8904.13
J3.4~	HPROUT	AO	Right headphone output (line or headphone output)	WM8904.15
J3.6~	HPOUTFB	AI	Headphone output ground loop noise rejection feedback	WM8904.14
J3.8~	LINEIN1_LP	AI	Left channel input	WM8904.26
J3.10~	LINEIN1_RP	AI	Right channel input	WM8904.24
J3.14~	DMIC_CLK	O	Digital microphone clock output	WM8904.1
J3.16~	DMIC_DATA	I	Digital microphone data input	WM8904.27
J3.12~	AGND	P	Audio interface ground reference	AUDIO AGND

NOTE

"~" Denotes interface available on DART-MX8M connector with ***"AC" configuration***.

6.7.2. SAI - Synchronous Audio Interface

The I2S (or I2S) module of the iMX 8M SOC, provides a synchronous audio interface (SAI) that supports fullduplex serial interfaces with frame synchronization such as I2S, AC97, TDM, and codec/DSP interfaces.

Main Features of the SAI include:

- Transmitter with independent bit clock and frame sync supporting 1 data line
- Receiver with independent bit clock and frame sync supporting 1 data line
- Each data line can support a maximum Frame size of 32 words
- Word size of between 8-bits and 32-bits
- Word size configured separately for first word and remaining words in frame
- Asynchronous 128 × 32-bit FIFO for each transmit and receive data line
- Supports graceful restart after FIFO error
- Supports automatic restart after FIFO error without software intervention
- Supports packing of 8-bit and 16-bit data into each 32-bit FIFO word

NOTE

Some of the features are not supported across all SAI instances; See i.MX 8M Applications Processors Reference Manual for further details.

Besides the general audio input/output function, the audio interfaces will support the following features:

- SAI-1 supports up to 16-channels TX (8 lanes) and 16-channels RX (8 lanes) at 384KHz/32-bit
- SAI-5 supports up to 8-channels TX (4 lanes) and 8-channels RX (4 lanes) at 384KHz/32-bit
- SAI-2/3/6 supports up to 2-channels TX (1 lanes) and 2-channels RX (1 lanes) at 384KHz/32-bit
- SAI-2/3/6 support up to 2-channels TX (1 lane) and 2-channels RX (1 lane) at 384KHz/32-bit
- SAI-1 supports glue-less switching between PCM and DSD operation for popular audio DACs
- SPDIF-1/2 supports raw capture mode that can save all the incoming bits into audio buffer

The DART-MX8M exposes all 5 SAI interfaces the iMX 8M SOC presents.

SAI3 interface used on SOM with ***"AC" Configuration*** for the Analog Audio interface, see section 6.7.1, can be available on the connector pins without "***AC" Configuration.***

The SAI-1/2/3/5/6 and SPDIF-1 share GPIO pads on the chip through IOMUX. Common **U**se **C**ases (UC) supported by the audio interfaces are listed in the table below (many other configurations are possible). The number is the data lanes supported.

The following tables list some common use cases, with and without ***"AC" Configuration*** ordering code.

Table 26: SAI Common Use Cases without *"AC" Configuration*

SAI#	DIR	UC1	UC2	UC3	UC4	UC5	UC6	UC7	UC8
SAI-1	TX	8	8	8	8	8	8	4	4
	RX	8	8	8	8	8	8	4	4
SAI-2	TX	1		1		1	1		1
	RX	1		1		1	1		1
SAI-3	TX	1			1	1	1	1	1
	RX	1			1	1	1	1	1
SAI-5	TX		4		4	1		4	1
	RX		4	4	4	1	4	4	1
SAI-6	TX	1						1	1
	RX	1						1	1
SPDIF	TX	1	1	1	1	1	1	1	1
	RX	1	1	1	1	1	1	1	1

Table 27: SAI Common Use Cases with *"AC" Configuration*

SAI#	DIR	UC1			UC4	UC5	UC6	UC7	UC8
SAI-1	TX	8			8	8	8	4	4
	RX	8			8	8	8	4	4
SAI-2	TX	1				1	1		1
	RX	1				1	1		1
SAI-5	TX				4	1		4	1
	RX				4	1	4	4	1
SAI-6	TX	1						1	1
	RX	1						1	1
SPDIF	TX	1	1	1	1	1	1	1	1
	RX	1	1	1	1	1	1	1	1

NOTE

Analog Audio interface available on DART-MX8M connector with ***"AC" configuration***.
In this case, do not alter the PINMUX functionality of SAI3 pins.

6.7.2.1. SAI Signals Definitions

The following table details the SAI interface signals definition.

Table 28: SAI interface signals definition

Name	Function	DIR
SAI_TXC	**Transmit Bit Clock.** The bit clock is an input when externally generated and an output when internally generated.	I/O
SAI_TXFS	**Transmit Frame Sync.** The frame sync is an input sampled synchronously by the bit clock when externally generated and an output generated synchronously by the bit clock when internally generated.	I/O
SAI_TXD[0:0]	**Transmit Data.** The transmit data is generated synchronously by the bit clock and is tristate whenever not transmitting a word	O
SAI_RXC	**Receive Bit Clock.** The bit clock is an input when externally generated and an output when internally generated.	I/O
SAI_RXFS	**Receive Frame Sync.** The frame sync is an input sampled synchronously by the bit clock when externally generated and an output generated synchronously by the bit clock when internally generated.	I/O
SAI_RXD [0:0]	**Receive Data.** The receive data is sampled synchronously by the bit clock.	I
SAI_MCLK	**Audio Master Clock**.	I

6.7.2.2. SAI1 Signals

Table 29: SAI1 Signals

PIN#	PIN Function	Type	Description	BALL
J2.82*	SAI1_MCLK	O	SAI1 Master Clock	SOC.A3
J2.55*	SAI1_RXFS	IO	SAI1 Receive Frame Sync.	SOC.L1
J2.69*	SAI1_RXFS	IO	SAI1 Receive Frame Sync.	SOC.F1
J2.57*	SAI1_RXC	IO	SAI1 Receive Bit Clock	SOC.K1
J2.61*^	SAI1_RXD0	I	SAI1 Receive Data 0	SOC.K2
J2.59*^	SAI1_RXD1	I	SAI1 Receive Data 1	SOC.L2
J2.63*^	SAI1_RXD2	I	SAI1 Receive Data 2	SOC.H2
J2.62*^	SAI1_RXD3	I	SAI1 Receive Data 3	SOC.J2
J2.65*^	SAI1_RXD4	I	SAI1 Receive Data 4	SOC.J1
J2.69*^	SAI1_RXD5	I	SAI1 Receive Data 5	SOC.F1
J2.66*^	SAI1_RXD6	I	SAI1 Receive Data 6	SOC.G2
J2.68*^	SAI1_RXD7	I	SAI1 Receive Data 7	SOC.G1
J2.64*	SAI1_TXFS	IO	SAI1 Transmit Frame Sync.	SOC.H1
J2.38*	SAI1_TXFS	IO	SAI1 Transmit Frame Sync.	SOC.M4
J2.42*	SAI1_TXFS	IO	SAI1 Transmit Frame Sync.	SOC.L4

PIN#	PIN Function	Type	Description	BALL
J2.44*	SAI1_TXFS	IO	SAI1 Transmit Frame Sync.	SOC.K5
J2.68*	SAI1_TXFS	IO	SAI1 Transmit Frame Sync.	SOC.G1
J2.72*	SAI1_TXC	IO	SAI1 Transmit Bit Clock	SOC.E1
J2.46*	SAI1_TXC	IO	SAI1 Transmit Bit Clock	SOC.K4
J2.82*	SAI1_TXC	IO	SAI1 Transmit Bit Clock	SOC.A3
J2.70*^	SAI1_TXD0	O	SAI1 Transmit Data 0	SOC.F2
J2.34	SAI1_TXD0	O	SAI1 Transmit Data 0	SOC.N4
J2.67*^	SAI1_TXD1	O	SAI1 Transmit Data 1	SOC.E2
J2.40*	SAI1_TXD1	O	SAI1 Transmit Data 1	SOC.L5
J2.78*^	SAI1_TXD2	O	SAI1 Transmit Data 2	SOC.B2
J2.36*	SAI1_TXD2	O	SAI1 Transmit Data 2	SOC.M5
J2.73*^	SAI1_TXD3	O	SAI1 Transmit Data 3	SOC.D1
J2.42*	SAI1_TXD3	O	SAI1 Transmit Data 3	SOC.L4
J2.74*^	SAI1_TXD4	O	SAI1 Transmit Data 4	SOC.D2
J2.38*	SAI1_TXD4	O	SAI1 Transmit Data 4	SOC.M4
J2.68*	SAI1_TXD4	O	SAI1 Transmit Data 4	SOC.G1
J2.71*^	SAI1_TXD5	O	SAI1 Transmit Data 5	SOC.C2
J2.44*	SAI1_TXD5	O	SAI1 Transmit Data 5	SOC.K5
J2.80*^	SAI1_TXD6	O	SAI1 Transmit Data 6	SOC.B3
J2.76*^	SAI1_TXD7	O	SAI1 Transmit Data 7	SOC.C1

NOTE

"*" Denotes pins with alternative functions selected using the PINMUX

"^" Denotes pins which are **latched after reset for BOOT CONFIGURATION**, See section 6.18.1 for detailed information.

6.7.2.3. SAI2 Signals

Table 30: SAI2 Signals

PIN#	PIN Function	Type	Description	BALL
J2.54*	SAI2_MCLK	O	SAI2 Master Clock	SOC.H5
J2.48*	SAI2_RXFS	IO	SAI2 Receive Frame Sync.	SOC.J4
J2.50*	SAI2_RXC	IO	SAI2 Receive Bit Clock	SOC.H3
J2.58*	SAI2_RXD0	I	SAI2 Receive Data 0	SOC.H6
J2.52*	SAI2_TXFS	IO	SAI2 Transmit Frame Sync.	SOC.H4
J2.56*	SAI2_TXC	IO	SAI2 Transmit Bit Clock	SOC.J5
J2.60*	SAI2_TXD0	O	SAI2 Transmit Data 0	SOC.G5

NOTE

"*" Denotes pins with alternative functions selected using the PINMUX

6.7.2.4. SAI3 Signals

Table 31: SAI3 Signals

PIN#	PIN Function	Type	Description	BALL
J2.16*~	SAI3_MCLK	O	SAI3 Master Clock	SOC.D3
J2.6*~	SAI3_RXFS	IO	SAI3 Receive Frame Sync.	SOC.G4
J2.8*~	SAI3_RXC	IO	SAI3 Receive Bit Clock	SOC.F4
J2.14*~	SAI3_RXD	I	SAI3 Receive Data 0	SOC.F3
J2.10*~	SAI3_TXFS	IO	SAI3 Transmit Frame Sync.	SOC.G3
J2.4*~	SAI3_TXC	IO	SAI3 Transmit Bit Clock	SOC.C4
J2.2*~	SAI3_TXD	O	SAI3 Transmit Data 0	SOC.C3

NOTE

"*" Denotes pins with alternative functions selected using the PINMUX

"~" Denotes interface available on DART-MX8M connector without ***"AC" configuration***.

6.7.2.5. SAI5 Signals

Table 32: SAI5 Signals

PIN#	PIN Function	Type	Description	BALL
J2.46*	SAI5_MCLK	O	SAI5 Master Clock	SOC.K4
J2.54	SAI5_MCLK	O	SAI5 Master Clock	SOC.H5
J2.82	SAI5_MCLK	O	SAI5 Master Clock	SOC.A3
J2.16*~	SAI5_MCLK	O	SAI5 Master Clock	SOC.D3
J2.34*	SAI5_RXFS	IO	SAI5 Receive Frame Sync.	SOC.N4
J2.55	SAI5_RXFS	IO	SAI5 Receive Frame Sync.	SOC.L1
J2.6*~	SAI5_RXFS	IO	SAI5 Receive Frame Sync.	SOC.G4
J2.40*	SAI5_RXC	IO	SAI5 Receive Bit Clock	SOC.L5
J2.57*	SAI5_RXC	IO	SAI5 Receive Bit Clock	SOC.K1
J2.8*~	SAI5_RXC	IO	SAI5 Receive Bit Clock	SOC.F4
J2.36*	SAI5_RXD0	I	SAI5 Receive Data 0	SOC.M5
J2.61*	SAI5_RXD0	I	SAI5 Receive Data 0	SOC.K2
J2.14*~	SAI5_RXD0	I	SAI5 Receive Data 0	SOC.F3
J2.42*	SAI5_RXD1	I	SAI5 Receive Data 1	SOC.L4
J2.59*	SAI5_RXD1	I	SAI5 Receive Data 1	SOC.L2
J2.10*~	SAI5_RXD1	I	SAI5 Receive Data 1	SOC.G3
J2.38*	SAI5_RXD2	I	SAI5 Receive Data 2	SOC.M4
J2.63*	SAI5_RXD2	I	SAI5 Receive Data 2	SOC.H2
J2.4*~	SAI5_RXD2	I	SAI5 Receive Data 2	SOC.C4
J2.44*	SAI5_RXD3	I	SAI5 Receive Data 3	SOC.K5
J2.62*	SAI5_RXD3	I	SAI5 Receive Data 3	SOC.J2
J2.2*~	SAI5_RXD3	I	SAI5 Receive Data 3	SOC.C3

PIN#	PIN Function	Type	Description	BALL
J2.48*	SAI5_TXFS	IO	SAI5 Transmit Frame Sync.	SOC.J4
J2.64*	SAI5_TXFS	IO	SAI5 Transmit Frame Sync.	SOC.H1
J2.42*	SAI5_TXFS	IO	SAI5 Transmit Frame Sync.	SOC.L4
J2.50*	SAI5_TXC	IO	SAI5 Transmit Bit Clock	SOC.H3
J2.72*	SAI5_TXC	IO	SAI5 Transmit Bit Clock	SOC.E1
J2.38*	SAI5_TXC	IO	SAI5 Transmit Bit Clock	SOC.M4
J2.58*	SAI5_TXD0	O	SAI5 Transmit Data 0	SOC.H6
J2.70*	SAI5_TXD0	O	SAI5 Transmit Data 0	SOC.F2
J2.44*	SAI5_TXD0	O	SAI5 Transmit Data 0	SOC.K5
J2.52*	SAI5_TXD1	O	SAI5 Transmit Data 1	SOC.H4
J2.67*	SAI5_TXD1	O	SAI5 Transmit Data 1	SOC.E2
J2.56*	SAI5_TXD2	O	SAI5 Transmit Data 2	SOC.J5
J2.78*	SAI5_TXD2	O	SAI5 Transmit Data 2	SOC.B2
J2.60*	SAI5_TXD3	O	SAI5 Transmit Data 3	SOC.G5
J2.73*	SAI5_TXD3	O	SAI5 Transmit Data 3	SOC.D1

NOTE

"*" Denotes pins with alternative functions selected using the PINMUX

"~" Denotes pins, which exposes different functions depending on assembly options.

6.7.2.6. SAI6 Signals

Table 33: SAI6 Signals

PIN#	PIN Function	Type	Description	BALL
J2.76*^	SAI6_MCLK	O	SAI6 Master Clock	SOC.C1
J2.68*^	SAI6_MCLK	IO	SAI6 Receive Frame Sync.	SOC.G1
J2.80*^	SAI6_RXFS	IO	SAI6 Receive Frame Sync.	SOC.B3
J2.66*^	SAI6_RXFS	IO	SAI6 Receive Frame Sync.	SOC.G2
J2.74*^	SAI6_RXC	IO	SAI6 Receive Bit Clock	SOC.D2
J2.65*^	SAI6_RXC	IO	SAI6 Receive Bit Clock	SOC.J1
J2.71*^	SAI6_RXD0	I	SAI6 Receive Data 0	SOC.C2
J2.69*^	SAI6_RXD0	I	SAI6 Receive Data 0	SOC.F1
J2.66*^	SAI6_TXFS	IO	SAI6 Transmit Frame Sync.	SOC.G2
J2.80*^	SAI6_TXFS	IO	SAI6 Transmit Frame Sync.	SOC.B3
J2.65*^	SAI6_TXC	IO	SAI6 Transmit Bit Clock	SOC.J1
J2.74*^	SAI6_TXC	IO	SAI6 Transmit Bit Clock	SOC.D2
J2.69*^	SAI6_TXD0	O	SAI6 Transmit Data 0	SOC.F1
J2.71*^	SAI6_TXD0	O	SAI6 Transmit Data 0	SOC.C2

NOTE

"*" Denotes pins with alternative functions selected using the PINMUX

"^" Denotes pins which are **latched after reset for BOOT CONFIGURATION**, See section 6.18.1 for detailed information.

6.7.3. SPDIF – Sony Philips Digital Interface Format

A standard audio file transfer format, developed jointly by the Sony and Phillips corporations. It supports Transmitter and Receiver functionality including frequency measurement block that allows the precise measurement of an incoming sampling frequency.
The SPDIF receiver extracts the audio data from each SPDIF frame and places the data in the SPDIF Rx left and right FIFOs with Channel Status and User bits.
For the SPDIF transmitter, the audio data is provided by the processor dedicated registers along with Channel Status and User bits.

6.7.3.1. SPDIF Signals

Table 34: SPDIF Signals

PIN#	PIN Function	Type	Description	BALL
J3.28*	SPDIF_RX	I	SPDIF Receive data	SOC.G6
J3.36*	SPDIF_TX	O	SPDIF Receive data	SOC.F6
J3.32*	SPDIF_EXT_CLK	I	SPDIF External Clock (optional)	SOC.E6

NOTE
"*" Denotes pins with alternative functions selected using the PINMUX

6.8. UART Interfaces

The DART-MX8M exposes up to **four** UART interfaces some of which are multiplexed with other peripherals. UART4 is used on SOM for Bluetooth interface and can be accessible only if the on SOM buffer disabled or without ***"WBD" Configuration***.

The UART includes the following features:

- High-speed TIA/EIA-232-F compatible, up to 4 Mbit/s
- Serial IR interface low-speed, IrDA-compatible (up to 115.2 Kbit/s)
- 9-bit or Multidrop mode (RS-485) support (automatic slave address detection)
- 7 or 8 data bits for RS-232 characters, or 9-bit RS-485 format
- 1 or 2 stop bits
- Programmable parity (even, odd, and no parity)
- Hardware flow control support for request to send (RTS_B) and clear to send (CTS_B) signals
- RS-485 driver direction control via CTS_B signal
- Edge-selectable RTS_B and edge-detect interrupts
- Transmitter FIFO empty interrupt suppression
- Can serve both as DTE or DCE device
- Auto baud rate detection (up to 115.2 Kbit/s)
- Receiver and transmitter enable/disable for power saving
- RX_DATA input and TX_DATA output can be inverted respectively in RS-232/RS-485 mode

- RTS_B, IrDA asynchronous wake (AIRINT), receive asynchronous wake (AWAKE) interrupts wake the processor from STOP mode

Table 35: UART I/O Configuration vs. mode

Port	DTE Mode		DCE Mode	
	Direction	Description	Direction	Description
UARTx_RTS_B	Output	UARTx_RTS_B from DTE to DCE	Input	UARTx_RTS_B from DTE to DCE
UARTx_CTS_B	Input	UARTx_CTS_B from DCE to DTE	Output	UARTx_CTS_B from DCE to DTE
UARTx_TX_ DATA	Input	Serial data from DCE to DTE	Output	Serial data from DCE to DTE
UARTx_RX _DATA	Output	Serial data from DTE to DCE	Input	Serial data from DTE to DCE

6.8.1.1. UART1 Signals

Table 36: UART1 Signals

PIN#	PIN Function	Type	Description	BALL
J2.88*	UART1_RXD	I/O	UART Receive Data Input DCE mode / Output DTE mode	SOC.C7
J2.90*	UART1_TXD	O/I	UART Transmit Data Output DCE mode / Input DTE mode	SOC.A7
J2.89*	UART1_RTS_B	I/O	UART Ready to Send - Active Low Input DCE mode / Output DTE mode	SOC.B7
J2.87*	UART1_CTS_B	O/I	UART Clear to Send - Active Low Output DCE mode / Input DTE mode	SOC.A6

NOTE

"*" Denotes pins with alternative functions selected using the PINMUX

6.8.1.2. UART2 Signals

Table 37: UART2 Signals

PIN#	PIN Function	Type	Description	BALL
J2.85*	UART2_RXD	I/O	UART Receive Data Input DCE mode / Output DTE mode	SOC.B6
J2.86*	UART2_TXD	O/I	UART Transmit Data Output DCE mode / Input DTE mode	SOC.D6
J3.1*	UART2_RTS_B	I/O	UART Ready to Send - Active Low Input DCE mode / Output DTE mode	SOC.D7
J3.3*	UART2_CTS_B	O/I	UART Clear to Send - Active Low Output DCE mode / Input DTE mode	SOC.C6

NOTE

"*" Denotes pins with alternative functions selected using the PINMUX

6.8.1.3. UART3 Signals

Table 38: UART3 Signals

PIN#	PIN Function	Type	Description	BALL
J2.77*	UART3_RXD	I/O	UART Receive Data Input DCE mode / Output DTE mode	SOC.D5
J2.87*	UART3_RXD	I/O	UART Receive Data Input DCE mode / Output DTE mode	SOC.A6
J2.83*	UART3_TXD	O/I	UART Transmit Data Output DCE mode / Input DTE mode	SOC.A4
J2.89*	UART3_TXD	O/I	UART Transmit Data Output DCE mode / Input DTE mode	SOC.B7
J2.79*	UART3_RTS_B	I/O	UART Ready To Send - Active Low Input DCE mode / Output DTE mode	SOC.D4
J2.81*	UART3_CTS_B	O/I	UART Clear To Send - Active Low Output DCE mode / Input DTE mode	SOC.B4

NOTE

"*" Denotes pins with alternative functions selected using the PINMUX

6.8.1.4. UART4 Signals

Table 39: UART4 Signals

PIN#	PIN Function	Type	Description	BALL
J2.24*~	UART4_RXD	I/O	UART Receive Data Input DCE mode / Output DTE mode	SOC.C5
J3.3*	UART4_RXD	I/O	UART Receive Data Input DCE mode / Output DTE mode	SOC.C6
J2.20*~	UART4_TXD	O/I	UART Transmit Data Output DCE mode / Input DTE mode	SOC.E5
J3.1*	UART4_TXD	O/I	UART Transmit Data Output DCE mode / Input DTE mode	SOC.D7
J2.26*~	UART4_RTS_B	I/O	UART Ready to Send - Active Low Input DCE mode / Output DTE mode	SOC.A5
J2.22*~	UART4_CTS_B	O/I	UART Clear to Send - Active Low Output DCE mode / Input DTE mode	SOC.B5

NOTE

"*" Denotes pins with alternative functions selected using the PINMUX

"~" Denotes pins used on SOM with ***"WBD" Configuration***, See section 6.4.2 for detailed information.

6.9. ECSPI - Enhanced Configurable SPI

DART-MX8M exposes all ECSPI1/ ECSPI2/ ECSPI3 pins.
ECSPI2 signals used on SOM for alternate function with ***"WBD" Configuration.*** In case other alternative function is required with the ***"WBD"*** order option, see section 6.4.1 .

The Enhanced Configurable Serial Peripheral Interface (ECSPI) is a full-duplex, synchronous, four-wire serial communication block with full-duplex enhanced Synchronous Serial Interface and data rate up to 52 Mbit/s.

Key features of the ECSPI include:

- Full-duplex synchronous serial interface
- Master/Slave configurable
- Four Chip Select (SS) signals to support multiple peripherals
- Transfer continuation function allows unlimited length data transfers
- 32-bit wide by 64-entry FIFO for both transmit and receive data
- Polarity and phase of the Chip Select (SS) and SPI Clock (SCLK) are configurable
- Direct Memory Access (DMA) support
- Max operation frequency up to the reference clock frequency

6.9.1.1. ECSPI1 Signals

Table 40: ECSPI1 Signals

PIN#	PIN Function	Type	Description	BALL
J2.77*	ECSPI1_SCLK	O	SPI Serial Clock	SOC.D5
J2.83*	ECSPI1_MOSI	I/O	SPI Master data Out - Slave data In signal	SOC.A4
J2.81*	ECSPI1_MISO	I/O	SPI Master data In - Slave data Out signal	SOC.B4
J2.79*	ECSPI1_SS0	O	SPI Slave Select Signal	SOC.D4

NOTE

"*" Denotes pins with alternative functions selected using the PINMUX

6.9.1.2. ECSPI2 Signals

Table 41: ECSPI2 Signals

PIN#	PIN Function	Type	Description	BALL
J2.24*~	ECSPI2_SCLK	O	SPI Serial Clock	SOC.C5
J2.20*~	ECSPI2_MOSI	I/O	SPI Master data Out - Slave data In signal	SOC.E5
J2.22*~	ECSPI2_MISO	I/O	SPI Master data In - Slave data Out signal	SOC.B5
J2.26*~	ECSPI2_SS0	O	SPI Slave Select Signal	SOC.A5

6.9.1.3. ECSPI3 Signals

Table 42: ECSPI3 Signals

PIN#	PIN Function	Type	Description	BALL
J2.88*	ECSPI3_SCLK	O	SPI Serial Clock	SOC.C7
J2.90*	ECSPI3_MOSI	I/O	SPI Master data Out - Slave data In signal	SOC.A7
J2.85*	ECSPI3_MISO	I/O	SPI Master data In - Slave data Out signal	SOC.B6
J2.86*	ECSPI3_SS0	O	SPI Slave Select Signal	SOC.D6

NOTE

"*" Denotes pins with alternative functions selected using the PINMUX

"~" Denotes pins used on SOM with ***"WBD" Configuration***, See section 6.4.2 for detailed information.

6.10. QSPI - Quad Serial Peripheral Interface

DART-MX8M exposes the **two** QSPI interfaces iMX 8M features with one slave select signal.

The Quad SPI module acts as an interface to external serial flash devices. It can function as one of the boot devices.

This module contains the following features:

- Flexible sequence engine to support various flash vendor devices
- Single pad/Dual pad/Quad pad mode of operation
- Support for flash data strobe signal for data sampling in DDR and SDR mode
- Parallel flash mode
- DMA support to read RX Buffer data via AMBA AHB bus (64-bit width interface) or IP registers space (32-bit access).
  Inner loop size of DMA access can be configured.
- Multi master accesses with priority
- Memory mapped read access to connected flash devices
- Multi master access with priority and flexible and configurable buffer for each master
- Two identical serial flash devices can be connected and accessed in parallel for data read operations, forming one (virtual) flash memory with doubled readout bandwidth
- Thirteen interrupt conditions (see Table 10-10)
- Programmable sequence engine to cater to future command/protocol changes and able to support all existing vendor commands and operations:
  - Supports 3-byte and 4-byte addressing
  - TXFIFO size is 512Byte
  - RXFIFO size is 512Byte
  - AHB BUF size is 1KByte

6.10.1. QSPI A Signals

Table 43: QSPI_A Signals

PIN#	PIN Function	Type	Description	BALL
J1.40*	QSPIA_SCLK	O	Flash A Serial Clock	SOC.G19
J1.38*	QSPIA_DQS	O	Flash A Data strobe signal	SOC.M20
J1.48*	QSPIA_DATA0	IO	Flash A Data I/O 0	SOC.G20
J1.32*	QSPIA_DATA1	IO	Flash A Data I/O 1	SOC.J20
J1.50*	QSPIA_DATA2	IO	Flash A Data I/O 2	SOC.H22
J1.46*	QSPIA_DATA3	IO	Flash A Data I/O 3	SOC.J21
J1.34*	QSPIA_SS0_B	O	Flash A Slave Select 0 signal (active low)	SOC.H19

NOTE

"*" Denotes pins with alternative functions selected using the PINMUX

6.10.2. QSPI B Signals

Table 44: QSPI_B Signals

PIN#	PIN Function	Type	Description	BALL
J1.45*	QSPIB_SCLK	O	Flash B Serial Clock	SOC.H21
J1.41*	QSPIB_DQS	O	Flash B Data strobe signal	SOC.K19
J1.39*	QSPIB_DATA0	IO	Flash B Data I/O 0	SOC.L20
J1.43*	QSPIB_DATA1	IO	Flash B Data I/O 1	SOC.J22
J1.37*	QSPIB_DATA2	IO	Flash B Data I/O 2	SOC.L19
J1.35*	QSPIB_DATA3	IO	Flash B Data I/O 3	SOC.M19
J1.47*	QSPIB_SS0_B	O	Flash B Slave Select 0 signal (active low)	SOC.F21

NOTE

"*" Denotes pins with alternative functions selected using the PINMUX

6.11. NAND

The DART-MX8M exposes the iMX 8M NAND interface, which is an alternate function for the QSPI interface pins see 6.10.

The NAND support is part of the iMX 8M GPMI – General Purpose Media Interface.

This module contains the following features:

- ONFI 1.0 compatible - Asynchronous mode
- ONFI 2.x compatible - Source synchronous mode
- ONFI3.2 compatible - DDR Mode, Samsung / Toshiba Toggle NAND protocol
- Flexible interface NAND Flash controller with 8-bit data width, up to 200 MB/s I/O speed and individual chip select
- Fully configurable address and command behavior, providing support for future devices not yet specified

- Individual chip select pins and ganged ready/busy pin for up to four NANDs (***only two available on the DART-MX8M connectors***)
- Individual state machine and DMA channel for each chip select
- Special command modes work with DMA controller to perform all normal NAND functions without CPU intervention
- Configurable timing based on a dedicated clock allows optimal balance of high NAND performance and low system power
- GPMI and DMA have been designed to handle complex multi-page operations without CPU intervention. The DMA uses a linked descriptor function with branching capability to automatically handle all of the operations needed to read/write multiple pages:
    - **Data/Register Read/Write**- GPMI can be programmed to read or write multiple cycles to the NAND address, command or data registers.
    - **Wait for NAND Ready**- GPMI's Wait-for-Ready mode can monitor the ready/busy signal of a single NAND flash and signal the DMA when the device has become ready. It also has a time-out counter and can indicate to the DMA that a time-out error has occurred. The DMAs can conditionally branch to a different descriptor in the case of an error.
    - **Check Status**-The Read-and-Compare mode allows the GPMI to check NAND status against a reference. If an error found, the GPMI can instruct the DMA to branch to an alternate descriptor, which attempts to fix the problem or asserts a CPU IRQ.
- The BCH module provides up to 62-bit ECC encryption/decryption for NAND Flash controller (GPMI)

6.11.1. NAND Interface Signals

Table 45: NAND Signals

PIN#	PIN Function	Type	Description	BALL
J1.38*	NAND_DQS	I/O	Data Strobe – direction determined by read and write signals	SOC.M20
J1.40*	NAND_ALE	O	Address Latch Enable	SOC.G19
J1.45*	NAND_CLE	O	Command Latch Enable	SOC.H21
J1.41*	NAND_RE_B	O	Read Enable	SOC.K19
J1.42*	NAND_WP_B	O	Write Protect , Requires external PU	SOC.K21
J1.44*	NAND_WE_B	O	Write Enable	SOC.K22
J1.36*	NAND_READY_B	I	Memory Ready/Busy_B signal OD output from NAND, Requires external PU	SOC.K20
J1.34*	NAND_CE0_B	O	Chip Enable 0	SOC.H19
J1.47*	NAND_CE2_B	O	Chip Enable 2	SOC.F21
J1.48*	NAND_DATA00	IO	Data IO 0	SOC.G20
J1.32*	NAND_DATA01	IO	Data IO 1	SOC.J20
J1.50*	NAND_DATA02	IO	Data IO 2	SOC.H22
J1.46*	NAND_DATA03	IO	Data IO 3	SOC.J21
J1.39*	NAND_DATA04	IO	Data IO 4	SOC.L20
J1.43*	NAND_DATA05	IO	Data IO 5	SOC.J22
J1.37*	NAND_DATA06	IO	Data IO 6	SOC.L19

PIN#	PIN Function	Type	Description	BALL
J1.35*	NAND_DATA07	IO	Data IO 7	SOC.M19

NOTE

"*" Denotes pins with alternative functions selected using the PINMUX

6.12. I²C

The DART-MX8M SOM exposes up to three I2C interfaces on the connectors: I2C2, I2C3 and I2C4.

NOTE

- I2C1 used internally in the SOM :
  - Function must not be altered in the PINMUX!
- I2C3 Exposed to the connectors:
  - Used internally in the SOM and can be used to interface external devices with addresses Different than 0x60!
  - I2C transactions to Address 0x60 must be avoided!
  - 10K Ohm PU resistors included on SOM.

The Inter-Integrated Circuit (I2C) provides functionality of a standard I2C master and slave. I2C is a two-wire, bidirectional serial bus that provides a simple, efficient method of data exchange, minimizing the interconnection between devices.
This bus is suitable for applications requiring occasional communications over a short distance between many devices. The flexible I2C standard allows additional devices to be connected to the bus for expansion and system development.

The I2C has the following key features:

- Compatible with the I2C Bus Specification, version 2.1, by Philips Semiconductor (now NXP Semiconductors).
- Multi-master operation.
- After a reset, the I2C defaults to Slave Receive operations.
- Software programmability for one of 64 different serial clock frequencies:
  - Standard mode, I2C supports the data transfer rates up to 100 Kbits/s
  - In Fast mode, data transfer rates up to 400 Kbits/s can be achieved
- Software-selectable acknowledge bit
- Interrupt-driven, byte-by-byte data transfer
- Arbitration-lost interrupt with automatic mode switching from master to slave
- Calling address identification interrupt
- Start and stop signal generation/detection
- Repeated start signal generation
- Acknowledge bit generation/detection
- Bus-busy detection

6.12.1. I2C2 Signals

Table 46: I2C2 Signals

PIN#	PIN Function	Type	Description	BALL
J2.32*	I2C2_SCL	IO	I2C clock, Open Drain, Requires external PU	SOC.G7
J2.30*	I2C2_SDA	IO	I2C data, Open Drain, Requires external PU	SOC.F7

NOTE

"*" Denotes pins with alternative functions selected using the PINMUX

6.12.2. I2C3 Signals

Table 47: I2C3 Signals

PIN#	PIN Function	Type	Description	BALL
J3.46*	I2C3_SCL	IO	**Note: Used internally in SOM - Do not alter its function!** I2C clock, Open Drain, 10K internal SOM PU included.	SOC.G8
J3.42*	I2C3_SDA	IO	**Note: Used internally in SOM - Do not alter its function!** I2C data, Open Drain, 10K internal SOM PU included.	SOC.E9

NOTE

"*" Denotes pins with alternative functions selected using the PINMUX

6.12.3. I2C4 Signals

Table 48: I2C4 Signals

PIN#	PIN Function	Type	Description	BALL
J2.17*	I2C4_SCL	IO	I2C clock, Open Drain, Requires external PU	SOC.F8
J2.19*	I2C4_SDA	IO	I2C data, Open Drain, Requires external PU	SOC.F9

NOTE

"*" Denotes pins with alternative functions selected using the PINMUX

6.13. PWM - Pulse Width Modulation

The DART-MX8M exposes all 4 of the PWM outputs.

The following features characterize the PWM:

- 16-bit up-counter with clock source selection
- Can be programmed to select one of three clock signals as its source frequency, with a maximum of 66MHz
- 4 x 16 FIFO to minimize interrupt overhead
- 12-bit prescaler for division of clock
- Sound and melody generation
- Active high or active low configured output
- Can be programmed to be active in low-power mode
- Can be programmed to be active in debug mode
- Interrupts at compare and rollover

6.13.1. PWM Signals

Table 49: PWM Signals

PIN#	PIN Function	Type	Description	BALL
J1.19*	PWM1_OUT	O	Pulse Width Modulation 1	SOC.F9
J3.32*	PWM1_OUT	O	Pulse Width Modulation 1	SOC.E6
J3.64*	PWM1_OUT	O	Pulse Width Modulation 1	SOC.T7
J1.17*	PWM2_OUT	O	Pulse Width Modulation 2	SOC.F8
J3.28*	PWM2_OUT	O	Pulse Width Modulation 2	SOC.G6
J3.40*	PWM2_OUT	O	Pulse Width Modulation 2	SOC.K6
J3.36*	PWM3_OUT	O	Pulse Width Modulation 3	SOC.F6
J3.42*	PWM3_OUT		**NOTE: Pin function cannot be used other than I2C3_SDA function !**	SOC.E9
J2.16*~	PWM4_OUT	O	Pulse Width Modulation 4	SOC.D3
J3.38*	PWM4_OUT	O	Pulse Width Modulation 4	SOC.J6
J3.46*	PWM4_OUT		**NOTE: Pin function cannot be used other than I2C3_SCL function !**	SOC.G8

NOTE

"*" Denotes pins with alternative functions selected using the PINMUX

6.14. GPT – General Purpose Timer

The DART-MX8M exposes the GPT interface on its connectors.

Each GPT is a 32-bit "free-running" or "set-and-forget" mode timer with programmable pre-scaler and compare and capture register. A timer counter value can be captured using an external event and can be configured to trigger a capture event on either the leading or trailing edges of an input pulse (GPT_CAPTURE). When the timer is configured to operate in "set-and-forget" mode, it is capable of providing precise interrupts at regular intervals with minimal processor intervention. The counter has output compare logic to provide the status and interrupt at comparison. External pins (GPT_COMPARE) can output the comparison. This timer can be configured to run either on an external clock (GPT_CLK) or on an internal clock.

GPT Features include:

- One 32-bit up-counter with clock source selection, including external clock
- Two input capture channels with a programmable trigger edge
- Three outputs compare channels with a programmable output mode. A "forced compare" feature is also available
- Can be programmed to be active in low power and debug modes
- Interrupt generation at capture, compare, and rollover events
- Restart or free-run modes for counter operations

6.14.1. GPT Signals

Table 50: GPT Signals

PIN#	PIN Function	Type	Description	BALL
J2.10*~	GPT1_CLK	I	GPT1 Clock Source	SOC.G3
J2.6*~	GPT1_CAPTURE1	I	GPT1 Capture event 1	SOC.G4
J2.8*~	GPT1_CAPTURE2	I	GPT1 Capture event 2	SOC.F4
J2.14*~	GPT1_COMPARE1	O	GPT1 Compare event 1	SOC.F3
J2.4*~	GPT1_COMPARE2	O	GPT1 Compare event 2	SOC.C4
J2.2*~	GPT1_COMPARE3	O	GPT1 Compare event 3	SOC.C3
J3.46*	GPT2_CLK		**NOTE: Pin function cannot be used other than I2C3_SCL function!**	SOC.G8
J3.42*	GPT3_CLK		**NOTE: Pin function cannot be used other than I2C3_SDA function!**	SOC.E9

NOTE

"*" Denotes pins with alternative functions selected using the PINMUX

"~" Denotes pins used on SOM with ***"AC" Configuration***, See section 6.7.1 .

6.15. Reference Clocks

Two pairs of differential clock inputs, named CLK1 and CLK2, can be used as the reference clock for the PLL. This is mainly used for a high-speed clock input during testing.

Up to four clock outputs from the CCM available from normal GPIO pads via IOMUX can be used to clock external devices.

6.15.1. Clock Signals

Table 51: Clock Signals

PIN#	PIN Function	Type	Description	BALL
J1.23	CLK2_N	DSI	**Note: 100 Ohm Differential termination included on SOM** Alternative Clock source 2 NEG	SOC.U22
J1.25	CLK2_P	DSI	**Note: 100 Ohm Differential termination included on SOM** Alternative Clock source 2 POS	SOC.T22
J1.29	CLK1_N	DSI	**Note: 100 Ohm Differential termination included on SOM** Alternative Clock source 1 NEG	SOC.T23
J1.31	CLK1_P	DSI	**Note: 100 Ohm Differential termination included on SOM** Alternative Clock source 1 POS	SOC.R23
J1.1*	REF_CLK_32K	O	**Note: Used internally in SOM with *"WBD" Configuration see 0*** Can be shared for external devices requiring this clock, with high impedance inputs.	SOC.T6
J3.38*	CLKO2	O	SOC CCM Clock OUT 2	SOC.J6
J3.58*	EXT_CLK3	O	SOC CCM External Clock 3	SOC.N5
J3.64*	EXT_CLK2	O	SOC CCM External Clock 2	SOC.T7
J3.64*	REF_CLK_24M	O	SOC ANAMIX 24Mhz reference clock	SOC.T7

NOTE

"*" Denotes pins with alternative functions selected using the PINMUX

6.16. GPIO - General Purpose Input Output

The GPIO general-purpose input/output peripheral provides dedicated general-purpose pins that can be configured as either inputs or outputs.

- **When configured as an output:**
  It is possible to write to an internal register to control the state driven on the output pin
- **When configured as an input:**
  It is possible to detect the state of the input by reading the state of an internal register
- GPIO peripheral can produce CORE interrupts
- Input/output multiplexing controller (IOMUXC) to provide centralized pad control
- Up to 119 GPIO are available on the DART-MX8M

6.16.1. GPIO Signals

The DART-MX8M exposes up to 119 GPIO lines.

Table 52: GPIO Signals

PIN#	PIN Function	Type	Description	BALL
J1.1*	GPIO1_IO00	IO	**Note: Available without *"WBD" Configuration*** GPIO Bank 1 Bit 0	SOC.T6
J3.64*	GPIO1_IO01	IO	GPIO Bank 1 Bit 1	SOC.T7
J2.28	GPIO1_IO02	IO	GPIO Bank 1 Bit 2	SOC.R4
J3.54*	GPIO1_IO03	IO	GPIO Bank 1 Bit 3	SOC.P4
J3.62*	GPIO1_IO05	IO	GPIO Bank 1 Bit 5	SOC.P7
J3.58*	GPIO1_IO06	IO	GPIO Bank 1 Bit 6	SOC.N5
J3.60*	GPIO1_IO08	IO	GPIO Bank 1 Bit 8	SOC.N7
J3.52*	GPIO1_IO10	IO	GPIO Bank 1 Bit 10	SOC.M7
J3.30*	GPIO1_IO11	IO	GPIO Bank 1 Bit 11	SOC.L6
J3.50*	GPIO1_IO12	IO	GPIO Bank 1 Bit 12	SOC.L7
J3.40*	GPIO1_IO13	IO	GPIO Bank 1 Bit 13	SOC.K6
J3.48*	GPIO1_IO14	IO	GPIO Bank 1 Bit 14	SOC.K7
J3.38*	GPIO1_IO15	IO	GPIO Bank 1 Bit 15	SOC.J6
J1.13*	GPIO1_IO16	IO	**Note: Available without *"EC" Configuration*** GPIO Bank 1 Bit 16	SOC.N20
J1.11*	GPIO1_IO17	IO	**Note: Available without *"EC" Configuration*** GPIO Bank 1 Bit 17	SOC.N19
J1.8*~	GPIO1_IO18	IO	**Note: Available without *"EC" Configuration*** GPIO Bank 1 Bit 18	SOC.P20
J1.6*~	GPIO1_IO19	IO	**Note: Available without *"EC" Configuration*** GPIO Bank 1 Bit 19	SOC.R19
J1.2*~	GPIO1_IO20	IO	**Note: Available without *"EC" Configuration*** GPIO Bank 1 Bit 20	SOC.R21
J1.4*~	GPIO1_IO21	IO	**Note: Available without *"EC" Configuration*** GPIO Bank 1 Bit 21	SOC.R20
J1.3*~	GPIO1_IO22	IO	**Note: Available without *"EC" Configuration*** GPIO Bank 1 Bit 22	SOC.P19

PIN#	PIN Function	Type	Description	BALL
J1.5*~	GPIO1_IO23	IO	**Note: Available without *"EC" Configuration*** GPIO Bank 1 Bit 23	SOC.T19
J1.9*~	GPIO1_IO24	IO	**Note: Available without *"EC" Configuration*** GPIO Bank 1 Bit 24	SOC.T21
J1.7*~	GPIO1_IO25	IO	**Note: Available without *"EC" Configuration*** GPIO Bank 1 Bit 25	SOC.T20
J1.10*~	GPIO1_IO26	IO	**Note: Available without *"EC" Configuration*** GPIO Bank 1 Bit 26	SOC.U19
J1.12*~	GPIO1_IO27	IO	**Note: Available without *"EC" Configuration*** GPIO Bank 1 Bit 27	SOC.U21
J1.14*~	GPIO1_IO28	IO	**Note: Available without *"EC" Configuration*** GPIO Bank 1 Bit 28	SOC.U20
J1.16*~	GPIO1_IO29	IO	**Note: Available without *"EC" Configuration*** GPIO Bank 1 Bit 29	SOC.V19
J1.74*~	GPIO2_IO12	IO	**Note: Available without *"WBD" Configuration*** GPIO Bank 2 Bit 12	SOC.L21
J1.82*~	GPIO2_IO13	IO	**Note: Available without *"WBD" Configuration*** GPIO Bank 2 Bit 13	SOC.L22
J1.88*~	GPIO2_IO14	IO	**Note: Available without *"WBD" Configuration*** GPIO Bank 2 Bit 14	SOC.M22
J1.86*~	GPIO2_IO15	IO	**Note: Available without *"WBD" Configuration*** GPIO Bank 2 Bit 15	SOC.N22
J1.80*~	GPIO2_IO16	IO	**Note: Available without *"WBD" Configuration*** GPIO Bank 2 Bit 16	SOC.N21
J1.78*~	GPIO2_IO17	IO	**Note: Available without *"WBD" Configuration*** GPIO Bank 2 Bit 17	SOC.P22
J1.84*~	GPIO2_IO18	IO	**Note: Available without *"WBD" Configuration*** GPIO Bank 2 Bit 18	SOC.P21
J1.28*	GPIO2_IO19	IO	GPIO Bank 2 Bit 19	SOC.R22
J1.40*	GPIO3_IO00	IO	GPIO Bank 3 Bit 0	SOC.G19
J1.34*	GPIO3_IO01	IO	GPIO Bank 3 Bit 1	SOC.H19
J1.47*	GPIO3_IO03	IO	GPIO Bank 3 Bit 3	SOC.F21
J1.45*	GPIO3_IO05	IO	GPIO Bank 3 Bit 5	SOC.H21
J1.48*	GPIO3_IO06	IO	GPIO Bank 3 Bit 6	SOC.G20
J1.32*	GPIO3_IO07	IO	GPIO Bank 3 Bit 7	SOC.J20
J1.50*	GPIO3_IO08	IO	GPIO Bank 3 Bit 8	SOC.H22
J1.46*	GPIO3_IO09	IO	GPIO Bank 3 Bit 9	SOC.J21
J1.39*	GPIO3_IO10	IO	GPIO Bank 3 Bit 10	SOC.L20
J1.43*	GPIO3_IO11	IO	GPIO Bank 3 Bit 11	SOC.J22
J1.37*	GPIO3_IO12	IO	GPIO Bank 3 Bit 12	SOC.L19
J1.35*	GPIO3_IO13	IO	GPIO Bank 3 Bit 13	SOC.M19
J1.38*	GPIO3_IO14	IO	GPIO Bank 3 Bit 14	SOC.M20
J1.41*	GPIO3_IO15	IO	GPIO Bank 3 Bit 15	SOC.K19
J1.36*	GPIO3_IO16	IO	GPIO Bank 3 Bit 16	SOC.K20
J1.44*	GPIO3_IO17	IO	GPIO Bank 3 Bit 17	SOC.K22
J1.42*	GPIO3_IO18	IO	GPIO Bank 3 Bit 18	SOC.K21
J2.34*	GPIO3_IO19	IO	GPIO Bank 3 Bit 19	SOC.N4
J2.40*	GPIO3_IO20	IO	GPIO Bank 3 Bit 20	SOC.L5
J2.36*	GPIO3_IO21	IO	GPIO Bank 3 Bit 21	SOC.M5

PIN#	PIN Function	Type	Description	BALL
J2.42*	GPIO3_IO22	IO	GPIO Bank 3 Bit 22	SOC.L4
J2.38*	GPIO3_IO23	IO	GPIO Bank 3 Bit 23	SOC.M4
J2.44*	GPIO3_IO24	IO	GPIO Bank 3 Bit 24	SOC.K5
J2.46*	GPIO3_IO25	IO	GPIO Bank 3 Bit 25	SOC.K4
J2.55*	GPIO4_IO00	IO	GPIO Bank 4 Bit 0	SOC.L1
J2.57*	GPIO4_IO01	IO	GPIO Bank 4 Bit 1	SOC.K1
J2.61*^	GPIO4_IO02	IO	GPIO Bank 4 Bit 2	SOC.K2
J2.59*^	GPIO4_IO03	IO	GPIO Bank 4 Bit 3	SOC.L2
J2.63*^	GPIO4_IO04	IO	GPIO Bank 4 Bit 4	SOC.H2
J2.62*^	GPIO4_IO05	IO	GPIO Bank 4 Bit 5	SOC.J2
J2.65*^	GPIO4_IO06	IO	GPIO Bank 4 Bit 6	SOC.J1
J2.69*^	GPIO4_IO07	IO	GPIO Bank 4 Bit 7	SOC.F1
J2.66*^	GPIO4_IO08	IO	GPIO Bank 4 Bit 8	SOC.G2
J2.68*^	GPIO4_IO09	IO	GPIO Bank 4 Bit 9	SOC.G1
J2.64*	GPIO4_IO10	IO	GPIO Bank 4 Bit 10	SOC.H1
J2.72*	GPIO4_IO11	IO	GPIO Bank 4 Bit 11	SOC.E1
J2.70*^	GPIO4_IO12	IO	GPIO Bank 4 Bit 12	SOC.F2
J2.67*^	GPIO4_IO13	IO	GPIO Bank 4 Bit 13	SOC.E2
J2.78*^	GPIO4_IO14	IO	GPIO Bank 4 Bit 14	SOC.B2
J2.73*^	GPIO4_IO15	IO	GPIO Bank 4 Bit 15	SOC.D1
J2.74*^	GPIO4_IO16	IO	GPIO Bank 4 Bit 16	SOC.D2
J2.71*^	GPIO4_IO17	IO	GPIO Bank 4 Bit 17	SOC.C2
J2.80*^	GPIO4_IO18	IO	GPIO Bank 4 Bit 18	SOC.B3
J2.76*^	GPIO4_IO19	IO	GPIO Bank 4 Bit 19	SOC.C1
J2.82*	GPIO4_IO20	IO	GPIO Bank 4 Bit 20	SOC.A3
J2.48*	GPIO4_IO21	IO	GPIO Bank 4 Bit 21	SOC.J4
J2.50*	GPIO4_IO22	IO	GPIO Bank 4 Bit 22	SOC.H3
J2.58*	GPIO4_IO23	IO	GPIO Bank 4 Bit 23	SOC.H6
J2.52*	GPIO4_IO24	IO	GPIO Bank 4 Bit 24	SOC.H4
J2.56*	GPIO4_IO25	IO	GPIO Bank 4 Bit 25	SOC.J5
J2.60*	GPIO4_IO26	IO	GPIO Bank 4 Bit 26	SOC.G5
J2.54*	GPIO4_IO27	IO	GPIO Bank 4 Bit 27	SOC.H5
J2.6*~	GPIO4_IO28	IO	**Note: Available without "*AC" Configuration*** GPIO Bank 5 Bit 28	SOC.G4
J2.8*~	GPIO4_IO29	IO	**Note: Available without "*AC" Configuration*** GPIO Bank 5 Bit 29	SOC.F4
J2.14*~	GPIO4_IO30	IO	**Note: Available without "*AC" Configuration*** GPIO Bank 5 Bit 30	SOC.F3
J2.10*~	GPIO4_IO31	IO	**Note: Available without "*AC" Configuration*** GPIO Bank 5 Bit 31	SOC.G3
J2.4*~	GPIO5_IO00	IO	**Note: Available without "*AC" Configuration*** GPIO Bank 5 Bit 0	SOC.C4
J2.2*~	GPIO5_IO01	IO	**Note: Available without "*AC" Configuration*** GPIO Bank 5 Bit 1	SOC.C3
J2.16*~	GPIO5_IO02	IO	**Note: Available without "*AC" Configuration*** GPIO Bank 5 Bit 7	SOC.D3

PIN#	PIN Function	Type	Description	BALL
J3.36*	GPIO5_IO03	IO	GPIO Bank 5 Bit 3	SOC.F6
J3.28*	GPIO5_IO04	IO	GPIO Bank 5 Bit 4	SOC.G6
J3.32*	GPIO5_IO05	IO	GPIO Bank 5 Bit 5	SOC.E6
J2.77*	GPIO5_IO06	IO	GPIO Bank 5 Bit 6	SOC.D5
J2.83*	GPIO5_IO07	IO	GPIO Bank 5 Bit 5	SOC.A4
J2.81*	GPIO5_IO08	IO	GPIO Bank 5 Bit 8	SOC.B4
J2.79*	GPIO5_IO09	IO	GPIO Bank 5 Bit 9	SOC.D4
J2.24*~	GPIO5_IO10	IO	**Note: used on SOM with *"WBD" Configuration*, See section 6.4.1.1 for detailed information on alternate function use** GPIO Bank 5 Bit 10	SOC.C5
J2.20*~	GPIO5_IO11	IO	**Note: used on SOM with *"WBD" Configuration*, See section 6.4.1.1 for detailed information on alternate function use** GPIO Bank 5 Bit 11	SOC.E5
J2.22*~	GPIO5_IO12	IO	**Note: used on SOM with *"WBD" Configuration*, See section 6.4.1.1 for detailed information on alternate function use** GPIO Bank 5 Bit 12	SOC.B5
J2.26*~	GPIO5_IO13	IO	**Note: used on SOM with *"WBD" Configuration*, See section 6.4.1.1 for detailed information on alternate function use** GPIO Bank 5 Bit 13	SOC.A5
J2.32*	GPIO5_IO16	IO	GPIO Bank 5 Bit 16	SOC.G7
J2.30*	GPIO5_IO17	IO	GPIO Bank 5 Bit 17	SOC.F7
J3.46*	GPIO5_IO18	IO	**NOTE: Pin function cannot be used other than I2C3_SCL function!**	SOC.G8
J3.42*	GPIO5_IO19	IO	**NOTE: Pin function cannot be used other than I2C3_SDA function!**	SOC.E9
J1.17*	GPIO5_IO20	IO	GPIO Bank 5 Bit 20	SOC.F8
J1.19*	GPIO5_IO21	IO	GPIO Bank 5 Bit 21	SOC.F9
J2.88*	GPIO5_IO22	IO	GPIO Bank 5 Bit 22	SOC.C7
J2.90*	GPIO5_IO23	IO	GPIO Bank 5 Bit 23	SOC.A7
J2.85*	GPIO5_IO24	IO	GPIO Bank 5 Bit 24	SOC.B6
J2.86*	GPIO5_IO25	IO	GPIO Bank 5 Bit 25	SOC.D6
J2.87*	GPIO5_IO26	IO	GPIO Bank 5 Bit 26	SOC.A6
J2.89*	GPIO5_IO27	IO	GPIO Bank 5 Bit 27	SOC.B7
J3.3*	GPIO5_IO28	IO	GPIO Bank 5 Bit 28	SOC.C6
J3.1*	GPIO5_IO29	IO	GPIO Bank 5 Bit 29	SOC.D7

NOTE

"*" Denotes pins with alternative functions selected using the PINMUX

"^" Denotes pins which are **latched after reset for BOOT CONFIGURATION**, See section 6.18.1 for detailed information.

6.17. JTAG

The System JTAG Controller (SJC) provides debug and test control with maximum security. The test access port (TAP) is designed to support features compatible with the IEEE standard 1149.1 v2001 (JTAG). Support IEEE P1149.6 extensions to the JTAG standard are for AC testing of selected IO signals.

The JTAG port allows debug-related control and status, such as putting selected cores into reset and/or debug mode and the ability to monitor individual core status signals via JTAG. JTAG port interfaces the M4 and Cortex A53 Cores DAP - debug access port. Depending on the JTAG MOD pin:

Table 53: System JTAG Controller (SJC) Modes

MOD	Name	Description
0	Daisy chain ALL	For common SW debug (High speed and production)
1	SJC only	IEEE 1149.1 JTAG compliant mode

6.17.1. JTAG signals

Table 54: JTAG Signals

PIN#	PIN Function	Type	Description	BALL
J2.1	JTAG_TCK	I	JTAG Clock ; **Requires external 10K pull down**	SOC.T5
J2.3	JTAG_TMS	I	JTAG Test Mode Select	SOC.V5
J2.5	JTAG_TRST_B	I	JTAG Reset; Active Low	SOC.U6
J2.7	JTAG_TDI	I	JTAG Data In	SOC.W5
J2.9	JTAG_TDO	O	JTAG Data Out	SOC.U5

6.18. General System Control

6.18.1. Boot configuration

The DART-MX8M can be programmed to boot from the following sources:

- On board eMMC Flash memory (if available)
- External SD Card
- External NAND Flash memory (**Note: Currently not supported by BSP**)

The selection of the boot mode is done via strap options resistors on BOOT_CFG lines, which are latched on POR_B signal rise (values should remain valid 1ms after rise).

ATTENTION

External drivers connected to BOOT_CFG lines, **marked** by **"^"** in the interfaces, should be disabled on during reset (POR_B) on pins used as inputs to the SOM, otherwise they may change the boot option and the SOM will not boot.

6.18.2. Boot Configuration Signals

Table 55: Boot Signals

PIN#	PIN Function	Type	Description	BALL
J2.13	BOOT_MODE0	I	Boot mode bit 0; For normal boot apply 1K PD	SOC.W6
J2.11	BOOT_MODE1	I	Boot mode bit 1; For normal boot apply 1K PU to NVCC_3V3	SOC.V6
J2.61*^	BOOT_CFG00	I	Boot Configuration Bit 0; Apply **Low** signal during POR_B and 1ms after negate	SOC.K2
J2.59*^	BOOT_CFG01	I	Boot Configuration Bit 1 Apply **High** signal during POR_B and 1ms after negate	SOC.L2
J2.63*^	BOOT_CFG02	I	Boot Configuration Bit 2 Apply **Low** signal during POR_B and 1ms after negate	SOC.H2
J2.62*^	BOOT_CFG03	I	Boot Configuration Bit 3 Apply **Low** signal during POR_B and 1ms after negate	SOC.J2
J2.65*^	BOOT_CFG04	I	Boot Configuration Bit 4 Apply **Low** signal during POR_B and 1ms after negate	SOC.J1
J2.69*^	BOOT_CFG05	I	Boot Configuration Bit 5 Apply **Low** signal during POR_B and 1ms after negate	SOC.F1
J2.66*^	BOOT_CFG06	I	Boot Configuration Bit 6 Apply **Low** signal during POR_B and 1ms after negate	SOC.G2
J2.68*^	BOOT_CFG07	I	Boot Configuration Bit 7 Apply **Low** signal during POR_B and 1ms after negate	SOC.G1
J2.70*^	BOOT_CFG08	I	Boot Configuration Bit 8 Apply **Low** signal during POR_B and 1ms after negate	SOC.F2
J2.67*^	BOOT_CFG09	I	Boot Configuration Bit 9 Apply **Low** signal during POR_B and 1ms after negate	SOC.E2
J2.78*^	BOOT_CFG10	I	Boot Configuration Bit 10 Follow Table 56: Boot Options	SOC.B2
J2.73*^	BOOT_CFG11	I	Boot Configuration Bit 11 Apply **Low** signal during POR_B and 1ms after negate	SOC.D1

PIN#	PIN Function	Type	Description	BALL
J2.74*^	BOOT_CFG12	I	Boot Configuration Bit 12 Follow Table 56: Boot Options	SOC.D2
J2.71*^	BOOT_CFG13	I	Boot Configuration Bit 13 Follow Table 56: Boot Options	SOC.C2
J2.80*^	BOOT_CFG14	I	Boot Configuration Bit 14 Apply **Low** signal during POR_B and 1ms after negate	SOC.B3
J2.76*^	BOOT_CFG15	I	Boot Configuration Bit 15 Apply **Low** signal during POR_B and 1ms after negate	SOC.C1

NOTE

"*" Denotes pins with alternative functions selected using the PINMUX

Table 56 details the boot options for the DART-MX8M.

Table 56: Boot Options

	Ext SD	eMMC
BOOT_CFG10	Low	High
BOOT_CFG12	High	Low
BOOT_CFG13	Low	High

NOTE

Low – Represents pull down or floating.
High – Represents pull up of 4.7KΩ to 1KΩ.

6.18.3. General System Control Signals

The user must ensure not to drive any pins/function from the SOM before the appropriate IO power is up.

NVCC_3V3 SOM output is used to power most of the SOM pins and could be used to power the custom board. Refer to DART-MX8M CustomBoard schematics for implementation suggestion.

Table 57 details the SOM system control signals.

Table 57: System Control Signals

PIN#	PIN Function	Type	Description	BALL
J1.20	ONOFF	I	In **OFF mode, a brief connection to GND** causes the internal power management state machine to **change state to ON**. In **ON mode, a brief connection to GND** generates an interrupt (intended to initiate a software-controllable **power-down**). **An approximate 5 second or more connection to GND causes a forced OFF.** **When not used leave Floating**	SOC.W21

PIN#	PIN Function	Type	Description	BALL
J1.22	PMIC_ON_REQ	IO	**Note: Internal PU on SOM to NVCC_SNVS_3V3** OD output from SOC which controls the SOM power up/ down sequence; **Pulling the signal to GND** will force the **SOM power OFF**. External delay on this pin is recommended, see reference CustomBoard schematics. *Can be used to control the custom board power OFF state.* *Turn ON should use the NVCC_3V3 output to control CustomBoard power.*	SOC.V20
J1.26	PMIC_STBY_REQ	O	**Note: Internal PU on SOM to NVCC_SNVS_3V3** **Signal output from SOC controlling it's PMIC;** **0 to 1: Enter Standby** **1 to 0: Wake up from standby** *Can be used to control the custom board power.*	SOC.V21
J1.24	POR_B	IO	**Note: OD output from PMIC; Include 4.7K PU to NVCC_SNVS_3V3 on SOM** Signal is **asserted LOW** from assertion of PMIC_ON_REQ (if a valid VBAT exist) **Negates HIGH** at the end of power up sequence. Could be used to control buffers driving the configuration pins.	SOC.W20
J2.28*	WDOG_B [1]	O	Alternate pin function could be used to initiate power up sequence in case of a watch dog event.	SOC.R4

[1] Once the **WDOG** is activated, it must be serviced by the software on a periodic basis. If servicing does not take place, the timer times out. Upon timeout, the WDOG asserts the internal system reset signal, WDOG_RESET_B to the System Reset Controller(SRC). There is also a provision for WDOG signal assertion by timeout counter expiration. There is an option of programmable interrupt generation before the counter actually times out. The time at which the interrupt needs to be generated prior to counter timeout is programmable. There is a power down counter which is enabled out of any reset (POR, Warm/Cold). This counter has a fixed timeout period of 16 seconds, upon which it asserts the WDOG signal.

6.19. Power

6.19.1. Power

Table 58: Power Pins

PIN#	PIN Function	Type	Description	Note
J3. 71,73,75, 77,79,81, 83,85,87, 89	VBAT	PI	DART-MX8M Single Supply voltage input	
J3.69	LICELL[1]	PI	3.0V RTC back-up battery supply input	Max 4mA required.
J1.15	NVCC_SNVS_3V3[2]	PO	RTC Domain 3.0V power rail output	
J1.27	NVCC_3V3	PO	SOM Peripherals 3.3V Output	Max 100mA draw is allowed.
J1.90	NVCC_SD2_1V8_3V3	PO	SOM IO power for the SD2 interface. Use only for SD2 interface PU resistors on CD and CMD signals. See section 0.	
J1.41	VDD_PHY_1V8	PO	SOM core power for the HDMI interface See section 6.1.1.1 - HDMI termination	
J1.26	USB2_VBUS	PI	USB2 PHY VBUS	BALL SOC.D9
J2.66	USB1_VBUS	PI	USB1 PHY VBUS	BALL SOC.D14

6.19.2. Ground

Table 59: Ground Pins

PIN#	PIN Function	Type	Description
J1. 18,21,30 ,33,49,52 ,55,58,61 ,64,67,70 ,76,85	GND		J1 Digital Ground
J2. 18,23,47, 53,75,84	GND		J2 Digital Ground
J3. 9,15,21, 21,24,27, 33,34,39, 45,51,57, 63,68,74	GND		J3 Digital Ground
J2.12	AGND		Audio GND

[1] Variscite recommends using an external low power time keeping circuitry which is power efficient than the SOC RTC core; See CustomBoard for reference design supported by the BSP.
[2] NVCC_SNVS_3V3 power used for required PU resistors on signals controlling the power management of the SOC.

7. Electrical specifications

7.1. Absolute maximum ratings

Table 60: Absolute Maximum Ratings

Parameter	Min	Max	Unit
VBAT	-0.3	4.8	V
LICELL	-0.3	3.6	V
USB_VBUS	-0.3	5.25	V

7.2. Operating conditions

Table 61: Operating Ranges

Parameter	Min.	Typ.	Max.	Unit
VBAT	3.4	3.7	4.5	V
LICELL	1.8	3	3.3	V
USB_VBUS	4.75	5	5.25	V

7.3. Power consumption

Table 62: DART-MX8M Power Consumption

Mode	Voltage	Current	Power	Conditions
Run	3.7V	TBD	TBD	Linux up, Wi-Fi connected and Iperf is running 802.11 ac 5GHz
Run	3.7V	TBD	TBD	Linux up, Wi-Fi connected and Iperf is running 802.11 n 2.4GHz
Run	3.7V	TBD	TBD	Linux up
Standby	3.7V	TBD	TBD	Memory retention mode
Off (RTC)	3.7V	TBD	TBD	All power rails are Off, only Internal SOC RTC is powered

7.4. Peripheral Voltage Levels

All the peripheral interface lines used as inputs or output to the DART-MX8M use 3.3V LVCMOS levels, with the following interfaces: HDMI / PCIe / USB / DSI / CSI . The latter follow a different standard since they are high-speed signals.

SD2 (SDIO lines) interface IOs will change voltage between 3.3V and 1.8V depending on the SD card capabilities.

8. Environmental Specifications

Table 63: Environmental Specifications

Parameter	Min	Max
Commercial Operating Temperature Range	0°C	70°C
Extended Operating Temperature Range	-20°C	85°C
Industrial Operating Temperature Range	-40°C	85°C
Referring MIL-HDBK-217F-2 Parts Count Reliability Prediction Method Model:		
50°C, Class B-1, GM	121K hrs.	
50°C, Class B-1, GB	1400K hrs.	

NOTE

Extended and industrial temperature ranges based only on the operating temperature grade of the SOM components. Customer should consider specific thermal design for the final product based upon the specific environmental and operational conditions.

9. Mechanical Drawings

9.1. Carrier Board Mounting

The SOM has four mounting holes for mounting it to the carrier board which are plated holes and connected to GND.

NOTE

The size and footprint of SOM 90-pin connectors Hirose P/N: DF40C-90DP-0.4V(51) are different from mating carrier board 90-pin connectors (see section 5.1).

To ensure correct positioning of the carrier board connectors and holes please refer to VAR-DT8MCustomBoard DXF available here (under documentation tab): http://www.variscite.com/products/single-board-computers/var-dt8mcustomboard

It is recommended NOT place any components under the SOM.

9.2. Standoffs

Customers requiring a mechanical solution for mounting in harsh vibration environments can use the following standoff:

Manufacturer: **MAC8**

PN: **TH-1.6-1.5-M2**

Link: http://www.mac8japan.com/English%20Catalog/TH1.6%20Series-2.pdf

9.3. Thermal Management

In order to handle intensive applications where thermal management is required, Variscite offers a heat spreader:

Variscite PN: **TBD**

The heat spreader will allow the best solution to attach various heat sources on board to an additional passive or active solution will be required depending on the application.

9.4. SOM Dimensions

Figure 7 illustrates the top view of the DART-MX8M size and mounting holes relative location. **All dimensions given in [mm] units**.

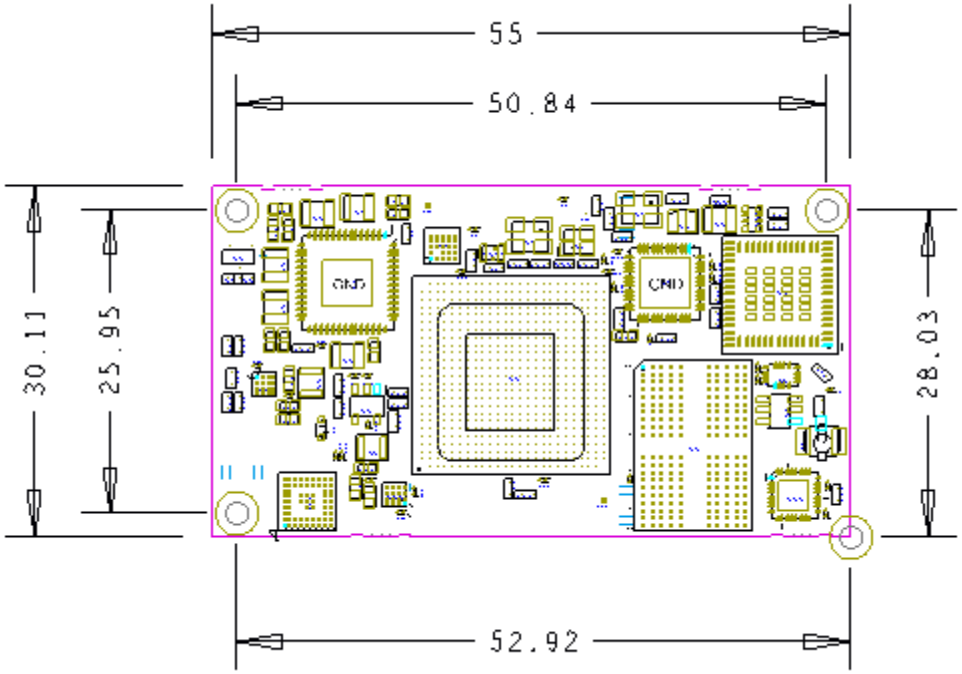

Figure 7: DART-MX8M Top View Mechanics

Dimensioning:

Width: 55 mm

Length: 30.11 mm

Height: 4.73 mm (Carrier PCB to highest component on SOM)

9.4.1. CAD Files

CAD files are available for download at http://www.variscite.com/

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