

# 1. Description

# 1.1. Project

Project Name	Nucleo-H7A3ZIQ_Test_01
Board Name	NUCLEO-H7A3ZI-Q
Generated with:	STM32CubeMX 6.8.1
Date	08/05/2024

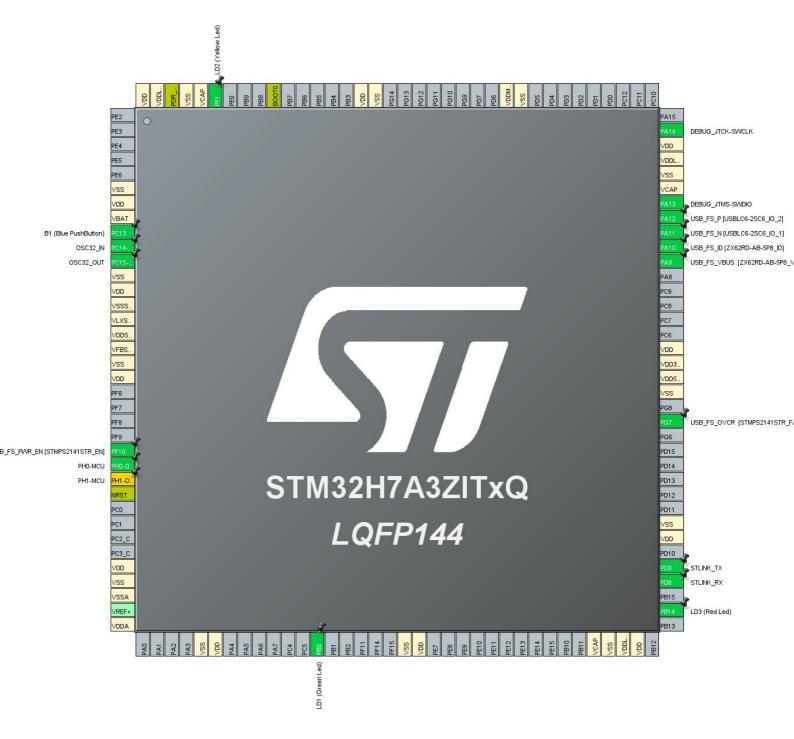
## 1.2. MCU

MCU Series	STM32H7
MCU Line	STM32H7A3/7B3
MCU name	STM32H7A3ZITxQ
MCU Package	LQFP144
MCU Pin number	144

# 1.3. Core(s) information

Core(s)	Arm Cortex-M7

# 2. Pinout Configuration



# 3. Pins Configuration

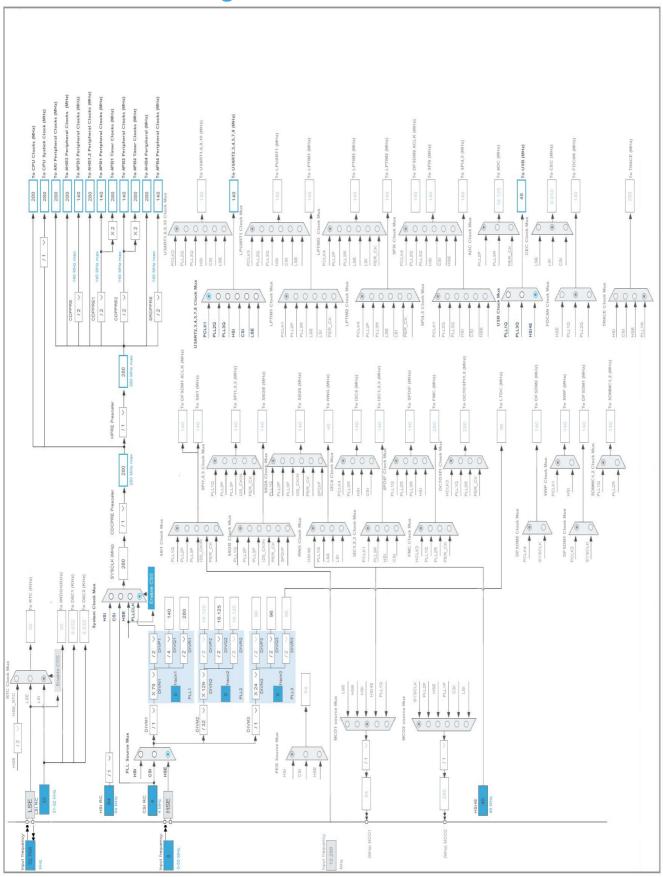
Pin Number	Pin Name	Pin Type	Alternate	Label
LQFP144	(function after		Function(s)	
	reset)			
6	VSS	Power		
7	VDD	Power		
8	VBAT	Power		
9	PC13 *	I/O	GPIO_Input	B1 (Blue PushButton)
10	PC14-OSC32_IN	I/O	RCC_OSC32_IN	OSC32_IN
11	PC15-OSC32_OUT	I/O	RCC_OSC32_OUT	OSC32_OUT
12	VSS	Power		
13	VDD	Power		
14	VSSSMPS	Power		
15	VLXSMPS	Power		
16	VDDSMPS	Power		
17	VFBSMPS	Power		
18	VSS	Power		
19	VDD	Power		
24	PF10 *	I/O	GPIO_Output	USB_FS_PWR_EN [STMPS2141STR_EN]
25	PH0-OSC_IN	I/O	RCC_OSC_IN	PH0-MCU
26	PH1-OSC_OUT **	I/O	RCC_OSC_OUT	PH1-MCU
27	NRST	Reset		
32	VDD	Power		
33	VSS	Power		
34	VSSA	Power		
36	VDDA	Power		
41	VSS	Power		
42	VDD	Power		
49	PB0 *	I/O	GPIO_Output	LD1 (Green Led)
55	VSS	Power		
56	VDD	Power		
68	VCAP	Power		
69	VSS	Power		
70	VDDLDO	Power		
71	VDD	Power		
74	PB14 *	I/O	GPIO_Output	LD3 (Red Led)
76	PD8	I/O	USART3_TX	STLINK_RX
77	PD9	I/O	USART3_RX	STLINK_TX
79	VDD	Power		

Pin Number LQFP144	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
80	VSS	Power		
87	PG7	I/O	GPIO_EXTI7	USB_FS_OVCR [STMPS2141STR_FAULT]
89	VSS	Power		
90	VDD50_USB	Power		
91	VDD33_USB	Power		
92	VDD	Power		
98	PA9	I/O	USB_OTG_HS_VBUS	USB_FS_VBUS [ZX62RD- AB-5P8_VBUS]
99	PA10	I/O	USB_OTG_HS_ID	USB_FS_ID [ZX62RD-AB- 5P8_ID]
100	PA11	I/O	USB_OTG_HS_DM	USB_FS_N [USBLC6- 2SC6_IO_1]
101	PA12	I/O	USB_OTG_HS_DP	USB_FS_P [USBLC6- 2SC6_IO_2]
102	PA13	I/O	DEBUG_JTMS-SWDIO	
103	VCAP	Power		
104	VSS	Power		
105	VDDLDO	Power		
106	VDD	Power		
107	PA14	I/O	DEBUG_JTCK-SWCLK	
118	VSS	Power		
119	VDDMMC	Power		
128	VSS	Power		
129	VDD	Power		
135	воото	Boot		
139	PE1 *	I/O	GPIO_Output	LD2 (Yellow Led)
140	VCAP	Power		
141	VSS	Power		
142	PDR_ON	Reset		
143	VDDLDO	Power		
144	VDD	Power		

<sup>\*</sup> The pin is affected with an I/O function

<sup>\*\*</sup> The pin is affected with a peripheral function but no peripheral mode is activated

# 4. Clock Tree Configuration



Page 5

# 5. Software Project

## 5.1. Project Settings

Name	Value
Project Name	Nucleo-H7A3ZIQ_Test_01
Project Folder	C:\000. Work\001. FW\Git_ESP32_Server_http_json\Nucleo-H7A3ZIQ_Test_01
Toolchain / IDE	STM32CubeIDE
Firmware Package Name and Version	STM32Cube FW_H7 V1.11.2
Application Structure	Advanced
Generate Under Root	Yes
Do not generate the main()	No
Minimum Heap Size	0x200
Minimum Stack Size	0x400

# 5.2. Code Generation Settings

Name	Value
STM32Cube MCU packages and embedded software	Copy only the necessary library files
Generate peripheral initialization as a pair of '.c/.h' files	Yes
Backup previously generated files when re-generating	No
Keep User Code when re-generating	Yes
Delete previously generated files when not re-generated	Yes
Set all free pins as analog (to optimize the power consumption)	No
Enable Full Assert	No

## 5.3. Advanced Settings - Generated Function Calls

Rank	Function Name	Peripheral Instance Name
1	SystemClock_Config	RCC
2	MX_GPIO_Init	GPIO
3	MX_USART3_UART_Init	USART3
4	MX_USB_OTG_HS_USB_Init	USB_OTG_HS
5	MX_TIM1_Init	TIM1

# 6. Power Consumption Calculator report

### 6.1. Microcontroller Selection

Series	STM32H7
Line	STM32H7A3/7B3
мси	STM32H7A3ZITxQ
Datasheet	DS13139_Rev0

## 6.2. Parameter Selection

Temperature	25
Vdd	3.0

## 6.3. Battery Selection

Battery	Li-SOCL2(A3400)
Capacity	3400.0 mAh
Self Discharge	0.08 %/month
Nominal Voltage	3.6 V
Max Cont Current	100.0 mA
Max Pulse Current	200.0 mA
Cells in series	1
Cells in parallel	1

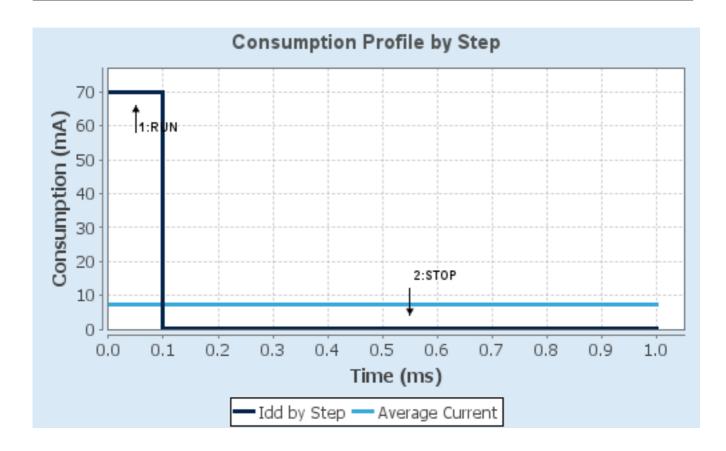
# 6.4. Sequence

Step	Step1	Step2
Mode	RUN	STOP
Vdd	3.0	3.0
Voltage Source	Battery	Battery
Range	VOS0	SVOS5
SRDomain	DRUN	DSTOP
n/a	SRDRUN	SRDSTOP
Fetch Type	ITCM/DTCM/Cache	NA
CPU Frequency	280 MHz	64 MHz
Clock Configuration	HSE PLL	HSI Flash-ON
Clock Source Frequency	16 MHz	64 MHz
Peripherals		
Additional Cons.	0 mA	0 mA
Average Current	69.92 mA	263.82 µA
Duration	0.1 ms	0.9 ms
DMIPS	599.0	0.0
Ta Max	115.77	124.97
Category	In DS Table	In DS Table

## 6.5. Results

Sequence Time	1 ms	Average Current	7.23 mA
Battery Life	19 days, 14 hours	Average DMIPS	599.2 DMIPS

## 6.6. Chart



# 7. Peripherals and Middlewares Configuration

#### **7.1. DEBUG**

**Debug: Serial Wire** 

#### 7.2. RCC

High Speed Clock (HSE): BYPASS Clock Source

Low Speed Clock (LSE): Crystal/Ceramic Resonator

7.2.1. Parameter Settings:

#### **Power Parameters:**

SupplySource PWR\_DIRECT\_SMPS\_SUPPLY
Power Regulator Voltage Scale Power Regulator Voltage Scale 0

**RCC Parameters:** 

TIM Prescaler Selection Disabled
HSE Startup Timout Value (ms) 100
LSE Startup Timout Value (ms) 5000
CSI Calibration Value 16
HSI Calibration Value 64

**System Parameters:** 

VDD voltage (V) 3.3

Flash Latency(WS) 7 WS (8 CPU cycle)

**PLL range Parameters:** 

PLL1 input frequency range Between 8 and 16 MHz
PLL1 clock Output range Wide VCO range

#### 7.3. SYS

Timebase Source: SysTick

#### 7.4. TIM1

**Clock Source: Internal Clock** 

7.4.1. Parameter Settings:

#### **Counter Settings:**

Prescaler (PSC - 16 bits value) 279 \*

Counter Mode Up

Counter Period (AutoReload Register - 16 bits value) 999 \*

Internal Clock Division (CKD)

No Division

Repetition Counter (RCR - 16 bits value) 0

auto-reload preload Disable

#### **Trigger Output (TRGO) Parameters:**

Master/Slave Mode (MSM bit) Disable (Trigger input effect not delayed)

Trigger Event Selection TRGO Reset (UG bit from TIMx\_EGR)

Trigger Event Selection TRGO2 Reset (UG bit from TIMx\_EGR)

#### **7.5. USART3**

### **Mode: Asynchronous**

#### 7.5.1. Parameter Settings:

#### **Basic Parameters:**

Baud Rate 115200

Word Length 8 Bits (including Parity)

Parity None Stop Bits 1

#### **Advanced Parameters:**

Data Direction Receive and Transmit

Over Sampling 16 Samples
Single Sample Disable
ClockPrescaler 1
Fifo Mode Disable

Txfifo Threshold 1 eighth full configuration Rxfifo Threshold 1 eighth full configuration

#### **Advanced Features:**

Auto Baudrate Disable TX Pin Active Level Inversion Disable Disable **RX Pin Active Level Inversion** Data Inversion Disable Disable TX and RX Pins Swapping Overrun Enable DMA on RX Error Enable MSB First Disable

#### 7.6. USB\_OTG\_HS

Internal FS Phy: OTG/Dual\_Role\_Device

<b>Activate</b>	VRUS-	Activate-\	/RUS

\* User modified value

# 8. System Configuration

# 8.1. GPIO configuration

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
DEBUG	PA13	DEBUG_JTMS- SWDIO	n/a	n/a	n/a	
	PA14	DEBUG_JTCK- SWCLK	n/a	n/a	n/a	
RCC	PC14- OSC32_IN	RCC_OSC32_IN	n/a	n/a	n/a	OSC32_IN
	PC15- OSC32_OU T	RCC_OSC32_O UT	n/a	n/a	n/a	OSC32_OUT
	PH0- OSC_IN	RCC_OSC_IN	n/a	n/a	n/a	PH0-MCU
USART3	PD8	USART3_TX	Alternate Function Push Pull	No pull-up and no pull-down	Low	STLINK_RX
	PD9	USART3_RX	Alternate Function Push Pull	No pull-up and no pull-down	Low	STLINK_TX
USB_OTG_ HS	PA9	USB_OTG_HS_ VBUS	Input mode	No pull-up and no pull-down	n/a	USB_FS_VBUS [ZX62RD-AB-5P8_VBUS]
	PA10	USB_OTG_HS_I D	Alternate Function Push Pull	No pull-up and no pull-down	Low	USB_FS_ID [ZX62RD-AB- 5P8_ID]
	PA11	USB_OTG_HS_ DM	Alternate Function Push Pull	No pull-up and no pull-down	Low	USB_FS_N [USBLC6- 2SC6_IO_1]
	PA12	USB_OTG_HS_ DP	Alternate Function Push Pull	No pull-up and no pull-down	Low	USB_FS_P [USBLC6- 2SC6_IO_2]
Single Mapped Signals	PH1- OSC_OUT	RCC_OSC_OUT	n/a	n/a	n/a	PH1-MCU
GPIO	PC13	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	B1 (Blue PushButton)
	PF10	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	USB_FS_PWR_EN [STMPS2141STR_EN]
	PB0	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	LD1 (Green Led)
	PB14	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	LD3 (Red Led)
	PG7	GPIO_EXTI7	External Interrupt Mode with Rising edge trigger detection	No pull-up and no pull-down	n/a	USB_FS_OVCR [STMPS2141STR_FAULT]
	PE1	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	LD2 (Yellow Led)

# 8.2. DMA configuration

nothing configured in DMA service

# 8.3. BDMA1 configuration

nothing configured in DMA service

# **8.4. BDMA2 configuration** nothing configured in DMA service

# **8.5. MDMA configuration** nothing configured in DMA service

# 8.6. NVIC configuration

# 8.6.1. NVIC

Interrupt Table	Enable	Preenmption Priority	SubPriority	
Non maskable interrupt	true	0	0	
Hard fault interrupt	true	0	0	
Memory management fault	true	0	0	
Pre-fetch fault, memory access fault	true	0	0	
Undefined instruction or illegal state	true	0	0	
System service call via SWI instruction	true	0	0	
Debug monitor	true	0	0	
Pendable request for system service	true	0	0	
System tick timer	true	0	0	
TIM1 update interrupt	true	0	0	
PVD and PVM interrupts through EXTI line	unused			
Flash global interrupt		unused		
RCC global interrupt		unused	unused	
EXTI line[9:5] interrupts	unused			
TIM1 break interrupt	unused			
TIM1 trigger and commutation interrupts	unused			
TIM1 capture compare interrupt	unused			
USART3 global interrupt		unused		
FPU global interrupt		unused		
HSEM1 global interrupt		unused		
ECC diagnostic Global Interrupt		unused		

# 8.6.2. NVIC Code generation

Enabled interrupt Table	Select for init sequence ordering	Generate IRQ handler	Call HAL handler
Non maskable interrupt	false	true	false
Hard fault interrupt	false	true	false
Memory management fault	false	true	false
Pre-fetch fault, memory access fault	false	true	false
Undefined instruction or illegal state	false	true	false
System service call via SWI instruction	false	true	false
Debug monitor	false	true	false
Pendable request for system service	false	true	false
System tick timer	false	true	true
TIM1 update interrupt	false	true	true

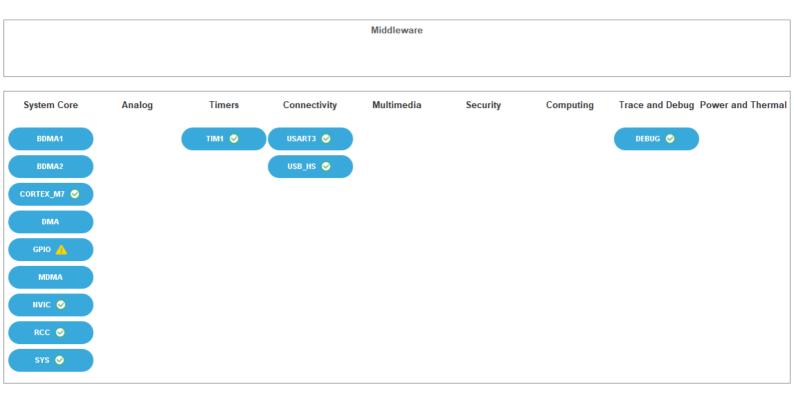
Nucleo-H7A3ZIQ_Test_01 Project
Configuration Repor

* He are see differed scales		
* User modified value		

# 9. System Views

9.1. Category view

9.1.1. Current



## 10. Docs & Resources

Type Link

BSDL files https://www.st.com/resource/en/bsdl\_model/stm32h7\_bsdl.zip

IBIS models https://www.st.com/resource/en/ibis\_model/stm32h7\_ibis.zip

System View https://www.st.com/resource/en/svd/stm32h7-svd.zip

Description

System View https://www.st.com/resource/en/svd/stm32h7rs-svd.zip

Description

Presentations https://www.st.com/resource/en/product\_presentation/microcontrollers\_st

m32h7\_series\_product\_overview.pdf

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- guide-for-stm8-stm32-and-legacy-mcus-stmicroelectronics.pdf
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- on-stm32f7-series-and-stm32h7-series-stmicroelectronics.pdf
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