UNIVERSITY OF TEHRAN
Electrical and Computer Engineering Department
Digital Logic Design, ECE 367 / Digital Systems I, ECE 894
Spring 1401-02
Computer Assignment 2
Basic RTL Packages
Week 6

Name:
Date:

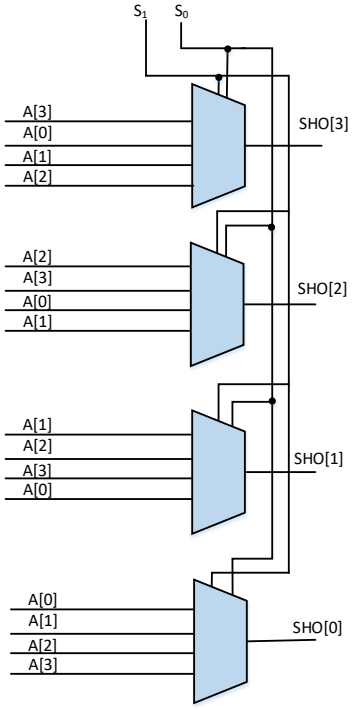
In this assignment you will use the multiplexer of Computer Assignment 1 to build n-bit barrel shifters. A barrel shifter is a circuit with an *n*-bit data-input, *A[n-1:0]*, and an *i*-bit shift-value, *N[i-1:0]*, input. The value of *i* is: $i=log_2 n$. The output of the shifter is the *A* input rotated *N* places to the right. Table below shows the output table for a 4-bit barrel shifter.

Shift Value N[1:0]	Shifted Output (SHO)			
00	A_3	A_2	A_1	A_0
01	A_0	A_3	A_2	A_1
10	A_1	A_0	A_3	A_2
11	A_2	A_1	A_0	A_3

1. Using an **assign** statement, write SystemVerilog description of the 4-to-1 MUX of Part 3 of CA 1. Use delay values as obtained from the simulation of multiplexer of Part 4 of CA 1.
2. Using four 4-to-1 Multiplexers of Part 1, build a 4-bit barrel shifter. The circuit for this purpose is shown below, and it implements the table shown above. Use module instantiations in a **generate** statement for instantiating four instances of the multiplexer shown. Simulate this circuit and find its worst-case delay values.
3. Using multiplexers of Part 1 generate a 16-to-1 multiplexer. Use **generate** statements for generating the necessary number of expressions or instances of the 4-to-1 multiplexer. Simulate this circuit and find its worst-case delay values.
4. Inspired by the 4-bit barrel shifter of Part 2 and using the 16-to-1 multiplexers of Part 3, build a 16-bit barrel shifter. Use **generate** statements for instantiating the necessary number of instances of the 16-to-1 multiplexer. Simulate this circuit and find its worst-case delay values.

In all the above parts, generate testbenches for your circuits in SystemVerilog and examine them for various input changes. Among the various input changes, make sure you test the circuits for

the worst-case delay of its output making To1 and To0 transitions. Make sure the time distance between your input changes is much larger than the circuit delay values.



Deliverables:

Generate a report that includes item discussed below for each of the four parts of this CA. Solutions without use of **generate** statements are not accepted.

A. Show the circuit diagram that you are analyzing. Show how the multiplexers are wired together to form the structure you are designing. Part 1 uses only a single multiplexer.
B. Hand-simulate the circuit you have shown in each part and write your expected values. For example, indicate what values you expect for the worst-case delays and express your reason for that.
C. Show your SystemVerilog description of the design you are simulating and the testbench for it. Best is to use the Snip tools to get the image from Notepad++. This way you see all keywords and indentations. Make sure your SV codes are properly indented and all line-up rules are followed.
D. Show an image of the project that you have created in ModelSim for the simulation of your circuit.
E. When simulation is complete, or even if you have a partial simulation, include an image of the output waveform showing signal names being displayed.

Make a PDF file of your report and name it with the format shown below:

FirstinitialLastnameStudentnumber-CAn-ECEmmm

Where *nn* is a two-digit number for the Computer Assignment, *mmm* is the three-digit course number under which you are registered, and hopefully you know the rest. For the *Firstinitial* use only one character. For *Lastname* and for the multi-part last names use the part you are most

identified with. Use the last five digits of your student id (exclude 8101) for the *Studentnumber* field of the report file name.