UNIVERSITY OF TEHRAN
Electrical and Computer Engineering Department
Digital Logic Design, ECE 367 / Digital Systems I, ECE 894
Spring 1402
Computer Assignment 3
RT Level Components, Iterative Logic, Synthesis - Week 12

Name:	**Date:**
Username:	

The problem for this assignment is a circuit that calculates the divide-by-seven remainder of a 48-bit input vector. The circuit has a 48-bit input, a 3-bit output, and it is built of cascadable modules in a regular structure.

1. Show the design of a residue-7 circuit that has two 3-bit inputs and a 3-bit output. Using the delay values from transistors of Computer Assignment 1, estimate the worst-case gate delays of your full-adder structures, the incrementer and other gates in the residue-7 circuit. Write a parameterized residue-7 using **assign** statements and abstract operations like add, compare, and selection operator.
2. Use **generate** statements, write SystemVerilog description for a 48-bit input residue7 circuit. Simulate this structure and verify your circuit and its worst-case delay values.
3. Based on delay values of Part 1, write a parametrized description of the 48-bit residue circuit. Use any operator that makes your description easier. Use **#parameter(…)** construct to specify the number of bits and the delay per 6-bit residue 7 circuit. You can use an **assign** statement for this description. No need to do a structural description like Part 2.
4. Test the 48-bit residue-7 circuit of Part 2 in a SystemVerilog testbench. Use constructs such as **repeat** and **$random()** for test data generation.
5. Test the 48-bit residue-7 circuit of Part 3 in a SystemVerilog testbench. Use constructs such as **repeat** and **$random()** for test data generation. Compare with simulations of Part 4
6. Using YoSys synthesize the circuit of Part 2 and that of Part 3 and compare the results.