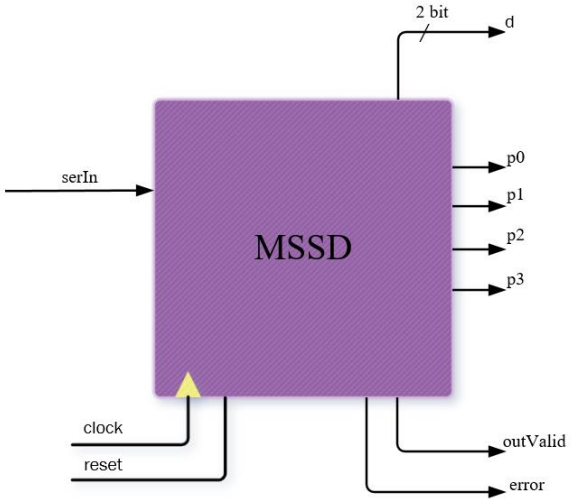
UNIVERSITY OF TEHRAN
Electrical and Computer Engineering Department
Digital Logic Design, ECE 367 / Digital Systems I, ECE 894
Spring 1402
Computer Assignment 4-5
State Machines and Basic RTL
Quartus Pre- and Post-Layout Simulation

Name:	**Date:**
Username:	

In this assignment, you will design a Multi-channel Synchronous Serial communication Demultiplexer MSSD. The source provides a stream of 1-bit data that includes the size of the data to be transferred, the destination port, and the actual data.

Problem Description: Serial bits of data appear on the *serIn* input of MSSD. Normally, in *"no-transmission mode"*, *serIn* is 1. Transmission begins when *serIn* makes a 1 to 0 transition. The 0 value bit marks the beginning of the transmission and has no other information. The two bits that follow are the port number, p, MSB first in time. The next 4 bits are the number of bytes, n, MSB comes first in time. With 1 + 2 + 4 + n×8 clock cycles after *serIn* becomes 0, it will return to 1 and another transmission begins with another start-bit. Data on *serIn* are synchronized with the MSSD clock, *clk*. This multiplexer extracts the destination code (*d*, two bits) and the number of bytes that will go to the destination port (*n*, 6 bits). Following this, the next *n*×8 bits will be transmitted to port *d*. In addition to the four ports of MSSD, i.e., *p0*, *p1*, *p2*, and *p3*, the active port id, i.e., *d*, an *outValid* signal, and an error signal are the outputs of MSSD. The *outValid* signal remains 1 for as long as actual data is being transmitted to an output port. The error signal should be issued if the value of *serIn* does not become 1(*"no-transmission mode"*) after 1 + 2 + 4 + *n*×8 clock cycles.



Simulation:

a. Using state machines, counters, shift-registers and other RTL components discussed in class show the design of the MSSD circuit.
b. In a SystemVerilog module describe individual components of this circuit and wire them together within the MSSD module.
c. Write a testbench to test your design of MSSD. Perform ModelSim simulation for several destinations and transmit data sizes.

Netlist Synthesis (basic gates target):

a. Take the entire MSSD module into Yosys and synthesize it to our standard library.
b. Run Verilog simulation to verify the operation of the post-synthesis Yosys output.

Synthesis and post-synthesis simulation (FPGA target):

c. Take the entire MSSD module into Quartus, synthesize it and generate a symbol for it.
d. Instantiate MSSD within a top-level Quartus Block Diagram, and connect the input output pins.
e. Synthesize the circuit you generated in Quartus to generate .vo and .sdo files.
f. Add the post-synthesis output of the previous part to the testbench you generated for simulation part and run the same simulations to compare the results.
g. Verify timing and operation of the post-synthesis output.

Deliverables:

A complete report containing answers to all parts of each question. Your report should include enough design illustration, description, actual data, and output justification. Note that your reports should be well-organized.

Attention:

Make a *PDF* file of your report and submit it to the course site. Also, compress all files and documents mentioned in the *Deliverables* section into a *zip* file and upload the generated file.