UNIVERSITY OF TEHRAN
Electrical and Computer Engineering Department
Digital Logic Design, ECE 367 / Digital Systems I, ECE 894
Spring 1402
Computer Assignment 6
RT Level Component Design and FPGA Implementation - Week 24

Name:	**Date:**
Username:	

1. **RTL Design of a Selection Sorter (ascending order).** A memory block of 256 16-bit words is given that contains binary data. This is an SRAM with a *readMem*, *writeMem, rdyMem* and clock control inputs. The memory has a 16-bit *inBus*, a 16-bit *outBus*, and 8 address lines (*addrBus*).
   In this assignment you are asked to design a Selection Sorter. The sorter has a *start* signal that begins the sorting of 256 words in the memory block, and a *done* signal that becomes 1 when sorting is complete, and it is waiting for the next start.
   a. Design an RTL circuit with a datapath and controller for sorting the data in the memory block.
   b. Write Verilog description of the sorter circuit.
   c. For initializing the SRAM, create the .hex file according to the attached tutorial and then fill the SRAM with the file.