An Enhanced Linear Active Disturbance Rejection Controller Based Dual Active Bridge Converters for EV Charging

Prashant Kumar, *Member, IEEE*, Ali Arzani, *Member, IEEE*,
Sohag Kumar Saha, *Student Member, IEEE*, and Satish M. Mahajan, *Life Senior Member, IEEE*
Center for Energy Systems Research (CESR), Tennessee Technological University, Cookeville, TN 38505, USA
{pkumar, aarzani, ssaha42, smahajan}@tntech.edu

2025 IEEE Energy Conversion Conference Congress and Exposition (ECCE) | 979-8-3315-4130-9/25/$31.00 ©2025 IEEE | DOI: 10.1109/ECCE58356.2025.11260107

***Abstract*—Dual active bridge (DAB) converters are a highly desirable converter topology for high-power battery charging in transportation electrification applications. This is mainly due to their bidirectional power flow capability and high power quality. Nevertheless, these converters may experience low-frequency output ripple due to system nonlinearities and power inconsistencies, hence diminishing output power quality and battery longevity. This paper presents an active disturbance rejection control (ADRC) algorithm to deal with the disturbances of the DAB converter. The enhanced ADRC controller estimates disturbances and reduces high-frequency gain, low-frequency ripple, and requirements for current sensors. Real-time simulations have been carried out on a Typhoon HIL 606 device to evaluate the proposed controller performance, demonstrating its rapid dynamic performance under diverse operating conditions.**

***Index Terms*—Active disturbance rejection controller, battery charging, dc offset, dual active bridge power converter**

I. Introduction

Dual active bridge (DAB) power converters have gained significant attention in different applications, including high-performance electric vehicle (EV) charging systems, due to their galvanic isolation, bidirectional power transfer capabilities, and soft-switching properties [1], [2]. Such advantages enable high-frequency operation with reduced switching losses of DAB converter [3]. The inherent flexibility of the DAB topology facilitates efficient voltage conversion and seamless integration with both the grid and distributed energy resources, making it a compelling choice for fast-charging infrastructure [4], [5]. However, despite these advantages, the DAB converter remains susceptible to performance degradation caused by low-frequency output voltage ripple, nonlinearities, and dynamic disturbances introduced by variations in load and input voltage [6]. Such disturbances, particularly under constant power loads and rapidly fluctuating demand, can severely impact output power quality and consequently the lifespan of EV batteries [7]–[9].

In DAB converters, the isolating stage uses a high-bandwidth closed-loop control, which can stress the intermediate dc-link capacitors and cause voltage fluctuations during load changes [10]. This may lead to overmodulation and high current surges. To address these challenges, advanced control methods are needed to attenuate the disturbances and uncertainties. While sliding mode control offers fast and robust voltage tracking, it suffers from chattering [11]. The uncertainty and disturbance estimator helps estimate disturbances but relies heavily on accurate models and is sensitive to noise. Model predictive control-based disturbance rejection was proposed in [12]. However, these methods involve the model based control design that necessitates the model information [11]. In contrast, active disturbance rejection control (ADRC) does not depend on precise models, actively compensates for disturbances, and offers robust performance [13]. Linear ADRC, using a linear extended state observer (LESO), further simplifies tuning to just one parameter and improves dynamic response and output impedance compared to traditional PI control [14].

Traditional feedback control methods often struggle to compensate for the coupled nonlinear dynamics and time-varying uncertainties inherent in DAB converter systems [15]. In contrast, ADRC has been developed as a model-independent approach that estimates and mitigates the overall disturbances in real time [16], [17]. With the extended state observer (ESO), ADRC incorporates dynamic feedback laws, and ensures improved transient response and tracking performance even in presence of modeling inaccuracies. To address the challenges posed by both periodic disturbances, such as low-frequency ripple, and non-periodic disturbances arising from load transients or source fluctuations, this paper proposes an enhanced linear ADRC framework tailored for DAB power converters with potential utilization in EV battery fast chargers.

The proposed control architecture integrates a Linear ESO

This work is supported by the U.S. Appalachian Regional Commission (ARC) under Grant MU-21579-23. Any opinions, findings, and conclusions or recommendations expressed in this material are those of the author(s) and do not necessarily reflect the views of ARC.

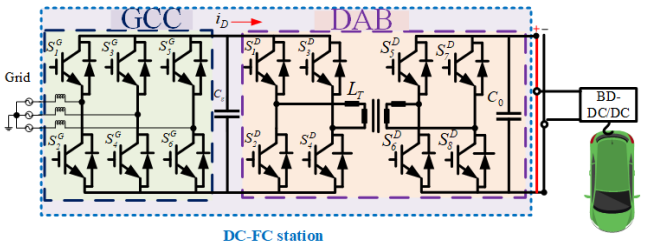


Fig. 1. DAB power converter topology

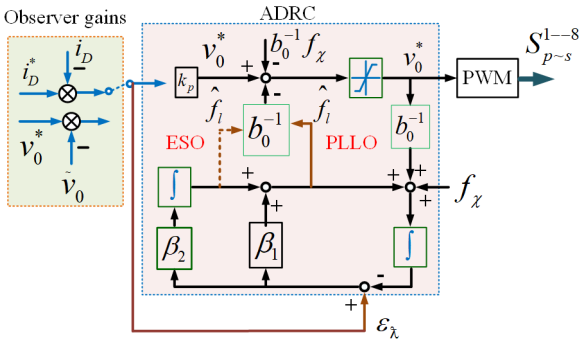


Fig. 2. Enhanced ADRC control for DAB converter system

(LESO) and a Phase-Locked Loop Observer (PLLO), offering a synergistic strategy that improves dynamic regulation, suppresses ripple, and minimizes reliance on current sensors. Such model-free control strategies improve disturbance rejection capabilities with fast dynamic response. Considering the measurement noise, external disturbances, and parameter variations, the controller performance indicates proper disturbance rejection. Real-time simulations in a Typhoon HIL 606 device have been carried out to show the efficacy of the method, demonstrating fast dynamic tracking and superior noise rejection under diverse operating conditions. In doing so, this work contributes a scalable, sensor-efficient solution for resilient battery charging to potentially utilize in next-generation mobility infrastructure.

The ADRC for DAB converter has been described in the following sections. Section II establishes small-signal modeling of DAB converter to present the disturbances in control loops. Section III provides formulations of the proposed LADRC for DAB converter. The validation of LADRC algorithm is provided in Section IV. Further, Section V discusses the conclusion.

II. DAB Converter Modeling and Proposed ADRC Methodology

Fig. 1 depicts the topological structure of a DAB converter. Single-phase-shift (SPS) modulation has been implemented as it provides simplest modulation scheme for DAB converter. A reduced-order modeling of the DAB converter is attempted without taking effect of i_p. This is because the dynamics of v_o is relatively unaffected by variations in i_p due to the isolation transformer and the slower response of v_o. The transmitted power (P_t), between active and front-end bridge of DAB converter is given in (1).

$$P_t = \frac{nV_{dc}v_o}{2f_sL_p}d(1-d) \tag{1}$$

Here, d represents phase shift ratio that can be expressed from phase, $\phi_{\text{ps}} = \pi d$, for $-0.5 < d < 0.5$ This allows for the computation of the average input current I_i and the output current I_o, considering a transfer coefficient, $\lambda_i = \frac{n}{2f_sL_p}$. n, v_{dc}, and d denotes transformer turns ratio, input DC voltage, nominal phase shift ratio, respectively. f_s, L_p, and C_o is the switching frequency, primary inductance, output filter capacitance, respectively. By introducing a general form, the average input and output currents can be expressed as (2), where $x \in \{\text{in}, o\}$, $v_{\text{in}} = v_o$, and $v_o = v_{\text{dc}}$.

$$I_x = \lambda_i \cdot v_x \cdot d(1-d), \quad x \in \{\text{in}, o\} \tag{2}$$

From (2), the small signal value of I_0 can be obtained by taking the partial derivative, where $\tilde{i}_o$, $\tilde{d}$ are the small signal values of I_o, d.

$$\tilde{i}_o = \lambda_i \cdot v_{\text{dc}} \cdot (1-2d) \cdot \tilde{d} \tag{3}$$

The dynamic equation of the capacitor current $(\tilde{i}_c = C_o\frac{d\tilde{v}_o}{dt})$ can be expressed as

$$\tilde{v}_o(t) = \tilde{v}_o(0) + \frac{1}{C_o}\int_0^t \left[\lambda_i v_{\text{dc}}(1-2d)\cdot\tilde{d}(\tau) - \frac{\tilde{v}_o(\tau)}{R_B}\right]d\tau \tag{4}$$

R_B denotes the equivalent load resistance in (Ω). Applying the Laplace transform to above, small-signal open-loop transfer function (TF)$G_{vd}(s)$ that corresponds to output voltage to phase-shift ratio

$$G_{vd}(s) = \underbrace{(\lambda_i v_{\text{dc}} R_B(1-2d))}_{\text{DC gain}} \cdot \frac{1}{\tau s + 1} \tag{5}$$

Here, $\tau = R_BC_o$ is the output filter constant.

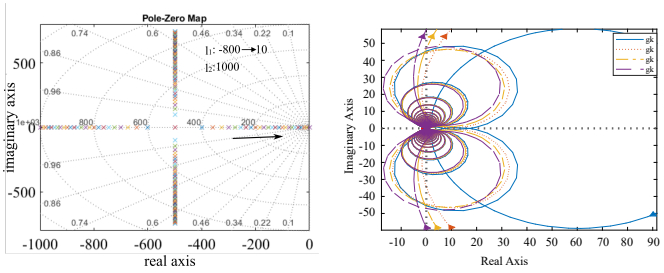
The dynamic equation of the system has been modified as

$$\dot{\tilde{v}}_o = b_0\tilde{d} - a\tilde{v}_o \tag{6}$$

where $a = \frac{1}{\tau}$, $b = \frac{\lambda_i v_i(1-2d)}{C_o}$ and $\tilde{d}$ are the control input.

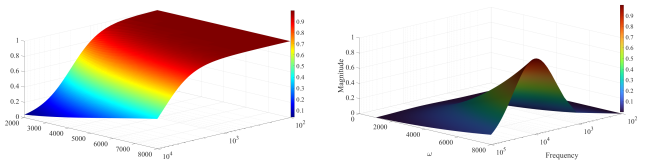
In the presence of disturbances, above expressions can be rewritten as

$$\dot{\tilde{v}}_o = b_0\tilde{d} + f_d \tag{7}$$



(a) pole-zero plot (b) varying controller gain

Fig. 3. Frequency response performance with varying parameters: (a) close loop poles trajectory, (b) magnitude plot



(a) varying gain with respect to ω (b) varying gain with a distinct peak behavior

Fig. 4. Frequency response performance with varying parameters: magnitude of disturbance with varying of different parameters

where, b_0 represents the nominal control gain evaluated at the steady-state operating point for ADRC implementation.

III. Design of Linear ADRC-based Current Controller

A. Current ADRC Design

The small-signal model of the DAB converter is derived by linearizing the output voltage dynamics around a stable operating point. The perturbed output voltage $\tilde{v}_o$ as a function of the perturbed control input $\tilde{d}$ is governed by the following differential equation:

$$\frac{d\tilde{v}_o}{dt} = \left(\frac{\lambda_i v_{dc}(1-2d)}{C_o}\right)\tilde{d} - \left(\frac{1}{\tau}\right)\tilde{v}_o \tag{8}$$

This expression highlights the dynamic dependence of the output voltage on the control input and load resistance. To facilitate control synthesis, this model is recast into an ADRC-compatible form:

$$\frac{d\hat{\tilde{v}}_o}{dt} = b_0\tilde{d} + f_v + f_l \tag{9}$$

where, $b_0 = \frac{\lambda_i v_{dc}(1-2d)}{C_o}$ is the control gain linking the phase shift perturbation to the output voltage change, f_v represents the known internal model dynamics, and f_l denotes the lumped external disturbances and unmodeled dynamics. The control block diagram with enhanced ADRC for the DAB converter is shown in Fig. 2.

1) Linear Extended State Observer: The LESO has been introduced to estimate both the output voltage and the total disturbance. The observer structure is defined by:

$$\frac{d\hat{\tilde{v}}_o}{dt} = b_0\tilde{d} + \hat{f}_v + \hat{f}_l + \beta_1\varepsilon_\chi \tag{10}$$

$$\frac{d\hat{f}_l}{dt} = \beta_2\varepsilon_\chi \tag{11}$$

where $\hat{v}_o$ is the estimated output voltage, $\hat{f}_\chi$ is the estimated total disturbance where $\chi \in \{l, v\}$, and $\varepsilon_\chi = \hat{v_o} - \hat{\tilde{v}}$ is the observer error. The observer gains β_1 and β_2 are tuned based on the desired convergence rate and system bandwidth, ensuring both stability and tracking precision.

Frequency response performance with varying parameters for the closed-loop poles trajectory and magnitude plot for different values of ω is presented in Fig. 3. It has been presented for the pole-zero plot and with different controller gains. The bode frequency response performance with varying parameters and different controller bandwidth frequency (BWF) as illustrated in Fig. 5. The f_l occurs at a lower BWF. From frequency domain analysis, the transient response of LESO, and PLLO observer with a bandwidth of 6000rad/s, are tested by varying v_o^* from 600V to 650V.

2) Phase-Locked Loop Observer: To enhance the disturbance estimation accuracy, especially under periodic disturbances such as low-frequency ripple, a Phase-Locked Loop Observer (PLLO) is incorporated:

$$\frac{d\hat{v}_o}{dt} = b_0\tilde{d} + \hat{f}_v + \hat{f}_l \tag{12}$$

$$\frac{d\hat{f}_l}{dt} = \beta_1\frac{d\varepsilon_\chi}{dt} + \beta_2\varepsilon_\chi \tag{13}$$

where the derivative of the error $\frac{d\varepsilon_\chi}{dt}$ is used to improve the responsiveness of the disturbance estimator, particularly in rejecting fast-changing components. This design ensures better rejection of both harmonic disturbances and aperiodic load variations, with lower sensitivity to sensor noise.

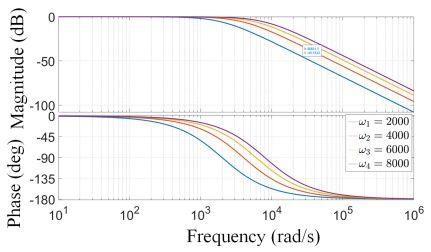
With the disturbance estimations provided by either LESO or PLLO, the closed-loop control law for the phase shift d is formulated as:

$$\tilde{d} = d_0 - b_0^{-1}\left(\hat{f}_v + \hat{f}_l\right) \tag{14}$$

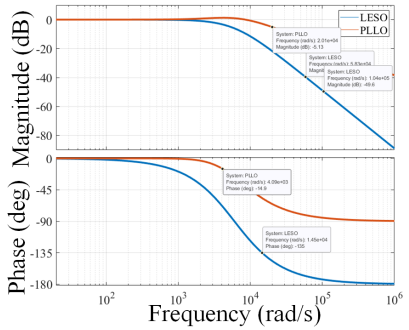
where d_0 is the nominal phase shift generated by the baseline controller (e.g., a proportional-integral controller or a feedforward loop). Substituting this into the perturbed system, the compensated dynamics are given by:

$$\frac{dv_o}{dt} = b_0 d + f_v + f_l = b_0 d_0 + (f_l - \hat{f}_l) \tag{15}$$

When the disturbance estimation error is minimal, i.e., $\hat{f}_l \approx f_l$, the system behaves as if it were undisturbed, thereby



(a) varying bandwidths at ω=2000, 4000, 6000 and 8000



(b) comparison between LESO and PLLO at ω=6000

Fig. 5. Bode frequency response performance with varying parameters

improving regulation performance. The disturbance rejection performance is quantified by the transfer function:

B. Investigation of Stability and Tracking Performance

The closed-loop performance can be attained with choosing a straightforward phase-shift error amplifier as the feedback, expressed as $d_0 = k_p\,(d^* - d)$, k_p denotes proportional constant of the error amplifier. The TF obtained establishes the relations of estimated interruptions $\hat{f}_l$ to the commanded interruptions f_l with the characteristic polynomial of $(s^2+\beta_1 s+\beta_2)$. The performance realised with the proposed algorithm with varying parameters has been presented in Fig. 3. It shows the frequency response performance with varying parameters for the closed-loop poles trajectory. The derived values are subsequently compared to the second-order undamped system $(s+\omega_o)^2$. ω_o denotes undamped natural frequency. ω_o is referred as the bandwidth of the desired closed-loop response. This relation highlights the ability of the observer to approximate the real disturbance within a defined frequency range. By adopting this ADRC structure with LESO and PLLO enhancements, the DAB converter achieves robust voltage regulation with reduced ripple and improved resilience to system uncertainties and load disturbances. From the surface plot of Fig. 4, it is noted that PLLO provides better disturbance rejection capability with varying gain with respect to ω and varying gain with a distinct peak behavior. However, it is more sensitive to noise.

C. Disturbance Transfer Function and its estimation

The gain values of the observer are tuned based on the parameterization that involves assigning the obtained eigenvalues to $-\omega_o$ [18].

$$\frac{\hat{f}_v(s)}{f_v(s)} = \begin{cases} \dfrac{\beta_2}{s^2+\beta_1 s+\beta_2} & \text{using LESO} \\ \dfrac{\beta_1 s+\beta_2}{s^2+\beta_1 s+\beta_2} & \text{using PLLO} \end{cases} \tag{16}$$

$$\Phi_e(s) = \frac{f_v(s)-\hat{f}_v(s)}{f_v(s)} = \begin{cases} \dfrac{s\,(s+\beta_1)}{s^2+\beta_1 s+\beta_2} & \text{using LESO} \\ \dfrac{s^2}{s^2+\beta_1 s+\beta_2} & \text{using PLLO} \end{cases} \tag{17}$$

The proposed algorithm is tested with an observer bandwidth of $\beta_1 = 2\omega_o$. The gain values $\beta_2 = (\omega_o)^2$ denotes the natural frequency. Using the disturbance estimation error transfer function, the error TF of the disturbance $\Phi_e(s)$ is calculated in (17) to assess steady-state response of the voltage ADRC. The $\beta_2 = (\omega_o)^2$ establishes the natural frequency of both the LESO and PLLO observers. The tracking performance depends on tuning these observer gains based on stability criteria.

D. Switching Criteria for DAB Converter

The control switching between PLLO, LESO, and ADRC is determined as follows [8]:

1) Threshold-Based Switching: The system is in a steady state when the output voltage error satisfies: $|v_o - v_{\text{ref}}| < \delta, \quad \delta = \frac{1}{2}\Delta v_o + \delta'$, where Δv_o is the maximum voltage ripple, and δ' accounts for hardware noise and disturbances. If the estimated disturbance $\hat{d}(t)$ satisfies: $|\hat{d}(t)| > \delta_D$

2) Time-Based Switching: If $e_v > \delta$ for $t_2 \geq t_{2d}$, PLLO is engaged to improve transient response. Once system stabilizes for $t_1 \geq t_{1d}$, LESO is switched on for steady-state operation. Delay times are set as: $t_{2d} = (2 \sim 3)T_s, \quad t_{1d} = 1.5t_e$, to prevent unnecessary switching and chattering.

IV. Results and Discussions

The proposed ADRC control scheme are validated through real-time simulations on Typhoon HIL 606 device. Different scenarios are designed to explore various aspects of the system performance under differing operational settings for the DAB converter connected to a high-power battery.

A. Steady-state and rated condition performance analysis:

This case analyzes the steady-state operation of the DAB converter while charging a battery at a 0.5C rate. Fig. 6 illustrates the output voltage (v_{co}) for 800V, succeeded by the output current measured across the battery I_{bat}=-6.15A. The negative current implies the charging of the battery. The input side of the front-end converter has been built to sustain

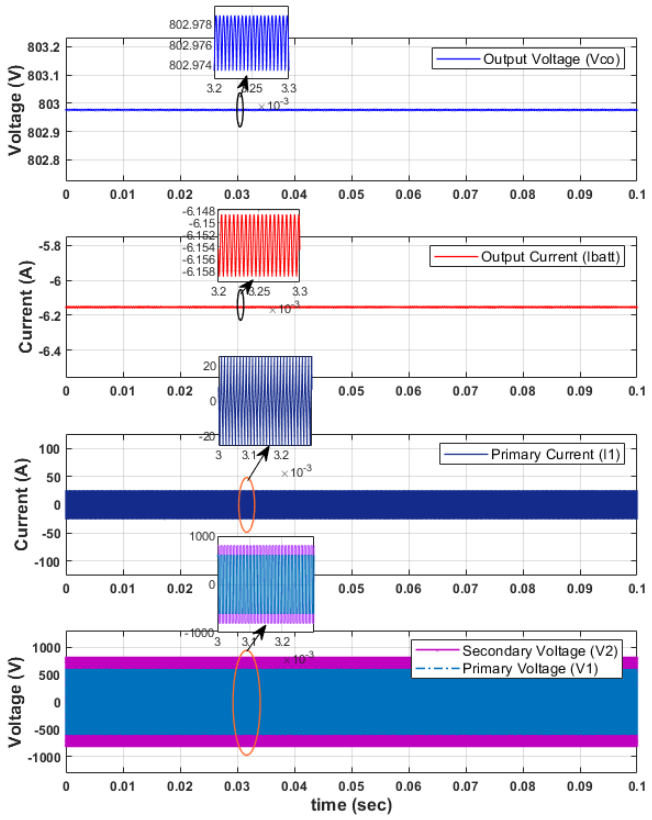


Fig. 6. The HIL results for battery voltage, battery current, primary current, primary and secondary side voltage of DAB.

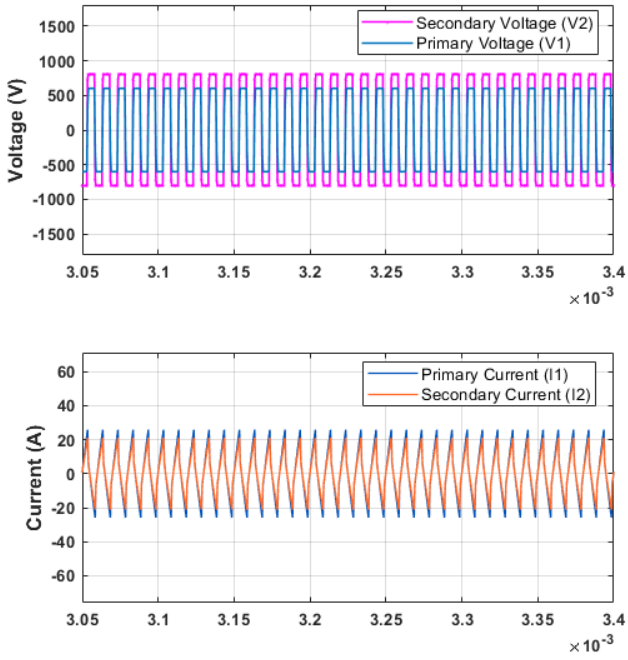


Fig. 7. HIL based voltage and current waveforms for primary and secondary side of DAB

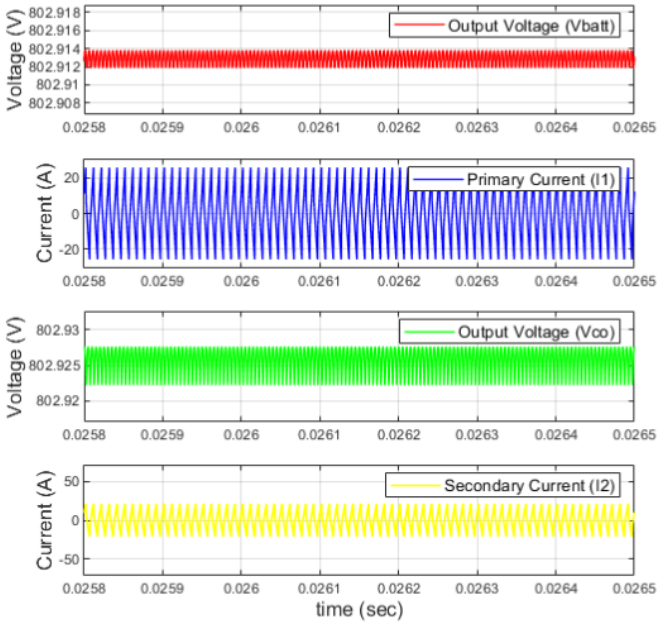


Fig. 8. HIL results for dynamic response of primary- and secondary-side voltage and current

a unity power factor and a stable DC link voltage of 600V, emphasizing the proposed controller's efficacy in eliminating low-frequency ripple, namely the double line frequency ripple (2ω ripple).

Fig. 7 shows the voltages and currents of the DAB converter. The output and input voltages are 800V and 600V, respectively. The current during the bidirectional operation of DAB converter reaches 20A. Such specifications meet the requirements for off-board EV chargers where the power level is larger than 50kW.

B. Dynamic response and stability performance:

The reference current signal is increased from a 0.5C rating to a 1C rating, and decreased to 0.5C. Fig. 8 depicts v_o, i_p, v_{Co} and i_{Co} representing v_o remains stable despite variations in i_{Co}. The settling time and voltage overshoot/undershoot are nearly 14–17ms and 10–11V, respectively, demonstrating the controller's robustness with significant current variations while maintaining stability and reduced voltage fluctuations.

C. System robustness by parameter variations:

This case examines the controller robustness against variations in system parameters by reducing both input and output dc link capacitance. Fig. 8 also shows the waveform considering the output dc link capacitance decreasing by 50%. From Figs. 5, 7 and 8, the transient response of LESO, and PLLO observer with a bandwidth of 6000rad/s, are tested by varying V_o^* from 600V to 650V. The proposed controller maintains low ripple levels due to its high gain at ripple frequencies. The transient response under this condition indicates that in spite

of varying observer bandwidth and varying the voltage, the controller shows very low voltage overshoot with fast settling time when the load is changed. When the load is stepped down, the output voltage overshoot is 5.8V, and the settling time is approximately 8.3ms. The output voltage undershoot is 1.9V with a settling time of 0.3ms when the load increases, and the voltage overshoot is 1.9V with a settling time of 0.4ms when the load decreases, which outperforms LESO. It demonstrates that the proposed LESO has superior voltage deviation and setting time. The susceptibility to parameter errors for each controller is also studied by deviating the inductance L_k and capacitance C_D by ±30% from their nominal values.

V. CONCLUSION

The proposed adaptive LESO demonstrates enhanced control performance in DAB power converter, by effectively rejecting disturbances, maintaining dynamic stability, and exhibiting strong robustness to parameter uncertainties. Comparative analysis confirms that adaptive LESO outperforms conventional observer-based control strategies in terms of transient response, disturbance estimation accuracy, and noise resilience. While the LESO component exhibits slightly increased execution latency relative to the PLLO, this is attributed to its adaptive logic, which dynamically distinguishes between steady-state and transient operating conditions. Importantly, this marginal increase in computation time does not compromise overall controller responsiveness or real-time implementation feasibility. The results validate adaptive LESO as a computationally efficient and highly robust control solution, making it well-suited for potential high-performance EV battery charging systems where precision, speed, and adaptability are critical.

REFERENCES

[1] G. A. Mudiyanselage, N. Keshmiri, and A. Emadi, "A review of dc-dc resonant converter topologies and control techniques for electric vehicle applications," *IEEE Open Journal of Power Electronics*, vol. 4, pp. 945–964, 2023.

[2] W. M. Khan, R. K. Singh, and R. Mahanty, "Current driven fractional power processor for ultrafast charging," *IEEE Transactions on Industrial Electronics*, pp. 1–11, 2025.

[3] Z. Guo and X. Han, "Control strategy of ac-dc converter based on dual active bridge with minimum current stress and soft switching," *IEEE Transactions on Power Electronics*, vol. 37, no. 9, pp. 10 178–10 189, 2022.

[4] D. Mishra, B. Singh, and B. K. Panigrahi, "Adaptive current control for a bidirectional interleaved ev charger with disturbance rejection," *IEEE Transactions on Industry Applications*, vol. 57, no. 4, pp. 4080–4090, 2021.

[5] S. Shao, L. Chen, Z. Shan, F. Gao, H. Chen, D. Sha, and T. Dragičević, "Modeling and advanced control of dual-active-bridge dc–dc converters: A review," *IEEE Transactions on Power Electronics*, vol. 37, no. 2, pp. 1524–1547, 2022.

[6] L. Deng, G. Zhou, Y. Li, and Z. Chen, "Communication-free pulsed power distribution and tracking method for hybrid energy storage system based on active disturbance rejection control," *IEEE Transactions on Power Electronics*, vol. 39, no. 3, pp. 3024–3036, 2024.

[7] M. Ali, M. Yaqoob, L. Cao, and K. H. Loo, "Disturbance-observer-based dc-bus voltage control for ripple mitigation and improved dynamic response in two-stage single-phase inverter system," *IEEE Transactions on Industrial Electronics*, vol. 66, no. 9, pp. 6836–6845, 2019.

[8] H. Yin, L. Cao, X. Zeng, K. H. Loo, and C. Sun, "Fast dynamic control of dual-active-bridge dc–dc converter based on an adaptive linear extended state observer," *IEEE Transactions on Power Electronics*, vol. 39, no. 12, pp. 16 019–16 030, 2024.

[9] K. A. Lodi, A. R. Beig, and K. A. A. Jaafari, "Enhancing open end winding induction motor performance for fault-tolerant all-wheel drive evs with ann-based dtc," *IEEE Transactions on Transportation Electrification*, pp. 1–1, 2025.

[10] H. Yin, L. Cao, X. Zeng, K. H. Loo, and X. Pan, "Enhanced observer with series-correction for active disturbance rejection control in dab converters," *IEEE Transactions on Power Electronics*, pp. 1–10, 2025.

[11] H. Sun, D. Kong, C. Liu, D. Zhu, J. Wang, Y. Jiang, and Z. Pei, "Model-free predictive control of dual active bridge converter based on sliding-mode observer considering parameters' uncertainty," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, pp. 1–1, 2025.

[12] Y. Deng, W. Song, S. Yin, M. Zhong, K. Yang, and X. Feng, "A model predictive control scheme without current sensor of dual active bridge dc–dc converters: Improving dynamic performance and reducing hardware cost," *IEEE Transactions on Transportation Electrification*, vol. 9, no. 2, pp. 2916–2928, 2023.

[13] L. Qin, T. X. Wu, Y. Guan, C. Chen, G. Zhang, and L. Liu, "Decoupling control strategy for input-series-output-parallel dual active bridge converter based on linear active disturbance rejection control," *IEEE Transactions on Industry Applications*, vol. 61, no. 4, pp. 6484–6498, 2025.

[14] J. Nie, Z. Zhao, L. Yuan, R. Duan, B. Shi, and L. Jin, "An energy balance active disturbance rejection control for improving converter stability while maintaining fast dynamic performance," *IEEE Transactions on Power Electronics*, vol. 35, no. 11, pp. 11 304–11 309, 2020.

[15] Y. Wu, M. H. Mahmud, Y. Zhao, and H. A. Mantooth, "Uncertainty and disturbance estimator-based robust tracking control for dual-active-bridge converters," *IEEE Transactions on Transportation Electrification*, vol. 6, no. 4, pp. 1791–1800, 2020.

[16] S. Bandyopadhyay, Z. Qin, and P. Bauer, "Decoupling control of multiactive bridge converters using linear active disturbance rejection," *IEEE Transactions on Industrial Electronics*, vol. 68, no. 11, pp. 10 688–10 698, 2021.

[17] R. Sarda, E. R. Ramos, N. B. Y. Gorla, G. G. Farivar, J. Pou, Y. H. Li, S. B. Vaisambhayana, and A. Tripathi, "A control strategy for solid-state transformers with coupled load disturbance attenuation ability," *IEEE Transactions on Power Electronics*, vol. 39, no. 4, pp. 4029–4041, 2024.

[18] P. Kumar, A. R. Beig, D. V. Bhaskar, K. A. Jaafari, U. R. Muduli, and R. K. Behera, "An enhanced linear active disturbance rejection controller for high performance pmbldcm drive considering iron loss," *IEEE Transactions on Power Electronics*, vol. 36, no. 12, pp. 14 087–14 097, 2021.