

National University of Computer & Emerging Sciences, Karachi  
 Department of Computer Science

SPRING 2022

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|                           |                                   |
|---------------------------|-----------------------------------|
| Course Code: EE-1005      | Course Name: Digital Logic Design |
| Course Teacher: Aamir Ali | Assignment No: 03                 |

21K - 3278

**Instructions for Submission:**

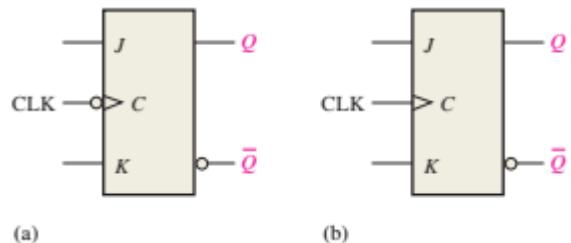
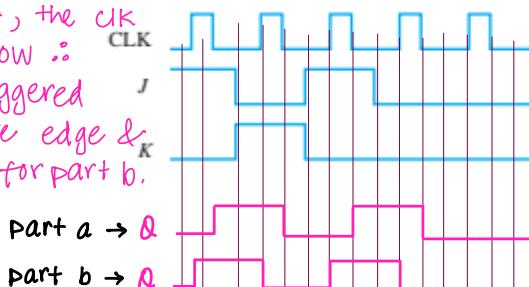
1. Use A4 size paper for solution of each Question.
2. You are required to submit an assignment in hardcopy and also upload scanned copy on Google classroom.
3. Show all steps, otherwise marks will be deducted.
4. The deadline for submission is **23<sup>rd</sup> April, 2022**.
5. **Copying is not allowed at all.** Any similarities among the submitted files of any student will result in **zero marks**.

**CLO #0**

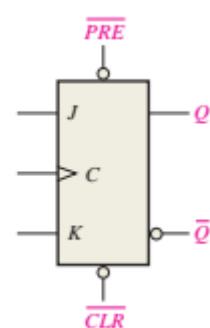
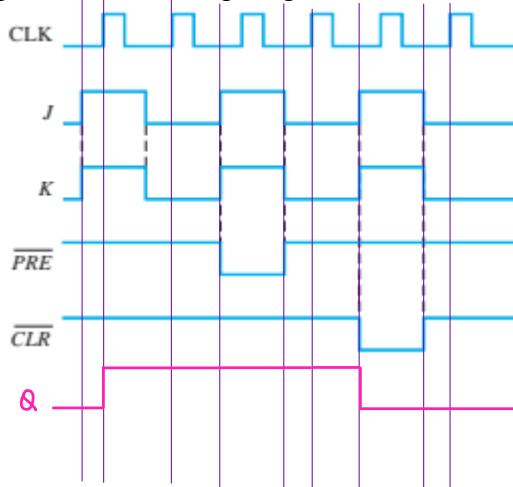
**(Total Marks -100)**

1. Two edge-triggered J-K flip-flops are shown in figure below, If the inputs are as shown, draw the Q output of each flip-flop relative to the clock, and explain the difference between the two. The flip-flops are initially RESET. [10]

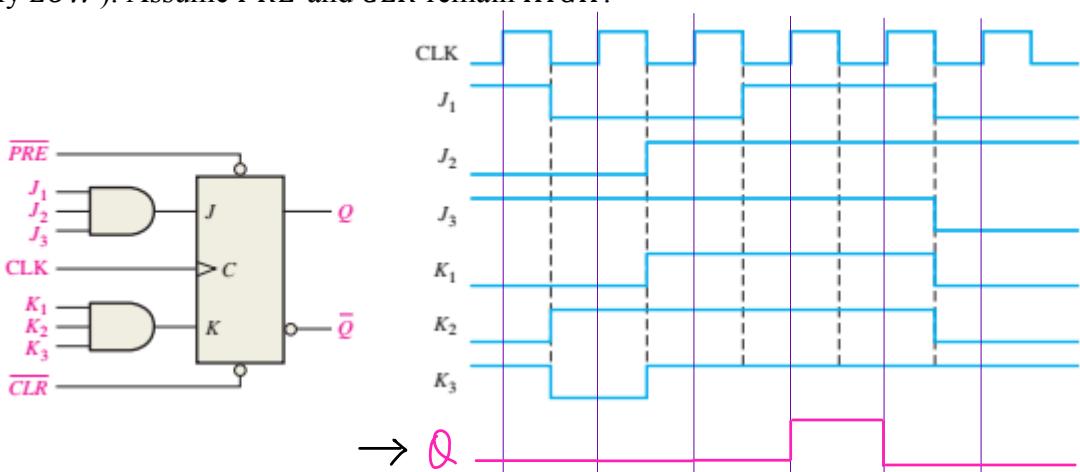
\* In part a, the CLK is active low ∵ it gets triggered on negative edge & vice versa for part b.



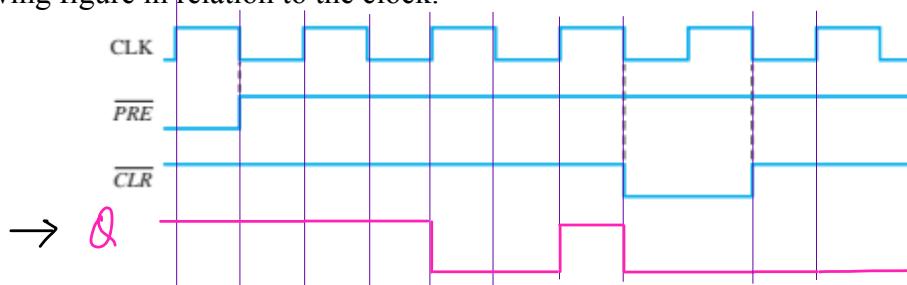
2. Determine the Q waveform relative to the clock if the signals shown in figure below, are applied to the inputs of the J-K flip-flop. Assume that Q is initially LOW. [10]



3. For the circuit in figure below, complete the timing diagram showing the Q output (which is initially *LOW*). Assume  $\overline{PRE}$  and  $\overline{CLR}$  remain *HIGH*. [10]



4. Solve Problem in 3 with the same J and K inputs but with the PRE and CLR inputs as shown in following figure in relation to the clock. [10]

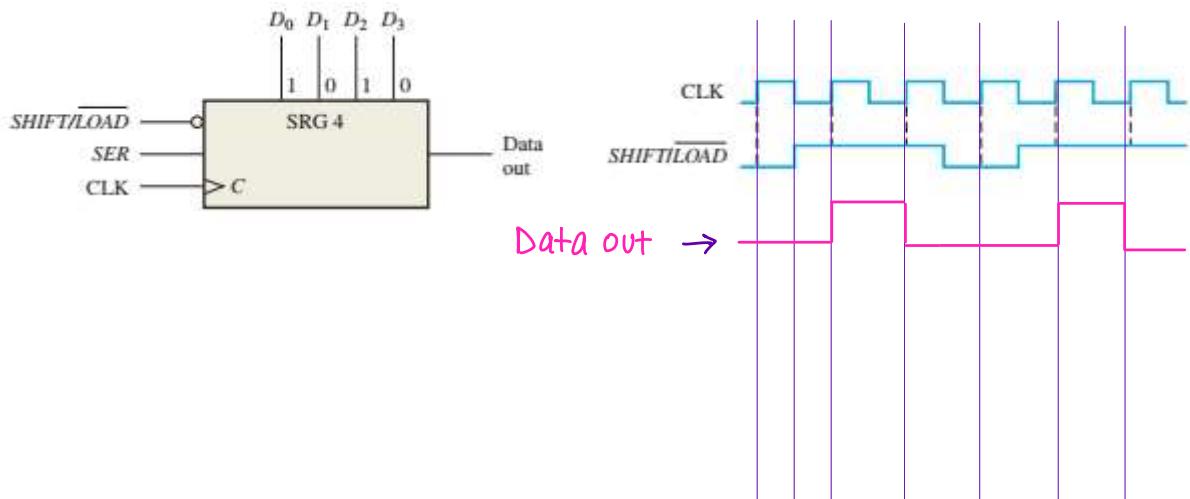


5. Determine the values of the external resistors for a 555 timer used as an astable multivibrator with an output frequency of 10 kHz, if the external capacitor C is 0.004 mF and the duty cycle is to be approximately 80%. [10]

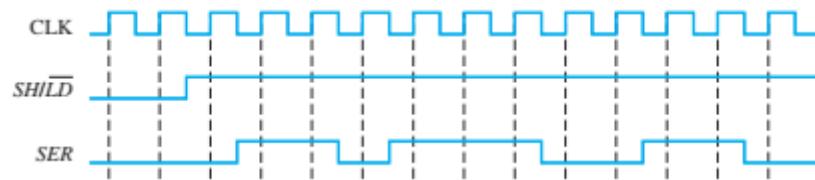
6. What is the state of the register in figure below after each clock pulse if it starts in the 101001111000 state? [10]



7. The shift register in figure below has  $SHIFT/LOAD$  and  $CLK$  inputs as shown in figure below. The serial data input ( $SER$ ) is a 0. The parallel data inputs are  $D_0 = 1$ ,  $D_1 = 0$ ,  $D_2 = 1$ , and  $D_3 = 0$  as shown. Develop the data-output waveform in relation to the inputs. [10]



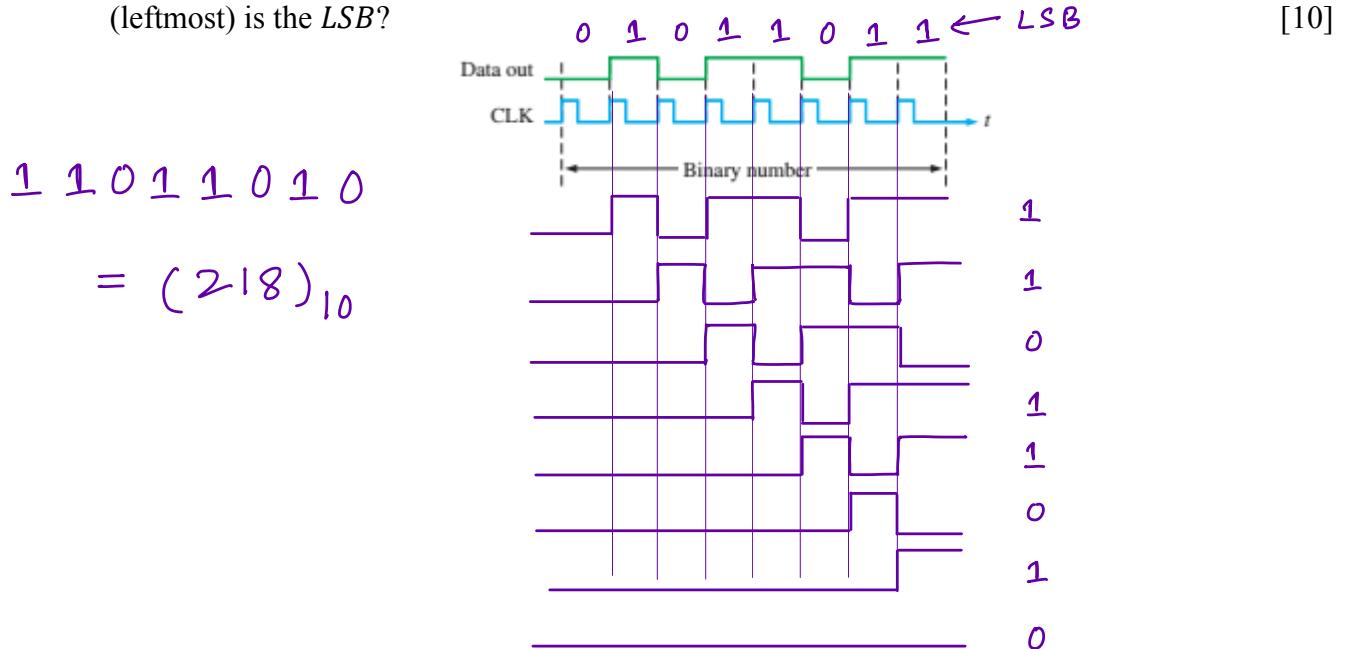
8. Develop the Q0 through Q7 outputs for a 8-bit Serial In Parallel Out shift register with the input waveforms shown in figure below. Here A and B are ANDed and used for Serial In to register. [10]



9. For the 8-bit bidirectional register in figure below, determine the state of the register after each clock pulse for the *RIGHT/LEFT* control waveform given. A *HIGH* on this input enables a shift to the right, and a *LOW* enables a shift to the left. Assume that the register is initially storing the decimal number seventy-six in binary, with the right-most position being the *LSB*. There is a *LOW* on the data-input line. [10]



10. A leading-edge clocked serial in/serial out shift register has a data-output waveform as shown in figure below, what binary number is stored in the 8-bit register if the first data bit out (leftmost) is the *LSB*? [10]



5. Determine the values of the external resistors for a 555 timer used as an astable multivibrator with an output frequency of 10 kHz, if the external capacitor C is 0.004 mF and the duty cycle is to be approximately 80%. [10]

$$T_H = 0.693(R_1 + R_2)C_1 \quad T_L = 0.693R_2C_1$$

$$T = T_H + T_L = 0.693(R_1 + 2R_2)C_1$$

$$f = \frac{1}{T} = \frac{1}{0.693(R_1 + 2R_2)C_1}$$

$$10 \times 10^3 = \frac{1}{0.693(R_1 + 2R_2) \times 0.004 \times 10^{-3}}$$

$$R_1 + 2R_2 = 36.075 \quad \text{--- (1)}$$

$$t_W \Rightarrow \frac{t_H}{T} \times 100 \Rightarrow \frac{R_1 + R_2}{R_1 + 2R_2} \times 100$$

$$0.8 = \frac{R_1 + R_2}{R_1 + 2R_2} \quad \text{--- (2)} \quad R_1 = 36.075 - 2R_2$$

$$0.8 = \frac{36.075 - R_2}{36.075}$$

$$R_1 = 21.645$$

$$R_2 = 7.215$$

$S\bar{H}/L\bar{D}$  is low  $\rightarrow$  asynchronous

$S\bar{H}/L\bar{D}$  is high  $\rightarrow$  synchronous (rising edge)

6. What is the state of the register in figure below after each clock pulse if it starts in the 101001111000 state? [10]



$$D_0 \dots D_{11} = 101001111000$$

$$\text{clock pulse } 1 = 0$$

$$\text{clock pulse } 2 = 0$$

$$\text{clock pulse } 3 = 0$$

$$\text{clock pulse } 4 = 1$$

$$\text{clock pulse } 5 = 1$$

$$\text{clock pulse } 6 = 1$$

$$\text{clock pulse } 7 = 1$$

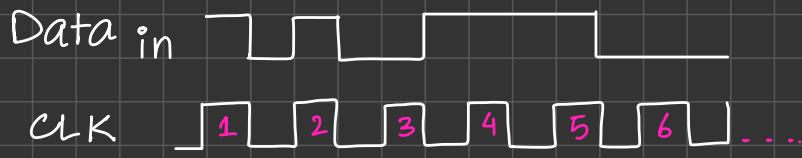
$$\text{clock pulse } 8 = 0$$

$$\text{clock pulse } 9 = 0$$

$$\text{clock pulse } 10 = 1$$

$$\text{clock pulse } 11 = 0$$

$$\text{clock pulse } 12 = 1$$



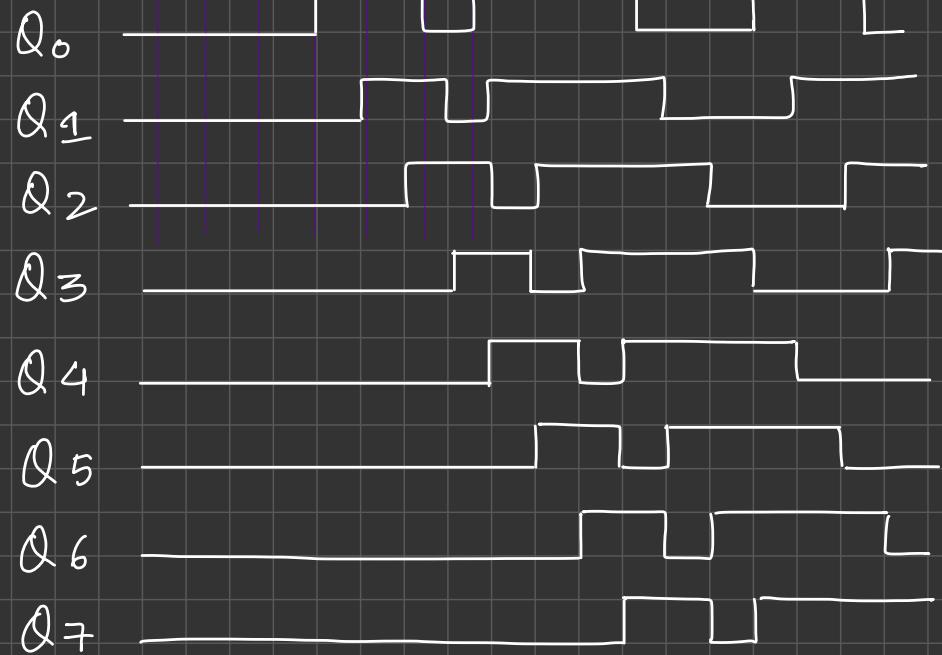
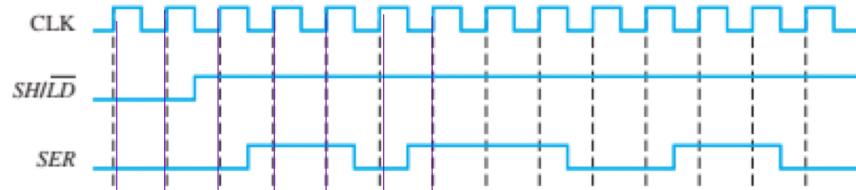
$$D_0 \dots D_{11} = 000111100101$$

output

↑  
first

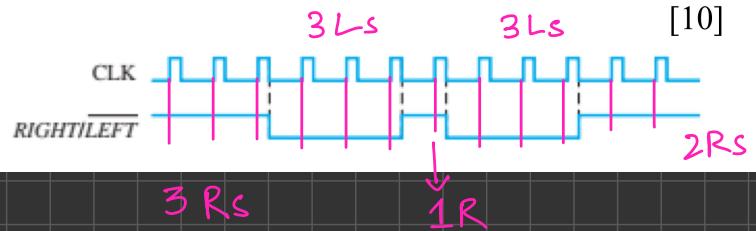
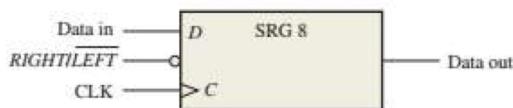
↑  
last

8. Develop the Q0 through Q7 outputs for a 8-bit Serial In Parallel Out shift register with the input waveforms shown in figure below. Here A and B are ANDed and used for Serial In to register. [10]



Each time  $Q$  is shifted by 1 pulse.

9. For the 8-bit bidirectional register in figure below, determine the state of the register after each clock pulse for the *RIGHT/LEFT* control waveform given. A *HIGH* on this input enables a shift to the right, and a *LOW* enables a shift to the left. Assume that the register is initially storing the decimal number seventy-six in binary, with the right-most position being the *LSB*. There is a *LOW* on the data-input line. [10]



$$76 = 01001100$$

(R) First 3 pulse : 00001001

(L) Next 3 pulse : 01001000

(R) Next 1 pulse : 00100100

(L) Next 3 pulse : 00100000

(R) Next 2 pulse : 00001000