Digital Logic Design

(EL-1005)

LABORATORY MANUAL

Spring 2022

LAB 04

Advance Logic Gate and Boolean Algebra

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MARKS AWARDED: /02

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LAB TASKS

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Exercise # 01 Implement the circuit for XOR Logic circuit using 74LS86 on Trainer

Exercise # 02 Implement the circuit for XNOR Logic circuit using Basic Gates (AND-OR-NOT) on Trainer

Exercise # 03 Implement the circuit for AND – OR and NOT Logic circuit using universal Gates (NAND or NOR Gates only) on Trainer.

Exercise # 04 Implement Even Parity and Odd Parity on Trainer.

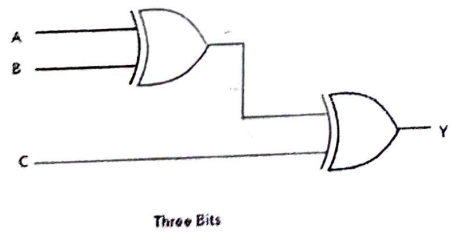
Parity Generator and Checker

A Parity Generator is a combinational logic circuit that generates the parity bit in the transmitter. On the other hand, a circuit that checks the parity in the receiver is called Parity Checker. A combined circuit or device of parity generators and parity checkers are commonly used in digital systems to detect the single bit errors in the transmitted data.

Even Parity and Odd Parity

The sum of the data bits and parity bits can be even or odd. In even parity, the added parity bit will make the total number of 1s an even number, whereas in odd parity, the added parity bit will make the total number of 1s an odd number.

The basic principle involved in the implementation of parity circuits is that sum of odd number of 1s is always 1 and sum of even number of 1s is always 0. Such error detecting and correction can be implemented by using Ex-OR gates (since Ex-OR gate produce zero output when there are even number of inputs).



Three Bits

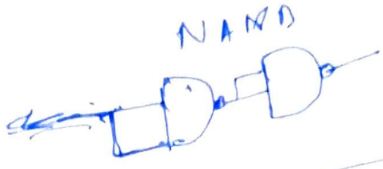
3-bit message			Even parity bit generator (P)
A	B	C	Y
0	0	0	0
0	0	1	1
0	1	0	1
0	1	1	0
1	0	0	1
1	0	1	0
1	1	0	0
1	1	1	1

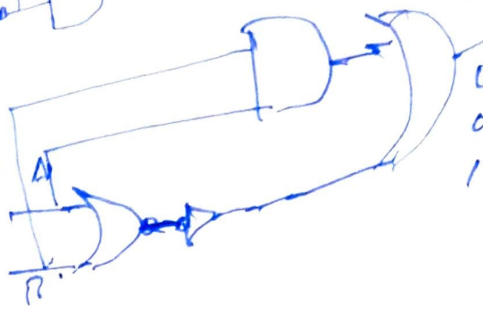
Even Parity Generator

Let us assume that a 3-bit message is to be transmitted with an even parity bit. Let the three inputs A, B and C are applied to the circuit and output bit is the parity bit P. The total number of 1s must be even, to generate the even parity bit P.

The figure shows the truth table of even parity generator in which 1 is placed as parity bit in order to make all 1s as even when the number of 1s in the truth table is odd.

00	1
01	0
10	0
11	1





A B

A	B	OR	NOR
0	0	0	1
0	1	1	0
1	0	1	0
1	1	1	0

XNOR

A B

A	B	AND
0	0	0
0	1	0
1	0	0
1	1	1

1	0	1
0	0	0
0	0	0
0	1	1

OR

A	B	C	A·B	NOT	C	
0	0	0	0	1	0	0
0	0	1	0	1	1	1
0	1	0	0	1	0	0
0	1	1	0	1	1	1
1	0	0	0	1	0	0
1	0	1	0	1	1	0
1	1	0	1	0	0	0
1	1	1	1	0	1	1

AND

NOT