Program	B. Tech CSE				
Year	II	Semester	IV		
Course Name	Computer Organization & Architecture				
Code	NCS4404				
Course Type	PCC	L	T	P	Credit
Pre-Requisite	Knowledge of Digital Logic Design	3	1	0	4
Course Objectives	1. To Study of the basic structure and operation of a digital computer system. 2. To understand how computer are constructed by a set of functional units. 3. Ability to analyse memory hierarchy and its impact on computer cost/performance. 4. Analyzing fundamental issues in architecture design and their impact on application performance.				
Course Outcomes					
CO1	Identify the basic structure and function unit of a digital computer.				
CO2	Understanding and analyze the effect of addressing modes and instructions				
CO3	Understanding Control Unit and ALU				
CO4	Understanding Interrupts and I/O				

Module	Course Contents	Contact Hrs.	Mapped CO
1	**Computer Evolution & Arithmetic** A Brief History of computers: Von Neumann Architecture, Hardware Architecture, Computer Components, Interconnection Structures, Bus Interconnection, Register Transfer Language, Bus and Memory Transfers, Bus Architecture, Bus Arbitration Techniques, Arithmetic Logic, Shift Micro operation, Arithmetic Logic Shift Unit, Arithmetic Algorithms (Addition, subtraction, Booth Multiplication, Division).	30 Hours	CO1
2	**Control Unit** Control Design: Hardwired & Micro Programmed, Performing of arithmetic or logical operations, Multiple Bus organization, Hardwired Control, Micro programmed control, Microinstruction, Micro program sequencing, Wide-Branch addressing, Microinstruction with Next-address field, Prefetching, Microinstruction, Pipeline control: Instruction pipelines, Pipeline performance.	30 Hours	CO2
3	**Processor Organization and Input-Output Organization** Processor Design: General register organization, Stack organization, Addressing mode, Instruction format, Data transfer & manipulations, Program Control, Reduced Instruction Set, Computer Memory Organization: Basic concept and hierarchy, semiconductor RAM memories,2D&2 1/2D memory organization, ROM memories, Cache memories, Concept and design issues & performance, Address mapping and replacement, Auxiliary memories: Magnetic disk, Magnetic tape and optical disks, Virtual memory, Concept implementation.	30 Hours	CO3

4	**Interrupts** Interrupt hardware, Types of interrupts and exceptions, Modes of Data Transfer: Programmed I/O, Interrupt initiated I/O, Direct Memory Access: I/O channels and processors, Serial Communication: Synchronous & asynchronous communication, Standard communication interfaces	30 Hours	CO4

Suggested Readings

1. Patterson, "Computer Organization and Design", Elsevier Publication.
2. Vravice, Hmacher & Zaky,"Computer Organization", TMH.
3. Moris Mano,"Computer System Architecture", PHI.
4. John P Hays,"Computer Organization", McGraw Hill.
5. Tannenbaum, "Structured Computer Organization", PHI.
6. P Pal Chaudhry," Computer Organization & Design", PHI.

Online Resources

1. https://nptel.ac.in/courses/106102062
2. https://archive.nptel.ac.in/courses/106/105/106105163/

Course Articulation Matrix

PO-PSO	PO 1	PO 2	PO 3	PO 4	PO 5	PO 6	PO 7	PO 8	PO 9	PO10	PO 11	PO 12	PSO 1	PSO 2
CO1	2	1												
CO2	2	1	1	1										
CO3	2	1	1	1										
CO4	2	1	1	1										