

COA TUTORIAL

Q1: A program runs on a 3 GHz processor with an IPC of 1.5. The program has 5 billion instructions. What is the execution time?

Answer:

Execution Time = Total Instructions / (IPC × Clock Speed)

Execution Time = $5 \times 10^9 / (1.5 \times 3 \times 10^9) = 5 / 4.5 \approx 1.11$ seconds

Q2: A system has a single-threaded portion that takes 30% of the time. If the parallel portion is speed up by a factor of 5, what is the effective speedup?

Answer:

$$1 / (1 - P + P / N)$$

$$\text{Speedup} = 1 / (0.3 + 0.7 / 5) = 1 / (0.3 + 0.14) = 1 / 0.44 \approx 2.27$$

Q3: A parallel program has 85% of its workload that can be parallelized. The parallel portion is executed on 8 cores. However, there is a 10% overhead for communication between cores. What is the effective speedup of the program?

Answer:

$$\text{Effective Parallel Portion} = 0.85 \times (1 - 0.10) = 0.765$$

$$\text{Speedup} = 1 / ((1 - 0.765) + 0.765 / 8) = 1 / (0.235 + 0.095625) = 1 / 0.330625 \approx 3.02$$

Q4: A CPU has a base CPI of 1.5 when all memory accesses hit in the cache. However, there is a 10% cache miss rate, and each cache miss incurs an additional 100 clock cycles. If 25% of the instructions involve memory access, what is the effective CPI of the CPU?

Answer:

$$\text{Effective CPI} = \text{Base CPI} + (\text{Miss Rate} \times \text{Miss Penalty} \times \text{Memory Access Percentage})$$

$$\text{Effective CPI} = 1.5 + (0.10 \times 100 \times 0.25) = 1.5 + 2.5 = 4$$

Q5: Memory operations currently take 30% of execution time. . A new widget called a “cache” speeds up 80% of memory operations by a factor of 4 . A second new widget called a “L2 cache” speeds up 1/2 the remaining 20% by a factor of 2. What is the total speed up?

Answer:

Initially: Not memory = 0.7

L1: $0.3 * 0.8 = 0.24$

L2: $(0.3 * 0.2) / 2 = 0.03$

no boost = 0.03

Total = 1

Later:

Not Memory = 0.7

L1: $0.24 / 4 = 0.06$

L2 : $0.03 / 2 = 0.015$

No boost = 0.03

Total = 0.805

Speedup = $1 / 0.805 = 1.24$

Q6: A processor can execute 2 threads in parallel, each with a latency of 50 milliseconds. Due to overhead, the execution time increases by 20% when both threads are executed in parallel. Calculate the latency and throughput for both serial and parallel execution modes.

Answer:

- **Serial Execution:**
 - Latency = $2 \times 50 \text{ ms} = 100 \text{ ms}$
 - Throughput = $2 / 100 \text{ ms} = 0.02 \text{ tasks / ms}$
- **Parallel Execution:**
 - Latency = $50 \times 1.20 = 60 \text{ ms}$
 - Throughput = $2 / 60 \text{ ms} \approx 0.033 \text{ tasks/ms}$

Q7: A processor can operate at 2 GHz consuming 100 watts or at 1 GHz consuming 50 watts. If a program takes 5 seconds to complete at 2 GHz, how much energy is saved by running the program at 1 GHz?

Answer:

At 2 GHz:

Time = 5 s, Power = 100 W, Energy = $100 \times 5 = 500 \text{ J}$ At 1 GHz:

Program time = 10 seconds (because speed is halved)

Energy = $50 \times 10 = 500$ joules

No energy is saved; both scenarios use the same energy.

Q8: A new compiler optimization reduces the instruction count of a program by 25% but increases the CPI by 10%. If the original program has an IPC of 2 on a 3 GHz processor, calculate the new execution time after optimization, given the original execution time was 4 seconds.

Answer:

Original Execution Time:

$$\text{Instructions} = 2 \times 3 \times 10^9 \times 4 = 24 \times 10^9 \text{ (#insn} = \text{IPC} \times f \times \text{ET})$$

$$\text{CPI} = 1 / 2 = 0.5$$

$$\text{New Instruction Count} = 0.75 \times 24 \times 10^9 = 18 \times 10^9$$

$$\text{New CPI} = 1.1 \times 0.5 = 0.55$$

New Execution Time:

$$\text{Execution Time} = 18 \times 10^9 / (0.55 \times 3 \times 10^9) \approx 10.91 \text{ seconds}$$

Q9: A processor consumes 60W of dynamic power at 2.2 GHz and 1.3V. If the frequency is reduced to 1.8 GHz and the voltage is scaled down to 1.1V(also known as DVFS: dynamic voltage frequency scaling), what will be the new dynamic power?

Answer:

First, calculate the reduction due to frequency:

$$P_{\text{new}} = 60\text{W} \times (1.8 / 2.2) \approx 49.09\text{W}$$

Now, account for voltage scaling:

$$P_{\text{new}} = 49.09\text{W} \times (1.1 / 1.3)^2 \approx 49.09\text{W} \times 0.716 = 35.15\text{W}$$

Q10: A processor has a dynamic power consumption of 75W at 2.5 GHz and 1.2V. If a design constraint requires that voltage and frequency be inversely proportional to maintain stability, what is the dynamic power if the voltage is reduced to 1.0V?

Answer:

Determine the new frequency:

$$f_{\text{new}} = (1.2 / 1.0) \times 2.5 \text{ GHz} = 3.0 \text{ GHz}$$

New power:

$$P_{\text{new}} = 75\text{W} \times (3.0 / 2.5) \times (1.0 / 1.2)^2 = 75\text{W} \times 1.2 \times 0.6944 \approx 62.5\text{W}$$