Indian Institute of Technology Bhubaneswar

School of Electrical and Computer Sciences
Midsem (Spring) Examination – 2024-25

Subject Name: ACA
Subject Code: CS6L047 Level: PG
Duration: 2 hours Full Marks: 30

Instructions: All questions are compulsory. Solve all the sub questions of a single question all together in one place of the answer sheet.

Q1. Consider a pipelined processor that uses branch prediction to improve performance. Analyze and compare the behavior of a dynamic two-bit branch predictor and a static branch predictor in two different scenarios:

(i) [5 marks] Describe a case where the two-bit predictor performs better than the static predictor.

(ii) [5 marks] Describe a case where the static predictor performs better than the two-bit predictor.

For each case:

- Provide a simple C or Assembly code snippet that illustrates the branch behavior.
- Show a table with iteration-by-iteration prediction outcomes and updates.
- Calculate and compare the misprediction rates for both predictors.
- Justify why one predictor outperforms the other in each scenario.

Q2. Loop: LD F0,0(R1) ;F0=vector element
ADDD F4,F0,F2 ;add scalar from F2
SD F4, 0(R1) ;store result
SUBI R1,R1,8. ;decrement pointer 8B (DW)
BNEZ R1,Loop ;branch if R1!=zero

Instruction Producing Result	Instruction Using Result	Latency in Clock cycles
FP ALU op	Another FP ALU op	5
FP ALU op	Store Double	1
Load Double	FP ALU op	2
Load Double	Store Double	0

The last column in the table shows the number of intervening clock cycles needed to avoid a stall. The latency of a floating-point load to a store is 0 because the result of the load can be bypassed without stalling the store.

Additional assumptions:

- Integer load latency = 1 cycle
- Integer ALU operation latency = 0 cycles (includes ALU-to-branch)
- Branch is handled via a branch delay slot

Answer the following:

(i) [2 marks] Identify all data dependencies and data hazards in the loop. For each dependency, specify:

- The instruction producing the result
- The instruction using the result
- The register involved in the dependency

(ii) [3 marks] Baseline Performance: Calculate the total number of cycles required per loop iteration without any ILP optimization.

(iii) [5 marks] Calculate the total number of cycles required per loop iteration with code scheduling and loop unrolling (unrolling factor = 3)

(iv) [5 marks] Assume the loop runs on a 2-issue superscalar processor with:

- One integer unit (handles integer ALU and load/store operations)
- One floating-point unit (handles FP operations)

Calculate the number of cycles per iteration with code scheduling optimization. Do not apply loop unrolling.

Q3. Amdahl's Law vs Gustafson's Law

(a) [2 marks] Explain the key difference between Amdahl's Law and Gustafson's Law in terms of how they model speedup and scalability. Use mathematical expressions to support your explanation.

(b) [3 marks] Consider a program where 90% of the workload is parallelizable. Calculate the speedup using both Amdahl's Law and Gustafson's Law for 10 processors. Explain your results.